SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

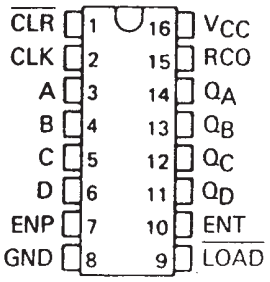
SDLS060 – OCTOBER 1976 – REVISED MARCH 1988

'160,'161,'LS160A,'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162,'163,'LS162A,'LS163A,'S162,'S163 . . . FULLY SYNCHRONOUS COUNTERS

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Load Control Line**
- **Diode-Clamped Inputs**

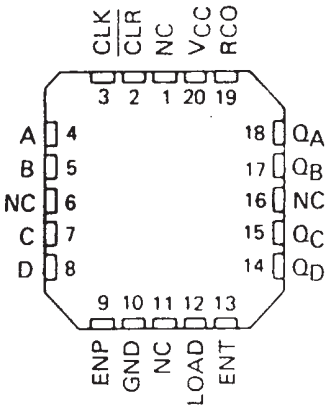
TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS162A thru 'LS163A	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

SERIES 54', 54LS' 54S' . . . J OR W PACKAGE
SERIES 74' . . . N PACKAGE
SERIES 74LS', 74S' . . . D OR N PACKAGE
(TOP VIEW)



NC—No internal connection

SERIES 54LS', 54S' . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160,'162,'LS160A,'LS162A, and 'S162 are decade counters and the '161,'163,'LS161A,'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip-flops on the rising edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS160A thru 'LS163A or 'S162 or 'S163. The clear function for the '160, '161,'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162,'163,'LS162A,'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

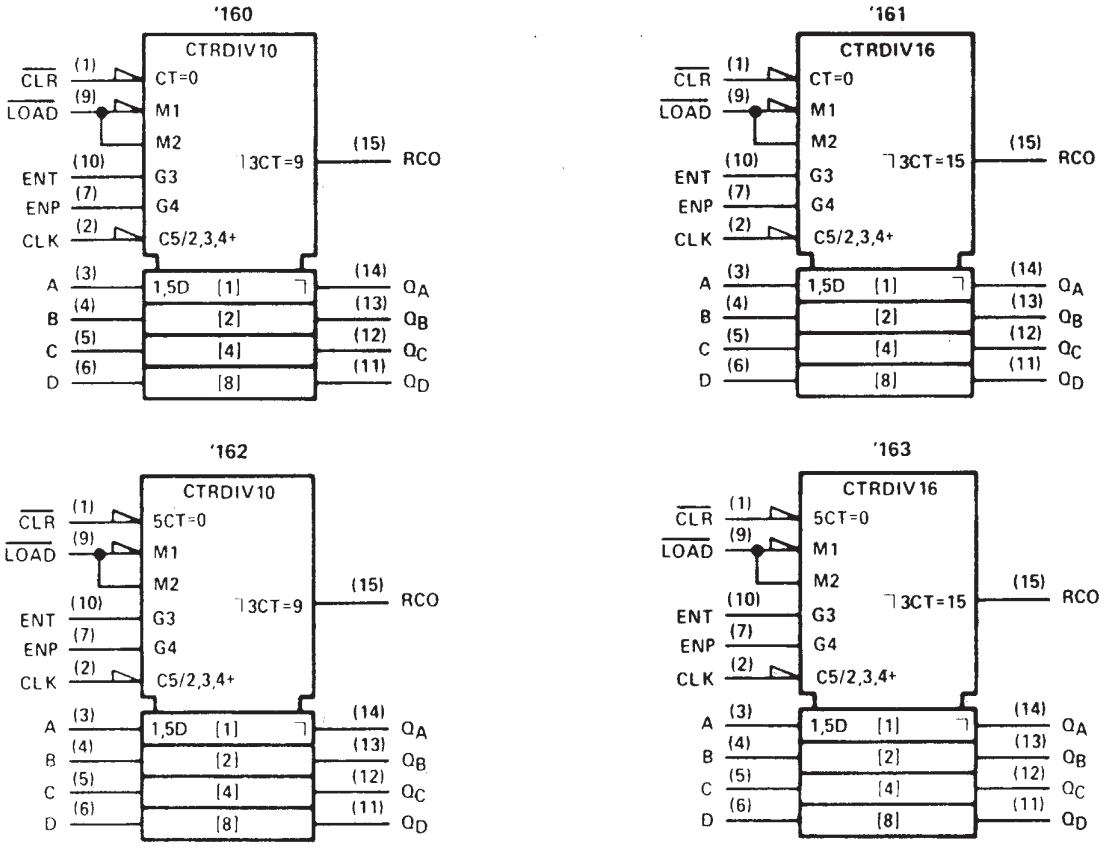
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 and 'S163 are allowed regardless of the level of the clock input.

'LS160A thru 'LS163A,'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

logic symbols†

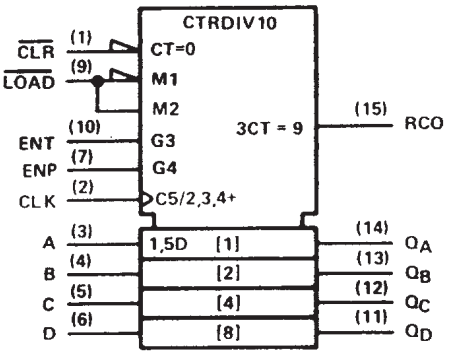


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

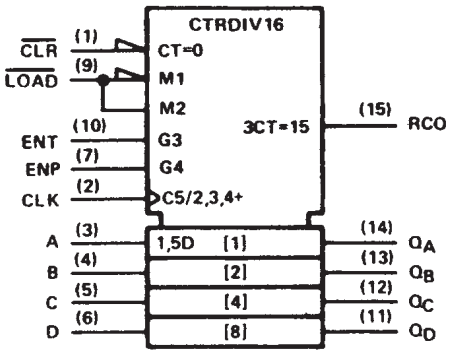
Pin numbers shown are for D, J, N, and W packages.

logic symbols (continued)†

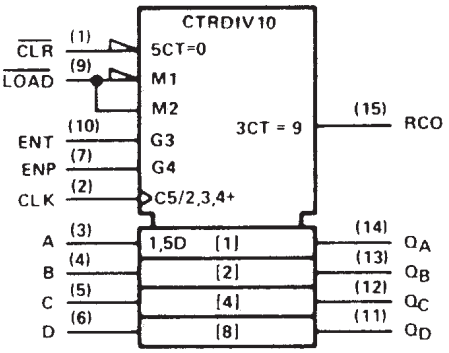
'LS160A



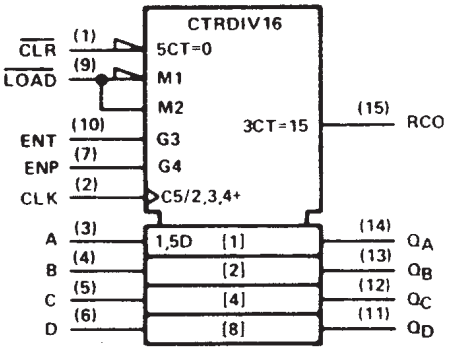
'LS161A



'LS162A, 'S162



'LS163A, 'S163



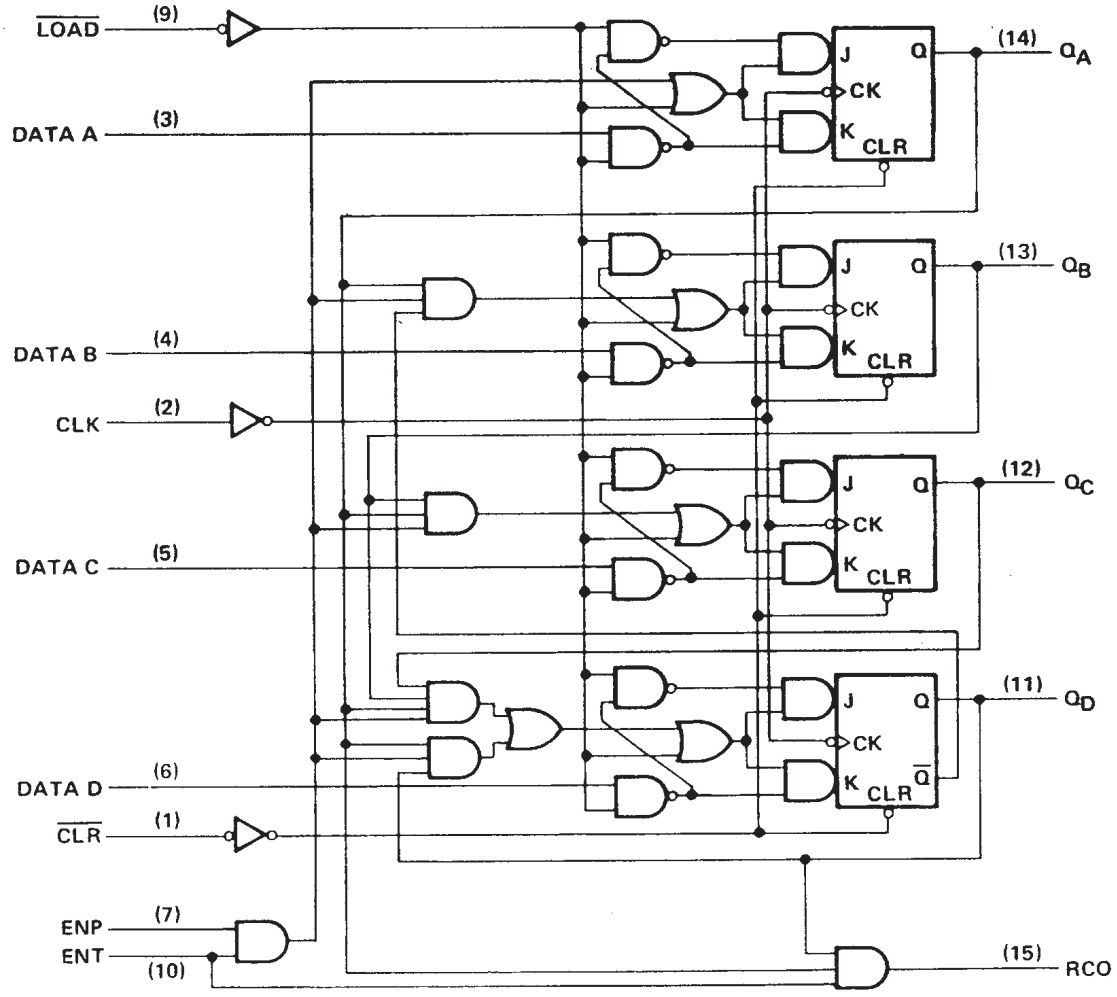
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.

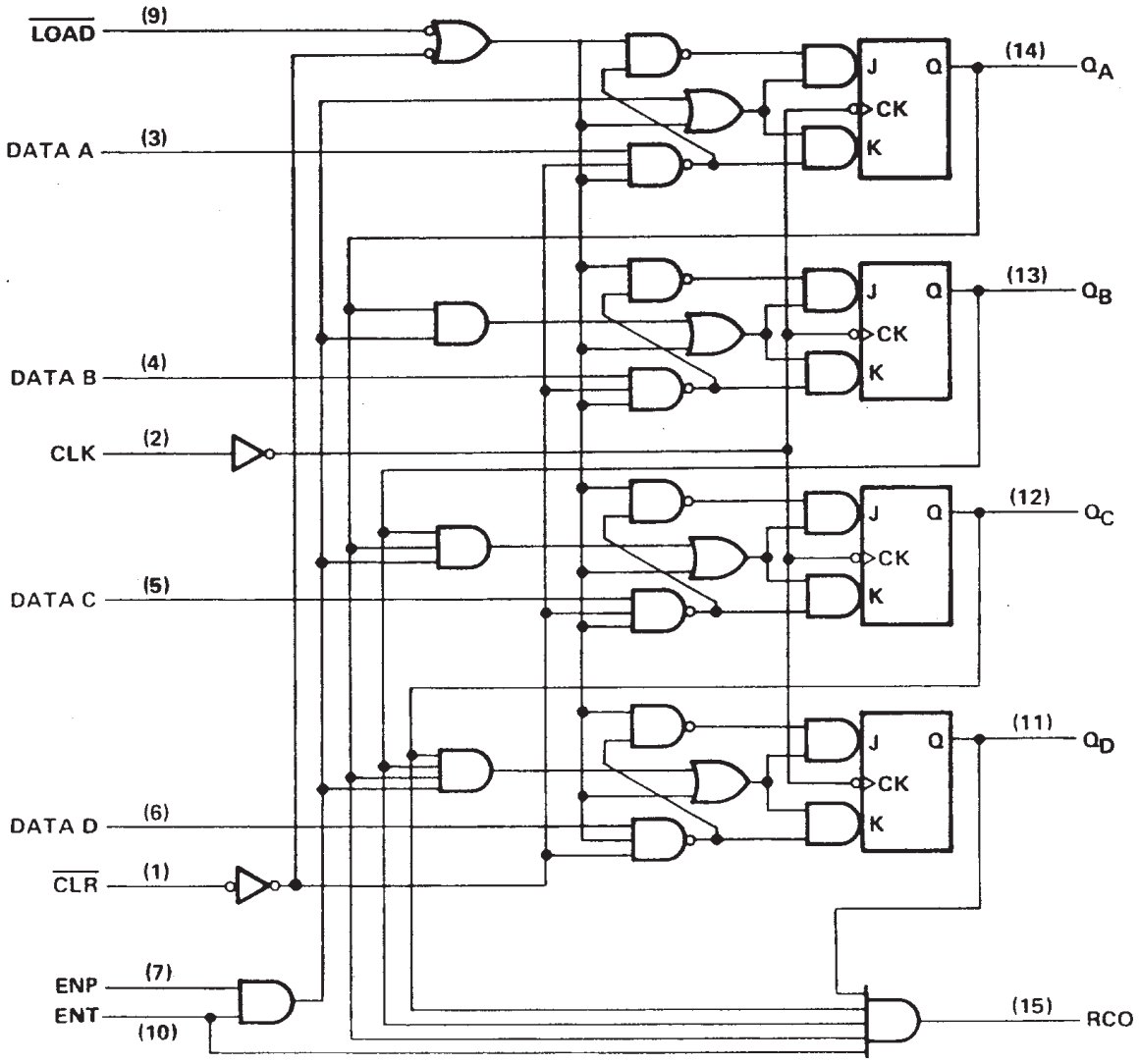


Pin numbers shown are for D, J, N, and W packages

logic diagram (positive logic)

SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.

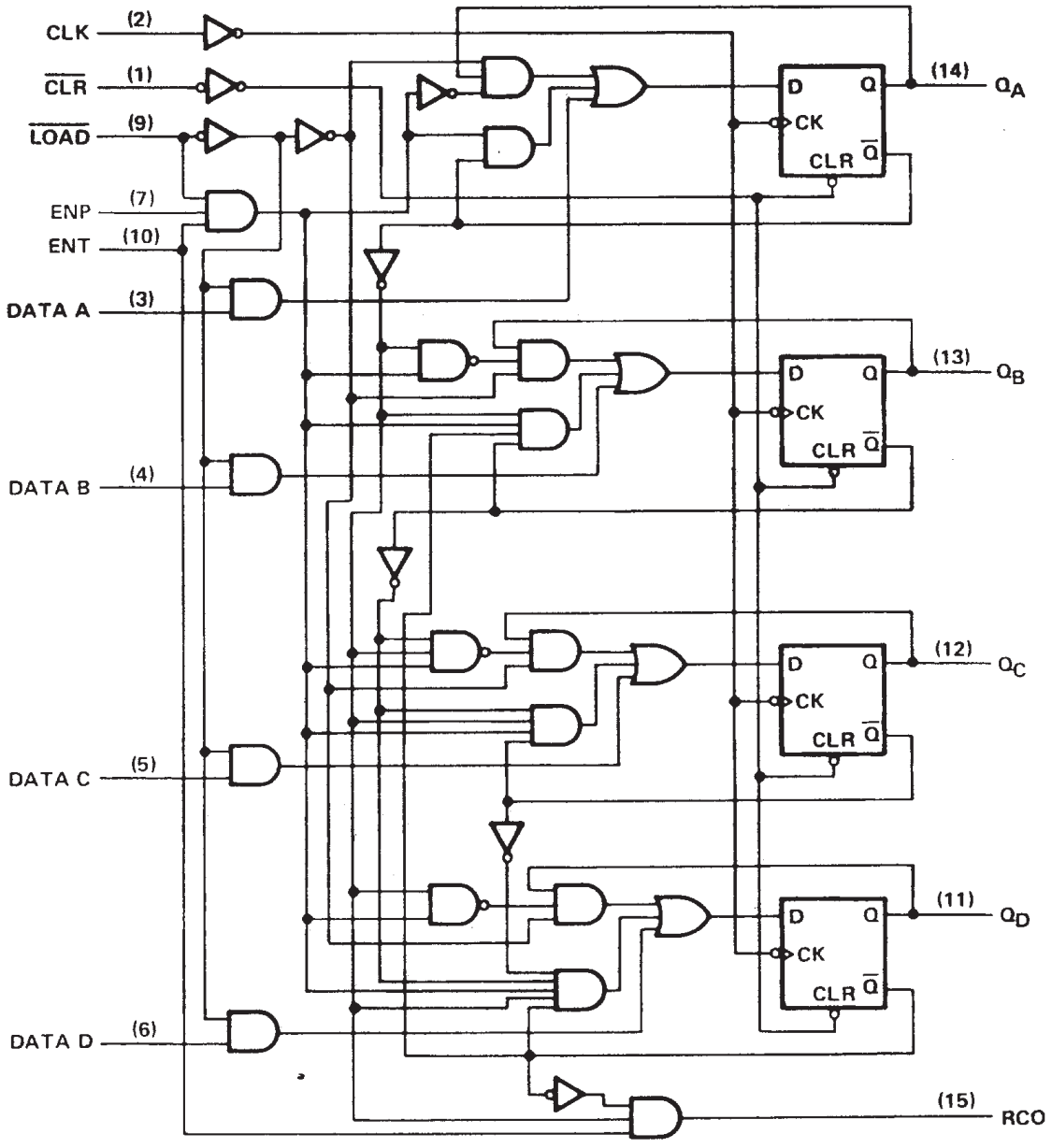


Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

SN54LS160A, SN74LS160A SYNCHRONOUS DECADE COUNTERS

SN54LS162A, SN74LS162A synchronous decade counters are similar; however the clear is synchronous as shown for the SN54LS163A, SN74LS163A binary counters at right.

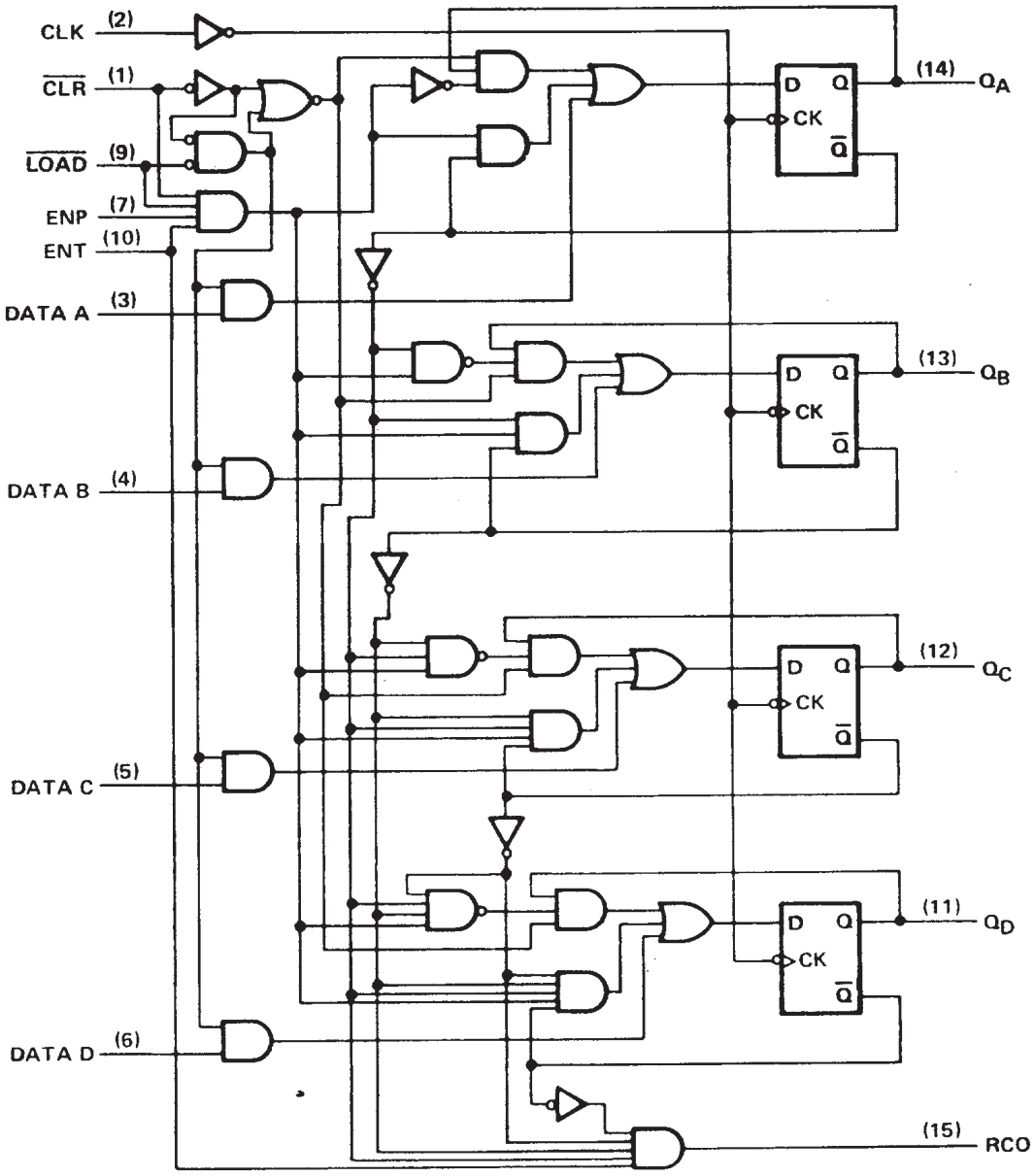


Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

SN54LS163A, SN74LS163A SYNCHRONOUS BINARY COUNTERS

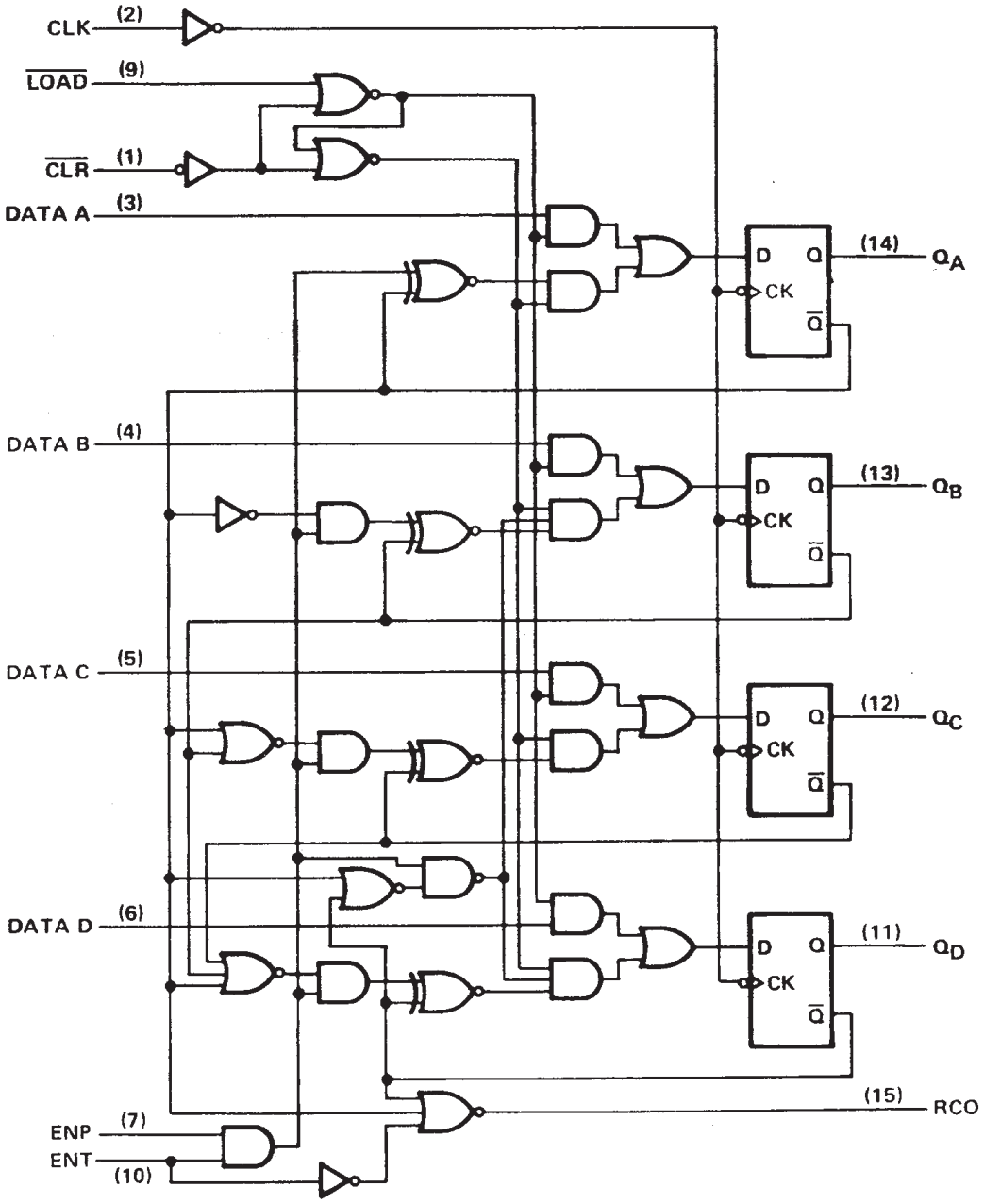
SN54LS161A, SN74LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54LS160A, SN74LS160A decade counters at left.



Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

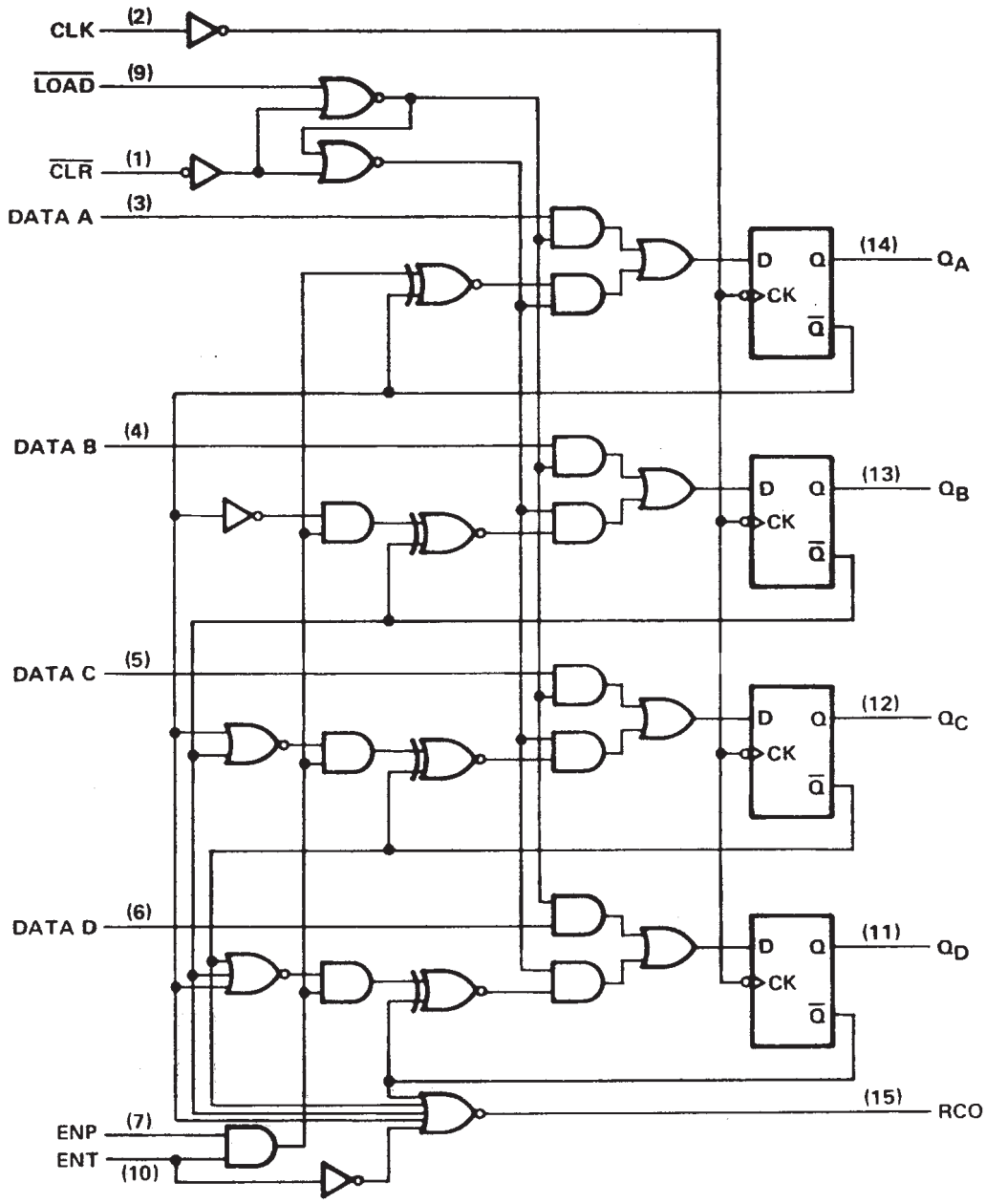
SN54S162, SN74S162 SYNCHRONOUS DECADE COUNTER



Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

SN54S163, SN74S163 SYNCHRONOUS DECADE COUNTER



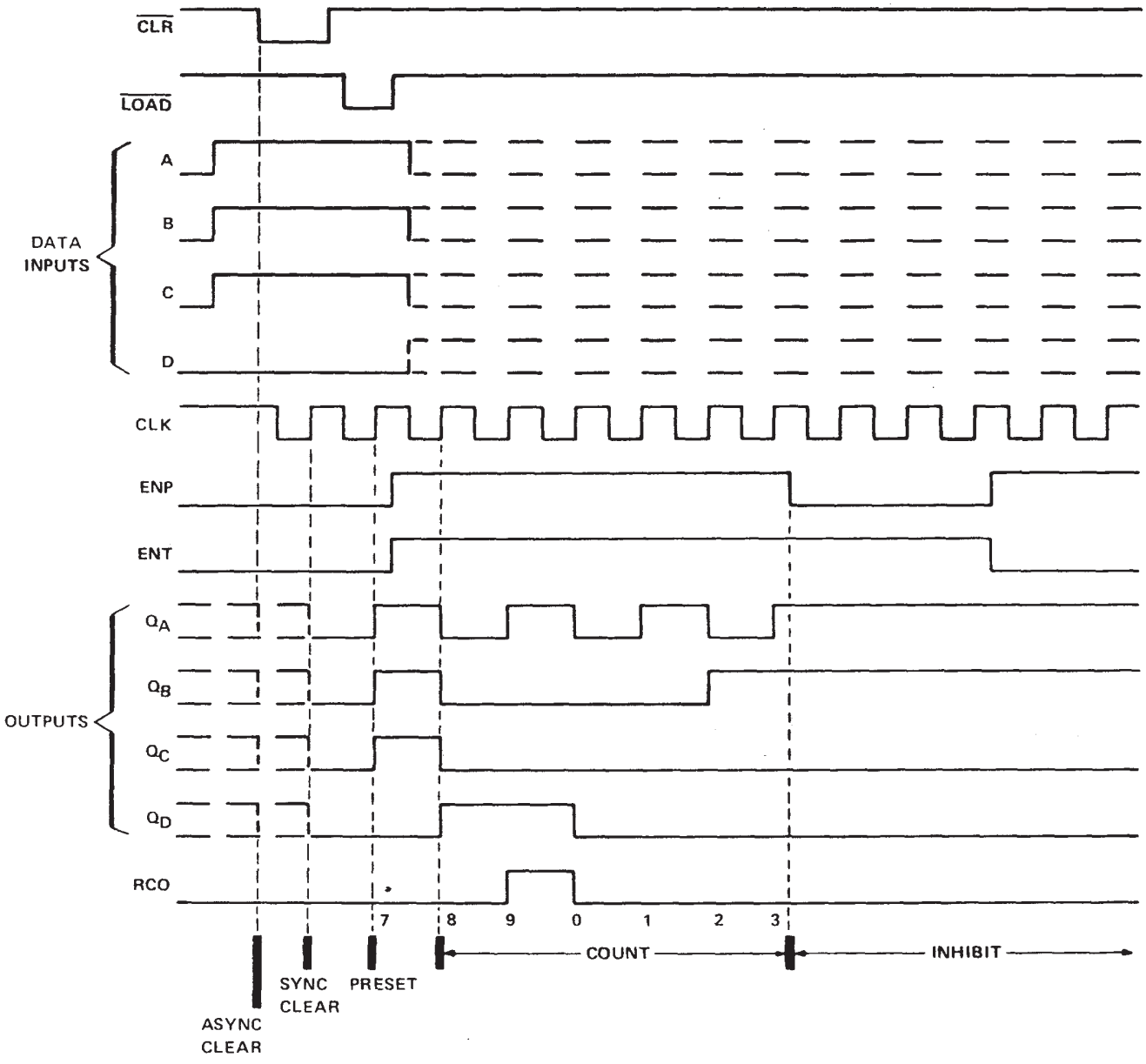
Pin numbers shown are for D, J, N, and W packages.

'160, '162, 'LS160A, 'LS162A, 'S162 DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('160 and 'LS160A are asynchronous; '162, 'LS162A, and 'S162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

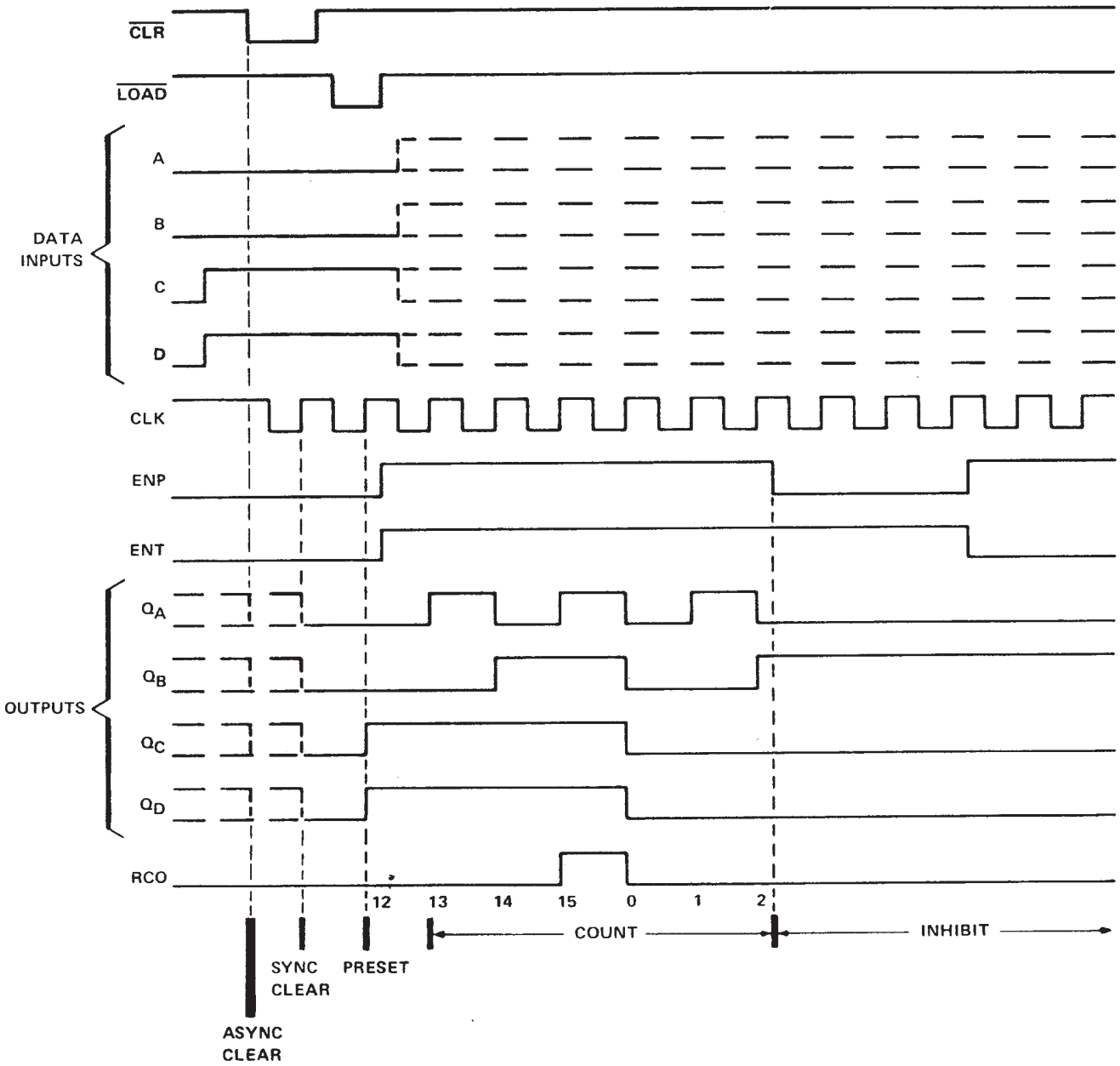


'161, 'LS161A, '163, 'LS163A, 'S163 BINARY COUNTERS

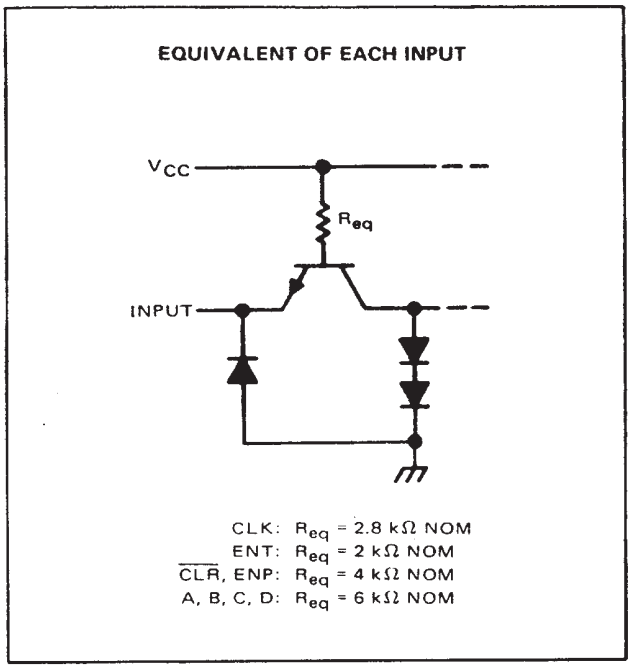
typical clear, preset, count, and inhibit sequences

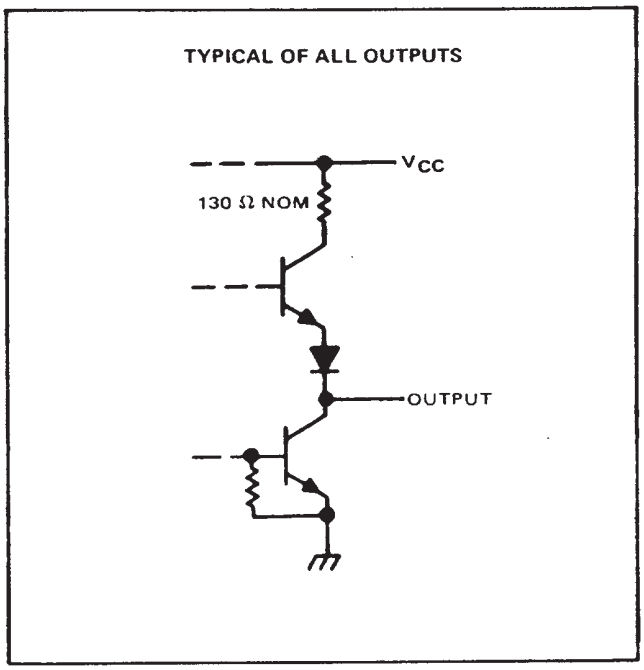
Illustrated below is the following sequence:

1. Clear outputs to zero ('161 and 'LS161A are asynchronous; '163, 'LS163A, and 'S163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

		SN54160, SN54161 SN54162, SN54163			SN74160, SN74161 SN74162, SN74163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{su} (see Figures 1 and 2)	Data inputs A, B, C, D	20			20			ns
	ENP	20			20			
	$\overline{LOAD}$	25			25			
	$\overline{CLR}$ †	20			20			
Hold time at any input, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

† This applies only for '162 and '163, which have synchronous clear inputs.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54160, SN54161 SN54162, SN54163			SN74160, SN74161 SN74162, SN74163			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = –12 mA			–1.5			–1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	CLK or ENT	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	CLK or ENT	V_{CC} = MAX, V_I = 0.4 V			–3.2			–3.2	mA
		Other inputs				–1.6			–1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	–20		–57	–18		–57	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = MAX, See Note 3		59	85		59	94	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		63	91		63	101	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

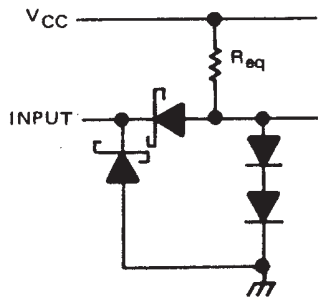
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 2 and Note 5	25	32		MHz
t_{PLH}	CLK	RCO			23	35	ns
t_{PHL}					23	35	
t_{PLH}	CLK (LOAD input high)	Any Q			13	20	ns
t_{PHL}					15	23	
t_{PLH}	CLK (LOAD input low)	Any Q			17	25	ns
t_{PHL}					19	29	
t_{PLH}	ENT	RCO			11	16	ns
t_{PHL}					11	16	
t_{PHL}	CLR	Any Q			26	38	ns

¶f_{max} = Maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 5: Propagation delay for clearing is measured from the clear input for the '160 and '161 or from the clock input transition for the '162 and '163.

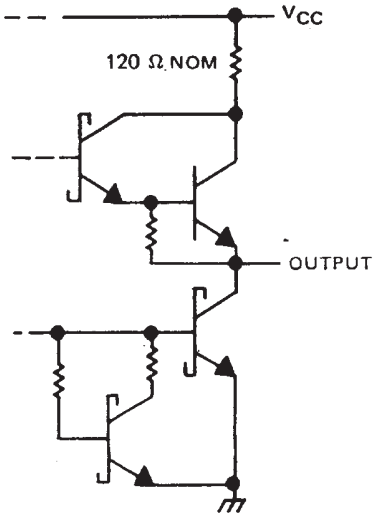
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Data: R_{eq} = 25 kΩ NOM
CLK, ENT, $\overline{LOAD}$: R_{eq} = 10 kΩ NOM
ENP: R_{eq} = 20 kΩ NOM
$\overline{CLR}$ ('LS160A, 'LS161A): R_{eq} = 20 kΩ NOM
$\overline{CLR}$ ('LS162A, 'LS163A): R_{eq} = 10 kΩ NOM

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 7) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS' Circuits . . . . . −55°C to 125°C
SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 7: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current				−400			−400	μA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		25	MHz
$t_{w(clock)}$	Width of clock pulse		25			25			ns
$t_{w(clear)}$	Width of clear pulse		20			20			ns
t_{su}	Setup time, (see Figures 1 and 2)	Data inputs A, B, C, D	20			20			ns
		ENP or ENT	20			20			
		$\overline{LOAD}$	20			20			
		$\overline{LOAD}$ inactive state	20			20			
		$\overline{CLR}$†	20			20			
		$\overline{CLR}$ inactive state	25			25			
t_h	Hold time at any input		3			3			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

† This applies only for 'LS162 and 'LS163, which have synchronous clear inputs.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage, Data or ENP	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
	$\overline{LOAD}$, CLK, or ENT					0.2			0.2	
	$\overline{CLR}$ ('LS160A, 'LS161A)					0.1			0.1	
	$\overline{CLR}$ ('LS162A, 'LS163A)					0.2			0.2	
I_{IH}	High-level input current, Data or ENP	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
	$\overline{LOAD}$, CLK, or ENT					40			40	
	$\overline{CLR}$ ('LS160A, 'LS161A)					20			20	
	$\overline{CLR}$ ('LS162A, 'LS163A)					40			40	
I_{IL}	Low-level input current, Data or ENP	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	$\overline{LOAD}$, CLK, or ENT					−0.8			−0.8	
	$\overline{CLR}$ ('LS160A, 'LS161A)					−0.4			−0.4	
	$\overline{CLR}$ ('LS162A, 'LS163A)					−0.8			−0.8	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX,	See Note 3		18	31		18	31	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX,	See Note 4		19	32		19	32	mA

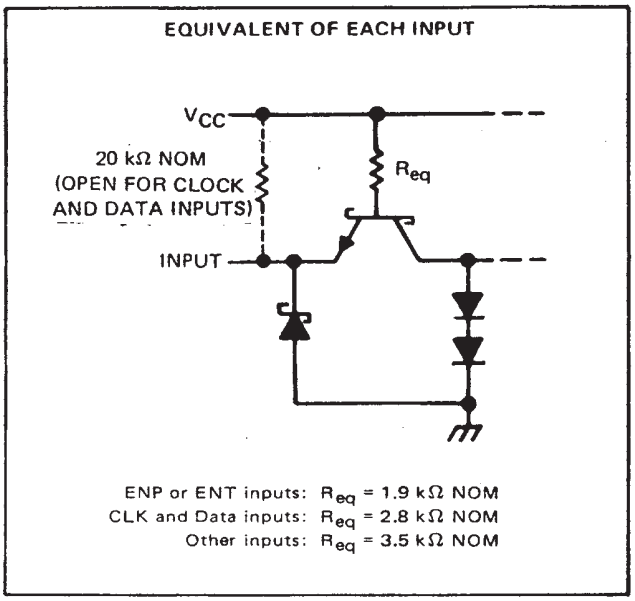
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

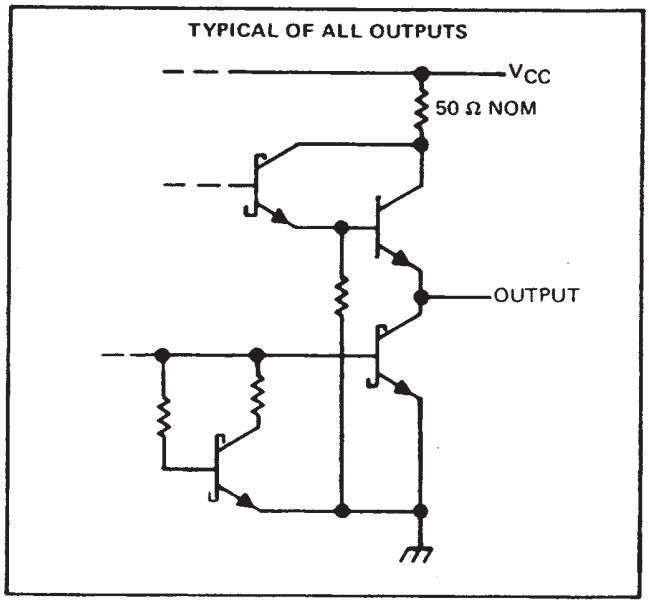
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See figures 1 and 2 and Note 8	25	32		MHz
t_{PLH}	CLK	RCO			20	35	ns
t_{PHL}					18	35	
t_{PLH}	CLK ($\overline{LOAD}$ input high)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	CLK ($\overline{LOAD}$ input low)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	ENT	RCO			9	14	ns
t_{PHL}					9	14	
t_{PHL}	$\overline{CLR}$	Any Q			20	28	ns

¶f_{max} = Maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.
NOTE 8: Propagation delay for clearing is measured from the clear input for the 'LS160A and 'LS161A or from the clock transition for the 'LS162A and 'LS163A.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54S162, SN54S163 (see Note 10) . . . . . −55°C to 125°C
SN74S162, SN74S163 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54S162, SN54S163			SN74S162, SN74S163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		40	0		40	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low)		10			10			ns
Width of clear pulse, $t_{w(clear)}$		10			10			ns
Setup time, t_{su} (see Figure 4)	Data inputs, A, B, C, D	4			4			ns
	ENP or ENT	12			12			
	$\overline{LOAD}$	14			14			
	$\overline{CLR}$	14			14			
	$\overline{LOAD}$ inactive-state	12			12			
	$\overline{CLR}$ inactive-state	12			12			
Release time, $t_{release}$ (see Figure 4)	ENP or ENT			4			4	ns
Hold time, t_h (see Figure 4)	Data inputs A, B, C, D	3			3			ns
	$\overline{LOAD}$	0			0			
	$\overline{CLR}$	0			0			
Operating free-air temperature, T_A (see Note 10)		55		125	0		70	C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.
10. An SN54S162 or SN54S163 in the W package operating at free air temperatures above 91°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54S162 SN54S163			SN74S162 SN74S163			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	CLK and data inputs	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
		Other inputs		−10		−200	−10		−200	
I_{IL}	Low-level input current	ENT	V_{CC} = MAX, V_I = 0.5 V			−4			−4	mA
		Other inputs				2			2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX		95	160		95	160	mA

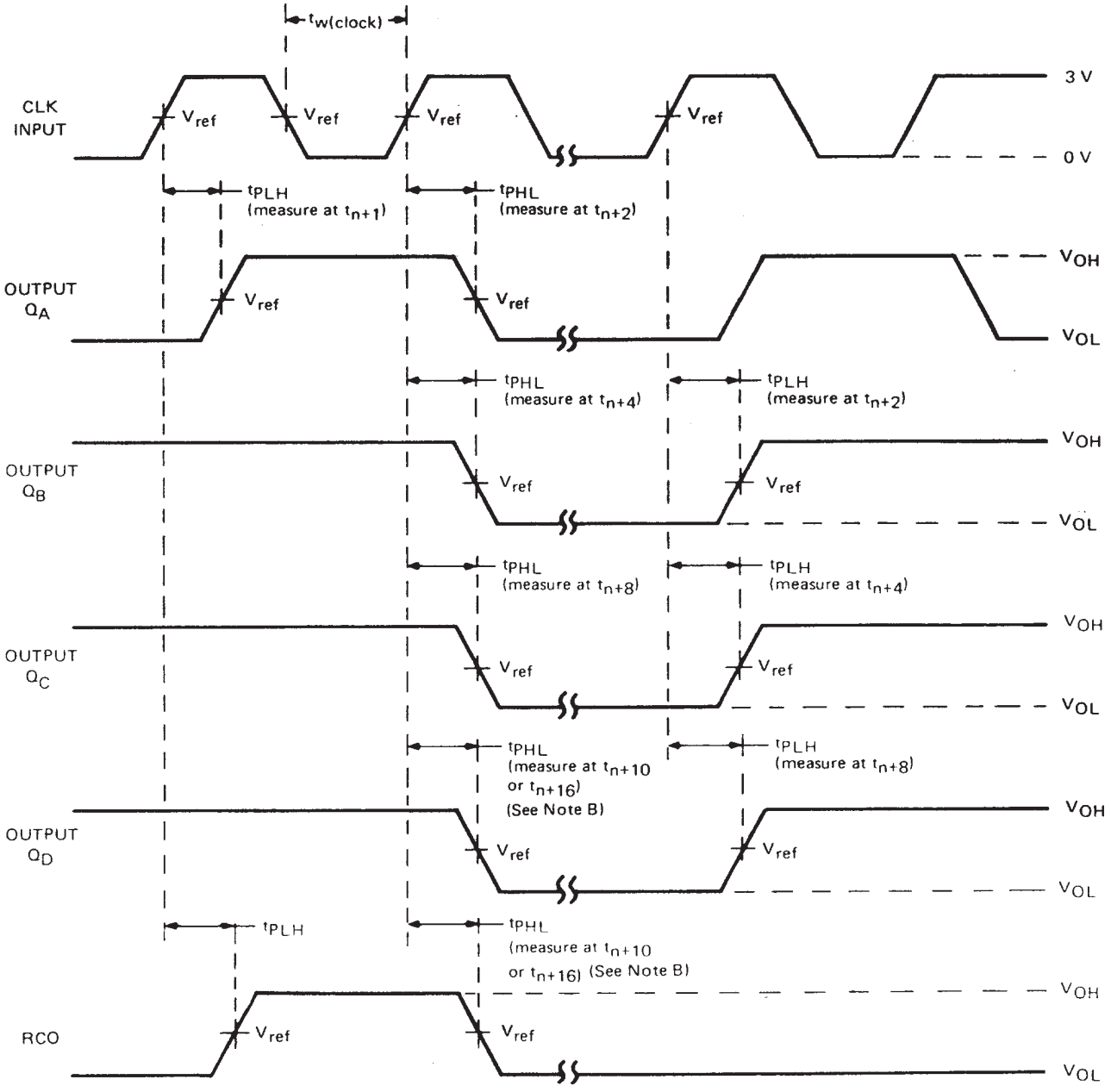
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Figures 1, 3, and 4	40	70		MHz
t_{PLH}	CLK	RCO			14	25	ns
t_{PHL}					17	25	
t_{PLH}	CLK	Any Q			8	15	ns
t_{PHL}					10	15	
t_{PLH}	ENT	RCO			10	15	ns
t_{PHL}					10	15	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low to high level output
t_{PHL} ≡ propagation delay time, high-to low level output

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

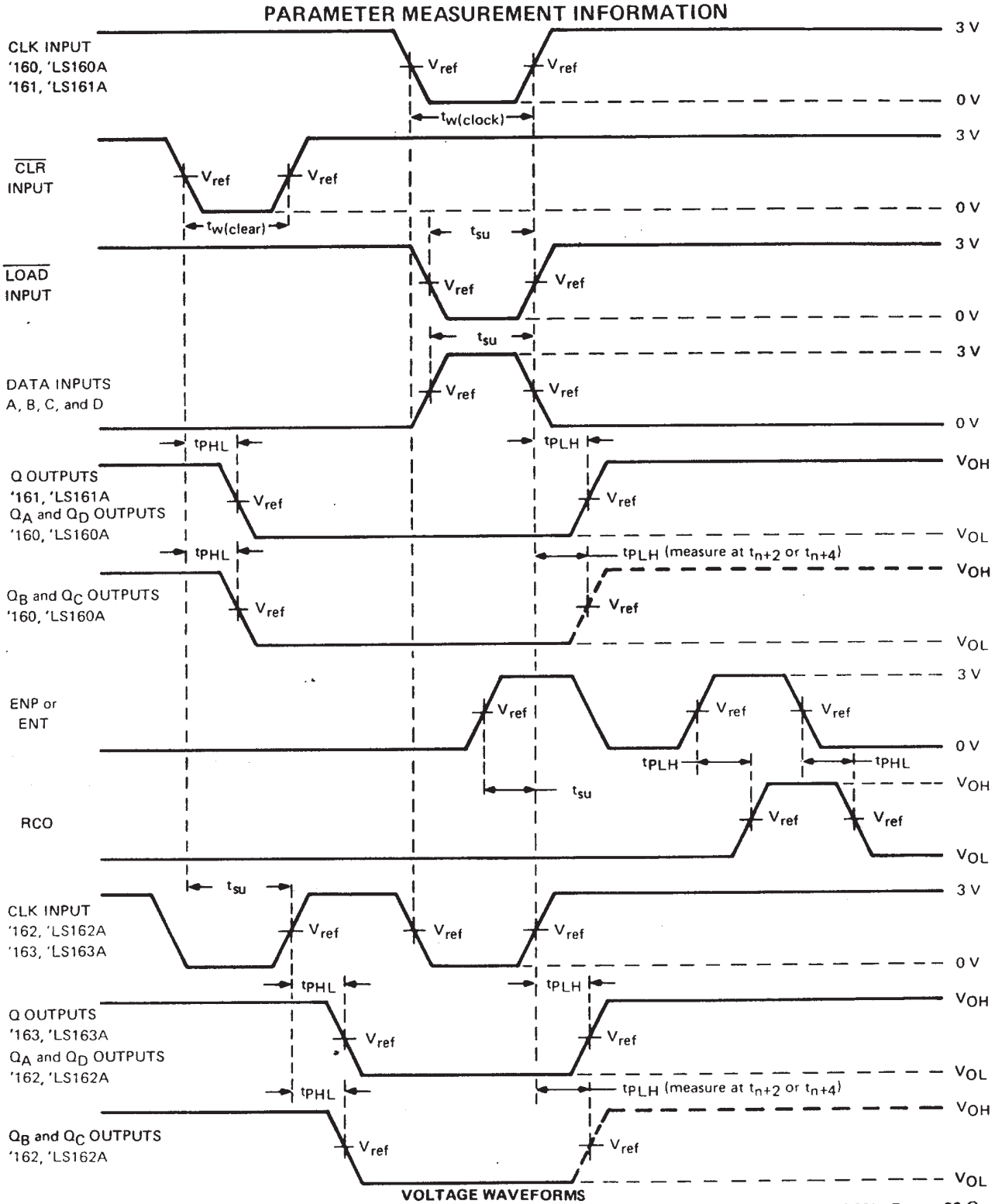
NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; for 'LS160A thru 'LS163A $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S162, 'S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for '160, '162, 'LS160A, 'LS162A, and 'S162, and at t_{n+16} for '161, '163, 'LS161A, 'LS163A, and 'S163, where t_n is the bit time when all outputs are low.

C. For '160 thru '163, 'S162, and 'S163, V_{ref} = 1.5 V; for 'LS160A thru 'LS163A, V_{ref} = 1.3 V.

FIGURE 1–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

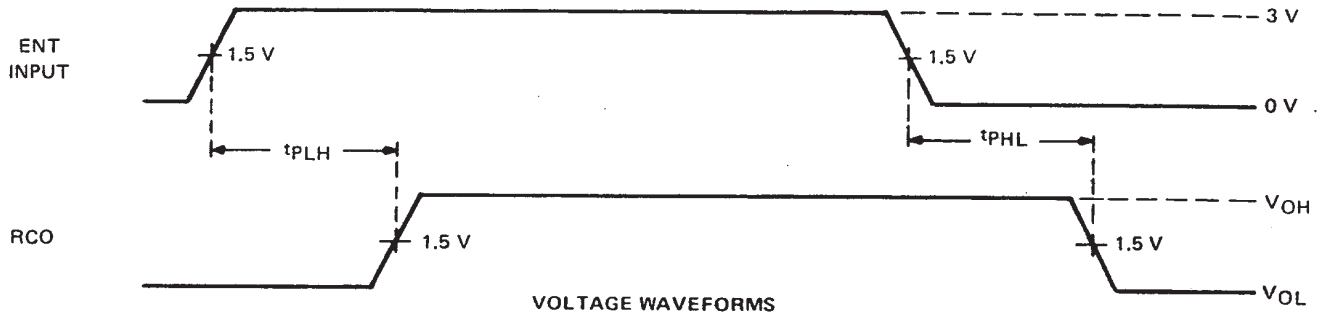
NOTES: A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; and for 'LS160A thru 'LS163A, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

B. Enable P and enable T setup times are measured at t_{n+0}.

C. For '160 thru '163, $V_{ref} = 1.5$ V; for 'LS160A thru 'LS163A, $V_{ref} = 1.3$ V.

FIGURE 2–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

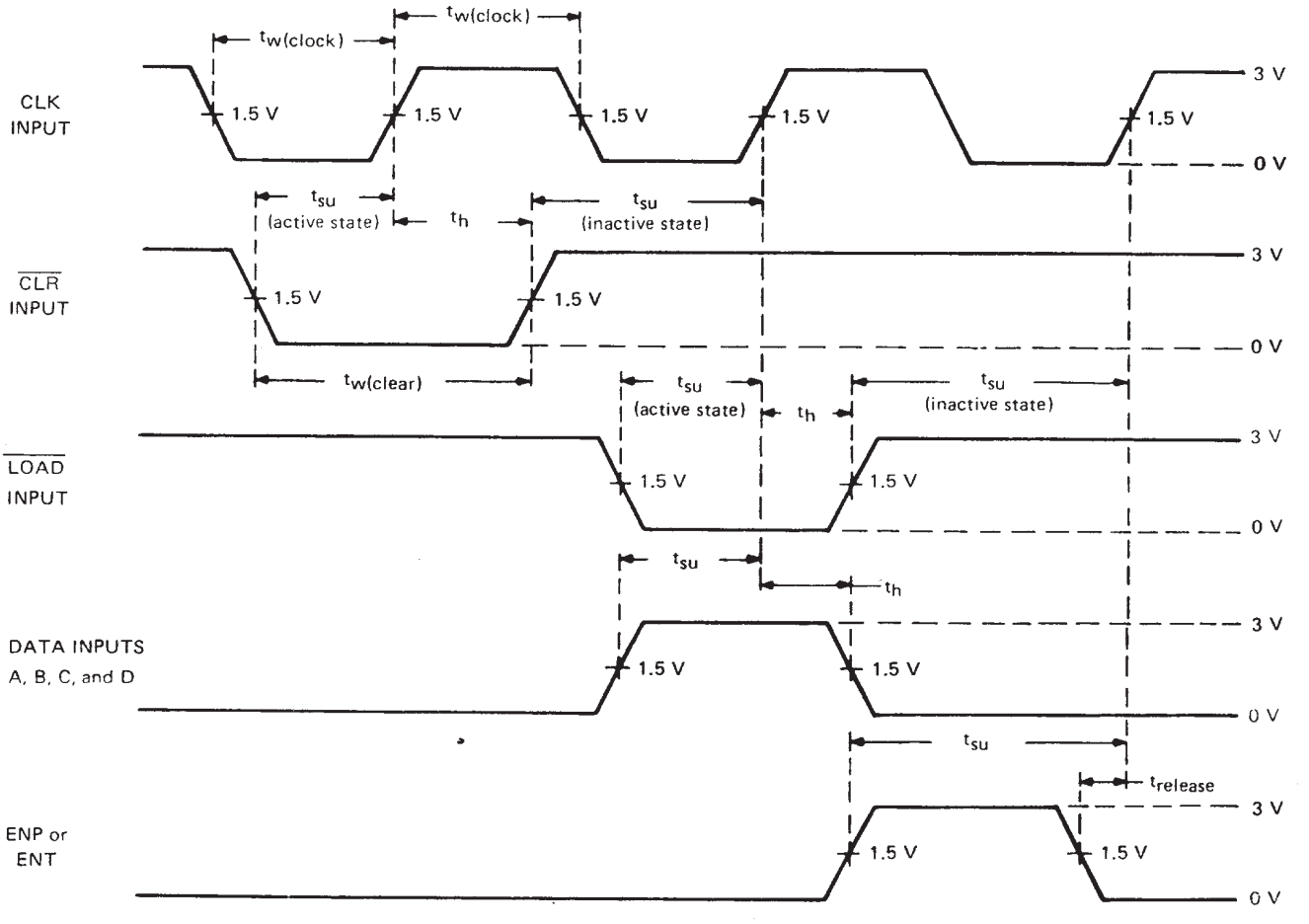


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: t_r ≤ 2.5 ns, t_f ≤ 2.5 ns, PRR = 1 MHz, duty cycle = 50%, Z_{out} ≈ 50 Ω.

B. t_{PLH} and t_{PHL} from enable T input to carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'S162, all Q outputs high for 'S163).

FIGURE 3–PROPAGATION DELAY TIMES FROM ENABLE T INPUT TO CARRY OUTPUT



VOLTAGE WAVEFORMS

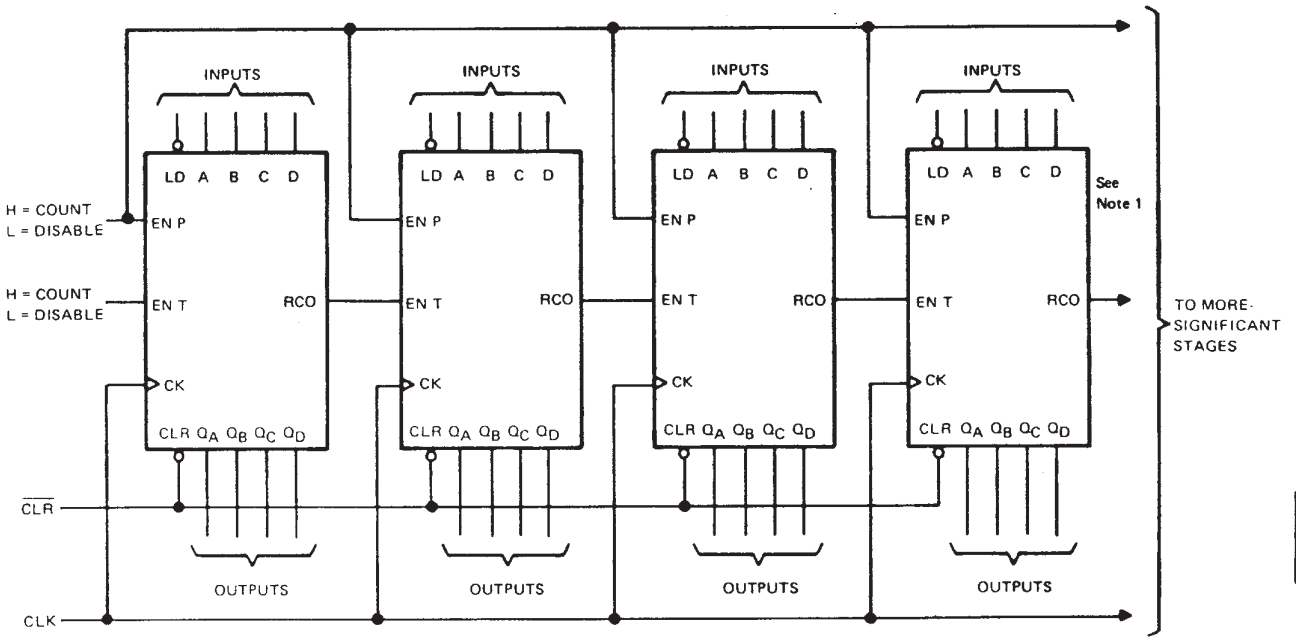
NOTE A: The input pulses are supplied by generators having the following characteristics: t_r = 2.5 ns, t_f = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, Z_{out} ≈ 50 Ω.

FIGURE 4–PULSE WIDTHS, SETUP TIMES, HOLD TIMES, AND RELEASE TIME

TYPICAL APPLICATION DATA

This application demonstrates how the ripple mode carry circuit (Figure 1) and the carry-look-ahead circuit (Figure 2) can be used to implement a high-speed N-bit counter. The '160, '162, 'LS160A, 'LS162A, or 'S162 will count in BCD and the '161, '163, 'LS161A, 'LS163A, or 'S163 will count in binary. When additional stages are added the f_{MAX} decreases in Figure 1, but remains unchanged in Figure 2.

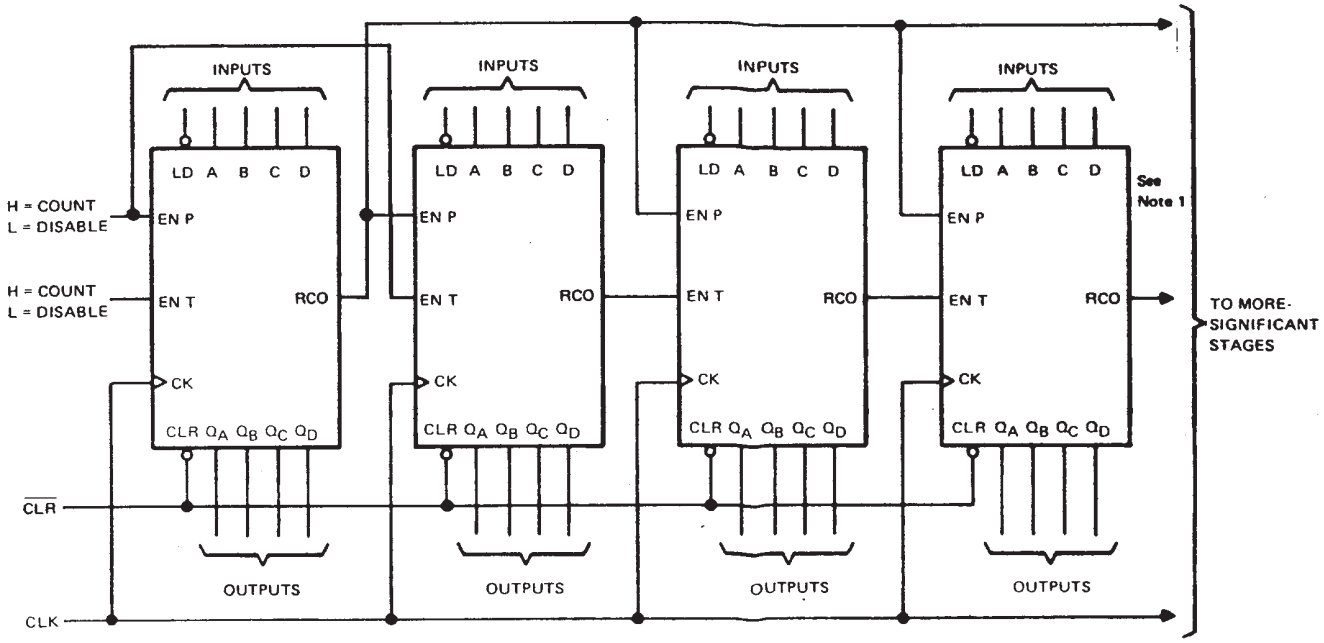
N-BIT SYNCHRONOUS COUNTERS



$f_{MAX} = 1/(\text{CLK to RCO } t_{PLH}) + (\text{ENT to RCO } t_{PLH})(N-2) + (\text{ENT } t_{su})$

FIGURE 1

TYPICAL APPLICATION DATA



$f_{MAX} = 1/(\text{CLK to RCO } t_{PLH} + \text{ENP } t_{su})$

FIGURE 2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-7600801VEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7600801VEA SNV54LS161AJ
5962-7600801VEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7600801VEA SNV54LS161AJ
5962-9754801QEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754801QEA SNJ54163J
5962-9754801QFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754801QFA SNJ54163W
76008012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	76008012A SNJ54LS 161AFK
7600801EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7600801EA SNJ54LS161AJ
7600801FA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7600801FA SNJ54LS161AW
76034012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	76034012A SNJ54LS 163AFK
7603401EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7603401EA SNJ54LS163AJ
7603401FA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7603401FA SNJ54LS163AW
JM38510/31504B2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31504B2A
JM38510/31504B2A.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31504B2A
JM38510/31504BEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31504BEA
JM38510/31504BEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31504BEA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/31504BFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31504BFA
JM38510/31504BFA.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31504BFA
JM38510/31512B2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31512B2A
JM38510/31512B2A.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31512B2A
JM38510/31512BEA	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31512BEA
JM38510/31512BEA.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31512BEA
JM38510/31512BFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31512BFA
JM38510/31512BFA.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31512BFA
M38510/31504B2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31504B2A
M38510/31504BEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31504BEA
M38510/31504BFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31504BFA
M38510/31512B2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31512B2A
M38510/31512BEA	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31512BEA
M38510/31512BFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31512BFA
SN54163J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54163J
SN54163J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54163J
SN54LS161AJ	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS161AJ
SN54LS161AJ.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS161AJ
SN54LS163AJ	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS163AJ
SN54LS163AJ.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS163AJ

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN54S163J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S163J
SN54S163J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54S163J
SN74LS161AD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	LS161A
SN74LS161ADR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS161A
SN74LS161ADR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS161A
SN74LS161AN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS161AN
SN74LS161AN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS161AN
SN74LS161ANSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS161A
SN74LS161ANSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS161A
SN74LS163AD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	LS163A
SN74LS163ADR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS163A
SN74LS163ADR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS163A
SN74LS163AN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS163AN
SN74LS163AN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS163AN
SN74LS163ANE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS163AN
SN74LS163ANSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS163A
SN74LS163ANSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS163A
SN74S163N	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74S163N
SN74S163N.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74S163N
SNJ54163J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754801QEA SNJ54163J
SNJ54163J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754801QEA SNJ54163J
SNJ54163W	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754801QFA SNJ54163W
SNJ54163W.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754801QFA SNJ54163W

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LS161AFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	76008012A SNJ54LS 161AFK
SNJ54LS161AFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	76008012A SNJ54LS 161AFK
SNJ54LS161AJ	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7600801EA SNJ54LS161AJ
SNJ54LS161AJ.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7600801EA SNJ54LS161AJ
SNJ54LS161AW	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7600801FA SNJ54LS161AW
SNJ54LS161AW.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7600801FA SNJ54LS161AW
SNJ54LS163AFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	76034012A SNJ54LS 163AFK
SNJ54LS163AFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	76034012A SNJ54LS 163AFK
SNJ54LS163AJ	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7603401EA SNJ54LS163AJ
SNJ54LS163AJ.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7603401EA SNJ54LS163AJ
SNJ54LS163AW	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7603401FA SNJ54LS163AW
SNJ54LS163AW.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7603401FA SNJ54LS163AW
SNJ54S163J	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S163J
SNJ54S163J.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54S163J

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54LS161A, SN54LS161A-SP, SN54LS163A, SN54S163, SN74LS161A, SN74LS163A, SN74S163 :

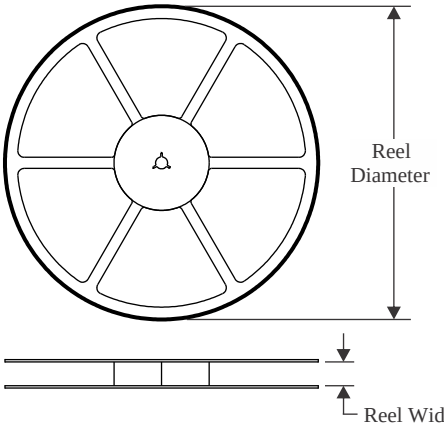
- Catalog : SN74LS161A, SN54LS161A, SN74LS163A, SN74S163
- Military : SN54LS161A, SN54LS163A, SN54S163
- Space : SN54LS161A-SP

NOTE: Qualified Version Definitions:

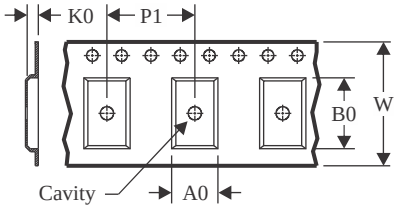
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

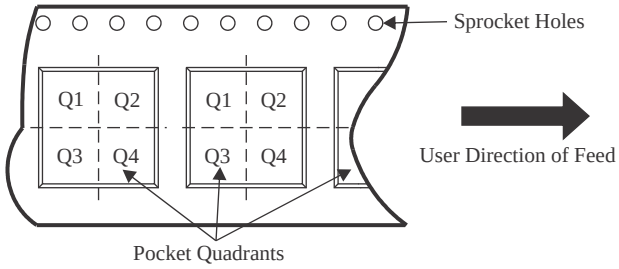


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

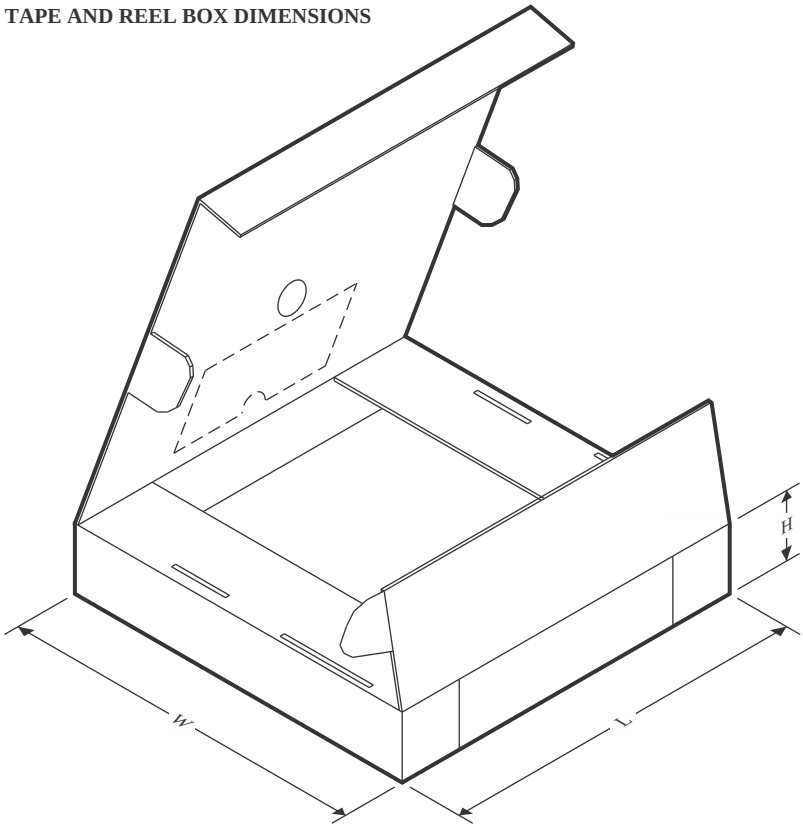
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS161ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS161ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LS163ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS163ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

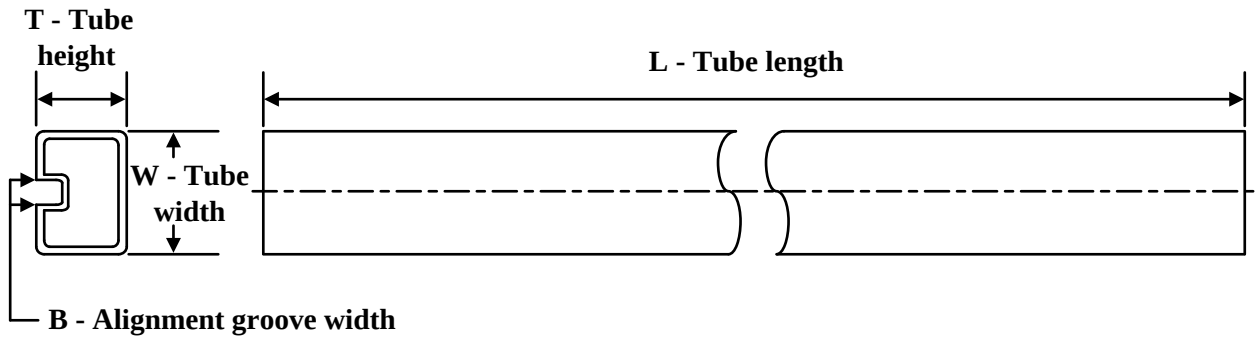
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS161ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS161ANSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74LS163ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS163ANSR	SOP	NS	16	2000	353.0	353.0	32.0

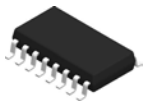
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9754801QFA	W	CFP	16	25	506.98	26.16	6220	NA
76008012A	FK	LCCC	20	55	506.98	12.06	2030	NA
7600801FA	W	CFP	16	25	506.98	26.16	6220	NA
76034012A	FK	LCCC	20	55	506.98	12.06	2030	NA
7603401FA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/31504B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/31504B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/31504BFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/31504BFA.A	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/31512B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/31512B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/31512BFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/31512BFA.A	W	CFP	16	25	506.98	26.16	6220	NA
M38510/31504B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/31504BFA	W	CFP	16	25	506.98	26.16	6220	NA
M38510/31512B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/31512BFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LS161AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS161AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS161AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS161AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS163AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS163AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS163AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS163AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS163ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS163ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74S163N	N	PDIP	16	25	506	13.97	11230	4.32
SN74S163N	N	PDIP	16	25	506	13.97	11230	4.32

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74S163N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74S163N.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54163W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54163W.A	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS161AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS161AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS161AW	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS161AW.A	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS163AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS163AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS163AW	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS163AW.A	W	CFP	16	25	506.98	26.16	6220	NA

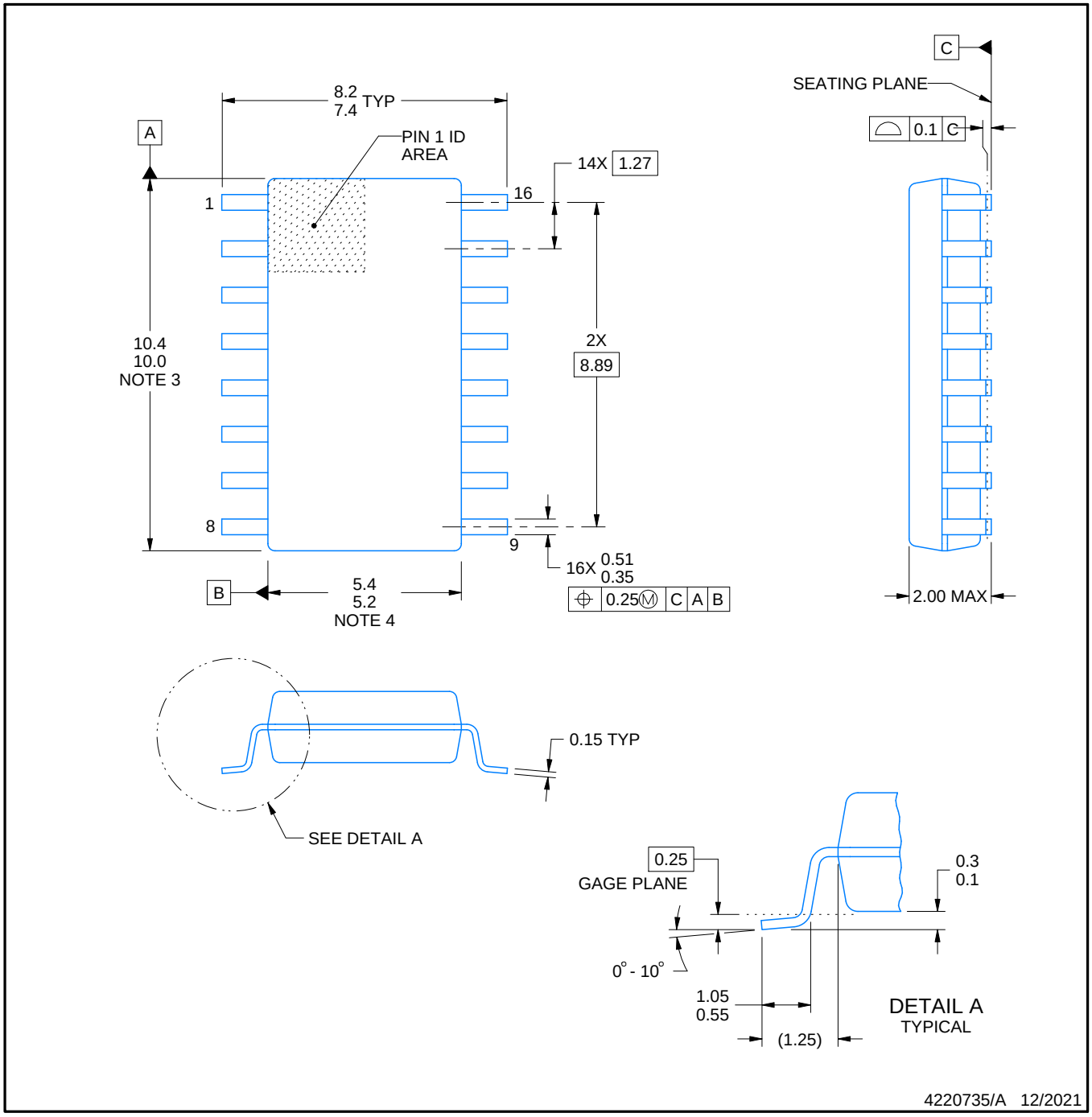


PACKAGE OUTLINE

NS0016A

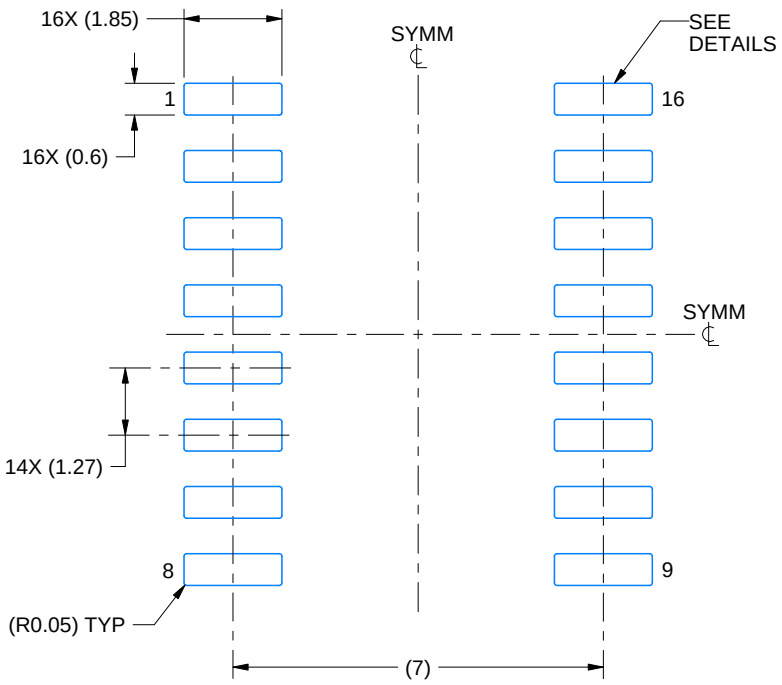
SOP - 2.00 mm max height

SOP

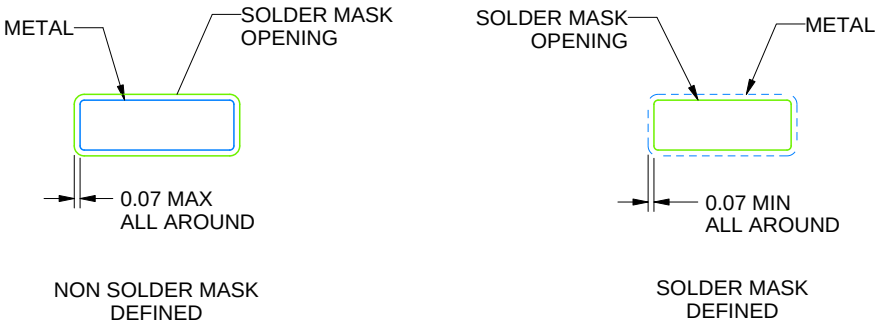


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

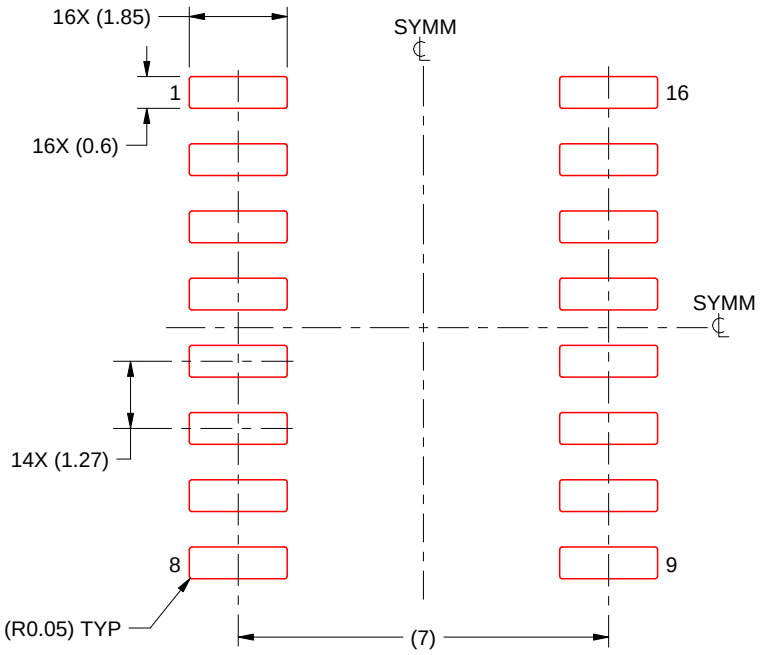
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



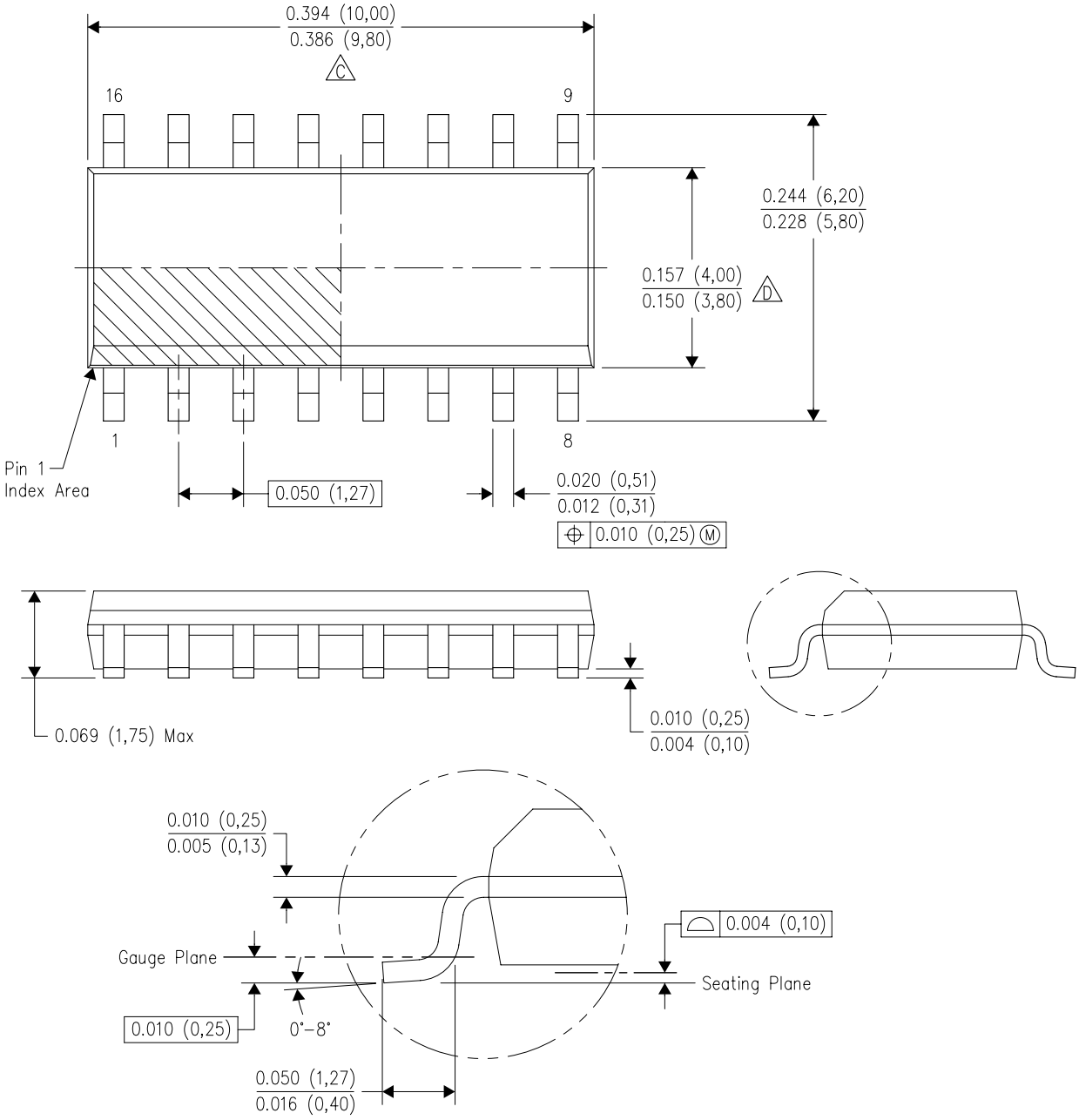
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

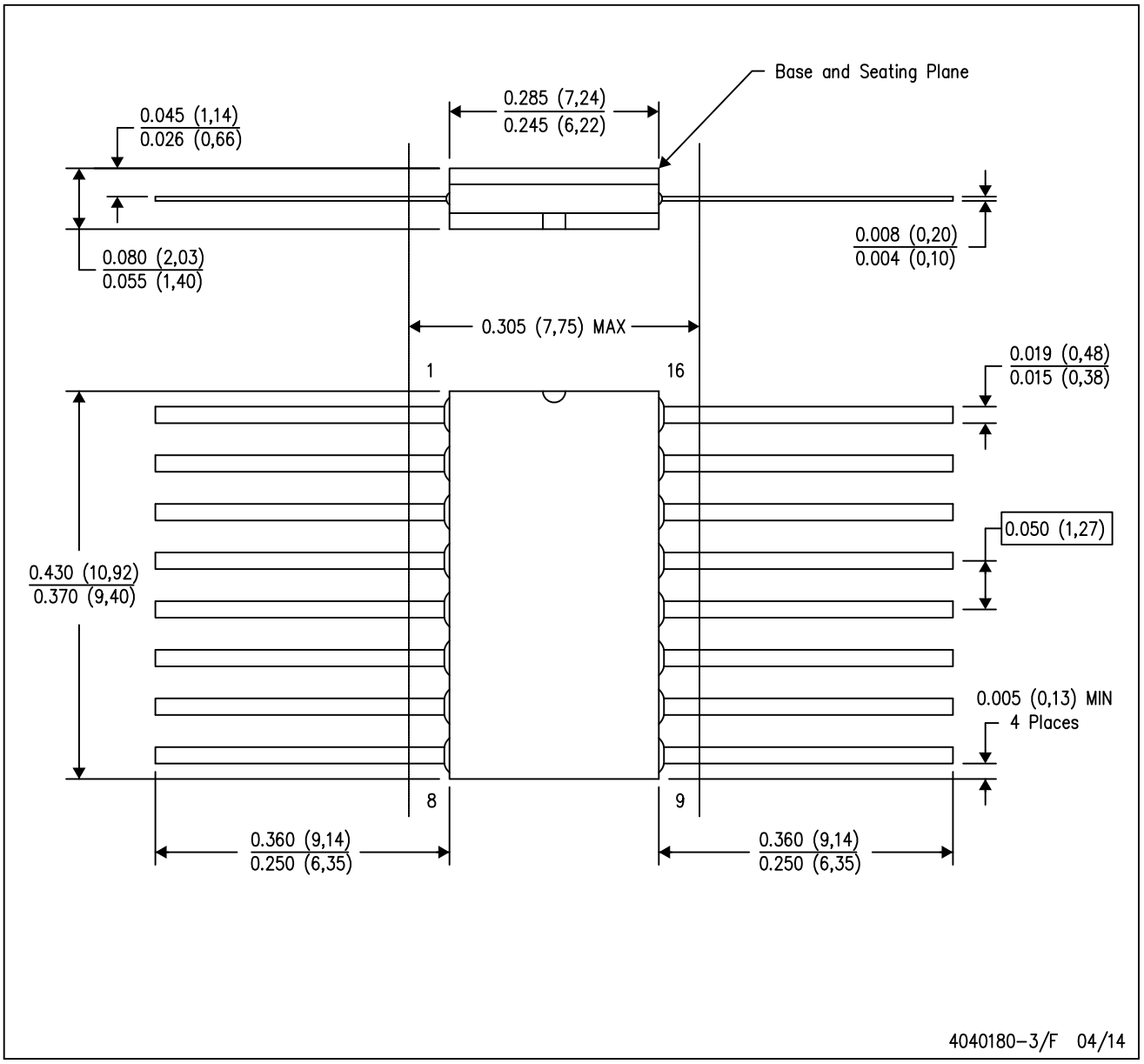
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

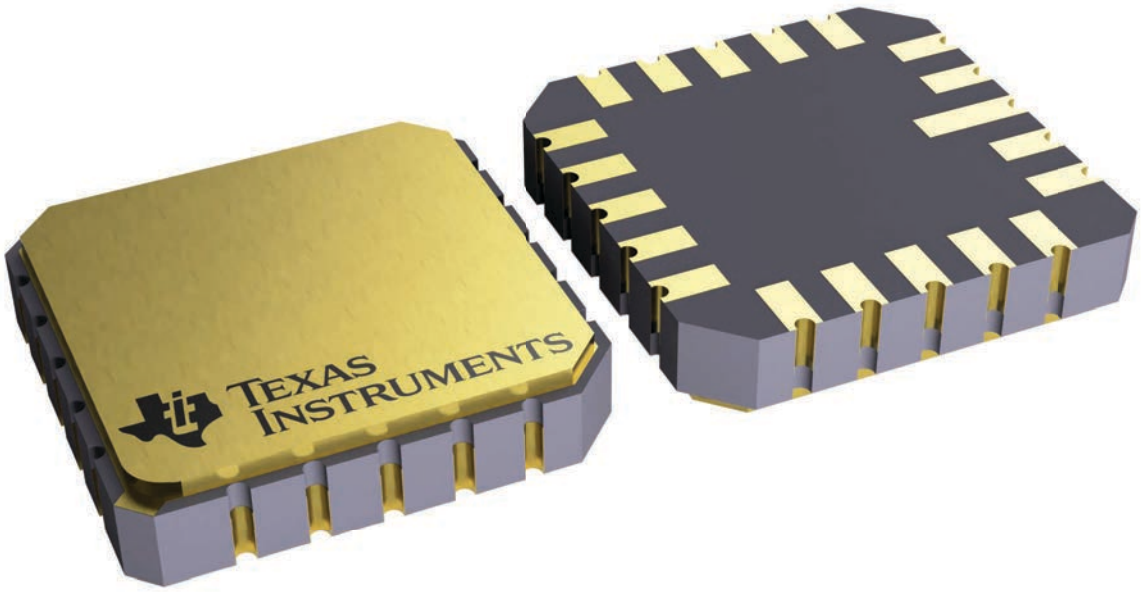
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

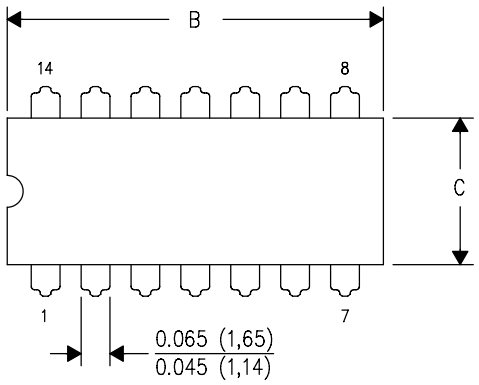


4229370VA\

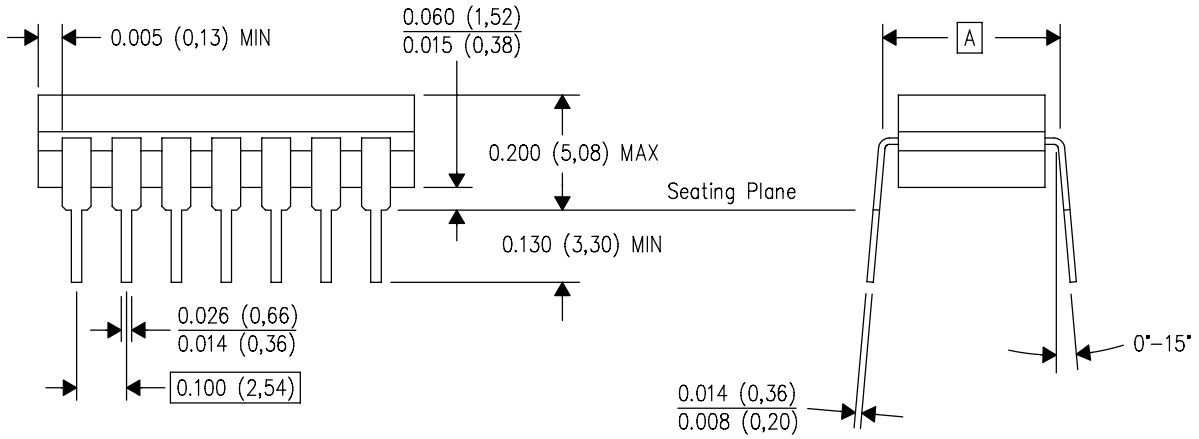
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



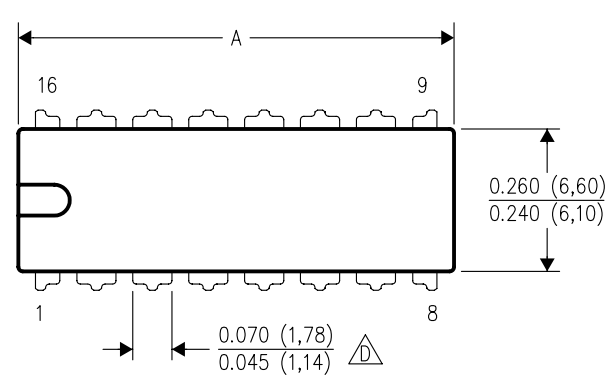
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

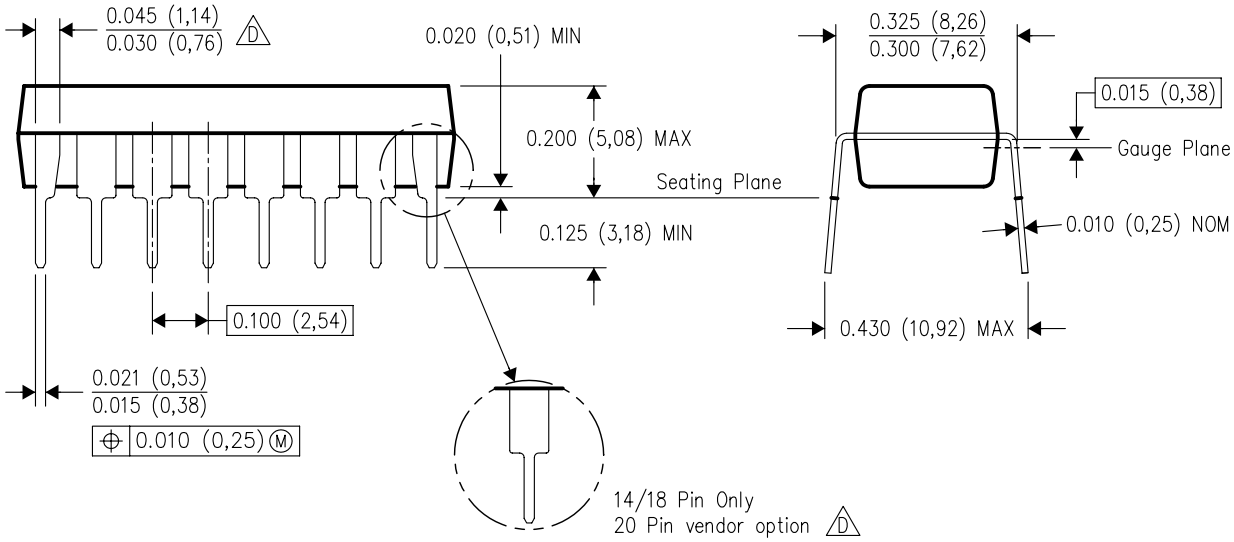
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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