# SNx4LVC02A 四路双输入正或非门

## 1 特性

- 1.65V 到 3.6V 的范围内运行
- 额定温度范围为 –40°C 至 85°C、–40°C 至 125°C 以及 –55°C 至 125°C
- 输入电压高达 5.5V
- 电压为 3.3V 时，$t_{pd}$ 最大值为 4.4ns
- $V_{OLP}$（输出接地反弹）典型值 < 0.8V（$V_{CC}$ = 3.3V、$T_A$ = 25°C）
- $V_{OHV}$（输出 $V_{OH}$ 下冲）典型值 > 2V（$V_{CC}$ = 3.3V、$T_A$ = 25°C）
- 闩锁性能超过 250mA，符合 JESD 17 规范

## 2 说明

输入可以由 3.3V 或 5V 器件驱动。此功能允许在 3.3V/5V 的混合系统环境中将这些器件用作转换器。

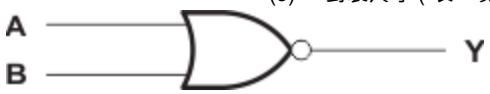
该器件以正逻辑执行布尔函数 $Y = \overline{A + B}$ 或 $Y = \overline{A} \cdot \overline{B}$。

输入可以由 3.3V 或 5V 器件驱动。此功能允许在 3.3V/5V 的混合系统环境中将该器件用作转换器。

**器件信息**

| 器件型号 | 封装尺寸(1) | 封装尺寸(2) | 封装尺寸(3) |
|---|---|---|---|
| SNx4LVC02A | BQA（WQFN，14） | 3mm × 2.5mm | 3mm × 2.5mm |
| | D（SOIC，14） | 8.65mm × 6mm | 8.65mm × 3.9mm |
| | DB（SSOP，14） | 6.2mm × 7.8mm | 6.2mm × 5.3mm |
| | NS（SOP，14） | 10.2mm × 7.8mm | 10.3mm × 5.3mm |
| | PW（TSSOP，14） | 5mm × 6.4mm | 5mm × 4.4mm |
| | RGY（VQFN，14） | 3.5mm × 3.5mm | 3.5mm × 3.5mm |
| | FK（LCCC，20） | 8.9mm x 8.9mm | 8.89mm × 8.89mm |
| | J（CDIP，14） | 19.55mm x 7.9mm | 19.55mm x 6.7mm |
| | W（CFP，14） | 9.21mm x 9mm | 9.21mm x 6.28mm |

(1) 更多相关信息，请参阅第 10 节。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 封装尺寸（长 × 宽）为标称值，不包括引脚。




**逻辑图，每个逻辑门（正逻辑）**

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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# 3 Pin Configuration and Functions

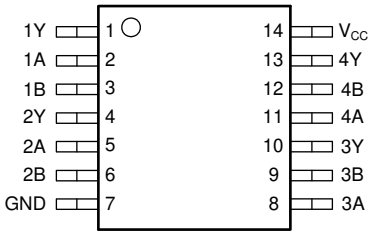



**图 3-1. SN54LVC02A J or W Package, 14-Pin (Top View)**
**SN74LVC02A D, DB, NS, or PW Package, 14-Pin SOIC, SSOP, SOP or TSSOP (Top View)**

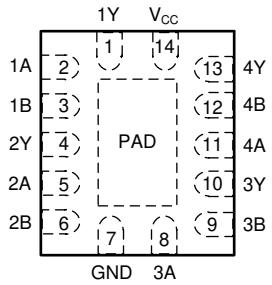



**图 3-2. SN74LVC02A RGY or BQA Package, 14-Pin VQFN or WQFN (Top View)**

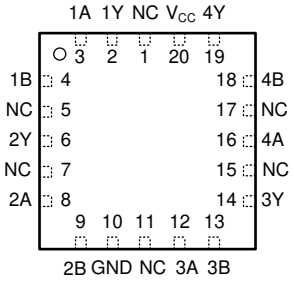



**图 3-3. SN54LVC02A FK Package, 20-Pin (Top View)**

**表 3-1. Pin Functions**

| PIN | | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | SN74LVC02A | SN54LVC02A | | | |
| | D, DB, NS, PW, RGY, BQA | J, W | FK | | |
| 1Y | 1 | 1 | 2 | O | 1Y Output |
| 1A | 2 | 2 | 3 | I | 1A Input |
| 1B | 3 | 3 | 4 | I | 1B Input |
| 2Y | 4 | 4 | 6 | O | 2Y Output |
| 2A | 5 | 5 | 8 | I | 2A Input |
| 2B | 6 | 6 | 9 | I | 2B Input |
| GND | 7 | 7 | 10 | — | Ground Pin |
| 3A | 8 | 8 | 12 | I | 3A Input |
| 3B | 9 | 9 | 13 | I | 3B Input |
| 3Y | 10 | 20 | 14 | O | 3Y Output |
| 4A | 11 | 11 | 16 | I | 4A Input |
| 4B | 12 | 12 | 18 | I | 4B Input |
| 4Y | 13 | 13 | 19 | O | 4Y Output |
| $V_{CC}$ | 14 | 14 | 20 | — | Power Pin |
| NC | — | — | 1, 5, 7, 11, 15, 17 | — | No Connection |

(1) I = input, O = output

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# 4 Specifications

## 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage range(1) | | –0.5 | 6.5 | V |
| $V_O$ | Output voltage range(1) (2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| $P_{tot}$ | Power dissipation | $T_A$ = –40°C to 125°C(3) (4) | | 500 | mW |

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(2) The value of $V_{CC}$ is provided in the recommended operating conditions table.
(3) For the D package: above 70°C, the value of $P_{tot}$ derates linearly with 8 mW/K.
(4) For the DB, NS, and PW packages: above 60°C, the value of $P_{tot}$ derates linearly with 5.5 mW/K.

## 4.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 4.3 Recommended Operating Conditions, SN54LVC02A

| | | | SN54LVC02A –55°C to 125°C | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{CC}$ | Supply voltage | Operating | 2 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2.7V to 3.6V | 2 | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2.7V to 3.6V | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.7V | | –12 | mA |
| | | $V_{CC}$ = 3V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.7V | | 12 | mA |
| | | $V_{CC}$ = 3V | | 24 | |

## 4.4 Recommended Operating Conditions, SN74LVC02A

| | | | SN74LVC02A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 3.6 | 1.65 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | 1.5 | | |


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| | | | SN74LVC02A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65V to 1.95V | 0.65 × $V_{CC}$ | | 0.65 × $V_{CC}$ | | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3V to 2.7V | 1.7 | | 1.7 | | 1.7 | | |
| | | $V_{CC}$ = 2.7V to 3.6V | 2 | | 2 | | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65V to 1.95V | | 0.35 × $V_{CC}$ | | 0.35 × $V_{CC}$ | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3V to 2.7 V | | 0.7 | | 0.7 | | 0.7 | |
| | | $V_{CC}$ = 2.7V to 3.6 V | | 0.8 | | 0.8 | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65V | | –4 | | –4 | | –4 | mA |
| | | $V_{CC}$ = 2.3V | | –8 | | –8 | | –8 | |
| | | $V_{CC}$ = 2.7V | | –12 | | –12 | | –12 | |
| | | $V_{CC}$ = 3V | | –24 | | –24 | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65V | | 4 | | 4 | | 4 | mA |
| | | $V_{CC}$ = 2.3V | | 8 | | 8 | | 8 | |
| | | $V_{CC}$ = 2.7V | | 12 | | 12 | | 12 | |
| | | $V_{CC}$ = 3V | | 24 | | 24 | | 24 | |

## 4.5 Thermal Information

| THERMAL METRIC[1] | | SN74LVC02A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BQA (WQFN) | D (SOIC) | DB (SSOP) | NS (SOP) | PW (TSSOP) | RGY (VQFN) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 102.3 | 127.8 | 140.4 | 123.8 | 150.8 | 92.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

## 4.6 Electrical Characteristics, SN54LVC02A

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | SN54LVC02A | | | UNIT |
|---|---|---|---|---|---|---|
| | | | –55°C to 125°C | | | |
| | | | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH}$ = –100µA | 2.7V to 3.6V | $V_{CC}$ – 0.2 | | | V |
| | $I_{OH}$ = –12mA | 2.7V | 2.2 | | | |
| | | 3V | 2.4 | | | |
| | $I_{OH}$ = –24mA | 3V | 2.2 | | | |
| $V_{OL}$ | $I_{OL}$ = 100µA | 2.7V to 3.6V | | | 0.2 | V |
| | $I_{OL}$ = 12mA | 2.7V | | | 0.4 | |
| | $I_{OL}$ = 24mA | 3V | | | 0.55 | |
| $I_I$ | $V_I$ = 5.5V or GND | 3.6V | | | ±5 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 3.6V | | | 10 | µA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6V, Other inputs at $V_{CC}$ or GND | 2.7V to 3.6V | | | 500 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3V | | 5[1] | | pF |

(1) $T_A$ = 25°C

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## 4.7 Electrical Characteristics, SN74LVC02A

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | SN74LVC02A | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –100µA | 1.65V to 3.6V | $V_{CC}$ – 0.2 | | | $V_{CC}$ – 0.2 | | $V_{CC}$ – 0.3 | | V |
| | $I_{OH}$ = –4mA | 1.65V | 1.29 | | | 1.2 | | 1.05 | | |
| | $I_{OH}$ = –8mA | 2.3V | 1.9 | | | 1.7 | | 1.55 | | |
| | $I_{OH}$ = –12mA | 2.7V | 2.2 | | | 2.2 | | 2.05 | | |
| | | 3V | 2.4 | | | 2.4 | | 2.25 | | |
| | $I_{OH}$ = –24mA | 3V | 2.3 | | | 2.2 | | 2 | | |
| $V_{OL}$ | $I_{OL}$ = 100µA | 1.65V to 3.6V | | | 0.1 | | 0.2 | | 0.3 | V |
| | $I_{OL}$ = 4mA | 1.65V | | | 0.24 | | 0.45 | | 0.6 | |
| | $I_{OL}$ = 8mA | 2.3V | | | 0.3 | | 0.7 | | 0.75 | |
| | $I_{OL}$ = 12mA | 2.7V | | | 0.4 | | 0.4 | | 0.6 | |
| | $I_{OL}$ = 24mA | 3V | | | 0.55 | | 0.55 | | 0.8 | |
| $I_I$ | $V_I$ = 5.5V or GND | 3.6V | | | ±1 | | ±5 | | ±20 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 3.6V | | | 1 | | 10 | | 40 | µA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | 2.7V to 3.6V | | | 500 | | 500 | | 5000 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 5 | | | | | | pF |

## 4.8 Switching Characteristics, SN54LVC02A

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN54LVC02A | | UNIT |
|---|---|---|---|---|---|---|
| | | | | –55°C to 125°C | | |
| | | | | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 2.7V | | 5.4 | ns |
| | | | 3.3V ± 0.3V | 1 | 4.4 | |

## 4.9 Switching Characteristics, SN74LVC02A

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74LVC02A | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A or B | Y | 1.8V ± 0.15V | 1 | 3.8 | 8.4 | 1 | 8.9 | 1 | 10.4 | ns |
| | | | 2.5V ± 0.2V | 1 | 2.9 | 6.9 | 1 | 7.4 | 1 | 9.5 | |
| | | | 2.7V | 1 | 3 | 5.2 | 1 | 5.4 | 1 | 7 | |
| | | | 3.3V ± 0.3V | 1 | 3.6 | 4.2 | 1 | 4.4 | 1 | 5.5 | |
| $t_{sk(o)}$ | | | 3.3V ± 0.3V | | | | | 1 | | 1.5 | ns |


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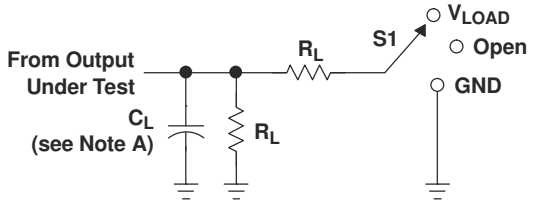
## 4.10 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per gate | f = 10MHz | 1.8V | 7.5 | pF |
| | | | 2.5V | 8.5 | |
| | | | 3.3V | 9.5 | |

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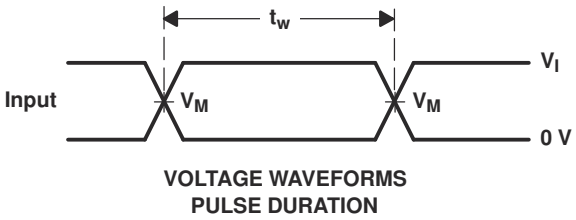
# 5 Parameter Measurement Information



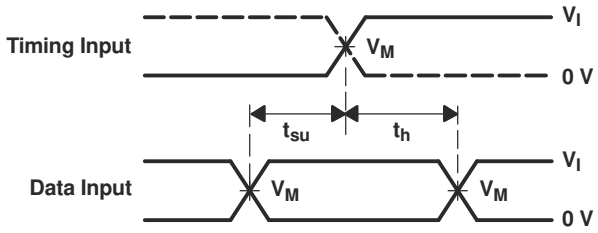

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

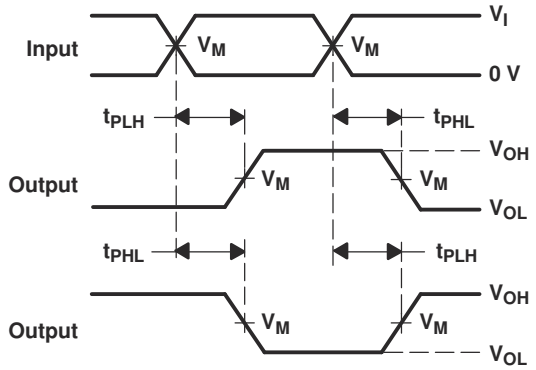
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



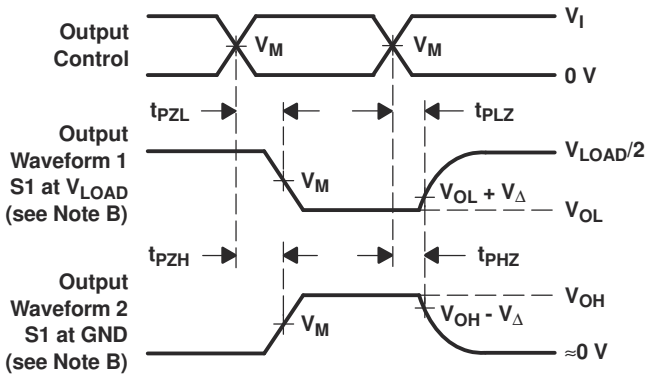

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**图 5-1. Load Circuit and Voltage Waveforms**


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# 6 Detailed Description

## 6.1 Functional Block Diagram




**图 6-1. Logic Diagram, Each Gate (Positive Logic)**

## 6.2 Device Functional Modes

**Function Table (Each Gate)**

| INPUTS | | OUTPUT Y |
|---|---|---|
| A | B | |
| H | X | L |
| X | H | L |
| L | L | H |

# 7 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

## 7.2 Layout

### *7.2.1 Layout Guidelines*

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

### *7.2.2 Layout Example*

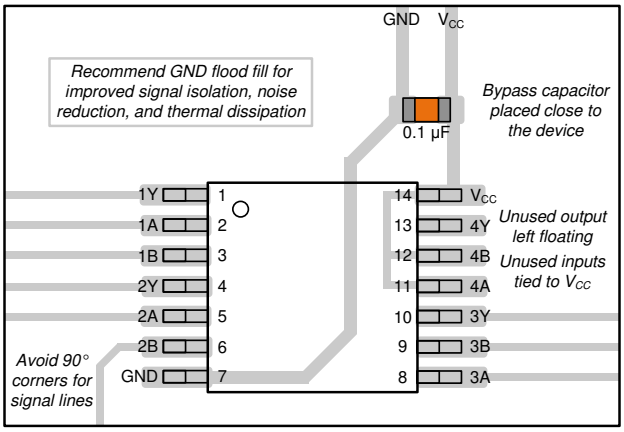



**图 7-1. Example Layout for the SNx4LVC02A**


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# 8 Device and Documentation Support

## 8.1 Documentation Support

### *8.1.1 Related Documentation*

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 8-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54LVC02A | Click here | Click here | Click here | Click here | Click here |
| SN74LVC02A | Click here | Click here | Click here | Click here | Click here |

## 8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

## 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 9 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision S (May 2024) to Revision T (December 2024) | Page |
|---|---|
| • Updated RθJA values: D = 86 to 127.8, all values in °C/W | 5 |

| Changes from Revision R (March 2024) to Revision S (May 2024) | Page |
|---|---|
| • Updated RθJA values: DB = 96 to 140.4, NS = 76 to 123.8, PW = 113 to 150.8, RGY = 47 to 92.1; Updated DB, NS, PW, and RGY packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W | 5 |

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## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9760401Q2A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9760401Q2A SNJ54LVC02AFK |
| 5962-9760401QCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9760401QCA SNJ54LVC02AJ |
| 5962-9760401QDA | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9760401QDA SNJ54LVC02AW |
| SN74LVC02ABQAR | Active | Production | WQFN (BQA) \| 14 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LVC02A |
| SN74LVC02ABQAR.A | Active | Production | WQFN (BQA) \| 14 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | LVC02A |
| SN74LVC02AD | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC02A |
| SN74LVC02AD.B | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC02A |
| SN74LVC02ADBR | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02ADBR.A | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02ADBR.B | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02ADR | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC02A |
| SN74LVC02ADR.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC02A |
| SN74LVC02ADR.B | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC02A |
| SN74LVC02ADRG4 | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC02A |
| SN74LVC02ANSR | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC02A |
| SN74LVC02ANSR.A | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC02A |
| SN74LVC02ANSR.B | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC02A |
| SN74LVC02APW | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02APW.B | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02APWE4 | Active | Production | TSSOP (PW) \| 14 | 90 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02APWR | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02APWR.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02APWR.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02APWR1G4 | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LVC02APWR1G4.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02APWR1G4.B | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02APWT | Active | Production | TSSOP (PW) \| 14 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02APWT.B | Active | Production | TSSOP (PW) \| 14 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC02A |
| SN74LVC02ARGYR | Active | Production | VQFN (RGY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC02A |
| SN74LVC02ARGYR.A | Active | Production | VQFN (RGY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC02A |
| SN74LVC02ARGYR.B | Active | Production | VQFN (RGY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC02A |
| SN74LVC02ARGYRG4 | Active | Production | VQFN (RGY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC02A |
| SN74LVC02ARGYRG4.A | Active | Production | VQFN (RGY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC02A |
| SN74LVC02ARGYRG4.B | Active | Production | VQFN (RGY) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC02A |
| SNJ54LVC02AFK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9760401Q2A SNJ54LVC 02AFK |
| SNJ54LVC02AJ | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9760401QC A SNJ54LVC02AJ |
| SNJ54LVC02AW | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9760401QD A SNJ54LVC02AW |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC02A, SN74LVC02A :**

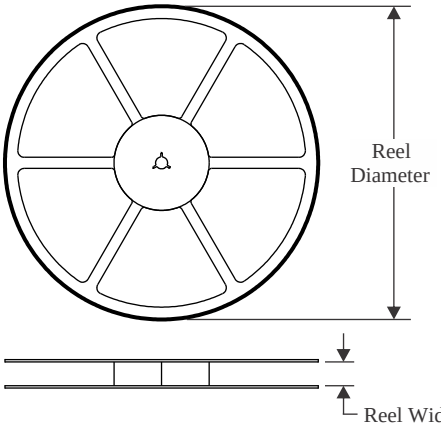
- Catalog : SN74LVC02A
- Automotive : SN74LVC02A-Q1, SN74LVC02A-Q1
- Enhanced Product : SN74LVC02A-EP, SN74LVC02A-EP
- Military : SN54LVC02A

NOTE: Qualified Version Definitions:

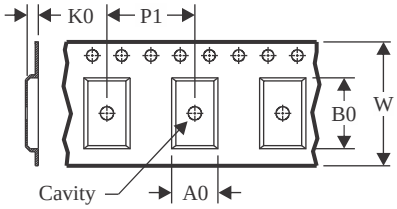
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

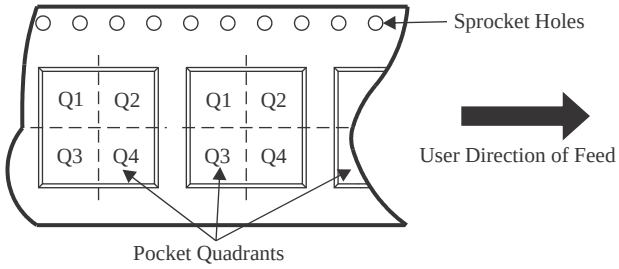



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

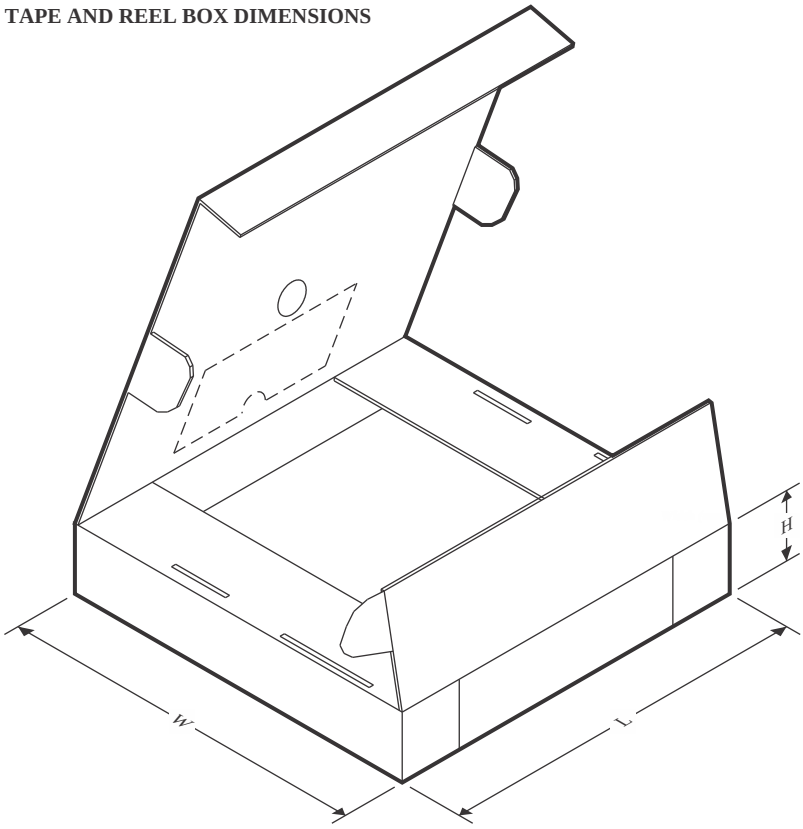
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC02ABQAR | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |
| SN74LVC02ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LVC02ANSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC02APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC02APWR1G4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC02APWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC02ARGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |
| SN74LVC02ARGYRG4 | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

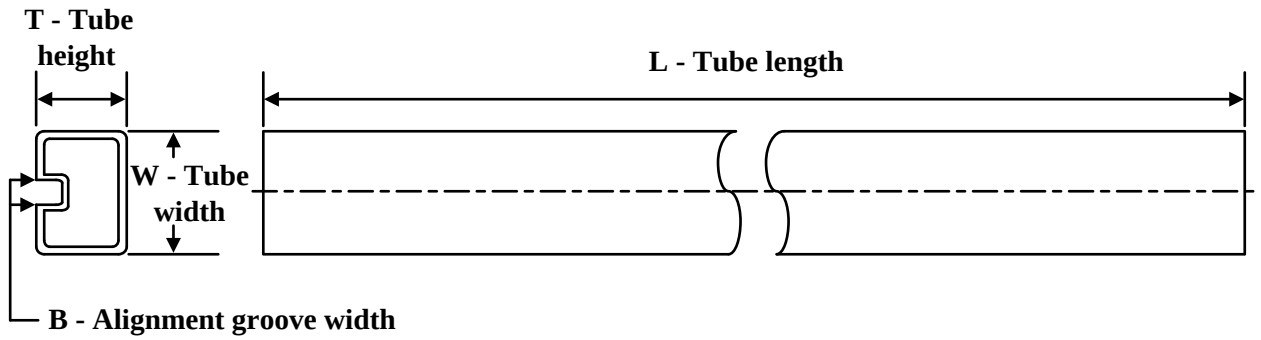
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC02ABQAR | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC02ADBR | SSOP | DB | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVC02ANSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVC02APWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVC02APWR1G4 | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVC02APWT | TSSOP | PW | 14 | 250 | 353.0 | 353.0 | 32.0 |
| SN74LVC02ARGYR | VQFN | RGY | 14 | 3000 | 360.0 | 360.0 | 36.0 |
| SN74LVC02ARGYRG4 | VQFN | RGY | 14 | 3000 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9760401Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9760401QDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74LVC02AD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LVC02AD.B | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LVC02APW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVC02APW.B | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVC02APWE4 | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| SNJ54LVC02AFK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54LVC02AW | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

# GENERIC PACKAGE VIEW

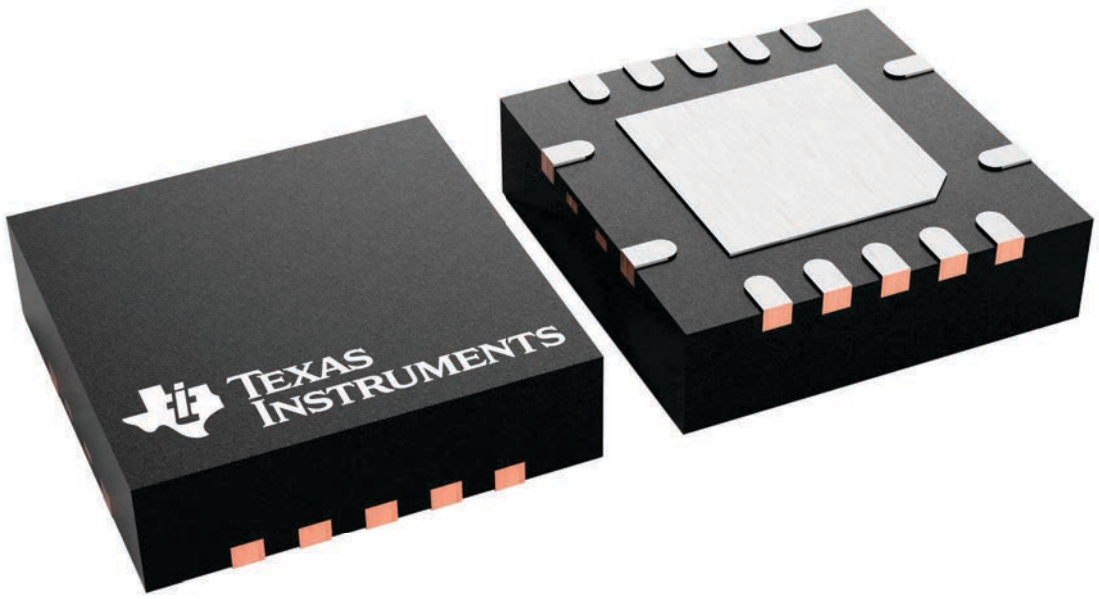
## RGY 14

## VQFN - 1 mm max height

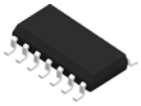
**3.5 x 3.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4231541/A

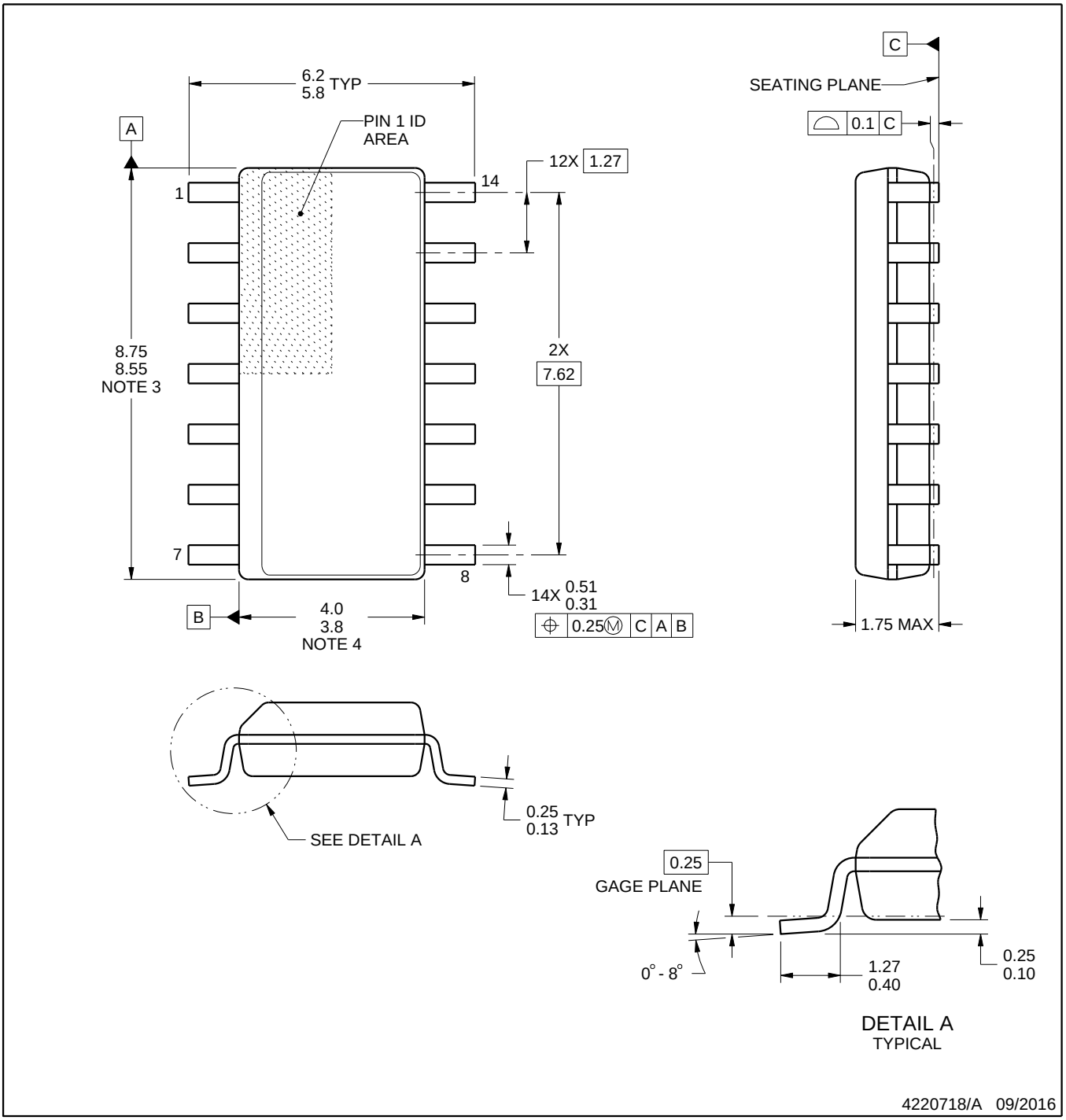


# PACKAGE OUTLINE

## D0014A

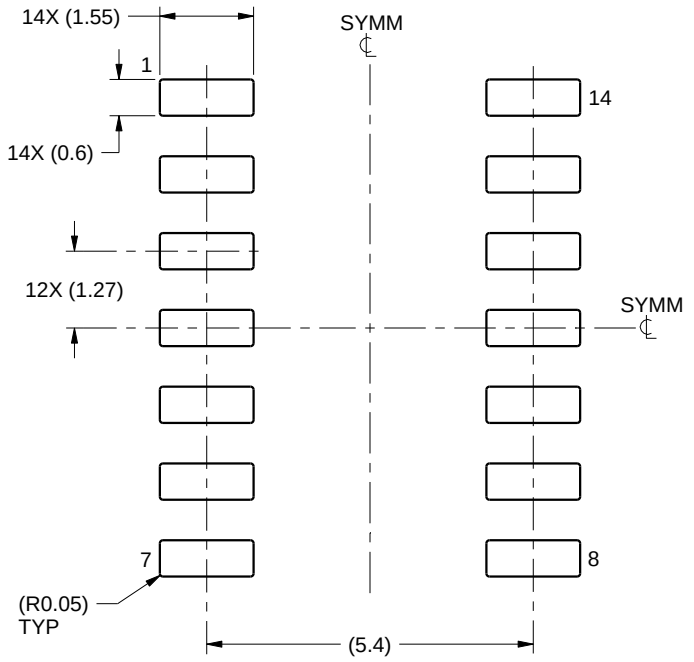
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

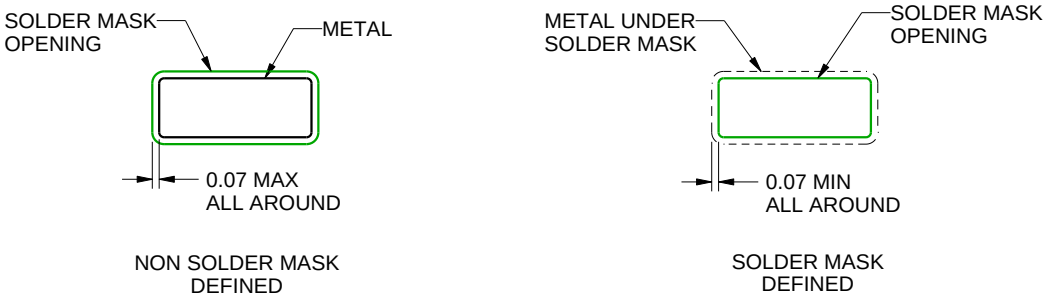



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

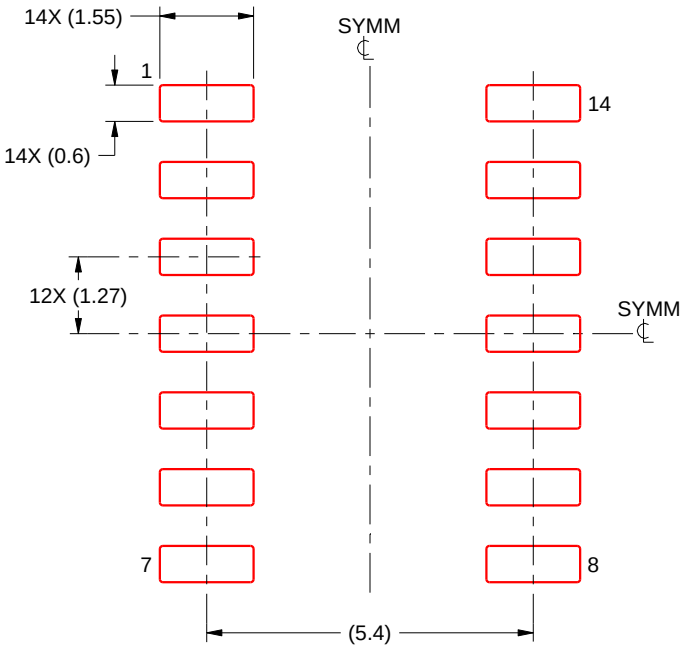
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

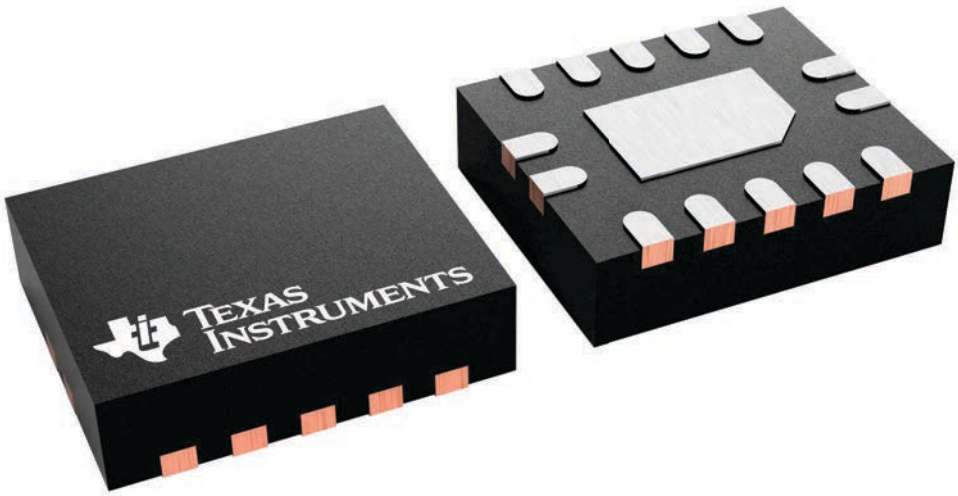
## BQA 14

## WQFN - 0.8 mm max height

**2.5 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

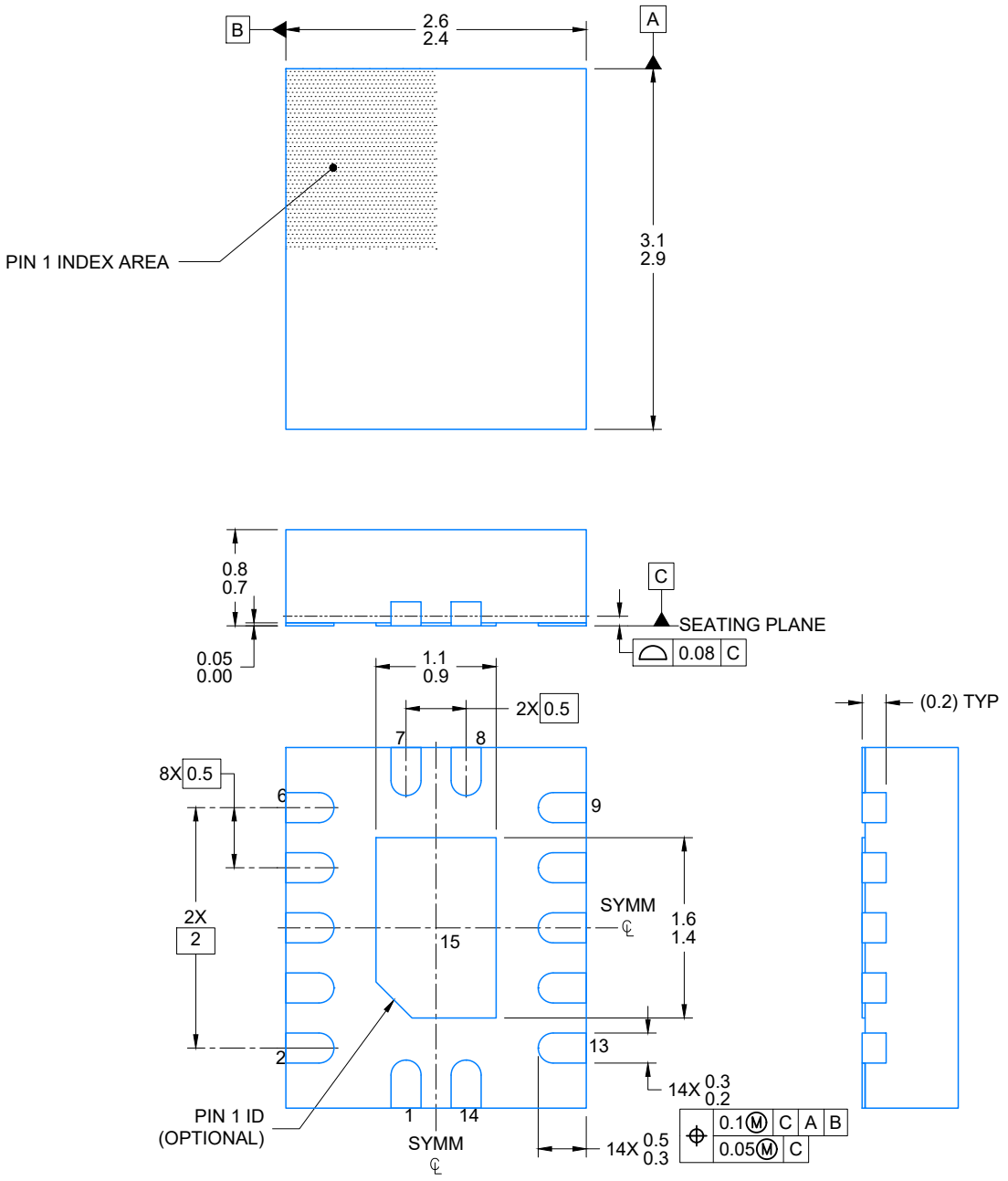


# PACKAGE OUTLINE

## BQA0014A

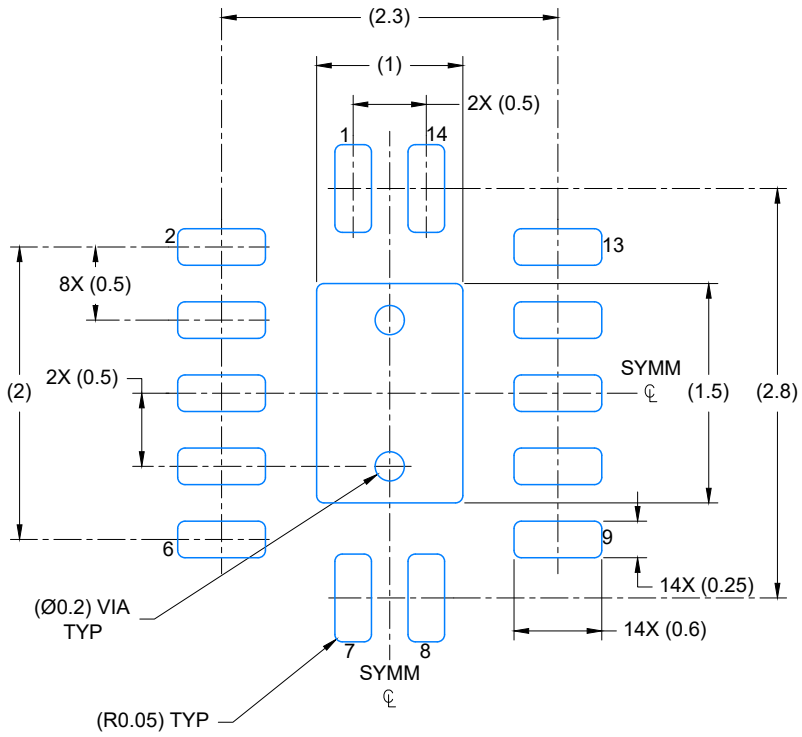
### WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

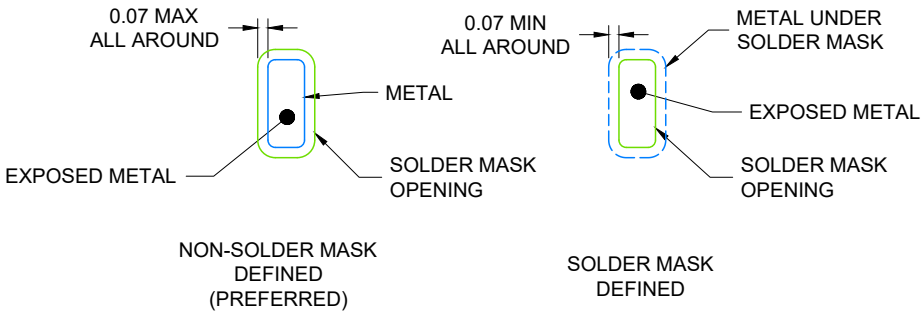



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



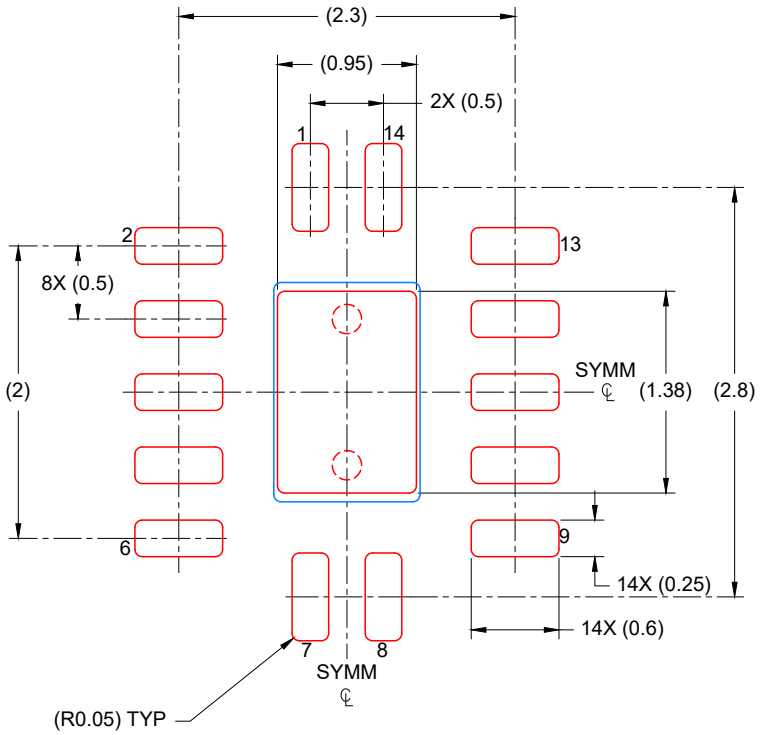

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

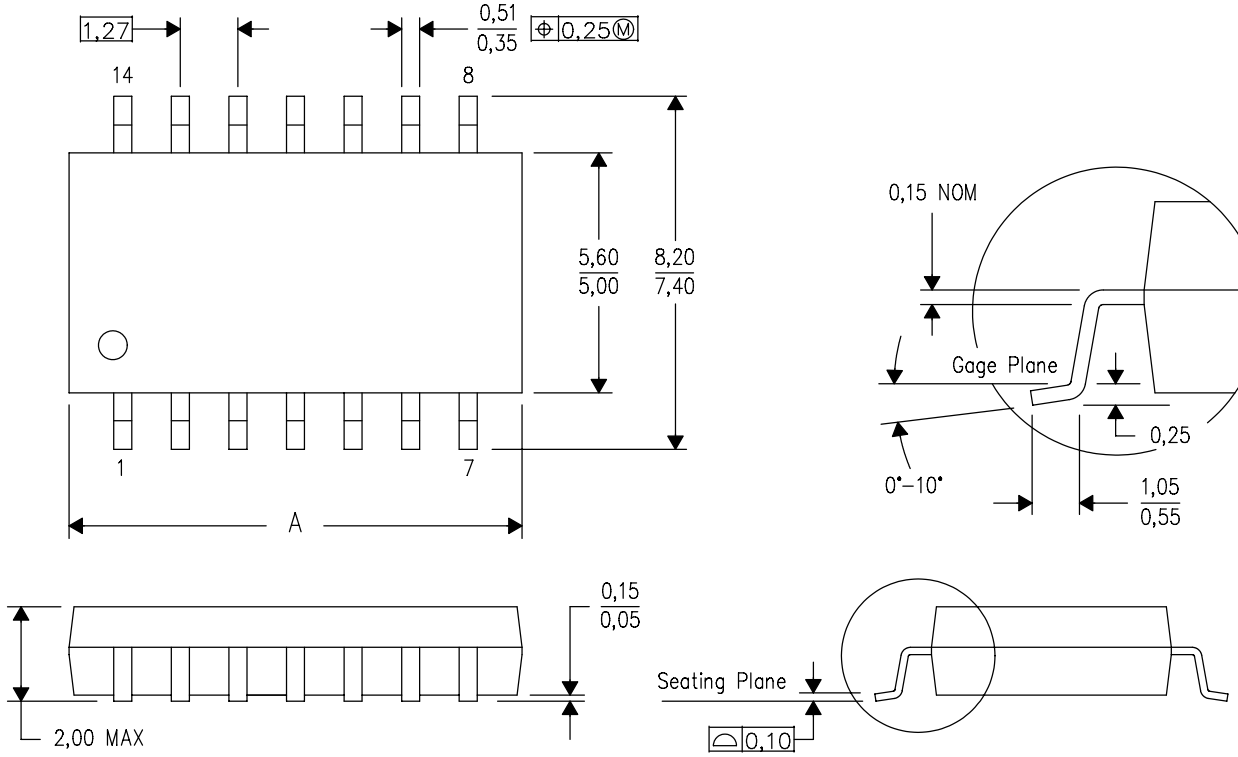
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

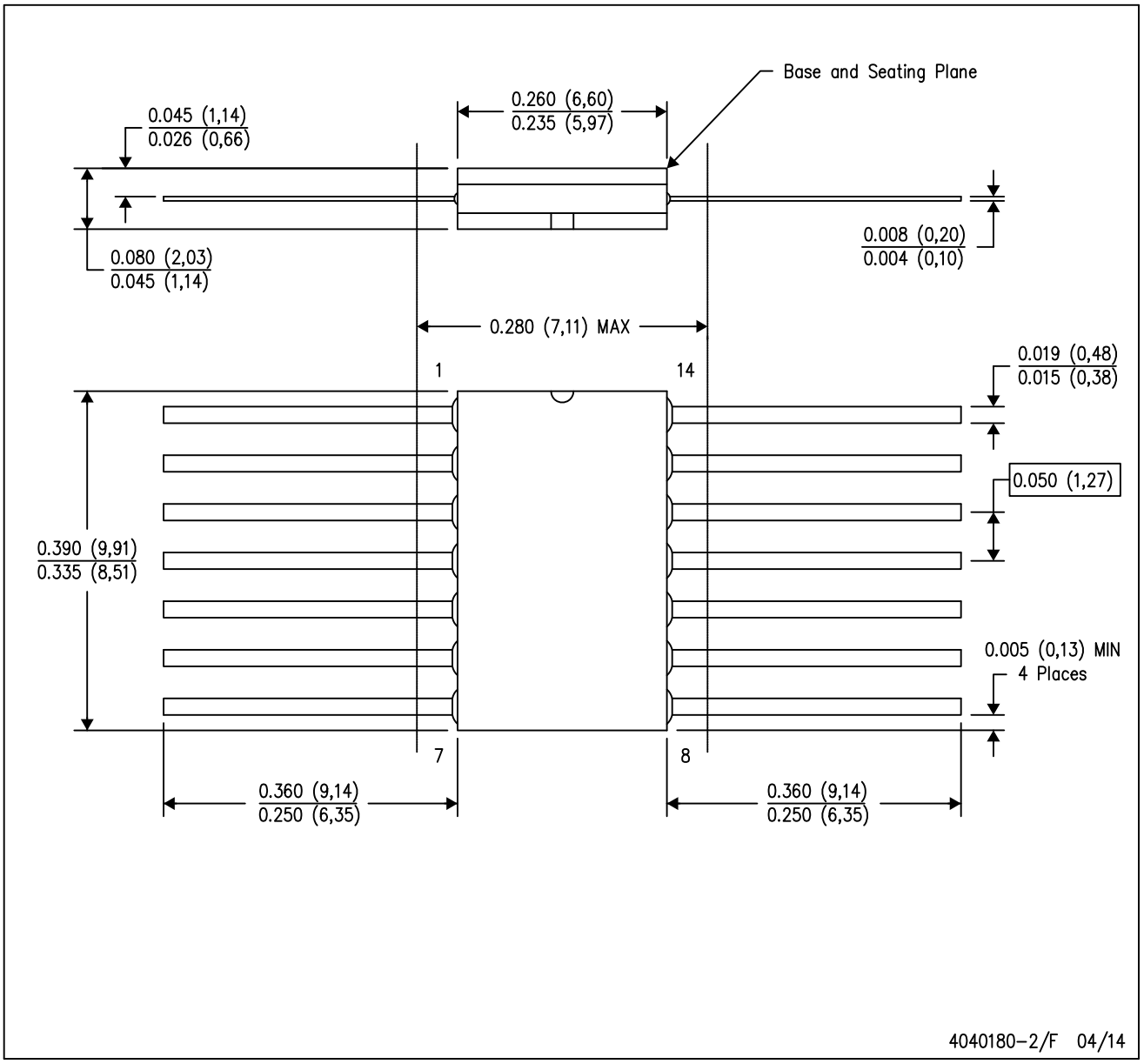



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



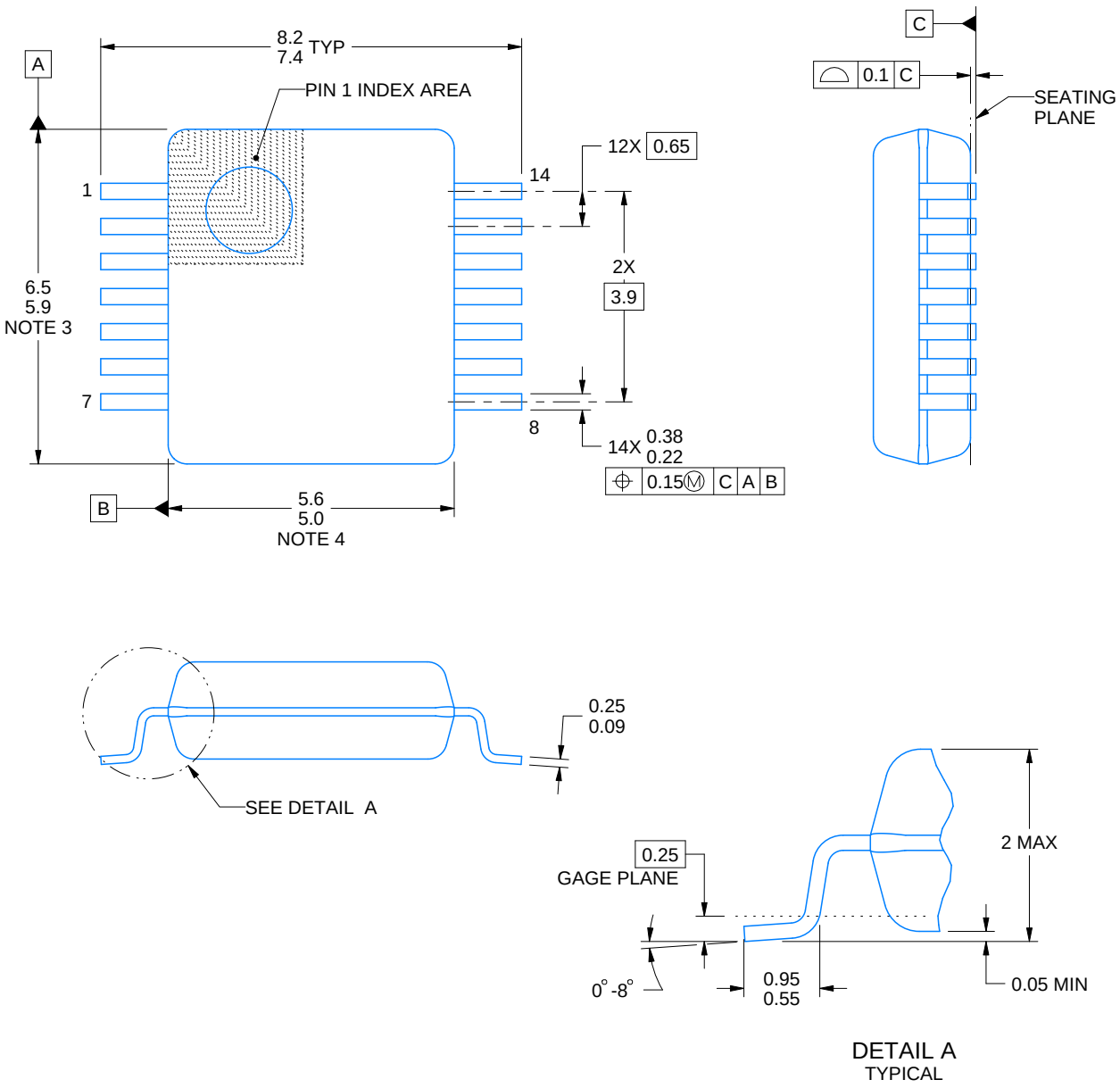

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

# PACKAGE OUTLINE

## DB0014A

## SSOP - 2 mm max height

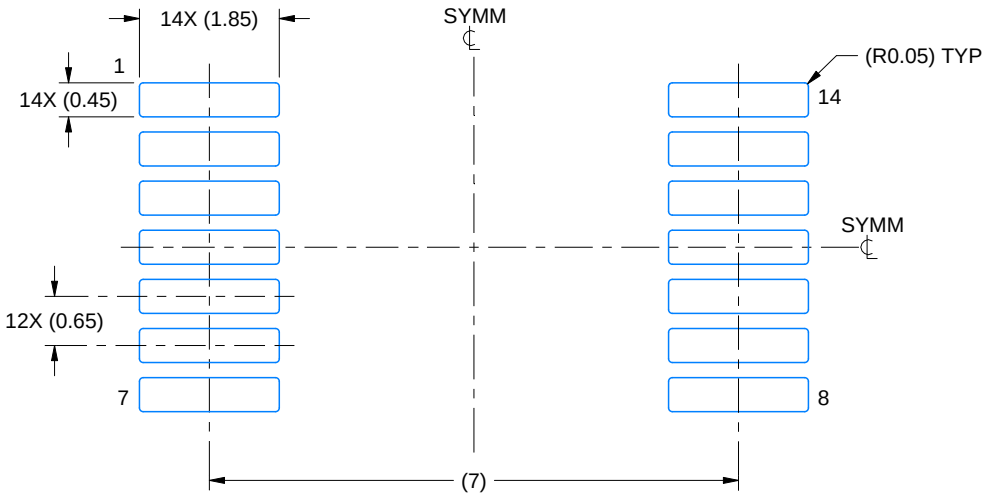
SMALL OUTLINE PACKAGE



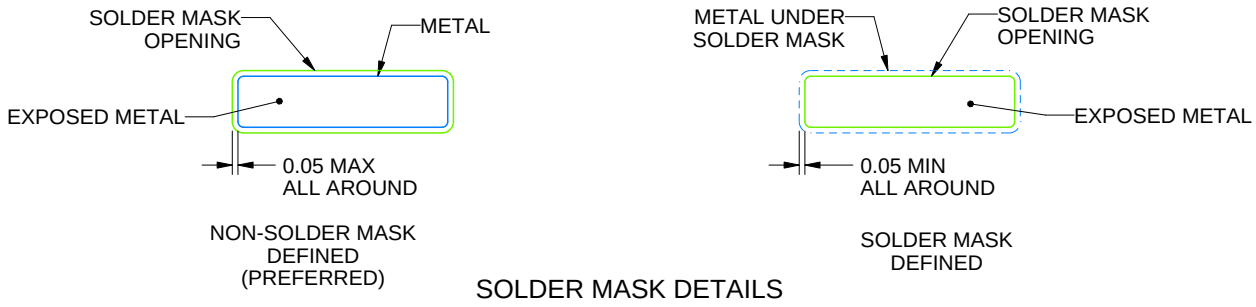

4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

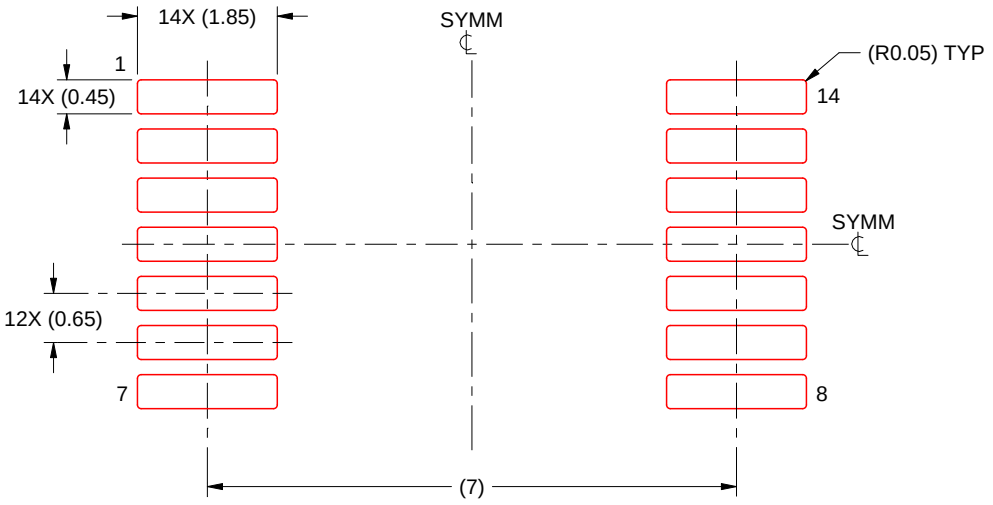



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

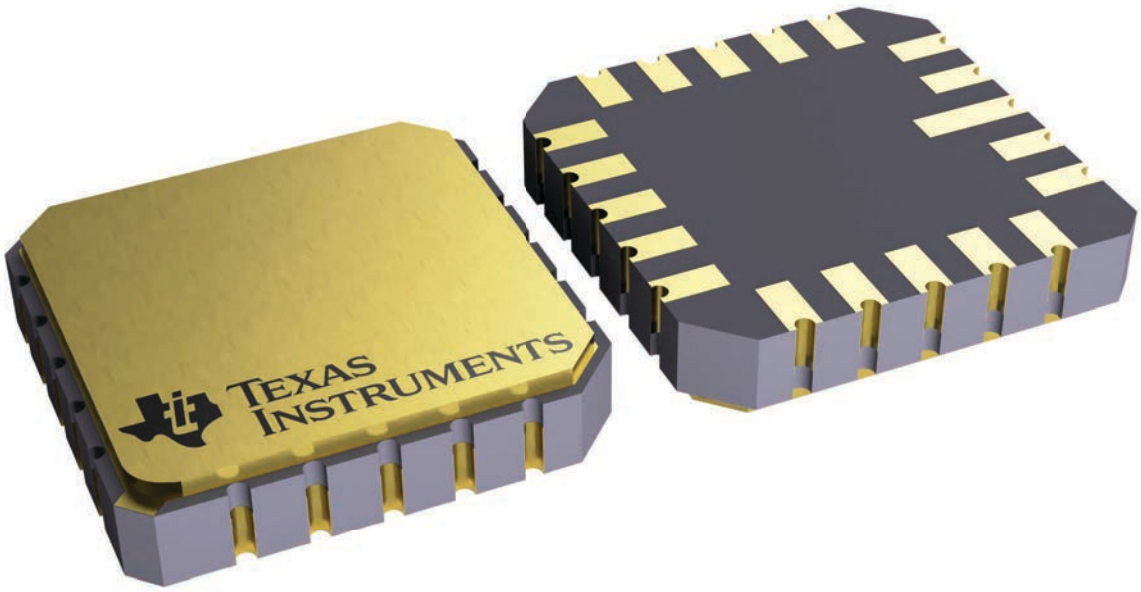
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

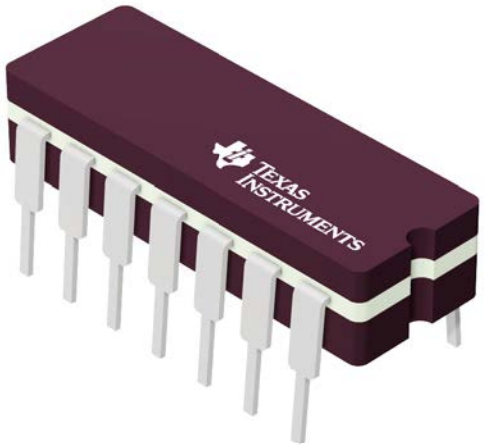



4229370VA\

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

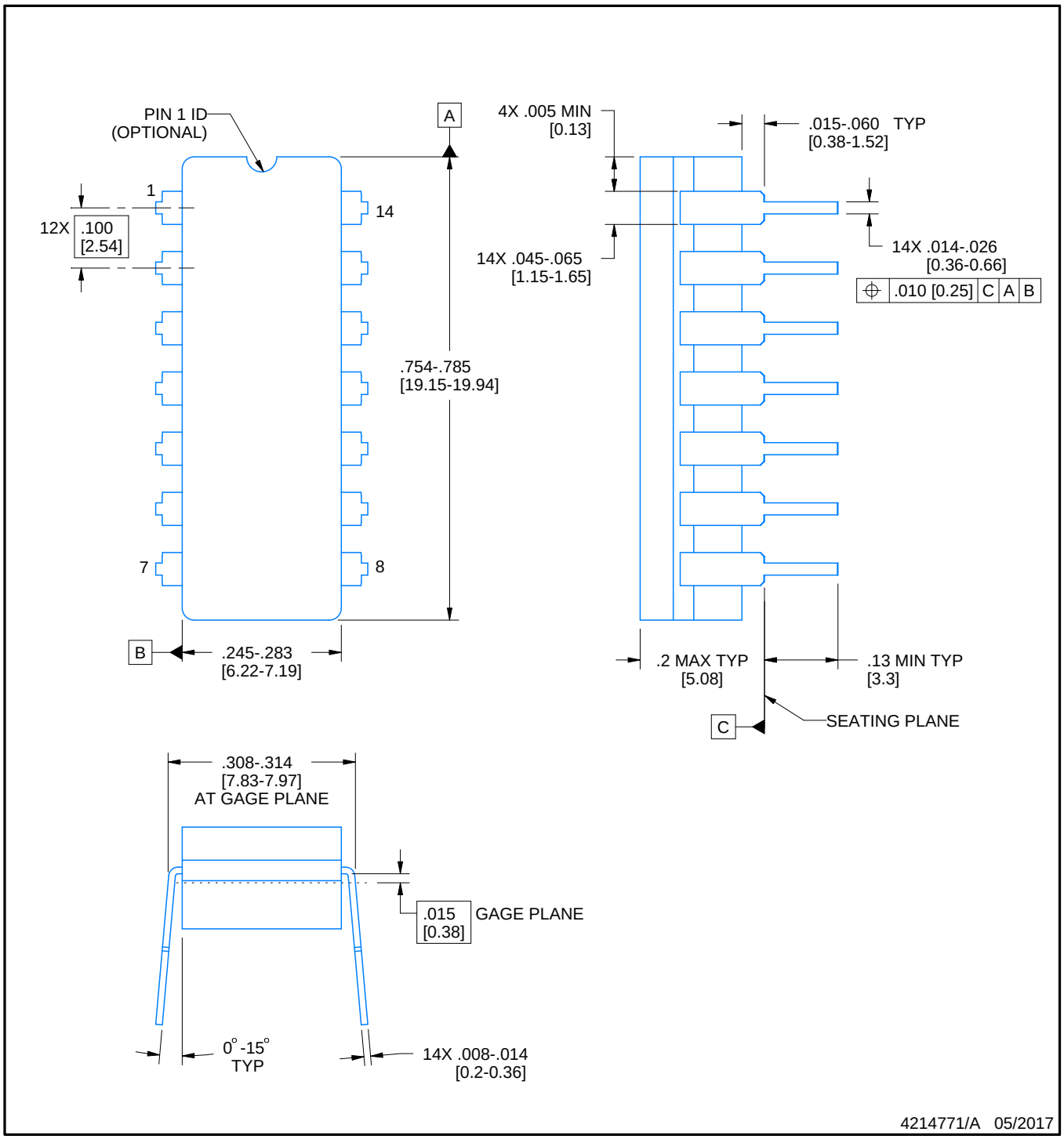


# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

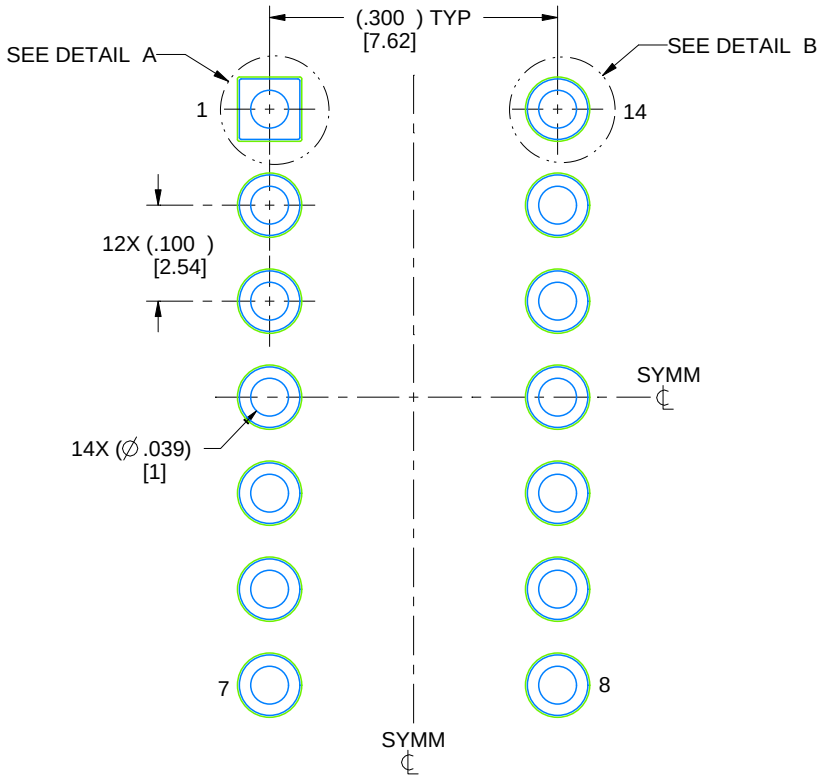
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

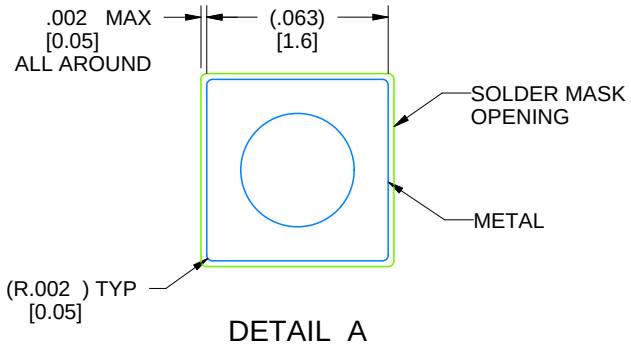
## J0014A

## CDIP - 5.08 mm max height

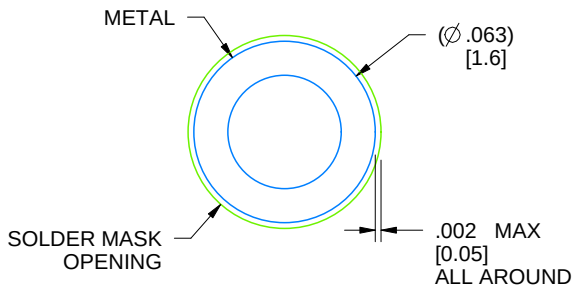
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X




DETAIL B
13X, SCALE: 15X

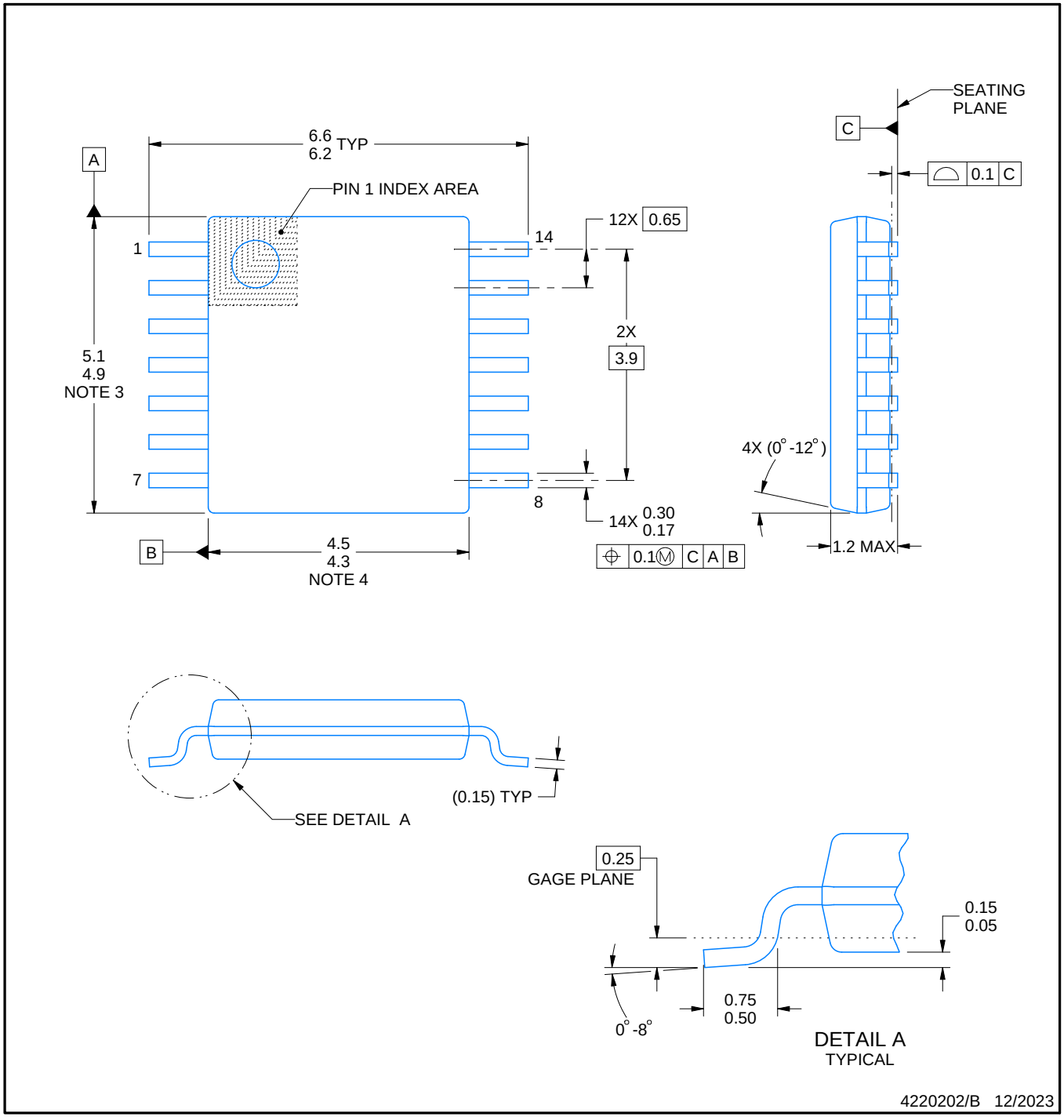
4214771/A 05/2017

# PACKAGE OUTLINE

## PW0014A

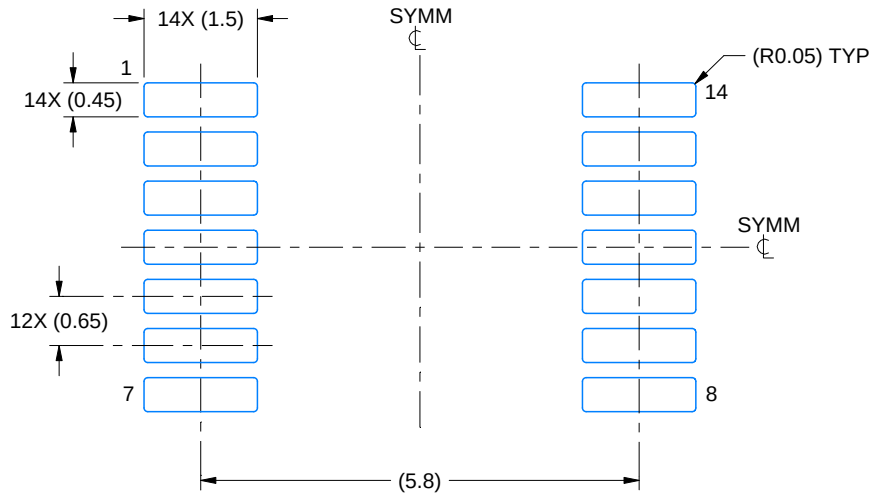
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

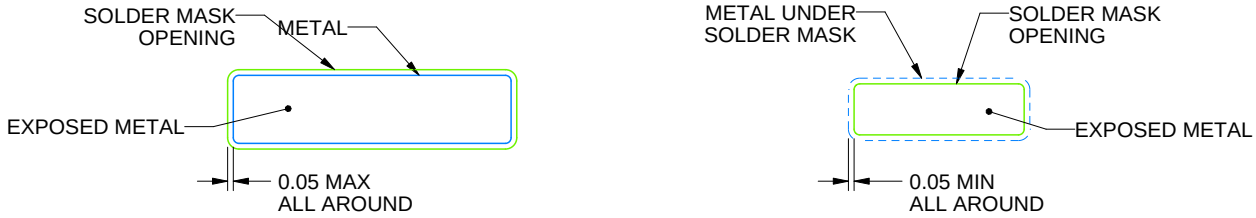



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

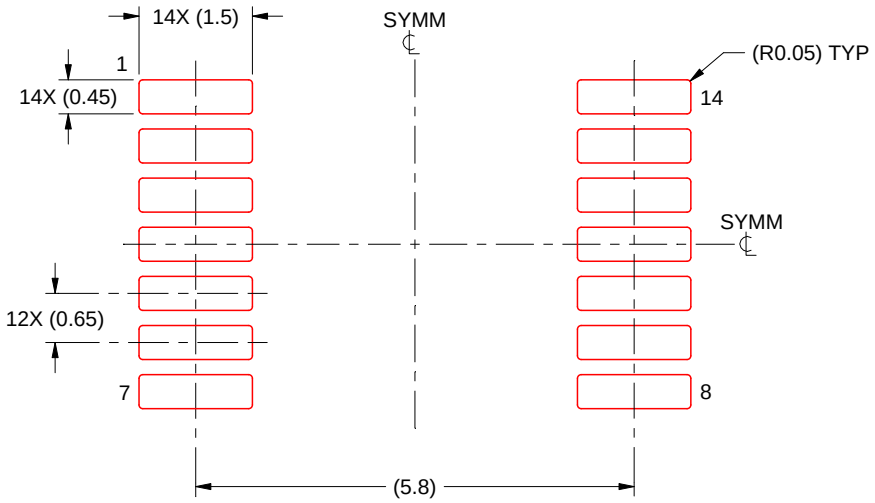



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月