

3.3-V ABT 16-Bit Buffers/Drivers With 3-State Outputs

Check for Samples: [SN54LVTH16244A](#), [SN74LVTH16244A](#)

FEATURES

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - **2000-V Human-Body Model (A114-A)**
 - **200-V Machine Model (A115-A)**

DESCRIPTION

The 'LVTH16244A devices are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

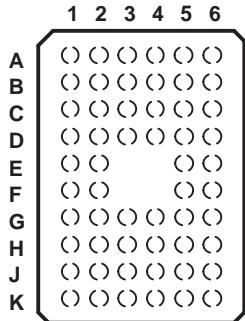


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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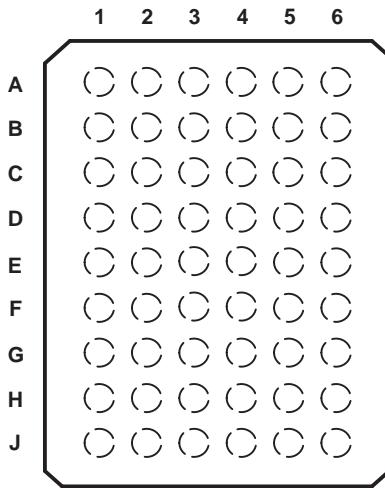
**SN54LVTH16244A... WD PACKAGE
SN74LVTH16244A... DGG, DGV, OR DL PACKAGE
(TOP VIEW)**

1	48	2	2
1Y1	47	1A1	
1Y2	46	1A2	
GND	45	GND	
1Y3	44	1A3	
1Y4	43	1A4	
V _{CC}	42	V _{CC}	
2Y1	41	2A1	
2Y2	40	2A2	
GND	39	GND	
2Y3	38	2A3	
2Y4	37	2A4	
3Y1	36	3A1	
3Y2	35	3A2	
GND	34	GND	
3Y3	33	3A3	
3Y4	32	3A4	
V _{CC}	31	V _{CC}	
4Y1	30	4A1	
4Y2	29	4A2	
GND	28	GND	
4Y3	27	4A3	
4Y4	26	4A4	
4	25	3	3

**GQL OR ZQL PACKAGE
(TOP VIEW)**

**TERMINAL ASSIGNMENTS⁽¹⁾
(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
A	1 \overline{OE}	NC	NC	NC	NC	2 \overline{OE}
B	1Y2	1Y1	GND	GND	1A1	1A2
C	1Y4	1Y3	V _{CC}	V _{CC}	1A3	1A4
D	2Y2	2Y1	GND	GND	2A1	2A2
E	2Y4	2Y3			2A3	2A4
F	3Y1	3Y2			3A2	3A1
G	3Y3	3Y4	GND	GND	3A4	3A3
H	4Y1	4Y2	V _{CC}	V _{CC}	4A2	4A1
J	4Y3	4Y4	GND	GND	4A4	4A3
K	4 \overline{OE}	NC	NC	NC	NC	3 \overline{OE}

(1) NC – No internal connection

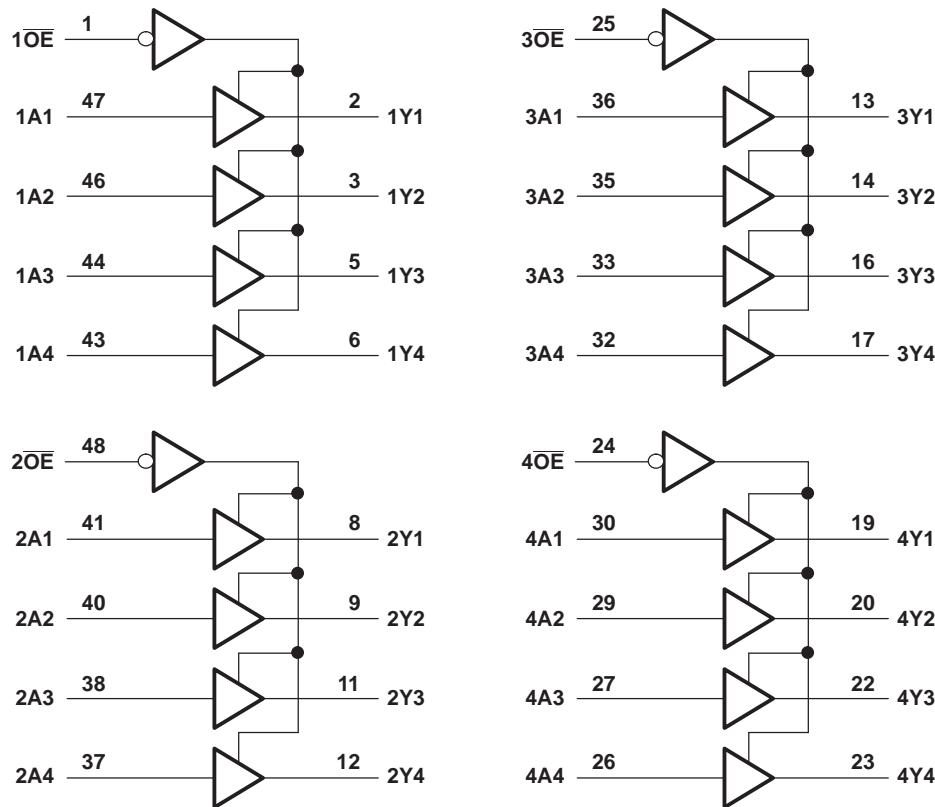
**GRD OR ZRD PACKAGE
(TOP VIEW)**

**TERMINAL ASSIGNMENTS⁽¹⁾
(54-Ball GRD/ZRD Package)**

	1	2	3	4	5	6
A	1Y1	NC	1 \overline{OE}	2 \overline{OE}	NC	1A1
B	1Y3	1Y2	NC	NC	1A2	1A3
C	2Y1	1Y4	V _{CC}	V _{CC}	1A4	2A1
D	2Y3	2Y2	GND	GND	2A2	2A3
E	3Y1	2Y4	GND	GND	2A4	3A1
F	3Y3	3Y2	GND	GND	3A2	3A3
G	4Y1	3Y4	V _{CC}	V _{CC}	3A4	4A1
H	4Y3	4Y2	NC	NC	4A2	4A3
J	4Y4	NC	4 \overline{OE}	3 \overline{OE}	NC	4A4

(1) NC – No internal connection

**FUNCTION TABLE
(EACH 4-BIT BUFFER)**

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)


Pin numbers shown are for the DGG, DGV, DL, and WD packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	4.6	V
V _I	Input voltage range ⁽²⁾	–0.5	7	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	7	V
V _O	Voltage range applied to any output in the high state ⁽²⁾	–0.5	V _{CC} + 0.5	V
I _O	Current into any output in the low state	SN54LVTH16244A	96	V
			128	
I _O	Current into any output in the high state ⁽³⁾	SN54LVTH16244A	48	V
			64	
I _{IK}	Input clamp current	V _I < 0	–50	mA
I _{OK}	Output clamp current	V _O < 0	–50	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DGG package	70	°C/W
		DGV package	58	
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
T _{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The current flows only when the output is in the high state and V_O > V_{CC}.
- (4) The package thermal impedance is calculated in accordance with JEDEC 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		SN54LVTH16244A		SN74LVTH16244A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		–25		–32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled	10	200	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate					μs/V
T _A	Operating free-air temperature	–55	125	–40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	SN54LVTH16244A			–40°C to 85°C SN74LVTH16244A			Recommended –40°C to 125°C SN74LVTH16244A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7 \text{ V}$ to 3.6 V, $I_{OL} = -100 \mu\text{A}$	$V_{CC} - 0.2$			$V_{CC} - 0.2$			$V_{CC} - 0.2$			V
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			2.4			
	$V_{CC} = 3 \text{ V}$, $I_{OH} = -24 \text{ mA}$	2						2		2	
V_{OL}	$V_{CC} = 2.7 \text{ V}$, $I_{OL} = 100 \mu\text{A}$		0.2		0.2			0.2			V
	$I_{OL} = 24 \text{ mA}$		0.5		0.5			0.5			
	$I_{OL} = 16 \text{ mA}$		0.4		0.4			0.4			
	$I_{OL} = 32 \text{ mA}$		0.5		0.5			0.5			
	$I_{OL} = 48 \text{ mA}$		0.55								
	$I_{OL} = 64 \text{ mA}$				0.55			0.55			
	$V_{CC} = 0$ or 3.6 V, $V_I = 5.5 \text{ V}$		50		10			10			
I_I	Control inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$ or GND		±1	±1			±1			μA
		$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$		1		1		1			
	Data inputs	$V_I = 0$		-5		-5		-5			
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0$ to 4.5 V			±100			±100				μA
$I_{(hold)}$	Data inputs	$V_{CC} = 3 \text{ V}$, $V_I = 0.8 \text{ V}$	75		75			75			μA
		$V_I = 2 \text{ V}$	-75		-75			-75			
		$V_{CC} = 3.6 \text{ V}$ ⁽²⁾ , $V_I = 0$ to 3.6 V			500			500			μA
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$		5		5			5			μA
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$		-5		-5			-5			μA
I_{OZPU}	$V_{CC} = 0$ to 1.5 V, $V_O = 0.5 \text{ V}$ to 3 V, \overline{OE} = don't care		±100 ⁽³⁾		±100			±100			μA
I_{OZPD}	$V_{CC} = 1.5 \text{ V}$ to 0, $V_O = 0.5 \text{ V}$ to 3 V, \overline{OE} = don't care		±100 ⁽³⁾		±100			±100			μA
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high	0.19		0.19			0.19			mA
		Outputs low	5		5			5			
		Outputs disabled	0.19		0.19			0.19			
$\Delta I_{CC}^{(4)}$	$V_{CC} = 3 \text{ V}$ to 3.6 V, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND		0.2		0.2			0.2			mA
C_I	$V_I = 3 \text{ V}$ or 0 V		4		4			4			pF
C_O	$V_O = 3 \text{ V}$ or 0 V		9		9			9			pF

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.
 (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
 (3) On products compliant to MIL-PRF-38535, this parameter does not apply.
 (4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

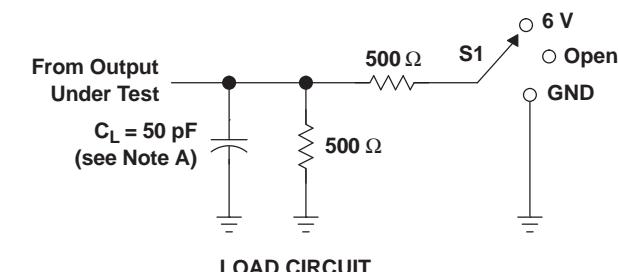
SWITCHING CHARACTERISTICS

over recommended operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see [Figure 1](#))⁽¹⁾

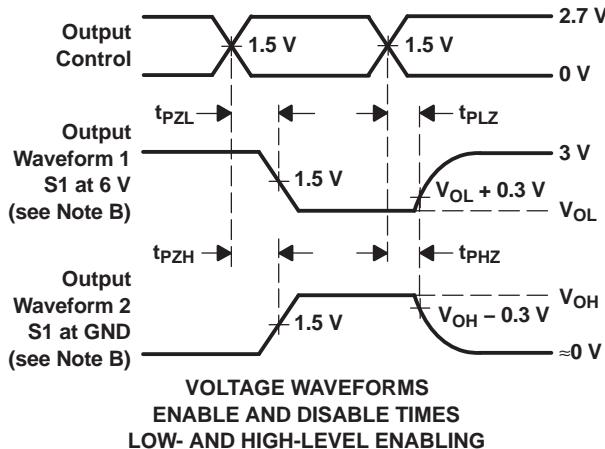
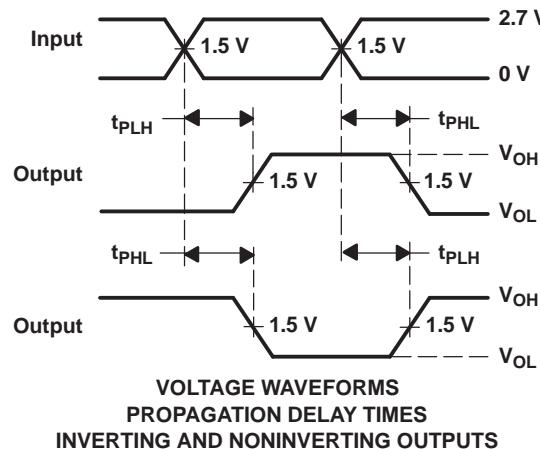
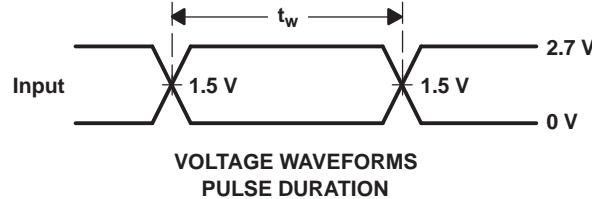
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16244A		–40°C to 85°C SN74LVTH16244A			Recommended –40°C to 125°C SN74LVTH16244A					UNIT	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.1	4.4	4.6	1.2	2.3	3.2		3.7	1.2	2.3	4.4	4.6
t_{PHL}			1.1	3.6	3.9	1.2	2	3.2		3.7	1.2	2	3.6	3.9
t_{PZH}	\overline{OE}	Y	1.1	4.6	5.4	1.2	2.6	4		5	1.2	2.6	4.6	5.4
t_{PZL}			1.1	5.4	6.2	1.2	2.7	4		5	1.2	2.7	5.4	6.2
t_{PHZ}	\overline{OE}	Y	1.6	5.7	6.2	2.2	3.3	4.5		5	2.2	3.3	5.7	6.2
t_{PLZ}			1.2	5	4.7	2	3.1	4.2		4.4	2	3.1	5	4.7
$t_{sk(LH)}$								0.5				0.5		ns
$t_{sk(HL)}$								0.5				0.5		

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
- The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision T (November 2006) to Revision U	Page
• Updated document to new TI data sheet format - no specification changes.	1
• Removed ordering information.	1
• Updated operating temperature range.	5

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9668501QXA	Active	Production	CFP (WD) 48	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9668501QX A SNJ54LVTH16244 AWD
5962-9668501VXA	Active	Production	CFP (WD) 48	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9668501VX A SNV54LVTH16244 AWD
74LVTH16244ADGGRE4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A
74LVTH16244ADGGRG4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A
74LVTH16244ADGVRG4	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LL244A
74LVTH16244ADGVRG4.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LL244A
74LVTH16244ADLR1G4	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A
74LVTH16244ADLR1G4.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A
SN74LVTH16244ADGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A
SN74LVTH16244ADGGR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A
SN74LVTH16244ADGVR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LL244A
SN74LVTH16244ADGVR.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LL244A
SN74LVTH16244ADL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A
SN74LVTH16244ADL.B	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A
SN74LVTH16244ADLG4	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A
SN74LVTH16244ADLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A
SN74LVTH16244ADLR.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVTH16244A
SNJ54LVTH16244AWD	Active	Production	CFP (WD) 48	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9668501QX A SNJ54LVTH16244 AWD

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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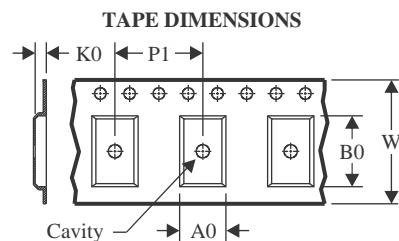
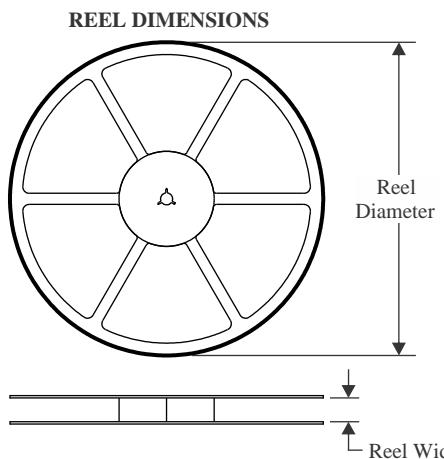
OTHER QUALIFIED VERSIONS OF SN54LVTH16244A, SN54LVTH16244A-SP, SN74LVTH16244A :

- Catalog : [SN74LVTH16244A](#), [SN54LVTH16244A](#)
- Enhanced Product : [SN74LVTH16244A-EP](#), [SN74LVTH16244A-EP](#)
- Military : [SN54LVTH16244A](#)
- Space : [SN54LVTH16244A-SP](#)

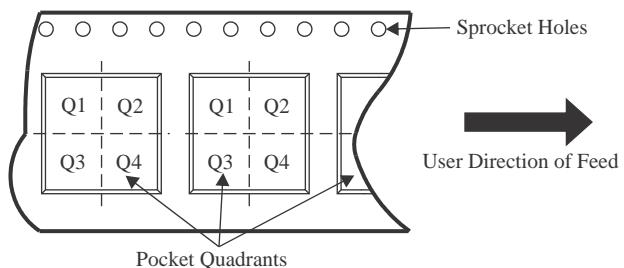
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

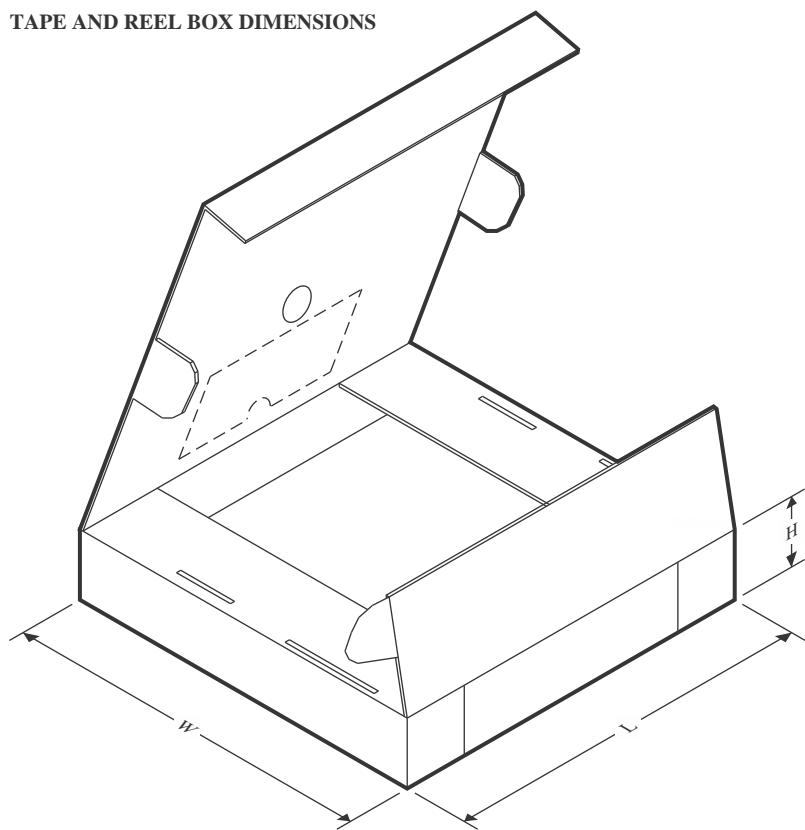
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


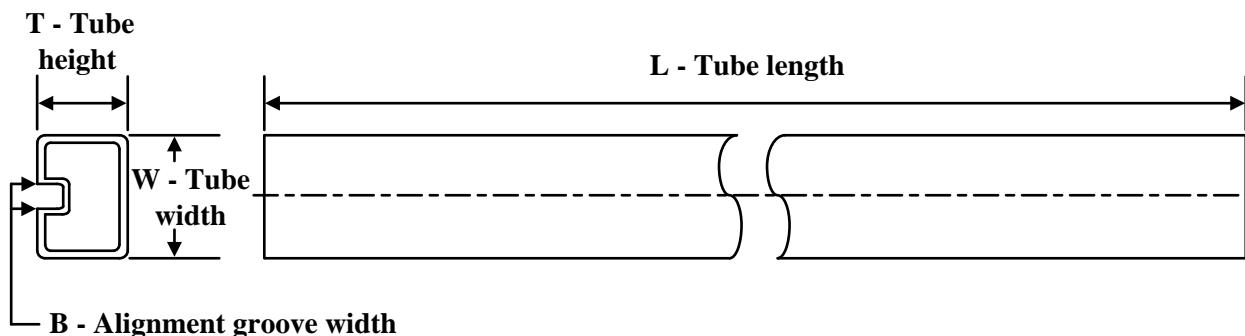
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVTH16244ADGVRG4	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
74LVTH16244ADLR1G4	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVTH16244ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH16244ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVTH16244ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVTH16244ADGVRG4	TVSOP	DGV	48	2000	353.0	353.0	32.0
74LVTH16244ADLR1G4	SSOP	DL	48	1000	356.0	356.0	53.0
SN74LVTH16244ADGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74LVTH16244ADGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74LVTH16244ADLR	SSOP	DL	48	1000	356.0	356.0	53.0

TUBE


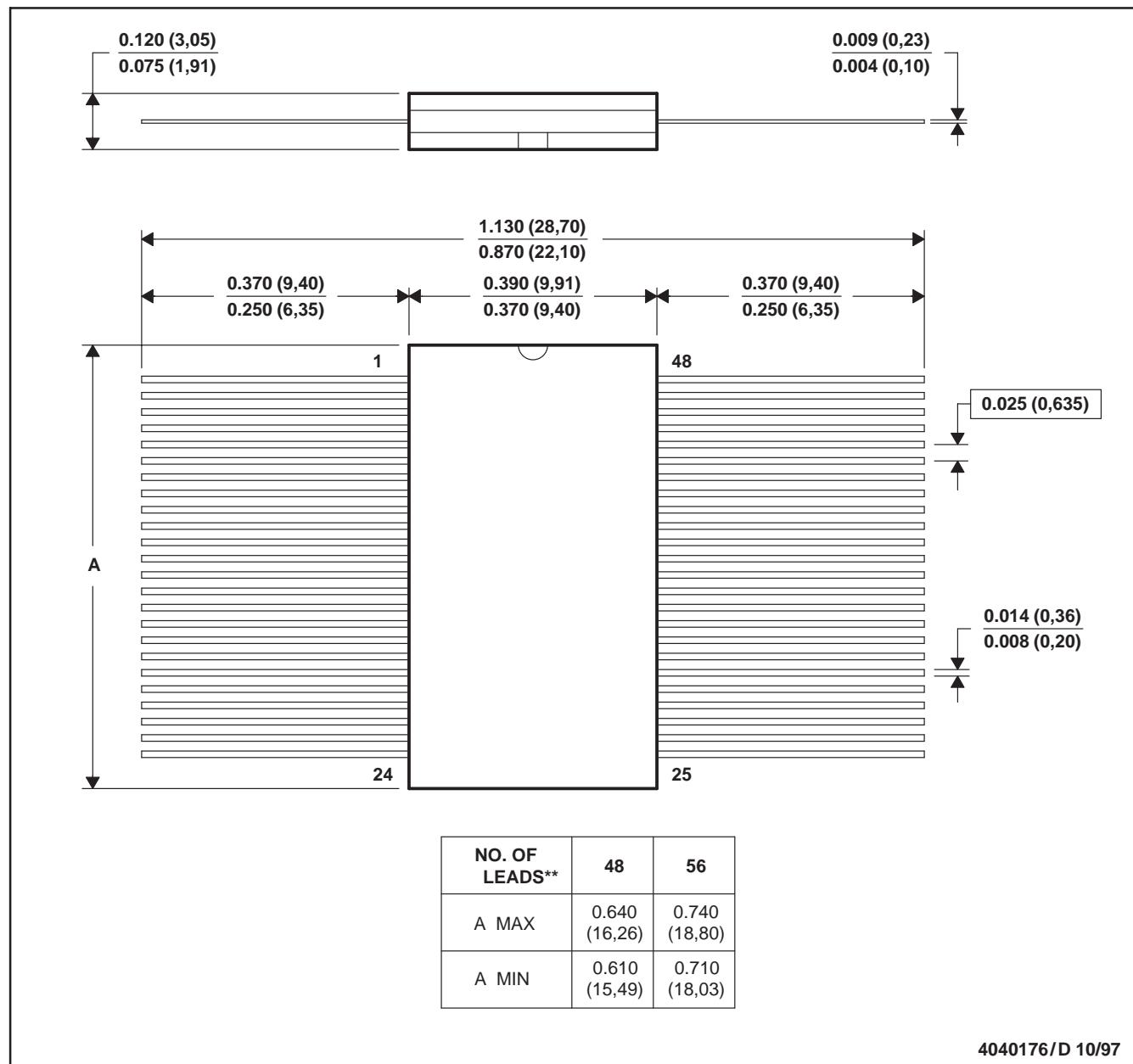
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
SN74LVTH16244ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74LVTH16244ADL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74LVTH16244ADLG4	DL	SSOP	48	25	473.7	14.24	5110	7.87

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

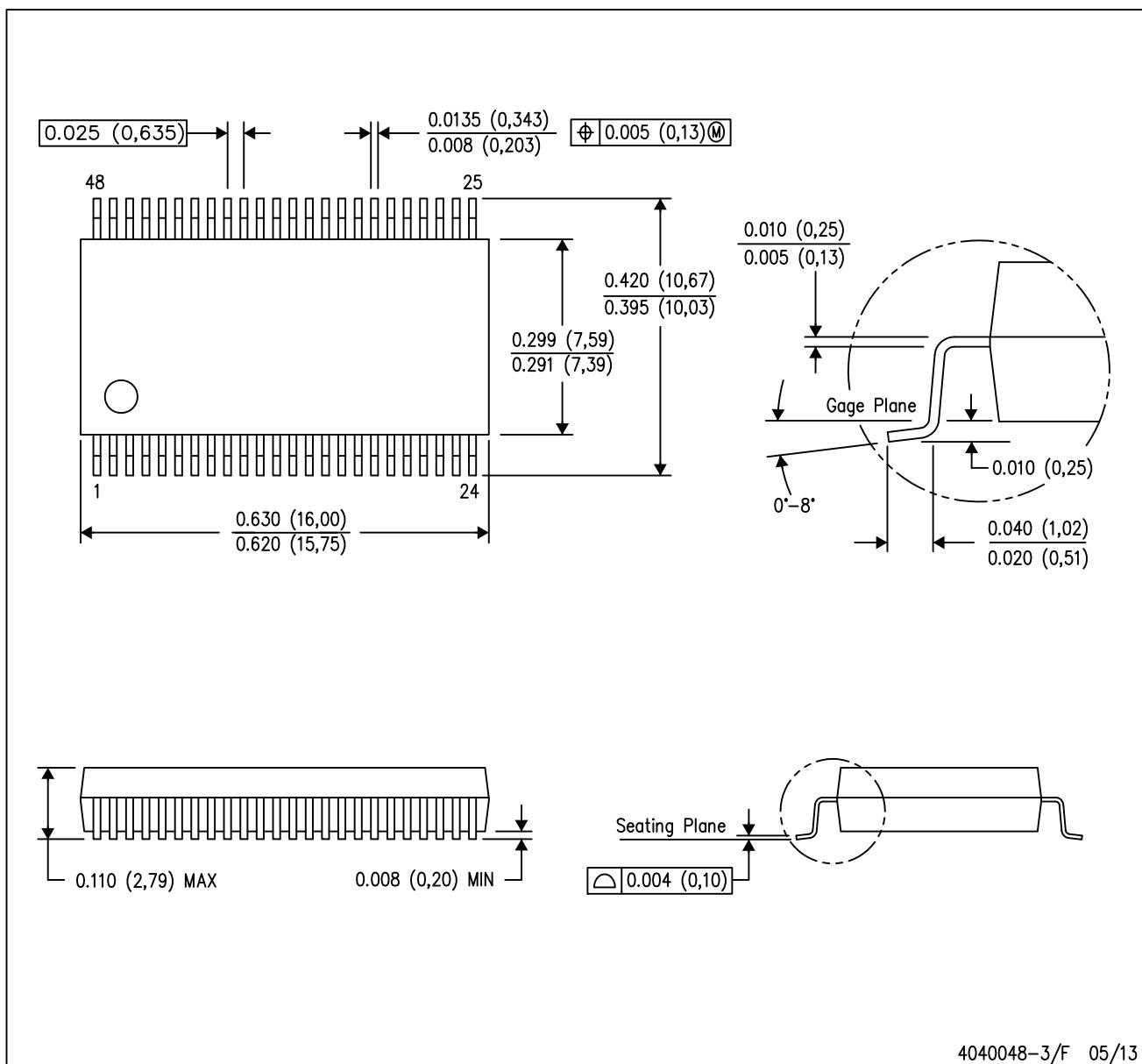
48 LEADS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



4040048-3/F 05/13

NOTES:

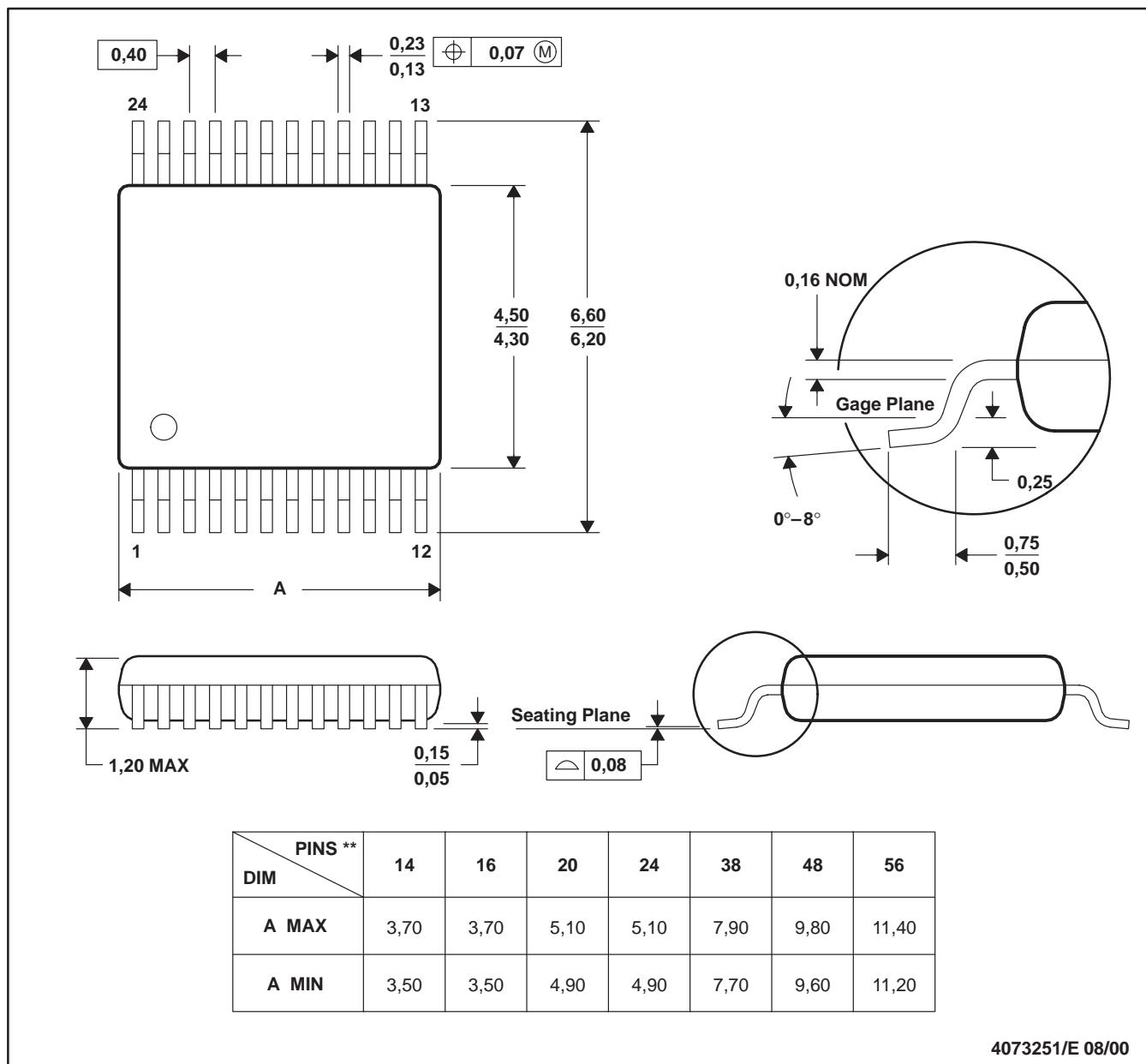
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

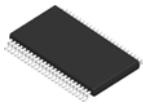
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

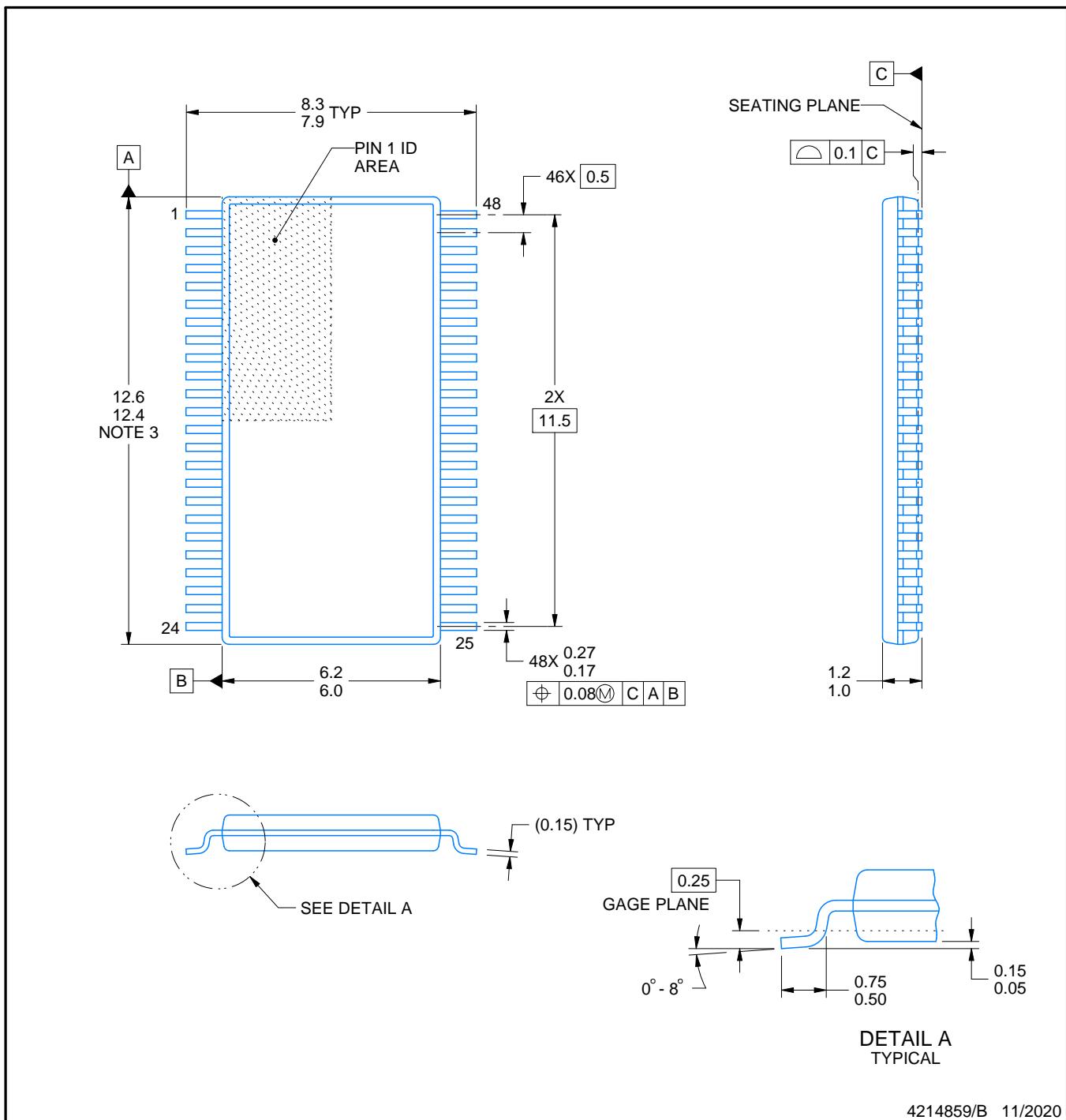
PACKAGE OUTLINE

DGG0048A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

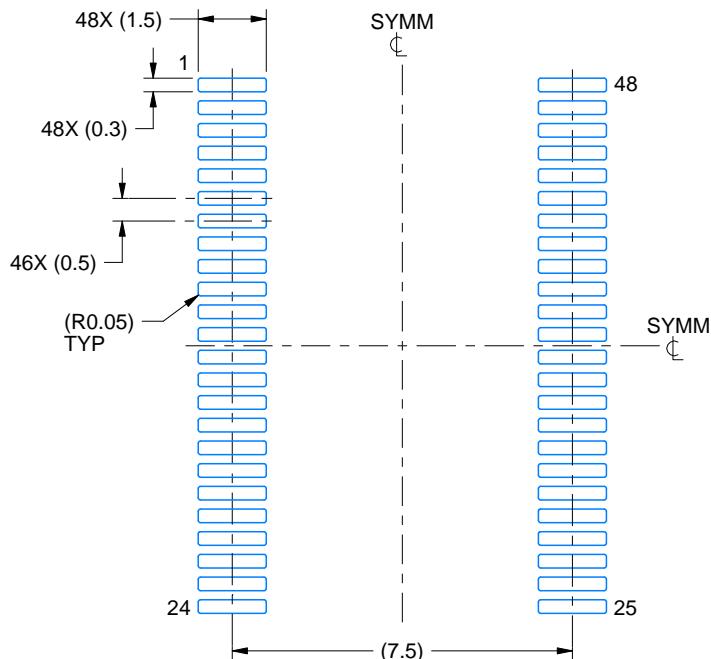
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

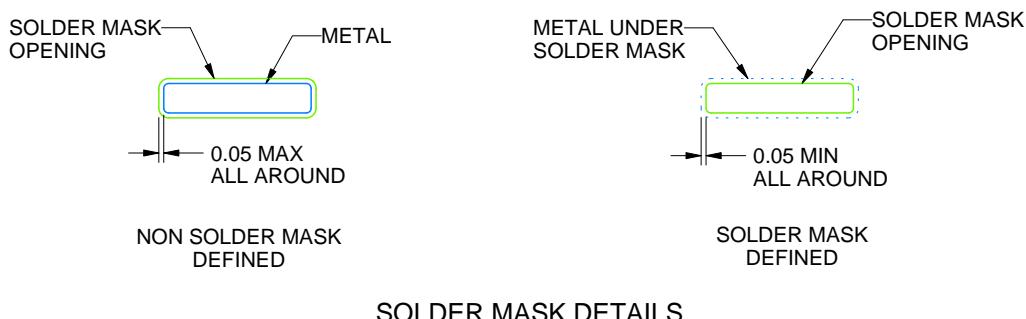
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

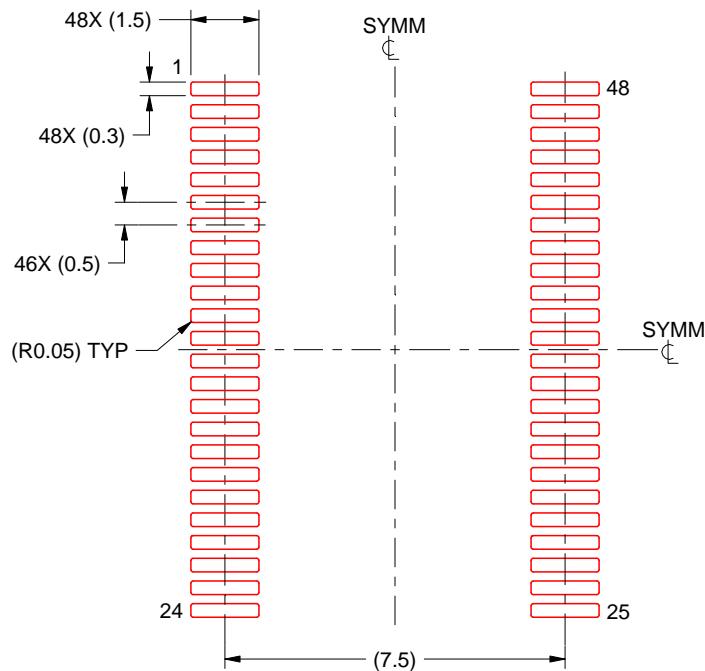
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

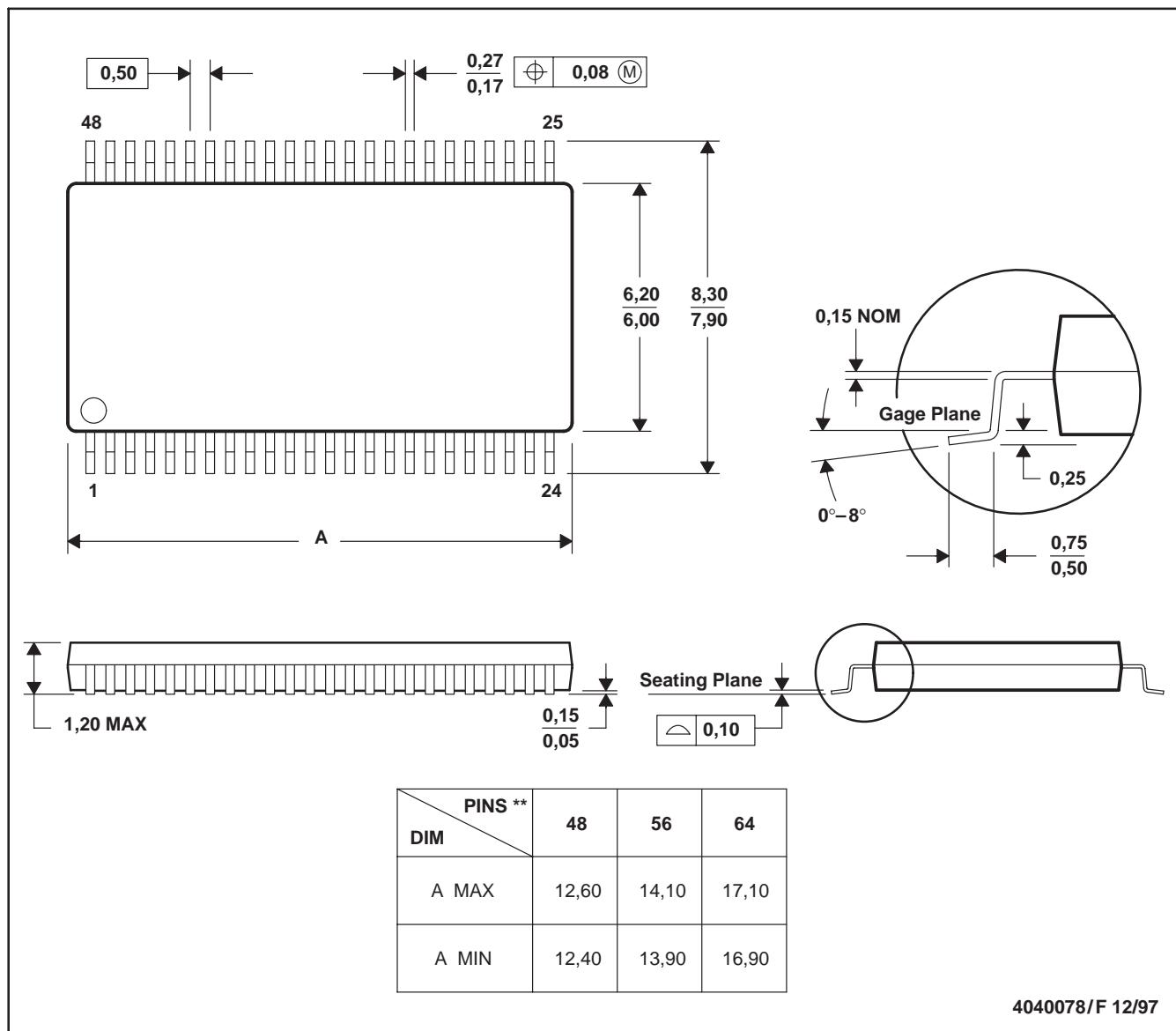
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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