4096 × 18 DSP-SYNC™ 先进先出存储器

查询样品: SN74V245-EP

特性

- **4096 × 18** 位组织阵列
- **7.5ns** 读取和写入周期时间
- **3.3V VCC，5V** 输入耐受
- 首字或标准直通时序
- 单一或双寄存器缓冲的空和满标志
- 可轻松扩展深度和宽度
- 异步或同步读取和写入时钟
- 带有缺省设置的异步或同步可编程几乎空和近满标志
- 半满标志功能
- 输出使能将输出数据总线置于高阻抗状态
- 高性能亚微米 **CMOS** 技术
- **DSP** 和微控制器接口控制逻辑
- 提供一个到德州仪器 **(TI) TMS320™ DSP** 的 **DSP** 无粘结接口
- ，此 **DSP** 封装在 **64** 引脚薄型四方扁平封装

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装和测试场所
- 一个制造场所
- 支持军用（**-55°C** 至 **125°C**）温度范围
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

说明/订购信息

SN74V245 是一款超高速、低功耗 CMOS 计时先进先出 (FIFO) 存储器。 它支持高达 133MHz 的时钟频率并且具有 5ns 的快速读取访问时间。 这个 DSP 同步 FIFO 存储器特有针对应用中使用的读取和访问控制，例如 DSP 到处理器通信，DSP 到模拟前端 (AFE) 缓冲，网络，视频和数据通信。

SN74V245 是一款同步 FIFO，这表示每个端口采用一个同步接口。 所有通过端口传输的数据被选通至由使能引脚计时的连续（自由运行）端口的低到高转换。 针对每个端口的连续时钟相互独立并可异步或同步。 可对每个端口的启用进行设置以在 DSP，微控制器和/或由一个同步接口控制的总线之间提供一个简单接口。 一个输出使能 ($\overline{OE}$) 输入控制 3 态输出。

同步 FIFO 有两个固定标志、空标志/输出就绪 ($\overline{EF}$/$\overline{OR}$) 和满标志/输入就绪 ($\overline{FF}$/$\overline{IR}$)，和两个可编程标志，几乎空 ($\overline{PAE}$) 和近满 ($\overline{PAF}$)。 可编程标志的偏移负载由一个简单状态机控制并通过将负载引脚 ($\overline{LD}$) 置为有效来启动。 当 FIFO 被用于单器件配置时，一个半满标志 ($\overline{HF}$) 可用。

SN74V245 可使用两个时序运行模式：首字直通 (FWFT) 模式和标准模式。

在 FWFT 模式中，被写入一个空 FIFO 的首字在 RCLK 信号的三次转换后被直接计时至数据输出线路。 不必将一个读取使能 ($\overline{REN}$) 置为有效来访问首字。

在标准模式中，被写入到空 FIFO 的首字并不出现在输出输出线路上，除非执行了一个特定的读取操作。 一个包含激活$\overline{REN}$并启用一个上升 RCLK 边沿的读取操作将把字从内部存储器移动至数据输出线路。

通过使用菊花链技术或 FWFT 模式，SN74V245 的深度是可扩展的。 $\overline{XI}$和$\overline{XO}$引脚被用于扩展 FIFO。 在深度扩展模式配置中，第一个器件上的首次载入 ($\overline{FL}$) 被接地并且针对菊花链上的所有其它器件被设定为高电平。

SN74V245 额定工作温度 -55°C 至 125°C。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

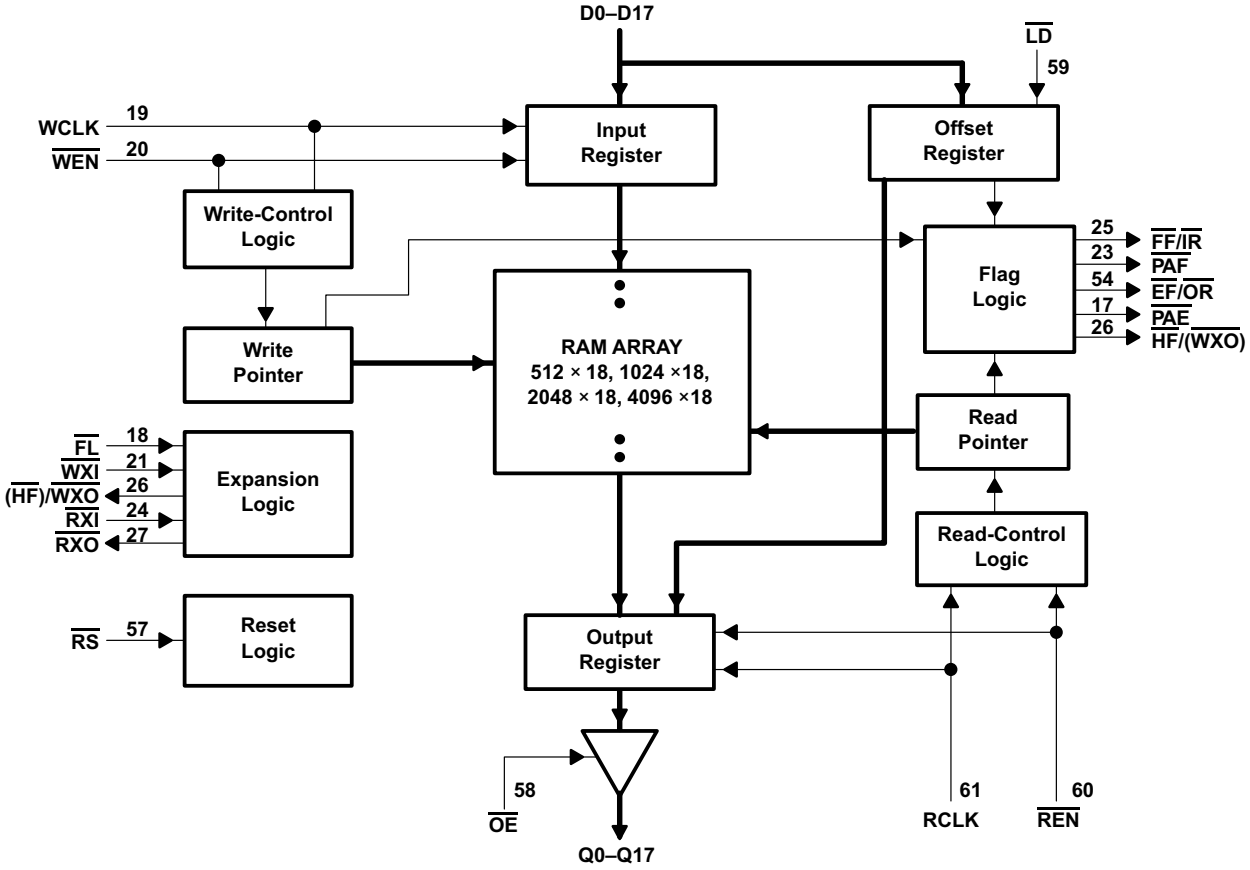
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	64-pin TQFP (PAG)	SN74V245-15PAGEP	V245-15EP	V62/13606-01XE

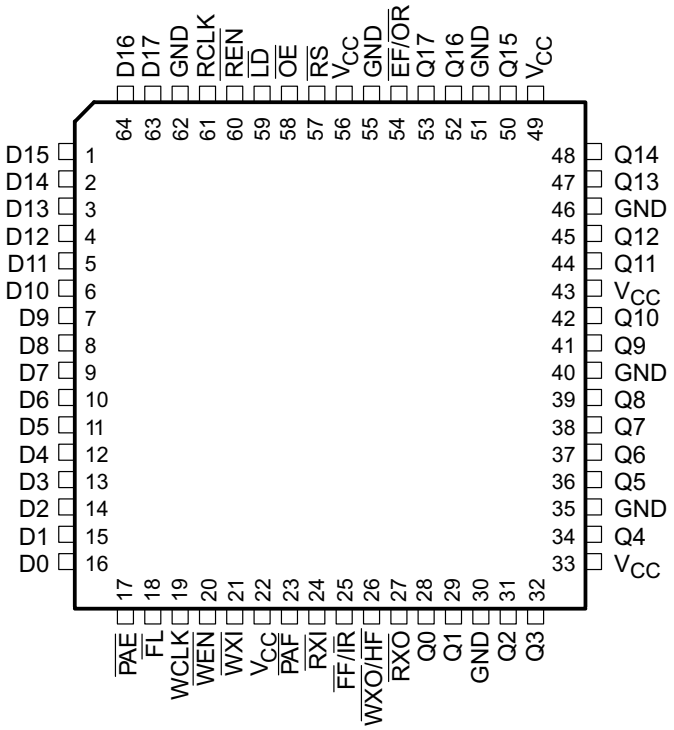
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTIONAL BLOCK DIAGRAM



DEVICE INFORMATION

PAG PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
D0–D17	1-16, 63, 64	I	Data inputs. Data inputs for an 18-bit bus.
$\overline{EF}/\overline{OR}$	54	O	Memory-empty/valid-data-available flag. In the standard mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether the FIFO memory is empty. In FWFT mode, the $\overline{OR}$ function is selected. $\overline{OR}$ indicates whether there is valid data available at the outputs.
$\overline{FF}/\overline{IR}$	25	O	Memory-full/space-available flag. In the standard mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether the FIFO memory is full. In the FWFT mode, the $\overline{IR}$ function is selected. $\overline{IR}$ indicates whether there is space available for writing to the FIFO memory.
$\overline{FL}$	18	I	Mode selection. In the single-device or width-expansion configuration, $\overline{FL}$, together with $\overline{WXI}$ and $\overline{RXI}$, determines if the mode is standard mode or first-word fall-through (FWFT) mode, as well as whether the $\overline{PAE}/\overline{PAF}$ flags are synchronous or asynchronous (see Table 5). In the daisy-chain depth-expansion configuration, $\overline{FL}$ is grounded on the first device (first-load device) and set to high for all other devices in the daisy chain.
GND	30, 35, 40, 46, 51, 55, 62		Ground
$\overline{LD}$	59	I	Read/write control. When $\overline{LD}$ is low, data on the inputs D0–D11 is written to the offset and depth registers on the low-to-high transition of the WCLK, when $\overline{WEN}$ is low. When $\overline{LD}$ is low, data on the outputs Q0–Q11 is read from the offset and depth registers on the low-to-high transition of RCLK when $\overline{REN}$ is low.
$\overline{OE}$	58	I	Output enable. When $\overline{OE}$ is low, the data output bus is active. If $\overline{OE}$ is high, the output data bus is in the high-impedance state.
$\overline{PAE}$	17	O	Programable almost-empty flag. When $\overline{PAE}$ is low, the FIFO is almost empty, based on the offset programmed into the FIFO. The default offset at reset is 127 from empty.
$\overline{PAF}$	23	O	Programable almost-full flag. When $\overline{PAF}$ is low, the FIFO is almost full, based on the offset programmed into the FIFO. The default offset at reset is 127 from full.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Q0–Q17	28, 29, 31, 32, 34, 36–39, 41, 42, 44, 45, 47, 48, 50, 52, 53	O	Data outputs. Data outputs for an 18-bit bus.
RCLK	61	I	Read clock. When $\overline{REN}$ is low, data is read from the FIFO on a low-to-high transition of RCLK, if the FIFO is not empty.
$\overline{REN}$	60	I	Read enable. When $\overline{REN}$ is low, data is read from the FIFO on every low-to-high transition of RCLK. When $\overline{REN}$ is high, the output register holds the previous data. Data is not read from the FIFO if $\overline{EF}$ is low.
$\overline{RS}$	57	I	Reset. When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial write after power up.
$\overline{RXI}$	24	I	Read expansion. In the single-device or width-expansion configuration, $\overline{RXI}$, together with $\overline{FL}$ and $\overline{WXI}$, determines if the mode is standard mode or FWFT mode, as well as whether the $\overline{PAE}$/$\overline{PAF}$ flags are synchronous or asynchronous (see Table 5). In the daisy-chain depth-expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (read expansion out) of the previous device.
$\overline{RXO}$	27	O	Last-location-read flag. In the depth-expansion configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
V_{CC}	22, 33, 43, 49, 56		Supply voltage. +3.3-V power-supply pins.
WCLK	19	I	Write clock. When $\overline{WEN}$ is low, data is written into the FIFO on a low-to-high transition of WCLK if the FIFO is not full.
$\overline{WEN}$	20	I	Write enable. When $\overline{WEN}$ is low, data is written into the FIFO on every low-to-high transition of WCLK. When $\overline{WEN}$ is high, the FIFO holds the previous data. Data is not written into the FIFO if $\overline{FF}$ is low.
$\overline{WXI}$	21	I	Width expansion. In the single-device or width-expansion configuration, $\overline{WXI}$, together with $\overline{FL}$ and $\overline{RXI}$, determines if the mode is standard mode or FWFT mode, as well as whether the $\overline{PAE}$/$\overline{PAF}$ flags are synchronous or asynchronous (see Table 5). In the daisy-chain depth-expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (write expansion out) of the previous device.
$\overline{WXO}$/$\overline{HF}$	26	O	Half-full flag. In the single-device or width-expansion configuration, the device is more than half full when $\overline{HF}$ is low. In the depth-expansion configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device when the last location in the FIFO is written.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	VALUE
Supply voltage range, V_{CC}	–0.5 V to 5 V
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Maximum junction temperature, Tj	150°C
Storage temperature range, T_{stg}	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		5	V
V_{IL}	Low-level input voltage			0.8	V
T_J	Operating junction temperature	–55		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

THERMAL INFORMATION

THERMAL METRIC(1)		SN74V245 PAG 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	46.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	5.8	
θ_{JB}	Junction-to-board thermal resistance(4)	19.7	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	19.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	

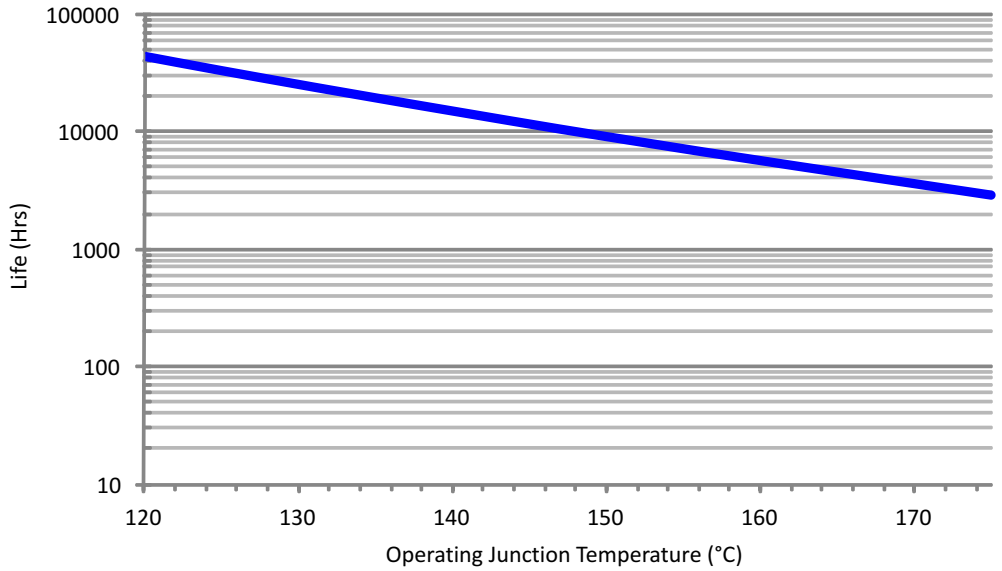
(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(6) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 3 V, I_{OH} = -2 mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 3 V, I_{OL} = 8 mA			0.4	V
I_I	Input current	V_{CC} = 3.6 V, V_I = V_{CC} to 0.4 V			±1	µA
I_{OZ}	High-impedance output current	V_{CC} = 3.6 V, $\overline{OE} \geq V_{IH}$, V_O = V_{CC} to 0.4 V			±10	µA
I_{CC1}	Supply current	V_{CC} = 3.3 V, See (1), (2) and (3)			35	mA
I_{CC2}		V_{CC} = 3.6 V, See (1) and (4)			5	mA
C_{IN}	Input capacitance	V_I = 0, T_A = 25°C, f = 1 MHz		10		pF
C_{OUT}		V_O = 0, T_A = 25°C, f = 1 MHz, Output deslected, ($\overline{OE} \geq V_{IH}$)		10		pF

(1) Tested with outputs disabled (I_{OUT} = 0).
(2) RCLK and WCLK switch at 20 MHz and data inputs switch at 10 MHz.
(3) Typical I_{CC1} = 2.04 + 0.88 × f_{SW} + 0.02 × CL × f_{SW} (in mA). These equations are valid under the following conditions: V_{CC} = 3.3 V, T_A = 25°C, f_{SW} = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at f_{SW}/2, C_L = capacitive load (in pF).
(4) All inputs = (V_{CC} – 0.2 V) or (GND + 0.2 V), except RCLK and WCLK, which switch at 20 MHz.



(1) See datasheet for absolute maximum and minimum recommended operating conditions.
(2) Silicon operating life design goal is 100,000 hrs at 106°C junction temperature (does not include package interconnect life).
(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

Figure 1. Electromigration Fail Mode Derating Chart

TIMING REQUIREMENTS

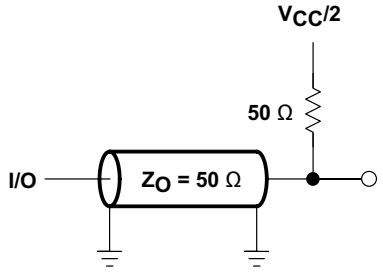
		MIN	MAX	UNIT
f_{clock}	Clock cycle frequency		66.7	MHz
t_A	Data access time	1	11	ns
t_{CLK}	Clock cycle time	16		ns
t_{CLKH}	Clock high time	7		ns
t_{CLKL}	Clock low time	7		ns
t_{DS}	Data setup time	5		ns
t_{DH}	Data hold time	2		ns
t_{ENS}	Enable setup time	5		ns
t_{ENH}	Enable hold time	2		ns
t_{LDS}	Load setup time	5		ns
t_{LDH}	Load hold time	2		ns
t_{RS}	Reset pulse width(1)	16		ns
t_{RSS}	Reset setup time	10.5		ns
t_{RSR}	Reset recovery time	10.5		ns
t_{RSF}	Reset to flag and output time		16	ns
t_{OLZ}	Output enable to output in low Z	0		ns
t_{OE}	Output enable to output valid	1.5	9	ns
t_{OHZ}	Output enable to output in high Z	1.5	9	ns
t_{WFF}	Write clock to Full flag		11	ns
t_{REF}	Read clock to Empty flag		11	ns
t_{PAFA}	Clock to asynchronous programmable Almost-Full flag		21	ns
t_{PAFS}	Write clock to synchronous programmable Almost-Full flag		11	ns
t_{PAEA}	Clock to asynchronous programmable Almost-Empty flag		21	ns
t_{PAES}	Read clock to synchronous programmable Almost-Empty flag		11	ns
t_{HF}	Clock to Half-Full flag		21	ns
t_{XO}	Clock to expansion out		11	ns
t_{XI}	Expansion in pulse duration	7		ns
t_{XIS}	Expansion in setup time	6		ns
t_{SKEW1}	Skew time between read clock and write clock for $\overline{FF}/\overline{IR}$ and $\overline{EF}/\overline{OR}$	6.5		ns
t_{SKEW2}	Skew time between read clock and write clock for $\overline{PAE}$ and $\overline{PAF}$ (synchronous only)	18.5		ns

(1) Pulse durations less than minimum values are not allowed.

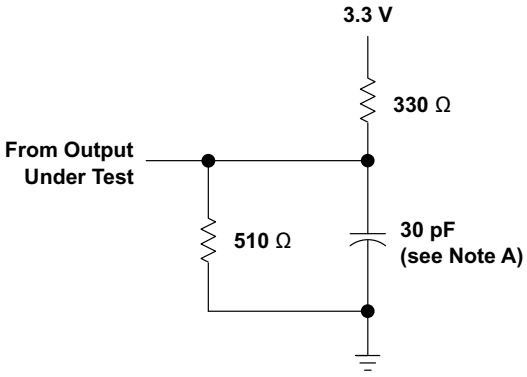
PARAMETER MEASUREMENT INFORMATION

AC TEST CONDITIONS

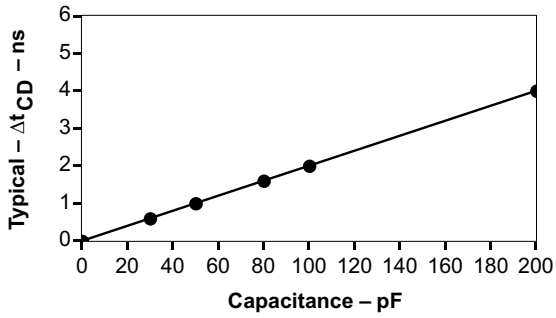
Input Pulse Levels	GND to 3.0 V
Input Rise/Fall Times	3 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load for t_{CLK} = 10 ns, 15 ns	See A
Output Load for t_{CLK} = 7.5 ns	See B and C



B. AC TEST LOAD FOR 7.5 SPEED GRADE



A. OUTPUT LOAD CIRCUIT FOR 10, 15, AND 20 SPEED GRADES



C. LUMPED CAPACITIVE LOAD, TYPICAL DERATING

A. Includes probe and jig capacitance

Figure 2. Load Circuits

DETAILED DESCRIPTION

INPUTS:

DATA IN (D0–D17)

Data inputs for 18-bit-wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished when $\overline{RS}$ is taken low. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The half-full flag ($\overline{HF}$) and programmable almost-full flag ($\overline{PAF}$) is reset to high after t_{RSF}. The programmable almost-empty flag (PAE) is reset to low after t_{RSF}. The full flag ($\overline{FF}$) resets to high. The empty flag ($\overline{EF}$) resets to low in standard mode, but resets to high in FWFT mode. During reset, the output register is initialized to all zeros, and the offset registers are initialized to their default values.

WRITE CLOCK (WCLK)

A write cycle is initiated on the low-to-high transition of WCLK. Data setup and hold times must be met with respect to the low-to-high transition of WCLK.

The write and read clocks can be asynchronous or coincident.

WRITE ENABLE ($\overline{WEN}$)

When $\overline{WEN}$ is low, data can be loaded into the FIFO RAM array on the rising edge of every WCLK cycle if the device is not full. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When $\overline{WEN}$ is high, no new data is written in the RAM array on each WCLK cycle.

To prevent data overflow in the standard mode, $\overline{FF}$ goes low, inhibiting further write operations. Upon completion of a valid read cycle, $\overline{FF}$ goes high, allowing a write to occur. The $\overline{FF}$ flag is updated on the rising edge of WCLK.

To prevent data overflow in the FWFT mode, $\overline{IR}$ goes high, inhibiting further write operations. Upon completion of a valid read cycle, $\overline{IR}$ goes low, allowing a write to occur. The $\overline{IR}$ flag is updated on the rising edge of WCLK.

$\overline{WEN}$ is ignored when the FIFO is full in either FWFT or standard mode.

READ CLOCK (RCLK)

Data can be read on the outputs on the low-to-high transition of RCLK when $\overline{OE}$ is low.

The write and read clocks can be asynchronous or coincident.

READ ENABLE ($\overline{REN}$)

When $\overline{REN}$ is low, data is loaded from the RAM array into the output register on the rising edge of every RCLK cycle if the device is not empty.

When $\overline{REN}$ is high, the output register holds the previous data and no new data is loaded into the output register. Data outputs Q0–Qn maintain the previous data value.

In the standard mode, every word accessed at Qn, including the first word written to an empty FIFO, must be requested using $\overline{REN}$. When the last word has been read from the FIFO, the empty flag ($\overline{EF}$) goes low, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. After a write is performed, $\overline{EF}$ goes high, allowing a read to occur. The $\overline{EF}$ flag is updated on the rising edge of RCLK.

In the FWFT mode, the first word written to an empty FIFO automatically goes to the outputs Qn, on the third valid low-to-high transition of RCLK + t_{SKEW} after the first write. $\overline{REN}$ need not be asserted low. To access all other words, a read must be executed using $\overline{REN}$. The RCLK low-to-high transition after the last word has been read from the FIFO, output ready ($\overline{OR}$) goes high with a true read (RCLK with $\overline{REN}$ low), inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

OUTPUT ENABLE ($\overline{OE}$)

When $\overline{OE}$ is low, the parallel output buffers transmit data from the output register. When $\overline{OE}$ is high, the Q-output data bus is in the high-impedance state.

LOAD ($\overline{LD}$)

The SN74V245 contains two 12-bit offset registers with data on the inputs, or read on the outputs. When $\overline{LD}$ is low and $\overline{WEN}$ is low, data on the inputs D0–D11 is written into the empty offset register on the first low-to-high transition of the write clock (WCLK). When $\overline{LD}$ and $\overline{WEN}$ are held low, data is written into the full offset register on the second low-to-high transition of WCLK (see Table 1, Table 2 and Table 3). The third transition of WCLK again writes to the empty-offset register.

However, writing to all offset registers need not occur at one time. One or two offset registers can be written and then, by bringing $\overline{LD}$ high, the FIFO is returned to normal read/write operation. When $\overline{LD}$ is low, and $\overline{WEN}$ is low, the next offset register in sequence is written.

Table 1. Writing to Offset Registers

$\overline{LD}$	$\overline{WEN}$	WCLK	SELECTION(1)
L	L	↑	Writing to offset registers: Empty offset Full offset
L	H	↑	No operation
H	L	↑	Write into FIFO
H	H	↑	No operation

(1) The same selection sequence applies to reading from the registers. REN is enabled and read is performed on the low-to-high transition of RCLK.

Table 2. Empty Offset Register Location and Default Values(1)

17 12	11 0
Not used	Empty Offset Register
	Default value 007FH

(1) Any bits of the offset register not being programmed should be set to zero.

Table 3. Full Offset Register Location and Default Values(1)

17 12	11 0
Not used	Full Offset Register
	Default value 007FH

(1) Any bits of the offset register not being programmed should be set to zero.

When $\overline{LD}$ is low and $\overline{WEN}$ is high, the WCLK input is disabled; then, a signal at this input can neither increment the write-offset-register pointer, nor execute a write.

The contents of the offset registers can be read on the output lines when $\overline{LD}$ is low and $\overline{REN}$ is low; then, data can be read on the low-to-high transition of RCLK. Reading the control registers employs a dedicated read-offset-register pointer (the read and write pointers operate independently). Offset register content can be read out in the standard mode only. It is inhibited in the FWFT mode.

A read from and a write to the offset registers should not be performed simultaneously.

FIRST LOAD ($\overline{FL}$)

For the single-device mode, see Table 6 for additional information. In the daisy-chain depth-expansion configuration, $\overline{FL}$ is grounded to indicate it is the first device loaded and is set high for all other devices in the daisy chain (see Operating Configurations for further details).

WRITE EXPANSION INPUT ($\overline{WXI}$)

This is a dual-purpose pin. For single-device mode, see Table 6 for additional information. $\overline{WXI}$ is connected to write expansion out ($\overline{WXO}$) of the previous device in the daisy-chain depth-expansion mode.

READ EXPANSION INPUT ($\overline{RXI}$)

This is a dual-purpose pin. For single-device mode, see Table 6 for additional information. $\overline{RXI}$ is connected to read expansion out ($\overline{RXO}$) of the previous device in the daisy-chain depth-expansion mode.

OUTPUTS:

FULL FLAG/INPUT READY ($\overline{FF}$/$\overline{IR}$)

This is a dual-purpose pin. In FWFT mode, the input ready ($\overline{IR}$) function is selected. $\overline{IR}$ goes low when memory space is available for writing data. When there is no free space left, $\overline{IR}$ goes high, inhibiting further write operations.

In standard mode, the $\overline{FF}$ function is selected. When the FIFO is full, $\overline{FF}$ goes low, inhibiting further write operations. When $\overline{FF}$ is high, the FIFO is not full. If no reads are performed after a reset, $\overline{FF}$ goes low after D writes to the FIFO. D = 4096.

$\overline{IR}$ goes high after D writes to the FIFO. D = 4097. The additional word in FWFT mode is due to the capacity of the memory plus output register.

$\overline{FF}$/$\overline{IR}$ is synchronous and updated on the rising edge of WCLK.

EMPTY FLAG/OUTPUT READY ($\overline{EF}$/$\overline{OR}$)

This is a dual-purpose pin. In FWFT mode, the $\overline{OR}$ function is selected. $\overline{OR}$ goes low at the same time the first word written to an empty FIFO appears valid on the outputs. $\overline{OR}$ stays low after the RCLK low-to-high transition that shifts the last word from the FIFO memory to the outputs. $\overline{OR}$ goes high only with a true read (RCLK with $\overline{REN}$ low). The previous data stays at the outputs, indicating that the last word was read. Further data reads are inhibited until $\overline{OR}$ goes low again.

In the standard mode, the $\overline{EF}$ function is selected. When the FIFO is empty, $\overline{EF}$ goes low, inhibiting further read operations. When $\overline{EF}$ is high, the FIFO is not empty.

$\overline{EF}$/$\overline{OR}$ is synchronous and updated on the rising edge of RCLK.

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

$\overline{PAF}$ goes low when the FIFO reaches the almost-full condition. In FWFT mode, if no reads are performed, $\overline{PAF}$ goes low after 4097 - m. Default values for m are in Table 4 and Table 5.

In standard mode, if no reads are performed after reset ($\overline{RS}$), $\overline{PAF}$ goes low after 4096 – m writes. The offset m is defined in Table 3.

If asynchronous $\overline{PAF}$ configuration is selected, $\overline{PAF}$ is asserted low on the low-to-high transition of WCLK. $\overline{PAF}$ is reset to high on the low-to-high transition of RCLK. If synchronous $\overline{PAF}$ configuration is selected (see Table 6), $\overline{PAF}$ is updated on the rising edge of WCLK.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

$\overline{PAE}$ goes low when the FIFO reaches the almost-empty condition. In FWFT mode, $\overline{PAE}$ goes low when there are n + 1 words, or fewer, in the FIFO. In standard mode, $\overline{PAE}$ goes low when there are n words or fewer in the FIFO. The offset n is defined as the empty offset. The default values for n are noted in Table 4 and Table 5.

If there is no empty offset specified, $\overline{PAE}$ is low when the device is 127 away from completely empty.

If asynchronous $\overline{PAE}$ configuration is selected, $\overline{PAE}$ is asserted low on the low-to-high transition of the read clock (RCLK). $\overline{PAE}$ is reset to high on the low-to-high transition of the write clock (WCLK). If synchronous $\overline{PAE}$ configuration is selected (see Table 6), $\overline{PAE}$ is updated on the rising edge of RCLK.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO}$/$\overline{HF}$)

This is a dual-purpose output. In the single-device and width-expansion mode, when write expansion in ($\overline{WXI}$) and/or read expansion in ($\overline{RXI}$) are grounded, this output acts as an indication of a half-full memory.

After one-half of the memory is filled, and at the low-to-high transition of the next write cycle, the half-full flag ($\overline{HF}$) goes low and remains set until the difference between the write pointer and read pointer is less than or equal to one-half of the total memory of the device. $\overline{HF}$ is then reset to high by the low-to-high transition of the read clock (RCLK). $\overline{HF}$ is asynchronous.

In the daisy-chain depth-expansion mode, $\overline{WXI}$ is connected to $\overline{WXO}$ of the previous device. This output acts as a signal to the next device in the daisy chain by providing a pulse when the previous device writes to the last location of memory.

READ EXPANSION OUT ($\overline{RXO}$)

In the daisy-chain depth-expansion configuration, read expansion in ($\overline{RXI}$) is connected to read expansion out ($\overline{RXO}$) of the previous device. This output acts as a signal to the next device in the daisy chain by providing a pulse when the previous device reads from the last location of memory.

DATA OUTPUTS (Q0–Q17)

Q0–Q17 are data outputs for 18-bit-wide data.

FUNCTIONAL DESCRIPTION

TIMING MODES:

STANDARD vs FIRST-WORD FALL-THROUGH (FWFT) MODE

The SN74V245 supports two different timing modes. The selection of the mode of operation is determined during configuration at reset ($\overline{RS}$). During an $\overline{RS}$ operation, the first load ($\overline{FL}$), read expansion input ($\overline{RXI}$), and write-expansion input ($\overline{WXI}$) pins are used to select the timing mode as shown in Table 6. In standard mode, the first word written to an empty FIFO does not appear on the data output lines unless a specific read operation is performed. A read operation, which consists of activating read enable ($\overline{REN}$) and enabling a rising read clock (RCLK) edge, shifts the word from internal memory to the data output lines. In FWFT mode, the first word written to an empty FIFO is clocked directly to the data output lines after three transitions of the RCLK signal. A $\overline{REN}$ does not have to be asserted to access the first word.

Various signals, both input and output signals, operate differently, depending on which timing mode is in effect.

FIRST-WORD FALL-THROUGH MODE (FWFT)

In this mode, status flags $\overline{IR}$, $\overline{PAF}$, $\overline{HF}$, $\overline{PAE}$, and $\overline{OR}$ operate in the manner outlined in Table 4. To write data into the FIFO, $\overline{WEN}$ must be low. Data presented to the data-in lines is clocked into the FIFO on subsequent transitions of WCLK. After the first write is performed, the output ready ($\overline{OR}$) flag goes low. Subsequent writes continue to fill the FIFO. $\overline{PAE}$ goes high after n + 2 words have been loaded into the FIFO, where n is the empty offset value. The default setting for this value is stated in the footnote of Table 4. This parameter also is user programmable. See the Programmable Flag Offset Loading section.

If data continues to be written into the FIFO, and no read operations are taking place, $\overline{HF}$ switches to low when the 2050th word is written into the FIFO. Continuing to write data into the FIFO causes $\overline{PAF}$ to go low. Again, if no reads are performed, $\overline{PAF}$ goes low after 4097 – m writes, where m is the full offset value. The default setting for this value is stated in the footnote of Table 4.

When the FIFO is full, the input ready ($\overline{IR}$) flag goes high, inhibiting further write operations. If no reads are performed after a reset, $\overline{IR}$ goes high after D writes to the FIFO. D = 4097. The additional word in FWFT mode is due to the capacity of the memory plus output register.

If the FIFO is full, the first read operation causes the $\overline{IR}$ flag to go low. Subsequent read operations cause $\overline{PAF}$ and $\overline{HF}$ to go high at the conditions described in Table 4. If further read operations occur without write operations, $\overline{PAE}$ goes low when there are n + 1 words in the FIFO, where n is the empty offset value. If there is no empty offset specified, $\overline{PAE}$ is low when the device is 128 away from empty. Continuing read operations cause the FIFO to be empty. When the last word has been read from the FIFO, $\overline{OR}$ goes high, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

Table 4. Status Flags for FWFT Mode

NUMBER OF WORDS IN FIFO	$\overline{IR}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{OR}$
0	L	H	H	L	H
1 to (n+1) (1)	L	H	H	L	L
(n+2) to 2049	L	H	H	H	L
2050 to [4097–(m+1)] (2)	L	H	L	H	L
(4097–m) to 4096	L	L	L	H	L
4097	H	L	L	H	L

(1) n = Empty offset = 127
(2) m = Full offset = 127

STANDARD MODE

In this mode, status flags $\overline{FF}$, $\overline{PAF}$, $\overline{HF}$, $\overline{PAE}$, and $\overline{EF}$ operate in the manner outlined in Table 5. To write data into the FIFO, write enable ($\overline{WEN}$) must be low. Data presented to the data-in lines is clocked into the FIFO on subsequent transitions of the write clock (WCLK). After the first write is performed, the empty flag ($\overline{EF}$) goes high. Subsequent writes continue to fill the FIFO. The programmable almost-empty flag ($\overline{PAE}$) goes high after n + 1 words have been loaded into the FIFO, where n is the empty offset value. The default setting for this value is stated in the footnote of Table 5. This parameter also is user programmable. See the Programmable Flag Offset Loading section.

If data continues to be written into the FIFO, and no read operations are taking place, the half-full flag ($\overline{HF}$) switches to low when the 2049th word is written into the FIFO. Continuing to write data into the FIFO causes the programmable almost-full flag ($\overline{PAF}$) to go low. Again, if no reads are performed, $\overline{PAF}$ goes low after 4096 – m writes. Offset m is the full offset value. This parameter also is user programmable. See the Programmable Flag Offset Loading section. If there is no full offset specified, $\overline{PAF}$ is low when the device is 127 away from full.

When the FIFO is full, the full flag ($\overline{FF}$) goes low, inhibiting further write operations. If no reads are performed after a reset, $\overline{FF}$ goes low after D writes to the FIFO. D = 4096.

If the FIFO is full, the first read operation causes $\overline{FF}$ to go high. Subsequent read operations cause $\overline{PAF}$ and the half-full flag ($\overline{HF}$) to go high under the conditions described in Table 5. If further read operations occur, without write operations, the programmable almost-empty flag ($\overline{PAE}$) goes low when there are n words in the FIFO, where n is the empty offset value. If there is no empty offset specified, $\overline{PAE}$ is low when the device is 127 away from completely empty. Continuing read operations cause the FIFO to be empty. When the last word has been read from the FIFO, $\overline{EF}$ goes low, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty.

Table 5. Status Flags for Standard Mode

NUMBER OF WORDS IN FIFO	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	H	H	H	L	L
1 to n (1)	H	H	H	L	H
(n+1) to 2048	H	H	H	H	H
2049 to [4096–(m+1)] (2)	H	H	L	H	H
(4096–m) to 4095	H	L	L	H	H
4096	L	L	L	H	H

(1) n = Empty offset = 127
(2) m = Full offset = 127

PROGRAMMABLE FLAG LOADING

Full- and empty-flag offset values can be user programmable. The SN74V245 has internal registers for these offsets. Default settings are stated in the footnotes of Table 4 and Table 5. Offset values are loaded into the FIFO using the data input lines D0–D11. To load the offset registers, the load ($\overline{LD}$) pin and $\overline{WEN}$ pin must be held low. Data present on D0–D11 is transferred to the empty offset register on the first low-to-high transition of WCLK. By continuing to hold the $\overline{LD}$ and $\overline{WEN}$ pins low, data present on D0–D11 is transferred into the full offset register on the next transition of the WCLK. The third transition again writes to the empty offset register. Writing to all offset registers does not have to occur at the same time. One or two offset registers can be written and then, by bringing the LD pin high, the FIFO is returned to normal read/write operation. When the $\overline{LD}$ pin and $\overline{WEN}$ again are set low, the next offset register in sequence is written.

The contents of the offset registers can be read on the data output lines Q0–Q11 when the $\overline{LD}$ pin is set low, and $\overline{REN}$ is set low. Data then can be read on the next low-to-high transition of RCLK. The first transition of RCLK presents the empty offset value to the data output lines. The next transition of RCLK presents the full offset value. Offset register content can be read in the standard mode only. It cannot be read in the FWFT mode.

SYNCHRONOUS vs ASYNCHRONOUS PROGRAMMABLE FLAG TIMING SELECTION

The SN74V245 can be configured during the configuration-at-reset cycle (see Table 6) with either asynchronous or synchronous timing for $\overline{PAE}$ and $\overline{PAF}$ flags.

If asynchronous $\overline{PAE}$/$\overline{PAF}$ configuration is selected (see Table 6), the $\overline{PAE}$ is asserted low on the low-to-high transition of RCLK. $\overline{PAE}$ is reset to high on the low-to-high transition of WCLK. Similarly, the $\overline{PAF}$ is asserted low on the low-to-high transition of WCLK, and $\overline{PAF}$ is reset to high on the low-to-high transition of RCLK. For detailed timing diagrams, see Figure 11 for asynchronous $\overline{PAE}$ timing and Figure 12 for asynchronous $\overline{PAF}$ timing.

If synchronous $\overline{PAE}$/$\overline{PAF}$ configuration is selected, $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only, but not WCLK. Similarly, $\overline{PAF}$ is asserted and updated on the rising edge of WCLK only, but not RCLK. For detailed timing diagrams, see Figure 20 for synchronous $\overline{PAE}$ timing and Figure 21 for synchronous $\overline{PAF}$ timing.

Table 6. Truth Table for Configuration at Reset

$\overline{FL}$	$\overline{RXI}$	$\overline{WXI}$	$\overline{EF}$/$\overline{OR}$	$\overline{FF}$/$\overline{IR}$	$\overline{PAE}$, $\overline{PAF}$	FIFO TIMING MODE
0	0	0	Single register-buffered empty flag	Single register-buffered full flag	Asynchronous	Standard
0	0	1	Triple register-buffered output-ready flag	Double register-buffered input ready flag	Asynchronous	FWFT
0	1	0	Double register-buffered empty flag	Double register-buffered full flag	Asynchronous	Standard
0(1)	1	1	Single register-buffered empty flag	Single register-buffered full flag	Asynchronous	Standard
1	0	0	Single register-buffered empty flag	Single register-buffered full flag	Synchronous	Standard
1	0	1	Triple register-buffered output-ready flag	Double register-buffered input ready flag	Synchronous	FWFT
1	1	0	Double register-buffered empty flag	Double register-buffered full flag	Synchronous	Standard
1(2)	1	1	Single register-buffered empty flag	Single register-buffered full flag	Asynchronous	Standard

(1) In daisy-chain depth expansion, $\overline{FL}$ is held low for the first-load device. The $\overline{RXI}$ and $\overline{WXI}$ inputs are driven by the corresponding $\overline{RXO}$ and $\overline{WXO}$ outputs of the preceding device.

(2) In daisy-chain depth expansion, $\overline{FL}$ is held high for members of the expansion other than the first-load device. The $\overline{RXI}$ and $\overline{WXI}$ inputs are driven by the corresponding $\overline{RXO}$ and $\overline{WXO}$ outputs of the preceding device.

REGISTER-BUFFERED FLAG OUTPUT SELECTION

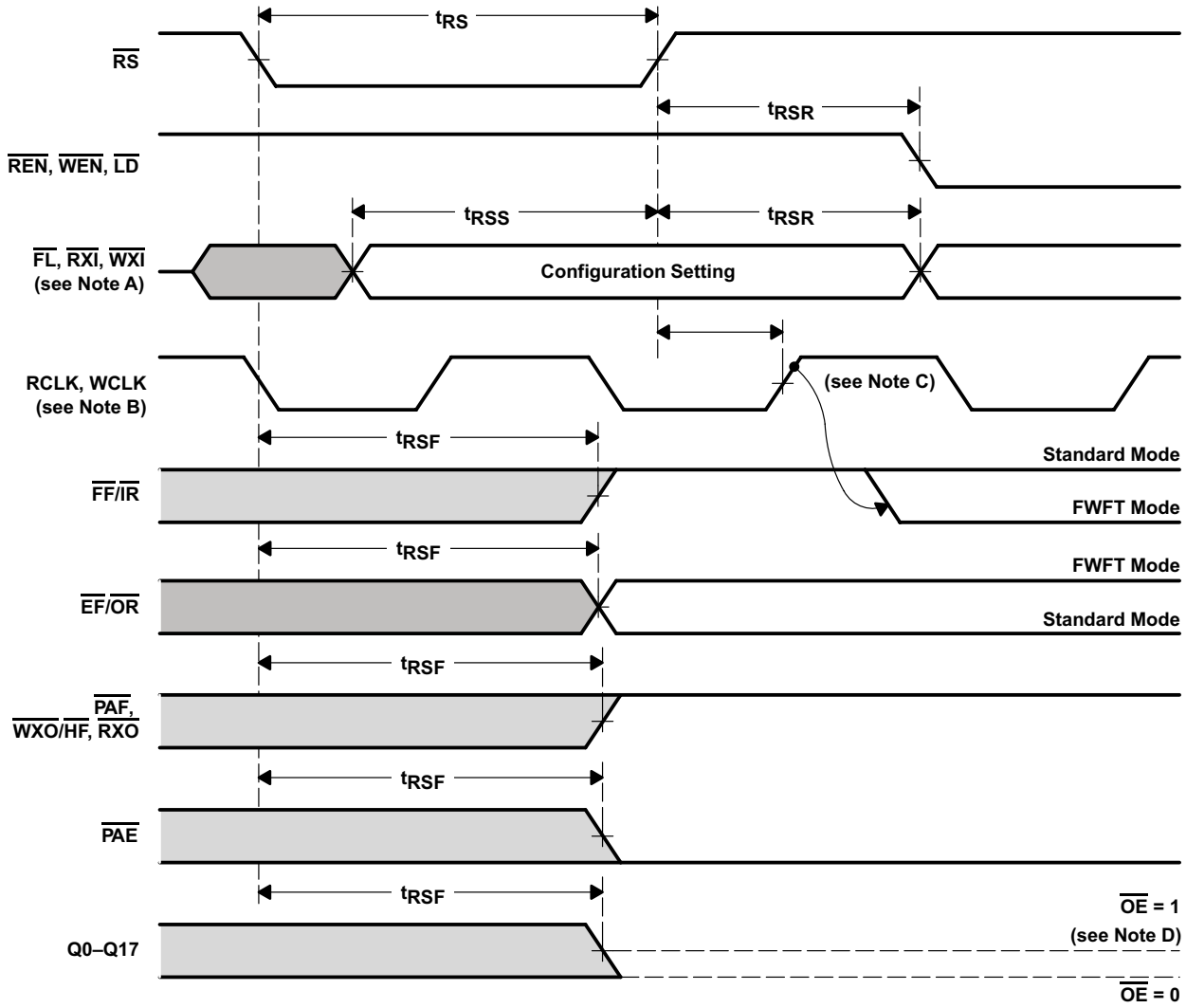
The SN74V245 can be configured during the configuration-at-reset cycle (see Table 8) with single, double, or triple register-buffered flag output signals. The various combinations available are described in Table 7 and Table 8. In general, going from single to double or triple register-buffered flag outputs removes the possibility of metastable flag indications on boundary states (empty or full conditions). The tradeoff is the addition of clock-cycle delays for the respective flag to be asserted. Not all combinations of register-buffered flag outputs are supported. Register-buffered outputs apply to the empty flag and full flag only. Partial flags are not affected. Table 7 and Table 8 summarize the options available.

Table 7. Register-Buffered Flag Output Options, FWFT Mode

OUTPUT READY ($\overline{OR}$)	INPUT READY ($\overline{IR}$)	PARTIAL FLAGS	PROGRAMMING AT RESET			FLAG TIMING DIAGRAMS
			$\overline{FL}$	$\overline{RXI}$	$\overline{WXI}$	
Triple	Double	Asynchronous	0	0	1	Figure 25
Triple	Double	Synchronous	1	0	1	Figure 18, Figure 19

Table 8. Register-Buffered Flag Output Options, Standard Mode

EMPTY FLAG ($\overline{EF}$) BUFFERED OUTPUT	FULL FLAG ($\overline{FF}$) BUFFERED OUTPUT	PARTIAL FLAGS TIMING MODE	PROGRAMMING AT RESET			FLAG TIMING DIAGRAMS
			$\overline{FL}$	$\overline{RXI}$	$\overline{WXI}$	
Single	Single	Asynchronous	0	0	0	Figure 7, Figure 8
Single	Single	Synchronous	1	0	0	Figure 7, Figure 8
Double	Double	Asynchronous	0	1	0	Figure 22, Figure 24
Double	Double	Synchronous	1	1	0	Figure 22, Figure 24



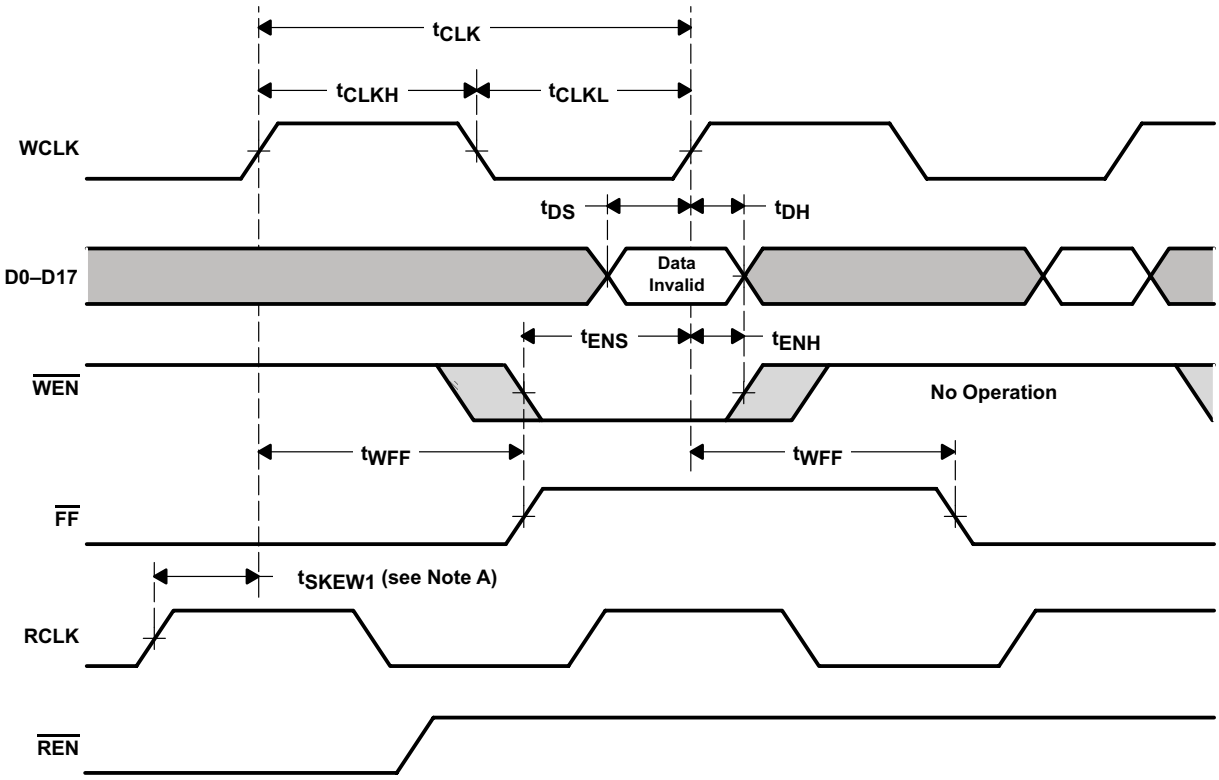
NOTES: A. Single-device mode ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,0,0), (0,0,1), (0,1,0), (1,0,0), (1,0,1) or (1,1,0). $\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$ should be static (tied to V_{CC} or GND).

B. The clocks (RCLK, WCLK) can be free-running asynchronously or coincidentally.

C. In FWFT mode, $\overline{IR}$ goes low based on the WCLK edge after reset.

D. After reset, the outputs are low if $\overline{OE}$ = 0 and 3-state if $\overline{OE}$ = 1.

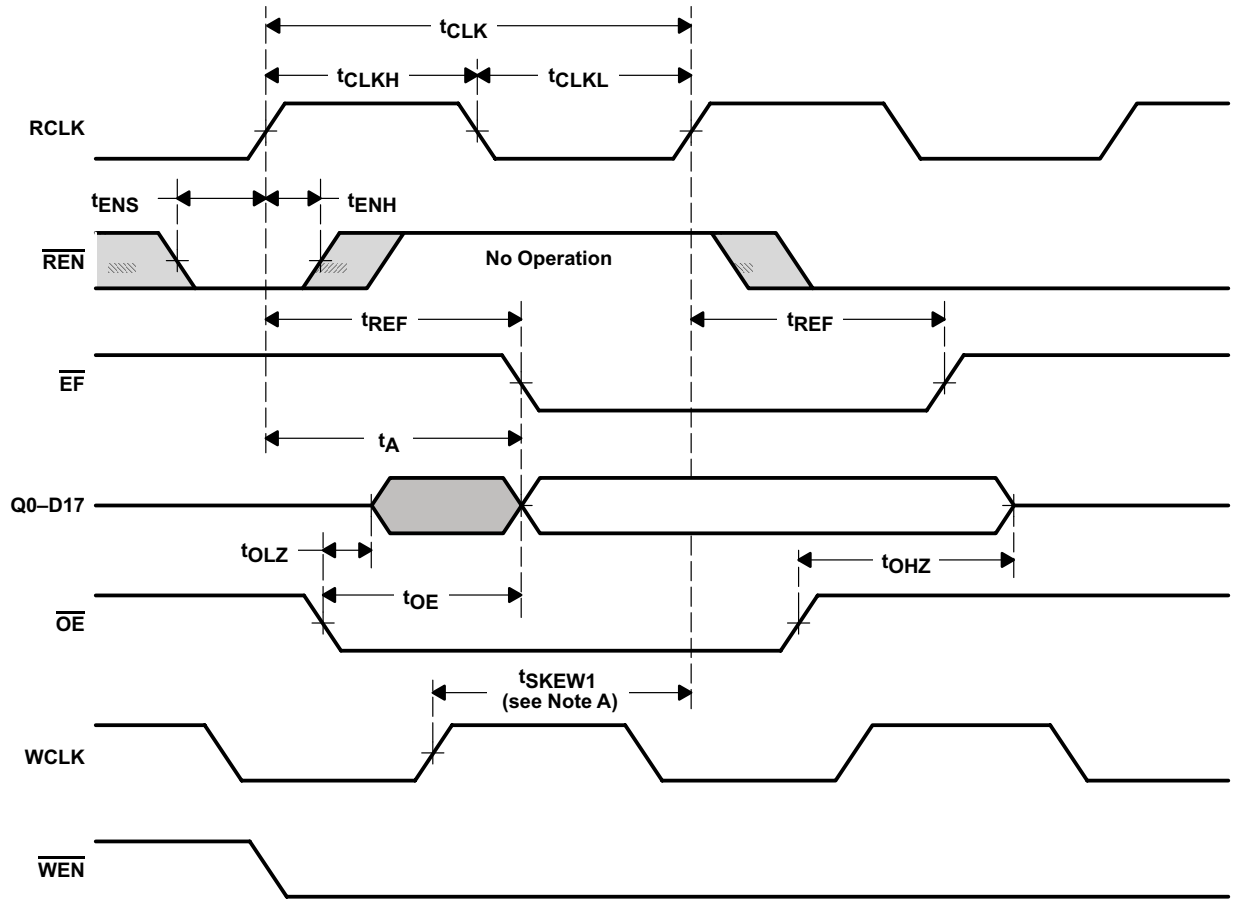
Figure 3. Reset Timing



NOTES: A. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{FF}$ goes high during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, $\overline{FF}$ might not change state until the next WCLK edge.

B. Select standard mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,0,0), (0,1,1), (1,0,0) or (1,1,1) during reset.

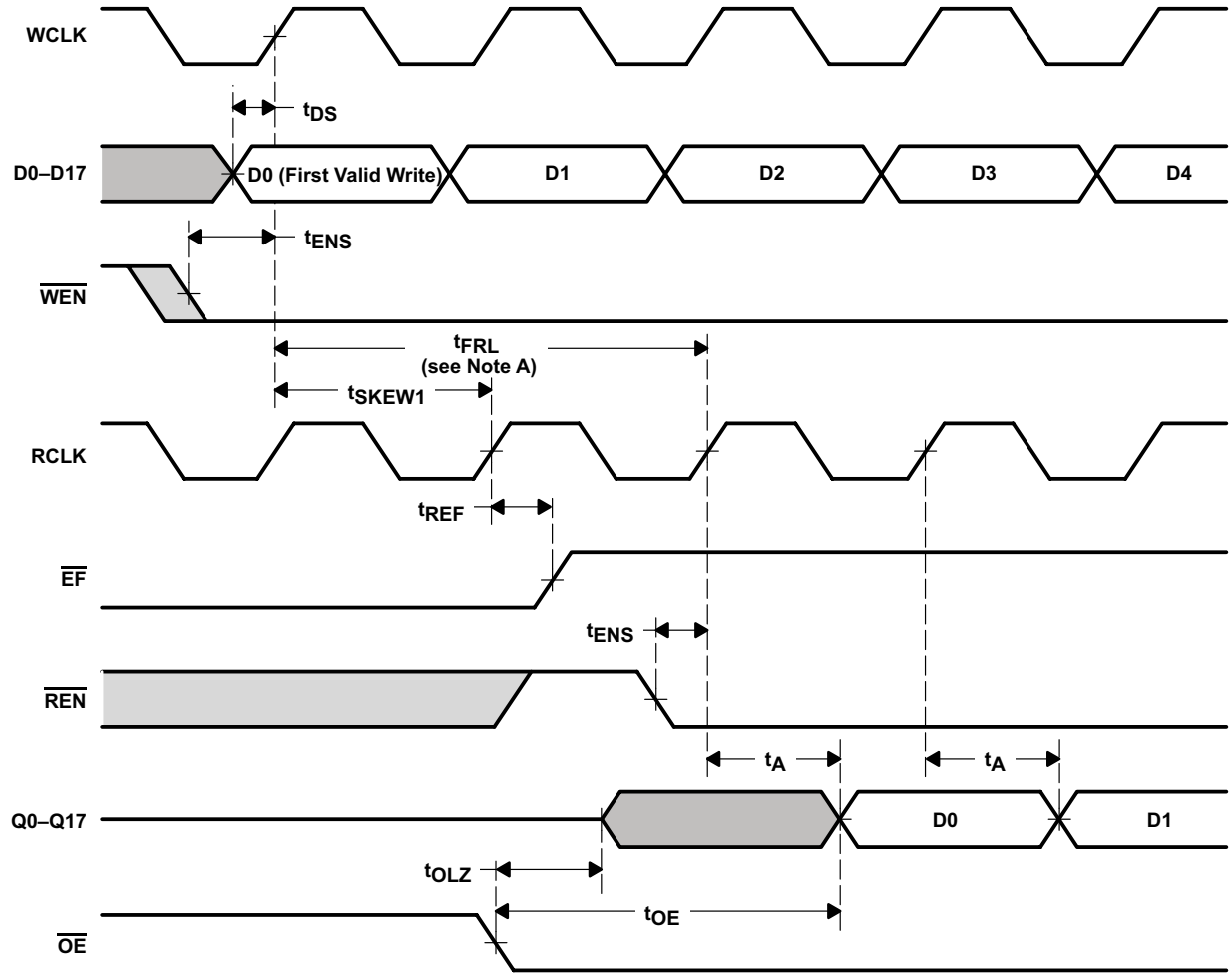
Figure 4. Write-Cycle Timing With Single Register-Buffered $\overline{FF}$ (Standard Mode)



NOTES: A. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to ensure that $\overline{EF}$ goes high during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, $\overline{EF}$ might not change state until the next RCLK edge.

B. Select standard mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,0,0), (0,1,1), (1,0,0) or (1,1,1) during reset.

Figure 5. Read-Cycle Timing With Single Register-Buffered $\overline{EF}$ (Standard Mode)

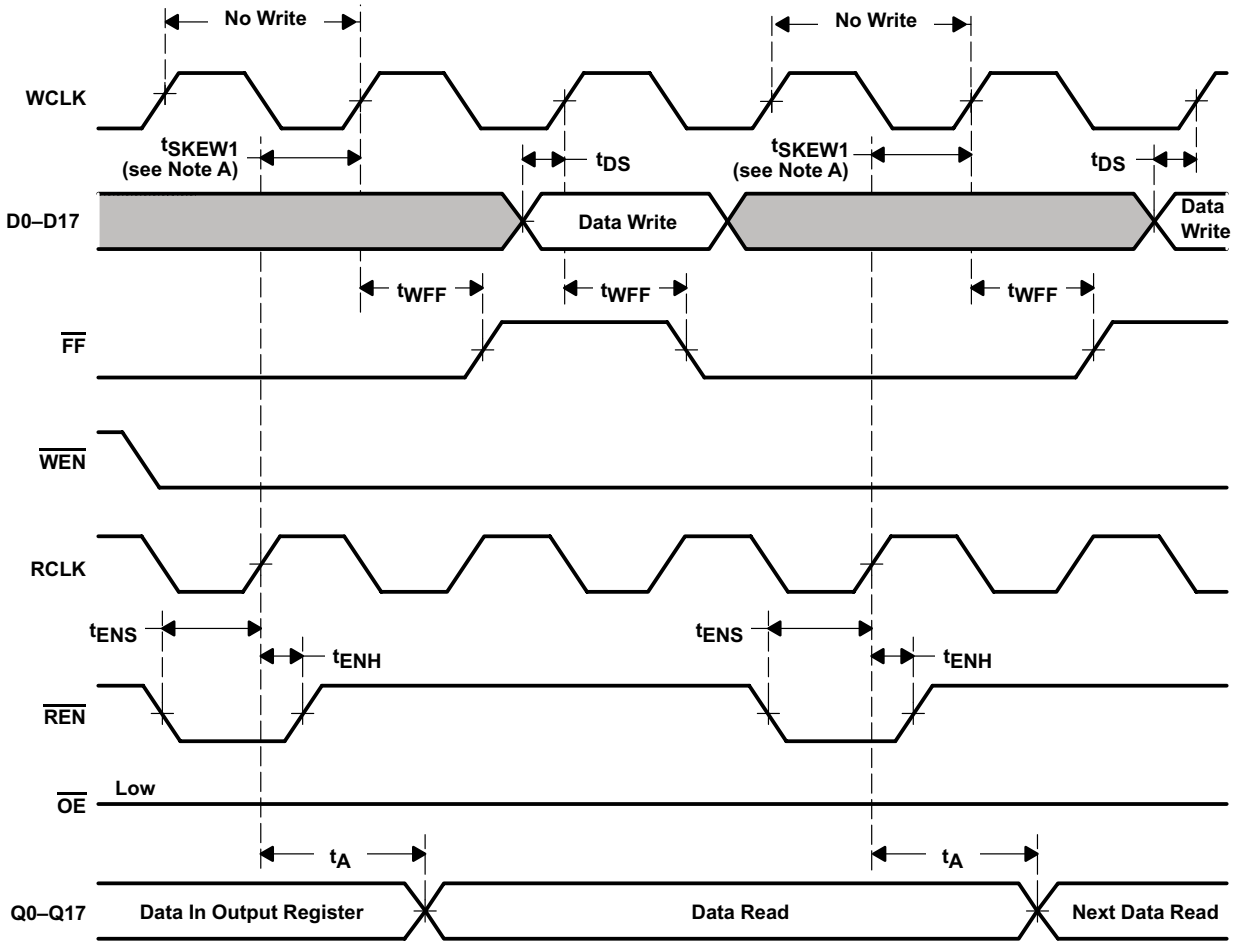


NOTES: A. When t_{SKEW1} is at the minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW1}. When t_{SKEW1} is less than the minimum specification, t_{FRL} (maximum) = either (2 × t_{CLK}) + t_{SKEW1} or t_{CLK} + t_{SKEW1}. The latency timing applies only at the empty boundary ($\overline{EF}$ is low).

B. The first word always is available the cycle after $\overline{EF}$ goes high.

C. Select standard mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,0,0), (0,1,1), (1,0,0) or (1,1,1) during reset.

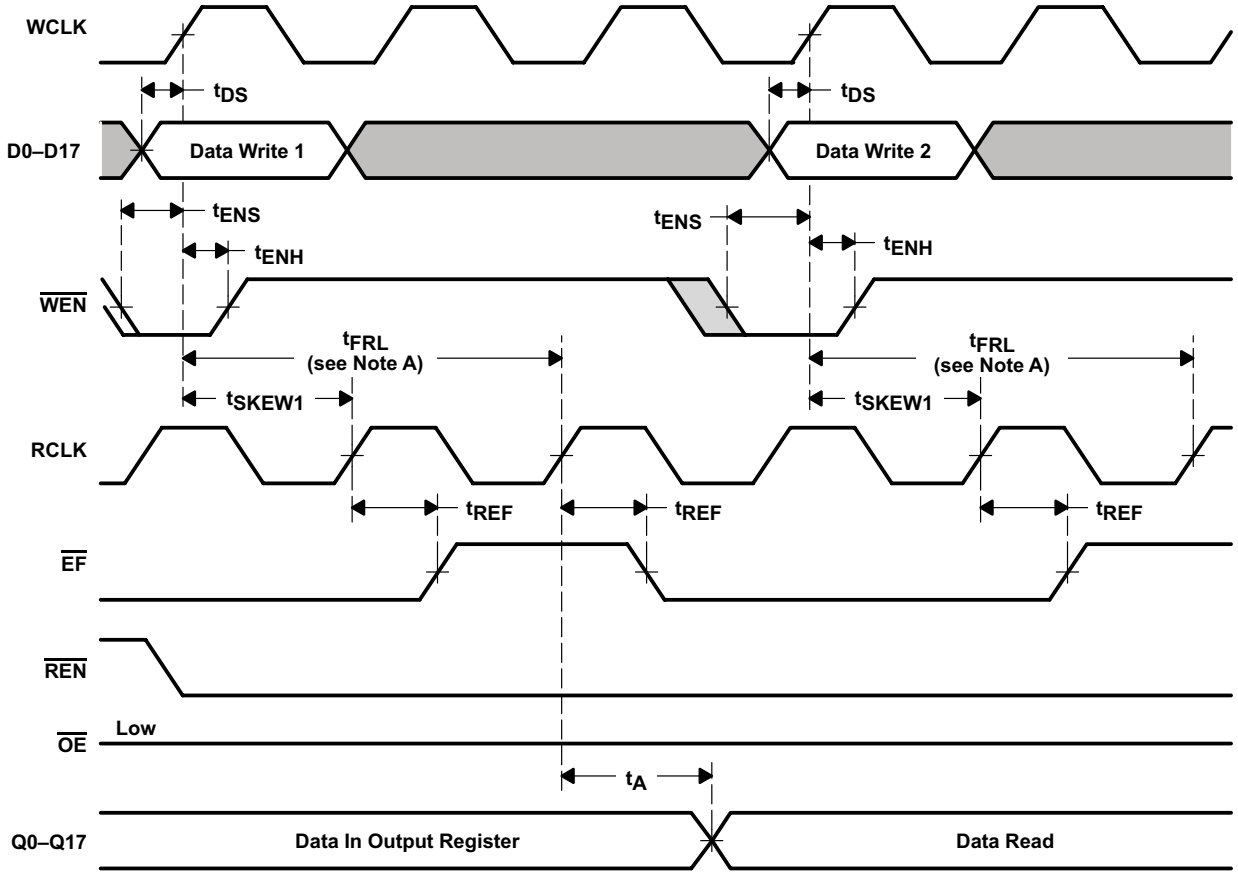
Figure 6. First-Data-Word Latency with Single Register-Buffered $\overline{EF}$ (Standard Mode)



NOTES: A. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{FF}$ goes high during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, $\overline{FF}$ might not change state until the next WCLK edge.

B. Select standard mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,0,0), (0,1,1), (1,0,0) or (1,1,1) during reset.

Figure 7. Single Register-Buffered Full-Flag Timing (Standard Mode)



NOTES: A. When t_{SKEW1} is at the minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW1}. When t_{SKEW1} is less than the minimum specification, t_{FRL} (maximum) = either (2 × t_{CLK}) + t_{SKEW1} or t_{CLK} + t_{SKEW1}. The latency timing applies only at the empty boundary ($\overline{EF}$ is low).

B. Select standard mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,0,0), (0,1,1), (1,0,0) or (1,1,1) during reset.

Figure 8. Single Register-Buffered Empty Flag Timing (Standard Mode)

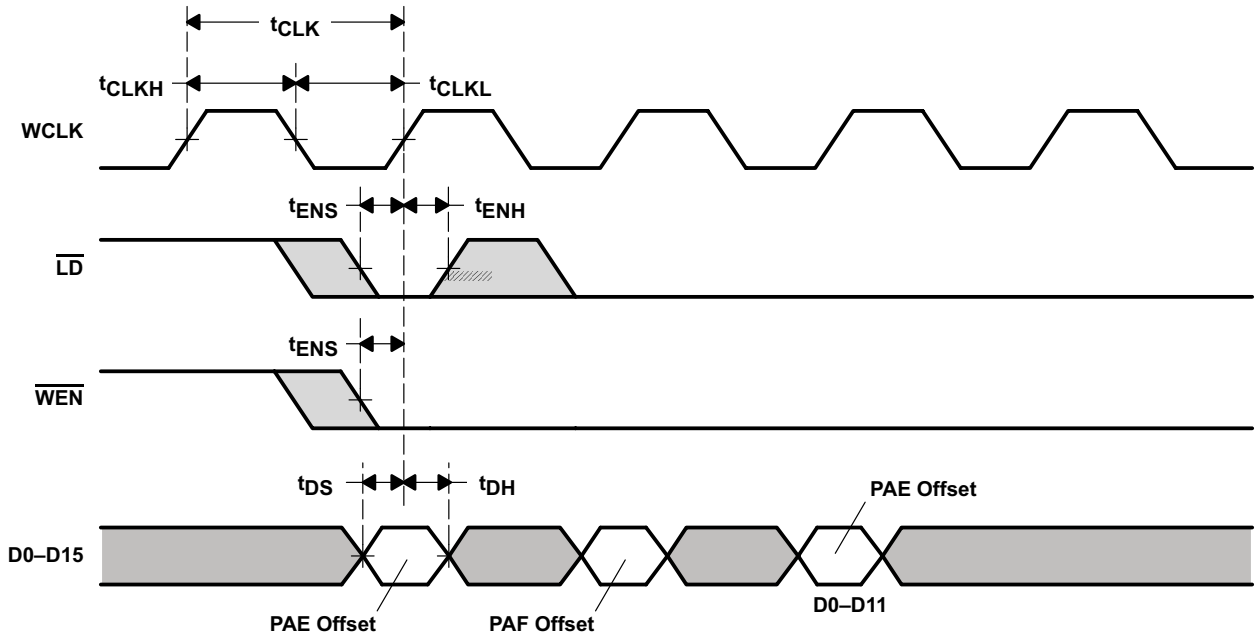


Figure 9. Write Programmable Registers (Standard and FWFT Modes)

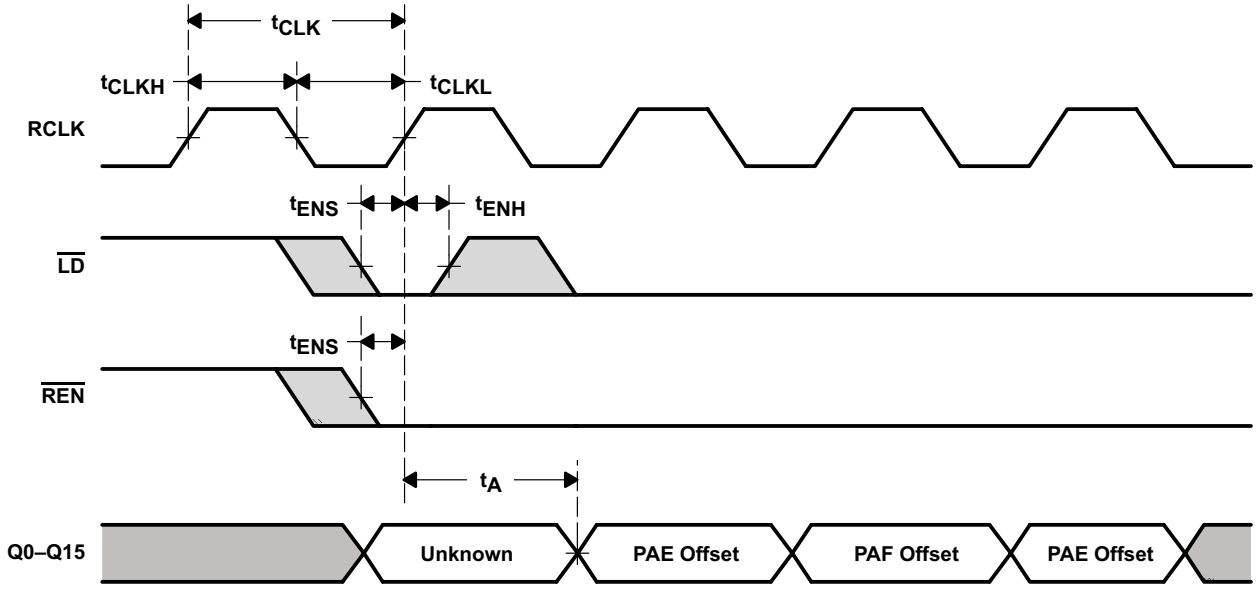
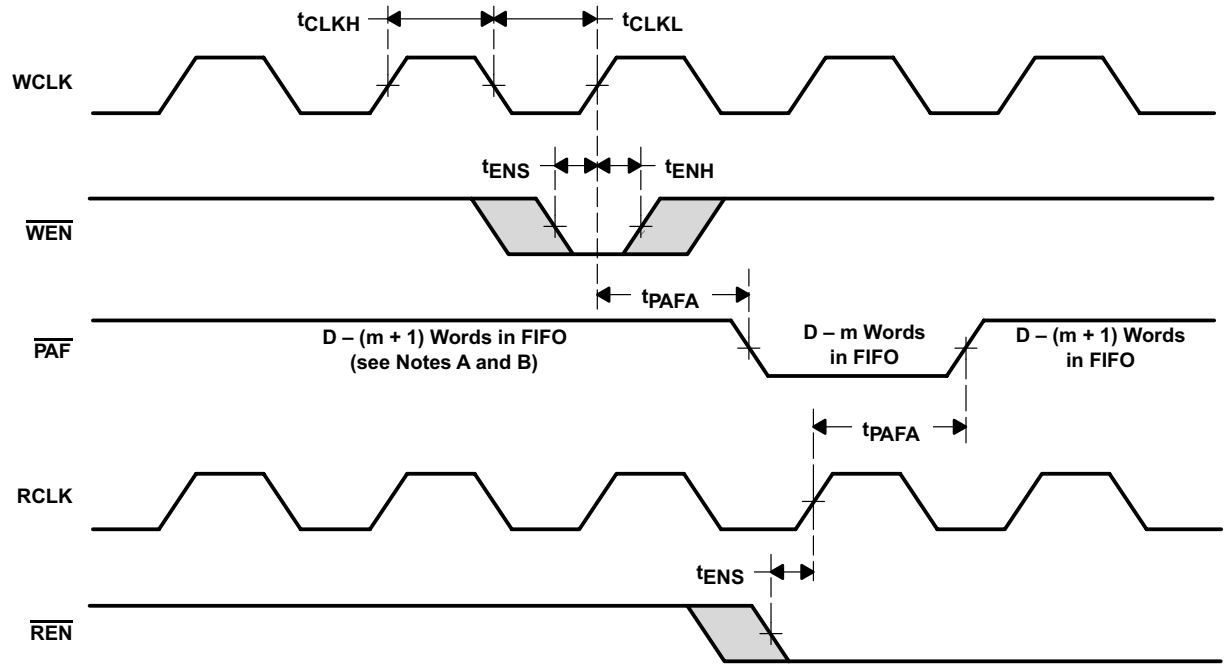
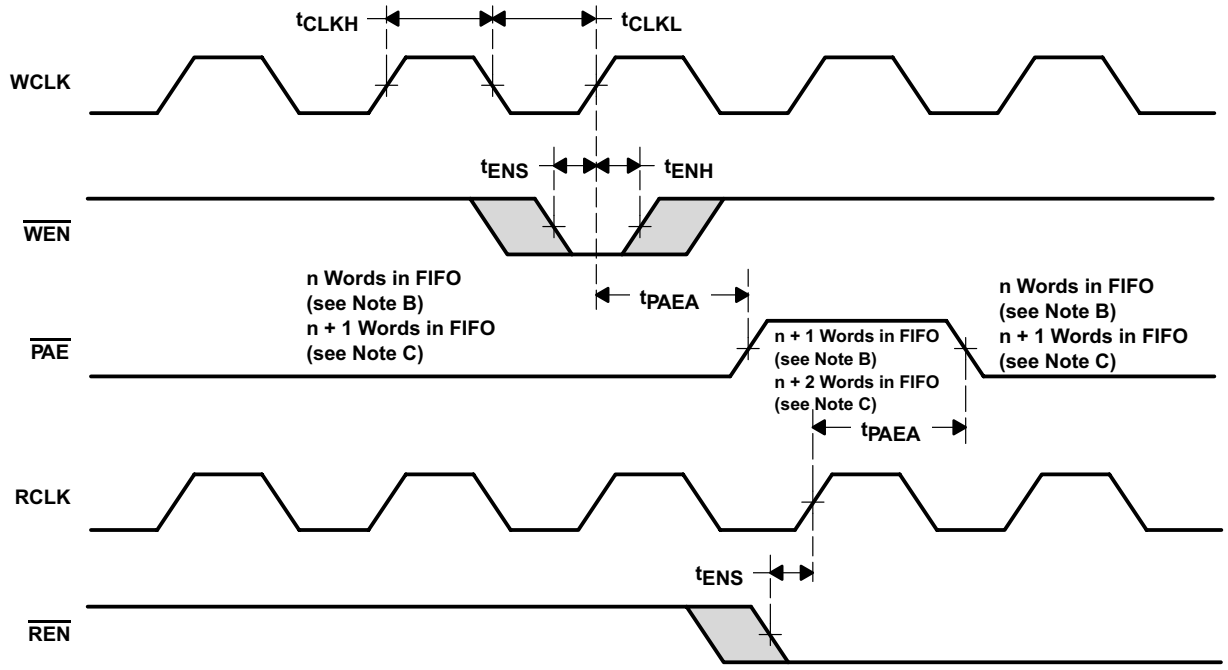


Figure 10. Read Programmable Registers (Standard Mode)



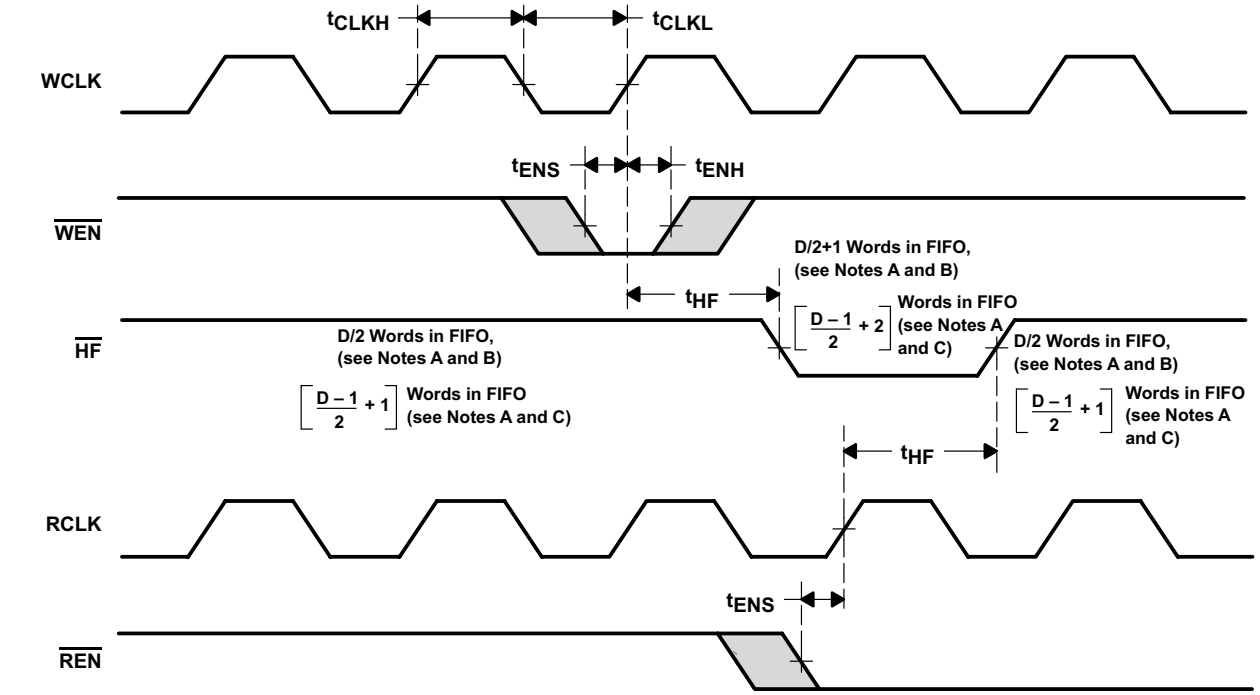
NOTES: A. m = $\overline{\text{PAF}}$ offset
B. D = maximum FIFO depth
In FWFT mode: D = 4097
In standard mode: D = 4096
C. $\overline{\text{PAF}}$ is asserted to low on WCLK transition and reset to high on RCLK transition.
D. Select asynchronous modes by setting ($\overline{\text{FL}}$, $\overline{\text{RXI}}$, $\overline{\text{WXI}}$) = (0,0,0), (0,0,1), (0,1,0), (0,1,1) or (1,1,1) during reset.

Figure 11. Asynchronous Programmable Almost-Empty-Flag Timing (Standard and FWFT Modes)



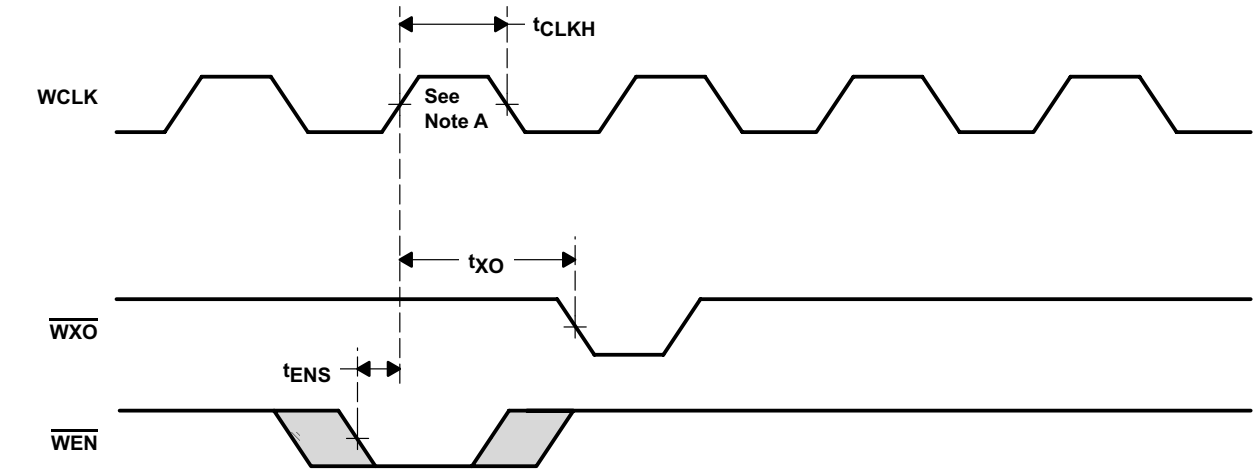
NOTES: A. n = $\overline{PAE}$ offset
B. For standard mode
C. For FWFT mode
D. $\overline{PAE}$ is asserted low on RCLK transition and reset to high on WCLK transition.
E. Select the asynchronous modes by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,0,0), (0,0,1), (0,1,0), (0,1,1) or (1,1,1) during reset.

Figure 12. Asynchronous Programmable Almost-Full-Flag Timing (Standard and FWFT Modes)



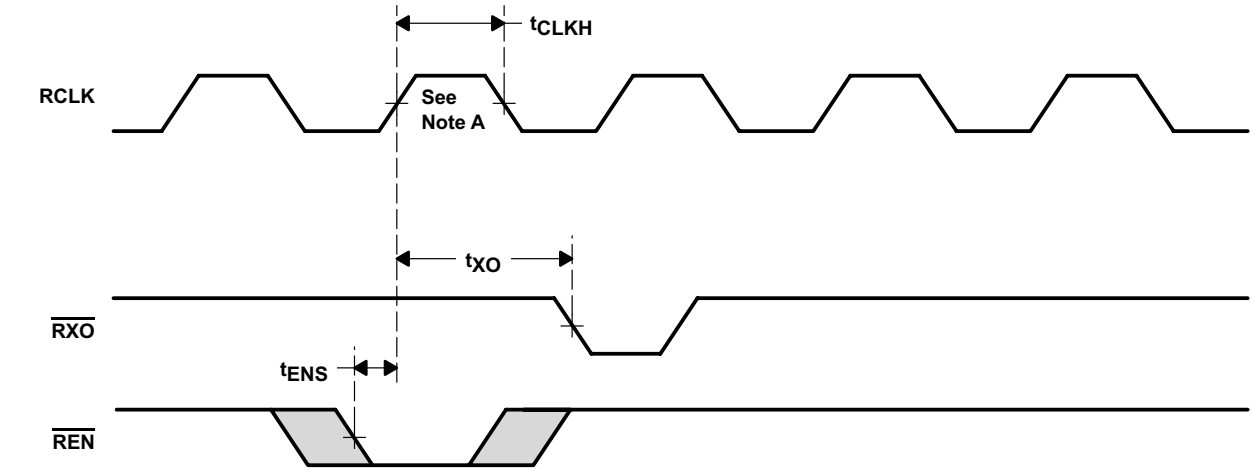
NOTES: A. D = maximum FIFO depth
In FWFT mode: D = 4097
In standard mode: D = 4096
B. For standard mode
C. For FWFT mode
D. Select single-device mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,0,0), (0,0,1), (0,1,0), (1,0,0), (1,0,1) or (1,1,0) during reset.

Figure 13. Half-Full-Flag Timing (Standard and FWFT Modes)



NOTE A: Write to last physical location.

Figure 14. Write-Expansion-Out Timing



NOTE A: Read from last physical location.

Figure 15. Read-Expansion-Out Timing

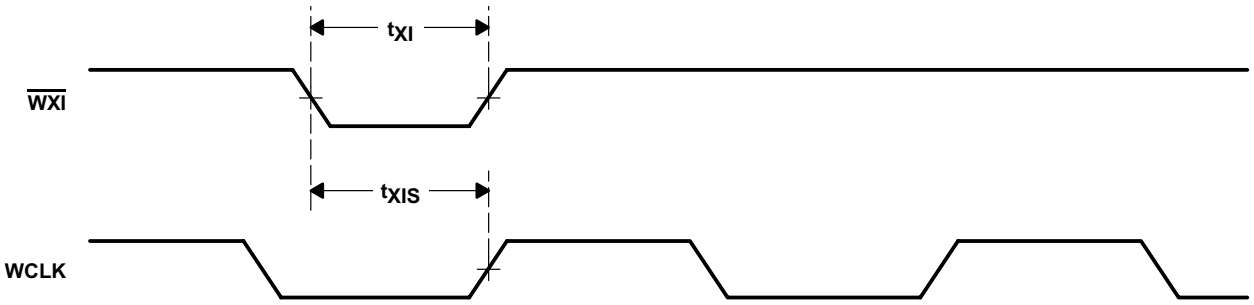


Figure 16. Write-Expansion-In Timing

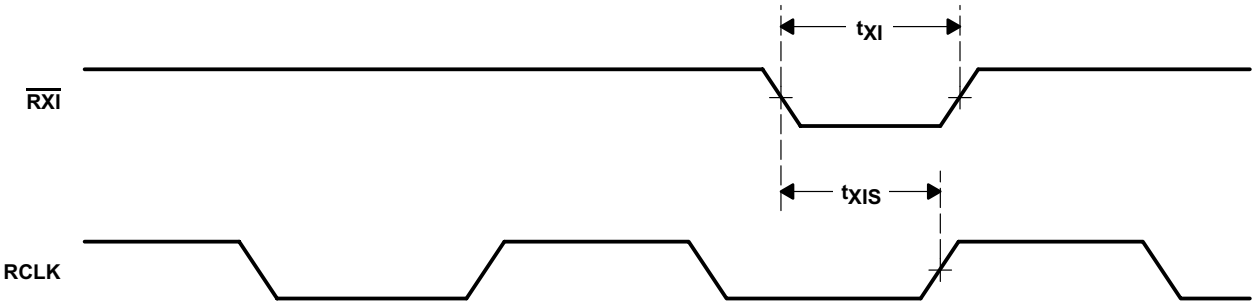
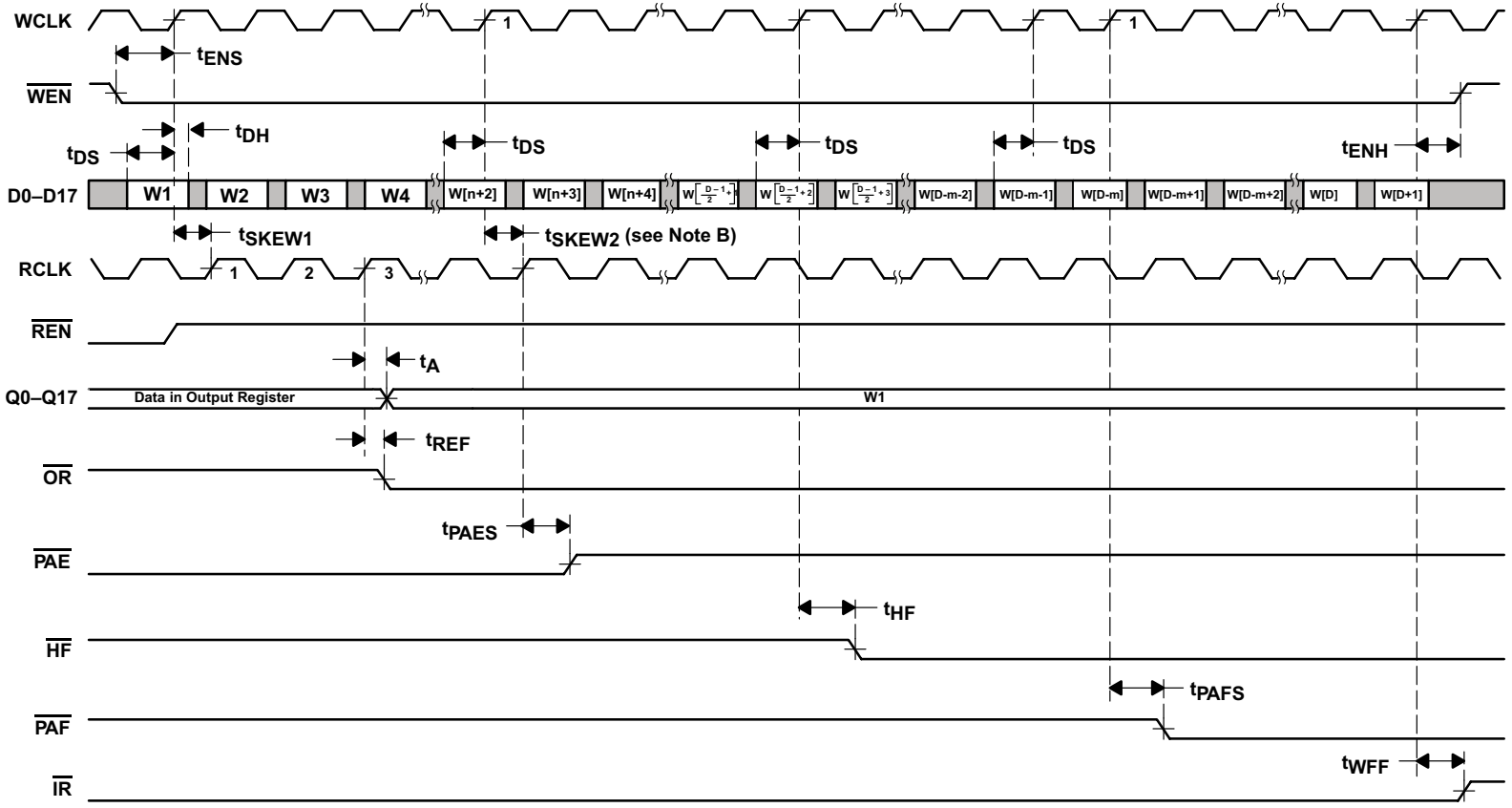


Figure 17. Read-Expansion-In Timing



NOTES: A. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{OR}$ to go low after two RCLK cycles plus t_{REF}. If the time between the rising edge of WLCK and the rising edge of RCLK is less than t_{SKEW1}, the $\overline{OR}$ deassertion might be delayed one extra RCLK cycle.

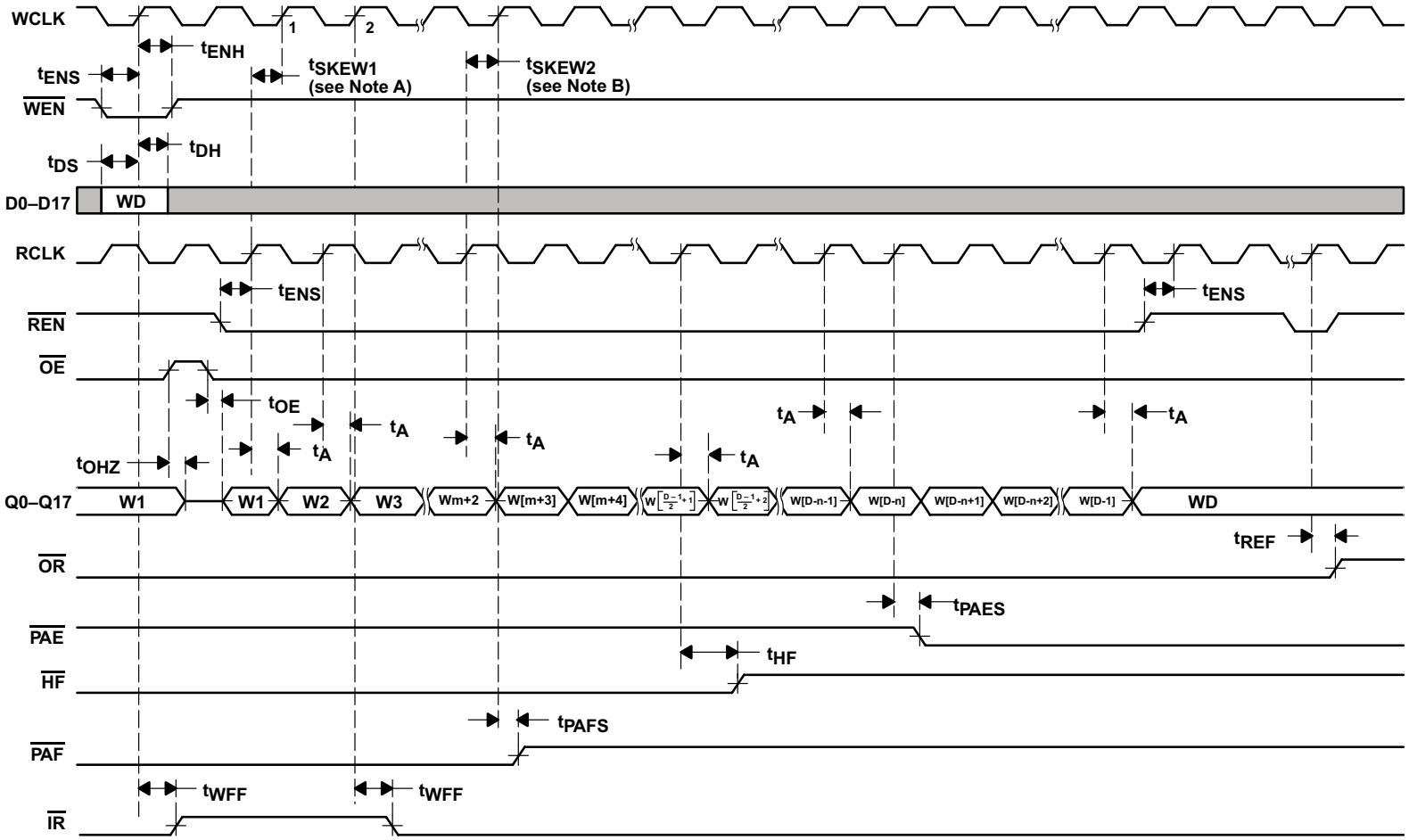
B. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to go high during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, the $\overline{PAE}$ deassertion might be delayed one extra RCLK cycle.

C. $\overline{LD}$ is high, $\overline{OE}$ is low.

D. n = $\overline{PAE}$ offset, m = $\overline{PAF}$ offset, D = maximum FIFO depth = 4097 words

E. Select synchronous FWFT mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (1,0,1) during reset.

Figure 18. Write Timing With Synchronous Programmable Flags (FWFT Mode)



NOTES: A. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{IR}$ goes low after one WCLK plus t_{WFF}. If the time between the rising edge of RLCK and the rising edge of WCLK is less than t_{SKEW1}, the $\overline{IR}$ assertion might be delayed an extra WCLK cycle.

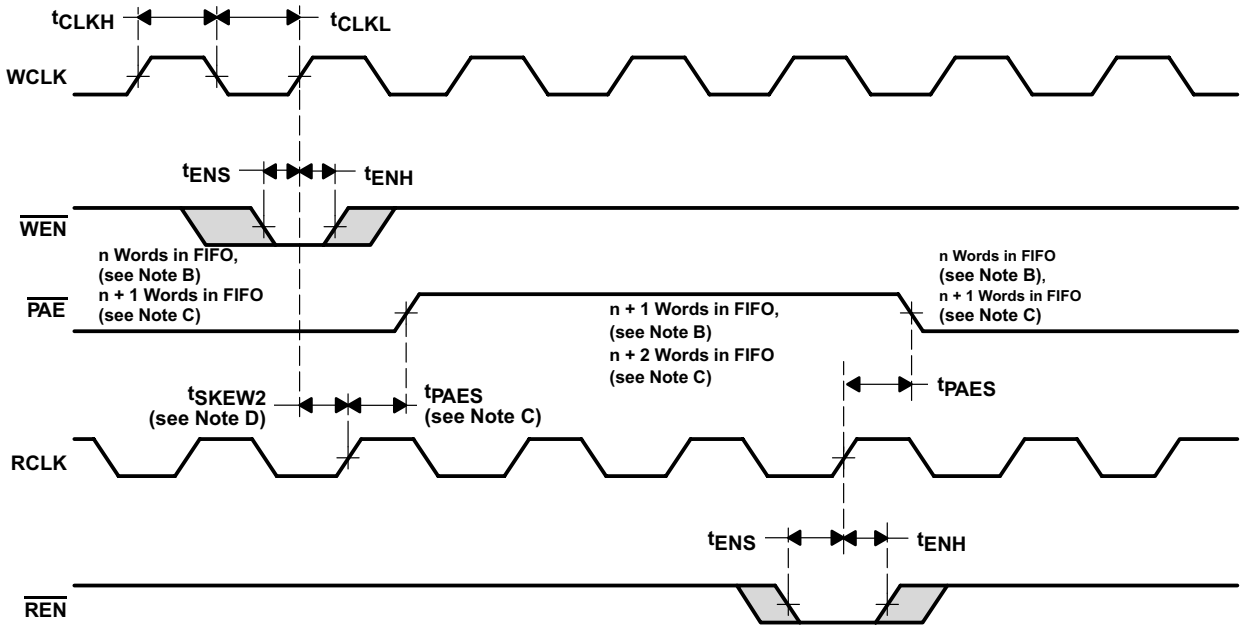
B. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to go high during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, the $\overline{PAF}$ deassertion time may be delayed an extra WCLK cycle.

C. $\overline{LD}$ is high.

D. n = $\overline{PAE}$ offset, m = $\overline{PAF}$ offset, D = maximum FIFO depth = 4097 words

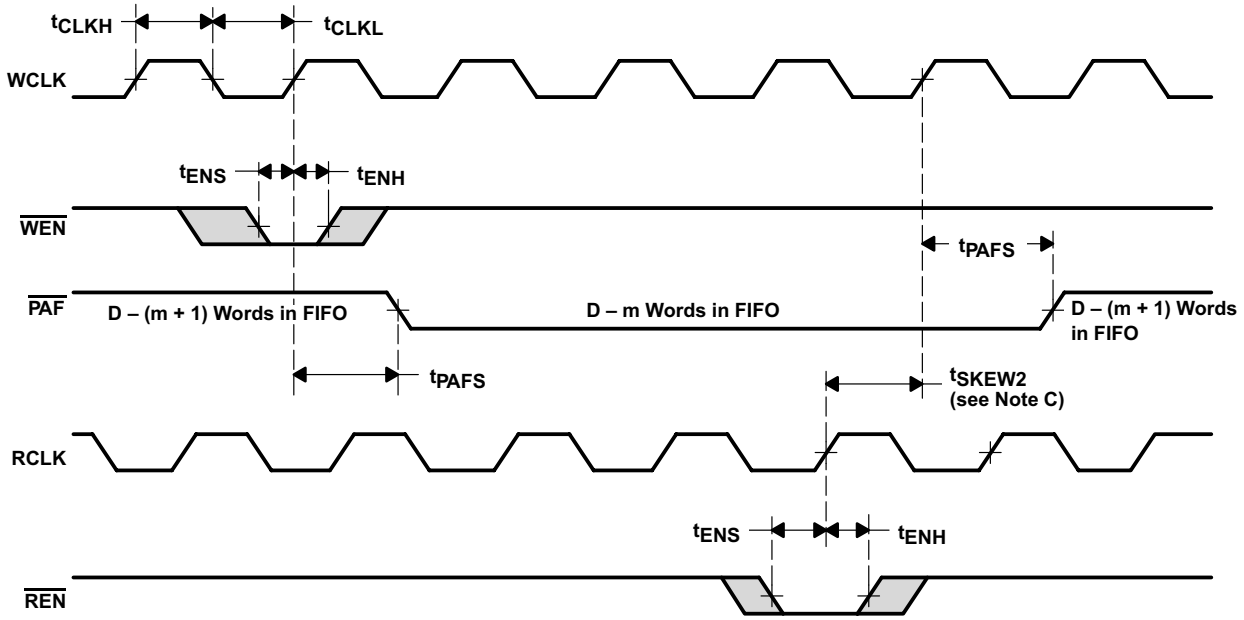
E. Select synchronous FWFT mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (1,0,1) during reset.

Figure 19. Read Timing With Synchronous Programmable Flags (FWFT Mode)



NOTES: A. n = $\overline{PAE}$ offset
B. For standard mode
C. For FWFT mode
D. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to go high during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, the $\overline{PAE}$ deassertion might be delayed one extra RCLK cycle.
E. $\overline{PAE}$ is asserted and updated on the rising edge of RCLK only.
F. Select synchronous modes by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (1,0,0), (1,0,1), or (1,1,0) during reset.

Figure 20. Synchronous Programmable Almost-Empty-Flag Timing (Standard and FWFT Modes)



NOTES: A. m = $\overline{\text{PAF}}$ offset

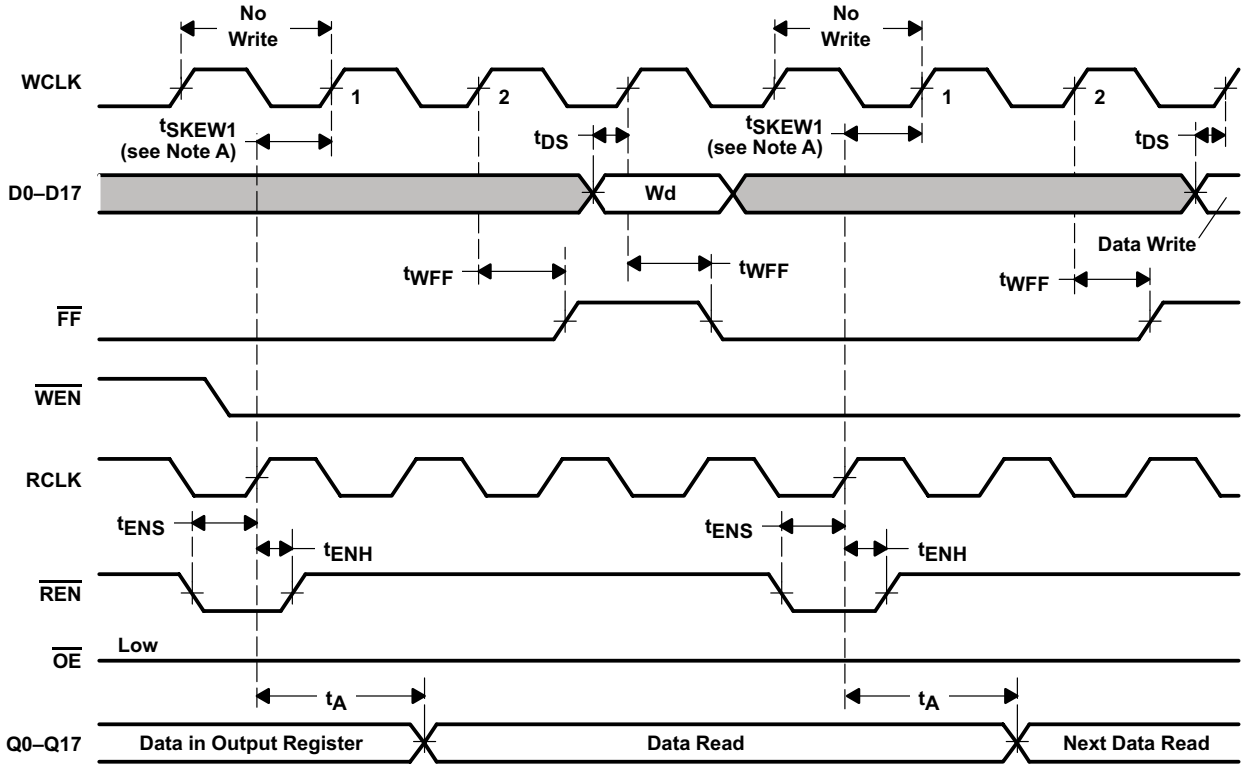
B. D = maximum FIFO depth
In FWFT mode: D = 513 for the SN74V215, 1025 for the SN74V225, 2049 for the SN74V235, and 4097 for the SN74V245.
In standard mode: D = 512 for the SN74V215, 1024 for the SN74V225, 2048 for the SN74V235, and 4096 for the SN74V245.

C. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{\text{PAF}}$ to go high during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, the $\overline{\text{PAF}}$ deassertion time might be delayed an extra WCLK cycle.

D. $\overline{\text{PAF}}$ is asserted and updated on the rising edge of WCLK only.

E. Select synchronous modes by setting ($\overline{\text{FL}}$, $\overline{\text{RXI}}$, $\overline{\text{WXI}}$) = (1,0,0), (1,0,1), or (1,1,0) during reset.

Figure 21. Synchronous Programmable Almost-Full-Flag Timing (Standard and FWFT Modes)

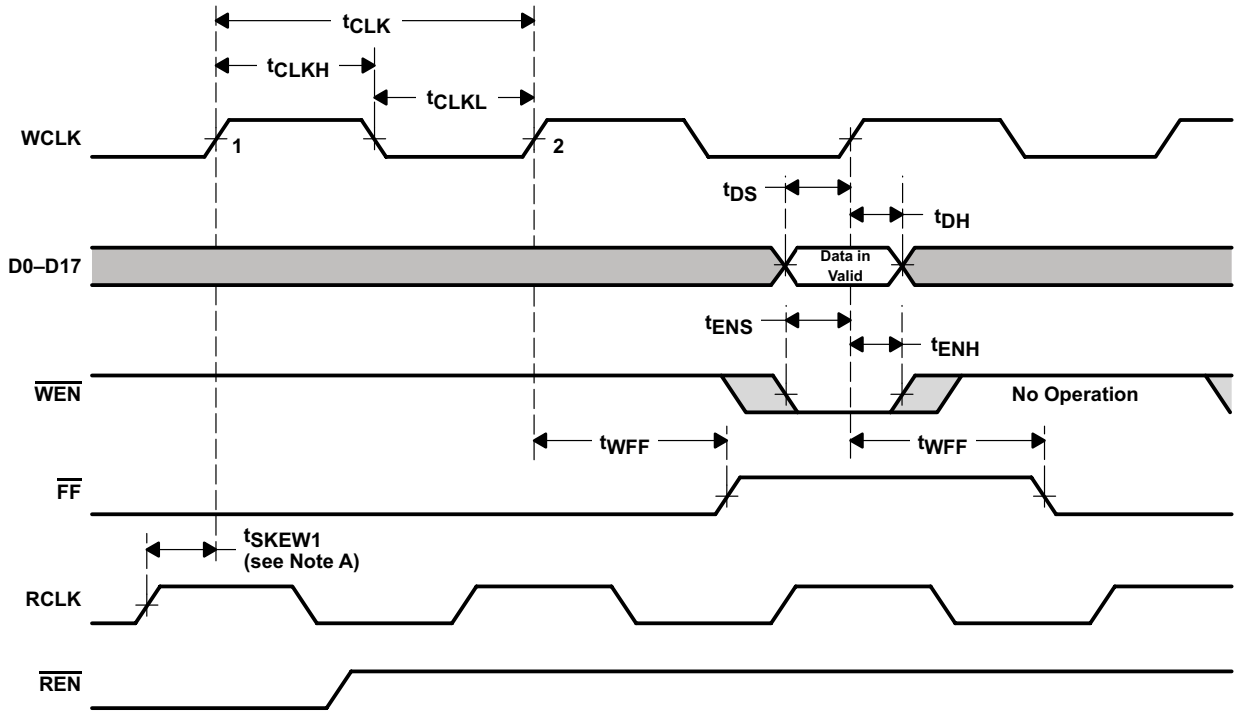


NOTES: A. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{FF}$ goes high after one WCLK cycle plus t_{WFF}. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, the $\overline{FF}$ deassertion time might be delayed an extra WCLK cycle.

B. $\overline{LD}$ is high.

C. Select double register-buffered standard mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,1,0) or (1,1,0) during reset.

Figure 22. Double Register-Buffered Full-Flag Timing (Standard Mode)

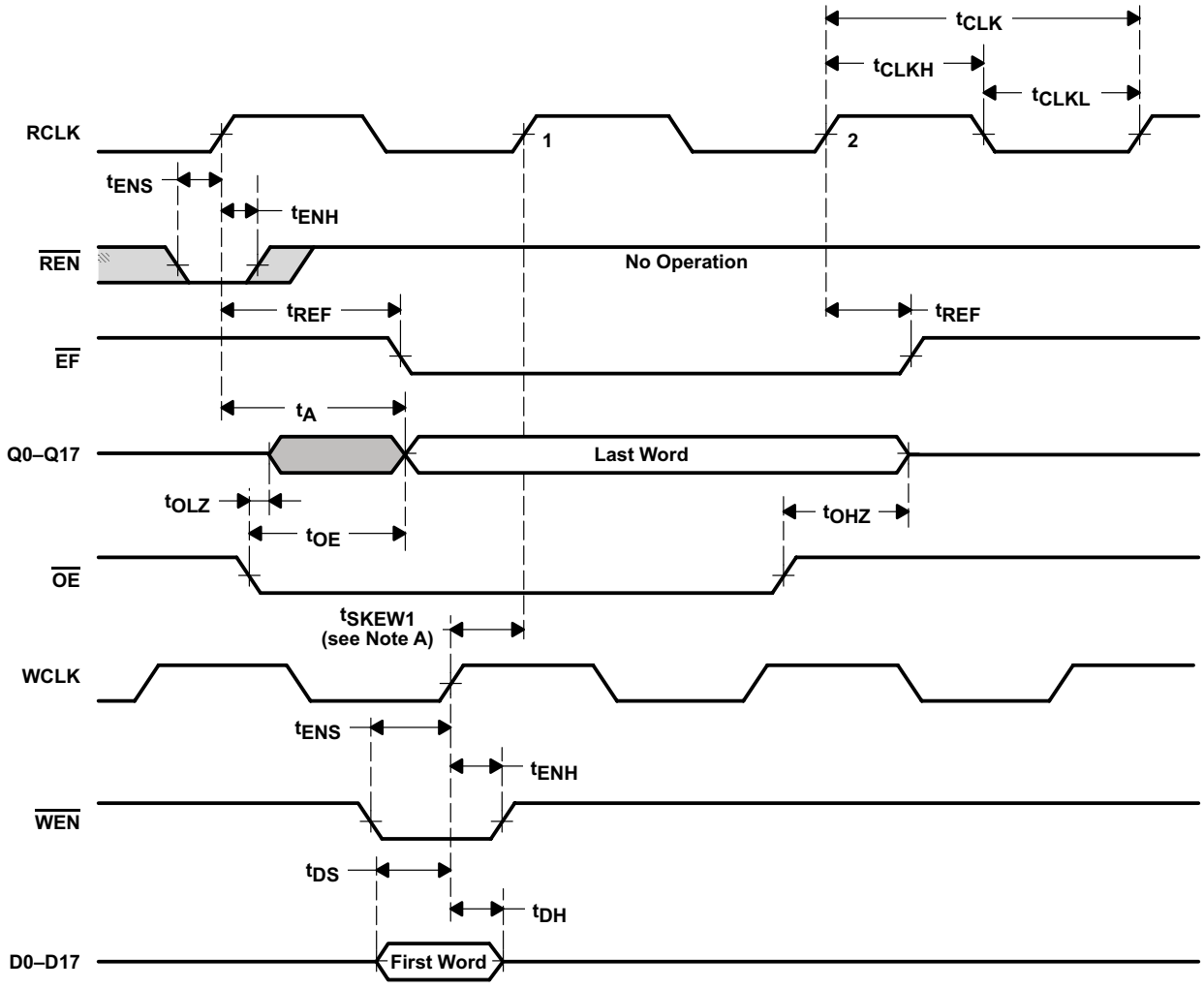


NOTES: A. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to ensure that $\overline{FF}$ goes high after one WCLK cycle plus t_{RFF}. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, the $\overline{FF}$ deassertion might be delayed an extra WCLK cycle.

B. $\overline{LD}$ is high.

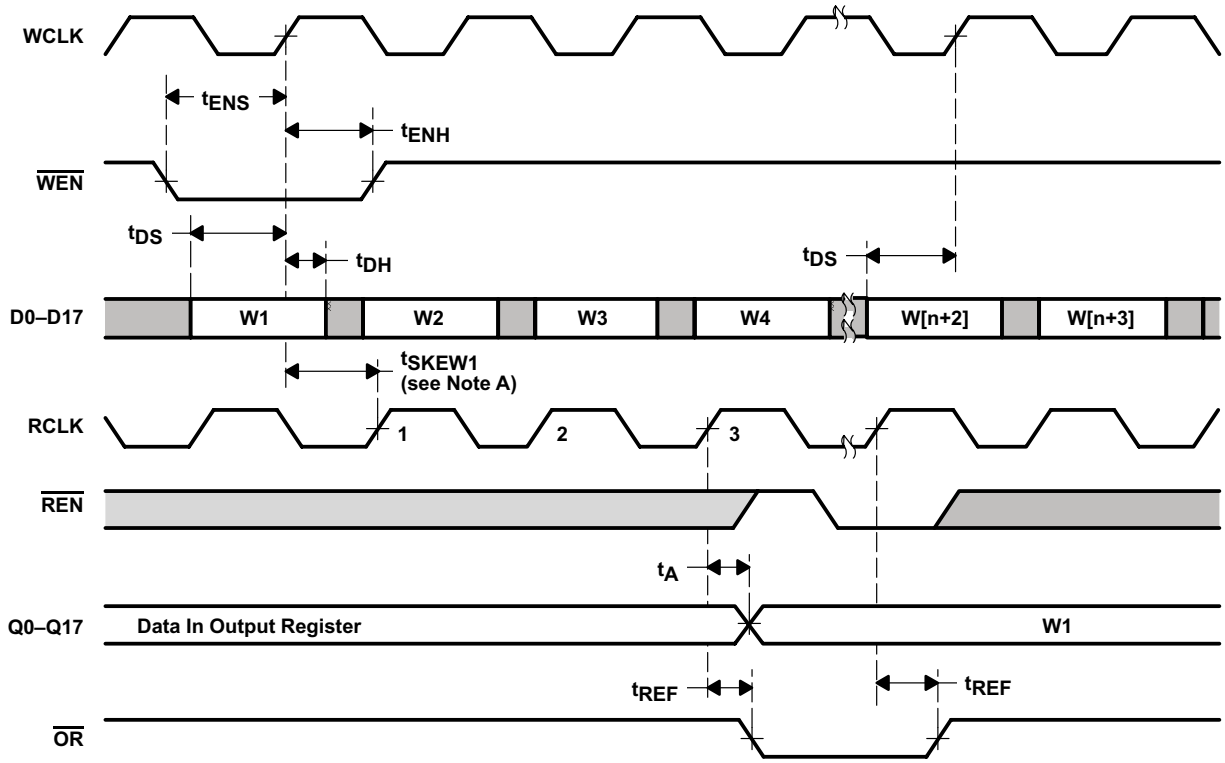
C. Select double register-buffered standard mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,1,0) or (1,1,0) during reset.

Figure 23. Write-Cycle Timing With Double Register-Buffered $\overline{FF}$ (Standard Mode)



NOTES: A. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to ensure that $\overline{EF}$ goes high after one RCLK cycle plus t_{REF}. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, the $\overline{EF}$ deassertion might be delayed an extra RCLK cycle.
B. $\overline{LD}$ is high.
C. Select double register-buffered standard mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,1,0) or (1,1,0) during reset.

Figure 24. Read-Cycle Timing With Double Register-Buffered $\overline{EF}$ (Standard Timing)



NOTES: A. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{OR}$ to go high during the current cycle. If the time between the rising edge of WLCK and the rising edge of RCLK is less than t_{SKEW1}, the $\overline{OR}$ deassertion might be delayed one extra RCLK cycle.

B. $\overline{LD}$ is high, $\overline{OE}$ is low.

C. Select FWFT mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,0,1) or (1,0,1) during reset.

Figure 25. $\overline{OR}$-Flag Timing and First Word Fall Through When FIFO is Empty (FWFT mode)

OPERATING CONFIGURATIONS

SINGLE-DEVICE CONFIGURATION

A single SN74V245 can be used when the application requirements are for 4096 words or fewer. These FIFOs are in a single-device configuration when the first load ($\overline{FL}$), write expansion in ($\overline{WXI}$) and read expansion in ($\overline{RXI}$) control inputs are configured as ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$ = (0,0,0), (0,0,1), (0,1,0), (1,0,0), (1,0,1) or (1,1,0) during reset (see Figure 26).

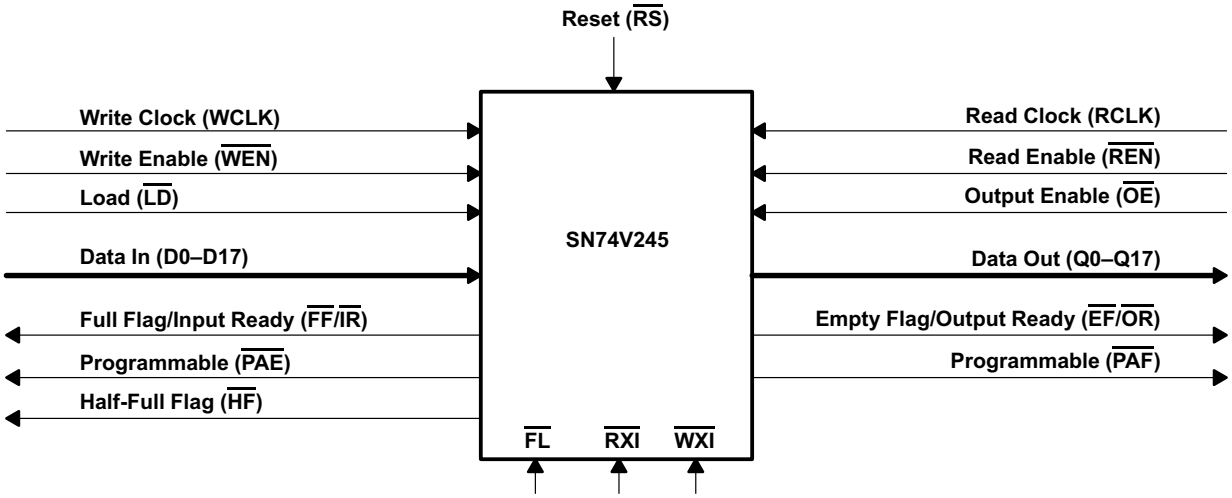
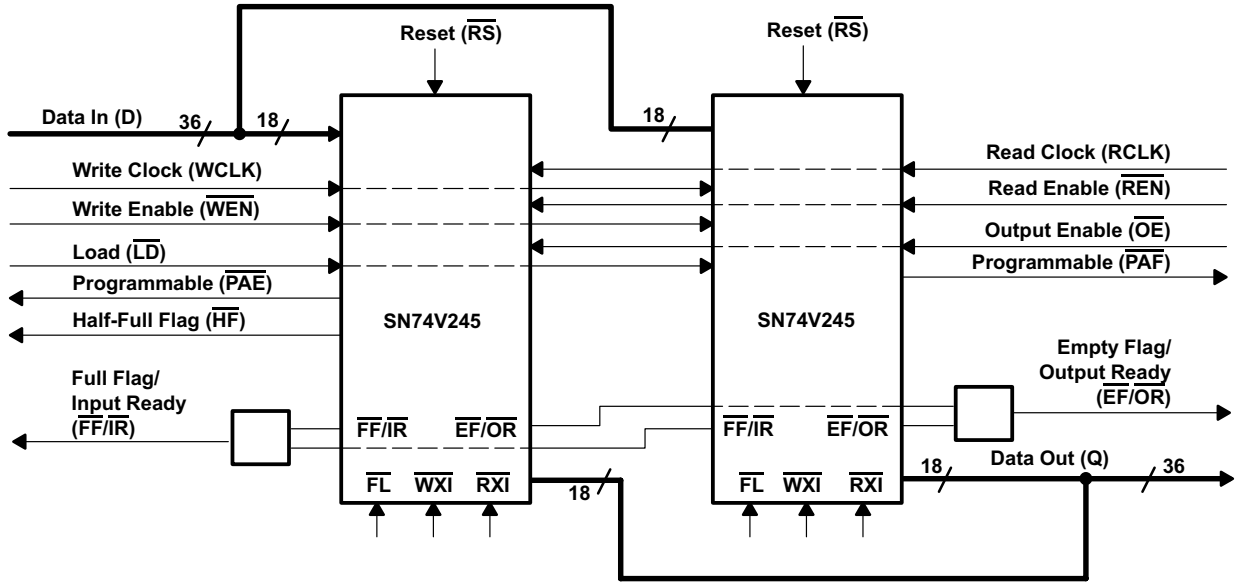


Figure 26. Block Diagram of Single 4096 × 18 Synchronous FIFO

WIDTH-EXPANSION CONFIGURATION

Word width may be increased simply by connecting together the control signals of multiple devices. Status flags can be detected from any one device. The exceptions are the empty flag/output ready and full flag/input ready. Because of variations in skew between RCLK and WCLK, it is possible for flag assertion and deassertion to vary by one cycle between FIFOs. To avoid problems, the user must create composite flags by gating the empty flags/output ready of every FIFO, and separately gating all full flags/input ready. Figure 27 demonstrates a 36-word width by using two SN74V245 memories. Any word width can be attained by adding additional SN74V245 memories. These FIFOs are in a single-device configuration when the first load ($\overline{FL}$), write expansion in ($\overline{WXI}$), and read expansion in ($\overline{RXI}$) control inputs are configured as ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$ = (0,0,0), (0,0,1), (0,1,0), (1,0,0), (1,0,1) or (1,1,0) during reset (see Figure 27).

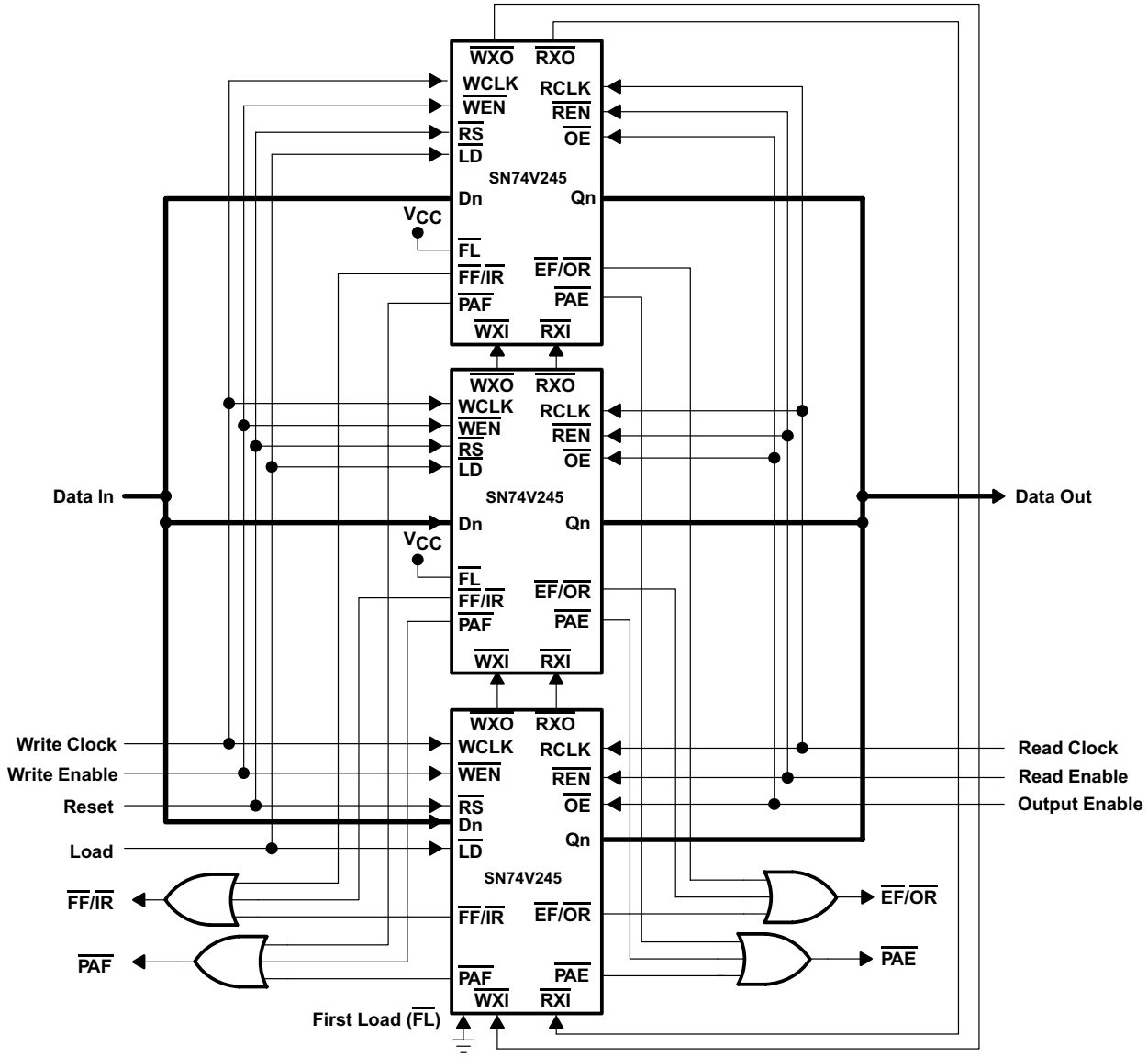


NOTE A: Do not connect any output control signals directly together.

Figure 27. Block Diagram of 4096 × 36 Synchronous FIFO Memory Used in a Width-Expansion Configuration

DEPTH-EXPANSION CONFIGURATION, DAISY-CHAIN TECHNIQUE (WITH PROGRAMMABLE FLAGS)

These devices can be adapted easily to applications requiring more than 4096 words of buffering. Figure 28 shows depth expansion using three SN74V245 memories. Maximum depth is limited only by signal loading.



NOTES: A. The first device must be designated by grounding the first load ($\overline{FL}$) control input.
B. All other devices must have $\overline{FL}$ in the high state.
C. The write expansion out ($\overline{WXO}$) pin of each device must be tied to the write expansion in ($\overline{WXI}$) pin of the next device.
D. The read expansion out ($\overline{RXO}$) pin of each device must be tied to the read expansion in ($\overline{RXI}$) pin of the next device.
E. All load ($\overline{LD}$) pins are tied together.
F. The half-full flag ($\overline{HF}$) is not available in this depth-expansion configuration.
G. $\overline{EF}$, $\overline{FF}$, $\overline{PAE}$, and $\overline{PAF}$ are created with composite flags by ORing together every respective flag for monitoring. The composite $\overline{PAE}$ and $\overline{PAF}$ flags are not precise.
H. In daisy-chain mode, the flag outputs are single-register buffered and the partial flags are in asynchronous timing mode.

Figure 28. Block Diagram of 12288 × 18 Synchronous FIFO Memory With Programmable Flags Used in Depth-Expansion Configuration

DEPTH-EXPANSION CONFIGURATION (FWFT MODE)

In FWFT mode, the FIFOs can be connected in series (the data outputs of one FIFO connected to the data inputs of the next) with no external logic necessary. The resulting configuration provides a total depth equivalent to the sum of the depths associated with each single FIFO. NO TAG shows a depth expansion using two SN74V245 memories.

Care should be taken to select FWFT mode during master reset for all FIFOs in the depth expansion configuration. The first word written to an empty configuration passes from one FIFO to the next (ripple down) until it finally appears at the outputs of the last FIFO in the chain. No read operation is necessary, but the RCLK of each FIFO must be free running. Each time the data word appears at the outputs of one FIFO, that device's OR line goes low, enabling a write to the next FIFO in line.

For an empty expansion configuration, the amount of time it takes for $\overline{OR}$ of the last FIFO in the chain to go low (i.e., valid data to appear on the last FIFO's outputs) after a word has been written to the first FIFO is the sum of the delays for each individual FIFO:

$$(N - 1) \times (4 \times \text{transfer clock}) + 3 \times T_{RCLK} \quad (1)$$

Where: N is the number of FIFOs in the expansion and T_{RCLK} is the RCLK period. Extra cycles should be added for the possibility that the t_{SKEW1} specification is not met between WCLK and transfer clock, or RCLK and transfer clock, for the $\overline{OR}$ flag.

The ripple-down delay is noticeable only for the first word written to an empty depth-expansion configuration. There is no delay evident for subsequent words written to the configuration.

The first free location created by reading from a full depth-expansion configuration bubbles up from the last FIFO to the previous one until finally it moves into the first FIFO of the chain. Each time a free location is created in one FIFO of the chain, that FIFO's $\overline{IR}$ line goes low, enabling the preceding FIFO to write a word to fill it.

For a full expansion configuration, the amount of time it takes for $\overline{IR}$ of the first FIFO in the chain to go low after a word has been read from the last FIFO is the sum of the delays for each individual FIFO:

$$(N - 1) \times (3 \times \text{transfer clock}) + 2T_{WCLK} \quad (2)$$

Where: N is the number of FIFOs in the expansion and T_{WCLK} is the WCLK period. Extra cycles should be added for the possibility that the t_{SKEW1} specification is not met between RCLK and transfer clock, or WCLK and transfer clock, for the $\overline{IR}$ flag.

The transfer clock line should be tied to either WCLK or RCLK, whichever is faster. Both these actions result in data moving, as quickly as possible, to the end of the chain and free locations to the beginning of the chain.

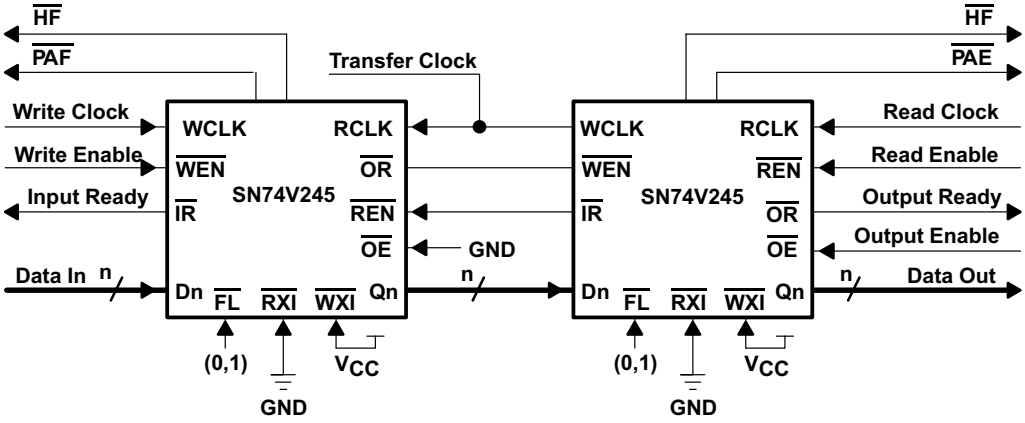


Figure 29. Block Diagram of 8192 × 18 Synchronous FIFO Memory With Programmable Flags Used in Depth-Expansion Configuration

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74V245-15PAGEP	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	V245-15EP
SN74V245-15PAGEP.A	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	V245-15EP
V62/13606-01XE	Active	Production	TQFP (PAG) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	V245-15EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

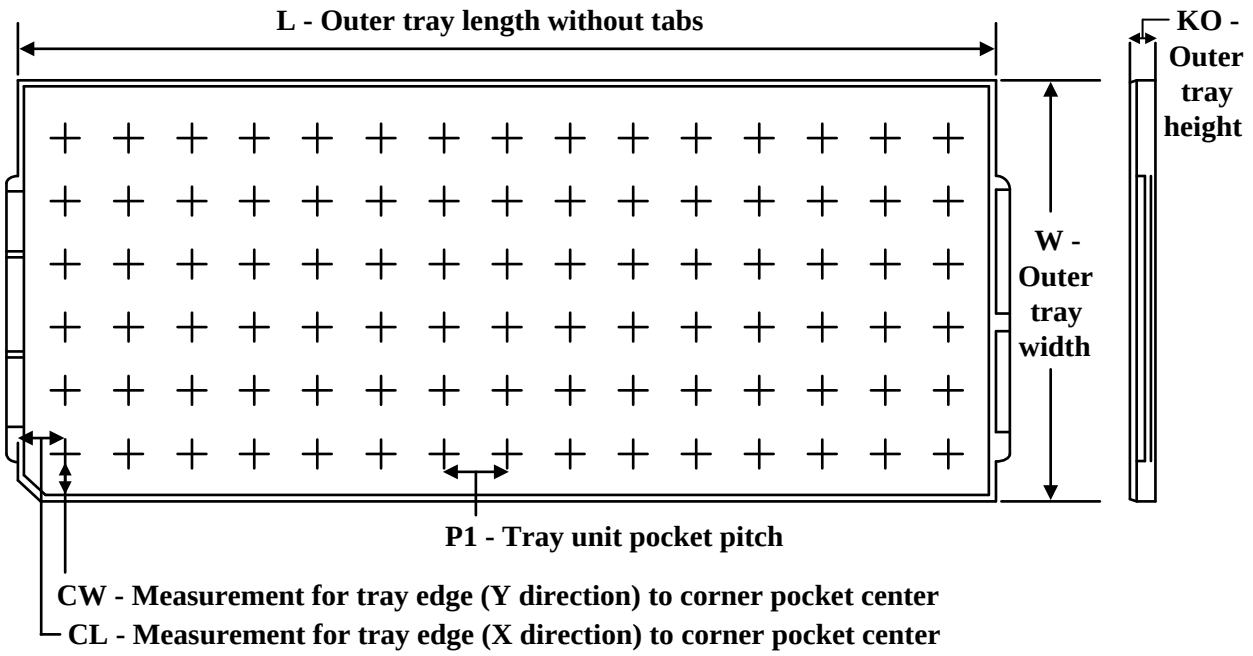
OTHER QUALIFIED VERSIONS OF SN74V245-EP :

- Catalog : SN74V245

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TRAY

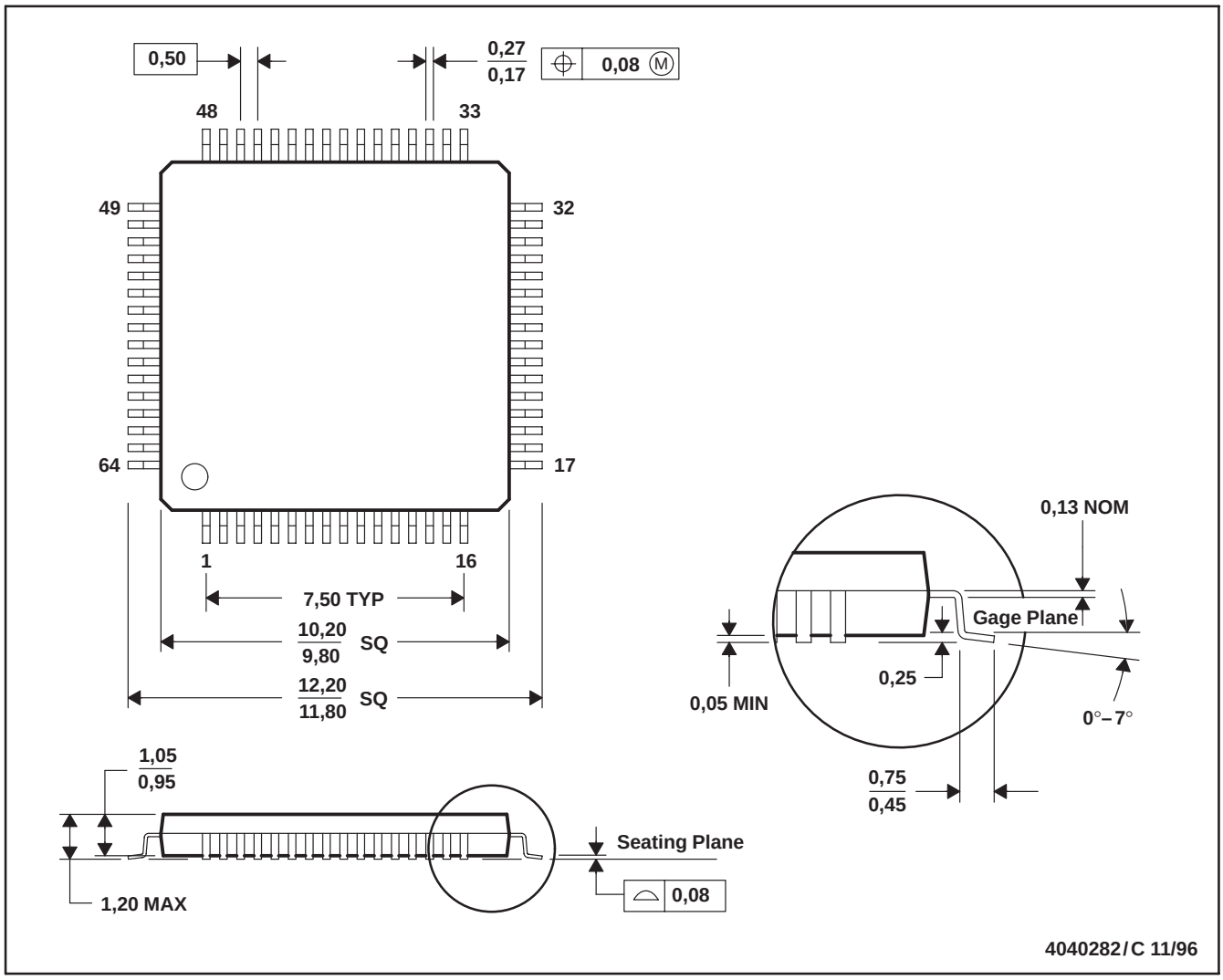


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

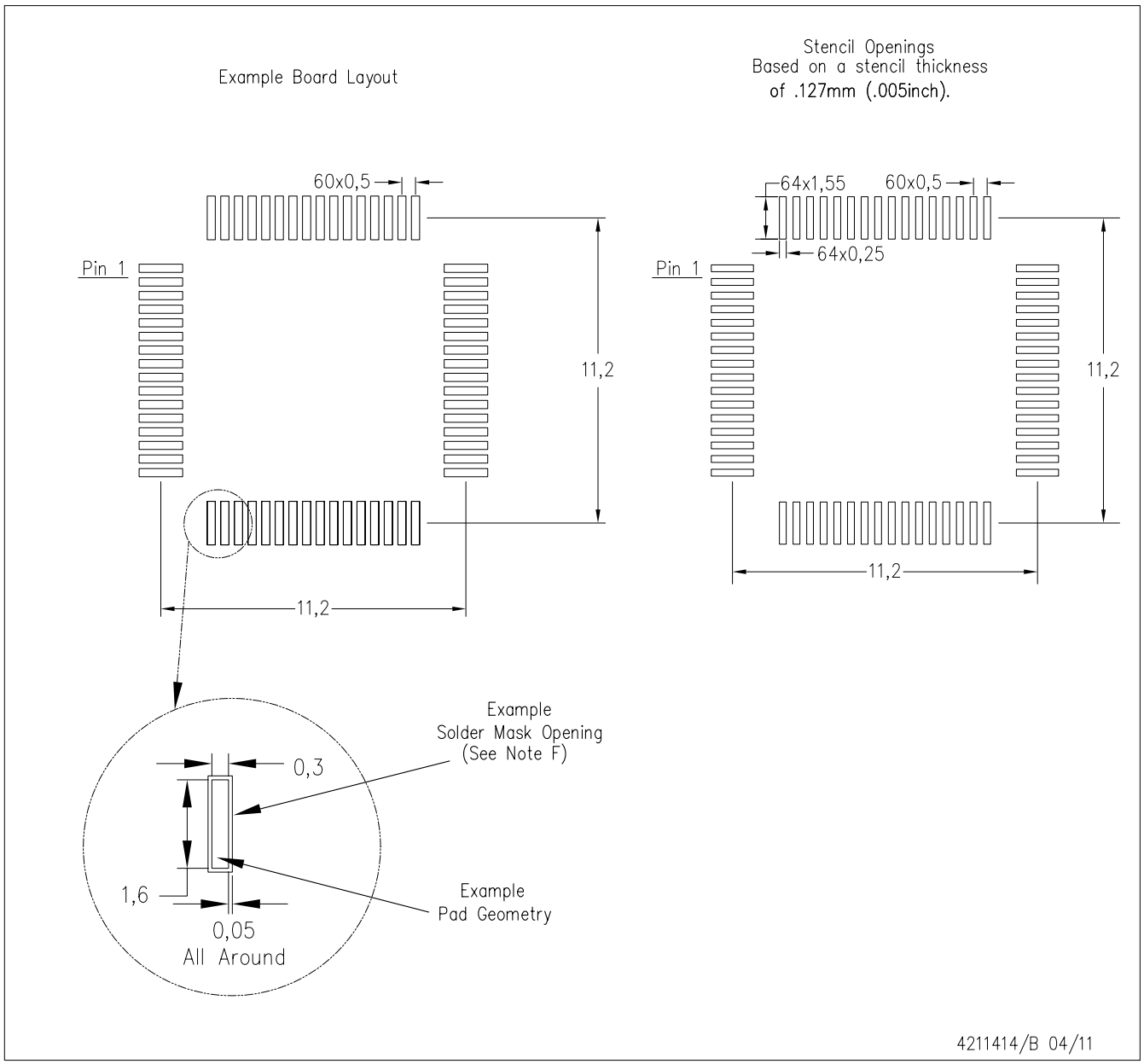
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SN74V245-15PAGEP	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
SN74V245-15PAGEP.A	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
V62/13606-01XE	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



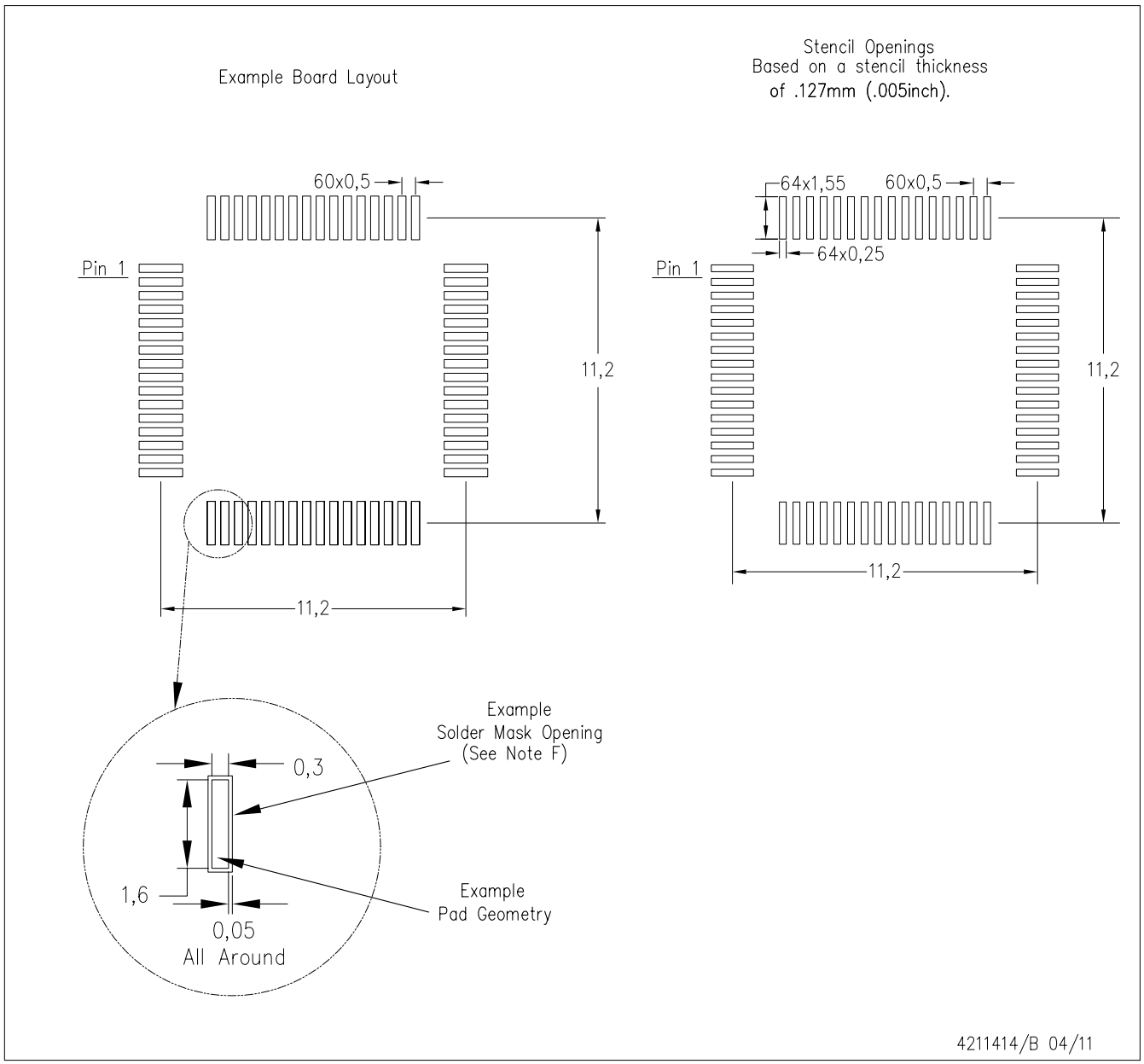
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PAG (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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