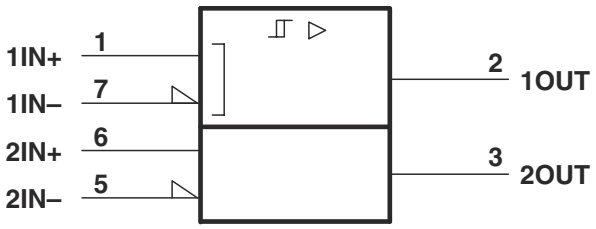
SN75157 双路差分线路接收器

1 特性

- 符合或超出 ANSI 标准 EIA/TIA-422-B 和 EIA/TIA-423-B 以及 ITU 建议 V.10 和 V.11 的要求
- 单一 5V 电源供电下工作
- 宽共模电压范围
- 高输入阻抗
- 兼容 TTL 的输出
- 高速肖特基电路
- 8 引脚双列直插式封装

2 应用

- 工厂自动化
- 交流和伺服电机驱动器



逻辑符号†

3 说明

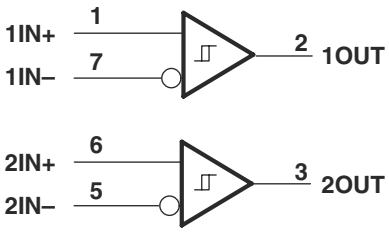
SN75157 是一款双路差分线路接收器，符合 EIA/TIA-422-B 和 EIA/TIA-423-B 标准以及 ITU V.10 和 V.11 规范的要求。该器件采用肖特基电路，并具有 TTL 兼容输出。输入与单端或差分线路系统兼容。该器件由单一 5V 电源供电，采用 8 引脚双列直插式封装和小外形封装。

SN75157 的工作温度范围是 0°C 至 70°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
SN75157	SOIC（D，8）	4.9mm × 6mm
	PDIP（P，8）	9.81mm × 9.43mm
	SOP（PS，8）	6.2mm x 7.8mm

(1) 有关更多信息，请参阅 节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）

† 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

Table of Contents

4 Pin Configuration and Functions

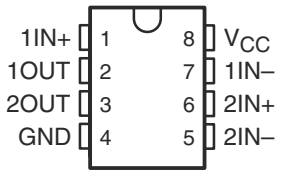


图 4-1. D, P, OR PS Package
(Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1IN+	1	I	Non-Inverting Differential Input for Channel 1's Differential Receiver
1OUT	2	O	Single Ended Output for Channel 1 Differential Receiver
2OUT	3	O	Single Ended Output for Channel 2 Differential Receiver
GND	4	GND	Device Ground
2IN-	5	I	Inverting Differential Input for Channel 2's Differential Receiver
2IN+	6	I	Non-Inverting Differential Input for Channel 2's Differential Receiver
1IN-	7	I	Inverting Differential Input for Channel 1's Differential Receiver
V_{CC}	8	POW	5V (+/-5%) Positive Supply Connection Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, POW = Power, GND = Ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	– 0.5	7	V
V_I	Input voltage range		±15	V
V_{ID}	Differential input voltage(3)		±15	v
V_O	Output voltage range(2)	– 0.5	5.5	V
I_{OL}	Low-level output current		50	mA
	Continuous total dissipation		See Dissipation Ratings	
T_J	Operating free-air temperature range	0	70	°C
T_{stg}	Storage temperature range	– 65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 s		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input voltage, are with respect to the network ground terminal.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Ratings

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A \leq 70°C$ POWER RATING
D	725mW	5.8mW/°C	464mW
P	1000mW	8.0mW/°C	640mW
PS	450mW	3.6mW/°C	288mW

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IC}	Common-mode input voltage			±7	V
T_A	Operating free-air temperature	0	25	70	°C

5.4 Thermal Resistance Characteristics

THERMAL METRIC(1)		D (SOIC)	P (PIDP)	PS (SOP)	UNIT
		8 Pins	8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	84.3	89.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	65.4	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	62.1	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	31.3	23.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	60.4	60.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage,common-mode input voltage, and operating free-air temperature (unless otherwise noted)(4)

PARAMETER		TEST CONDITIONS		MIN	TYP(5)	MAX	UNIT
V_{IT}	Input threshold voltage (V_{IT+} and V_{IT-})(2)			−0.2		0.2	V
				−0.4		0.4	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2V,	I_O = −1mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2V,	I_O = 20mA		0.35	0.5	V
I_I	Input current(3)	V_{CC} = 0 to 5.5V,	V_I = 10V		1.1	3.25	mA
			V_I = −1 V		−1.6	−3.25	
I_{OS}	Short-circuit output current(1)	V_O = 0V,	V_{ID} = 0.2V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5V,	No load		35	50	mA

(1) Only one output should be shorted at a time and duration of the short circuit should not exceed one second.
(2) The expanded threshold parameter is tested with a 500-W resistor in series with each input.
(3) The input not under test is grounded.
(4) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
(5) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.6 Switching Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15pF, see 图 6-1		15	25	ns
t_{PHL}	Propagation delay time,high- to low-level output			13	25	ns

5.7 Typical Characteristics

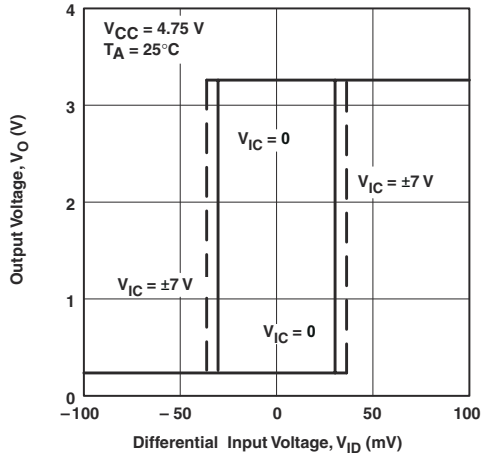


图 5-1. Output Voltage vs Differential Input Voltage

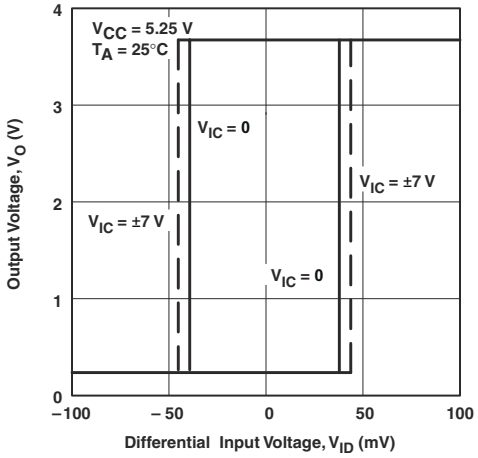


图 5-2. Output Voltage vs Differential Input Voltage

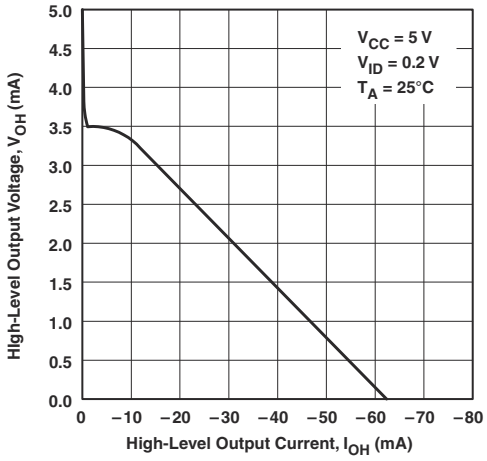


图 5-3. High-Level Output Voltage vs High-Level Output Current

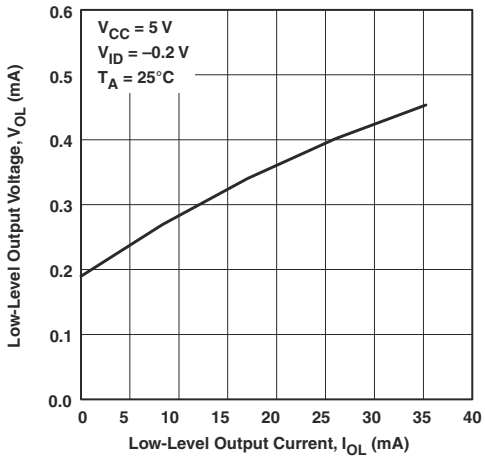


图 5-4. Low-Level Output Voltage vs Low-Level Output Current

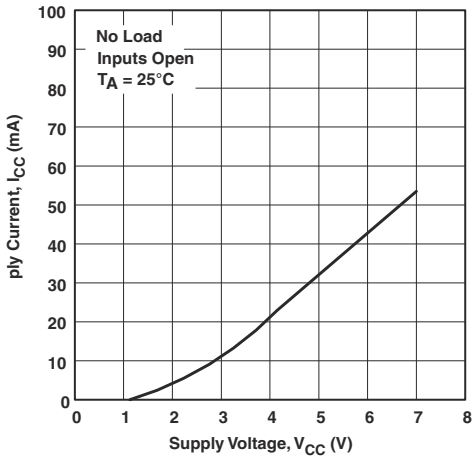
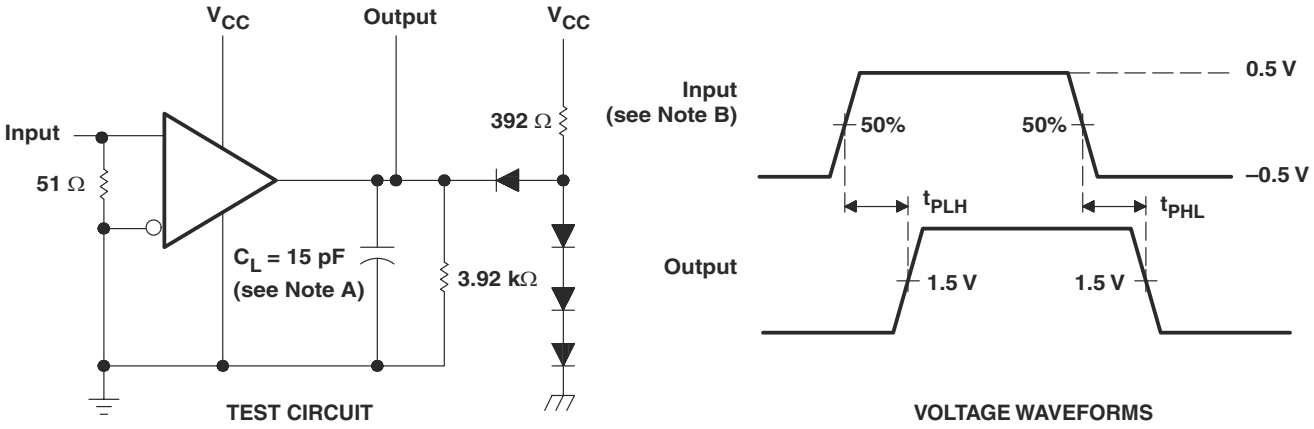


图 5-5. Supply Current vs Supply Voltage

Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: $t_r \leqslant 5$ ns, $t_f \leqslant 5$ ns, PRR $\leqslant 5$ MHz, duty cycle = 50%.

图 6-1. Test Circuit and Voltage Waveforms

6 Detailed Description

6.1 Device Functional Modes

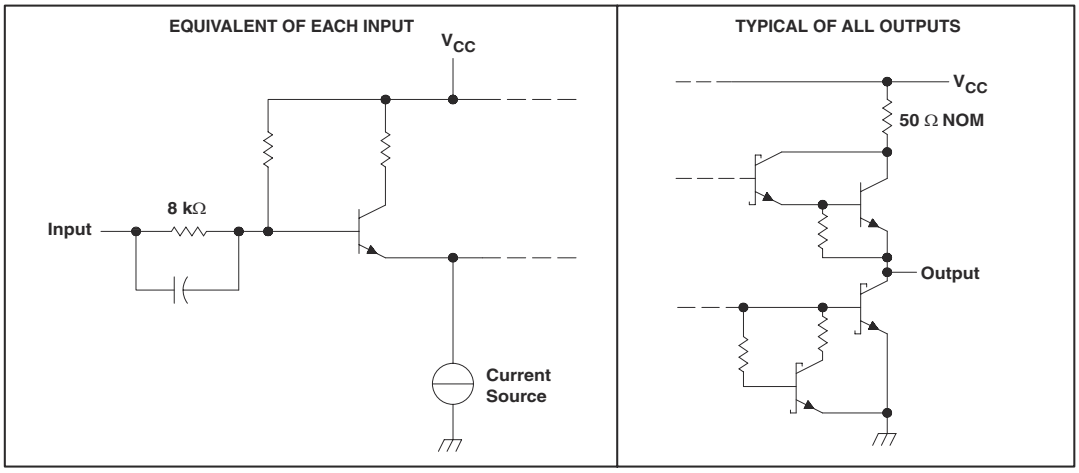


图 6-1. Schematics of Inputs and Outputs

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Typical Application

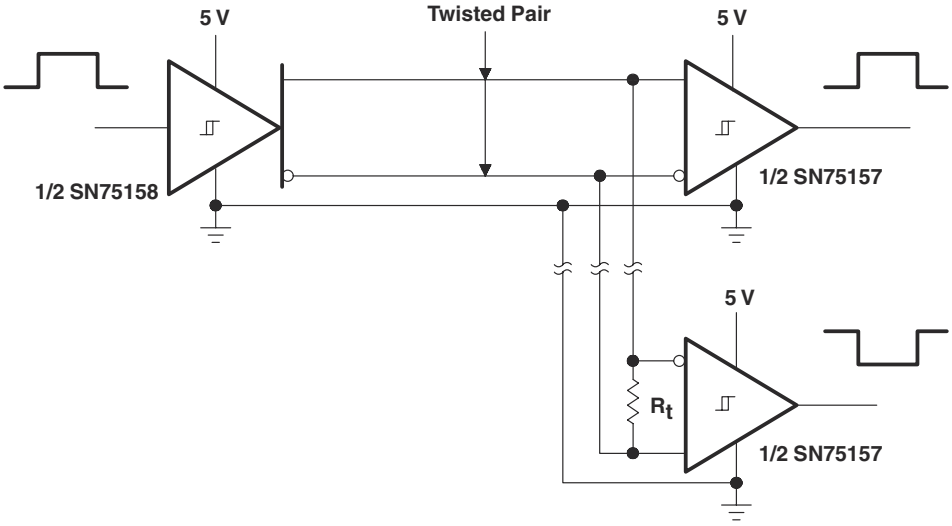


图 7-1. EIA/TIA-422-B System Application

8 Device and Documentation Support

8.1 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.2 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.3 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.4 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (March 1997) to Revision D (January 2024)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75157D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	75157
SN75157DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75157
SN75157DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75157
SN75157P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75157P
SN75157P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75157P
SN75157PSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A157
SN75157PSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A157

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

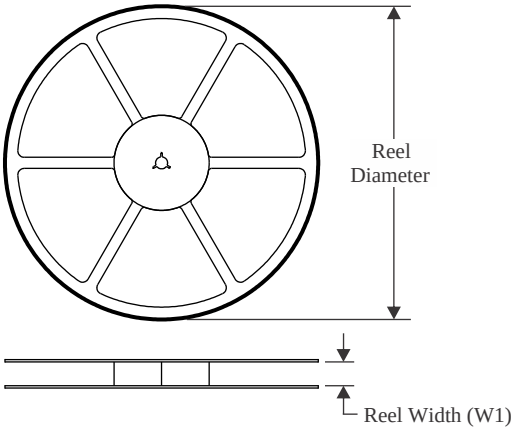
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

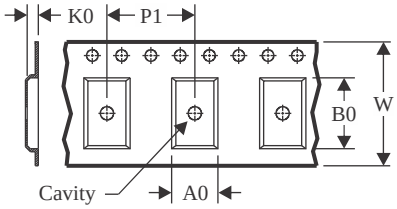
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

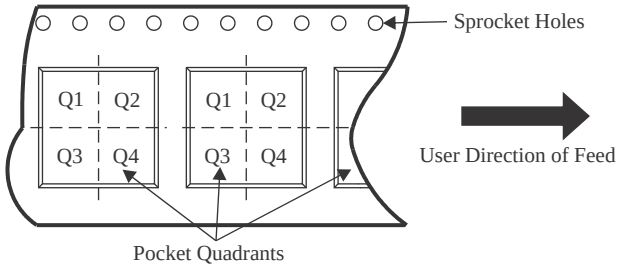


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

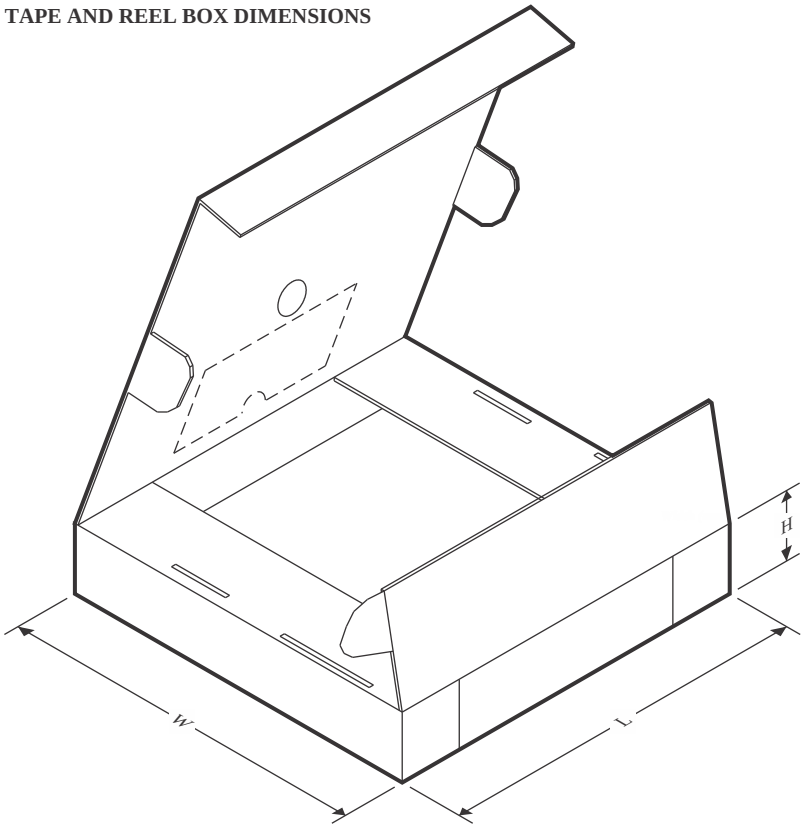
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75157DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75157DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75157PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

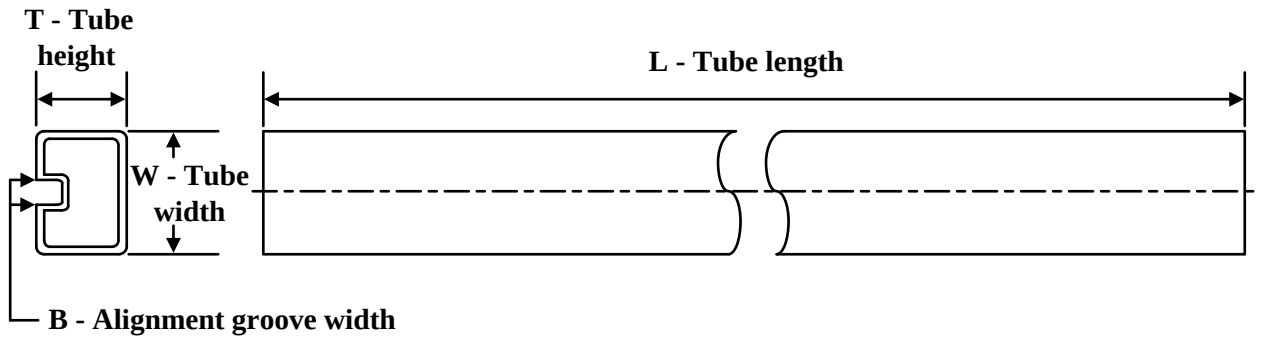
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

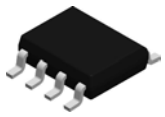
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75157DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75157DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75157PSR	SO	PS	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75157P	P	PDIP	8	50	506	13.97	11230	4.32
SN75157P.A	P	PDIP	8	50	506	13.97	11230	4.32

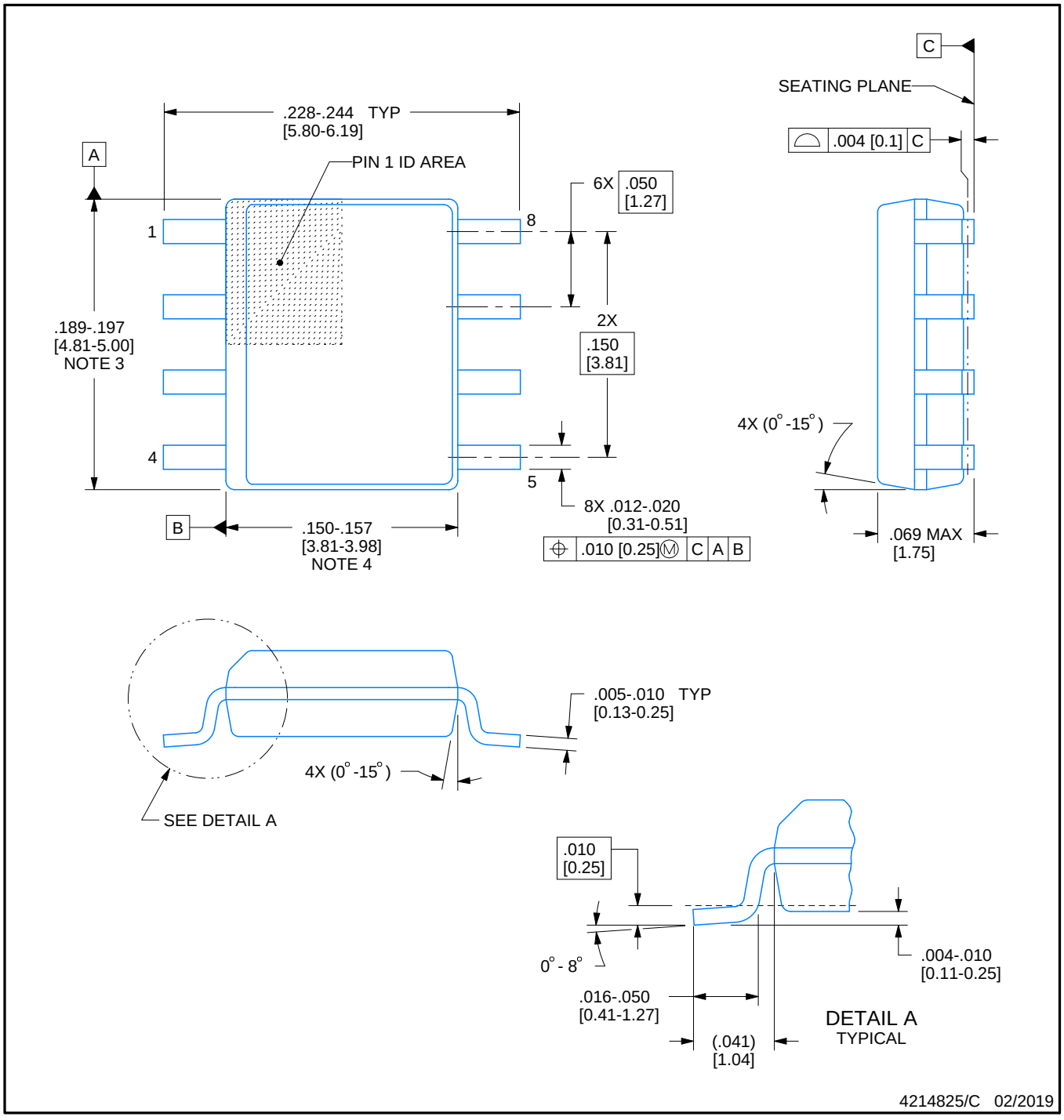


PACKAGE OUTLINE

D0008A

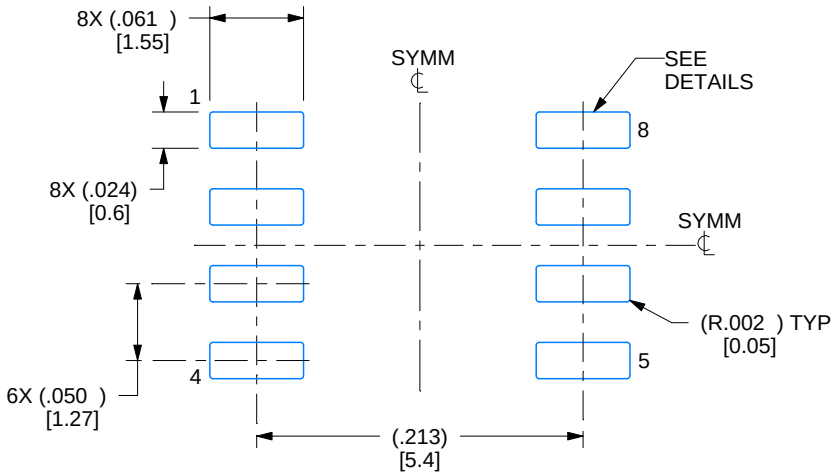
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

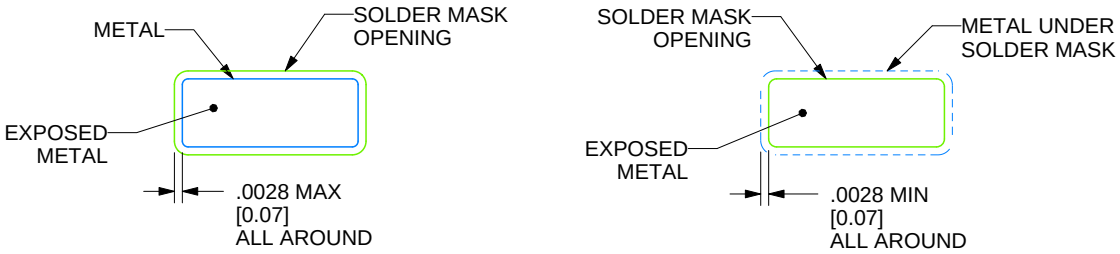


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

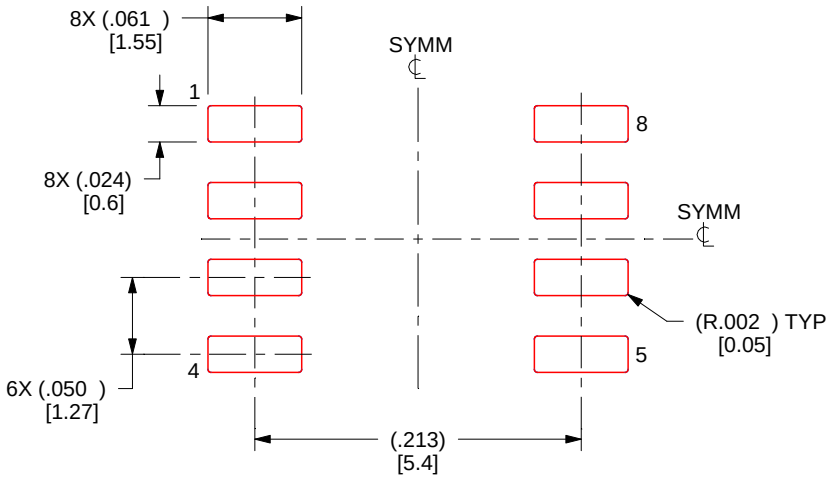
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

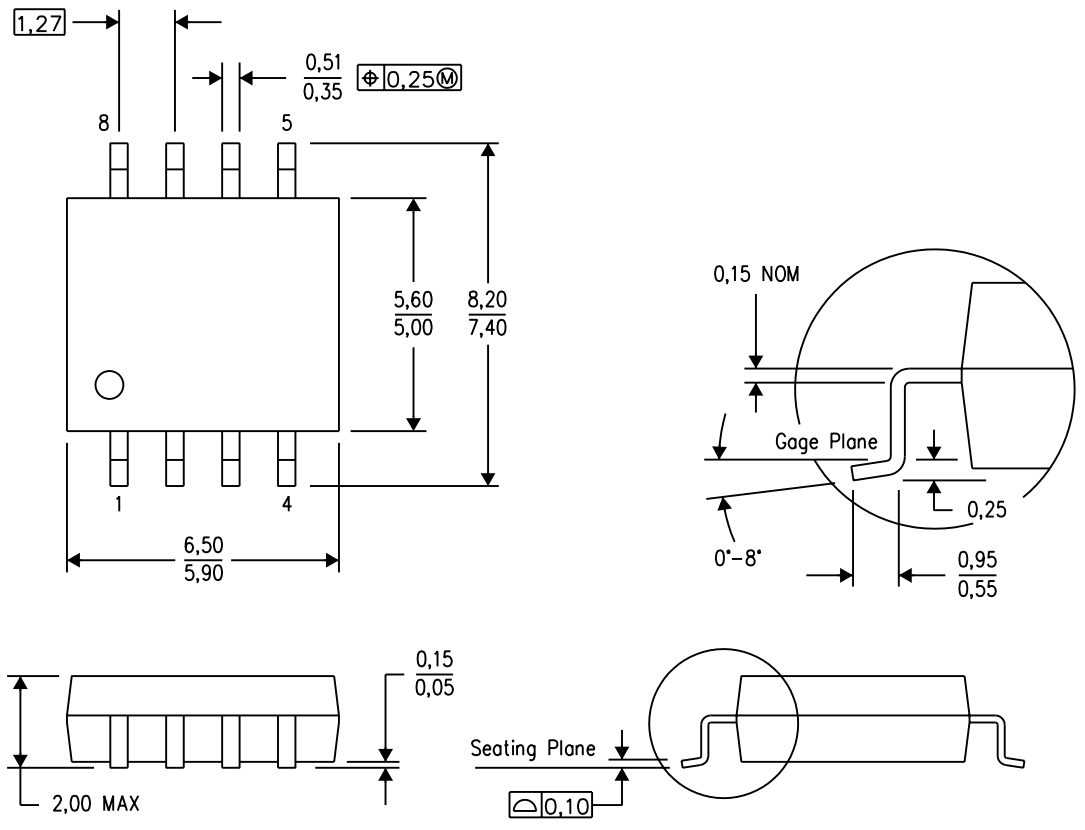
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

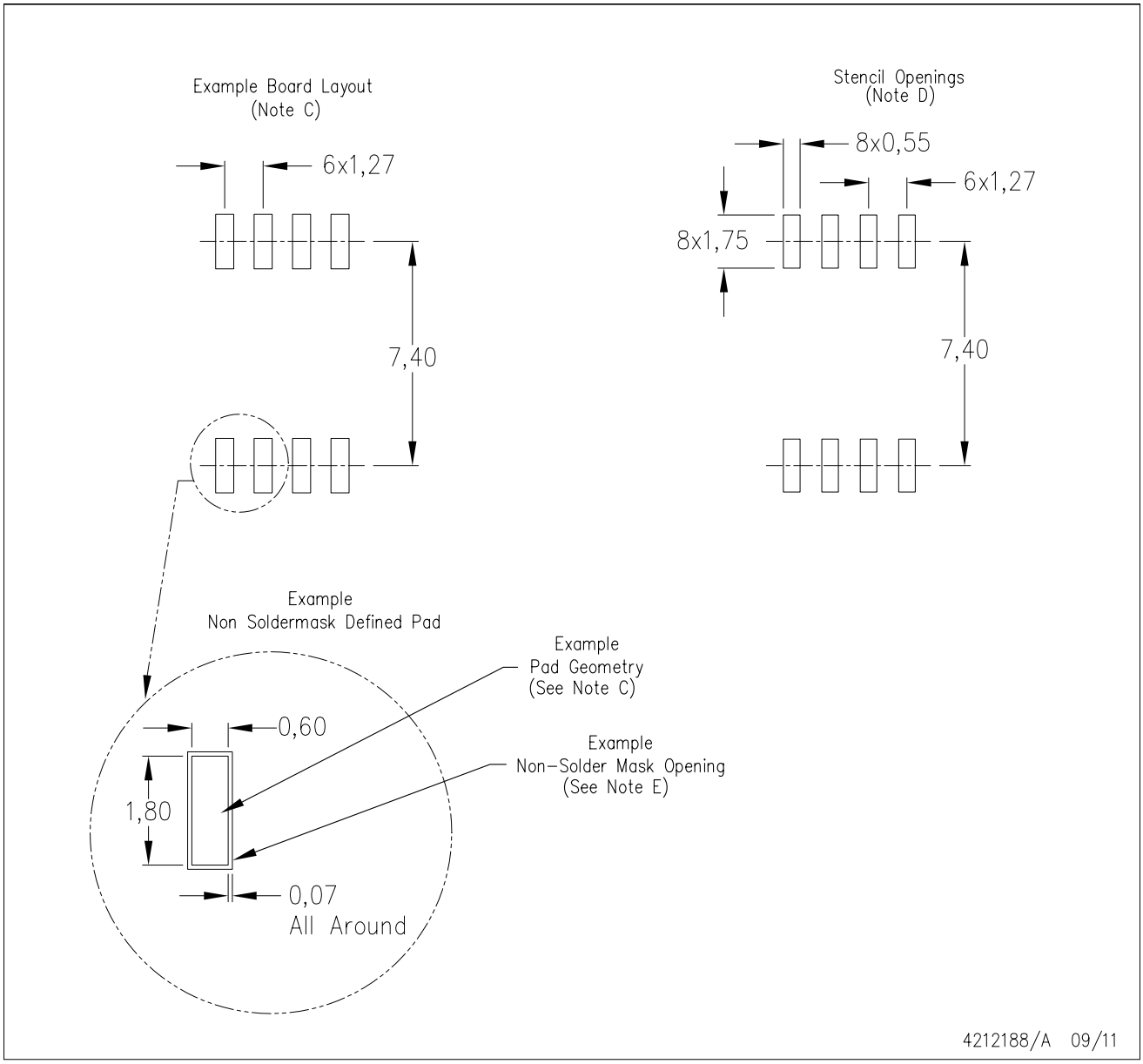
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

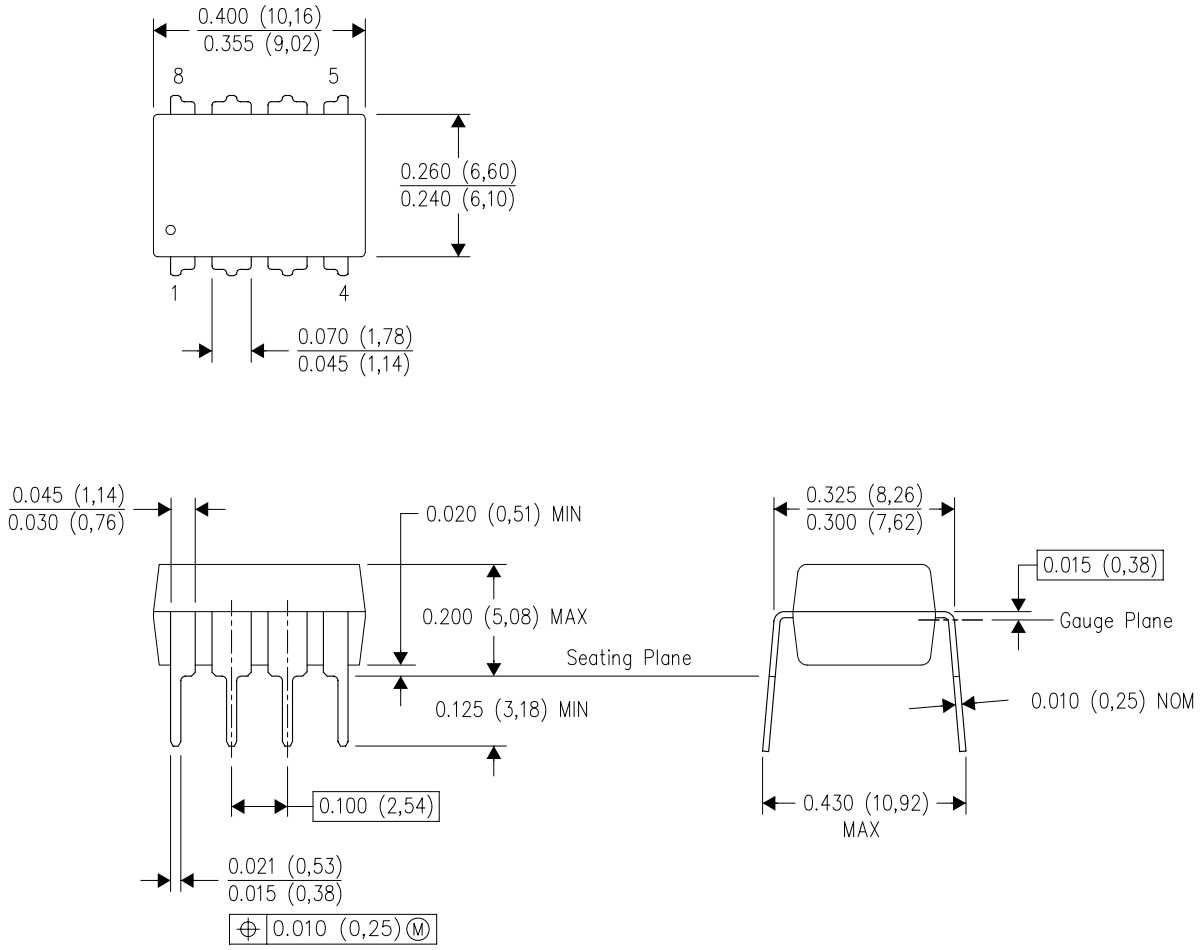
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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