

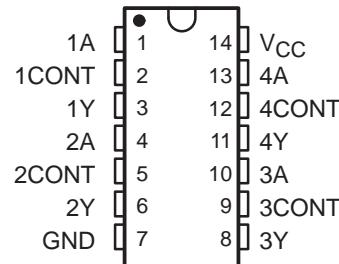
- Input Resistance . . . 3 k Ω to 7 k Ω
- Input Signal Range . . . ± 30 V
- Operate From Single 5-V Supply
- Built-In Input Hysteresis (Double Thresholds)
- Response Control that Provides:
 - Input Threshold Shifting
 - Input Noise Filtering
- Meet or Exceed the Requirements of TIA/EIA-232-F and ITU Recommendation V.28
- Fully Interchangeable With MotorolaTM MC1489 and MC1489A

description

These devices are monolithic low-power Schottky quadruple line receivers designed to satisfy the requirements of the standard interface between data-terminal equipment and data-communication equipment as defined by TIA/EIA-232-F. A separate response-control (CONT) terminal is provided for each receiver. A resistor or a resistor and bias-voltage source can be connected between this terminal and ground to shift the input threshold levels. An external capacitor can be connected between this terminal and ground to provide input noise filtering.

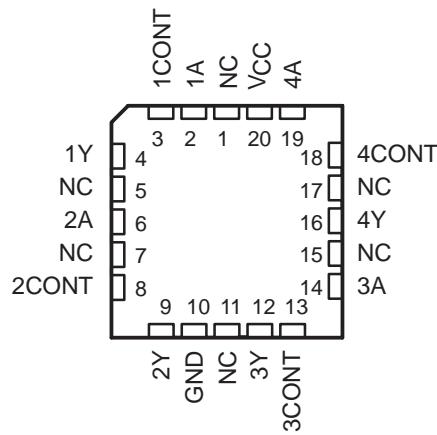
The SN55189 and SN55189A are characterized for operation over the full military temperature range of -55°C to 125°C . The MC1489, MC1489A, SN75189, and SN75189A are characterized for operation from 0°C to 70°C .

SN55189, SN55189A . . . J OR W PACKAGE
MC1489, MC1489A, SN75189, SN75189A
D, N, OR NS[†] PACKAGE
(TOP VIEW)



[†] The NS package is only available left-end taped and reeled. For SN75189, order SN75189NSR.

SN55189, SN55189A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



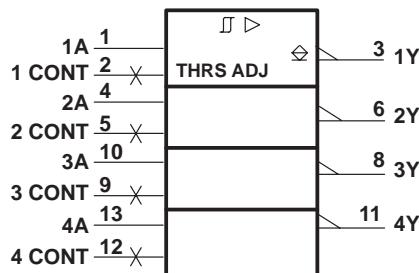
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

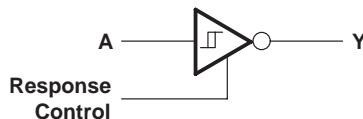
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logic symbol†

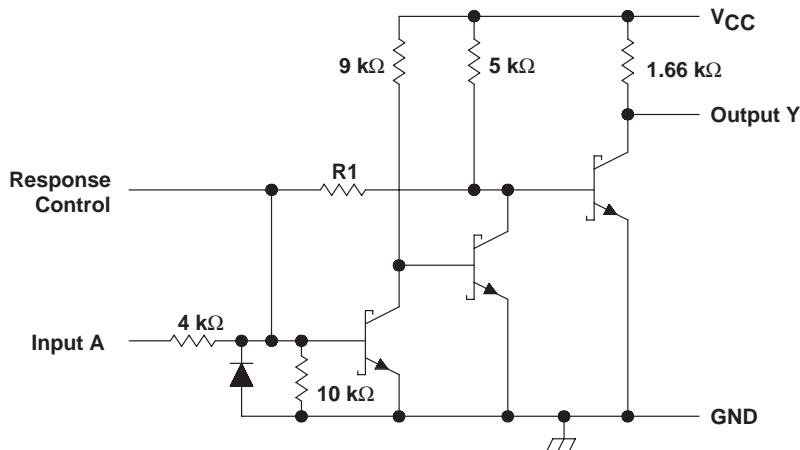


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, NS, and W packages.

logic diagram (positive logic)



schematic (each receiver)



| | MC1489 SN55189 SN75189 | MC1489A SN55189A SN75189A |
|----|------------------------------|---------------------------------|
| R1 | 8.4 kΩ | 1.84 kΩ |

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|---|------------------------------|
| Supply voltage, V_{CC} (see Note 1) | 10 V |
| Input voltage, V_I | ± 30 V |
| Output voltage, I_O | 20 mA |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A : SN55189, SN55189A | -55°C to 125°C |
| MC1489, MC1489A, SN75189, SN75189A | 0°C to 70°C |
| Storage temperature range, T_{STG} | -65°C to 150°C |
| Case temperature for 60 seconds, FK package | 260°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J or W package | 300°C |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D, N, or NS package | 260°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ C$ | $T_A = 70^\circ C$ POWER RATING | $T_A = 125^\circ C$ POWER RATING |
|---------|---------------------------------------|---|------------------------------------|-------------------------------------|
| D | 950 mW | 7.6 mW/°C | 608 mW | N/A |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J‡ | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | N/A |
| NS | 625 mW | 4.0 mW/°C | 445 mW | N/A |
| W | 1000 mW | 8.0 mW/°C | 640 mW | 200 mW |

‡ In the J package, SN55189 and SN55189A chips are either silver glass or alloy mounted.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---------------------------------------|-----|-----|------|------|
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | V |
| Input voltage, V_I | -25 | | 25 | V |
| High-level output current, I_{OH} | | | -0.5 | mA |
| Low-level output current, I_{OL} | | | 10 | mA |
| Operating free-air temperature, T_A | 0 | | 70 | °C |

MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

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electrical characteristics over operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 1\%$ (unless otherwise noted)

| PARAMETER | TEST FIGURE | TEST CONDITIONS [†] | SN55189 SN55189A | | | MC1489, MC1489A SN75189 SN75189A | | | UNIT | |
|--|-------------|---|--|------------------|-------|--|------------------|------|------|----|
| | | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | | |
| V _{IT+} Positive-going input threshold voltage | 1 | '89 | $T_A = 25^\circ\text{C}$ | 1 | 1.3 | 1.5 | 1 | 1.3 | 1.5 | V |
| | | | $T_A = 0^\circ\text{C}$ to 70°C | | | | 0.9 | | 1.6 | |
| | | | $T_A = -55^\circ\text{C}$ to 125°C | 0.6 | | 1.9 | | | | |
| | | '89A | $T_A = 25^\circ\text{C}$ | 1.75 | 1.9 | 2.25 | 1.75 | 1.9 | 2.25 | |
| | | | $T_A = 0^\circ\text{C}$ to 70°C | | | | 1.55 | | 2.25 | |
| | | | $T_A = -55^\circ\text{C}$ to 125°C | 1.30 | | 2.65 | | | | |
| V _{IT-} Negative-going input threshold voltage | 1 | '89, '89A | $T_A = 25^\circ\text{C}$ | 0.75 | 1.0 | 1.25 | 0.75 | 1.0 | 1.25 | V |
| | | | $T_A = 0^\circ\text{C}$ to 70°C | | | | 0.65 | | 1.25 | |
| | | | $T_A = -55^\circ\text{C}$ to 125°C | 0.35 | | 1.6 | | | | |
| V _{OH} High-level output voltage | 1 | $V_I = 0.75 \text{ V}$, $I_{OH} = -0.5 \text{ mA}$ | | | 2.6 | 4 | 5 | 2.6 | 4 | V |
| | | Input open, $I_{OH} = -0.5 \text{ mA}$ | | | 2.6 | 4 | 5 | 2.6 | 4 | |
| V _{OL} Low-level output voltage | 1 | $V_I = 3 \text{ V}$, $I_{OL} = 10 \text{ mA}$ | | | 0.2 | 0.45 | | 0.2 | 0.45 | V |
| I _{IH} High-level input current | 2 | $V_I = 25 \text{ V}$ | | | 3.6 | 8.3 | 3.6 | 8.3 | | mA |
| | | $V_I = 3 \text{ V}$ | | | 0.43 | | 0.43 | | | |
| I _{IL} Low-level input current | 2 | $V_I = -25 \text{ V}$ | | | -3.6 | -8.3 | -3.6 | -8.3 | | mA |
| | | $V_I = -3 \text{ V}$ | | | -0.43 | | -0.43 | | | |
| I _{OS} Short-circuit output current | 3 | | | | -3 | | | -3 | | mA |
| I _{CC} Supply current | 2 | $V_I = 5 \text{ V}$, Outputs open | | | 20 | 26 | | 20 | 26 | mA |

[†] All characteristics are measured with the response-control terminal open.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 15 \text{ pF}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST FIGURE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-------------|-----------------------------|-----|-----|-----|------|
| t _{PLH} Propagation delay time, low- to high-level output | 4 | $R_L = 3.9 \text{ k}\Omega$ | | 25 | 85 | ns |
| | | $R_L = 390 \Omega$ | | 25 | 50 | |
| | | $R_L = 3.9 \text{ k}\Omega$ | | 120 | 175 | ns |
| | | $R_L = 390 \Omega$ | | 10 | 20 | |
| t _{PHL} Propagation delay time, high- to low-level output | | | | | | |
| t _{TLH} Transition time, low- to high-level output | | | | | | |
| t _{THL} Transition time, high- to low-level output | | | | | | |

PARAMETER MEASUREMENT INFORMATION[†]

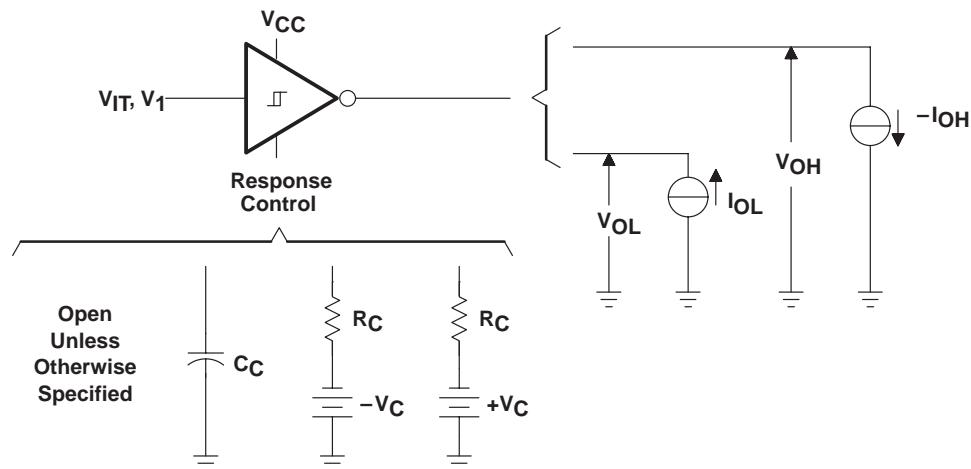
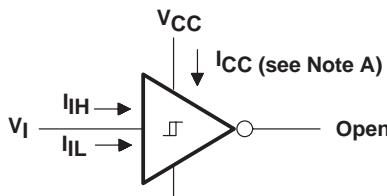


Figure 1. V_{IT+} , V_{IT-} , V_{OH} , V_{OL}



NOTE A: I_{CC} is tested for all four receivers simultaneously.

Figure 2. I_{IH} , I_{IL} , I_{CC}

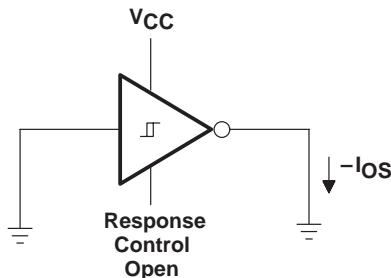


Figure 3. I_{OS}

[†] Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

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PARAMETER MEASUREMENT INFORMATION

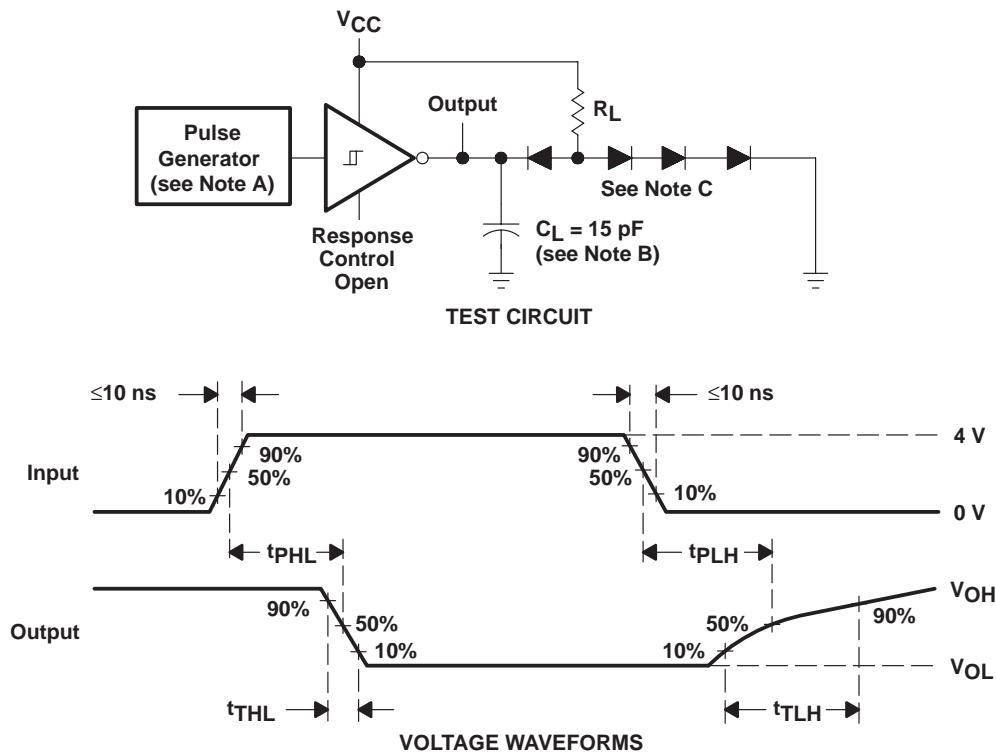


Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SN65189, SN75189
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

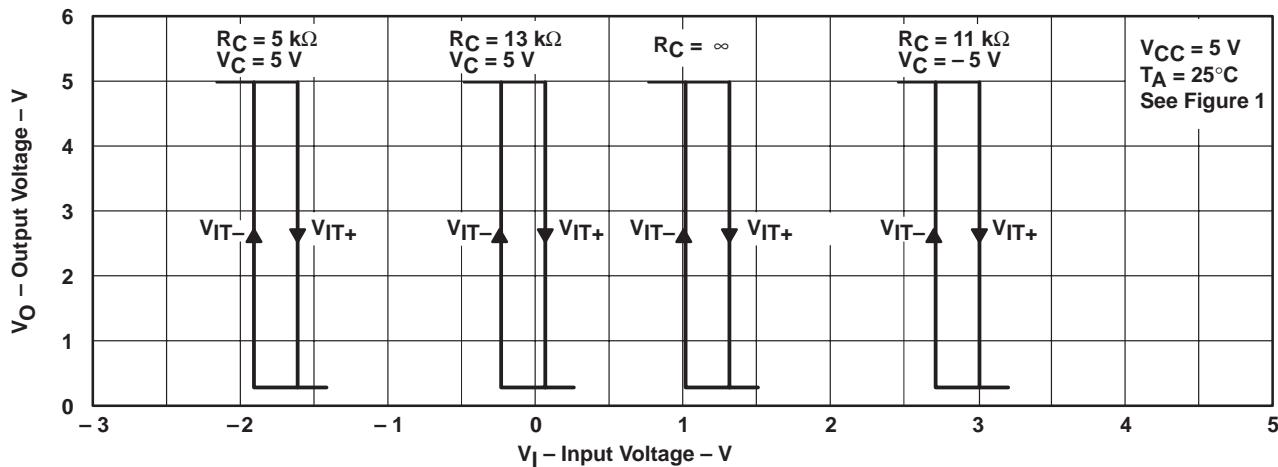


Figure 5

SN65189A, SN75189A
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

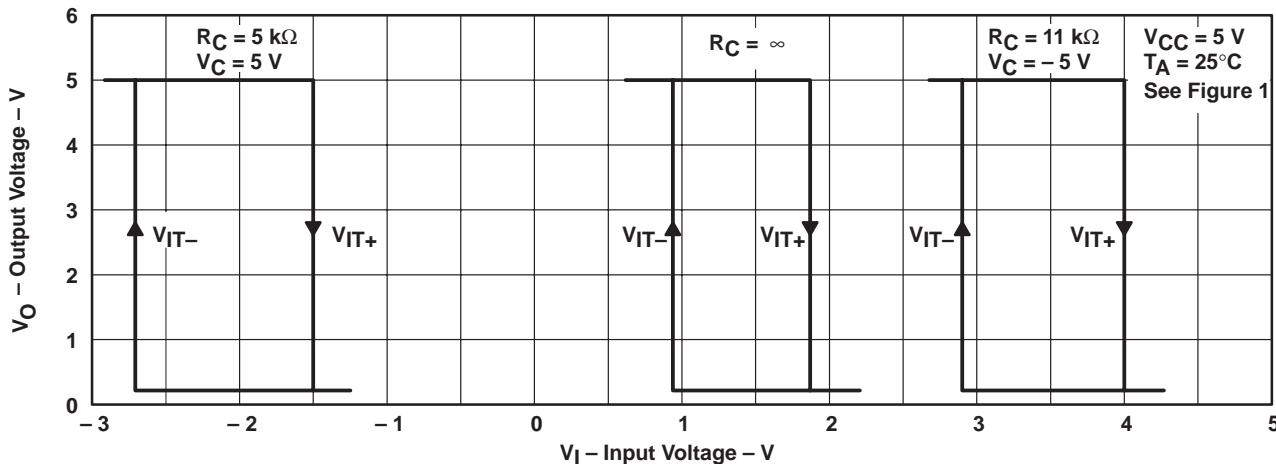
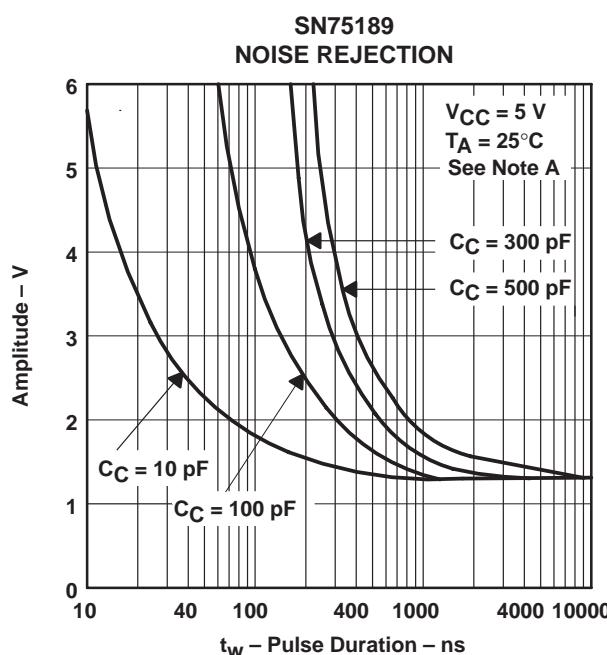
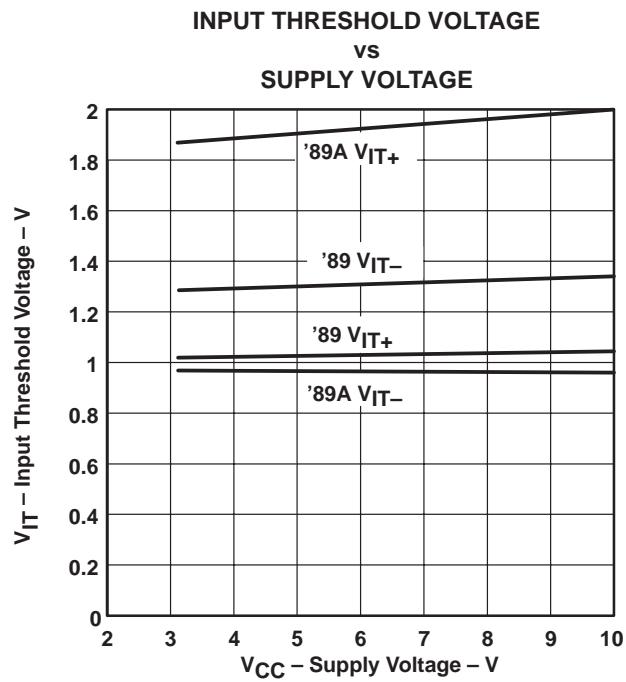
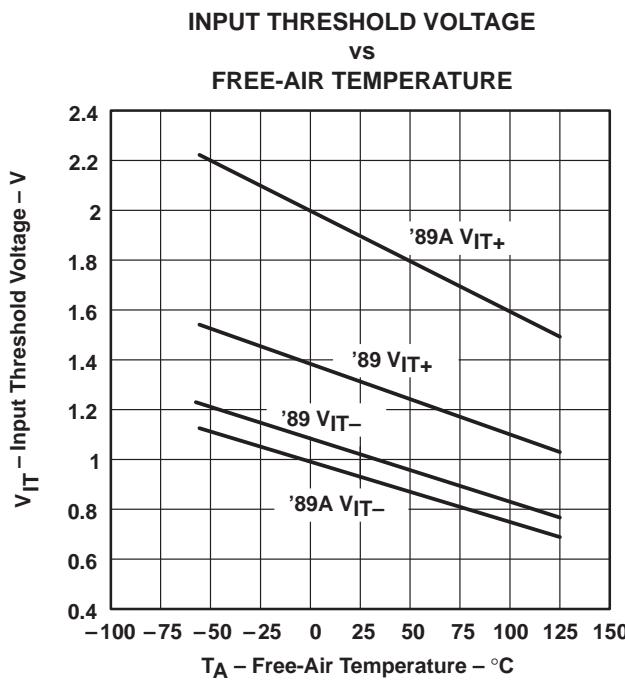


Figure 6

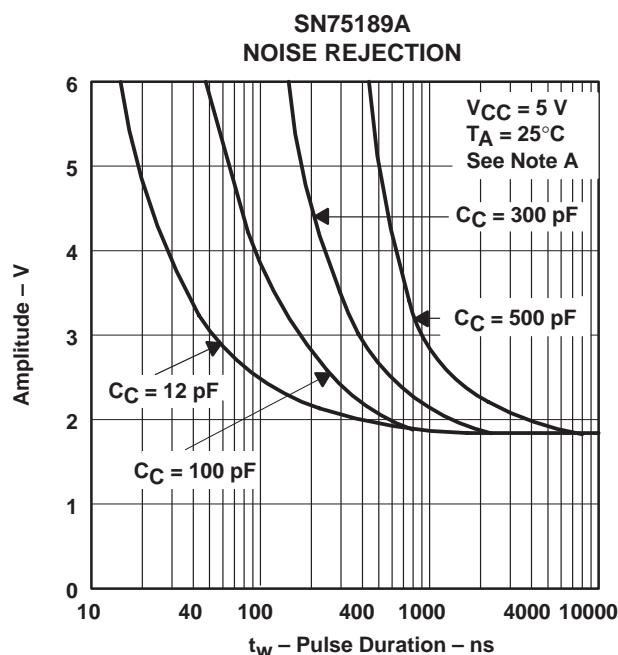
MC1489, MC1489A, SN55189, SN55189A, SN75189, SN75189A QUADRUPLE LINE RECEIVERS

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TYPICAL CHARACTERISTICS[†]



NOTE A: Maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.



NOTE A: Maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

[†] Data for free-air temperatures below 0°C and above 70°C are applicable to SN55189 and SN55189A circuits only.

TYPICAL CHARACTERISTICS

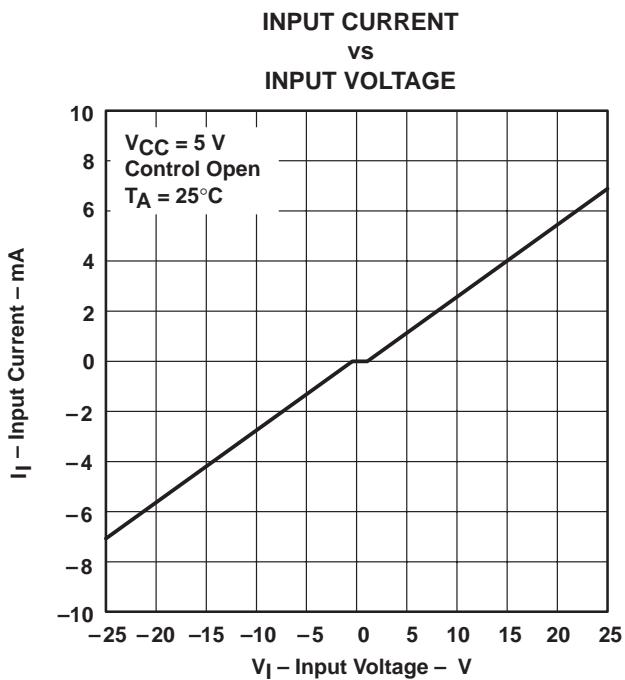


Figure 11

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| 5962-86888022A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-86888022A SNJ55189AFK |
| 5962-8688802CA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8688802CA SNJ55189AJ |
| 5962-8688802DA | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8688802DA SNJ55189AW |
| MC1489AN | Obsolete | Production | PDIP (N) 14 | - | - | Call TI | Call TI | 0 to 70 | MC1489AN |
| MC1489N | Obsolete | Production | PDIP (N) 14 | - | - | Call TI | Call TI | 0 to 70 | MC1489N |
| SN55189AJ | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN55189AJ |
| SN55189AJ.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN55189AJ |
| SN75189AD | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189A |
| SN75189AD.A | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189A |
| SN75189ADR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189A |
| SN75189ADR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189A |
| SN75189ADRG4 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189A |
| SN75189AN | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75189AN |
| SN75189AN.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75189AN |
| SN75189ANSR | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189A |
| SN75189ANSR.A | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189A |
| SN75189ANSRG4 | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189A |
| SN75189APWR | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | A189A |
| SN75189APWR.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | A189A |
| SN75189D | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189 |
| SN75189D.A | Active | Production | SOIC (D) 14 | 50 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189 |
| SN75189DR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189 |
| SN75189DR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189 |
| SN75189N | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75189N |
| SN75189N.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75189N |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------------------------|
| SN75189NSR | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189 |
| SN75189NSR.A | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75189 |
| SNJ55189AFK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 86888022A SNJ55 189AFK |
| SNJ55189AFK.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 86888022A SNJ55 189AFK |
| SNJ55189AJ | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8688802CA SNJ55189AJ |
| SNJ55189AJ.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8688802CA SNJ55189AJ |
| SNJ55189AW | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8688802DA SNJ55189AW |
| SNJ55189AW.A | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8688802DA SNJ55189AW |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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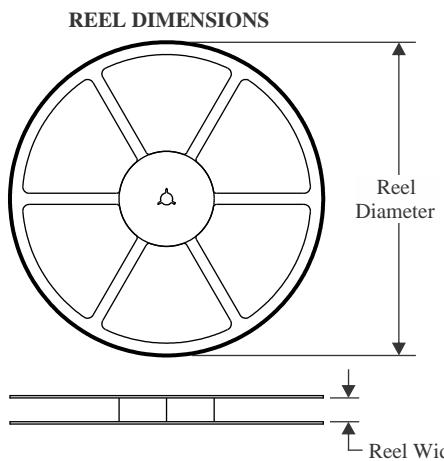
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55189A, SN75189A :

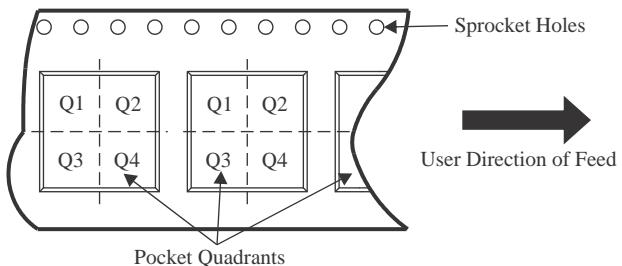
- Catalog : [SN75189A](#)
- Military : [SN55189A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

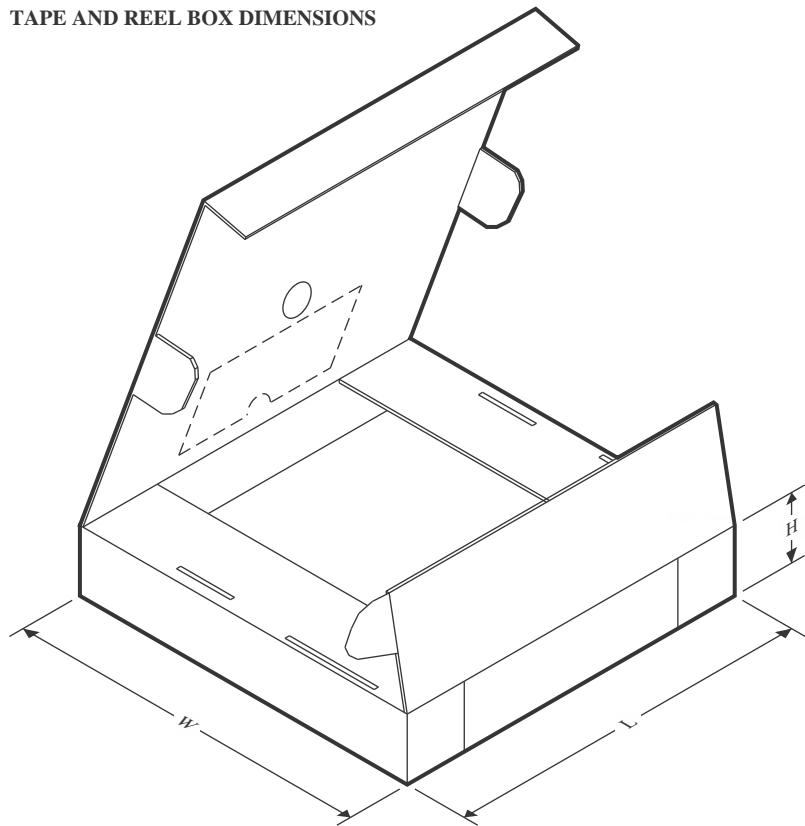
TAPE AND REEL INFORMATION


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


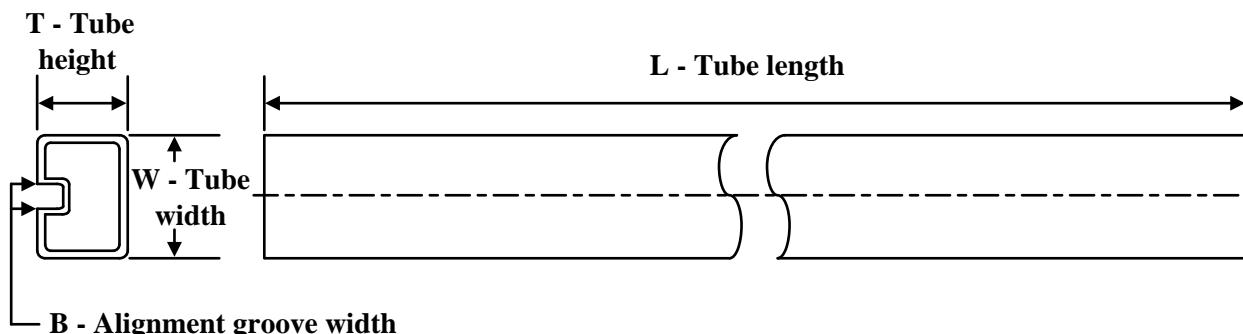
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75189ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN75189ANSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN75189APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN75189DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN75189NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75189ADR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN75189ANSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN75189APWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN75189DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN75189NSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

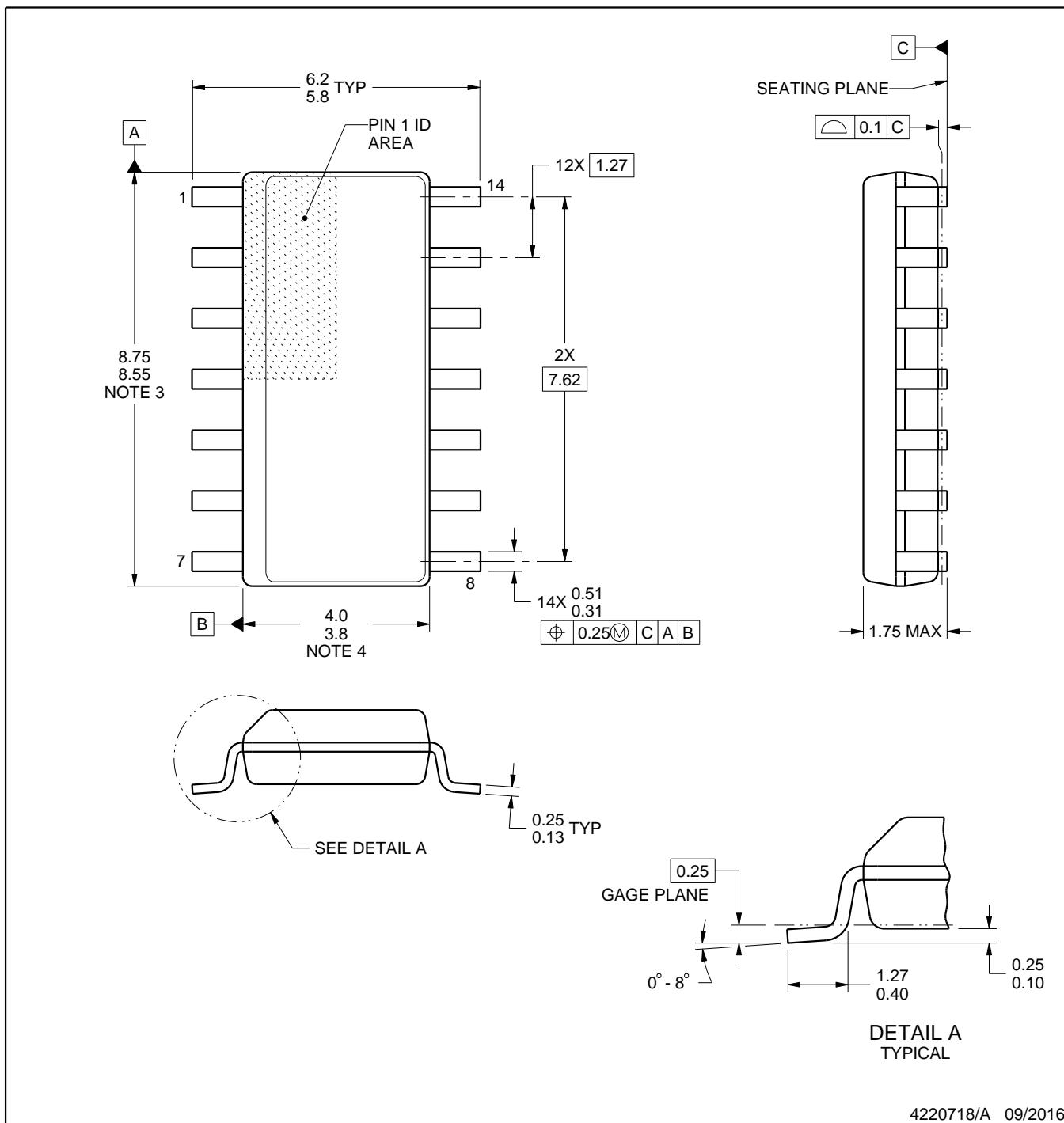
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-86888022A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8688802DA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN75189AD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN75189AD | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| SN75189AD.A | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN75189AD.A | D | SOIC | 14 | 50 | 507 | 8 | 3940 | 4.32 |
| SN75189AN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN75189AN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN75189AN.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN75189AN.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN75189D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN75189D.A | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN75189N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN75189N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ55189AFK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ55189AFK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ55189AW | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ55189AW.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

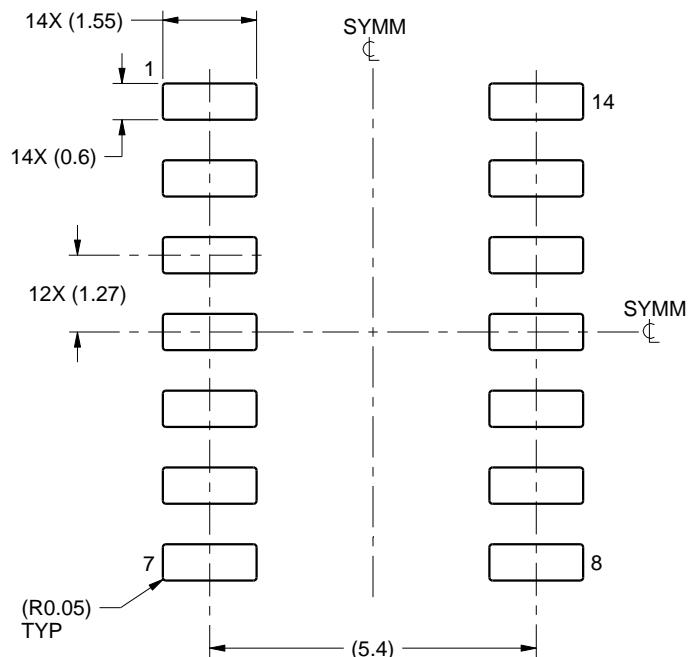
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

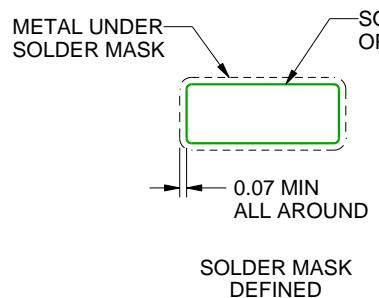
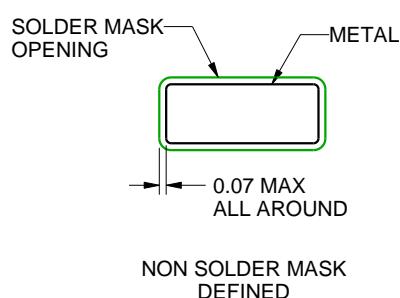
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

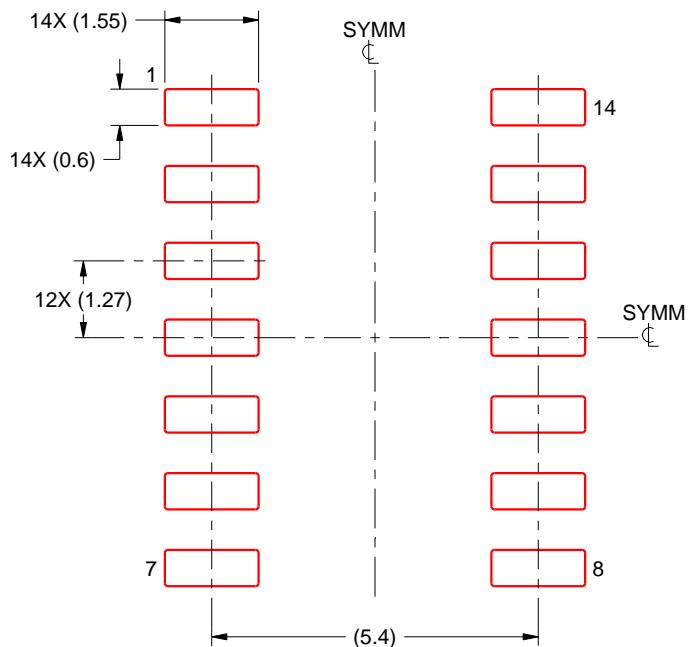
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



**SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X**

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

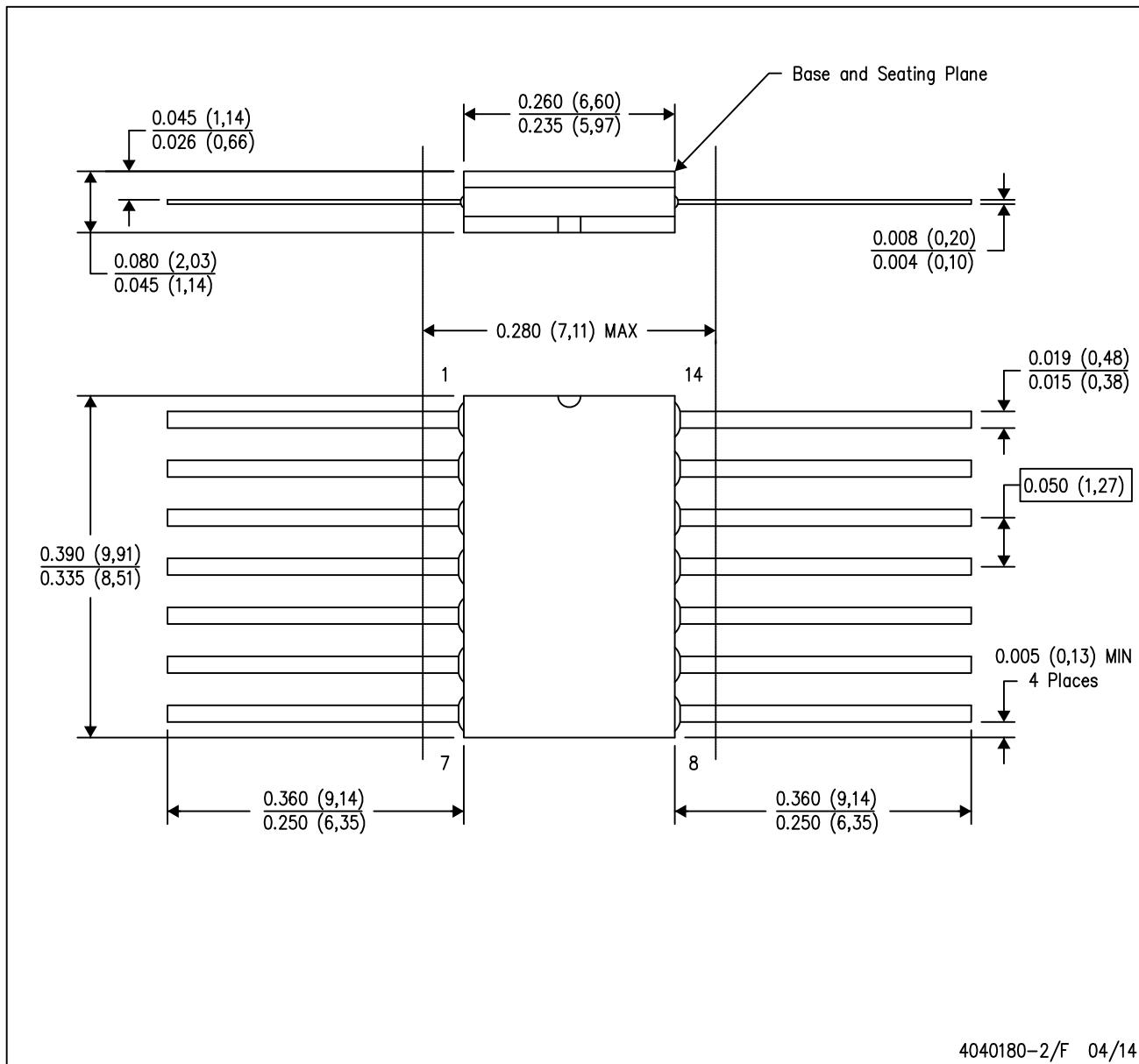


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

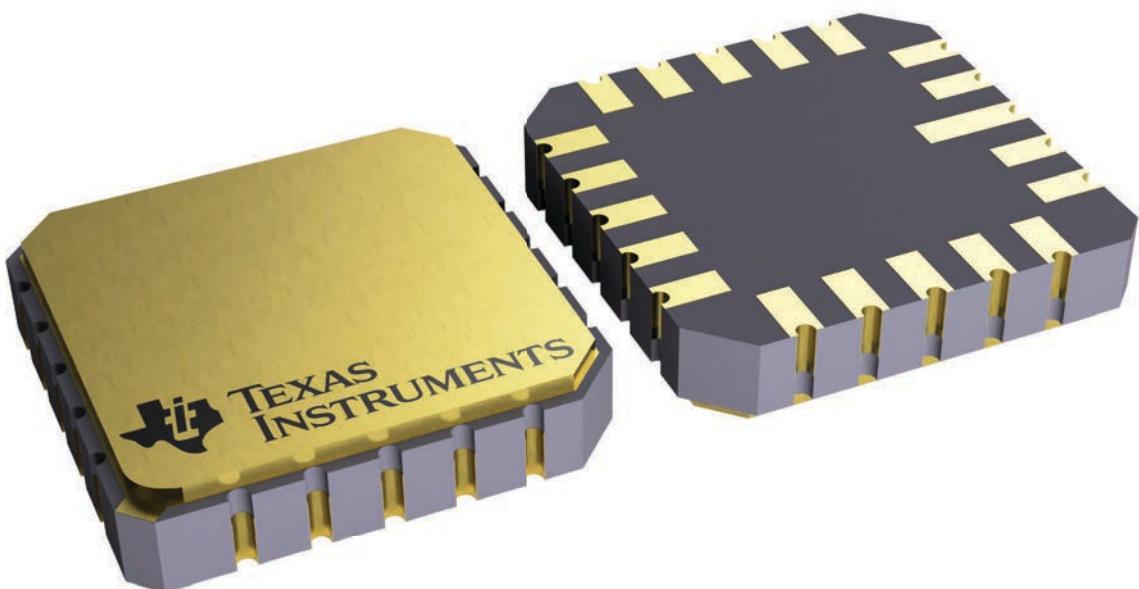
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



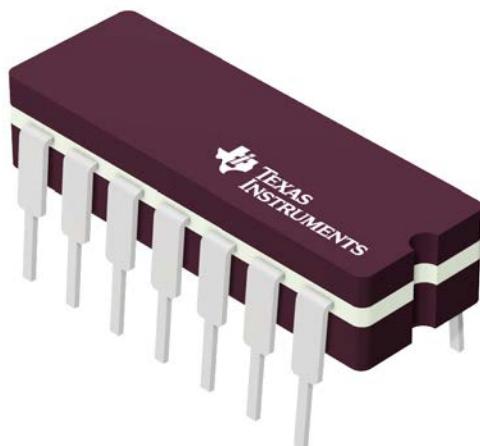
4229370VA\

GENERIC PACKAGE VIEW

J 14

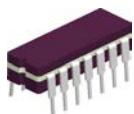
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

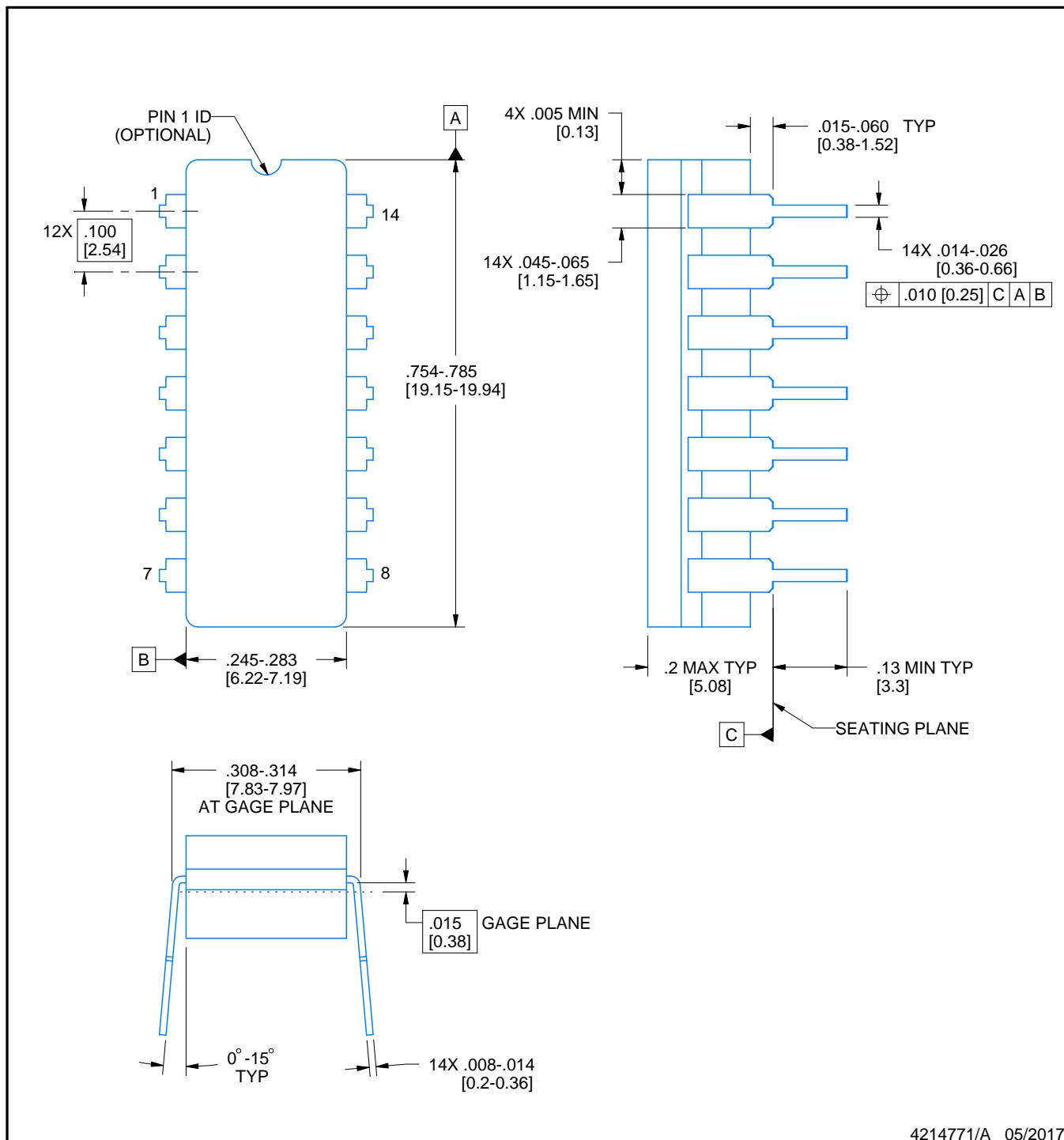


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

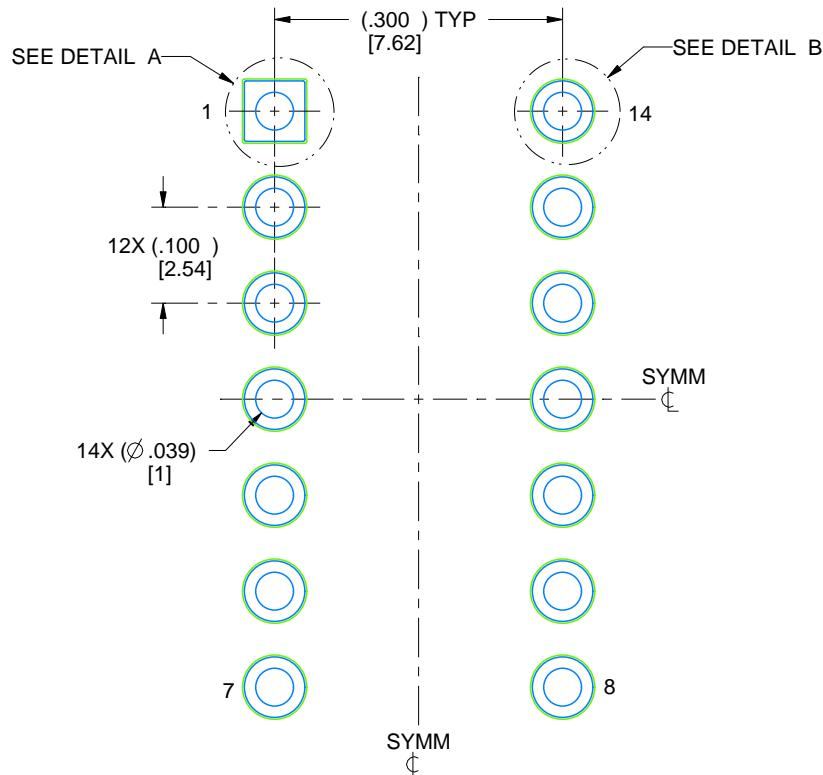
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

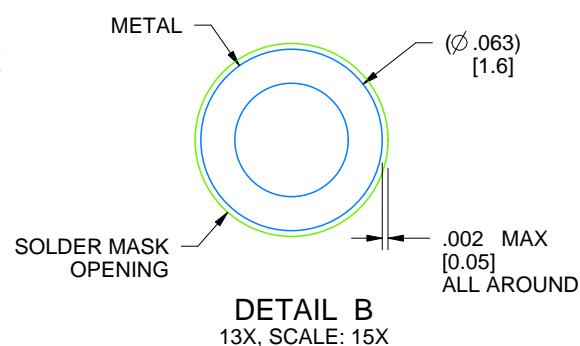
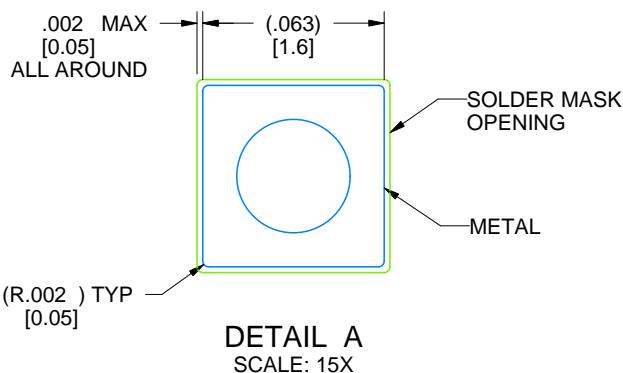
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

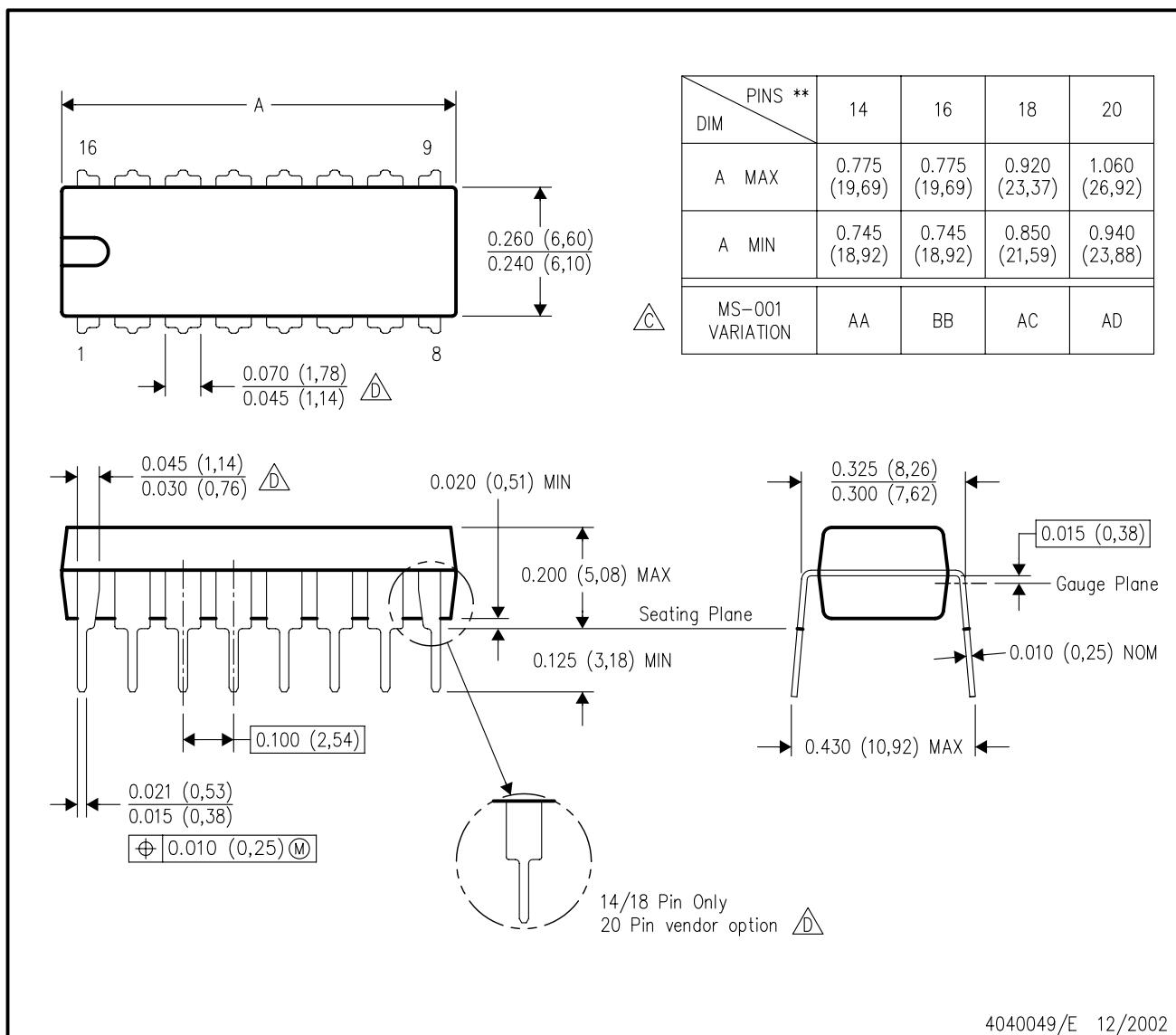


4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



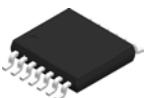
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

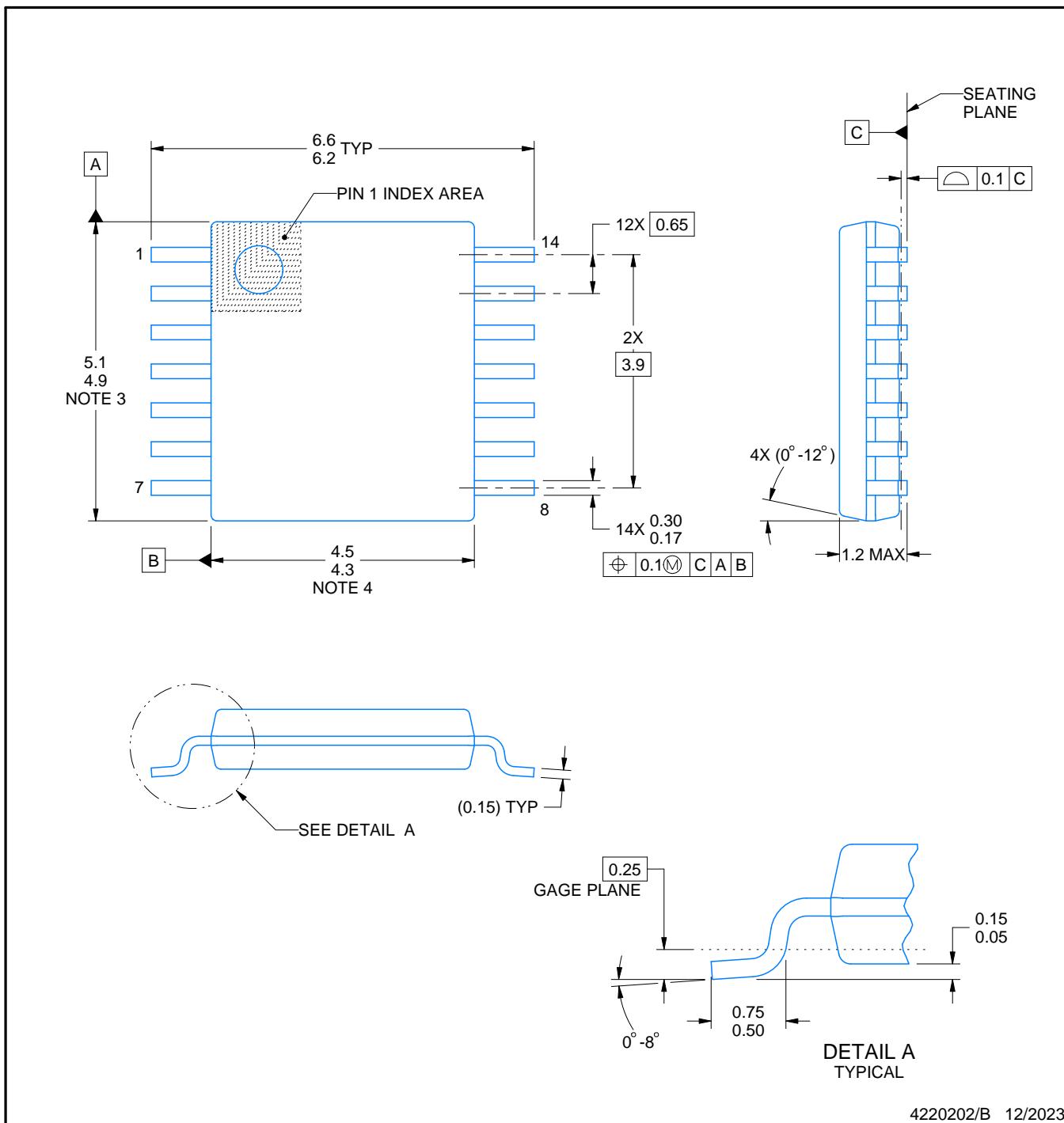
PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

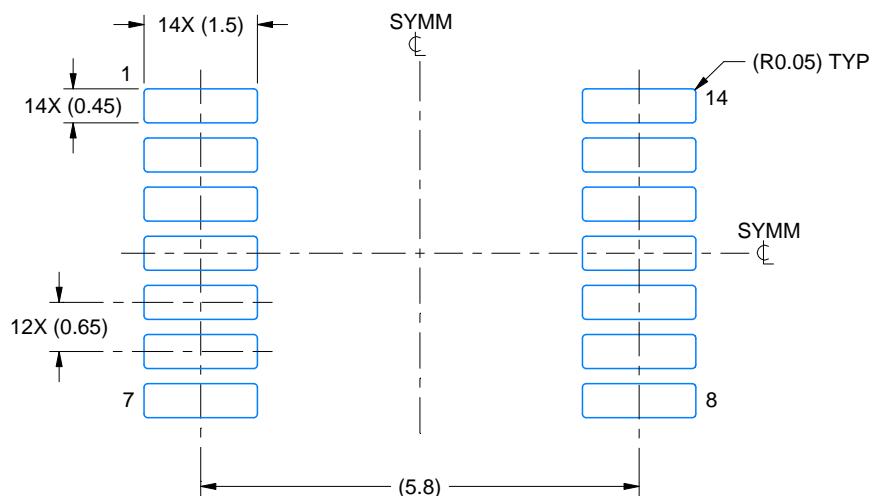
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

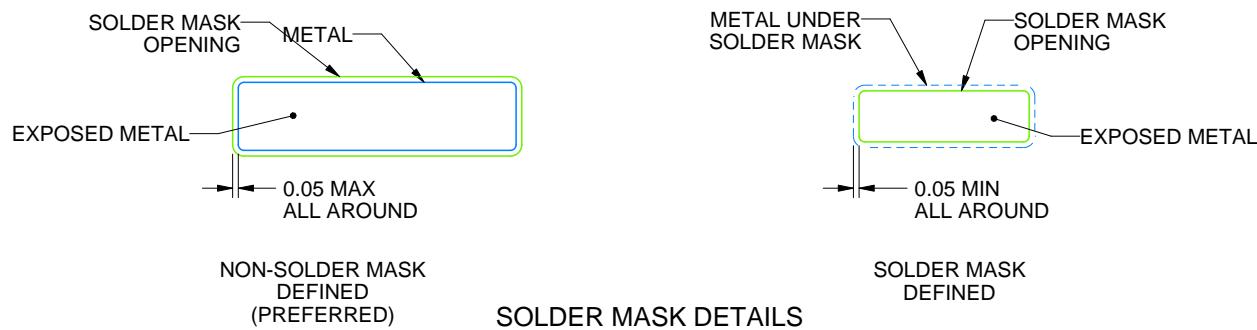
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

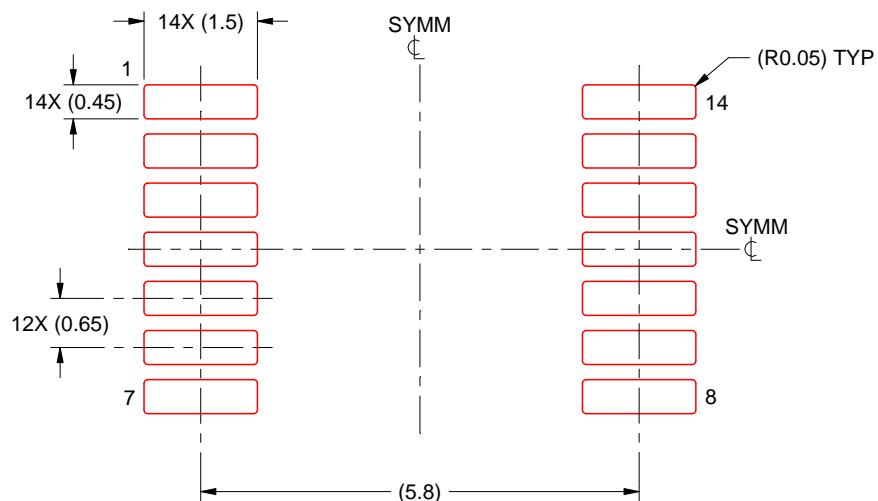
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X**

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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