Texas Instruments

SN75LVPE802 双通道 8Gbps SATA Express 均衡器和转接驱动器

1 特性

- SATA Express 支持
- 可选均衡和去加重功能
- 支持热插拔功能
- 接收器检测与带外 (OOB) 支持
- 集成输出静噪
- 多速率运行
  - SATA：1.5Gbps、3Gbps、6Gbps
  - PCIe：2.5Gbps、5Gbps、8Gbps
- 出色的抖动和损耗补偿功能，支持长达 24 英寸 (61cm) 以上的 FR4 走线
- 低功耗
  - < 220mW（典型值）
  - < 50mW（在自动低功耗模式下）
  - < 5mW（在待机模式下）
- 20 引脚 4mm x 4mm 四方扁平无引线 (QFN) 封装
- 较高水平的静电放电 (ESD) 瞬态保护
  - 人体模型 (HBM)：10,000V
  - 组件充电模式 (CDM)：1500V
  - 机器放电模式 (MM)：200V
- 扩展商业级温度范围为 0°C 至 85°C

2 应用

- 平板电脑
- 笔记本电脑
- 台式机
- 扩展坞

3 说明

SN75LVPE802 是一款通用型双通道 SATA Express 信号调节器，最高可支持 8Gbps 的数据速率。此器件支持 SATA Gen 1、2 和 3 规范以及 PCIe 1、2 和 3。SN75LVPE802 由 3.3V 单电源供电运行，并且配有带自偏置特性的 100Ω 线路端接电阻，适用于交流耦合。输入端包含一个带外 (OOB) 检测器，可在输入差分电压低于阈值时自动抑制输出端噪声，同时保持一个稳定的共模电压。此外，该器件还被设计成依据 SATA 标准处理扩频时钟 (SSC) 传输。

SN75LVPE802 通过可选均衡设置来处理其输入端的互连损耗，能够通过编程来匹配通道中的损耗。对于 3Gbps 及以下的数据速率，SN75LVPE802 可为最大规格达 50 英寸的 FR4 电路板材料提供信号均衡。对于 8Gbps 的数据速率，该器件可为最大规格达 40 英寸的 FR4 材料提供补偿。均衡级别通过设置信号控制引脚 EQ 来控制。

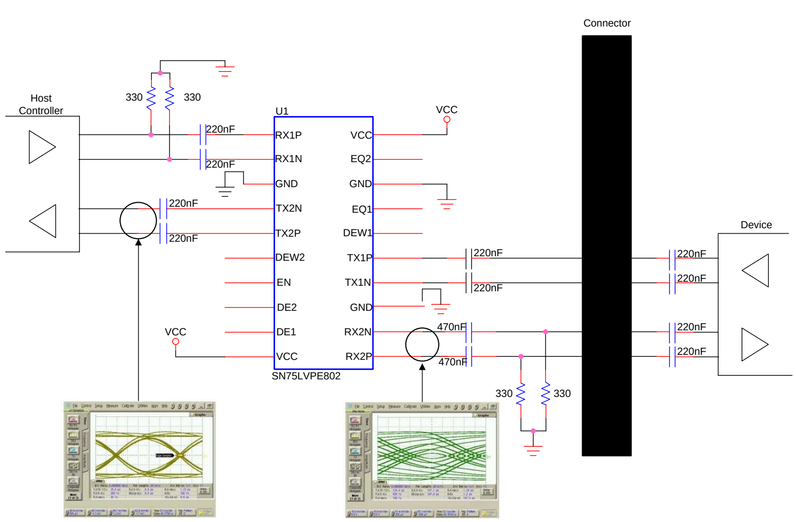
发送侧有两个去加重级别可供选择，用于为输出端提供 0 或 1.2dB 的附加高频损耗补偿。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN75LVPE802	超薄四方扁平无引线 (WQFN) (20)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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4 修订历史记录

Changes from Revision A (September 2016) to Revision B **Page**

- Changed 图 27 note From: Input Trace Length = 53 in. To: Input Trace Length = 3 in. ... 22
- Changed title of 图 35 From: Output Eye (TP2) to: Input Eye (TP2) ... 23
- Changed 图 37 note From: Input Trace Length = 36 in. To: Input Trace Length = 48 in. ... 23
- Changed 图 38 note From: Input Trace Length = 36 in. To: Input Trace Length = 48 in. ... 23
- Changed title of 图 38 From: Input Eye (TP4) To: Output Eye (TP4) ... 23
- Changed note in 图 40 From: Output Trace Length = 0 in To: Output Trace Length = 3 in. ... 24
- Changed note in 图 42 From: Output Trace Length = 6 in To: Output Trace Length = 12 in. ... 24

Changes from Original (January 2016) to Revision A **Page**

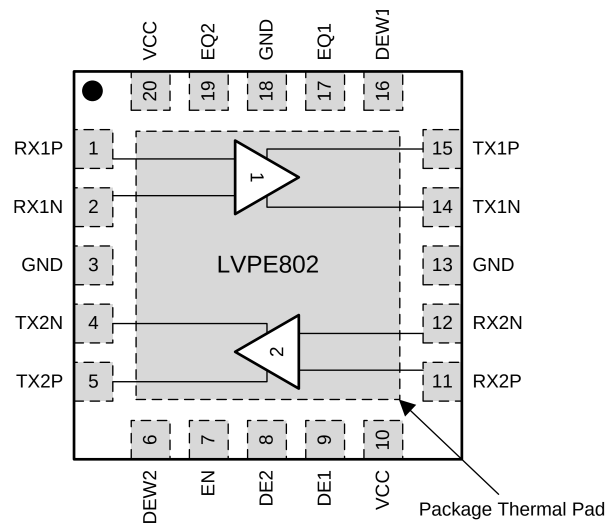
- 已将器件状态从“产品预览”更改为“量产数据” ... 1

5 说明 （续）

该器件支持热插拔功能（要求在差分输入和输出使用交流耦合电容），能够防止器件在热插入（例如，异步信号插/拔、不带电插/拔、带电插/拔或意外插/拔）情况下遭到损坏。

6 Pin Configuration and Functions

**RTJ Package
20 Pin (WQFN)
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Control Pins			
DE1 (1)	9	I, LVCMOS	Selects de-emphasis settings for CH 1 and CH 2 per 表 1. Internally tied to V_{CC} / 2.
DE2 (1)	8	I, LVCMOS	
DEW1	16	I, LVCMOS	De-emphasis width control for CH 1 and CH 2. 0 = De-emphasis pulse duration, short 1 = De-emphasis pulse duration, long (default)
DEW2	6	I, LVCMOS	
EN	7	I, LVCMOS	Device enable and disable pin, internally pulled to V_{CC}. 0 = Device in standby mode 1 = Device enabled (default)
EQ1 (1)	17	I, LVCMOS	Select equalization settings for CH 1 and CH 2 per 表 1. Internally tied to V_{CC} / 2.
EQ2 (1)	19	I, LVCMOS	
High Speed Differential I/O			
RX1N	2	I, CML	Non-inverting and inverting CML differential input for CH 1 and CH 2. These pins connect to an internal voltage bias via a dual termination resistor circuit.
RX1P	1	I, CML	
RX2N	12	I, CML	
RX2P	11	I, CML	
TX1N	14	O, VML	Non-inverting and inverting VML differential input for CH 1 and CH 2. These pins connect to an internal voltage bias via a dual termination resistor circuit.
TX1P	15	O, VML	
TX2N	4	O, VML	
TX2P	5	O, VML	
POWER			
GND	3, 13, 18	Power	Supply ground
VCC	10, 20	Power	Positive supply must be 3.3V ± 10%

(1) Internally biased to V_{CC} / 2 with >200-Ωk pullup or pulldown. When 3-state pins are left as NC, board leakage at the pin pad must be < 1 µA; otherwise, drive to V_{CC} / 2 to assert mid-level state.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range(2), V_{CC}		–0.5	4	V
Voltage Range	Differential I/O	–0.5	4	V
	Control I/O	–0.5	VCC + 0.5	V
Continuous power dissipation		See Thermal Information		
Storage temperature, T_{stg}			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±10000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Machine model(3)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Tested in accordance with JEDEC Standard 22, Test Method A115-A

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	3	3.3	3.6	V
$C_{(coupling)}$	Coupling Capacitor		12		nF
T_A	Operating free-air temperature	0		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		SN75LVPE802 RTJ (WQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	0.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Power dissipation in active mode	DEWX = EN = VCC, EQX = DEX = NC, K28.5 pattern at 6 Gbps, V_{ID} = 700 mVpp		188	205	mW
P_{SD}	Power dissipation in standby mode	EN = 0 V, DEWX = EQX = DEX = NC, K28.5 pattern at 6 Gbps, V_{ID} = 700 mVpp			4	mW
I_{CC}	Active mode supply current	EN = 3.3 V, DEWX = EQX = DEX = NC, K28.5 pattern at 6 Gbps, V_{ID} = 700 mVpp		57	62	mA
$I_{CC(STDBY)}$	Standby mode supply current	EN = 0 V			1	mA
	Maximum data rate				8	Gbps
OOB						
$V_{(OOB)}$	Input OOB threshold	F = 750 MHz	50	78	150	mVpp
$DV_{diff(OOB)}$	OOB differential delta				25	mV
$DV_{CM(OOB)}$	OOB common-mode delta				50	mV
CONTROL LOGIC						
V_{IH}	High-level input voltage	For all control pins	1.4			V
V_{IL}	Low-level input voltage				0.5	V
$V_{IN(HYS)}$	Input hysteresis			115		mV
I_{IH}	High-level input current	EQx, DEx = VCC			30	µA
		EN, DEWx = VCC			1	µA
I_{IL}	Low-level input current	EQx, DEx = GND	–30			µA
		EN, DEWx = GND	–10			µA
RECEIVER AC/DC						
$Z_{(DIFFRX)}$	Differential-Input Impedance		85	100	115	Ω
$Z_{(SERX)}$	Single-Ended Input Impedance		40			Ω
$V_{CM(RX)}$	Common-mode voltage			1.8		V
$R_{L(DiffRX)}$	Differential mode return Loss (R_L)	f = 150 MHz – 300 MHz	22	28		dB
		f = 300 MHz – 600 MHz	14	17		dB
		f = 600 MHz – 1.2 GHz	10	12		dB
		f = 1.2 GHz – 2.4 GHz	8	9		dB
		f = 2.4 GHz – 3 GHz	7	9		dB
		f = 3 GHz – 5 GHz	6	8		dB
$R_{X(DiffRLSlope)}$	Differential mode R_L slope	f = 300 MHz – 6 GHz		14		dB/dec
$R_{L(CMRX)}$	Common mode return loss	f = 150 MHz – 300 MHz	9	10		dB
		f = 300 MHz – 600 MHz	14	17		dB
		f = 600 MHz – 1.2 GHz	15	23		dB
		f = 1.2 GHz – 2.4 GHz	13	16		dB
		f = 2.4 GHz – 3 GHz	10	12		dB
		f = 3 GHz – 5 GHz	4	6		dB
$V_{(diffRX)}$	Differential input voltage PP	f = 1.5 GHz and 3 GHz	120		1600	mVppd
$I_{B(RX)}$	Impedance Balance	f = 150 MHz – 300 MHz	30	41		dB
		f = 300 MHz – 600 MHz	30	38		dB
		f = 600 MHz – 1.2 GHz	20	32		dB
		f = 1.2 GHz – 2.4 GHz	10	26		dB
		f = 2.4 GHz – 3 GHz	10	25		dB
		f = 3 GHz – 5 GHz	4	20		dB
		f = 5 GHz – 6.5 GHz	4	17		dB
TRANSMITTER AC/DC						
$Z_{(diffTX)}$	Pair differential impedance		85	100	122	Ω
$Z_{(SETX)}$	Single-Ended input Impedance		40			Ω
$V_{(TXtrans)}$	Sequencing transient voltage	Transient voltages on the serial data bus during power sequencing (lab load)	–1.2		1.2	V

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{L(DiffTX)}$	Diff Mode return Loss	f = 150 MHz – 300 MHz	19	25		dB
		f = 300 MHz – 600 MHz	17	19		dB
		f = 600 MHz – 1.2 GHz	11	14		dB
		f = 1.2 GHz – 2.4 GHz	8	10		dB
		f = 2.4 GHz – 3 GHz	8	10		dB
		f = 3 GHz – 5 GHz	8	10		dB
$T_{X(DiffRLSlope)}$	Differential-mode R_L slope	f = 300 MHz to 3 GHz		14		dB/dec
$R_{L(CMTX)}$	Common Mode return Loss	f = 150 MHz – 300 MHz	16	20		dB
		f = 300 MHz – 600 MHz	15	19		dB
		f = 600 MHz – 1.2 GHz	14	17		dB
		f = 1.2 GHz – 2.4 GHz	10	12		dB
		f = 2.4 GHz – 3 GHz	9	11		dB
		f = 3 GHz – 5 GHz	6	7		dB
$I_{(BTX)}$	Impedance Balance	f = 150 MHz – 300 MHz	30	41		dB
		f = 300 MHz – 600 MHz	30	38		dB
		f = 600 MHz – 1.2 GHz	20	33		dB
		f = 1.2 GHz – 2.4 GHz	10	24		dB
		f = 2.4 MHz – 3 GHz	10	26		dB
		f = 3 GHz – 5 GHz	4	22		dB
		f = 5 GHz – 6.5 GHz	4	21		dB
DE	Output de-emphasis (relative to transition bit)	DE1 0r DE2 = 0		0		dB
		DE1 0r DE2 = 1		–2		dB
		DE1 0r DE2 = NC		–4		dB
$Diff_{(VppTX\_DE)}$	Differential output-voltage swing dc level	DE1 0r DE2 = 0		550		mV
		DE1 0r DE2 = 1		830		mV
		DE1 0r DE2 = NC		630		mV
$V_{(CMAC\_TX)}$	TX AC CM Voltage	At 1.5 GHz		20	50	mVppd
		At 3 GHz		12	26	dBmV (rms)
		At 6 GHz		13	30	dBmV (rms)
$V_{(CMTX)}$	Common-Mode Voltage			1.8		V
$T_{X(R/FImb)}$	TX rise-fall imbalance	At 3 GHz		6%	20%	V
$T_{X(AmpImb)}$	TX amplitude imbalance			2%	10%	V

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
DEVICE PARAMETERS						
	Auto low-power entry time	Electrical idle at input (see 图 24)	80	105	130	ps
	Auto low-power exit time	After first signal activity (see 图 24)		42	50	ps
TRANSMITTER AC/DC						
t_{DE}	Input OOB threshold	DEW1 or DEW2 = 0		94		ps
		DEW1 or DEW2 = 1		215		ps
OUT-OF-BAND (OOB)						
t_{OOB1}	OOB mode enter	See 图 23		3	5	ns
t_{OOB2}	OOB mode exit			3	5	ns

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
t_{PDelay}	Propagation delay	Measured using K28.5 pattern (see 图 1)		323	400	ps
t_{ENB}	Device enable time	EN 0 → 1			5	µs
t_{DIS}	Device disable time	EN 1 → 0			2	µs
RECEIVER AC/DC						
$t_{20\text{-}80RX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal. SATA 6-Gbps speed measured 1 in, (2.5 cm) from device pin.	62		75	ps
t_{SKEWRX}	Differential skew	Difference between the single-ended midpoint of the RX+ signal rising or falling edge, and the single-ended midpoint of the RX– signal falling or rising edge.			30	ps
TRANSMITTER AC/DC						
$t_{20\text{-}80TX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal. At 6 Gbps under no load conditions.	42	55	75	ps
t_{SKEWTX}	Differential skew	Difference between the single-ended midpoint of the TX+ signal rising or falling edge, and the single-ended midpoint of the TX– signal falling or rising edge.		6	20	ps
TRANSMITTER JITTER						
DJ_{TX}	Deterministic jitter (1) at CP in	V_{ID} = 500 mVpp, UI = 333 ps, K28.5 control character		0.06	5	UIp-p
RJ_{TX}	Residual Random jitter(1)	V_{ID} = 500 mVpp, UI = 333 ps, K28.7 control character		0.01	5	ps-rms
DJT_X	Deterministic jitter (1) at CP in	V_{ID} = 500 mVpp, UI = 167 ps, K28.5 control character		0.08	0.16	UIp-p
RJ_{TX}	Residual random jitter (1)	V_{ID} = 500 mVpp, UI = 167 ps, K28.7 control character		0.09	2	ps-rms
DJ_{TX}	Deterministic jitter (1) at CP in	V_{ID} = 500 mVpp, UI = 125 ps, K28.5 control character		0.1	0.2	UIp-p
RJ_{TX}	Residual random jitter(1)	V_{ID} = 500 mVpp, UI = 125 ps, K28.7 control character		0.3	1.5	ps-rms

(1) (1) T_J = (14.1 x RJSD + DJ), where RJSD is one standard deviation value

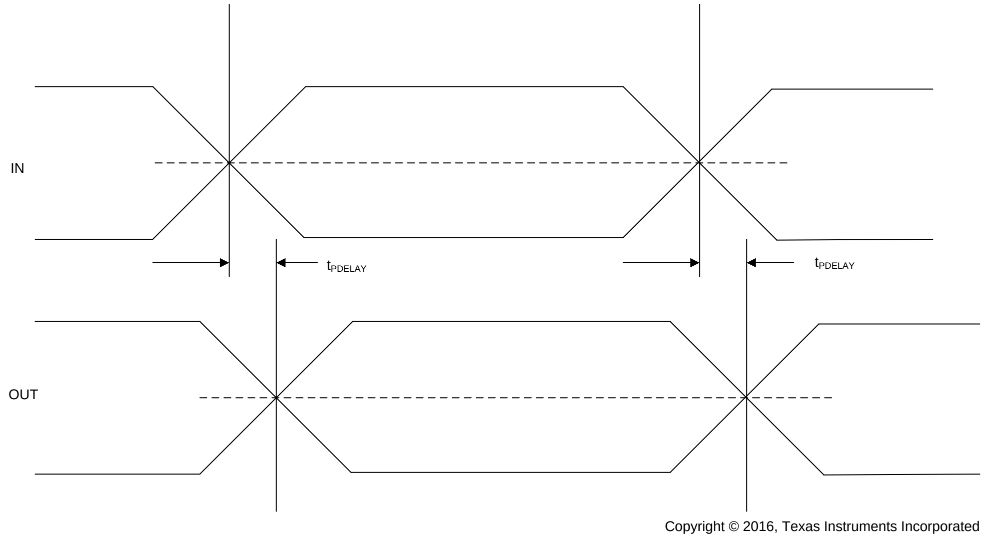


图 1. Propagation Delay Timing Diagram

7.8 Typical Characteristics

Input signal characteristics:

- Data rate = 8 Gbps 6 bps, 3 Gbps, 1.5 Gbps
- Amplitude = 500 mVpp
- o Data pattern = K28.5

SN75LVPE802 device setup:

- Temperature = 25°C
- Voltage = 3.3 V
- De-emphasis duration = 117 ps (short)
- Equalization and de-emphasis set to optimize performance at 6 Gbps

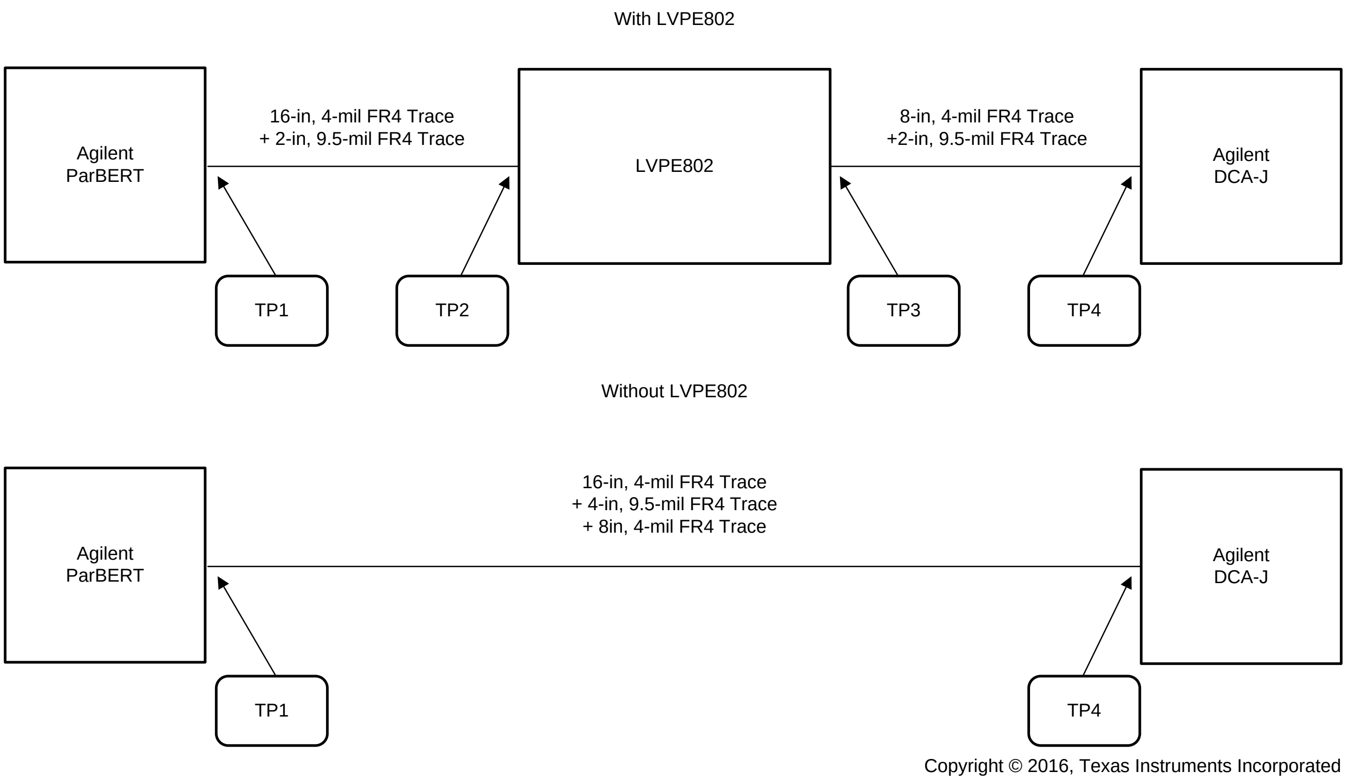


图 2. Performance Curve Measurement Setup

Typical Characteristics (接下页)

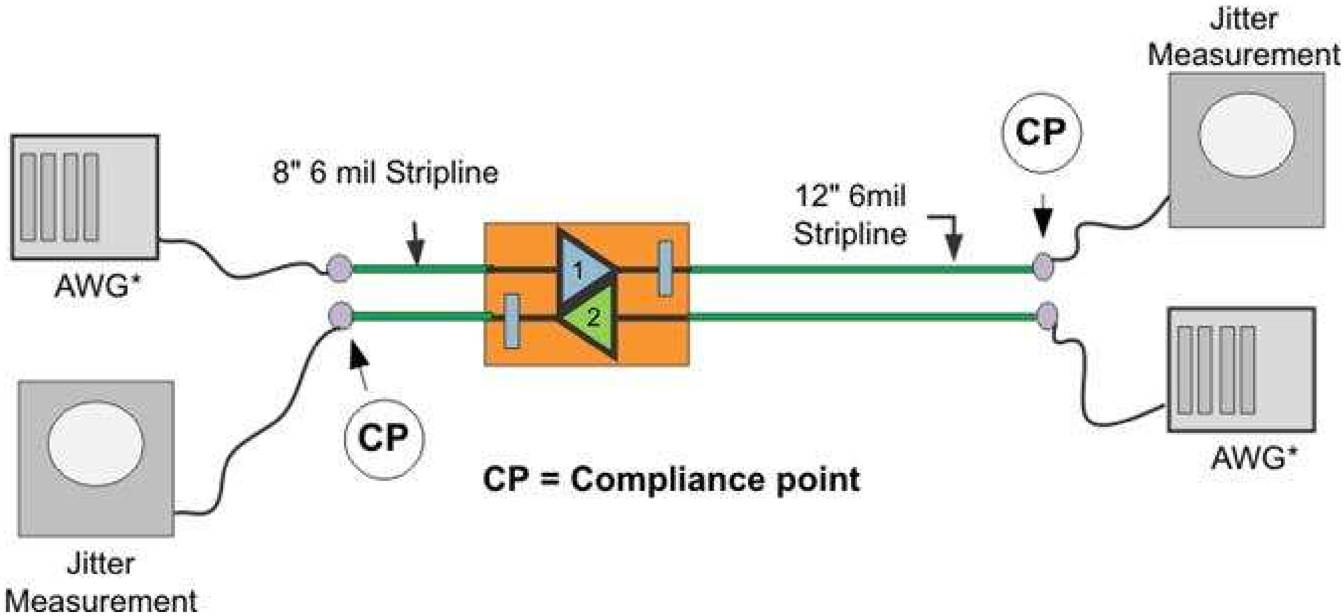
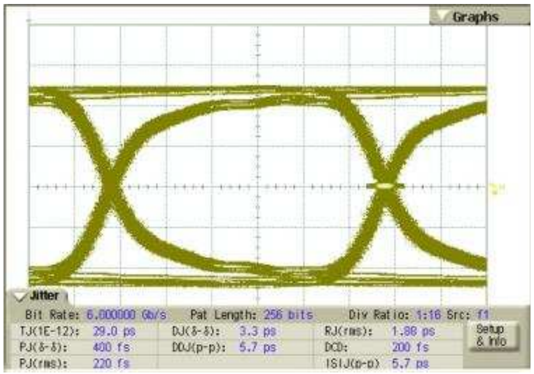


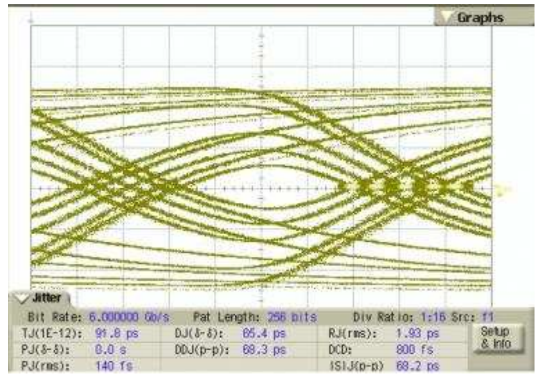
图 3. Jitter Measurement Test Condition

7.8.1 Jitter and VOD results: Case 1 at 6 Gbps



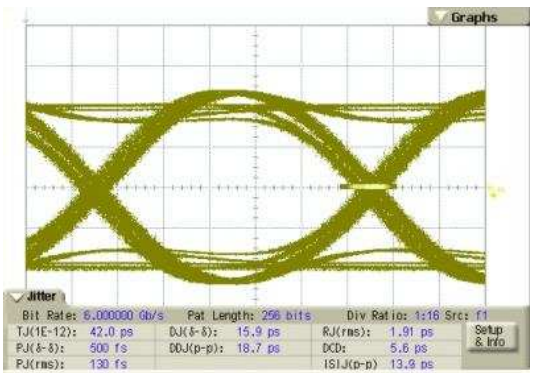
TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
29	3.3	1.88	412.4	159.2	350.52

图 4. Test Point 1



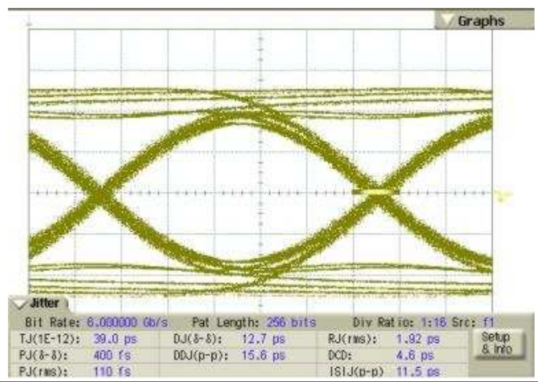
TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
91.8	65.4	1.93	240	28.9	81.24

图 5. Test Point 2



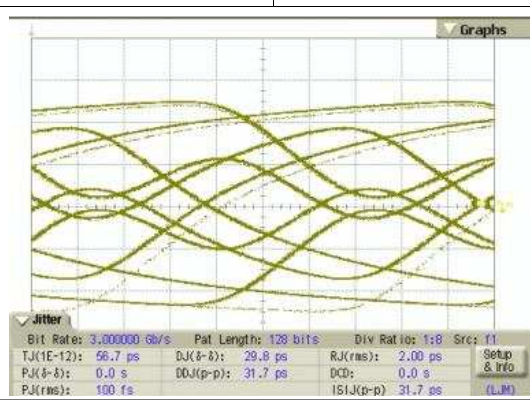
TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
42	15.9	1.91	788.8	141.3	623.02

图 6. Test Point 3



TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
39	12.7	1.92	557.1	149.7	459.62

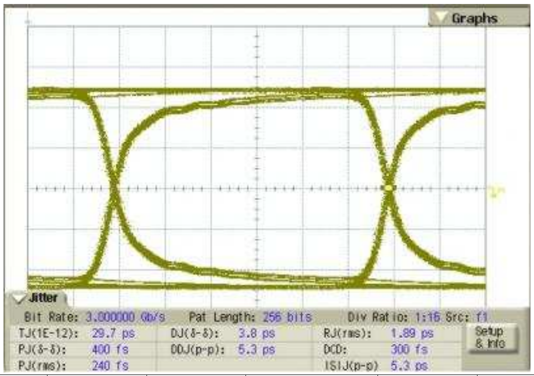
图 7. Test Point 4 With LVPE802



TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
56.7	29.8	2	165.4	101	13.24

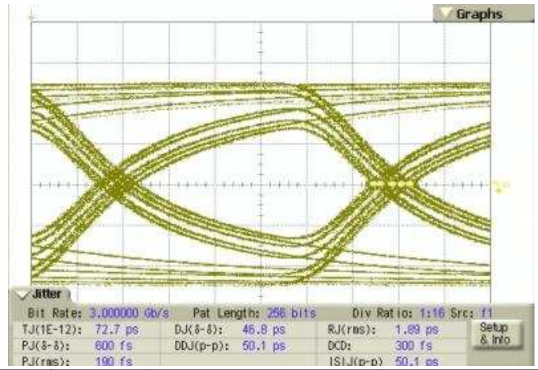
图 8. Test Point 4 Without LVPE802

7.8.2 Jitter and VOD Results: Case 2 at 3 Gbps



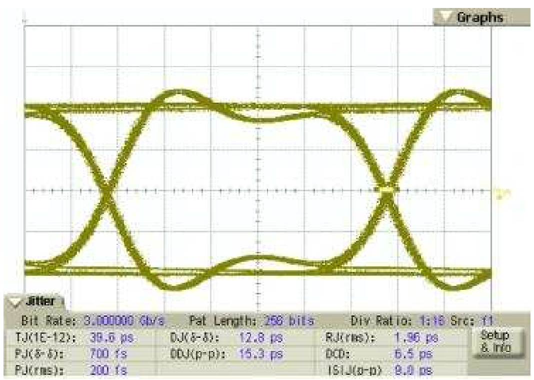
TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
29.7	3.8	1.89	430.9	326	392.84

图 9. Test Point 1



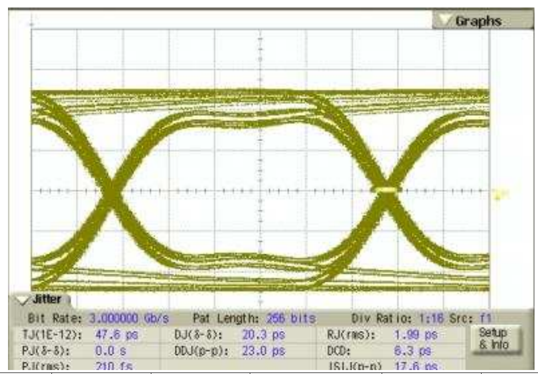
TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
72.7	46.8	1.89	314.9	237	222.36

图 10. Test Point 2



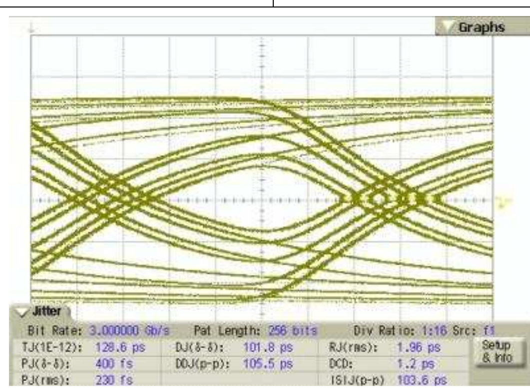
TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
39.6	12.8	1.96	714.5	321	611.62

图 11. Test Point 3



TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
47.9	20.3	1.99	615.3	305.0	463.42

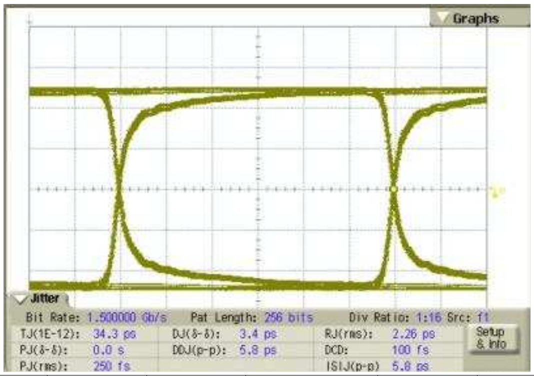
图 12. Test Point 4 With LVPE802



TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV
128.6	101.8	1.96	258.8	118	122.26

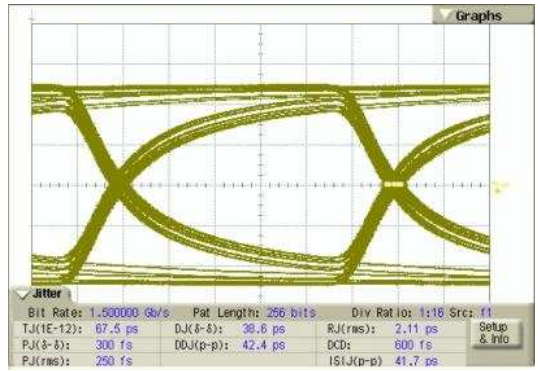
图 13. Test Point 4 Without LVPE802

7.8.3 Jitter and VOD Results: Case 3 at 1.5 Gbps



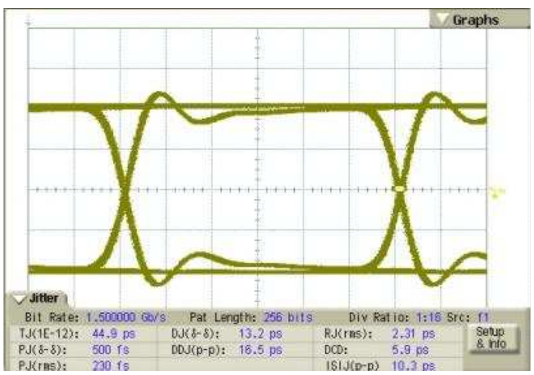
TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
34.3	3.4	2.26	448	659	417.28

图 14. Test Point 1



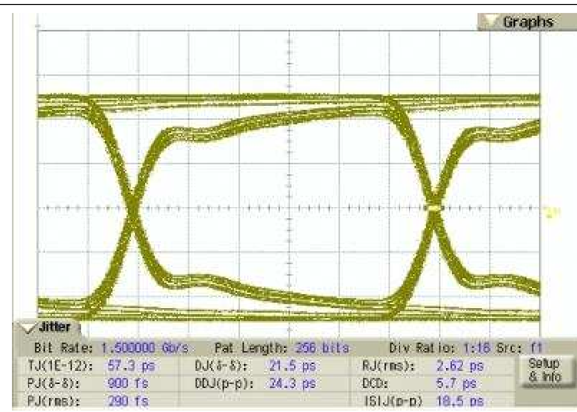
TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
67.5	38.6	2.11	363.4	595	318.48

图 15. Test Point 2



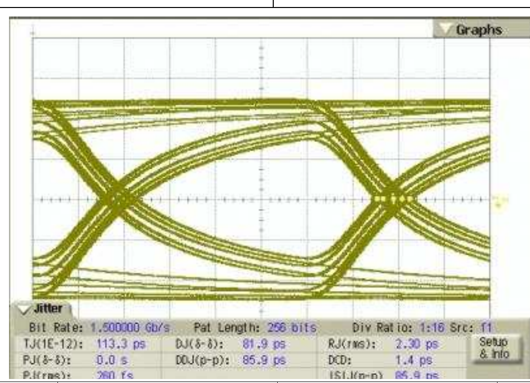
TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
44.9	13.2	2.31	753.1	649	604.02

图 16. Test Point 3



TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
57.3	21.5	2.62	672.8	632	442.42

图 17. Test Point 4 With LVPE802

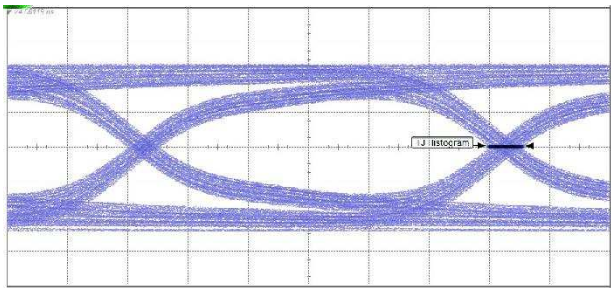


TJ	DJ	RJ	Eye	Eye	Eye
(1e-12) ps	(σ-σ) ps	(rms) ps	Amplitude mV	Width ps	Opening (mV)
113.3	81.9	2.3	322.8	493	217.48

图 18. Test Point 4 Without LVPE802

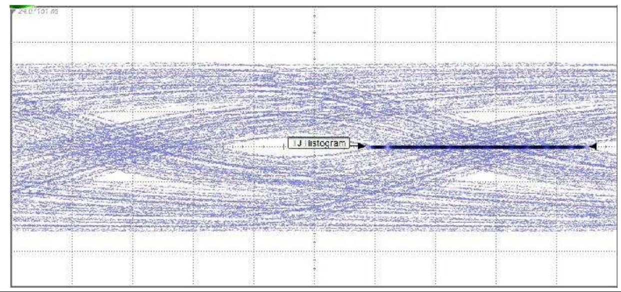
7.8.4 Jitter and VOD Results: Case 4 at 8 Gbps

图 21 Test Point 3 and 图 22 Test Point 4 were taken without pre-emphasis.



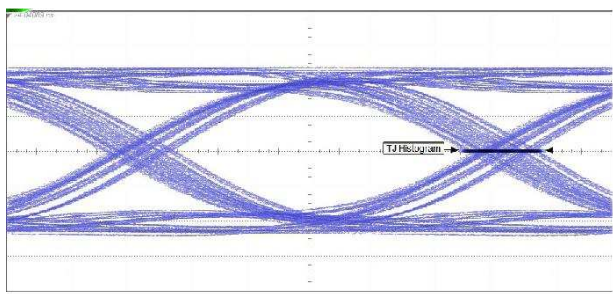
TJ (1e-12) ps	DJ (σ-σ) ps	RJ (rms) ps	Eye Amplitude mV	Eye Width ps	Eye Opening (mV)
14.4	10.1	0.31	580	108	274

图 19. Test Point 1



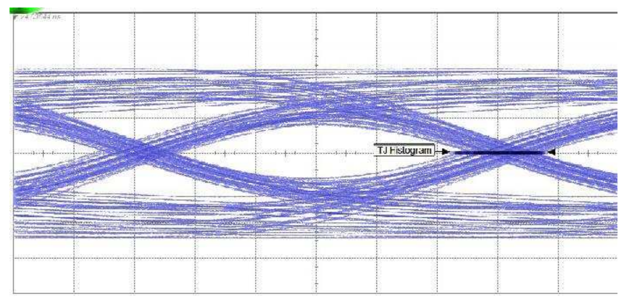
TJ (1e-12) ps	DJ (σ-σ) ps	RJ (rms) ps	Eye Amplitude mV	Eye Width ps	Eye Opening (mV)
78.1	68.9	0.67	310	45	48

图 20. Test Point 2



TJ (1e-12) ps	DJ (σ-σ) ps	RJ (rms) ps	Eye Amplitude mV	Eye Width ps	Eye Opening (mV)
30.6	23.6	0.51	406	86	292

图 21. Test Point 3



TJ (1e-12) ps	DJ (σ-σ) ps	RJ (rms) ps	Eye Amplitude mV	Eye Width ps	Eye Opening (mV)
34.4	26.8	0.56	262	85	95

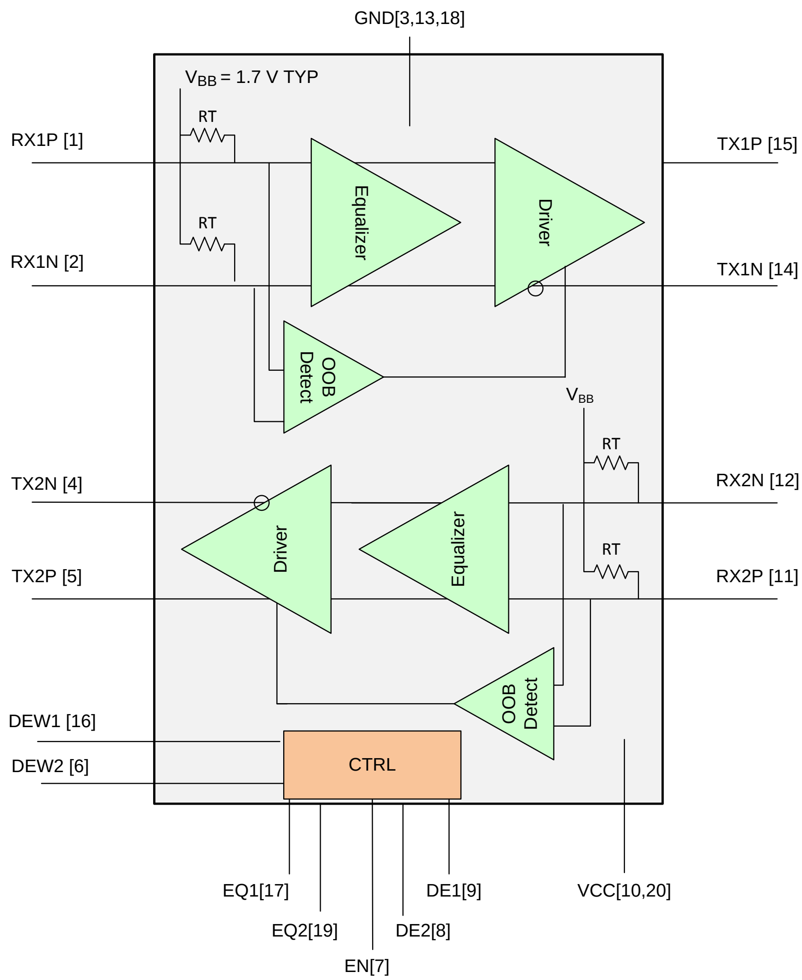
图 22. Test Point 4

8 Detailed Description

8.1 Overview

The SN75LVPE802 is a dual channel equalizer and redriver. The device operates over a wide range of signaling rates, supporting operation from DC to 8 Gbps. The wide operating range supports SATA Gen 1, 2, 3 (1.5 Gbps, 3.0 Gbps, and 6.0 Gbps respectively) as well as PCI Express 1.0, 2.0, 3.0 (2.5 Gbps, 5.0 Gbps, and 8.0 Gbps). The device also supports SATA Express (SATA 3.2) which is a form factor specification that allows for SATA and PCI Express signaling over a single connector.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 SATA Express

SATA Express (sometimes SATAe) is an electro-mechanical standard that supports both SATA and PCI Express storage devices. SATAe is standardized in the SATA 3.2 standard. The standard is concerned with providing a smooth transition from SATA to PCIe storage devices. The standard provides for standardized cables and connectors, and muxes the PCIe and SATA lanes at the host side so that either SATA compliant or PCIe compliant devices may operate with a host.

SATAe provides support for SATA1, SATA2 and SATA3 devices (operating from 1.5 Gbps to 6.0 Gbps), as well as PCIe1, PCIe2 and PCIe3 devices (operating from 2.5 Gbps to 8.0 Gbps).

Feature Description (接下页)

The SN75LVPE802 provides for equalization and re-drive of a single channel input signal complying with any of the SATA or PCIe standards available with SATAe.

The SATAe standard provides for a mechanism for a host to recognize and detect whether a SATA or PCIe device is plugged into the host. See the *Typical SATA Application* section for the details of the SATA Express Interface Detect operation.

8.3.2 Receiver Termination

The receiver has integrated terminations to an internal bias voltage. The receiver differential input impedance is nominally 100 Ω, with a ±15% variation.

8.3.3 Receiver Internal Bias

The SN75LVPE802 receiver is internally biased to 1.7 V, providing support for AC coupled inputs.

8.3.4 Input Equalization

The SN75LVPE802 incorporates programmable equalization. The EQ input controls the level of equalization that is used to open the eye of the received input signal. If the EQ input is left open, or pulled LO, 6 dB (at 3 GHz) of equalization is applied. When the EQ input is HIGH, the equalization is set to 13 dB (again at 3 GHz). 表 1 shows the equalization values discussed.

表 1. EQ and DE Settings

EQ1 OR EQ2	CH1 OR CH2 EQUALIZATION dB (at 6 Gbps)	CH1 OR CH2 EQUALIZATION dB (at 8 Gbps)	DE1 OR DE2	CH1 OR CH2 DE-EMPHASIS dB (at 6 Gbps)
NC (default)	0	0	NC (default)	-4
0	6	7	0	0
1	13	15	1	-2

8.3.5 OOB/Squelch

The SN75LVPE802 receiver incorporates an Out-Of-Band (OOB) detection circuit in addition to the main signal chain receiver. The OOB detector continuously monitors the differential input signal to the device. The OOB detector has a 50-mVpp entry threshold. If the differential signal at the receiver input is less than the OOB entry threshold, the device transmitter transitions to squelch. The SN75LVPE802 enters squelch within 5 ns of the input signal falling below the OOB entry threshold. The SN75LVPE802 continues to monitor the input signal while in squelch. While in squelch, if the OOB detector determines that the input signal now exceeds the 90 mVpp exit threshold, the SN75LVPE802 exits squelch within 5 ns.

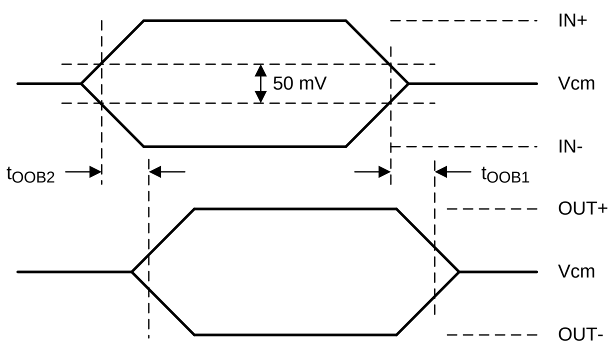


图 23. OOB Enter and Exit Timing Receiver Input Termination Is Disabled

When the SN75LVPE802 enters squelch state the transmitter output is squelched. The transmitter non-inverting (TX+) output and the transmitter inverting output (TX-) are both driven to the transmitter nominal common mode voltage which is 1.7 V.

8.3.6 Auto Low Power

The SN75LVPE801 also includes an Auto Low Power Mode (ALP). ALP is entered when the differential input signal has been less than 50 mV for > 10 µs. The device enters and exits Low Power Mode by actively monitoring the input signal level. In this state the device selectively shuts off internal circuitry to lower power by > 90% of its normal operating power. While in ALP mode the device continues to actively monitor input signal levels. When the input signal exceeds the OOB exit threshold level, the device reverts to the active state. Exit time from Auto Low Power Mode is < 50 ns (max).

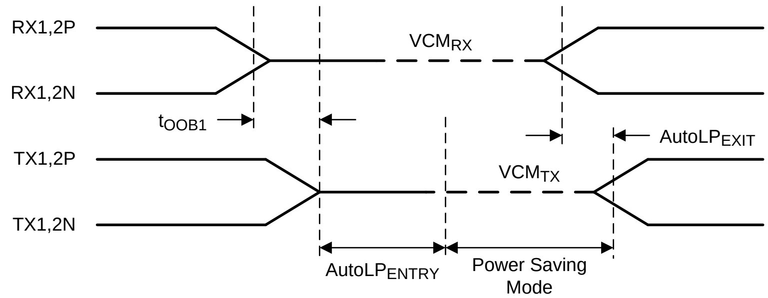


图 24. Auto Low Power Mode Entry and Exit Timing

8.3.7 Transmitter Output Signal

The SN75LVPE802 differential output signal is 650 mVpp when de-emphasis is disabled (DE input is open or pulled low).

8.3.8 Transmitter Common Mode

The SN75LVPE802 transmitter common mode output is set to 1.7 V.

8.3.9 De-Emphasis

The SN75LVPE802 device provides the de-emphasis settings shown in 表 2. De-emphasis control is independent for each channel, controlled by the DE1 and DE2 pin settings as shown in 表 2. The reference for the de-emphasis settings available in the device is the transition bit amplitude for each given configuration; this transition bit amplitude is different at 0 dB than the –2-dB and –4-dB settings by design. DEW1 and DEW2 control the DE durations for channels one and two, respectively. 表 2 lists the recommended settings for these control pins. Output de-emphasis is capable of supporting FR4 trace at the output anywhere from 2 in. (5.1 cm) to 12 in. (30.5 cm) at SATA 3G/6G speed.

表 2. TX and Rx EQ and DE Pulse-Duration Settings

DEW1 OR DEW2	DEVICE FUNCTION → DE WIDTH FOR CH1/CH2
0	De-emphasis pulse duration, short
1 (default)	De-emphasis pulse duration, long

8.3.10 Transmitter Termination

The SN75LVPE802 transmitter includes integrated terminations. The receiver differential output impedance is nominally 100 Ω, with a ≤ 22% variation.

8.4 Device Functional Modes

8.4.1 Low-Power Mode

There are two low-power modes supported by the SN75LVPE802 device, listed as follows:

1. Standby mode (triggered by the EN pin, EN = 0 V)
   - The enable (EN) pin controls th low-power mode. Pulling this pin LOW puts the device in standby mode within 2 µs (max). In this mode, the device drives all its active components to their quiescent level, and differential outputs Hi-Z (open). Maximum power dissipation in this mode is 5 mW. Exiting from this mode to normal operation requires a maximum latency of 5 µs.
2. Auto low-power mode (triggered when a given channel is in the electrically idle state for more than 100 µs and EN = VCC)
   - The device enters and exits low-power mode by actively monitoring the input signal (V_{IDp-p}) level on each of its channels independently. When the input signal on either or both channels is in the electrically idle state, that is, V_{IDp-p} < 50 mV and stays in this state for > 100 µs, the associated channel enters into the low-power state. In this state, output of the associated channel goes to VCM and the device selectively shuts off some circuitry to lower power by > 80% of its normal operating power. Exit time from the auto low-power mode is < 50 ns.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN75LVPE802 can be used for SATA applications as well as SATA Express applications. The device supports SATA Gen1, Gen2, and Gen3 applications with data rates from 1.5 to 6 Gbps. The built-in equalization circuits provide up to 13 dB of equalization at 3 GHz. This equalization can support SATA GEN2 (3 Gbps) applications over up to 50 inches of FR-4 material. The same 13 dB equalizer is suited to SATA Gen3 (6 Gbps) applications up to 40 inches of FR4.

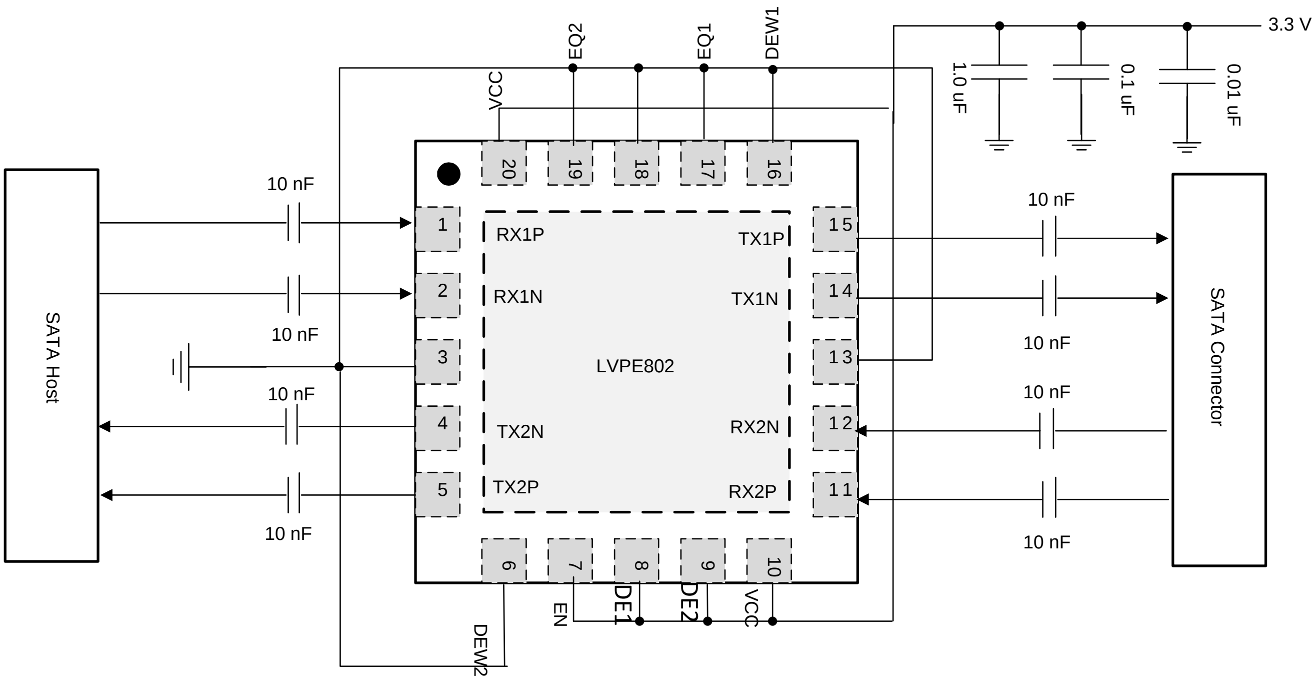
In addition to SATA applications, the SN75LVPE802 can support SATA Express applications. SATA Express provides a standardized interface to support both SATA (Gen1, Gen2, and Gen3) and PCI Express (PCIe 1, 2 and 3).

All applications of the SN75LVPE802 share some common applications issues. For example, power supply filtering, board layout, and equalization performance with varying interconnect losses. Other applications issues are specific, such as implementing receiver detection for SATA Express applications. The Typical Application examples demonstrate common implementations of the SN75LVPE802 supporting SATA, as well as SATA Express applications.

9.2 Typical SATA Application

This typical application describes how to configure the EQ, DE, and DEW configuration pins of the SN75LVPE802 device based on board trace length between the SATA Host and the SN75LVPE802 and the SN75LVPE802 and SATA Device. Actual configuration settings may differ due to additional factors such as board layout, trace widths, and connectors used in the signal path.

Typical SATA Application (接下页)



(1) Place supply caps close to device pin

(2) EN can be left open or tied to supply when no external control is implemented

(3) Output de-emphasis selection is set at -3 dB, EQ at 7 dB and DE width for SATA I/II/III operation for both channels.

(4) Actual EQ/DE/DE width settings will depend on device placement relative to host and SATA connector.

图 25. Typical Device Implementation

9.2.1 Design Requirements

Typically, system trace length from the SATA host to the SN75LVPE802 device and trace length from the SN75LVPE802 device to a SATA device differ and require different equalization and de-emphasis settings for the host side and device side.

For example:

- A system with a 6-inch trace from the SN75LVPE802 device to a SATA host may set EQ1 (Rx1±) to 7 dB, and DE2 (Tx2±) to –2 dB and DEW2 (Tx2±) to long pulse duration.
- The same system with a 1-inch trace from the SN75LVPE802 device to a SATA HDD may set EQ2 (Rx2±) to 0 dB, and DE1 (Tx1±) to 0 dB and DEW1 (Tx1±) to short pulse duration.

Refer to Application Curves for recommended EQ, DE and DEW settings based on trace length. It is highly recommended to add both pullup- and pulldown-resistor options in the layout to fine-tune the settings if needed. Input Signal Characteristics:

- Data Rate: 6 Gbps
- Pattern: PRBS7
- No pre-emphasis
- Signal amplitude: 500 mVpp
- 18-inch SMA cable from test equipment to input and output trace

Typical SATA Application (接下页)

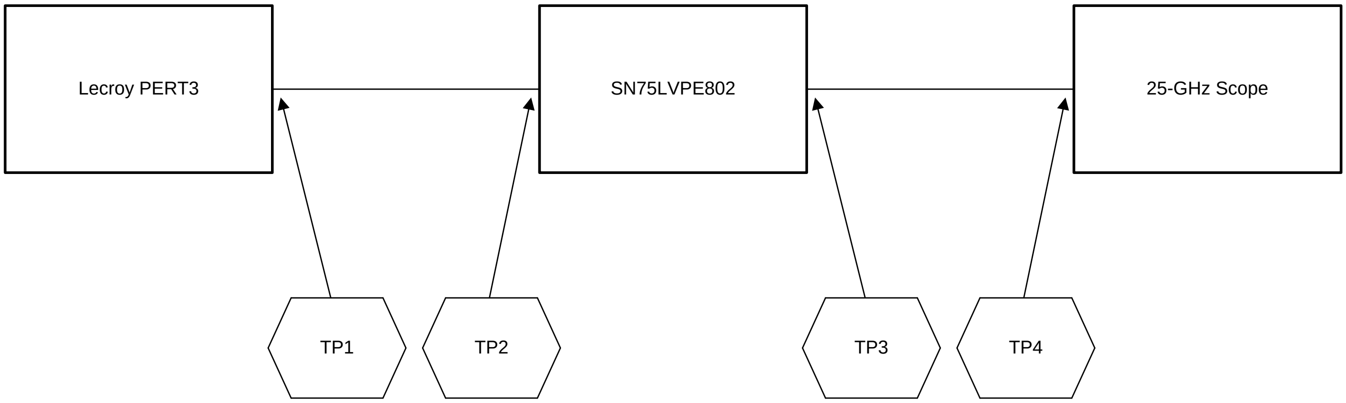


图 26. Measurement Set-up

9.2.2 Detailed Design Procedure

9.2.2.1 Equalization Configuration

Each differential input of the SN75LVPE802 device has programmable equalization in the front stage. The equalization setting is shown in 表 1. The input equalizer is designed to recover a signal even when no eye is present at the receiver and effectively supports FR4 trace input from 3 inches to greater than 24 inches at SATA 6 Gbps speed.

9.2.3 De-emphasis Configuration

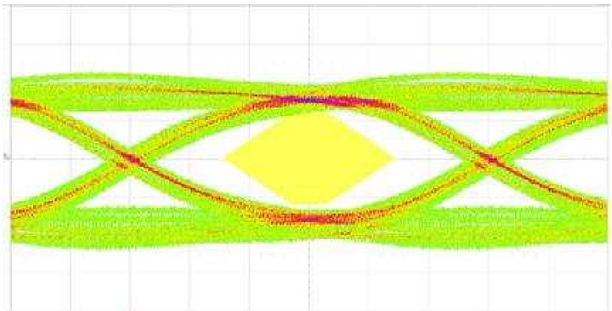
The SN75LVPE802 device provides the de-emphasis settings shown in 表 1 and 表 2. TX and Rx EQ and DE Pulse-Duration Settings. De-emphasis is controlled independently for each channel and is set by the DE1, DE2, DEW1 and DEW2 pins of the SN75LVPE802 device.

Typical SATA Application (接下页)

9.2.4 Application Curves

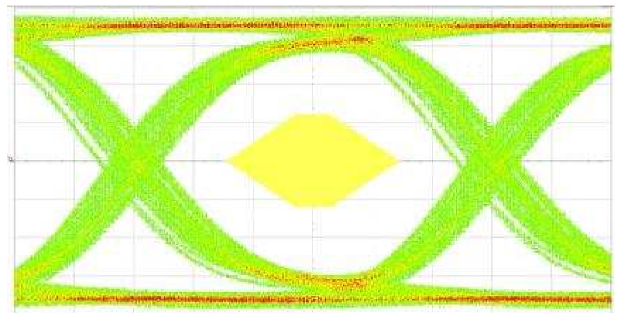
Typical application curves correspond to SATA application at 6 Gbps.

9.2.4.1 SN75LVPE802 Equalization Settings for Various Input Trace Length



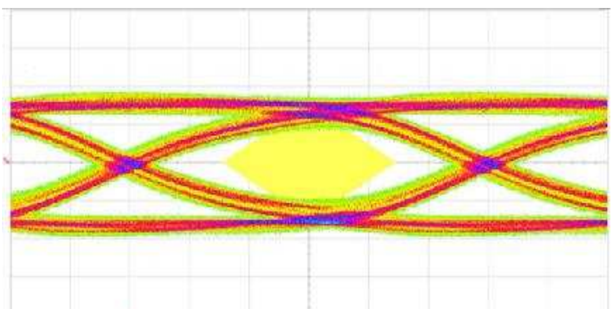
Input Trace Length = 3 in.
EQ1, EQ2 Setting = NC (0 dB)

图 27. Input Eye (TP2)



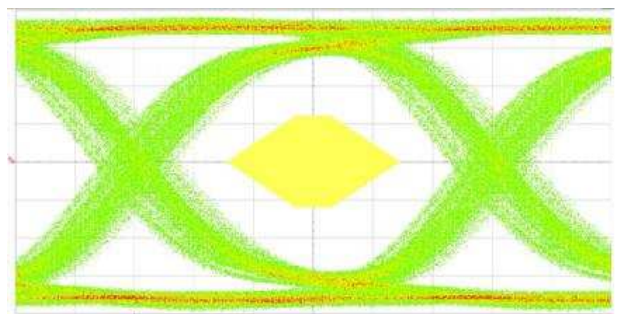
Input Trace Length = 3 in.
EQ1, EQ2 Setting = NC (0 dB)

图 28. Output Eye (TP4)



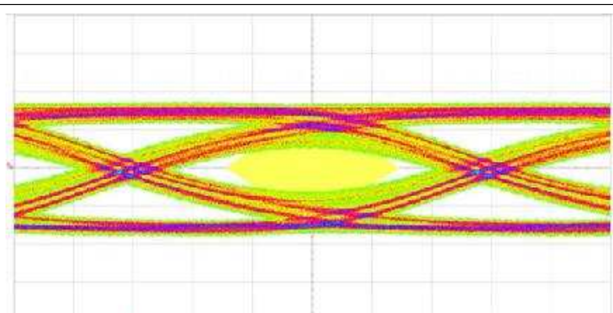
Input Trace Length = 6 in.
EQ1, EQ2 Setting = 0 (7 dB)

图 29. Input Eye (TP2)



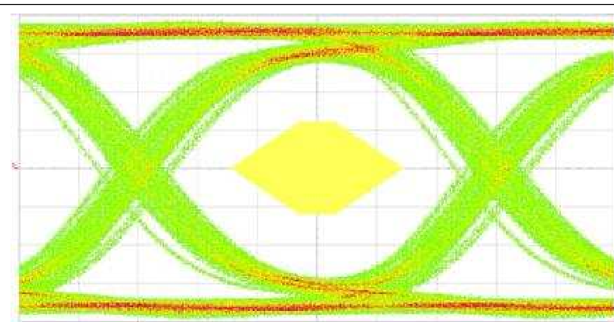
Input Trace Length = 6 in.
EQ1, EQ2 Setting = 0 (7 dB)

图 30. Output Eye (TP4)



Input Trace Length = 12 in.
EQ1, EQ2 Setting = 0 (7 dB)

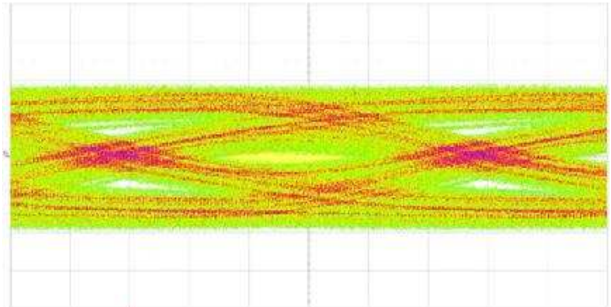
图 31. Input Eye (TP2)



Input Trace Length = 12 in.
EQ1, EQ2 Setting = 0 (7 dB)

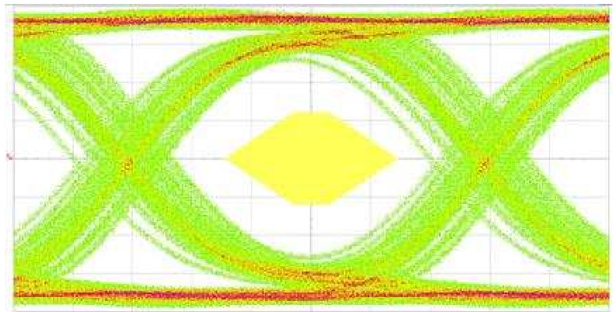
图 32. Output Eye (TP4)

Typical SATA Application (接下页)



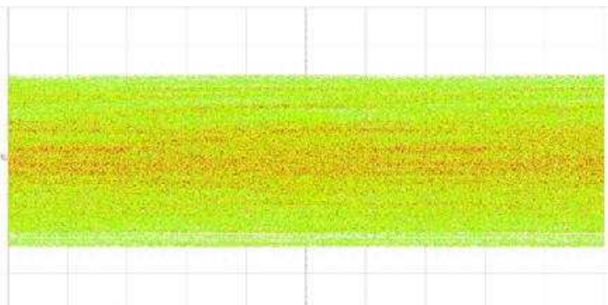
Input Trace Length = 24 in.
EQ1, EQ2 Setting = 0 (7 dB)

图 33. Input Eye (TP2)



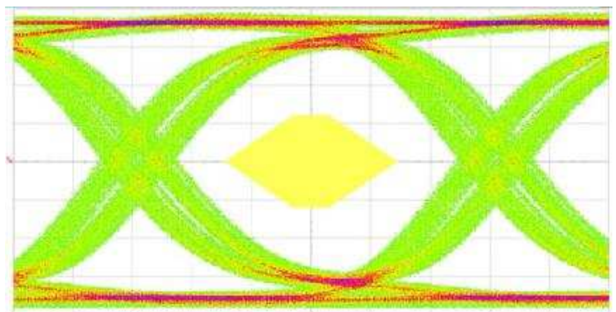
Input Trace Length = 24 in.
EQ1, EQ2 Setting = 0 (7 dB)

图 34. Output Eye (TP4)



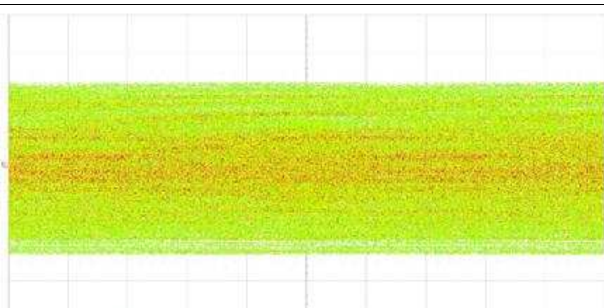
Input Trace Length = 36 in.
EQ1, EQ2 Setting = 1 (14 dB)

图 35. Input Eye (TP2)



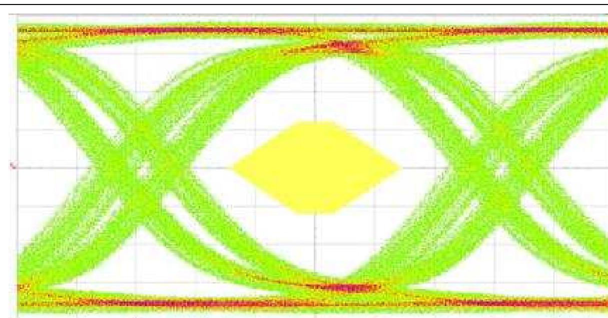
Input Trace Length = 36 in.
EQ1, EQ2 Setting = 1 (14 dB)

图 36. Output Eye (TP4)



Input Trace Length = 48 in.
EQ1, EQ2 Setting = 1 (14 dB)

图 37. Input Eye (TP2)

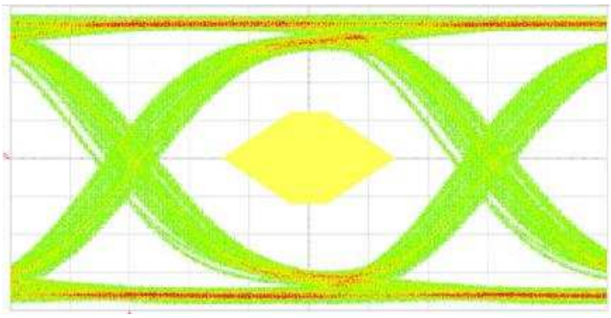


Input Trace Length = 48 in.
EQ1, EQ2 Setting = 1 (14 dB)

图 38. Output Eye (TP4)

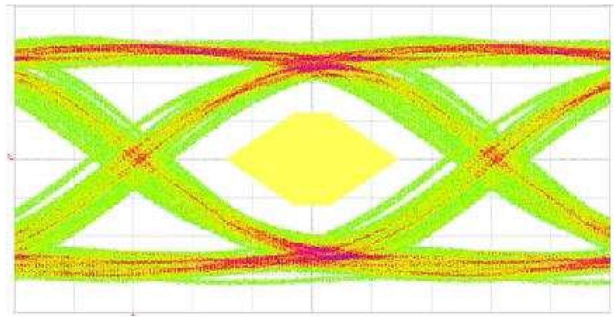
Typical SATA Application (接下页)

9.2.4.2 SN75LVCP802 De-emphasis Settings For various Output Trace Lengths



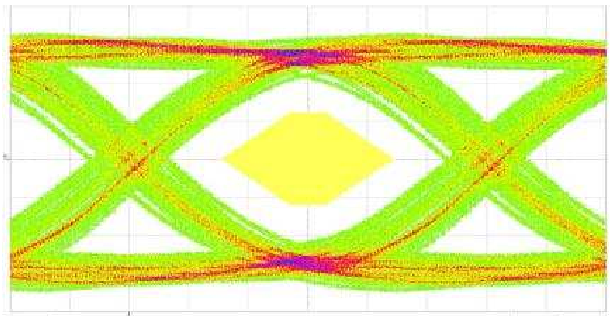
Output Trace Length = 0 in. DE, DE2 Setting = 0 (0 dB)
DEW1, DEW2 Setting = 0 (Short pulse duration)

图 39. Output Eye (TP4)



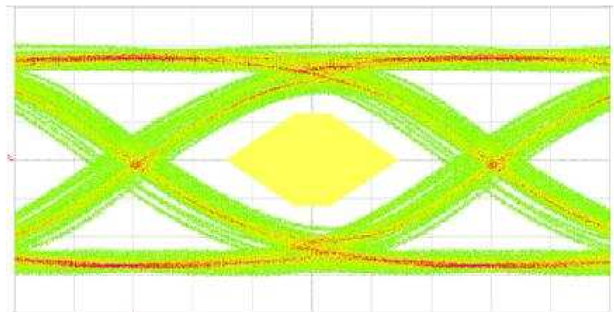
Output Trace Length = 3 in. DE, DE2 Setting = 0 (0 dB)
DEW1, DEW2 Setting = 0 (Short pulse duration)

图 40. Output Eye (TP4)



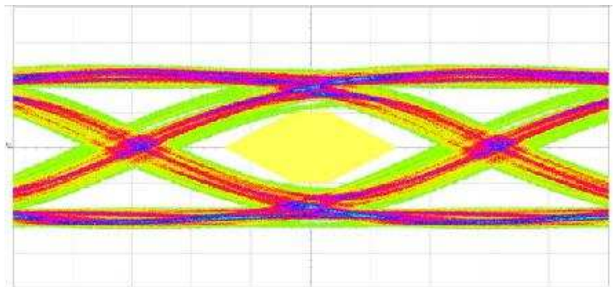
Output Trace Length = 6 in. DE, DE2 Setting = 1 (-2 dB)
DEW1, DEW2 Setting = 1 (Long pulse duration)

图 41. Output Eye (TP4)



Output Trace Length = 12 in. DE, DE2 Setting = 1 (-2 dB)
DEW1, DEW2 Setting = 1 (Long pulse duration)

图 42. Output Eye (TP4)



Output Trace Length = 12 in. DE, DE2 Setting = NC (-4 dB)
DEW1, DEW2 Setting = 1 (Long pulse duration)

图 43. Output Eye (TP4)

9.3 SATA Express Applications

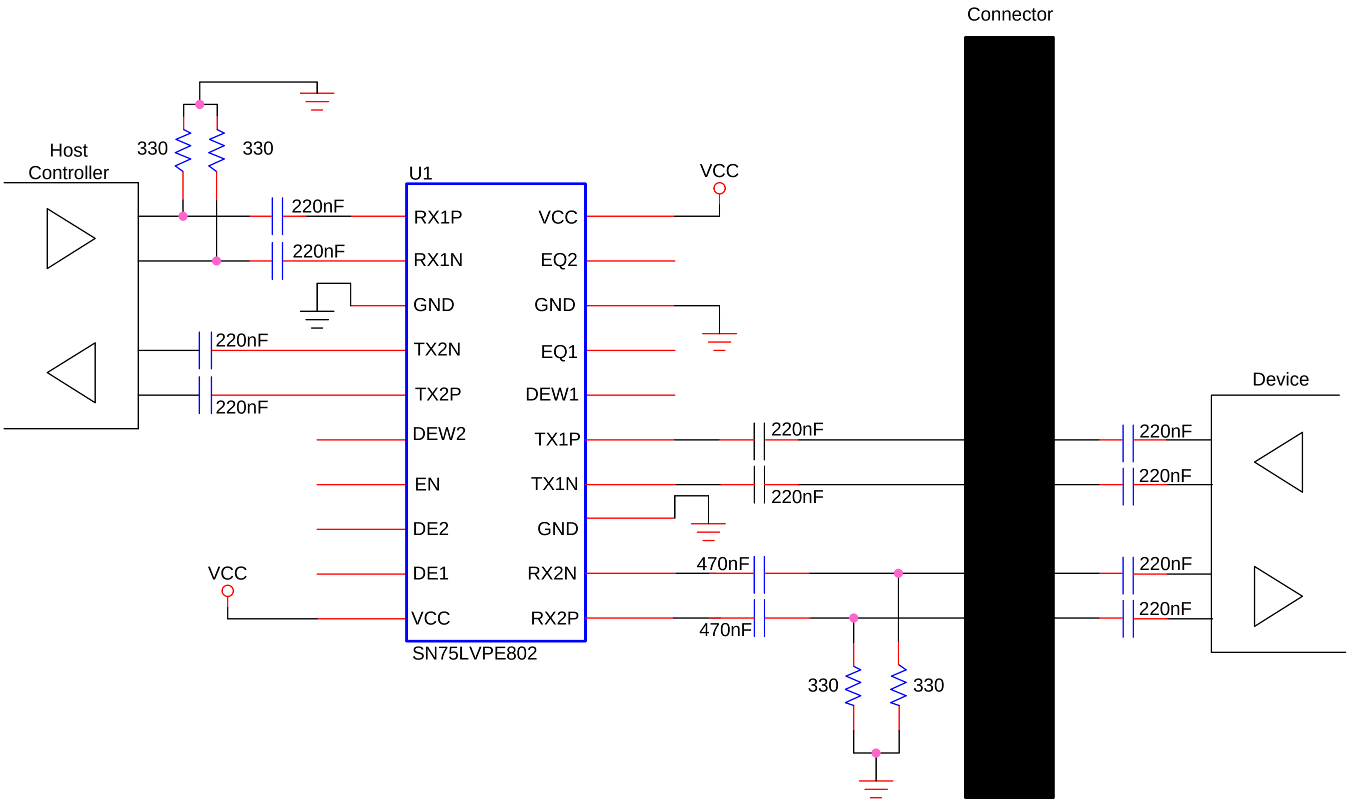


图 44. SATAe Reference Schematic

9.3.1 Detailed Design Procedure

图 44 is a reference schematic of a SATAe implementation using the SN75LVPE802. With a SATAe design, both SATA and PCI Express must be supported. SATAe supports both cabled and direct connections. Using a cabled application as an example, the SATAe power connector includes an Interface Detect (IFDet, power connector pin P4) signal that indicates whether a SATA client or a PCIe client is connected.

When the SATAe host determines that a PCIe client is connected, the SATAe host performs receiver detection. Receiver detection determines the presence of a client by detecting the load impedance. The transmitter performs a common mode voltage shift, and measures the rate at which the voltage at the transmitter output changes. The rate of change indicates if a client is present (fast charging when a low impedance load is present, or slow charging when the load is open or high impedance). With the implementation in 图 44, 330-Ω pulldowns have been inserted between the host and the SN75LVPE802. The pulldown resistors indicate to the host that a client is present. While an actual client would be expected to have an active load of 50 Ω single ended, the 330 Ω is chosen here to meet two requirements. The 330 Ω is low enough to force the SATAe host to decide that a receiver is present, while also high enough to only marginally affect the load when the SN75LVPE802 is active, and presenting a 50-Ω load. With the 50 Ω and 330 Ω are both present, the parallel combination of 43 Ω is satisfactory for most applications.

Assuming that the SATAe host has detected (via IFDet) that a SATA client is present, the SATAe host communicates with the client via the SN75LVPE802. The SATA standard does not have a receiver detection mode as is present in PCIe. A SATA host does use OOB signaling to communicate identification information. The SN75LVPE802 incorporates an OOB detector in order to support OOB signaling through the device. The OOB detector drives a squelch circuit on the SN75LVPE802 output transmitter. (See *OOB/Squelch* for more details on the OOB/Squelch circuitry.)

SATA Express Applications (接下页)

Returning to 图 44, there is a 200-nF AC coupling capacitors on the device or client side of the interface. These capacitors allow interfacing to both SATA and PCIe clients. In the case of a PCIe client, the 200 nF is within the acceptable range for all PCIe devices. When a SATA client is present, the 200 nF capacitor has little effect on the overall link, as it appears in series with the 12-nF (max) AC coupling capacitor incorporated into the SATA client. The 200 nF in series with the 12 nF presents an effective capacitance of 11.3 nF, as expected less than the 12-nF maximum permitted.

9.3.2 PCIe Applications

PCIe-only applications are implemented in a manner very similar to SATA Express applications as covered in *Detailed Design Procedure*. Looking at 图 45 and comparing it to the SATA Express application in Figure 8 20 SATAe Reference Schematic, a single change is noted. For PCIe applications the 220 nF AC-coupling capacitors on the Host-to-Device link are relocated from the Device side of the connector to the Host side. No other changes are required.

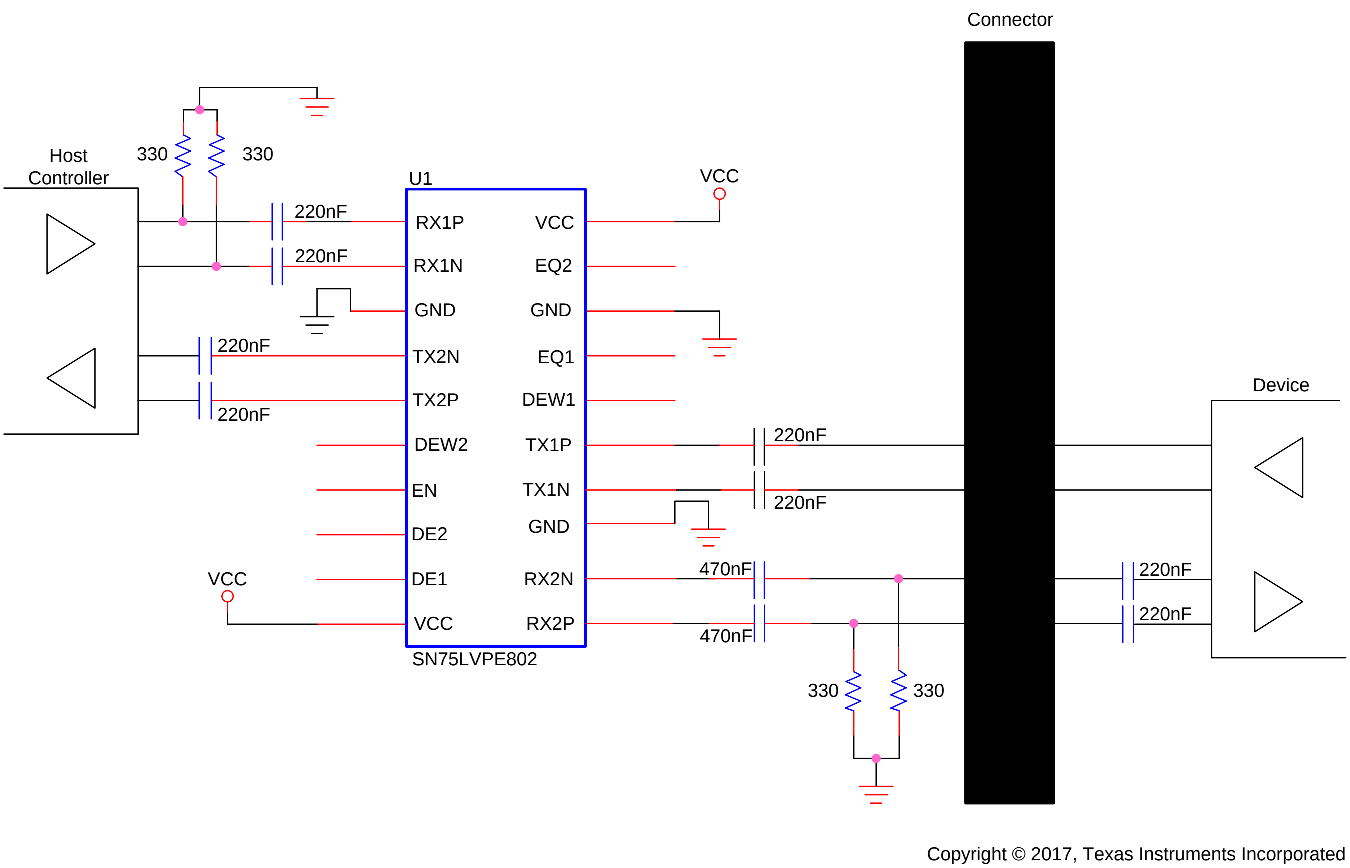


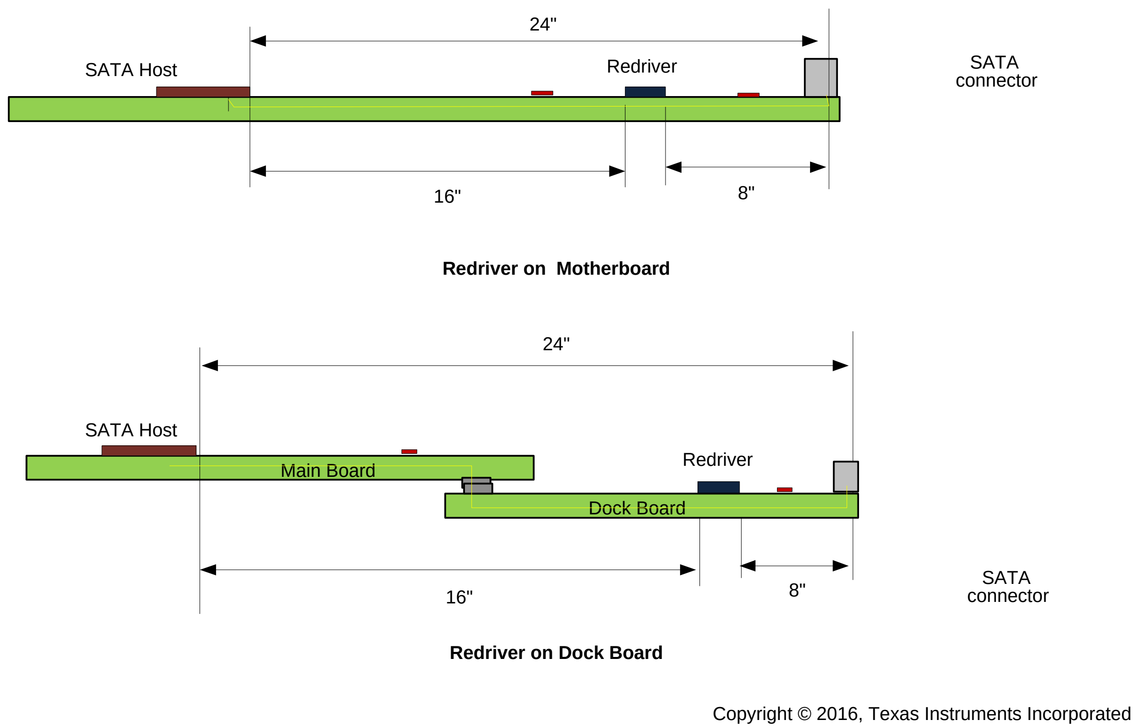
图 45. SN75LVPE802 PCIe Reference Schematic

10 Power Supply Recommendations

The design of SN75LVPE802 device is for operation from one 3.3-V supply. Always practice proper power supply sequencing procedure. Apply VCC first, before application of any input signals to the device. The power down sequence is in reverse order.

11 Layout

11.1 Layout Guidelines



(1) Trace lengths are suggested values based on TI spice simulations (done over programmable limits of input EQ and output de-emphasis) to meet SATA loss and jitter spec. Actual trace length supported by the LVPE802 may be more or less than suggested values and will depend on board layout, trace widths and number of connectors used in the SATA signal path.

图 46. Trace Length Example for LVPE802

11.2 Layout Example

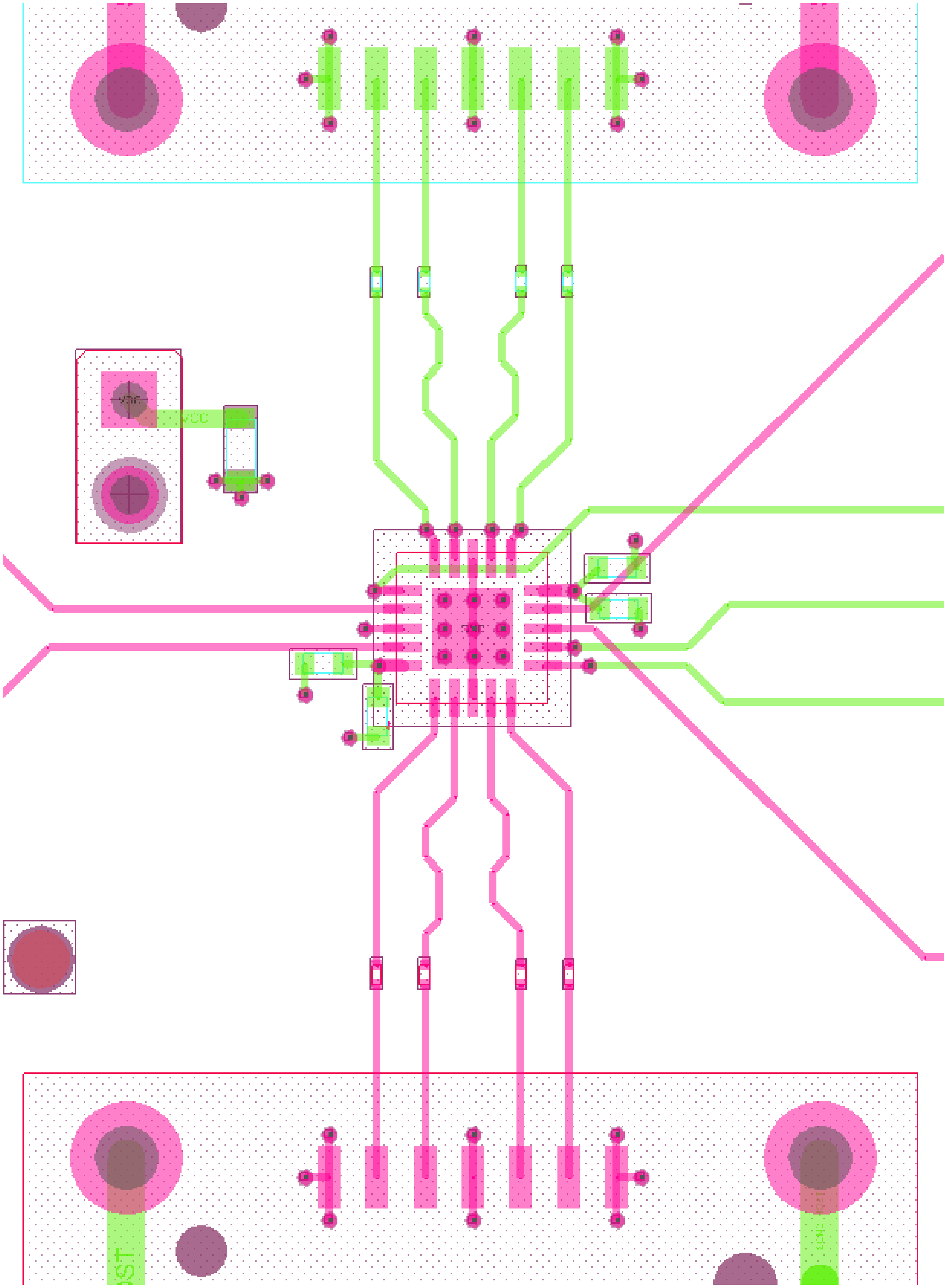


图 47. Example Layout

12 器件和文档支持

12.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

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12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LVPE802RTJR	Active	Production	QFN (RTJ) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	LVP802
SN75LVPE802RTJR.B	Active	Production	QFN (RTJ) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	LVP802
SN75LVPE802RTJT	Active	Production	QFN (RTJ) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	LVP802
SN75LVPE802RTJT.B	Active	Production	QFN (RTJ) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 85	LVP802

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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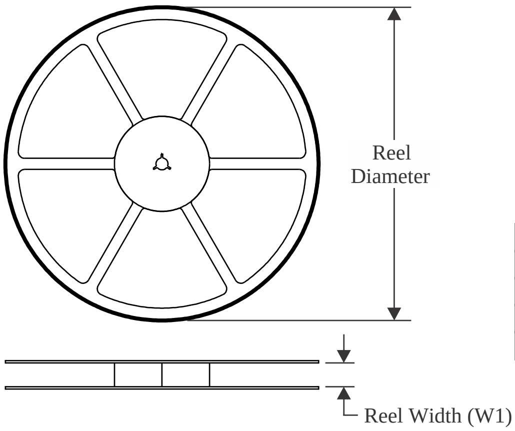
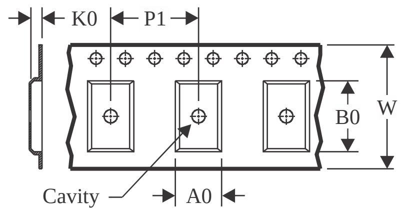
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

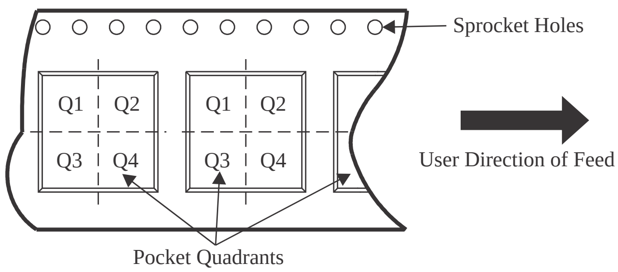


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

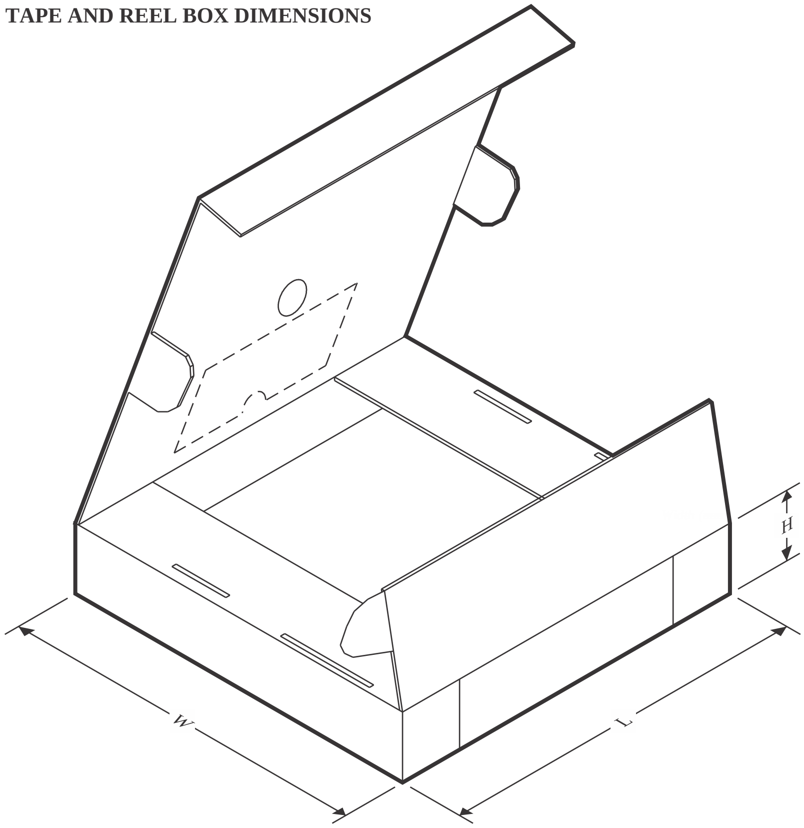
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVPE802RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN75LVPE802RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVPE802RTJR	QFN	RTJ	20	3000	346.0	346.0	33.0
SN75LVPE802RTJT	QFN	RTJ	20	250	210.0	185.0	35.0

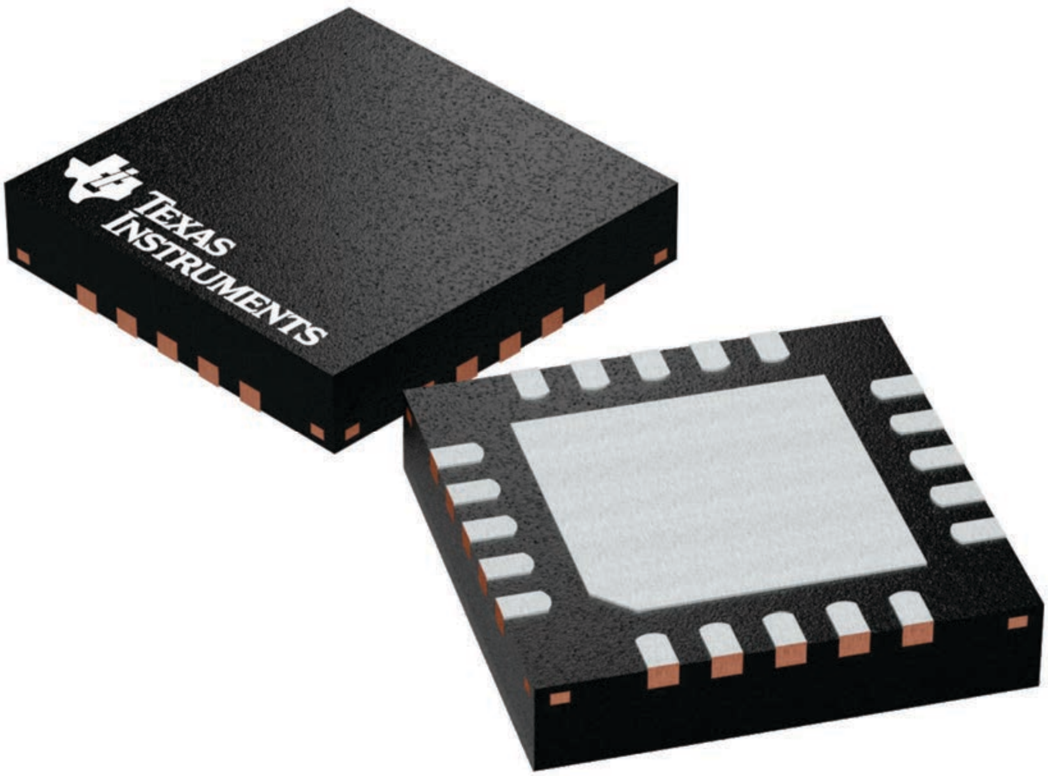
RTJ 20

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

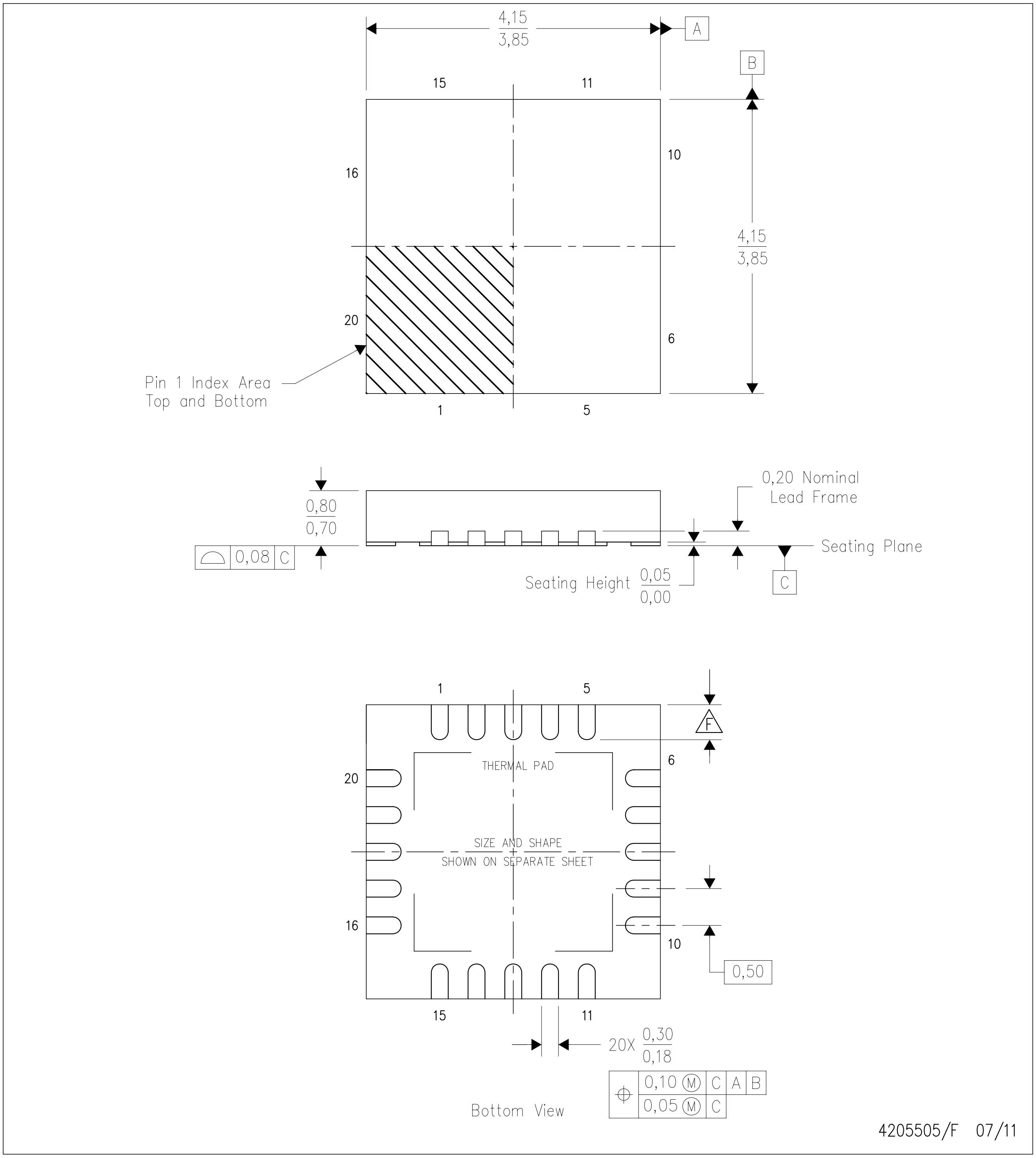
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224842/A

RTJ (S-PWQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

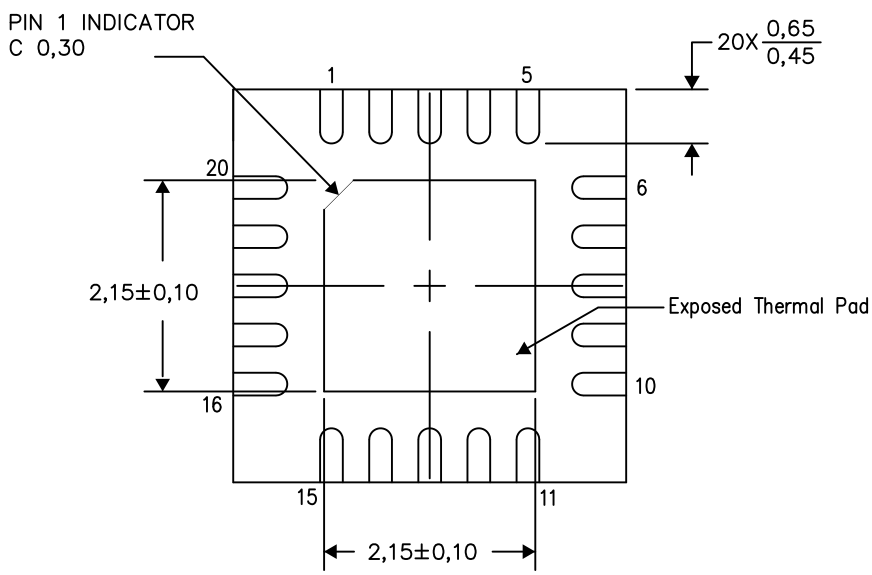
RTJ (S-PWQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206256-3/V 05/15

NOTE: All linear dimensions are in millimeters

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