TAS5624A 150W 立体声/300W 单声道 PurePath™ HD 数字输入 D 类功率级

1 特性

- PurePath™HD 集成反馈提供：
  - 1W 功率/4Ω 负载条件下的总谐波失真 (THD) 为 0.025%
  - 电源抑制比 (PSRR) > 65dB（无输入信号）
  - （A 加权）信噪比 (SNR) > 105dB
- 用于控制 G 类电源的预钳位输出
- 通过使用 40mΩ 输出金属氧化物半导体场效应晶体管 (MOSFET) 减小了散热器体积，满输出功率时效率 > 90%
- 总谐波失真+噪声 (THD+N) 为 10% 时的输出功率
  - 150W/4Ω，桥接负载 (BTL) 立体声配置
  - 300W/2Ω，并行桥接负载 (PBTL) 单声道配置
- 总谐波失真+噪声 (THD+N) 为 10% 时的输出功率
  - 125W/4Ω，桥接负载 (BTL) 立体声配置
  - 250W/2Ω，并行桥接负载 (PBTL) 单声道配置
- 启动时无喀哒声和噼啪声
- 采用具有错误报告功能的自我保护设计，包含欠压保护 (UVP)、过热保护和短路保护
- 采用推荐的系统设计时，符合电磁干扰 (EMI) 标准
- 采用 44 引脚散热薄型小外形尺寸 (HTSSOP) (DDV) 封装，减小了电路板尺寸

2 应用

- 蓝光碟™和 DVD 接收器
- 高功率条形音响
- 有源超低音扬声器和有源扬声器
- 微型 Combo 系统

3 说明

TAS5624A 器件是一款基于 TAS5614A 的散热增强型 D 类功率放大器，其使用大型 MOSFET 提升功率效率，并采用新型栅极驱动方案降低空闲状态下和输出信号较低时的损耗，从而减小散热器尺寸。

该器件可使用独特的预钳位输出信号来控制 G 类电源。这一优势与 TAS5624A 的低空闲损耗和高功率效率相结合，可实现行业领先水平的效率，从而确保构建超级“绿色”系统。

TAS5624A 使用恒定电压增益。内部匹配的增益电阻保证了器件能够拥有较高的电源抑制比，从而使输出电压只取决于音频输入电压，不受任何电源的影响。

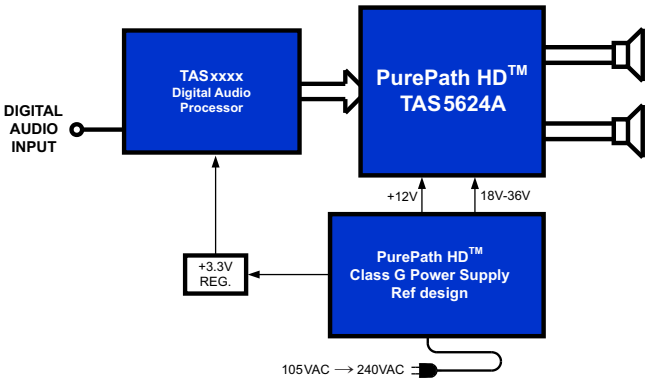
TAS5624A 的高集成度使得放大器易于使用；另外，使用 TI 的参考原理图和 PCB 布局缩短了设计时间。TAS5624A 采用节省空间的表面贴装 44 引脚 HTSSOP 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TAS5624A	HTSSOP (44)	14.00mm x 6.10mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

TAS5624A 典型应用框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (May 2012) to Revision A **Page**

- 已添加 *ESD 额定值表*，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 ... 1

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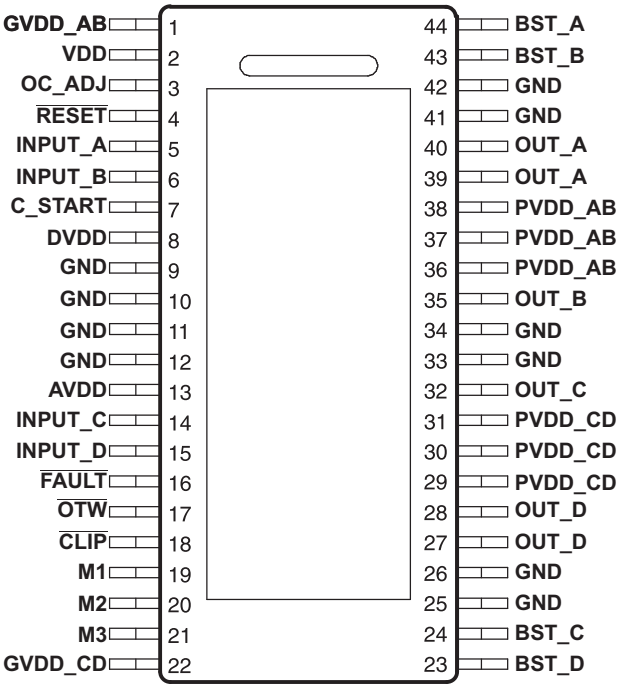
5 Device Comparison Table

FEATURES	TAS5624A	TAS5612A	TAS5612LA	TAS5614A	TAS5614LA	TAS5622A
Maximum Power to Single-Ended Load	75		65		75	65
Maximum Power to Bridge Tied Load	200	165	125	200	150	150
Maximum Power to Parallel Bridge Tied Load	400	250	250	300	300	300
Minimum Supported Single-Ended Load	2		2		2	2
Minimum Supported Bridge Tied Load	3	3	4	3	4	3
Minimum Supported Parallel Bridge Tied Load	1.5	2	2	2	2	2
Closed-Loop and Open-Loop	Closed	Closed	Closed	Closed	Closed	Closed
Maximum Speaker Outputs (#)	4	2	4	2	4	2
Input Type	PWM	PWM	PWM	PWM	PWM	PWM
Control Type	Hardware	Hardware	Hardware	Hardware	Hardware	Hardware

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6 Pin Configuration and Functions

DDV Package
44-Pin HTSSOP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
AVDD	13	P	Internal voltage regulator, analog section
BST_A	44	P	Bootstrap pin, A-side
BST_B	43	P	Bootstrap pin, B-side
BST_C	24	P	Bootstrap pin, C-side
BST_D	23	P	Bootstrap pin, D-side
C_START	7	O	Start-up ramp
$\overline{\text{CLIP}}$	18	O	Clipping warning; open-drain; active-low
DVDD	8	P	Internal voltage regulator, digital section
$\overline{\text{FAULT}}$	16	O	Shutdown signal, open-drain; active-low
GND	9, 10, 11, 12, 25, 26, 33, 34, 41, 42	P	Ground
GVDD_AB	1	P	Gate-drive voltage supply; AB-side
GVDD_CD	22	P	Gate-drive voltage supply; CD-side
INPUT_A	5	I	PWM Input signal for half-bridge A
INPUT_B	6	I	PWM Input signal for half-bridge B
INPUT_C	14	I	PWM Input signal for half-bridge C
INPUT_D	15	I	PWM Input signal for half-bridge D
M1	19	I	Mode selection 1 (LSB)
M2	20	I	Mode selection 2
M3	21	I	Mode selection 3 (MSB)

(1) I = Input, O = Output, and P = Power
(2) Located on the top side of the device for convenient thermal coupling to the heat sink.

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Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
OC_ADJ	3	O	Overcurrent threshold programming pin
$\overline{OTW}$	17	O	Overtemperature warning; open-drain; active-low
OUT_A	39, 40	O	Output, half-bridge A
OUT_B	35	O	Output, half-bridge B
OUT_C	32	O	Output, half-bridge C
OUT_D	27, 28	O	Output, half-bridge D
PowerPAD™	—	P	Ground, connect to grounded heat sink
PVDD_AB	36, 37, 38	P	PVDD supply for half-bridge A and B
PVDD_CD	29, 30, 31	P	PVDD supply for half-bridge C and D
$\overline{RESET}$	4	I	Device reset Input; active-low
VDD	2	P	Input power supply

Mode Selection Pins

MODE PINS			PWM Input(1)	OUTPUT CONFIGURATION	INPUT A	INPUT B	INPUT C	INPUT D	MODE
M3	M2	M1							
0	0	0	2N + 1	2 × BTL	PWMa	PWMb	PWMc	PWMd	AD Mode
0	0	1	1N + 1(2)	2 × BTL	PWMa	Unused	PWMc	Unused	AD Mode
0	1	0	2N + 1	2 × BTL	PWMa	PWMb	PWMc	PWMd	BD Mode
0	1	1	1N + 1(2)	1 × BTL + 2 × SE	PWMa	Unused	PWMc	PWMd	AD Mode
1	0	0	2N + 1	1 × PBTL	PWMa	PWMb	0	0	AD Mode
1	0	0	1N + 1(2)	1 × PBTL	PWMa	Unused	0	1	AD Mode
1	0	0	2N + 1	1 × PBTL	PWMa	PWMb	1	0	BD Mode
1	0	1	1N + 1	4 × SE(3)	PWMa	PWMb	PWMc	PWMd	AD Mode

(1) The 1N and 2N naming convention is used to indicate the number of PWM lines to the power stage per channel in a specific mode.
(2) Using 1N interface in BTL and PBTL mode results in increased DC offset on the output terminals.
(3) The 4 × SE mode can be used as 1 × BTL + 2 × SE configuration by feeding a 2N PWM signal to either INPUT_AB or INPUT_CD for improved DC offset accuracy

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

	MIN	MAX	UNIT
VDD to GND, GVDD_X(2) to GND	–0.3	13.2	V
PVDD_X(2) to GND, OUT_X to GND, BST_X to GVDD_X(2)	–0.3	50	V
BST_X to GND(3)	–0.3	62.5	V
DVDD to GND	–0.3	4.2	V
AVDD to GND	–0.3	8.5	V
OC_ADJ, M1, M2, M3, C_START, INPUT_X to GND	–0.3	4.2	V
$\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, $\overline{\text{OTW}}$, $\overline{\text{CLIP}}$, to GND	–0.3	4.2	V
Maximum continuous sink current ($\overline{\text{FAULT}}$, $\overline{\text{OTW}}$, $\overline{\text{CLIP}}$)		9	mA
Maximum operating junction temperature, T_J	0	150	°C
Lead temperature	260	260	°C
Storage temperature, T_{stg}	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) GVDD_X and PVDD_X represents a full-bridge gate drive or power supply. GVDD_X is GVDD_AB or GVDD_CD, PVDD_X is PVDD_AB or PVDD_CD
(3) Maximum BST_X to GND voltage is the sum of maximum PVDD to GND and GVDD to GND voltages minus a diode drop.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
PVDD_X	Full-bridge supply		DC supply voltage	12	36	38	V
GVDD_X	Supply for logic regulators and gate-drive circuitry		DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage		DC supply voltage	10.8	12	13.2	V
R_L	Load impedance	BTL	Output filter: L = 10 uH, 1 µF. Output AD modulation, switching frequency > 350 kHz.	2.5	4		Ω
		SE		1.5	3		
		PBTL		1.5	2		
L_{OUTPUT}	Output filter inductance		Minimum inductance at overcurrent limit, including inductor tolerance, temperature and possible inductor saturation	5			µH
F_{PWM}	PWM frame rate			352	384	500	kHz
C_{PVDD}	PVDD close decoupling capacitors			0.44	1		µF
C_START	Start-up ramp capacitor		BTL and PBTL configuration		100		nF
			SE and 1 × BTL+ 2 × SE configuration		1		µF
R_{OC}	Overcurrent programming resistor		Resistor tolerance = 5%	24		33	kΩ
$R_{OC_LATCHED}$	Overcurrent programming resistor		Resistor tolerance = 5%	47	62	68	kΩ
T_J	Junction temperature			0		125	°C

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7.4 Thermal Information

THERMAL METRIC(1)		TAS5624A DDV (HTSSOP) 44 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	1.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	1.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	1.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

PVDD_X = 36 V, GVDD_X = 12 V, VDD = 12 V, T_C (case temperature) = 75°C, f_S = 384 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
DVDD	Voltage regulator, only used as a reference node	VDD = 12 V	3	3.3	3.6	V
AVDD	Voltage regulator, only used as a reference node	VDD = 12 V		7.8		V
I_{VDD}	VDD supply current	Operating, 50% duty cycle		20		mA
		Idle, reset mode		20		
I_{GVDD_X}	Gate-supply current per full-bridge	50% duty cycle		12		mA
		Reset mode		3		
I_{PVDD_X}	Full-bridge idle current	50% duty cycle without load		15		mA
		$\overline{\text{RESET}}$ low		1.9		
		VDD and GVDD_X at 0 V		0.4		
OUTPUT-STAGE MOSFETs						
$R_{DS(on),\ LS}$	Drain-to-source resistance, low-side (LS)	T_J = 25°C, excludes metallization resistance, GVDD = 12 V		40		mΩ
$R_{DS(on),\ HS}$	Drain-to-source resistance, high-side (HS)			40		mΩ
I/O PROTECTION						
$V_{uvp,GVDD}$	Undervoltage protection limit, GVDD_X			8.5		V
$V_{uvp,GVDD,\ hyst}$ (1)	Undervoltage protection limit, GVDD_X			0.7		V
$V_{uvp,VDD}$	Undervoltage protection limit, VDD			8.5		V
$V_{uvp,VDD,\ hyst}$ (1)	Undervoltage protection limit, VDD			0.7		V
$V_{uvp,PVDD}$	Undervoltage protection limit, PVDD_X			8.5		V
$V_{uvp,PVDD,hyst}$ (1)	Undervoltage protection limit, PVDD_X			0.7		V
OTW(1)	Overtemperature warning		115	125	135	°C
OTW_{hyst} (1)	Temperature drop needed below OTW temperature for $\overline{\text{OTW}}$ to be inactive after $\overline{\text{OTW}}$ event.			25		°C
OTE(1)	Overtemperature error		145	155	165	°C
$OTE\text{-}OTW_{differential}$ (1)	OTE-OTW differential			30		°C
OTE_{HYST} (1)	A device reset is needed to clear $\overline{\text{FAULT}}$ after an OTE event			25		°C
OLPC	Overload protection counter	f_{PWM} = 384 kHz		2.6		ms
I_{OC}	Overcurrent limit protection	Resistor-programmable, nominal peak current in 1-Ω load, ROC = 24 kΩ		15		A
$I_{OC_LATCHED}$	Overcurrent limit protection, latched	Resistor-programmable, nominal peak current in 1-Ω load, ROC = 62 kΩ		15		A
I_{OCT}	Overcurrent response time	Time from application of short condition to Hi-Z of affected half-bridge		150		ns
I_{PD}	Internal pulldown resistor at output of each half-bridge	Connected when $\overline{\text{RESET}}$ is active to provide bootstrap charge. Not used in SE mode.		3		mA

(1) Specified by design.

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Electrical Characteristics (continued)

PVDD_X = 36 V, GVDD_X = 12 V, VDD = 12 V, T_C (case temperature) = 75°C, f_S = 384 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High level input voltage	INPUT_X, M1, M2, M3, $\overline{RESET}$	1.9			V
V_{IL}	Low level input voltage				0.8	V
LEAKAGE	Input leakage current				100	µA
OTW / SHUTDOWN (FAULT)						
R_{INT_PU}	Internal pullup resistance, $\overline{OTW}$, $\overline{CLIP}$, $\overline{FAULT}$ to DVDD		20	26	33	kΩ
V_{OH}	High level output voltage	Internal pullup resistor	3	3.3	3.6	V
V_{OL}	Low level output voltage	I_O = 4 mA		200	500	mV
FANOUT	Device fanout $\overline{OTW}$, $\overline{FAULT}$, $\overline{CLIP}$	No external pullup		30		devices

7.6 Electrical Characteristics – Audio Specification Stereo (BTL)

Audio performance is recorded as a chipset consisting of a *TAS5558 8-Channel HD Compatible Audio Processor with ASRC and PWM Output* (SLES273), PWM Processor (modulation index limited to 97.7%) and a TAS5624A power stage with PCB and system configurations in accordance with recommended guidelines.

Audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 3 Ω, 10% THD+N		200		W
		R_L = 4 Ω, 10% THD+N		150		
		R_L = 3 Ω, 1% THD+N		160		
		R_L = 4 Ω, 1% THD+N		125		
THD+N	Total harmonic distortion + noise	1-W, 1-kHz signal		0.025%		
V_n	Output integrated noise	A-weighted, AES17 measuring filter		180		µV
V_{OS}	Output offset voltage	No signal		10	20	mV
SNR	Signal-to-noise ratio(1)	A-weighted, AES17 measuring filter		105		dB
DNR	Dynamic range	A-weighted, –60 dBFS (rel 1% THD+N)		105		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, channels switching(2)		1		W

(1) SNR is calculated relative to 1% THD-N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

7.7 Electrical Characteristics – Audio Specification 4 Channels (SE)

Audio performance is recorded as a chipset consisting of a TASxxxx, PWM Processor (modulation index limited to 97.7%) and a TAS5624A power stage with PCB and system configurations in accordance with recommended guidelines.

Audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12V, R_L = 4 Ω, f_S = 384 kHz, R = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, C_{DCB} = 470 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 3 Ω, 10% THD+N		50		W
		R_L = 3 Ω, 1% THD+N		42		
THD+N	Total harmonic distortion + noise	1-W, 1-kHz signal		0.025%		
V_n	Output integrated noise	A-weighted, AES17 measuring filter		180		µV
SNR	Signal-to-noise ratio(1)	A-weighted, AES17 measuring filter		102		dB
DNR	Dynamic range	A-weighted, –60 dBFS (rel 1% THD+N)		102		dB
P_{idle}	Power dissipation due to Idle losses (IPVDD_X)	P_O = 0, channels switching(2)		1		W

(1) SNR is calculated relative to 1% THD-N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

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7.8 Electrical Characteristics – Audio Specification Mono (PBTL)

Audio performance is recorded as a chipset consisting of a TASxxxx, PWM Processor (modulation index limited to 97.7%) and a TAS5624A power stage with PCB and system configurations in accordance with recommended guidelines.
Audio frequency = 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, unless otherwise noted.

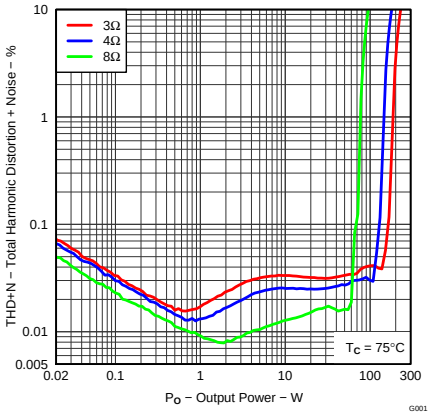
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 1.5 Ω, 10%, THD+N		400		W
		R_L = 2 Ω, 10% THD+N		300		
		R_L = 4 Ω, 10% THD+N		160		
		R_L = 1.5 Ω, 1% THD+N		320		
		R_L = 2 Ω, 1% THD+N		250		
		R_L = 4 Ω, 1% THD+N		130		
THD+N	Total harmonic distortion + noise	1-W, 1-kHz signal		0.025%		
V_n	Output integrated noise	A-weighted, AES17 measuring filter		180		µV
V_{OS}	Output offset voltage	No signal		10	20	mV
SNR	Signal-to-noise ratio(1)	A-weighted, AES17 measuring filter		105		dB
DNR	Dynamic range	A-weighted, –60 dBFS (rel 1% THD)		105		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, All channels switching(2)		1		W

(1) SNR is calculated relative to 1% THD-N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

7.9 Typical Characteristics

7.9.1 BTL Configuration

Measurement conditions are: 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, 20-Hz to 20-kHz BW (AES17 lowpass filter), unless otherwise noted.



1 kHz

Figure 1. Total Harmonic + Noise vs Output Power

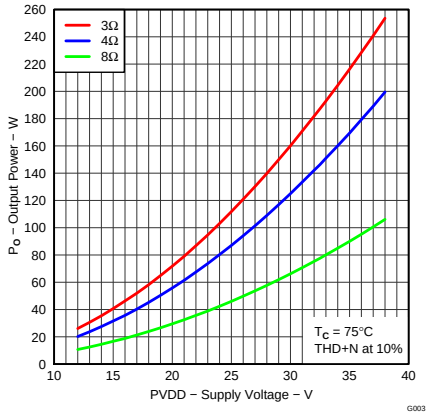
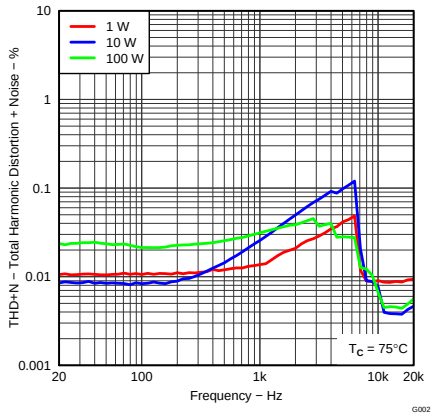


Figure 2. Output Power vs Supply Voltage vs Distortion + Noise = 10%

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BTL Configuration (continued)

Measurement conditions are: 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, 20-Hz to 20-kHz BW (AES17 lowpass filter), unless otherwise noted.



4 Ω

Figure 3. Total Harmonic Distortion + Noise vs Frequency

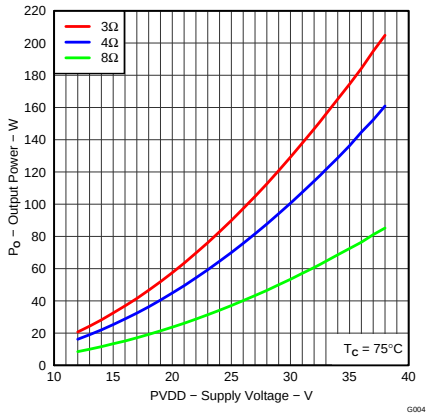


Figure 4. Output Power vs Supply Voltage, Distortion + Noise = 1%

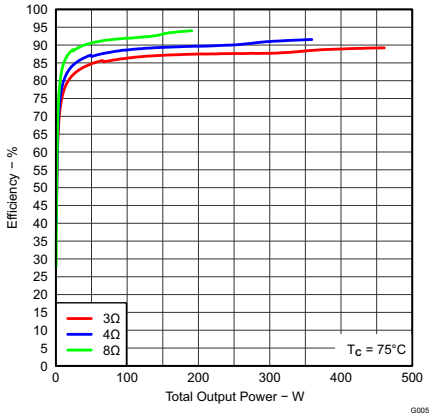


Figure 5. System Efficiency vs Output Power

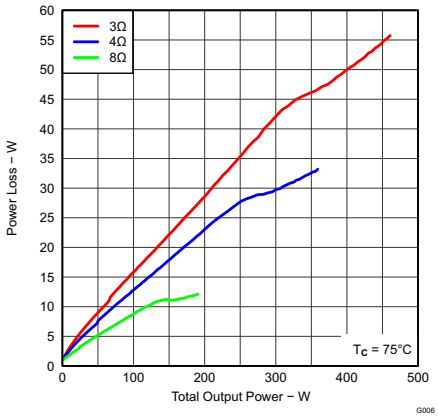


Figure 6. System Power Loss vs Output Power

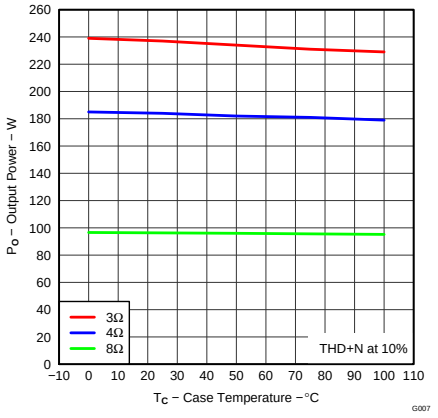


Figure 7. Output Power vs Temperature

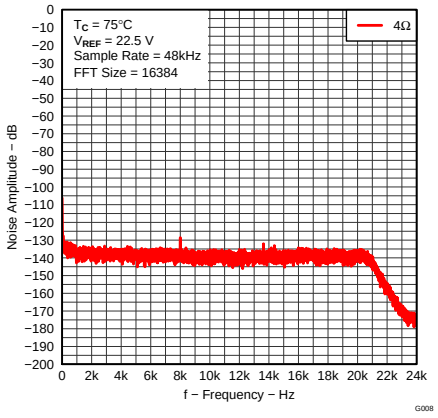


Figure 8. Noise Amplitude vs Frequency

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7.9.2 SE Configuration

Measurement conditions are: 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, C_{DCB} = 470 µF, 20-Hz to 20-kHz BW (AES17 lowpass filter), unless otherwise noted.

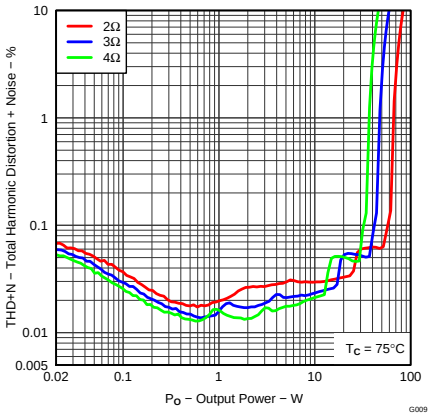


Figure 9. Total Harmonic Distortion + Noise vs Output Power

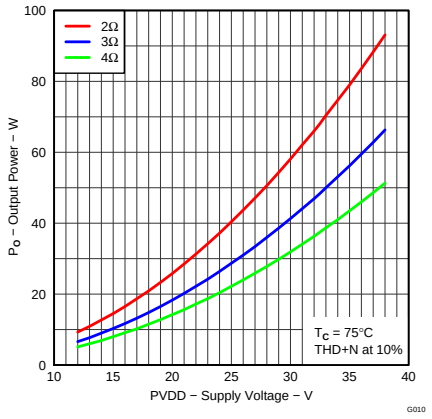


Figure 10. Output Power vs Supply Voltage

7.9.3 PBTL Configuration

Measurement conditions are: 1 kHz, PVDD_X = 36 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, 20-Hz to 20-kHz BW (AES17 lowpass filter), unless otherwise noted.

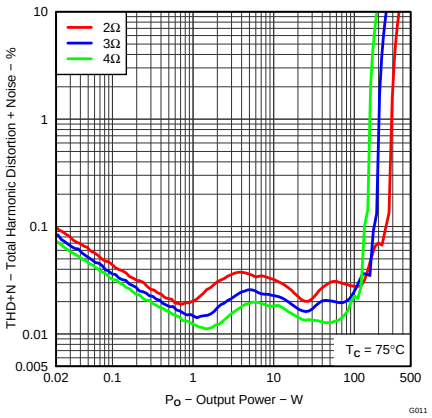


Figure 11. Total Harmonic Distortion + Noise vs Output Power

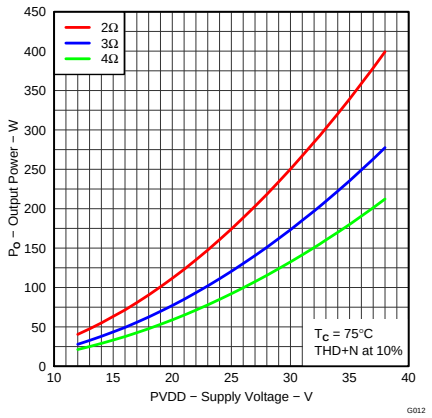


Figure 12. Output Power vs Supply Voltage

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8 Parameter Measurement Information

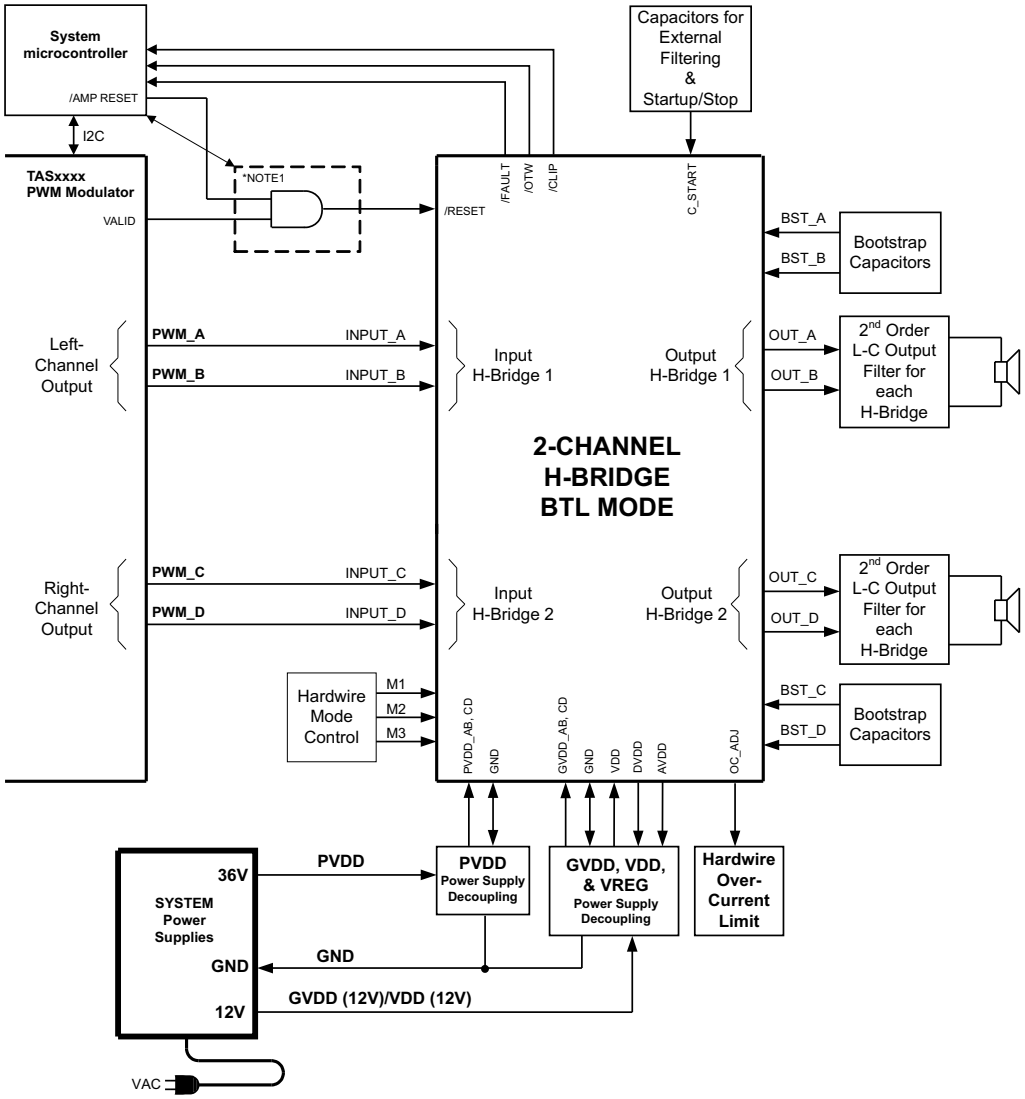
All parameters are measured according to the conditions described in the *Specifications* section.

9 Detailed Description

9.1 Overview

TAS5624A is a PWM input, audio PWM (class-D) amplifier. the output of the TAS5624A can be configured for single-ended, bridge-tied load (BTL) or parallel BTL (PBTL) output. It requires two railes for power supply, PVDD and 12 V (GVDD and VDD). Figure 13 shows typical connections for BTL outputs. A detailed schematic can be viewed in *TAS5624A EVM User's Guide* (SLAU376).

9.2 Functional Block Diagrams



(1) Logic AND is inside or outside the microprocessor

Figure 13. Typical System Block Diagram

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Functional Block Diagrams (continued)

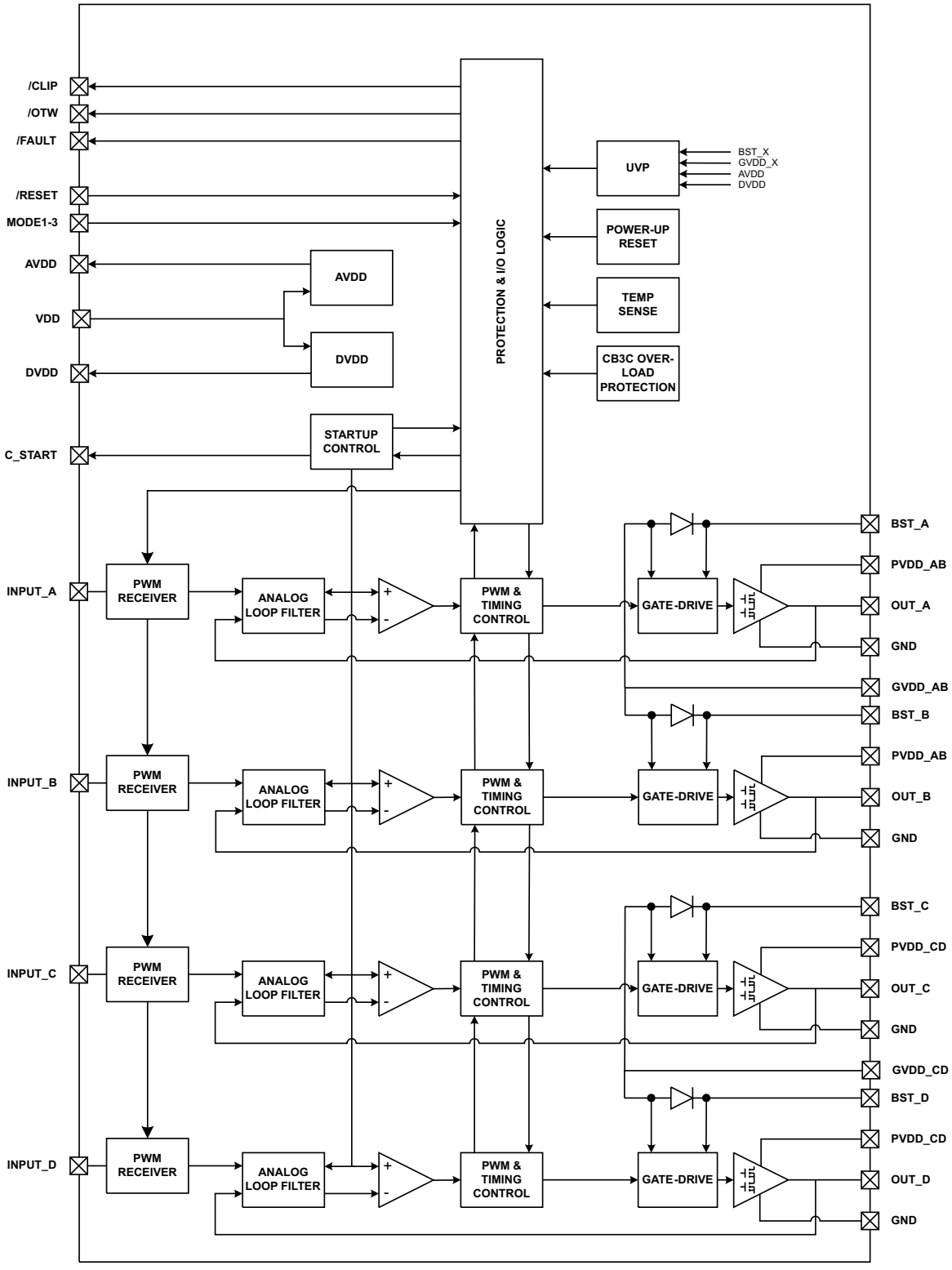


Figure 14. Functional Block Diagram

9.3 Feature Description

9.3.1 System Power-Up and Power-Down Sequence

9.3.1.1 Powering Up

The TAS5624A does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* table of this data sheet). Although not specifically required, TI recommends to hold RESET in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

9.3.1.2 Powering Down

The TAS5624A does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* table of this data sheet). Although not specifically required, it is a good practice to hold RESET low during power down, thus preventing audible artifacts including pops or clicks.

9.3.2 Start-Up and Shutdown Ramp Sequence

The integrated start-up and stop sequence ensures a click-free and pop-free start-up and shutdown sequence of the amplifier. The start-up sequence uses a voltage ramp with a duration set by the CSTART capacitor. The sequence uses the input PWM signals to generate output PWM signals, hence input idle PWM must be present during both start-up and shutdown ramping sequences.

VDD, GVDD_X and PVDD_X power supplies must be turned on and with settled outputs before starting the start-up ramp by setting RESET high.

During start-up and shutdown ramp, the input PWM signals must be in muted condition with the PWM processor noise shaper activity turned off (50% duty cycle).

The duration of the start-up and shutdown ramp is 100 ms + X ms, where X is the CSTART capacitor value in nF.

TI recommends using a 100-nF CSTART in BTL and PBTL mode and 1 µF in SE mode configuration. This results in ramp times of 200 ms and 1.1 s respectively. The longer ramp time in SE configuration allows charge and discharge of the output AC-coupling capacitor without audible artifacts.

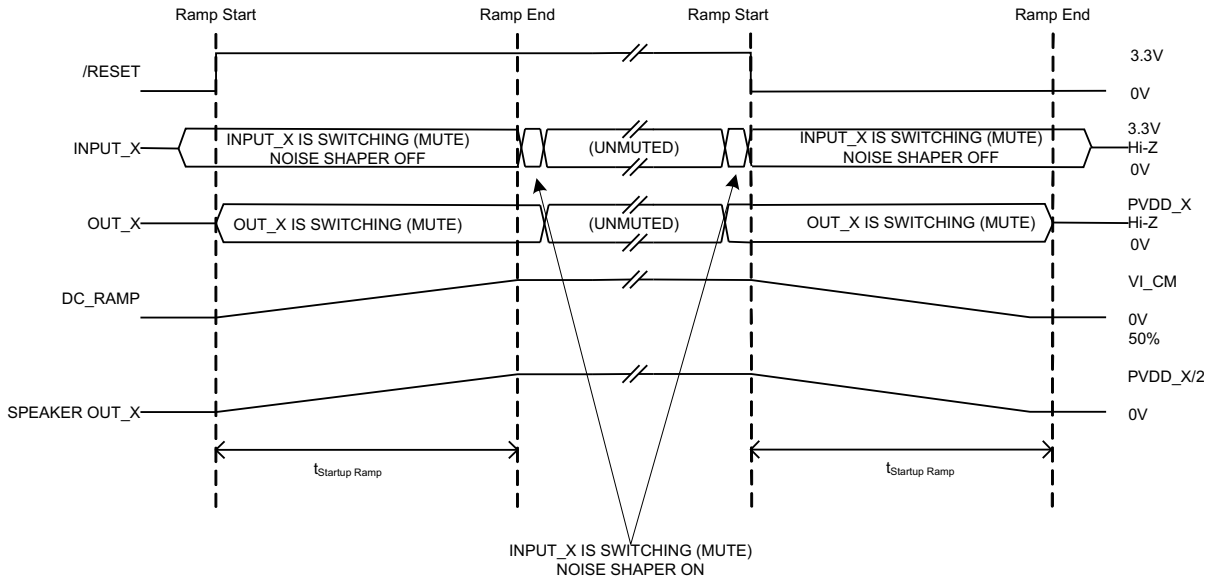


Figure 15. Start-Up and Shutdown Ramp

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Feature Description (continued)

9.3.3 Unused Output Channels

If all available output channels are not used, TI recommends disabling of unused output nodes to reduce power consumption. Furthermore by disabling unused output channels the cost of unused output LC demodulation filters can be avoided.

Disabling a channel is done by leave the bootstrap capacitor (BST) unstuffed and connecting the respective input to GND. The unused output pins can be left floating.

NOTE

The PVDD decoupling capacitors must still be mounted.

Table 1. Unused Output Channels

OPERATING MODE	PWM INPUT	OUTPUT CONFIGURATION	UNUSED CHANNEL	INPUT_A	INPUT_B	INPUT_C	INPUT_D	UNSTUFFED COMPONENT
000	2N + 1	2 × BTL	AB CD	GND PWMa	GND PWMb	PWMc GND	PWMd GND	BST_A & BST_B capacitor BST_C & BST_D capacitor
001	1N + 1							
010	2N + 1							
101	1N + 1	4 × SE	A	GND	PWMb	PWMc	PWMd	BST_A capacitor
			B	PWMa	GND	PWMc	PWMd	BST_B capacitor
			C	PWMa	PWMb	GND	PWMd	BST_C capacitor
			D	PWMa	PWMb	PWMc	GND	BST_D capacitor

9.3.4 Device Protection System

The TAS5624A contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5624A responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the $\overline{\text{FAULT}}$ pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, that is, the supply voltage has increased.

The device will function on errors, as shown in Table 2.

Table 2. Device Protection

BTL MODE		PBTL MODE		SE MODE	
CHANNEL FAULT	TURNS OFF	CHANNEL FAULT	TURNS OFF	CHANNEL FAULT	TURNS OFF
A	A + B	A	A + B + C + D	A	A + B
B		B		B	
C	C + D	C		C	C + D
D		D		D	

Bootstrap UVP does not shutdown according to the table, it shuts down the respective high-side FET.

9.3.5 Pin-to-Pin Short-Circuit Protection (PPSC)

The PPSC detection system protects the device from permanent damage if a power output pin (OUT_X) is shorted to GND or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at start-up, for example, when VDD is supplied, consequently a short to either GND or PVDD_X after system start-up does not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half-bridges are kept in a Hi-Z state until the short is removed, the device then continues the start-up sequence and starts switching. The detection is controlled globally by a two-step sequence. The first step ensures that there are no shorts from OUT_X to GND, the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The

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typical duration is < 15 ms/µF. While the PPSC detection is in progress, $\overline{\text{FAULT}}$ is kept low, and the device will not react to changes applied to the $\overline{\text{RESET}}$ pins. If no shorts are present the PPSC detection passes, and $\overline{\text{FAULT}}$ is released. A device reset will not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations, the detection is not performed in SE mode. To make sure not to trip the PPSC detection system, TI recommends not to insert resistive load to GND or PVDD_X.

9.3.6 Overtemperature Protection

The TAS5624A has a two-level, temperature-protection system that asserts an active-low warning signal ($\overline{\text{OTW}}$) when the device junction temperature exceeds 125°C (typical). If the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{\text{RESET}}$ must be asserted. Thereafter, the device resumes normal operation.

9.3.7 Overtemperature Warning, $\overline{\text{OTW}}$

The overtemperature warning $\overline{\text{OTW}}$ asserts when the junction temperature has exceeded recommended operating temperature. Operation at junction temperatures above $\overline{\text{OTW}}$ threshold is exceeding recommended operation conditions and is strongly advised to avoid.

If $\overline{\text{OTW}}$ asserts, take action to reduce power dissipation to allow junction temperature to decrease until it gets below the $\overline{\text{OTW}}$ hysteresis threshold. This action can be decreasing audio volume or turning on a system cooling fan.

9.3.8 Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5624A fully protect the device in any power-up, power-down, or brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach stated in the *Electrical Characteristics* table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

9.3.9 Error Reporting

NOTE

Asserting $\overline{\text{RESET}}$ low forces the $\overline{\text{FAULT}}$ signal high, independent of faults being present.

TI recommends monitoring the $\overline{\text{OTW}}$ signal using the system microcontroller and responding to an overtemperature warning signal by, for example, turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on $\overline{\text{FAULT}}$, $\overline{\text{CLIP}}$, and $\overline{\text{OTW}}$ outputs. See *Electrical Characteristics* table for actual values.

The $\overline{\text{FAULT}}$ and $\overline{\text{OTW}}$ pins are active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{\text{FAULT}}$ pin going low. Likewise, $\overline{\text{OTW}}$ goes low when the device junction temperature exceeds 125°C (see Table 3).

Table 3. Error Reporting

$\overline{\text{FAULT}}$	$\overline{\text{OTW}}$	DESCRIPTION
0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP)
0	1	Overload (OLP) or undervoltage (UVP)
1	0	Junction temperature higher than 125°C (overtemperature warning)
1	1	Junction temperature lower than 125°C and no OLP or UVP faults (normal operation)

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9.3.10 Fault Handling

If a fault situation occurs while in operation, the device will act accordingly to the fault being a global or a channel fault. A global fault is a chip-wide fault situation and causes all PWM activity of the device to shut down, and will assert $\overline{\text{FAULT}}$ low. A global fault is a latching fault and clearing $\overline{\text{FAULT}}$ and restart operation requires resetting the device by toggling $\overline{\text{RESET}}$. Toggling $\overline{\text{RESET}}$ must never be allowed with excessive system temperature, so it is advised to monitor $\overline{\text{RESET}}$ by a system microcontroller and only allow releasing $\overline{\text{RESET}}$ ($\overline{\text{RESET}}$ high) if the $\overline{\text{OTW}}$ signal is cleared (high). A channel fault will result in shutdown of the PWM activity of the affected channels. Asserting $\overline{\text{RESET}}$ low forces the $\overline{\text{FAULT}}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{\text{OTW}}$ signal using the system microcontroller and responding to an overtemperature warning signal by, for example, turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

Table 4. Fault Handling

FAULT AND EVENT	FAULT AND EVENT DESCRIPTION	GLOBAL OR CHANNEL	REPORTING METHOD	LATCHED AND SELF CLEARING	ACTION NEEDED TO CLEAR	OUTPUT FETs
PVDD_X UVP	Voltage Fault	Global	$\overline{\text{FAULT}}$ Pin	Self-Clearing	Increase affected supply voltage	Hi-Z
VDD UVP						
GVDD_X UVP						
AVDD UVP						
POR (DVDD UVP)	Power On Reset	Global	$\overline{\text{FAULT}}$ Pin	Self-Clearing	Allow DVDD to rise	H-Z
BST UVP	Voltage Fault	Channel (half-bridge)	None	Self-Clearing	Allow BST cap to recharge (lowside on, VDD 12 V)	HighSide Off
OTW	Thermal Warning	Global	$\overline{\text{OTW}}$ Pin	Self-Clearing	Cool below lower OTW threshold	Normal operation
OTE (OTSD)	Thermal Shutdown	Global	$\overline{\text{FAULT}}$ Pin	Latched	Toggle $\overline{\text{RESET}}$	Hi-Z
OLP (CBC > 2.6ms)	OC shutdown	Channel	$\overline{\text{FAULT}}$ Pin	Latched	Toggle $\overline{\text{RESET}}$	Hi-Z
Latched OC (ROC > 47k)	OC shutdown	Channel	$\overline{\text{FAULT}}$ Pin	Latched	Toggle $\overline{\text{RESET}}$	Hi-Z
CBC (24k < ROC < 33k)	OC Limiting	Channel	None	Self-Clearing	Reduce signal level or remove short	Flip state, cycle by cycle at fs / 2
Stuck at Fault(1) (1 to 3 channels)	No PWM	Channel	None	Self-Clearing	Resume PWM	Hi-Z
Stuck at Fault(1) (All channels)	No PWM	Global	None	Self-Clearing	Resume PWM	Hi-Z

(1) Stuck at Fault occurs when input PWM drops below minimum PWM frame rate given in *Recommended Operating Conditions*.

9.3.11 Device Reset

When $\overline{\text{RESET}}$ is asserted low, all power-stage FETs in the four half-bridges are forced into a high-impedance (Hi-Z) state.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs. In the SE mode, the output is forced into a high impedance state when asserting the reset input low. Asserting reset input low removes any fault information to be signaled on the $\overline{\text{FAULT}}$ output, that is, $\overline{\text{FAULT}}$ is forced high. A rising-edge transition on reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of $\overline{\text{RESET}}$ must occur no sooner than 4 ms after the falling edge of $\overline{\text{FAULT}}$.

9.3.12 System Design Consideration

A rising-edge transition on $\overline{\text{RESET}}$ input allows the device to execute the start-up sequence and starts switching.

Apply audio only according to the timing information for start-up and shutdown sequence. That will start and stop the amplifier without audible artifacts in the output transducers.

The $\overline{\text{CLIP}}$ signal indicates that the output is approaching clipping (when output PWM starts skipping pulses due to loop filter saturation). The signal can be used to initiate an audio volume decrease or to adjust the power supply rail.

The device inverts the audio signal from input to output.

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The DVDD and AVDD pins are not recommended to be used as a voltage source for external circuitry.

9.4 Device Functional Modes

There are three main output modes that the user can configure the device as per application requirement. In addition, there are two PWM modulation modes, AD and BD. AD modulation can have single-ended (SE) or differential analog inputs. AD modulation can also be configured to have SE, BTL, BTL + SE, or PBTL outputs. BD modulation requires differential analog inputs. BD modulation can only be configured in BTL or PBTL mode.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device in several popular use cases. Each of these configurations can be realized using the evaluation modules (EVMs) for the device. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit the E2E Forum at www.e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

10.2 Typical Applications

10.2.1 Typical BTL Application

See Figure 16 for application schematic. In this application, differential PWM inputs are used with AD modulation from the PWM modulator (TAS5558). AD modulation scheme is defined as PWM(+) as opposite polarity from PWM(–).

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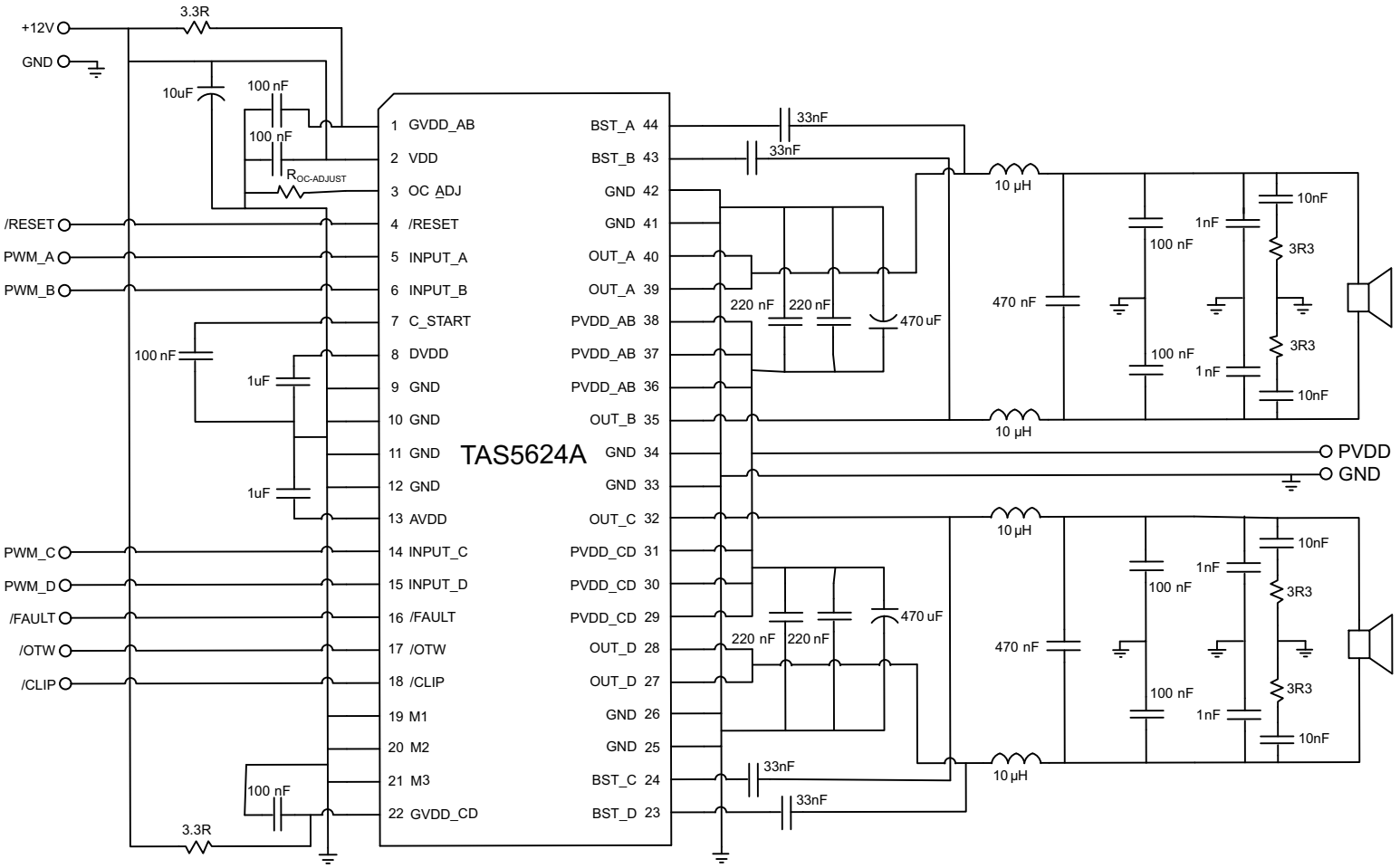


Figure 16. Typical Differential (2N) BTL Application With AD Modulation Filters

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10.2.1.1 Design Requirements

Table 5 lists the design parameters of Figure 16.

Table 5. Design Requirements

PARAMETER	VALUE
Digital regulator supply	12 V
Full-bridge power supply	12 V to 38 V
PWM modulator	TAS5558
Output filters	Inductor-capacitor lowpass filter
Speaker	2.5 Ω minimum

10.2.1.2 Detailed Design Procedure

Using Figure 16 as a guide, integrate the hardware into the system schematic.

Following the recommended component placement, schematic layout and routing given in *Layout Example*, integrate the device and its supporting components into the system PCB file.

- The most critical section of the circuit is the power supply inputs, the amplifier output signals, and the high-frequency signals which go to the serial audio port. TI recommends that these be constructed to ensure they are given precedent as design trade-offs are made.
- For questions and support go to the E2E Forum at www.e2e.ti.com. If it is necessary to deviate from the recommended layout, please visit the E2E Forum to request a layout review.

10.2.1.2.1 Pin Connections

- Pin 1 - GVDD_AB is the gate-drive voltage for half-bridges A and B. It needs a 3.3-Ω isolation resistor and a 0.1-µF decoupling capacitor.
- Pin 2 - VDD is the supply for internal voltage regulators AVDD and DVDD. It needs a 10-µF bulk capacitor and a 0.1-µF decoupling capacitor.
- Pin 3 - Roc adjust is the overcurrent programming resistor. Depending on the application, this resistor can be between 24 kΩ to 68 kΩ.
- Pin 4 - RESET pin when asserted, it keeps outputs Hi-Z and no PWM switching. This pin can be controlled by a microprocessor.
- Pins 5 and 6 - These are PWM(+) and PWM(–) pins with signals provided by a PWM modulator such as the TAS5558. These are PWM differential pairs.
- Pin 7 - Start-up ramp capacitor must be 1 µF for SE configuration.
- Pin 8 - Digital output supply pin is connected to 1-µF decoupling capacitor.
- Pins 9-12 - Ground pins are connected to board ground.
- Pin 13 - Analog output supply pin is connected to 1-µF decoupling capacitor.
- Pins 14 and 15 - These are PWM(+) and PWM(–) pins with signals provided by a PWM modulator such as the TAS5558. These are PWM differential pair.
- Pin 16 - Fault pin can be monitored by a microcontroller through GPIO pin. System can decide to assert reset or shutdown.
- Pin 17 - Overtemperature warning pin can be monitored by a microcontroller through a GPIO pin. System can decide to turn on fan or lower output power.
- Pin 18 - Output clip indicator can be monitored by a microcontroller through a GPIO pin. System can decide to lower the volume.
- Pins 19-21 - Mode pins set the input and output configurations. For this configuration M1-M3 are grounded. These mode pins must be hardware configured, such as, not through GPIO pins from a microcontroller.
- Pin 22 - GVDD_CD is the gate-drive voltage for half-bridges C and D. This pin needs a 3.3-Ω isolation resistor and a 0.1-µF decoupling capacitor.
- Pins 23, 24, 43, 44 - Bootstrap pins for half-bridges A, B, C, and D. Connect 33 nF from this pin to corresponding output pins.
- Pins 25, 26, 33, 34, 41, 42 - These ground pins must be used to ground decoupling capacitors from PVDD_X.
- Pins 27, 28, 32, 35, 39, 40 - Output pins from half-bridges A, B, C, and D. Connect appropriate bootstrap

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capacitors and differential LC filter as shown in Figure 20.

- Pins 29, 30, 31, 36, 37, 38 - Power supply pins to half-bridges A, B, C, and D. A and B form a full-bridge and C and D form another full-bridge. A 470-µF bulk capacitor is recommended for each full-bridge power pins. Two 0.22-µF decoupling capacitors are placed on each full-bridge power pins. See Figure 20 for details.

10.2.1.3 Application Curves

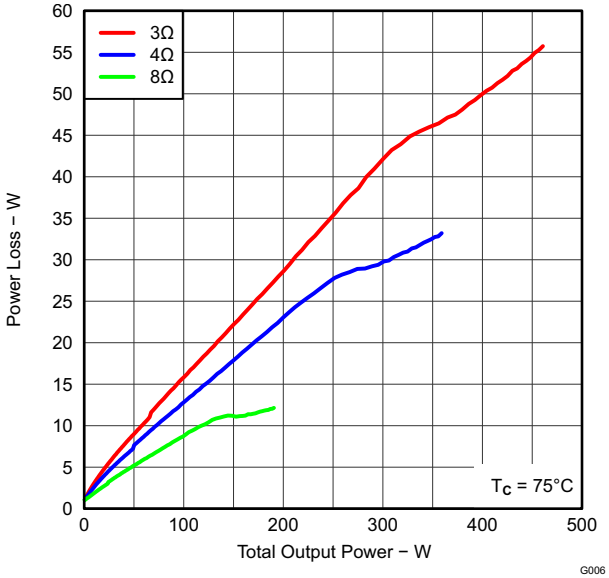


Figure 17. System Power Loss vs Output Power

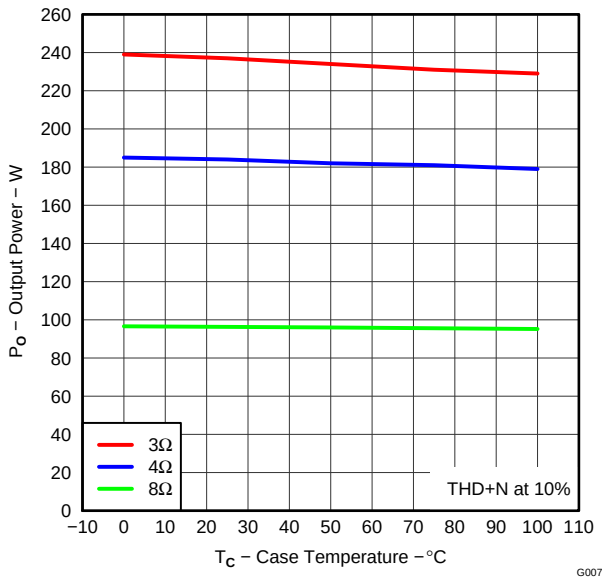


Figure 18. Output Power vs Temperature

10.2.2 Typical SE Configuration

See Figure 19 for application schematic. In this application, four single-ended PWM inputs are used with AD modulation from the PWM modulator such as the TAS5558. AD modulation scheme is defined as PWM(+) is opposite polarity from PWM(–). The single-ended (SE) output configuration is often used to drive four independent channels in one TAS5622A device.

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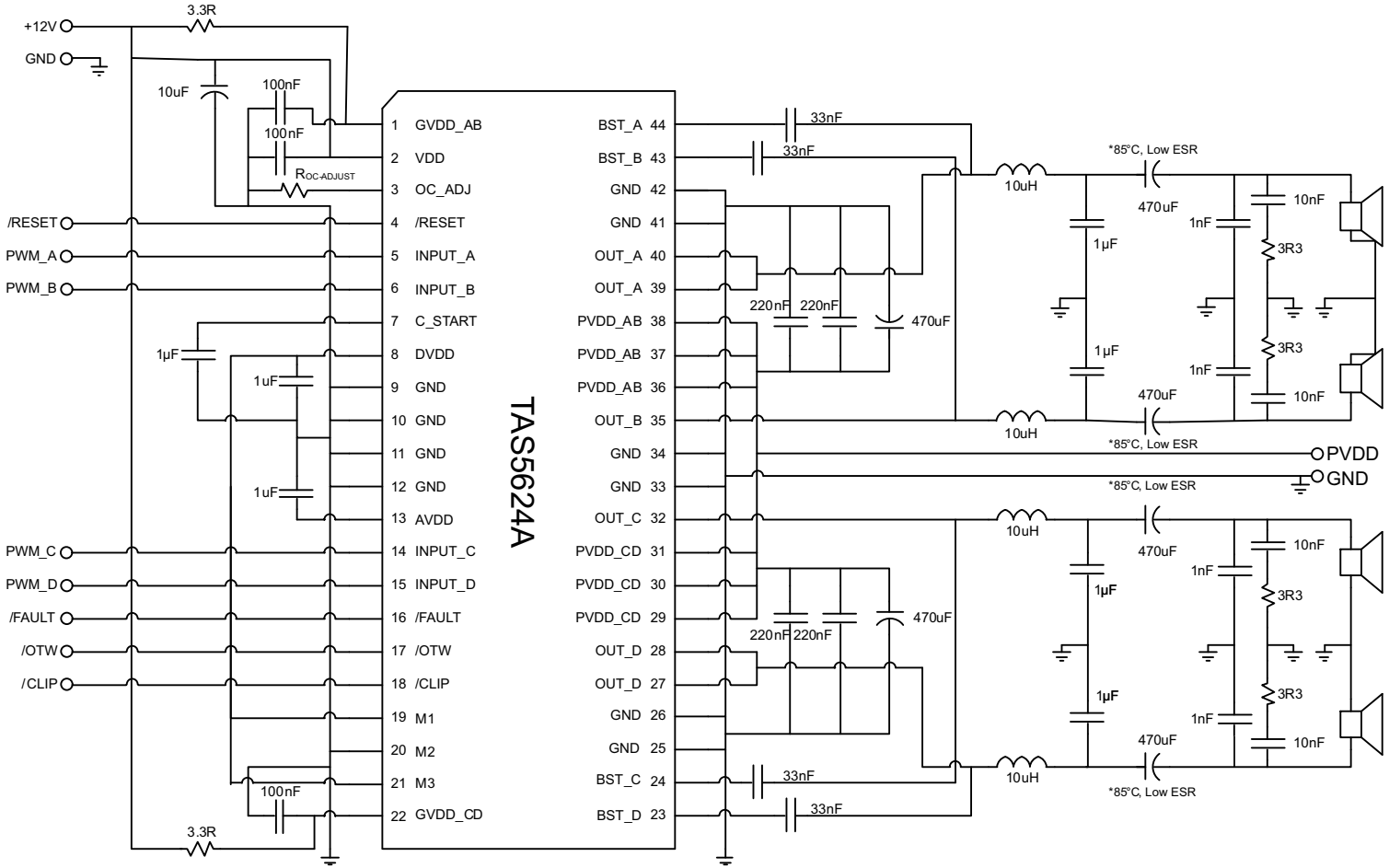


Figure 19. Typical (1N) SE Application

10.2.2.1 Design Requirements

Design Requirements lists the design parameters of Figure 19.

10.2.2.2 Detailed Design Procedure

Using Figure 16 as a guide, follow the design procedure in *Detailed Design Procedure*.

10.2.2.3 Application Curves

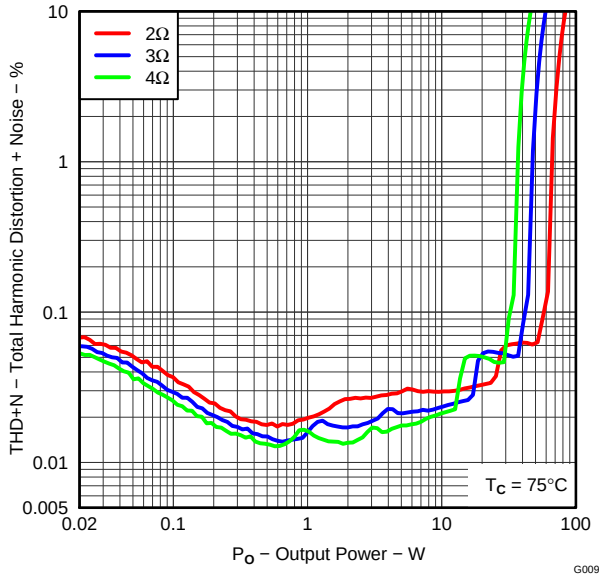


Figure 20. Total Harmonic Distortion + Noise vs Output Power

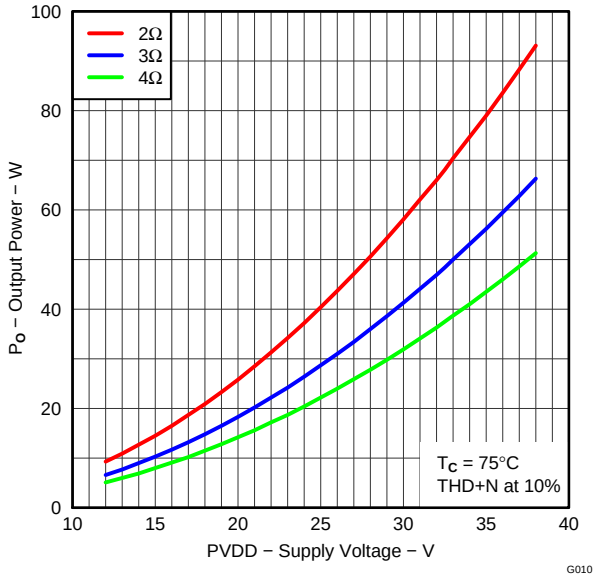


Figure 21. Output Power vs Supply Voltage

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10.2.3 Typical PBTL Configuration

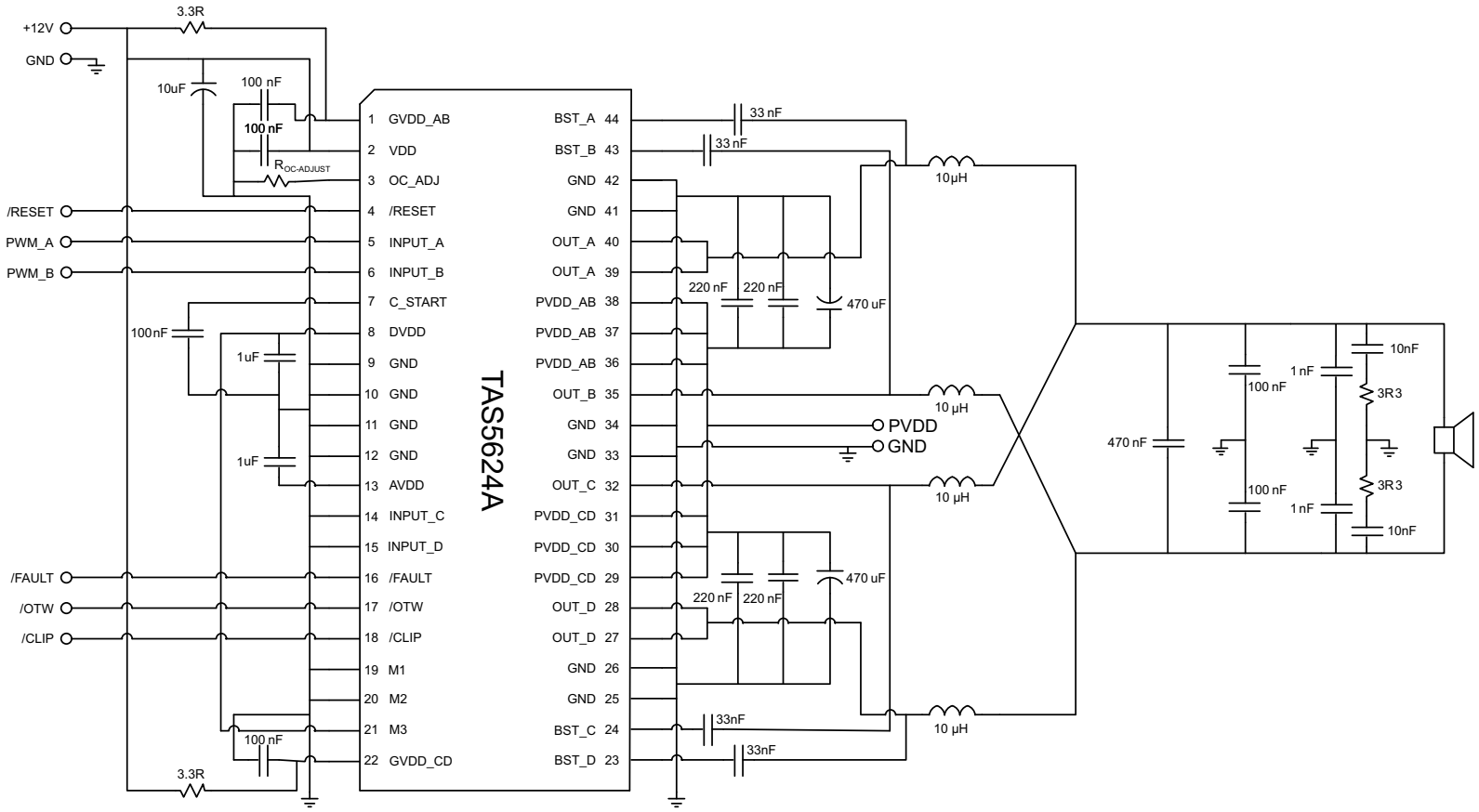


Figure 22. Typical Differential (2N) PBTL Application With AD Modulation Filter

10.2.3.1 Design Requirements

Design Requirements lists the design parameters of Figure 19.

10.2.3.2 Detailed Design Procedure

Using Figure 16 as a guide, follow the design procedure in *Detailed Design Procedure*.

10.2.3.3 Application Curves

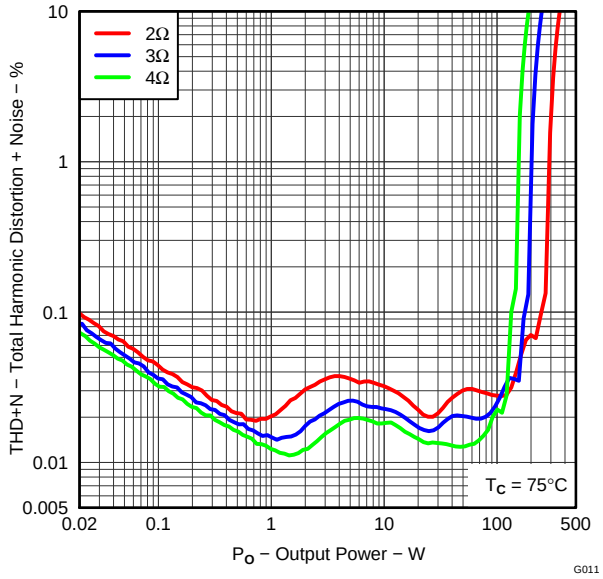


Figure 23. Total Harmonic Distortion + Noise vs Output Power

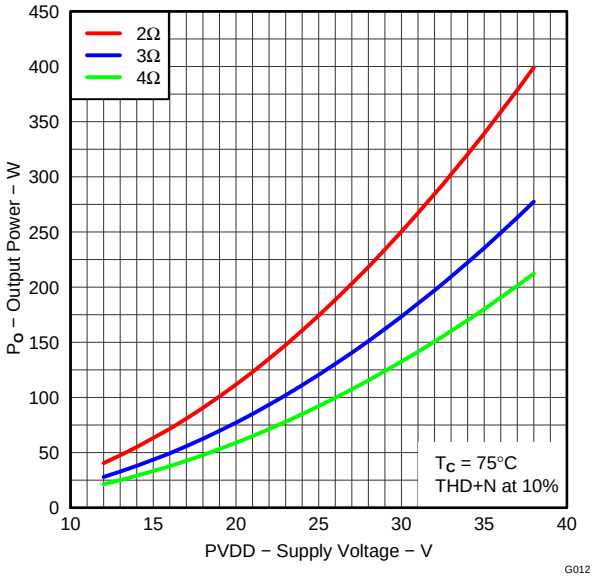


Figure 24. Output Power vs Supply Voltage

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11 Power Supply Recommendations

11.1 Power Supplies

To facilitate system design, the TAS5624A needs only a 12-V supply in addition to the (typical) 36-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, for example, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

To provide outstanding electrical and acoustical characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_X) and each full-bridge has separate power stage supply (PVDD_X) and gate supply (GVDD_X) pins. Furthermore, an additional pin (VDD) is provided as supply for all common circuits. Although supplied from the same 12-V source, TI highly recommends separating GVDD_AB, GVDD_CD, and VDD on the printed-circuit-board (PCB) by RC filters (see *Layout Example* for details). These RC filters provide the recommended high-frequency isolation. Pay special attention to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided.

Pay special attention to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each full-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X connection is decoupled with minimum 2x, 220-nF ceramic capacitors placed as close as possible to each supply pin. TI recommends following the PCB layout of the TAS5624A reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The 12-V supply must be from a low-noise, low-output-impedance voltage regulator. Likewise, the 36-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on reset circuit. Moreover, the TAS5624A is fully protected against erroneous power-stage turn on due to parasitic gate charging when power supplies are applied. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the *Recommended Operating Conditions* table of this data sheet).

11.2 Boot Strap Supply

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 300 kHz to 400 kHz, TI recommends using 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

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12 Layout

12.1 Layout Guidelines

12.1.1 PCB Material Recommendation

FR-4 Glass Epoxy material with 1-oz. (35-µm) is recommended for use with the TAS5624A. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance.

12.1.2 PVDD Capacitor Recommendation

The large capacitors used in conjunction with each full-bridge, are referred to as the PVDD Capacitors. These capacitors must be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well-designed system power supply, 1000-µF, 50-V capacitors support most applications. The PVDD capacitors must be low-ESR types because they are used in a circuit associated with high-speed switching.

12.1.3 Decoupling Capacitor Recommendation

To design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good-quality decoupling capacitors must be used. In practice, X5R or better must be used in this application.

The voltage of the decoupling capacitors must be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the close decoupling capacitor that is placed on the power supply to each half-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 50 V is required for use with a 36-V power supply.

See the *TAS5624A EVM User's Guide*, (SLAU376) for more details including bill of materials.

12.1.4 Circuit Component and Printed-Circuit-Board Recommendation

These requirements must be followed to achieve best performance and reliability and minimum ground bounce at rated output power of TAS5624A.

12.1.4.1 Circuit Component Requirements

A number of circuit components are critical to performance and reliability. They include LC filter inductors and capacitors, decoupling capacitors and the heat sink. The best detailed reference for these is the TAS5624A EVM BOM in the user's guide, which includes components that meet all the following requirements.

- High-frequency decoupling capacitors: small high-frequency decoupling capacitors are placed next to the IC to control switching spikes and keep high-frequency currents in a tight loop to achieve best performance and reliability and EMC. They must be high-quality ceramic parts with material like X7R or X5R and voltage ratings at least 30% greater than PVDD, to minimize loss of capacitance caused by applied DC voltage. (Capacitors made of materials like Y5V or Z5U must never be used in decoupling circuits or audio circuits because their capacitance falls dramatically with applied DC and AC voltage, often to 20% of rated value or less.)
- Bulk decoupling capacitors: large bulk decoupling capacitors are placed as close as possible to the IC to stabilize the power supply at lower frequencies. They must be high-quality aluminum parts with low ESR and ESL and voltage ratings at least 25% more than PVDD to handle power supply ripple currents and voltages.
- LC filter inductors: to maintain high efficiency, short-circuit protection, and low distortion, LC filter inductors must be linear to at least the OCP limit and must have low DC resistance and core losses. For SCP, minimum working inductance, including all variations of tolerance, temperature and current level, must be 5 µH. Inductance variation of more than 1% over the output current range can cause increased distortion.
- LC filter capacitors: to maintain low distortion and reliable operation, LC filter capacitors must be linear to twice the peak output voltage. For reliability, capacitors must be rated to handle the audio current generated in them by the maximum expected audio output voltage at the highest audio frequency.
- Heat sink: The heat sink must be fabricated with the PowerPAD contact area spaced 1.0 mm ±0.01 mm

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Layout Guidelines (continued)

above mounting areas that contact the PCB surface. It must be supported mechanically at each end of the IC. This mounting ensures the correct pressure to provide good mechanical, thermal and electrical contact with TAS5624A PowerPAD. The PowerPAD contact area must be bare and must be interfaced to the PowerPAD with a thin layer (about 1 mill) of a thermal compound with high thermal conductivity.

12.1.4.2 Printed-Circuit-Board Requirements

PCB layout, audio performance, EMC, and reliability are linked closely together, and solid grounding improves results in all these areas. The circuit produces high, fast-switching currents, and take care controlling current flow and minimizing voltage spikes and ground bounce at IC ground pins. Critical components must be placed for best performance and PCB traces must be sized for the high audio currents that the IC circuit produces.

Grounding: ground planes must be used to provide the lowest impedance and inductance for power and audio signal currents between the IC and its decoupling capacitors, LC filters and power supply connection. The area directly under the IC must be treated as central ground area for the device, and all IC grounds must be connected directly to that area. A matrix of vias must be used to connect that area to the ground plane. Ground planes can be interrupted by radial traces (traces pointing away from the IC), but they must never be interrupted by circular traces, which disconnect copper outside the circular trace from copper between it and the IC. Top and bottom areas that do not contain any power or signal traces must be flooded and connected with vias to the ground plane.

Decoupling capacitors: high-frequency decoupling capacitors must be located within 2 mm of the IC and connected directly to PVDD and GND pins with solid traces. Vias must not be used to complete these connections, but several vias must be used at each capacitor location to connect top ground directly to the ground plane. Placement of bulk decoupling capacitors is less critical, but they still must be placed as close as possible to the IC with strong ground return paths. Typically the heat sink sets the distance.

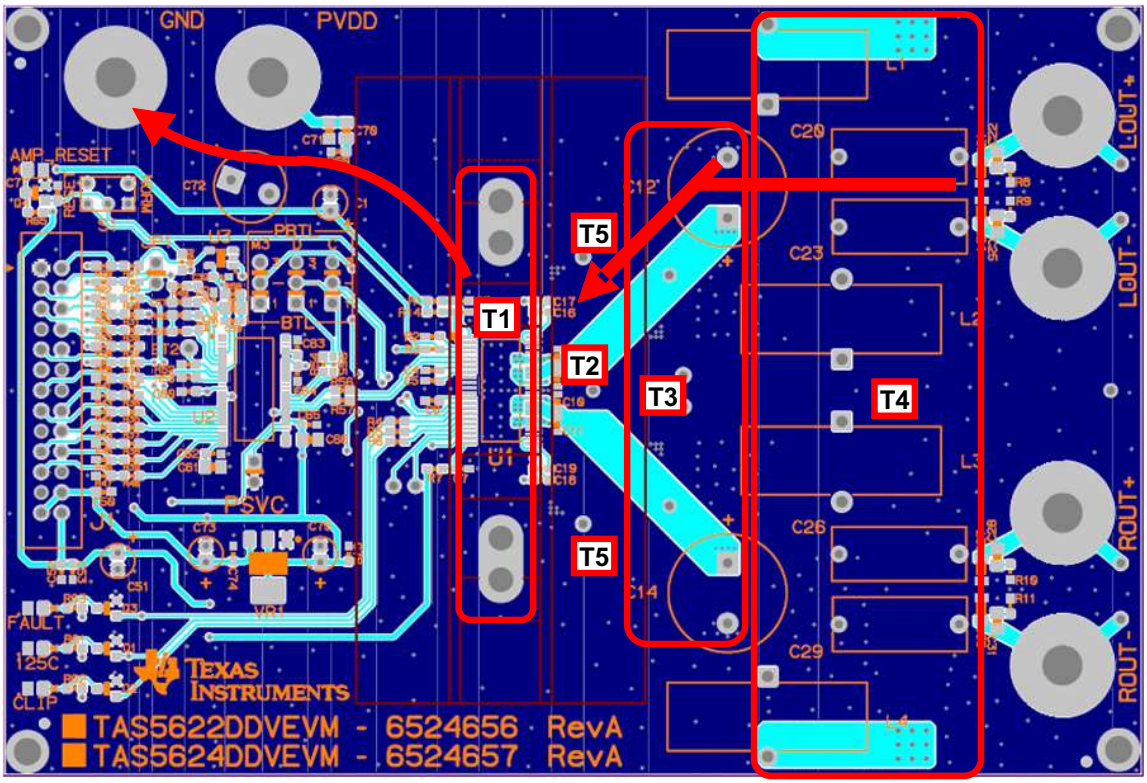
LC filters: LC filters must be placed as close as possible to the IC after the decoupling capacitors. The capacitors must have strong ground returns to the IC through top and bottom grounds for effective operation.

PCB copper must be at least 1-oz. thickness. PVDD and output traces must be wide enough to carry expected average currents without excessive temperature rise. PWM input traces must be kept short and close together on the input side of the IC and must be shielded with ground flood to avoid interference from high power switching signals.

The heat sink must be grounded well to the PCB near the IC, and a thin layer of highly conductive thermal compound (about 1 mill) must be used to connect the heat sink to the PowerPAD.

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12.2 Layout Example



Note T1: Bottom and top layer ground plane areas are used to provide strong ground connections. The area under the IC must be treated as central ground, with IC grounds connected there and a strong via matrix connecting the area to bottom ground plane. The ground path from the IC to the power supply ground through top and bottom layers must be strong to provide very low impedance to high power and audio currents.

Note T2: Low impedance X7R or X5R ceramic high frequency decoupling capacitors must be placed within 2mm of PVDD and GND pins and connected directly to them and to top ground plane to provide good decoupling of high frequency currents for best performance and reliability. Their DC voltage rating must be 2 times PVDD.

Note T3: Low impedance electrolytic bulk decoupling capacitors must be placed as close as possible to the IC. Typically the heat sink sets the distance. Wide PVDD traces are routed on the top layer with direct connections to the pins, without going through vias.

Note T4: LC filter inductors and capacitors must be placed as close as possible to the IC after decoupling capacitors. Inductors must have low DC resistance and switching losses and must be linear to at least the OCP (over current protection) limit. Capacitors must be linear to at least twice the maximum output voltage and must be capable of conducting currents generated by the maximum expected high frequency output.

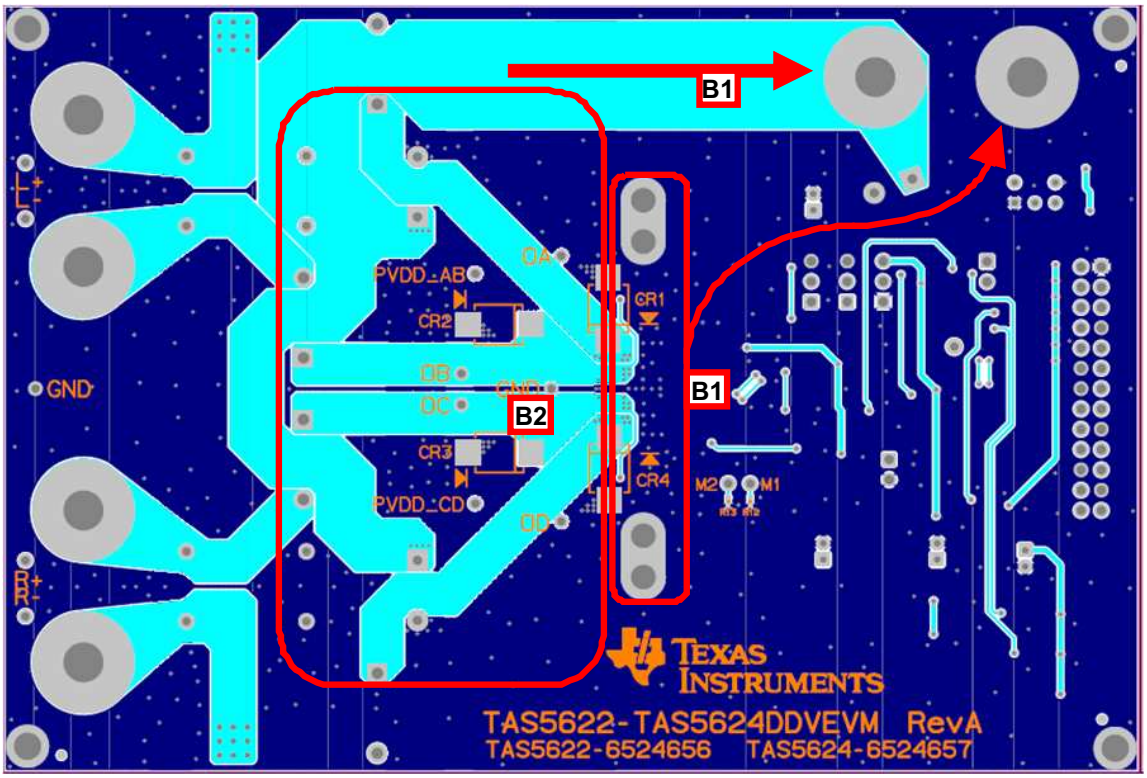
Note T5: Bulk decoupling capacitors and LC filter capacitors must have strong ground return paths through ground plane to the central ground area under the IC.

Note T6: The heat sink must have a good thermal and electrical connection to PCB ground and to the IC PowerPAD. It must be connected to the PowerPad through a thin layer, about 1 mil, of highly conductive thermal compound.

Figure 25. Printed-Circuit-Board - Top Layer

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Layout Example (continued)



Note B1: A wide PVDD bus and a wide ground path must be used to provide very low impedance to high power and audio currents to the power supply. Top and bottom ground planes must be connected with vias at many points to reinforce the ground connections.

Note B2: Wide output traces can be routed on the bottom layer and connected to output pins with strong via arrays.

Figure 26. Printed-Circuit-Board - Bottom Layer

13 器件和文档支持

13.1 器件支持

- *《具有 ASRC 和 PWM 输出的 8 通道 HD 可兼容音频处理器》*（文献编号：TAS5558）
- *《150W 立体声/300W 单声道 PurePath HD 数字输入 D 类功率级》*（文献编号：TAS5624A）

13.2 文档支持

13.2.1 相关文档

- *音频特性鉴定入门教程》*（文献编号：SLAA641）
- *《计算音频放大器增益》*（文献编号：SLOA105）
- *《TAS5558 具有 ASRC 和 PWM 输出的 8 通道 HD 可兼容音频处理器》*（文献编号：SLES273）
- *《TAS5624A EVM 用户指南》*（文献编号：SLAU376）

13.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 商标

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13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5624ADDV	Active	Production	HTSSOP (DDV) | 44	35 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5624A
TAS5624ADDV.A	Active	Production	HTSSOP (DDV) | 44	35 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5624A
TAS5624ADDV.B	Active	Production	HTSSOP (DDV) | 44	35 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5624A
TAS5624ADDVR	Active	Production	HTSSOP (DDV) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5624A
TAS5624ADDVR.A	Active	Production	HTSSOP (DDV) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5624A
TAS5624ADDVR.B	Active	Production	HTSSOP (DDV) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TAS5624A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

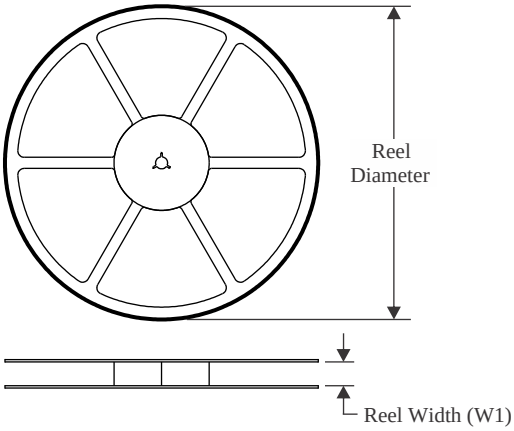
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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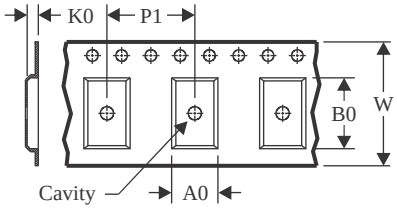
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

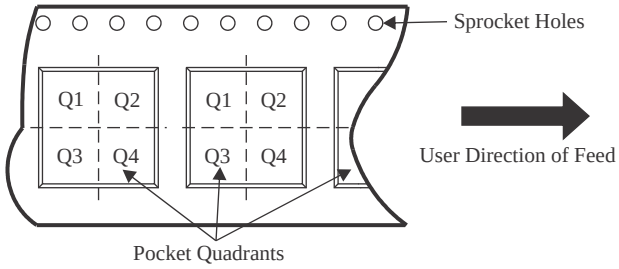


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

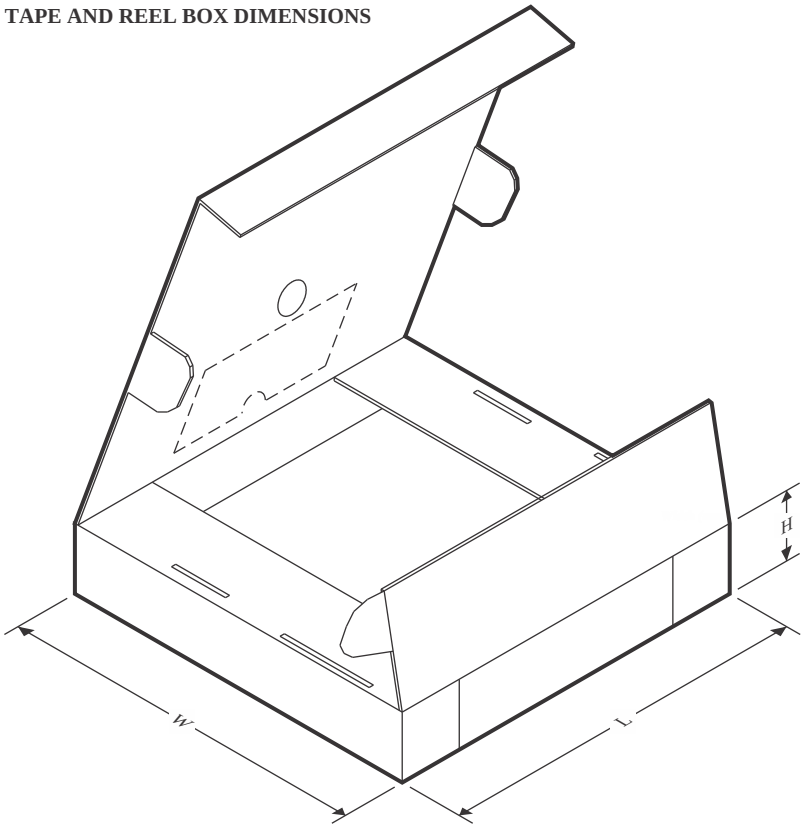
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5624ADDVR	HTSSOP	DDV	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

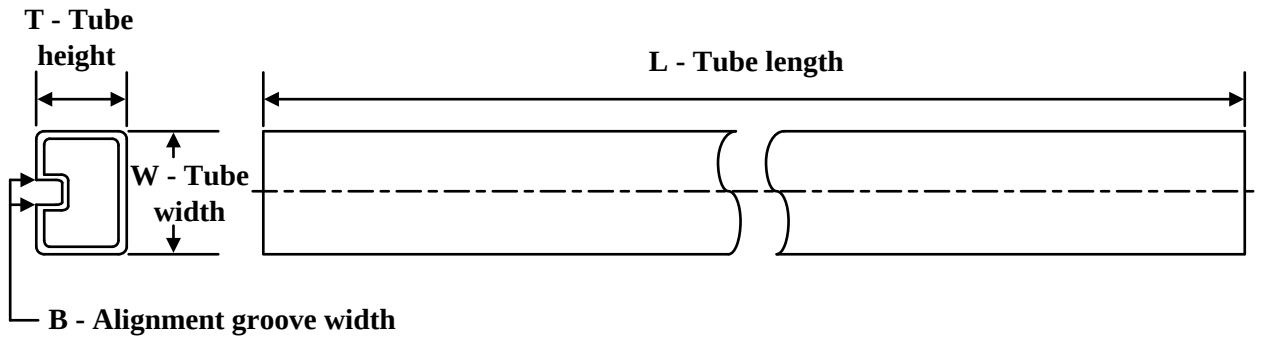
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5624ADDVR	HTSSOP	DDV	44	2000	350.0	350.0	43.0

TUBE

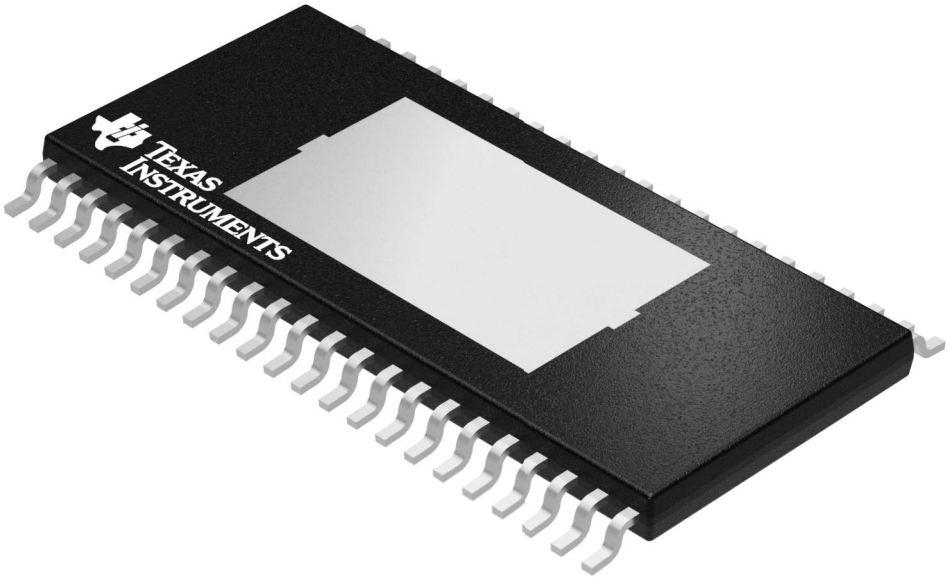


*All dimensions are nominal

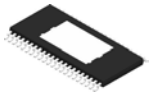
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TAS5624ADDV	DDV	HTSSOP	44	35	530	11.89	3600	4.9
TAS5624ADDV.A	DDV	HTSSOP	44	35	530	11.89	3600	4.9
TAS5624ADDV.B	DDV	HTSSOP	44	35	530	11.89	3600	4.9

DDV 44 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

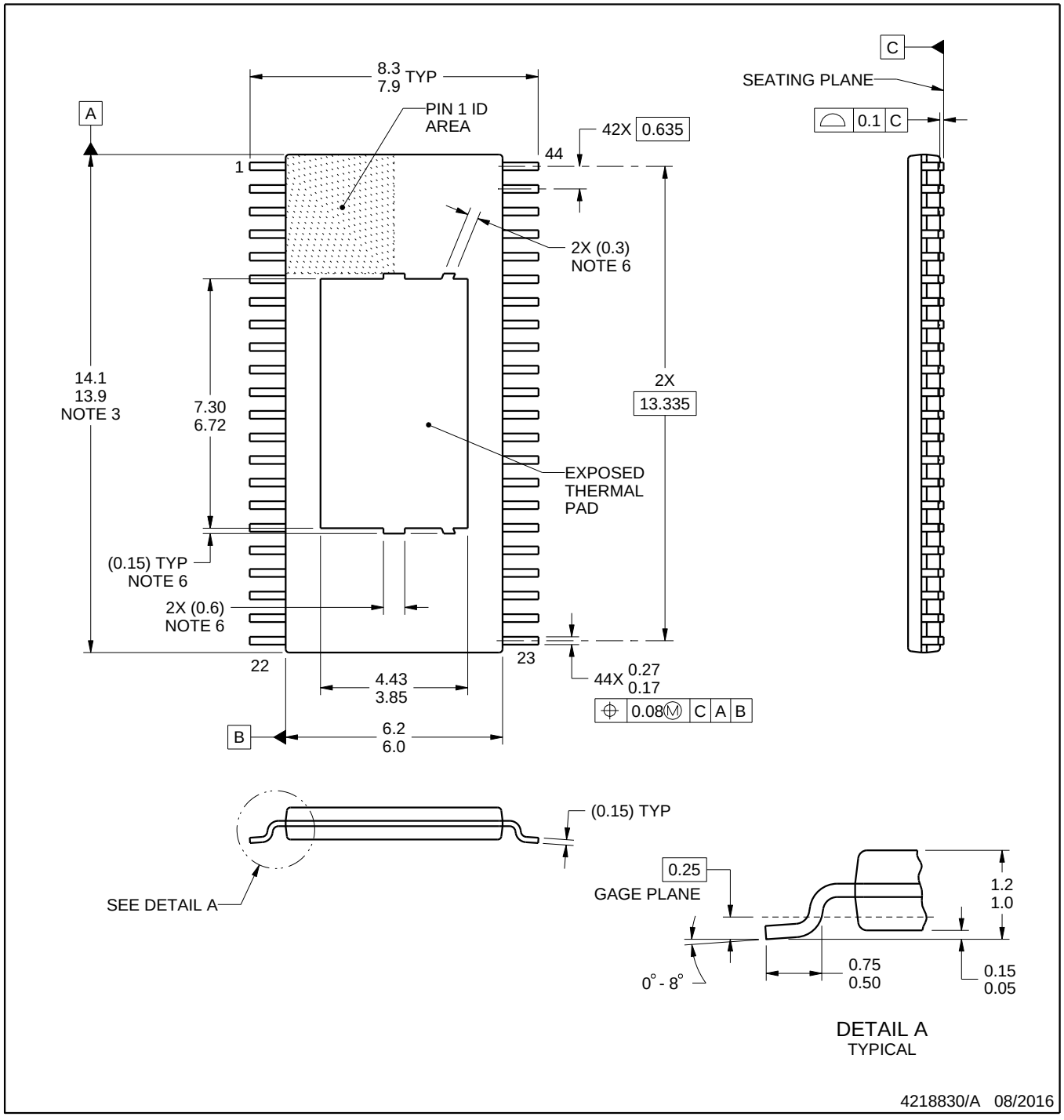


PACKAGE OUTLINE

DDV0044D

PowerPAD™ TSSOP - 1.2 mm max height

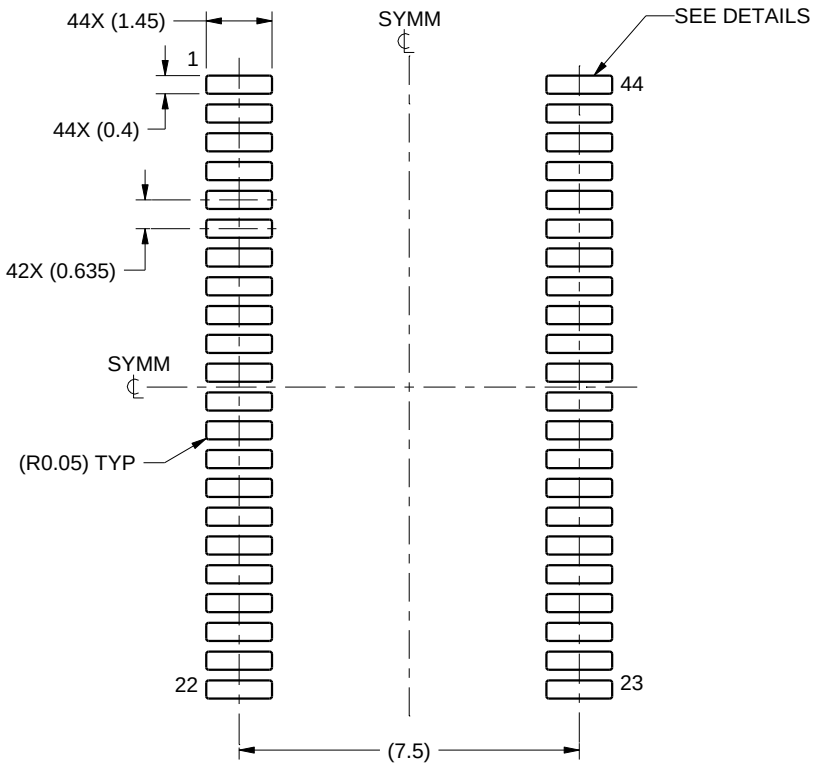
PLASTIC SMALL OUTLINE



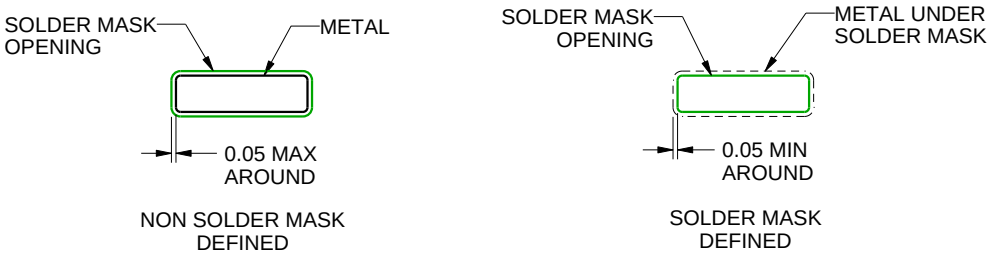
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:6X

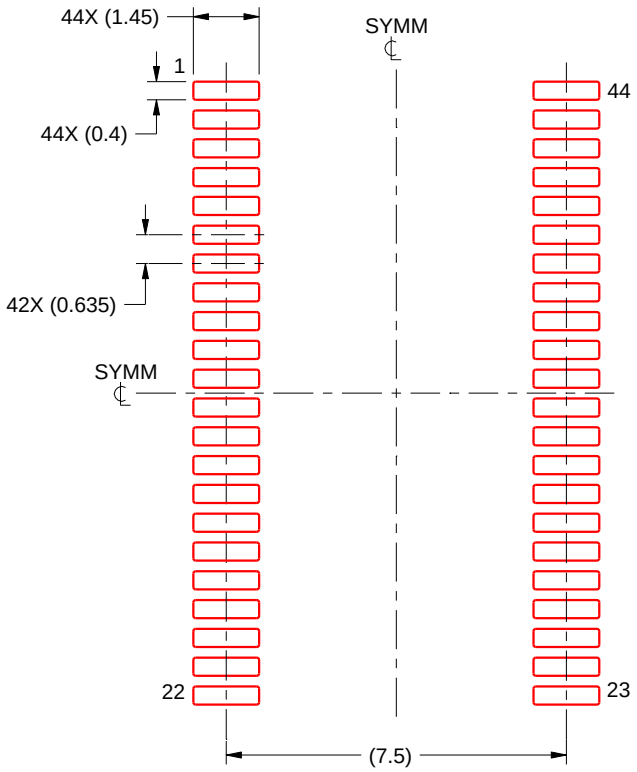


SOLDER MASK DETAILS
NOT TO SCALE

4218830/A 08/2016

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE :6X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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