20-W STEREO DIGITAL AUDIO POWER AMPLIFIER

Check for Samples: TAS5701

FEATURES

- **Audio Input/Output**
  - **20-W Into an 8-Ω Load From an 18-V Supply**
  - **Wide PVDD Range (0 V to 21 V)**
  - **Efficient Class-D Operation Eliminates Need for Heat Sinks**
  - **Two Serial Audio Inputs (3 Audio channels)**
  - **Supports 32-kHz to 192-kHz Sample Rates (LJ/RJ/I^2S)**
  - **Line-Level Subwoofer PWM Outputs**
- **Audio/PWM Processing**
  - **BD (Filter-free) Modulation Supporting Bridge-Tied Loads ONLY**
  - **4-Step Volume Control (0 dB, 6 dB, 12 dB, 18 dB)**
    - **All Channels Share Same Control**
  - **Soft Mute (50% Duty Cycle)**
  - **DC Blocking Filters**
  - **Fixed Maximum Modulation Limit At 97.7%**
  - **≥100-dB SNR – Measured at Maximum Output With THD+N = 1%, 1 kHz, A-Weighted Noise, Gain = 0 dB**
  - **THD < 0.1% at 1/2 Rated Power**
- **General Features**
  - **5-V Tolerant Inputs (See pin list for details on which inputs are 5-V tolerant)**
  - **Shutdown Mode for Low Power Consumption**
  - **Thermal and Short-Circuit Protection**
  - **Autodetect: Automatically Detect Sample-Rate Changes – No Need for External Microprocessor Intervention**

DESCRIPTION

The TAS5701 is a 20-W efficient, digital audio power amplifier for driving stereo bridge-tied speakers. Two serial data inputs support up to 3 discrete audio channels. The SDIN1 input is routed to the internal left and right outputs. The SDIN2 input is dedicated to the SUB_PWM± outputs.

The TAS5701 is a clock slave-only device receiving clocks from external sources. The TAS5701 operates at a 384-kHz switching rate for 32-, 48-, 96-, and 192-kHz data and 352.8-kHz switching rate 44.1-,88.2-, and 176.4-kHz data. The 8× oversampling combined with the fourth-order noise shaper provides a flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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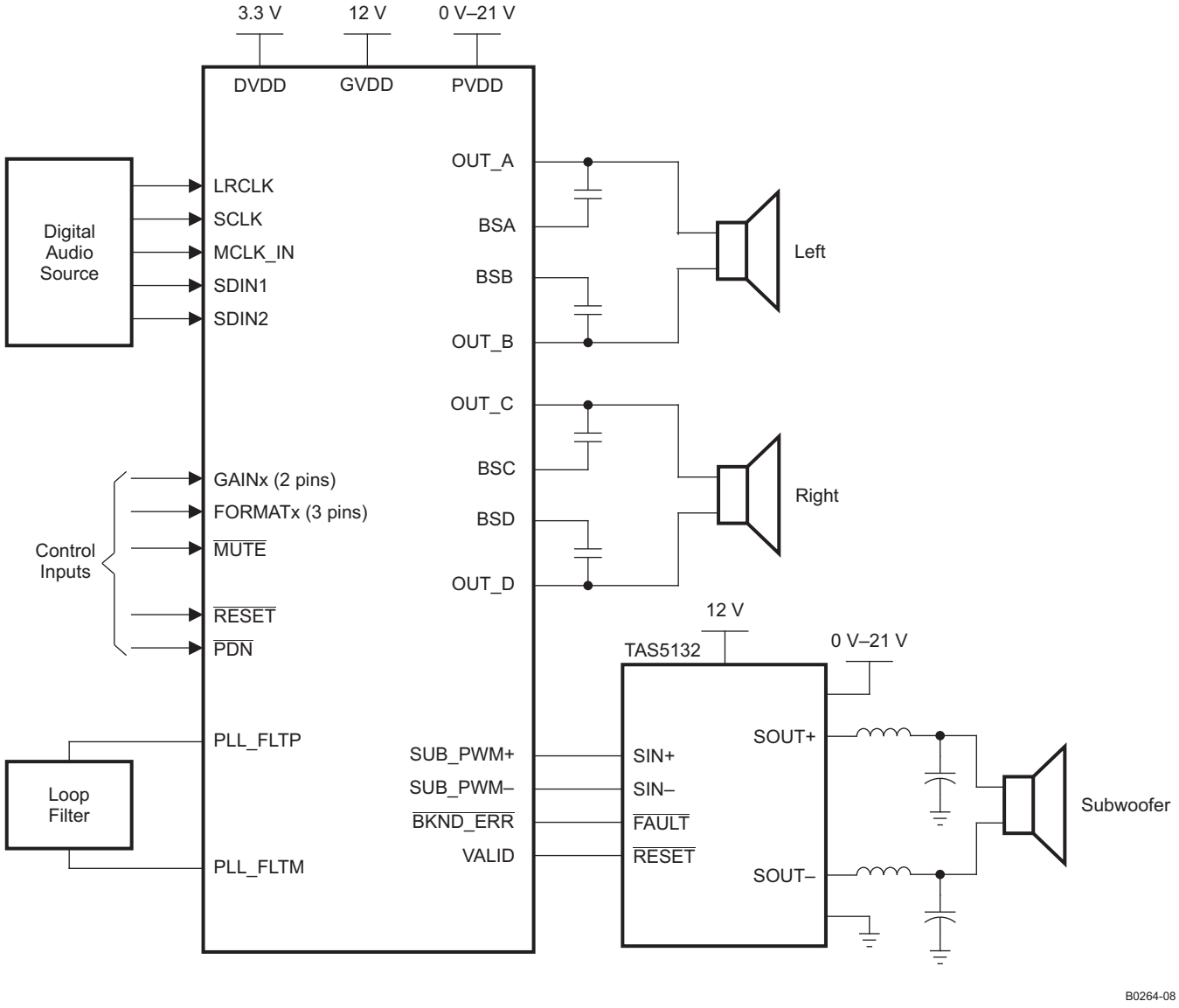
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SIMPLIFIED APPLICATION DIAGRAM



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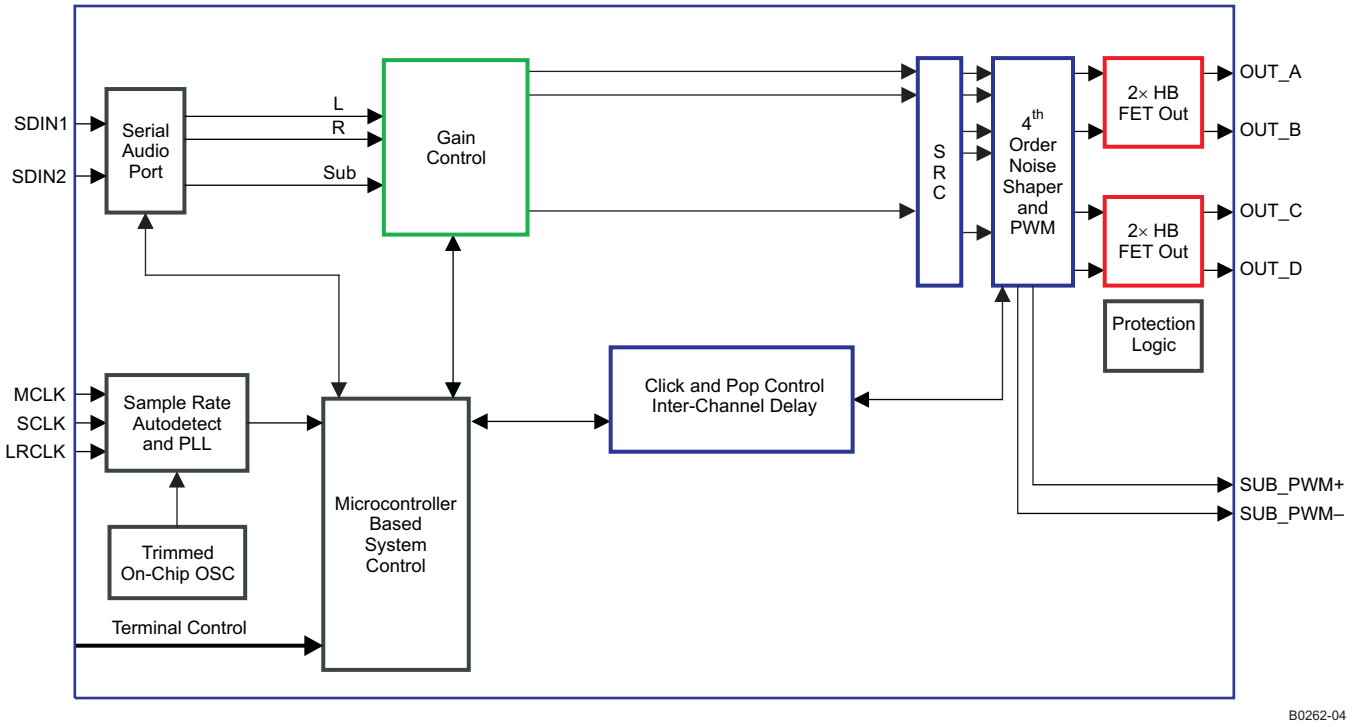
FUNCTIONAL BLOCK DIAGRAM



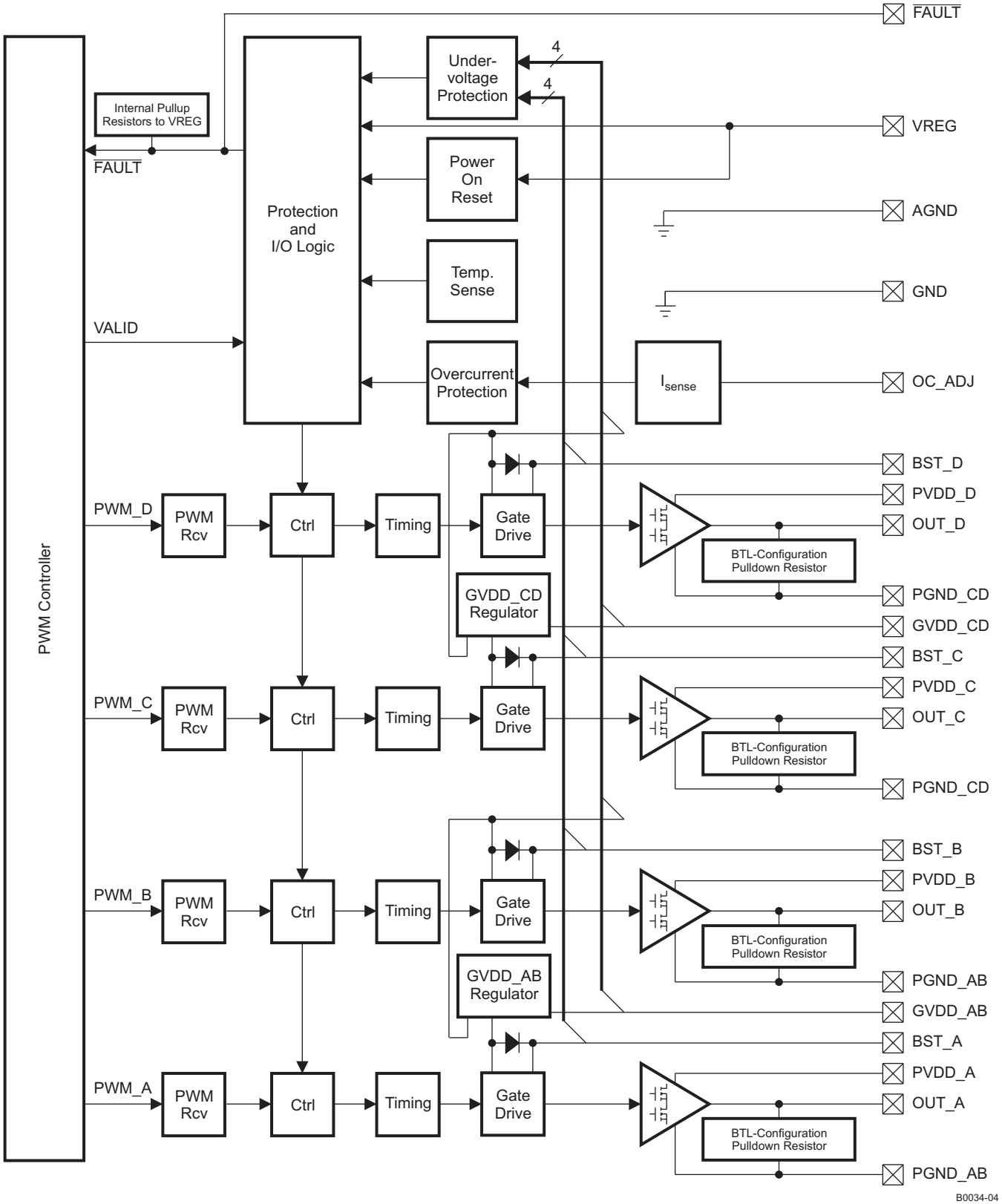


Figure 1. Power Stage Functional Block Diagram

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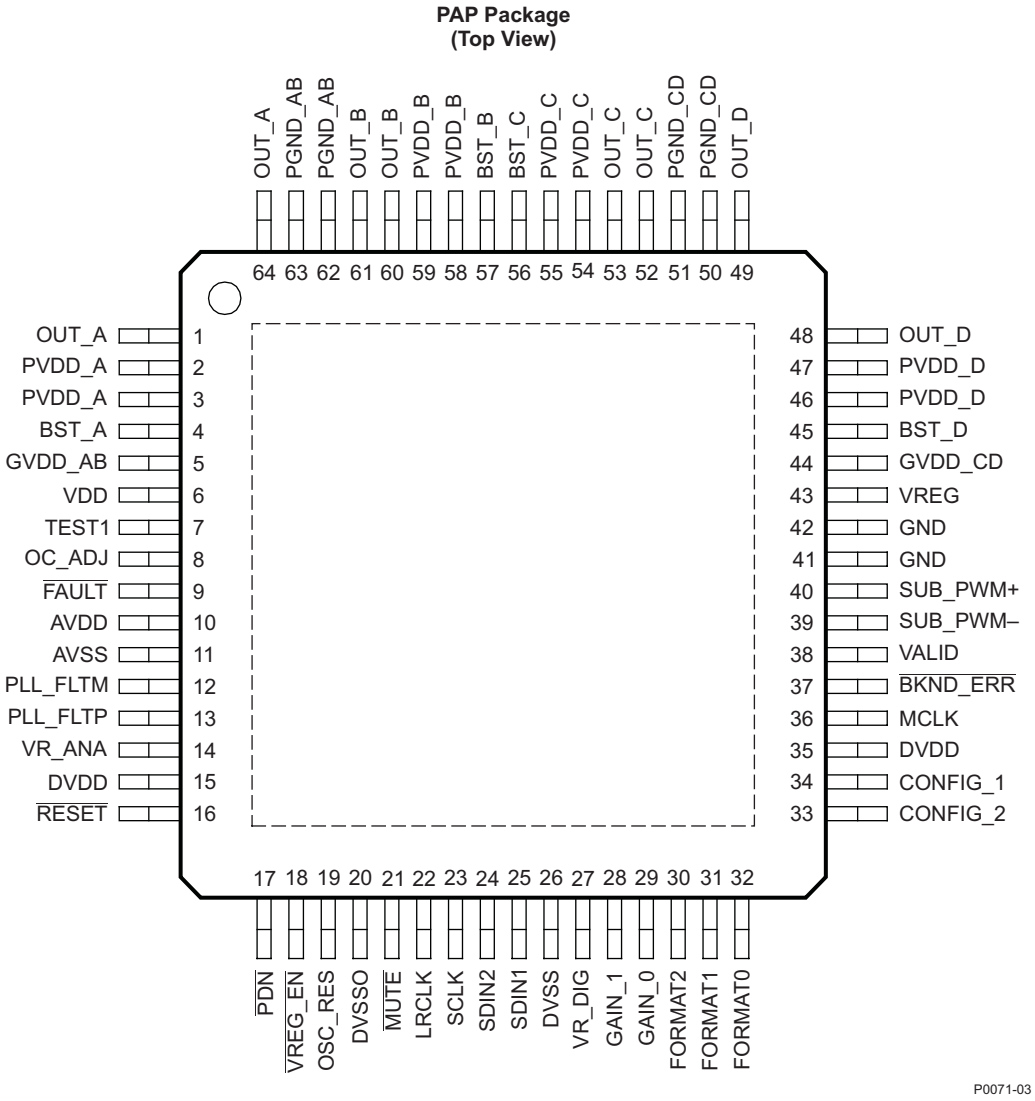
64-PIN, HTQFP PACKAGE (TOP VIEW)



PIN FUNCTIONS

PIN		I/O(1)	5-V TOLERANT	TERMINATION (2) (3)	DESCRIPTION
NAME	NO.				
AVDD	10	P			3.3-V Analog power supply
AVSS	11	P			Analog 3.3-V supply ground
BKND_ERR	37	DI		Pullup	Active low. A back-end error sequence is initiated by applying a logic low to this pin. Connect to an external power stage. If no external power stage is used, connect directly to DVDD.
BST_A	4	P			High-side bootstrap supply for half-bridge A
BST_B	57	P			High-side bootstrap supply for half-bridge B
BST_C	56	P			High-side bootstrap supply for half-bridge C

(1) TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output
(2) All pullups are 20-μA *weak* pullups and all pulldowns are 20-μA *weak* pulldowns. The pullups and pulldowns are included to assure proper input logic levels if the terminals are left unconnected (pullups → logic 1 input; pulldowns → logic 0 input). Devices that drive inputs with pullups must be able to sink 50 μA while maintaining a logic-0 drive level. Devices that drive inputs with pulldowns must be able to source 50 μA while maintaining a logic-1 drive level.
(3) If desired, low-ESR capacitance values can be implemented by paralleling two or more ceramic capacitors of equal value. Paralleling capacitors of equal value provides an extended high-frequency supply decoupling. This approach avoids the potential of producing parallel resonance circuits that have been observed when paralleling capacitors of different values.

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PIN FUNCTIONS (continued)

PIN		I/O(1)	5-V TOLERANT	TERMINATION (2) (3)	DESCRIPTION
NAME	NO.				
BST_D	45	P			High-side bootstrap supply for half-bridge D
CONFIG_2	33	P		Pulldown	Input/output configuration. Connect this terminal directly to GND.
CONFIG_1	34	P		Pulldown	Input/output configuration. Connect this terminal directly to DVDD.
DVDD	15, 35	P			3.3-V Digital power supply
DVSS	26	P			Digital ground
DVSSO	20	P			Oscillator ground
$\overline{\text{FAULT}}$	9	DO			Overtemperature, undervoltage, and overcurrent fault reporting. Active low indicates fault. If high, normal operation.
FORMAT2	30	DI		Pulldown	Digital data format select MSB.
FORMAT1	31	DI		Pulldown	Digital data format select LSB.
FORMAT0	32	DI		Pulldown	Digital data format select.
GAIN_1	28	DI	5-V		MSB of gain select.
GAIN_0	29	DI	5-V		LSB of gain select. GAIN_0 and GAIN_1 allow 4 possible gain selections.
GND	41, 42	P			Analog ground for power stage.
GVDD_AB	5	P			Gate drive voltage for half-bridges A and B (10.8 V to 13.2 V)
GVDD_CD	44	P			Gate drive voltage for half-bridges C and D (10.8 V to 13.2 V)
LRCLK	22	DI	5-V		Input serial audio data left/right clock (sampling rate clock)
MCLK	36	DI	5-V		Clock master input. The input frequency of this clock can range from 4.9 MHz to 49 MHz.
$\overline{\text{MUTE}}$	21	DI	5-V	Pullup	Performs a soft mute of outputs, active-low. A logic low on this pin sets the outputs equal to 50% duty cycle. A logic high on this pin allows normal operation. The mute control provides a noiseless volume ramp to silence. Releasing mute provides a noiseless ramp to previous volume.
OC_ADJ	8	AO			Analog overcurrent programming. Requires 22-kΩ resistor to ground.
OSC_RES	19	AO			Oscillator trim resistor. Connect an 18.2-kΩ (1% tolerance is required) resistor to DVSSO.
OUT_A	1, 64	O			Output, half-bridge A
OUT_B	60, 61	O			Output, half-bridge B
OUT_C	52, 53	O			Output, half-bridge C
OUT_D	48, 49	O			Output, half-bridge D
$\overline{\text{PDN}}$	17	DI	5-V	Pullup	Power down, active-low. $\overline{\text{PDN}}$ stops all clocks, and outputs stop switching whenever a logic low is applied. When $\overline{\text{PDN}}$ is released, the device powers up all logic, starts all clocks, and performs a soft start that returns to the previous configuration changes to FORMATx and GAINx pins are ignored on $\overline{\text{PDN}}$ cycling.
PGND_AB	62, 63	P			Power ground for half-bridges A and B
PGND_CD	50, 51	P			Power ground for half-bridges C and D
PLL_FLTM	12	AO			PLL negative loop filter terminal
PLL_FLTP	13	AI			PLL positive loop filter terminal
PVDD_A	2, 3	P			Power supply input for half-bridge output A (0 V–21 V)
PVDD_B	58, 59	P			Power supply input for half-bridge output B (0 V–21 V)
PVDD_C	54, 55	P			Power supply input for half-bridge output C (0 V–21 V)
PVDD_D	46, 47	P			Power supply input for half-bridge output D(0 V–21 V)
$\overline{\text{RESET}}$	16	DI	5-V	Pullup	Reset, active-low. A system reset is generated by applying a logic low to this terminal. $\overline{\text{RESET}}$ is an asynchronous control signal that sets the VALID outputs low, and places the PWM in the hard mute state (stop switching). Gain is immediately set to full attenuation. Upon the release of $\overline{\text{RESET}}$, if $\overline{\text{PDN}}$ is high, the system performs a 4-ms to 5-ms device initialization and sets the gain and format to the settings determined by the hardware pins.

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PIN FUNCTIONS (continued)

PIN		I/O[1]	5-V TOLERANT	TERMINATION[2] [3]	DESCRIPTION
NAME	NO.				
SCLK	23	DI	5-V		Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock.
SDIN1	25	DI	5-V		Serial audio data 1 input is one of the serial data input ports. SDIN1 supports three discrete (stereo) data formats.
SDIN2	24	DI	5-V		Serial audio data 2 input is one of the serial data input ports. SDIN2 supports three discrete (stereo) data formats.
SUB_PWM–	39	DO			Subwoofer negative PWM output. BD modulated signal.
SUB_PWM+	40	DO			Subwoofer positive PWM output. BD modulated signal.
TEST1	7	DI			Test pin. Connect directly to GND.
VALID	38	DO			Output indicating validity of ALL PWM channels, active-high. This pin is connected to an external power stage. If no external power stage is used, leave this pin floating.
VDD	6	P			Power supply for VREG (10.8 V to 13.2 V)
VR_ANA	14	P			Internally regulated 1.8-V analog supply voltage. This terminal must not be used to power external devices.
VR_DIG	27	P			Internally regulated 1.8-V analog supply voltage. This terminal must not be used to power external devices.
VREG	43	P			Digital regulator output. Not to be used for powering external circuitry.
$\overline{\text{VREG\_EN}}$	18	DI		Pulldown	Voltage regulator enable. Connect directly to GND.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1]

		VALUE	UNIT
Supply voltage	GVDD, VDD	–0.3 to 13.2	V
	PVDD	–0.3 to 23	
	DVDD	–0.3 to 3.6	
	AVDD	–0.3 to 3.6	
	OUT_X to GND_X	–0.3 to 30	
	BST_X to GND_X	–0.3 to 43.2	
Input voltage	3.3-V digital input	–0.5 to DVDD + 0.5	V
	5-V tolerant[2] digital input	–0.5 to DVDD + 2.5	
Input clamp current, I_{IK} (V_I < 0 or V_I > 1.8 V)		±20	mA
Output clamp current, I_{OK} (V_O < 0 or V_O > 1.8 V)		±20	mA
Operating free-air temperature		0 to 85	°C
Operating junction temperature range		0 to 150	°C
Storage temperature range, T_{stg}		–40 to 125	°C

(1) Stresses beyond those listed under *absolute ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operation conditions* are not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
(2) 5-V tolerant inputs are $\overline{\text{PDN}}$, $\overline{\text{RESET}}$, $\overline{\text{MUTE}}$, SCLK, LRCLK, MCLK, SDIN1, SDIN2.

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THERMAL INFORMATION

THERMAL METRIC(1)(2)		TAS5701 PAP (64 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	27.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	16	
θ_{JB}	Junction-to-board thermal resistance	13	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	7.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Gate drive supply voltage	GVDD, VDD	10.8	12	13.2	V
	Output bridge supply voltage	PVDD	0		21	V
	Digita supply voltage	DVDD	3	3.3	3.6	V
	Analog supply voltage	AVDD	3	3.3	3.6	V
V_{IH}	High-level input voltage	3.3-V TTL, 5-V tolerant	2			V
V_{IL}	Low-level input voltage	3.3-V TTL, 5-V tolerant			0.8	V
T_A	Operating ambient temperature range		0		85	°C
T_J	Operating junction temperature range		0		150	°C
R_L (BTL)	Load impedance	Output filter: L = 22 μH, C = 680 nF.	6.0	8		Ω
R_L (SE)			3.2	4		
R_L (PBTL)			3.2	4		
L_O (BTL)	Output-filter inductance	Minimum output inductance under short-circuit condition		10		μH
L_O (SE)				10		
L_O (PBTL)				10		

PWM OPERATION AT RECOMMENDED OPERATING CONDITIONS

PARAMETER	TEST CONDITIONS	MODE	VALUE	UNIT
Output sample rate 2×–1× oversampled	32–kHz data rate ±2%	12× sample rate	384	kHz
	44.1-, 88.2-, 176.4-kHz data rate ±2%	8×, 4×, and 2× sample rates	352.8	kHz
	48-, 96-, 192-kHz data rate ±2%	8×, 4×, and 2× sample rates	384	kHz

PLL INPUT PARAMETERS AND EXTERNAL FILTER COMPONENTS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MCLKI}	Frequency, MCLK (1 / t_{cyc2})		4.9		49.2	MHz
	MCLK duty cycle		40%	50%	60%	
	MCLK minimum high time	≥2-V MCLK = 49.152 MHz, within the min and max duty cycle constraints	8			ns
	MCLK minimum low time	≤0.8-V MCLK = 49.152 MHz, within the min and max duty cycle constraints	8			ns
	LRCLK allowable drift before LRCLK reset				4	MCLKs
	External PLL filter capacitor C1	SMD 0603 Y5V		47		nF
	External PLL filter capacitor C2	SMD 0603 Y5V		4.7		nF
	External PLL filter resistor R	SMD 0603, metal film		470		Ω

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ELECTRICAL CHARACTERISTICS

DC Characteristics

T_A = 25 °C, PVCC_X = 18 V, DVDD = AVDD = 3.3 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	3.3-V TTL and 5-V tolerant (1)	I_{OH} = –4 mA	2.4			V
V_{OL}	Low-level output voltage	3.3-V TTL and 5-V tolerant (1)	I_{OL} = 4 mA			0.5	V
I_{IL}	Low-level input current	LRCLK, SCLK, SDINx, MCLK, GAIN_x, VREG_EN, FORMATx, CONFIG_x	V_I = 0 V, DVDD = 3.6 V			±2	µA
		BKND_ERR, RESET, PDN, MUTE	V_I = 0 V, DVDD = 3.6 V			±50	
I_{IH}	High-level input current	RESET, PDN, MUTE, GAIN_x, BKND_ERR	V_I = 3.6 V, DVDD = 3.6 V			±2	µA
		VREG_EN, FORMAT_x, CONFIG_x, LRCLK, SCLK, SDINx, MCLK	V_I = 3.6 V, DVDD = 3.6 V			±50	
		RESET, PDN, MUTE, LRCLK, SCLK, SDINx, MCLK, GAIN_x	V_I = 5.5 V, DVDD = 3.6 V			±50	
I_{DD}	Input digital supply current	Supply voltage (DVDD, AVDD)	Normal mode, 50% duty cycle		65	80	mA
			Power down (PDN = low)		8	16	
			Reset (RESET = low)		23	33	
I_{GVDD}	Gate supply current per GVDD_xx input		Normal mode, 50% duty cycle		5	10	mA
			RESET = 0		2.2	4	
			PDN = 0		2.2	4	
I_{PVDD}	Input power supply current		No load		30	60	mA
I_{PVDD}(PDN)	Power-down current		No load, PDN = 0		1	100	µA
I_{PVDD}(RESET)	Reset current		No load, RESET = 0		1	100	µA
$r_{DS(on)}$	Drain-to-source resistance, LS	T_J = 25°C, includes metallization resistance			140		mΩ
	Drain-to-source resistance, HS	T_J = 25°C, includes metallization resistance			140		
I/O Protection							
V_{uvp}	Undervoltage protection limit	PVDD falling			9.2		V
$V_{uvp,hyst}$	Undervoltage protection limit	PVDD rising			9.6		V
OTE (2)	Overtemperature error				150		°C
OTE_{HYST} (2)	Extra temperature drop required to recover from error				30		°C
OLPC	Overload protection counter	f_{PWM} = 384 kHz			1.25		ms
I_{OC}	Overcurrent limit protection	R_{OCP} = 22 kΩ			4.5		A
I_{OCT}	Overcurrent response time				150		ns
R_{OCP}	OC programming resistor range	Resistor tolerance = 5% for typical value; the minimum resistance should not be less than 20 kΩ.		20	22		kΩ
R_{PD}	Internal pulldown resistor at the output of each half-bridge	Connected when RESET is active to provide bootstrap capacitor charge.			3		kΩ

(1) 5-V tolerant inputs are PDN, RESET, MUTE, SCLK, LRCLK, MCLK, SDIN1, SDIN2, GAIN_0, and GAIN_1.
(2) Specified by design.

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AC Characteristics (BTL)

PVDD_X = 18 V, BTL mode, R_L = 8 Ω, R_{OC} = 22 kΩ, C_{BST} = 33-nF, audio frequency = 1 kHz, AES17 filter, F_{PWM} = 384 kHz, T_A = 25°C (unless otherwise noted). All performance is I naccordance with recommended operating conditions, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	PVDD = 18 V, 10% THD, 1-kHz input signal		20.0		W
		PVDD = 18 V, 7% THD, 1-kHz input signal		18.6		
		PVDD = 12 V, 10% THD, 1-kHz input signal		9		
		PVDD = 12 V, 7% THD, 1-kHz input signal		8.3		
THD+N	Total harmonic distortion + noise	PVDD = 18 V, P_O = 10 W (half-power)		0.1%		
		PVDD = 12 V, P_O = 4.5 W (half-power)		0.08%		
		1 W		0.05%		
V_n	Output integrated noise	A-weighted		50		μV
	Crosstalk	P_O = 1 W, f = 1 kHz		–73		dB
SNR	Signal-to-noise ratio (1)	A-weighted, f = 1 kHz, maximum power at THD < 1%		101		dB
P_D	Power dissipation due to idle losses (I_{PVDD_X})	P_O = 0 W, 4 channels switching (2)		0.6		W

(1) SNR is calculated relative to 0-dBFS input level.
(2) Actual system idle losses are affected by core losses of output inductors.

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SERIAL AUDIO PORTS SLAVE MODE

Serial audio ports slave mode over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLKIN}	Frequency, SCLK 32 × f_S, 48 × f_S, 64 × f_S	C_L = 30 pF	1.024		12.288	MHz
t_{su1}	Setup time, LRCLK to SCLK rising edge		10			ns
t_{h1}	Hold time, LRCLK from SCLK rising edge		10			ns
t_{su2}	Setup time, SDIN to SCLK rising edge		10			ns
t_{h2}	Hold time, SDIN from SCLK rising edge		10			ns
	LRCLK frequency		32	48	192	kHz
	SCLK duty cycle		40%	50%	60%	
	LRCLK duty cycle		40%	50%	60%	
	SCLK rising edges between LRCLK rising edges		32		64	SCLK edges
$t_{(edge)}$	LRCLK clock edge with respect to the falling edge of SCLK		–1/4		1/4	SCLK period

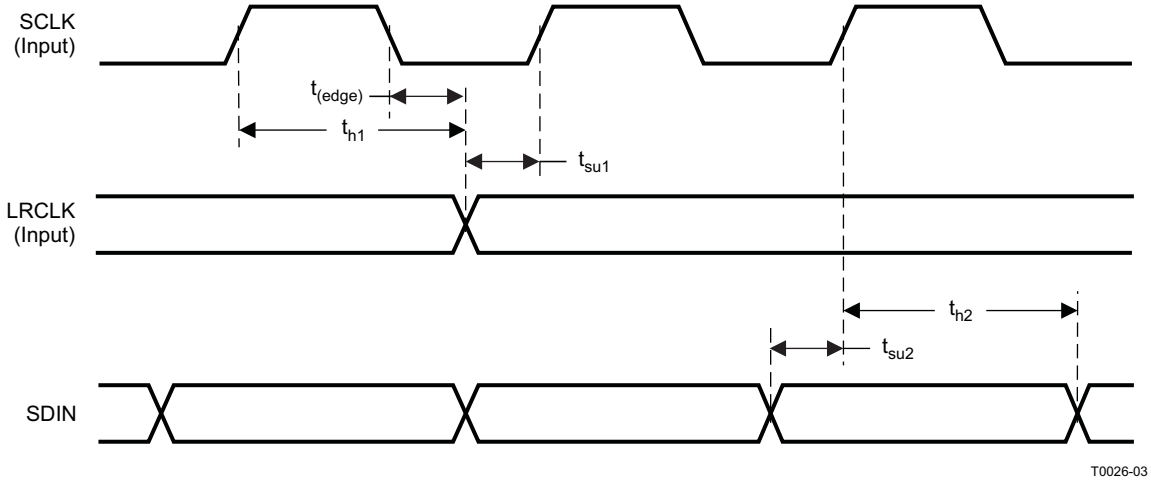

Figure 2. Slave Mode Serial Data Interface Timing

HARDWARE SELECT PINS

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
t_{su}	Setup time, FORMATx, CONFIG_x, GAIN_x to $\overline{\text{RESET}}$ rising edge	100			µs

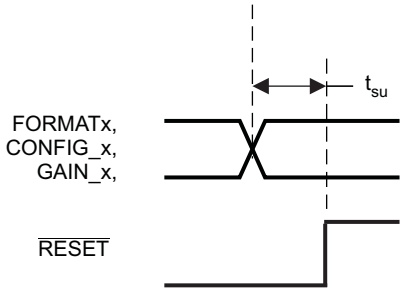

Figure 3. Mode Pins Setup Time

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RESET TIMING ($\overline{\text{RESET}}$) AND POWER-ON RESET

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(VALID\_LOW)}$	Time to assert VALID (reset to power stage) low		100		ns
$t_{w(RESET)}$	Pulse duration, $\overline{\text{RESET}}$ active	100	200		ms
$t_{d(START)}$	Time to start-up		3.6		ms

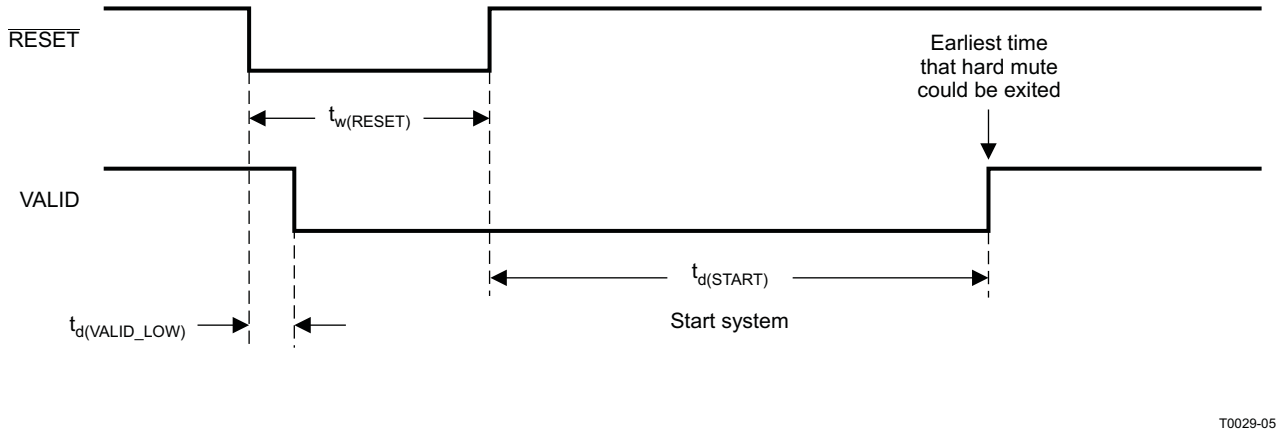

Figure 4. Reset Timing

When power is applied to DVDD, $\overline{\text{RESET}}$ must be held low for at least 100 μs after DVDD reaches 3.0 V.

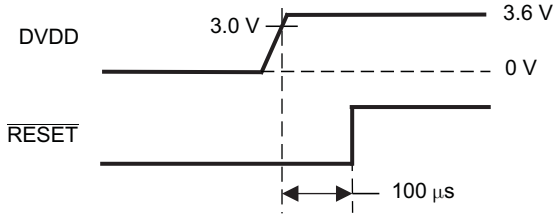

Figure 5. Power-On Reset Timing

POWER-DOWN ($\overline{\text{PDN}}$) TIMING

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(VALID\_LOW)}$	Time to assert VALID (reset to power stage) low		725		μs
$t_{d(STARTUP)}$	Device start-up time		650		μs
t_w	Minimum pulse duration required	1			μs

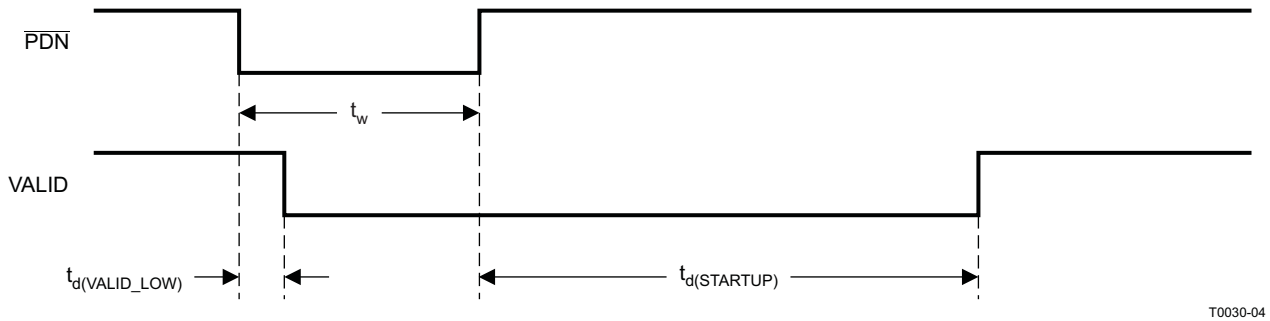

Figure 6. Power-Down Timing

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BACK-END ERROR ($\overline{\text{BKND\_ERR}}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(ER)}$	Pulse duration, $\overline{\text{BKND\_ERR}}$ active (active-low)	350			ns
$t_{p(valid\_high)}$	Time to stay in the OUT_x low state. After $t_{p(valid\_high)}$, the TAS5701 attempts to bring the system out of the OUT_x low state if $\overline{\text{BKND\_ERR}}$ is high.		300		ms
$t_{p(valid\_low)}$	Time TAS5701 takes to bring OUT_x low after $\overline{\text{BKND\_ERR}}$ assertion.		350		ns

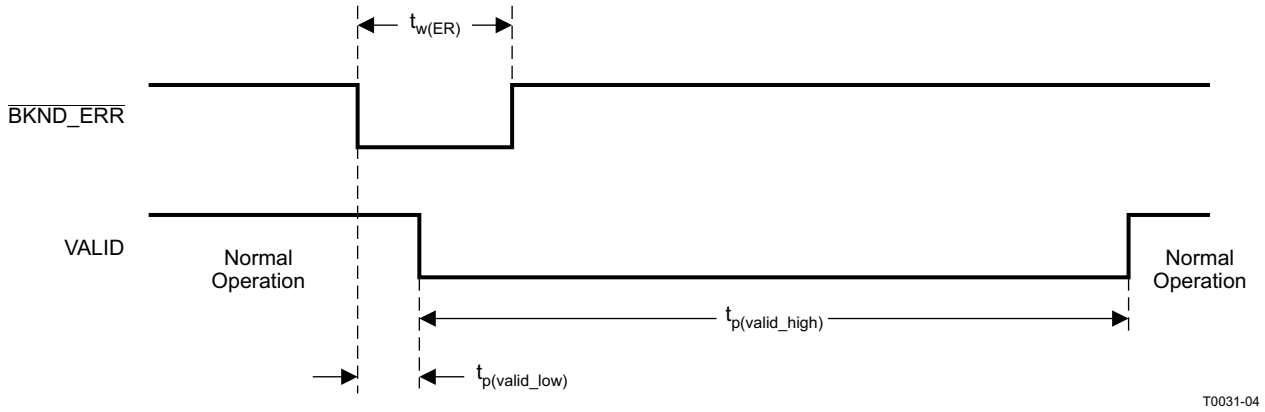

Figure 7. Error Recovery Timing

MUTE TIMING ($\overline{\text{MUTE}}$)

Control signal parameters over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(VOL)}$	Volume ramp time. Ramp time = Number of steps × stepsize(1)		1024		steps

(1) Stepsize = 4 LRCLKs (for 32–48 kHz sample rate); 8 LRCLKs (for 88.2–96 kHz sample rate); 16 LRCLKs (for 176.4–192 kHz sample rate)

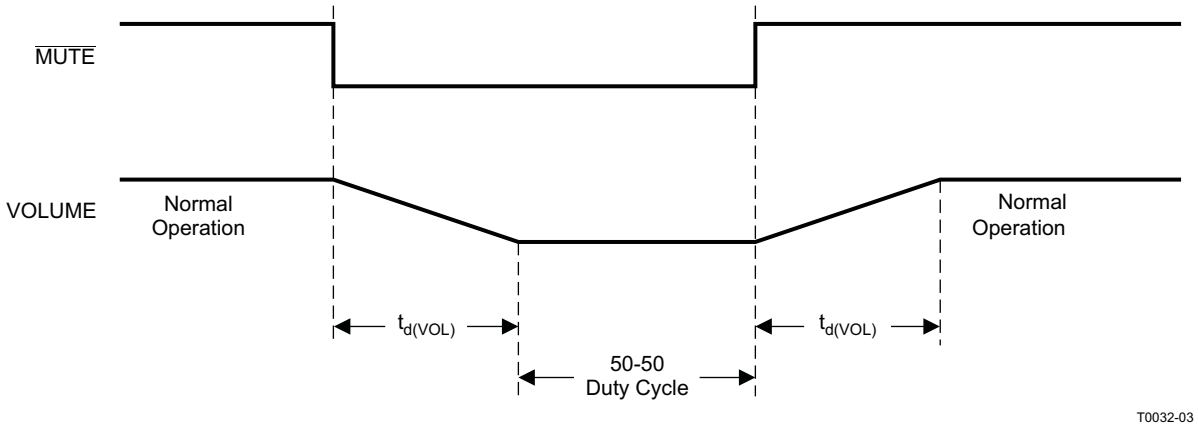

Figure 8. Mute Timing

TYPICAL CHARACTERISTICS, BTL CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

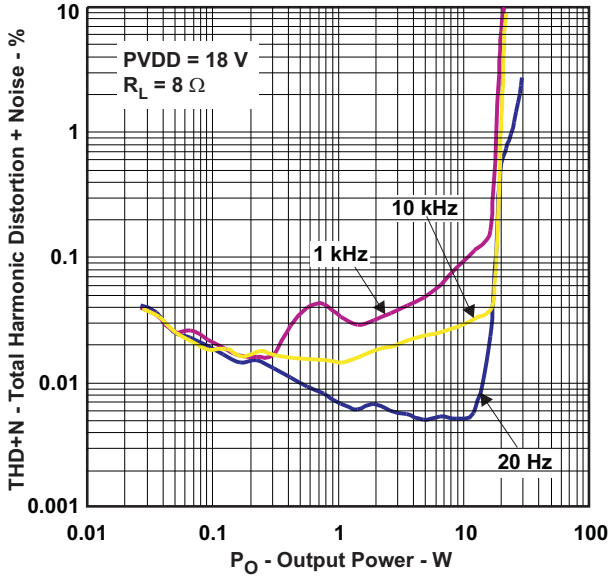

Figure 9.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

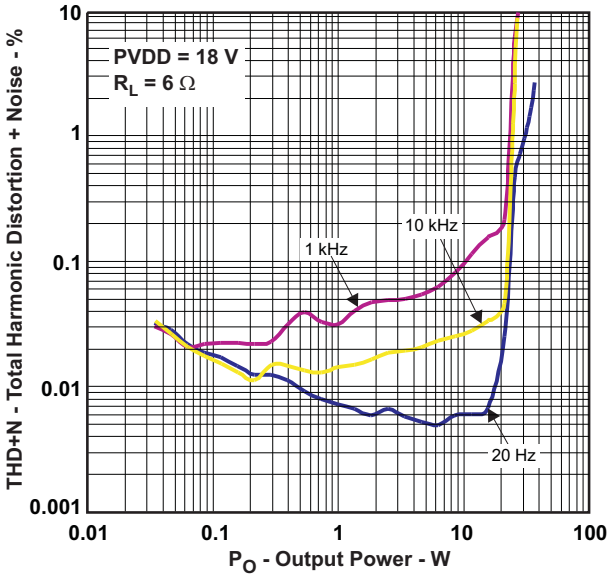

Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

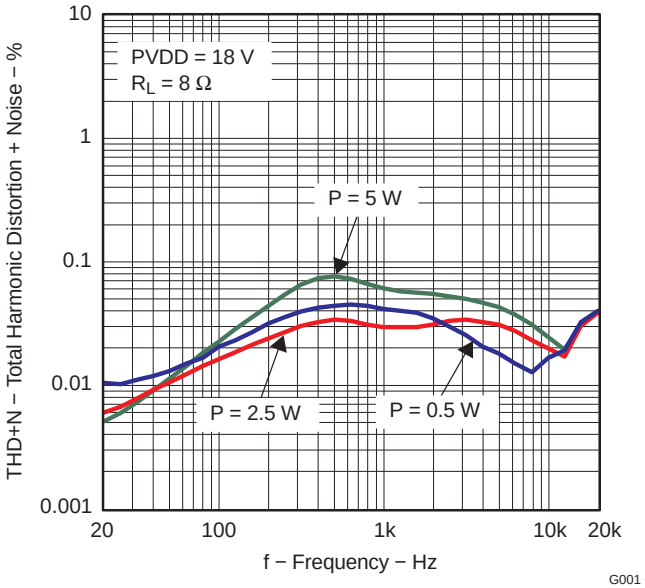

Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

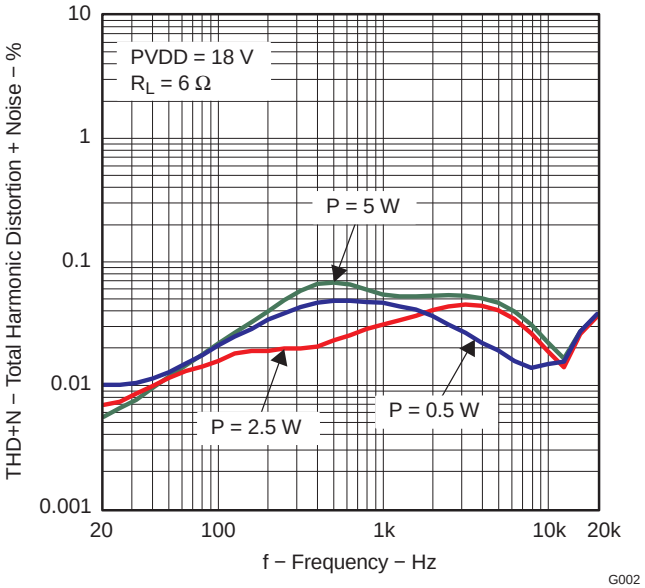

Figure 12.

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TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

SYSTEM EFFICIENCY vs OUTPUT POWER

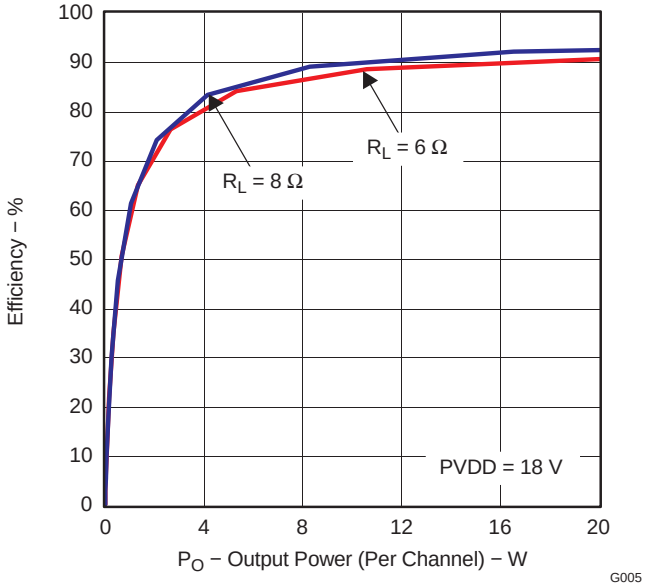

Figure 13.

SUPPLY CURRENT vs OUTPUT POWER

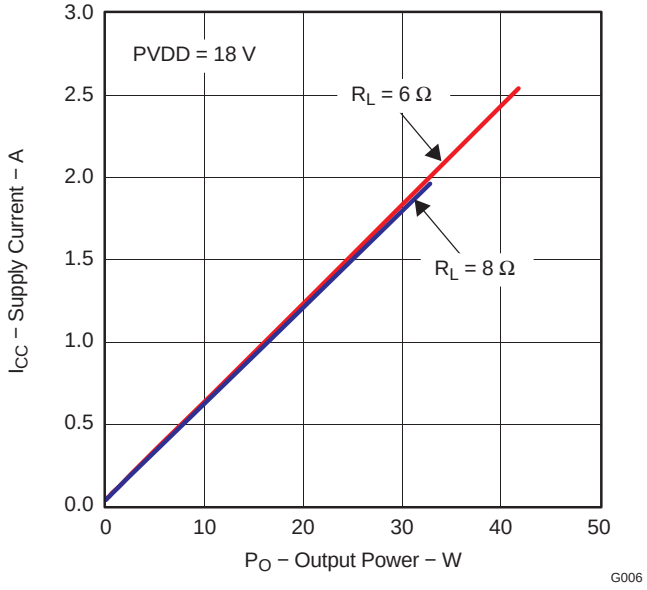

Figure 14.

OUTPUT POWER vs SUPPLY VOLTAGE

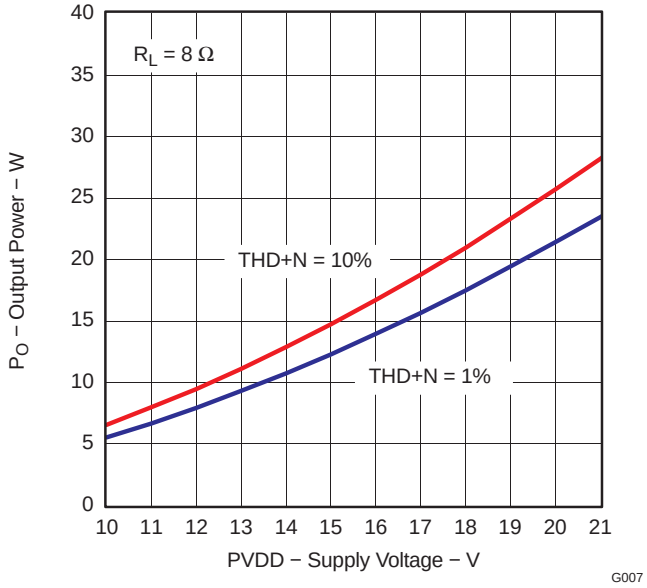

Figure 15.

OUTPUT POWER vs SUPPLY VOLTAGE

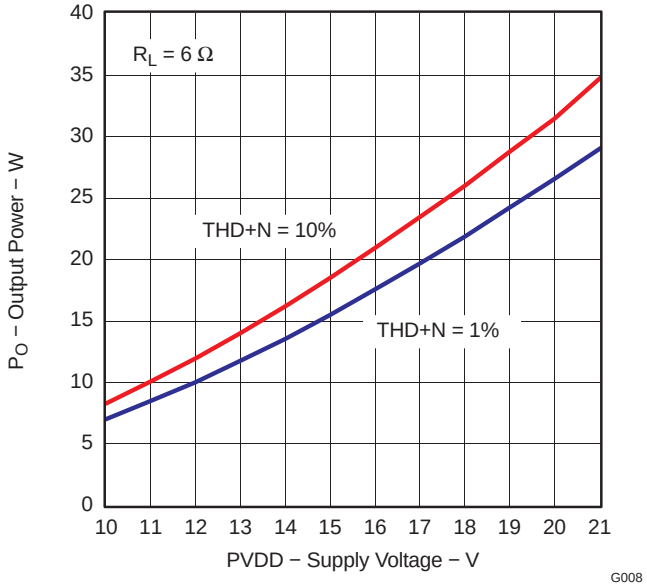

Figure 16.

TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

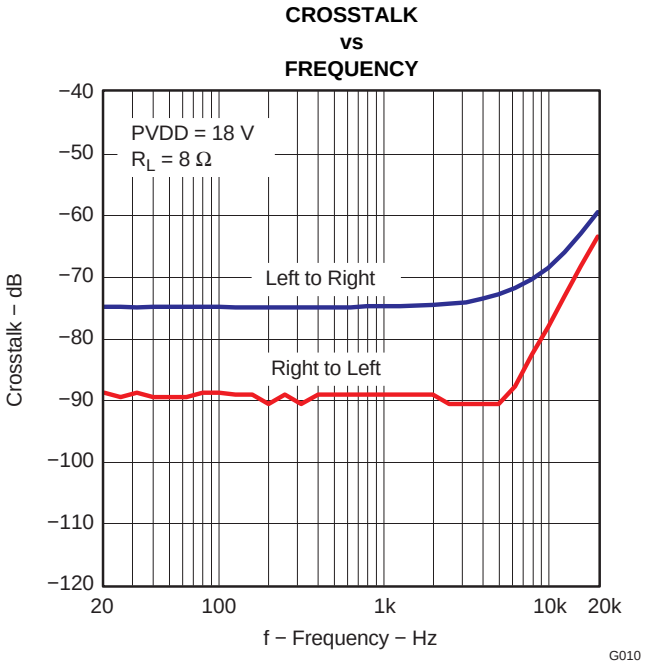

Figure 17.

DETAILED DESCRIPTION

POWER SUPPLY

The digital portion of the chip requires 3.3 V, and the analog portion can work with a variable range up to 12 V. PVDD has a maximum operational range up to 22 V.

To facilitate system design, the TAS5701 needs only a 12-V supply in addition to the (typical) 18-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide outstanding electrical and acoustical characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate gate drive supply (GVDD_X), bootstrap pins (BST_X), and power-stage supply pins (PVDD_X). Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 352 kHz to 384 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle. In an application running at a reduced switching frequency, generally 192 kHz, the bootstrap capacitor might need to be increased in value.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X pin is decoupled with a 100-nF ceramic capacitor placed as close as possible to each supply pin.

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The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 18-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5701 is fully protected against erroneous power-stage turnon due to parasitic gate charging.

Clock, Auto Detection, and PLL

The TAS5701 digital audio processor (DAP) is a clock slave device. It accepts MCLK, SCLK, and LRCLK.

The TAS5701 checks to verify that SCLK is a specific value of 32-f_s, 48- f_s, or 64-f_s. The DAP only supports a 1 × f_s LRCLK. The timing relationship of these clocks to SDIN1and SIN2 is shown in subsequent sections. The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable or absent) to produce the internal clock.

The DAP can auto-detect and set the internal clock control logic to the appropriate settings for the frequencies of 32 kHz, normal speed (44.1 or 48 kHz), double speed (88.2 kHz or 96 kHz), and quad speed (176.4 kHz or 192 kHz).

SERIAL DATA INTERFACE

Serial data is input on SDIN1 and SIN2. The PWM outputs are derived from SDIN1 ands SIN2. The TAS5701 DAP accepts 32-, 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz serial data in 16-, 18-, 20-, or 24-bit data in left-justified, right-justified, and I^2S serial data formats. See Table 1 for format control settings.

SDIN1 left channel data is sent to OUTA/OUTB configured in BTL. SDIN1 right channel data is sent to OUTC/OUTD. SDIN2 left channel data is sent to SUB_PWM+/–. The right channel data of SDIN2 is ignored.

PWM SECTION

The DAP (digital audio processor) has three channels of high-performance digital PWM modulators that are designed to drive bride-tied output H-bridge configurations with BD modulation.

The DAP uses noise-shaping and sophisticated error correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper to provide >100-dB SNR performance from 20 Hz to 20 kHz.

The PWM section accepts 24-bit PCM data from the DAP and outputs three PWM audio output channels. The PWM section output supports bridge-tied loads ONLY.

The PWM section has individual channel dc blocking filters that are ALWAYS enabled. The filter cutoff frequency is less than 1 Hz.

Finally, the PWM section has a fixed maximum modulation limit of 97.7%.

SERIAL INTERFACE CONTROL AND TIMING

I^2S Timing

I^2S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A system clock (SCLK) running at 32, 48, or 64 × f_s is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

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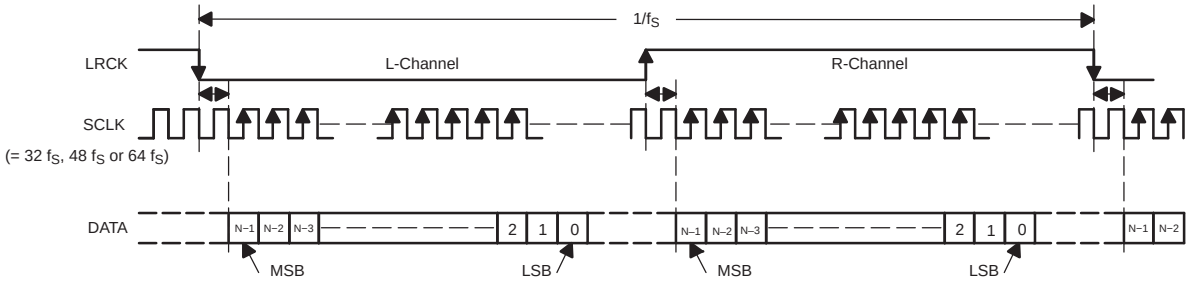

Figure 18. I²S Format

Left-Justified

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f_s is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

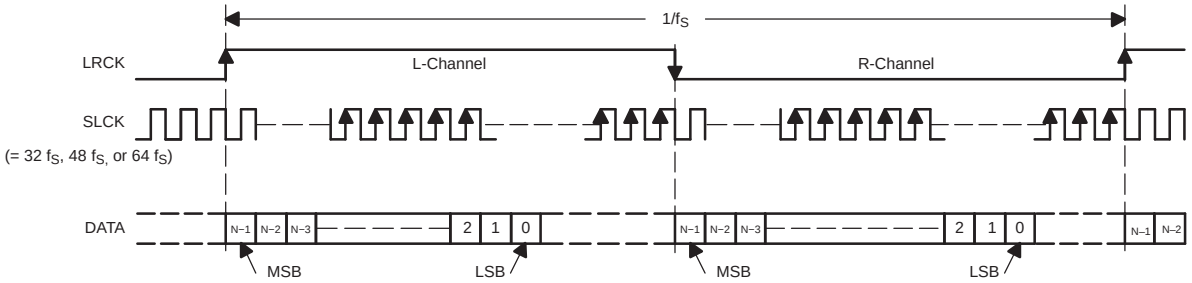

Figure 19. Left-Justified Format

Right-Justified

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f_s is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused leading data bit positions.

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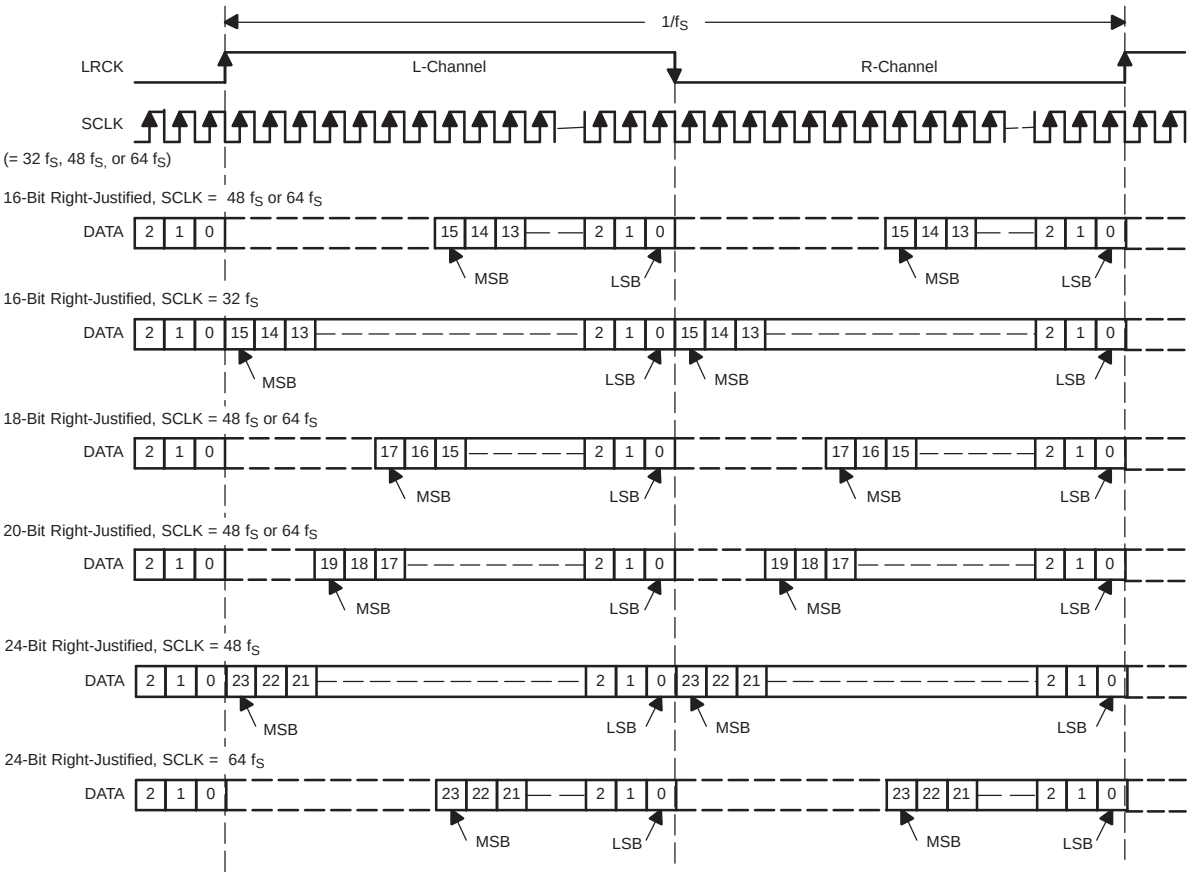

Figure 20. Right-Justified Format

Format Control

The digital data input format is selected via three external terminals (FORMAT0, FORMAT1, and FORMAT2). Table 1 lists the corresponding data format for SDIN1 and SDIN2. LRCLK and SCLK are shared clocks for SDIN1 and SDIN2. Changes to the FORMATx terminals are latched in immediately on a rising edge of $\overline{\text{RESET}}$. Changes to the FORMATx terminals while $\overline{\text{RESET}}$ is high are not allowed.

Table 1. Format Control

FORMAT2	FORMAT1	FORMAT0	SERIAL DIGITAL DATA FORMAT
0	0	0	16-Bit right-justifed
0	0	1	18-Bit right-justified
0	1	0	20-Bit right-justified
0	1	1	24-Bit right-justified
1	0	0	16-, 24-Bit I^2S
1	0	1	16-, 24-Bit left-justified
1	1	0	Reserved. Setting is not allowed.
1	1	1	Reserved. Setting is not allowed.

Gain Control

The gain of the DAP is selected via two external gain pins (GAIN_0 and GAIN_1). Table 2 lists the corresponding channel gain (for ALL channels) for GAIN_0 and GAIN_1 settings. Individual channel gain is not possible. Changes to the GAIN_x terminals are latched in immediately on a rising edge of $\overline{\text{RESET}}$. Changes to the GAIN_x terminals while $\overline{\text{RESET}}$ is high are not allowed.

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Table 2. Gain Control

GAIN_1	GAIN_0	CHANNEL GAIN (dB)
0	0	0
0	1	6
1	0	12
1	1	18

DEVICE PROTECTION SYSTEM

The TAS5701 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overtemperature, and undervoltage. The TAS5701 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and reporting the error on the $\overline{\text{FAULT}}$ pin ($\overline{\text{FAULT}}$ = 0); the device automatically recovers when the fault condition has been removed.

Short-Circuit Protection

The device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored by a protection system. If a high-current condition situation exists, i.e., the power stage outputs are shorted, the protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ going low. Overcurrent protection is not independent for half-bridges A and B and, respectively, C and D. That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shut down.

Overtemperature Protection

If the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ going low. Once the temperature decreases 30°C (typical), the device resumes normal operation.

Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5701 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the protection circuitry and ensures that all circuits are fully operational when the VDD and GVDD_X supply voltages reach 9.6 V (typical). Although GVDD_x and VDD pins are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_x pin results in all outputs immediately being set in the high-impedence (Hi-Z) state and $\overline{\text{FAULT}}$ pin being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

REVISION HISTORY

Changes from Original (June 2008) to Revision A **Page**

- Replaced the with the DISSIPATION RATINGS table Thermal Information table 8

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5701PAP	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (5+1)	Yes	Call TI	Call TI	0 to 85	TAS5701
TAS5701PAP.A	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (5+1)	-	Call TI	Call TI	0 to 85	TAS5701
TAS5701PAP.B	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (5+1)	-	Call TI	Call TI	0 to 85	
TAS5701PAPR	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	Call TI	Call TI	0 to 85	TAS5701
TAS5701PAPR.A	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	-	Call TI	Call TI	0 to 85	TAS5701

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

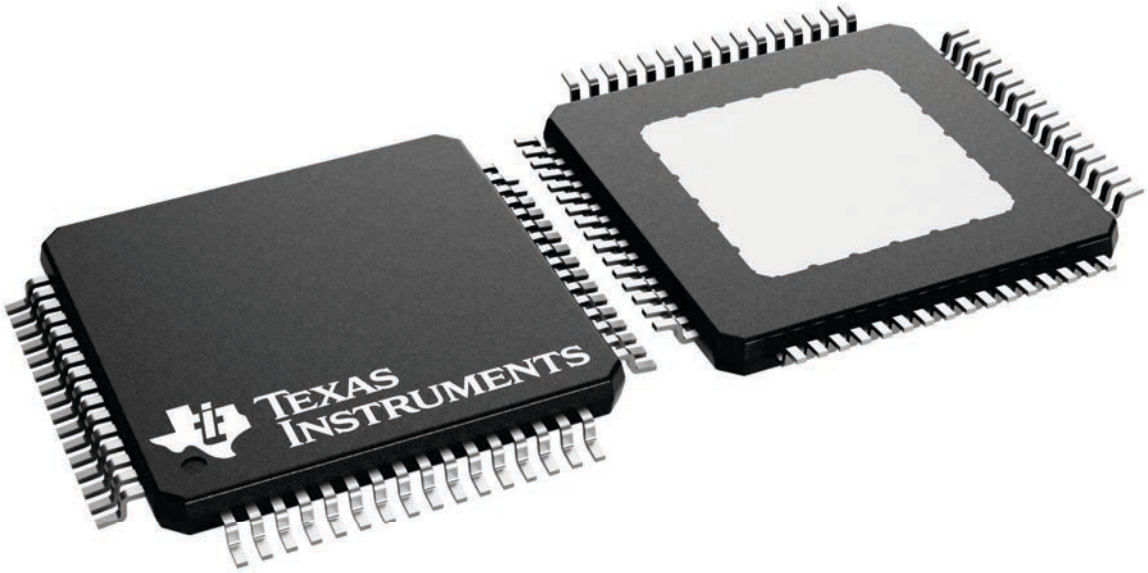
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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