TCAN1046A-Q1 具有待机模式的汽车类双路 CAN FD 收发器

1 特性

- AEC-Q100（等级 1）：符合汽车应用要求
- 两个具有模式控制功能的独立高速 CAN FD 收发器
- 符合 ISO 11898-2:2016 物理层标准要求
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 支持传统 CAN 和经优化的 CAN FD 性能（数据速率为 2、5 和 8Mbps）
  - 具有较短的对称传播延迟时间，可增加时序裕量
- 支持 12V 和 24V 电池应用
- 接收器共模输入电压：±12V
- 保护特性：
  - 总线故障保护：±58V
  - 欠压保护
  - TXD 显性超时 (DTO)
    - 数据速率低至 9.2kbps
  - 热关断保护 (TSD)
- 工作模式：
  - 正常模式
  - 支持远程唤醒请求功能的低功耗待机模式
- 优化了未上电时的性能
  - 总线和逻辑引脚为高阻抗（运行总线或应用上无负载）
  - 支持热插拔：在总线和 RXD 输出上可实现上电和断电无干扰运行
- 结温范围：–40°C 至 150°C
- 采用 SOIC (14) 封装和无引线 VSON (14) 封装 (4.5mm x 3.0mm)，具有改进的自动光学检查 (AOI) 功能

2 应用

- 汽车和运输
  - 车身控制模块
  - 汽车网关
  - 高级驾驶辅助系统 (ADAS)
  - 信息娱乐系统

3 说明

TCAN1046A-Q1 是一款双路高速控制器局域网 (CAN) 收发器，符合 ISO 11898-2:2016 高速 CAN 规范的物理层要求。

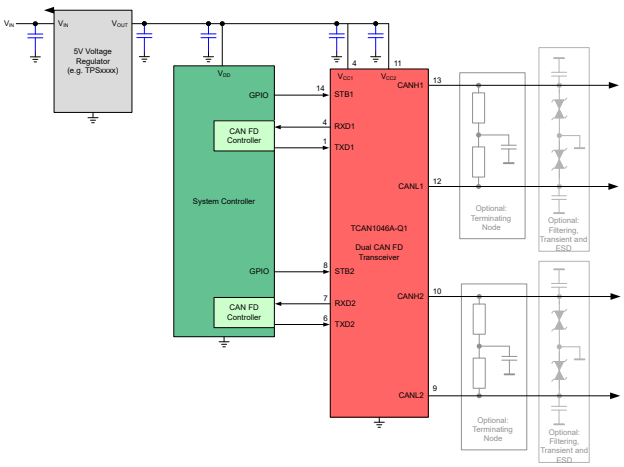
该器件支持传统 CAN 和 CAN FD 网络（数据速率高达 8 兆位/秒 (Mbps)）。此外，该器件具有两个带独立电源（V_{CC1} 和 V_{CC2}）和模式控制引脚（STB1 和 STB2）的 CAN FD 通道，允许每个 CAN 通道真正独立地运行。在需要冗余或额外 CAN FD 通道作为系统故障时的备份的应用中，能够独立操作每个通道的能力非常重要。

该器件具有很多保护和诊断功能，包括热关断 (TSD)、TXD 显性超时 (DTO) 和高达 ±58V 的总线故障保护，并且定义了电源欠压或引脚悬空情况下的失效防护行为。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TCAN1046A-Q1	VSON (DMT) (14)	4.50mm x 3.00mm
	SOIC (D) (14)	8.95mm x 3.91mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

ADVANCE INFORMATION

ADVANCE INFORMATION

4 Pin Configuration and Functions

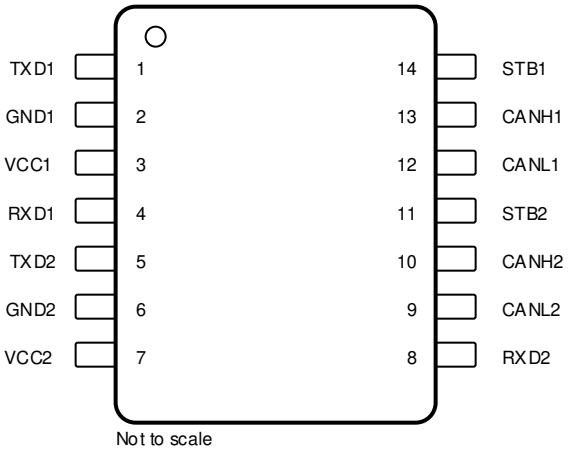


图 4-1. D Package, 14 Pin SOIC, Top View

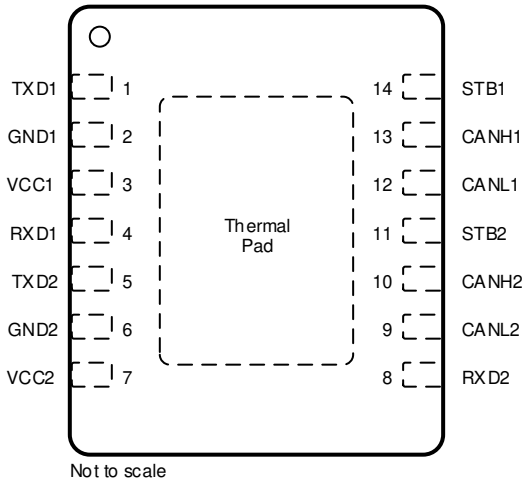


图 4-2. DMT Package, 14 Pin VSON, Top View

表 4-1. Pin Functions

Pins		Type	Description
Name	No.		
TXD1	1	Digital Input	CAN transmit data input 1, integrated pull-up
GND1	2	GND1	Ground connection, transceiver 1
V_{CC1}	3	Supply	5-V supply voltage, transceiver 1
RXD1	4	Digital Output	CAN receive data output 1, tri-state when V_{CC} < UV_{VCC}
TXD2	5	Digital Input	CAN transmit data input 2, integrated pull-up
GND2	6	GND2	Ground connection, transceiver 2
V_{CC2}	7	Supply	5-V supply voltage, transceiver 2
RXD2	8	Digital Output	CAN receive data output 2, tri-state when V_{CC} < UV_{VCC}
CANL2	9	Bus IO	Low-level CAN bus 2 input/output line
CANH2	10	Bus IO	High-level CAN bus 2 input/output line
STB2	11	Digital Input	Standby input 2 for mode control, integrated pull-up
CANL1	12	Bus IO	Low-level CAN bus 1 input/output line
CANH1	13	Bus IO	High-level CAN bus 1 input/output line
STB1	14	Digital Input	Standby input 1 for mode control, integrated pull-up
Thermal Pad (VSON only)		—	Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

5 Device and Documentation Support

5.1 Device Support

This device conforms to the following CAN standards. The core of what is needed is covered within this system specification; however, reference should be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed. However, for a full understanding of CAN including the protocol these additional sources are helpful as the scope of CAN protocol in detail is outside the scope of this physical layer (transceiver) specification.

5.1.1 Device Nomenclature

CAN Transceiver Physical Layer Standards:

- ISO 11898-2:2016 High speed medium access unit (original High Speed CAN transceiver standard)
- ISO 11898-5 High speed medium access unit with low power mode (super sets -2 standard electrically in several specs and adds the original wake up capability via the bus in low power mode).
- ISO 11898-6 High speed medium access unit with selective wake.
- ISO 8802-3: CSMA/CD – referenced for collision detection from ISO11898-2
- CAN FD 1.0 Spec and Papers
- Bosch “Configuration of CAN Bit Timing”, Paper from 6th International CAN Conference (ICC), 1999. This is repeated a lot in the DCAN IP CAN Controller spec copied into this system spec.
- GMW3122: GM requirements for HS CAN
- SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
- SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps

EMC requirements:

- HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for HS CAN

Conformance Test requirements:

- HS_TRX_Test_Spec_V_1_0: GIFT / ICT CAN test requirements for High Speed Physical Layer

5.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

5.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

5.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ADVANCE INFORMATION

5.6 术语表

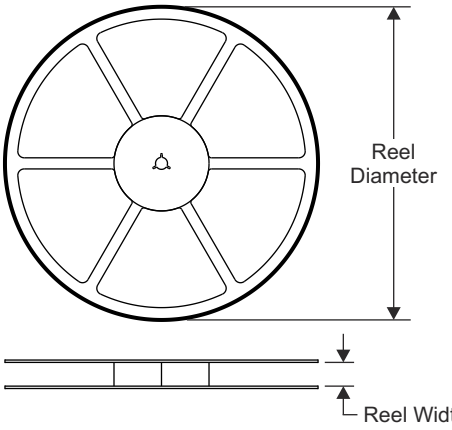
TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

Mechanical, Packaging, and Orderable Information

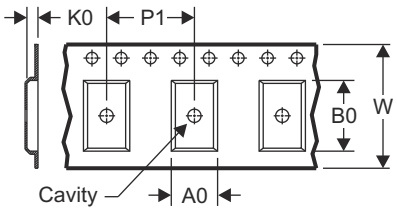
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

6.1 Tape and Reel Information

REEL DIMENSIONS

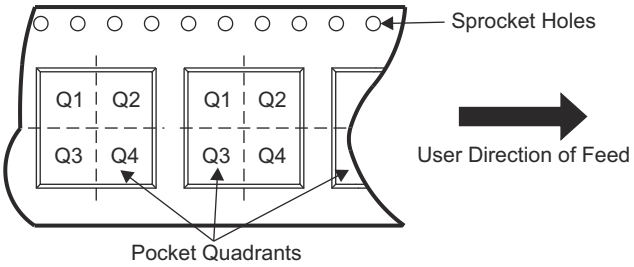


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

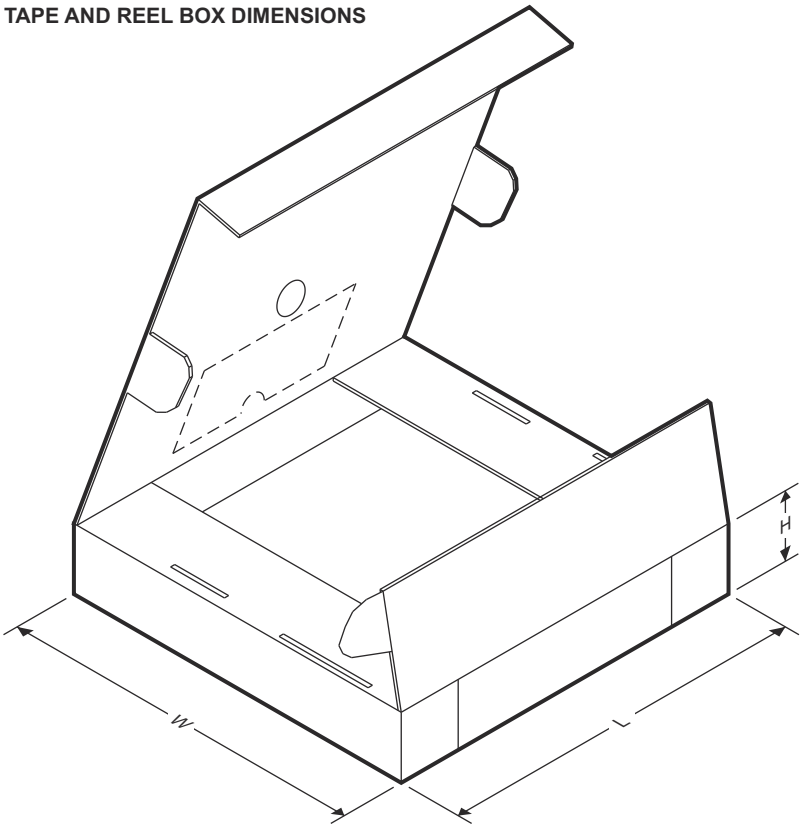


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1046ADMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.2	4.7	1.15	8.0	12.0	Q1
TCAN1046ADRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



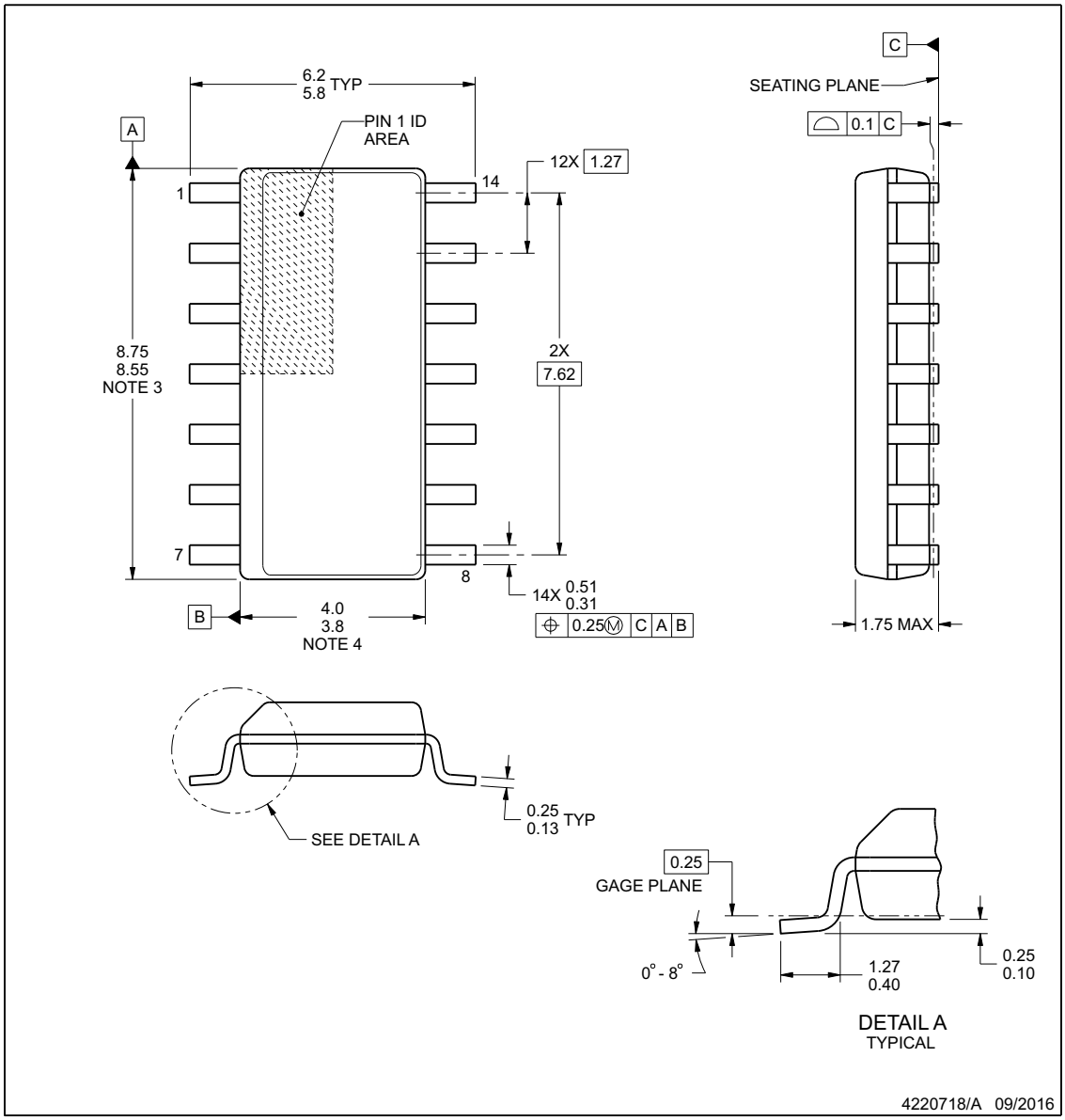
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1046ADMTRQ1	VSON	DMT	14	3000	370.0	355.0	55.0
TCAN1046ADRQ1	SOIC	D	14	2500	853.0	449.0	35.0

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

ADVANCE INFORMATION

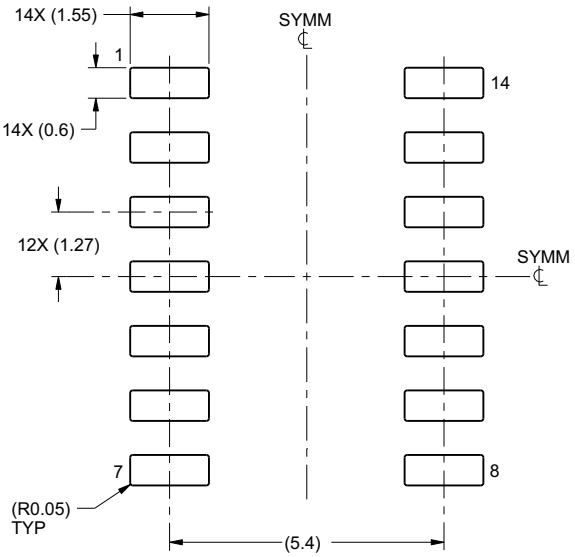
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

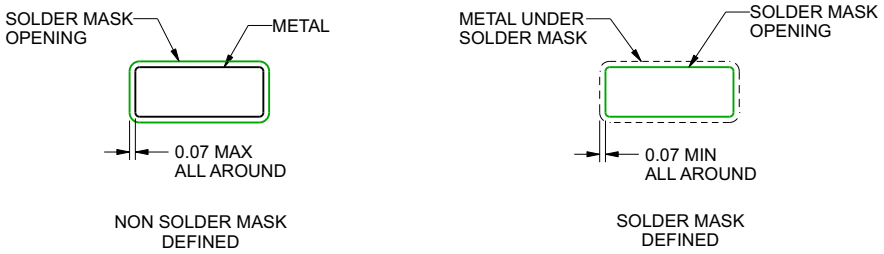
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

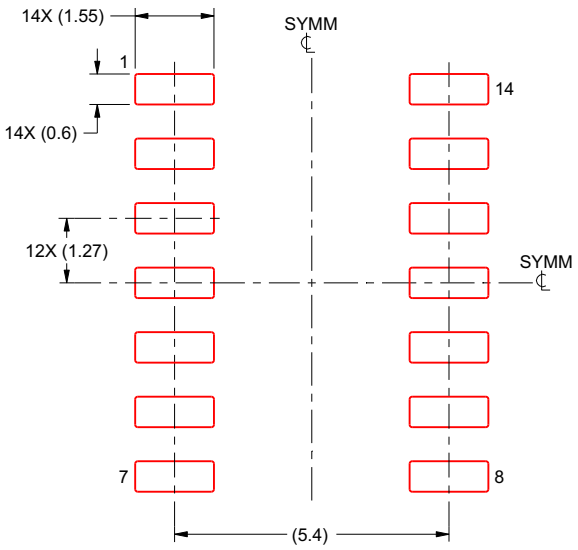
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

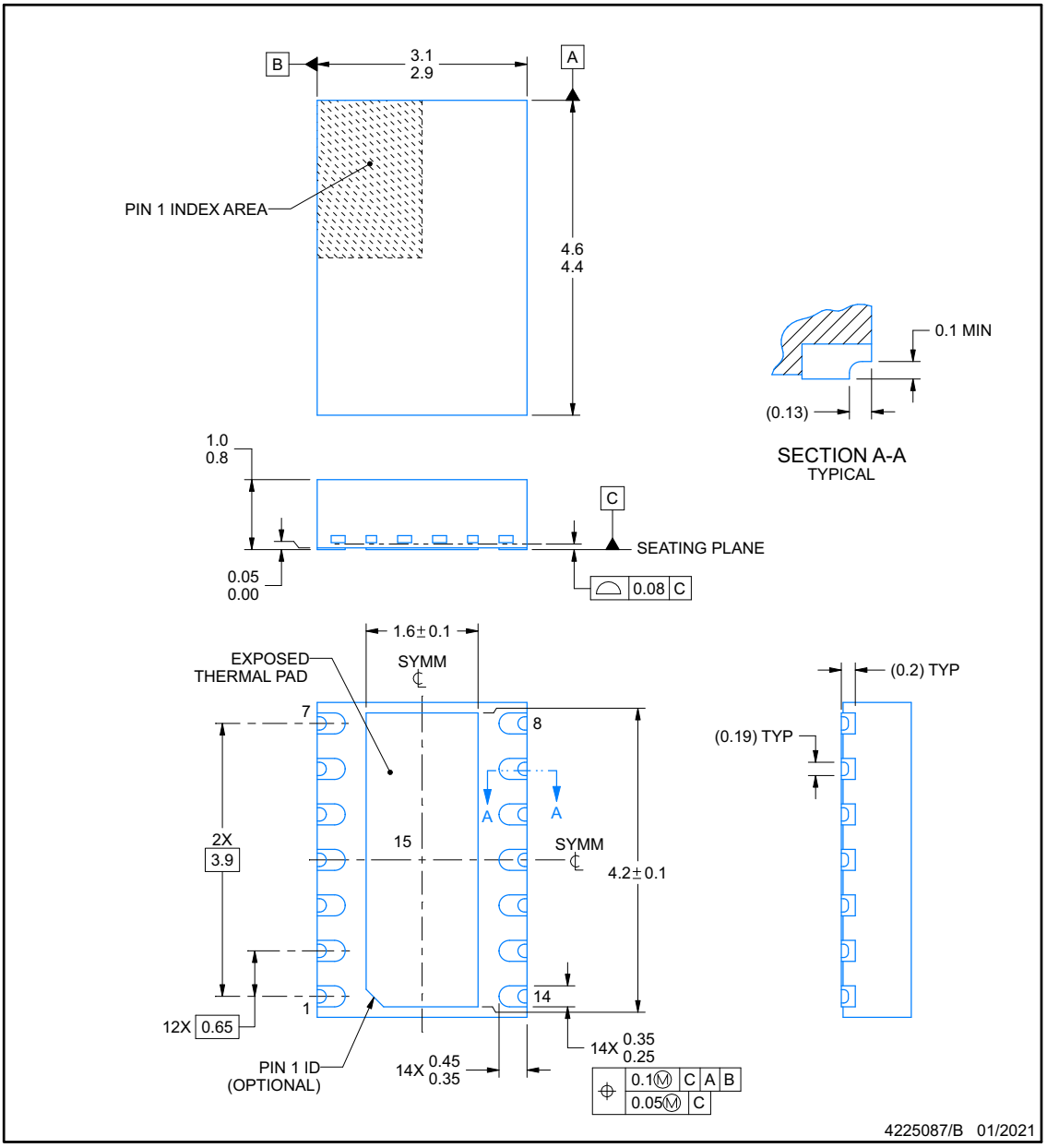
ADVANCE INFORMATION

PACKAGE OUTLINE

DMT0014B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

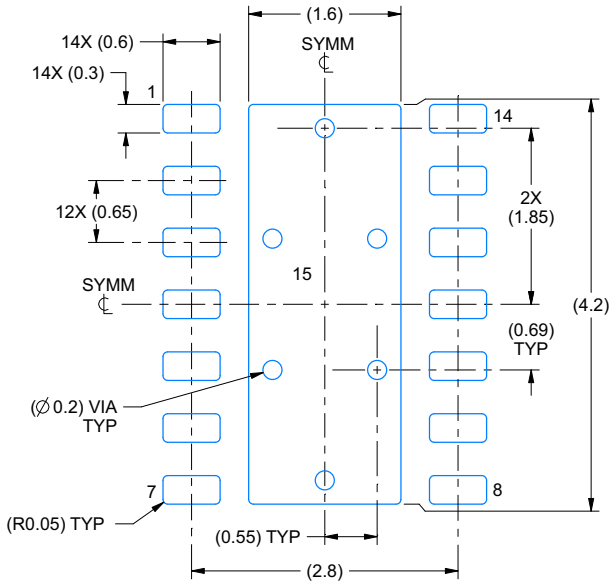
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

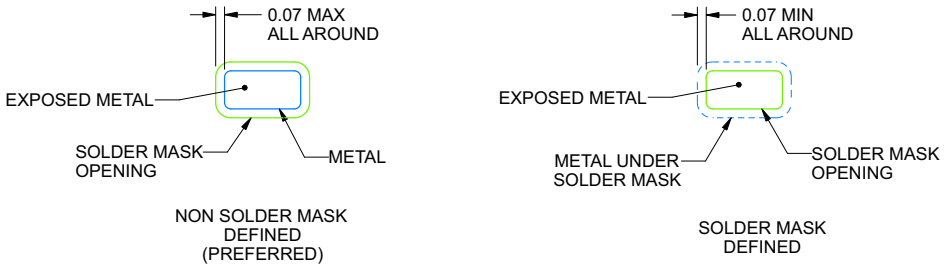
DMT0014B

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4225087/B 01/2021

NOTES: (continued)

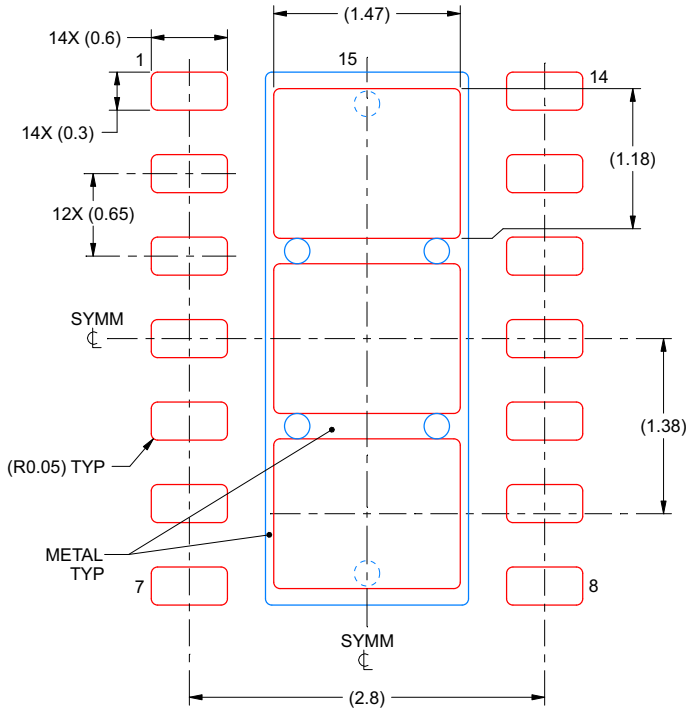
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DMT0014B — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/B 01/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1046ADMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1046A
TCAN1046ADMTRQ1.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	1046A
TCAN1046ADRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1046A
TCAN1046ADRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1046A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

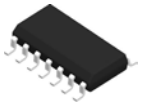
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

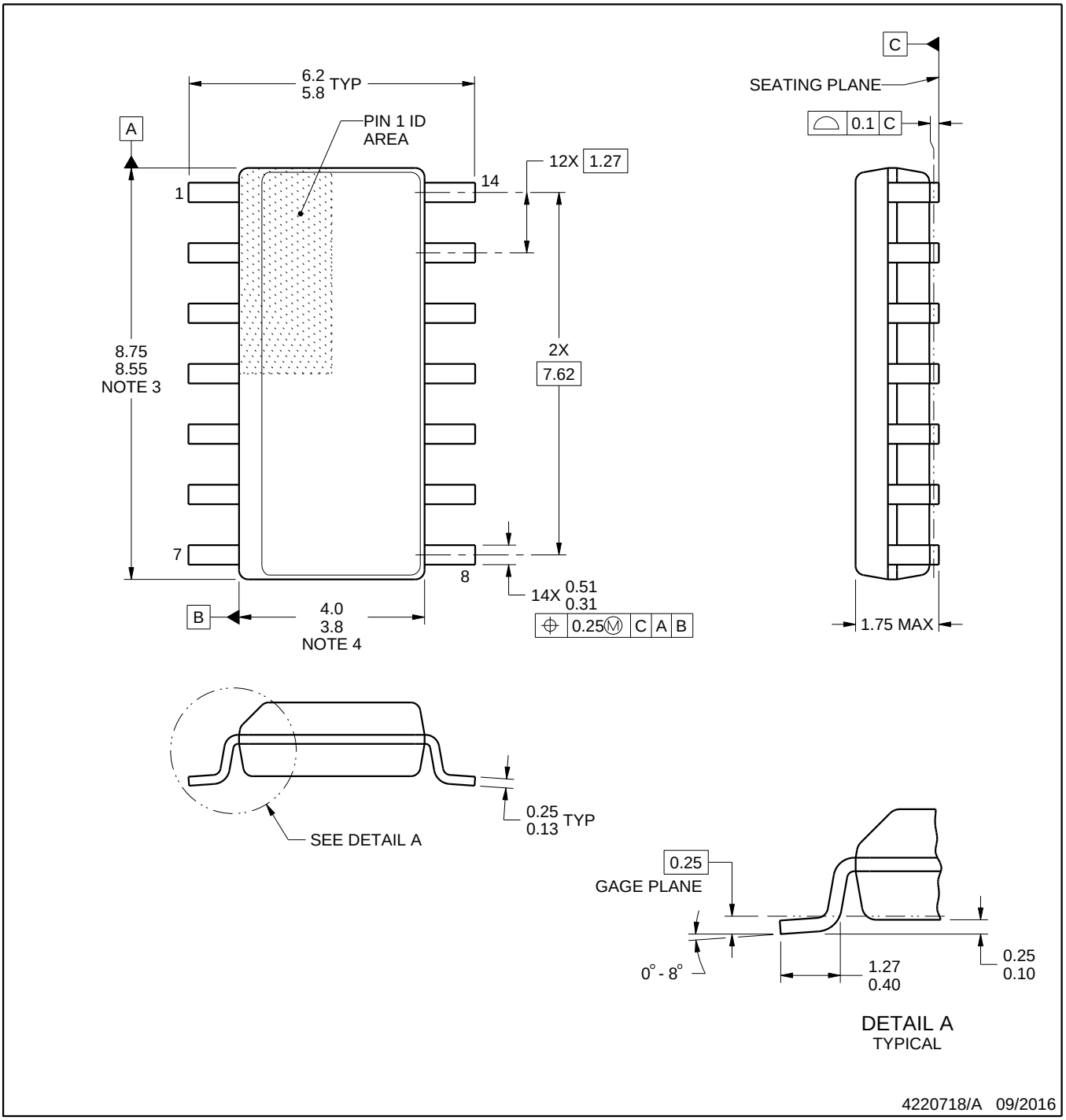


PACKAGE OUTLINE

D0014A

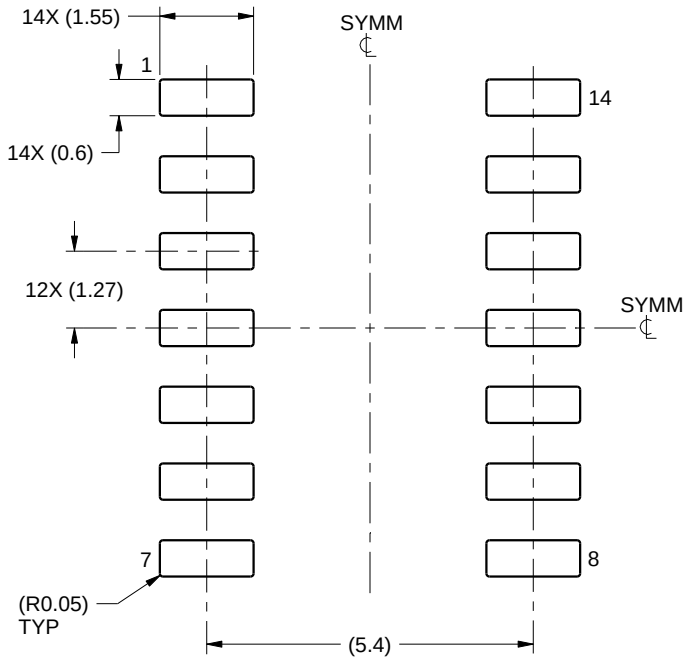
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

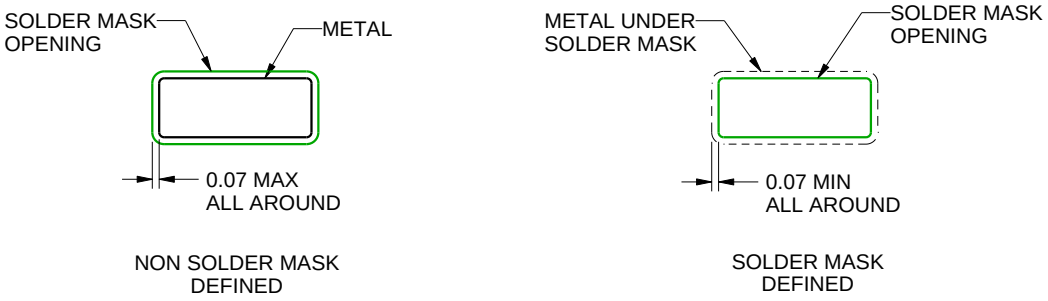


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

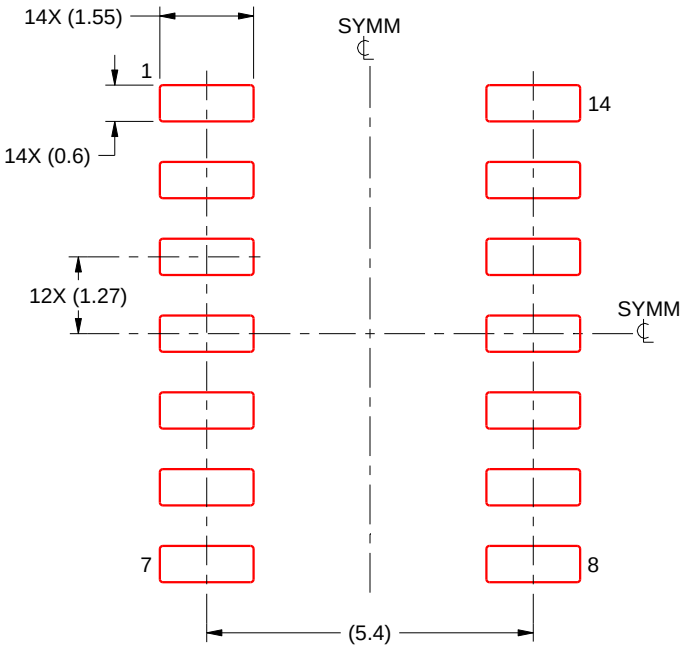
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

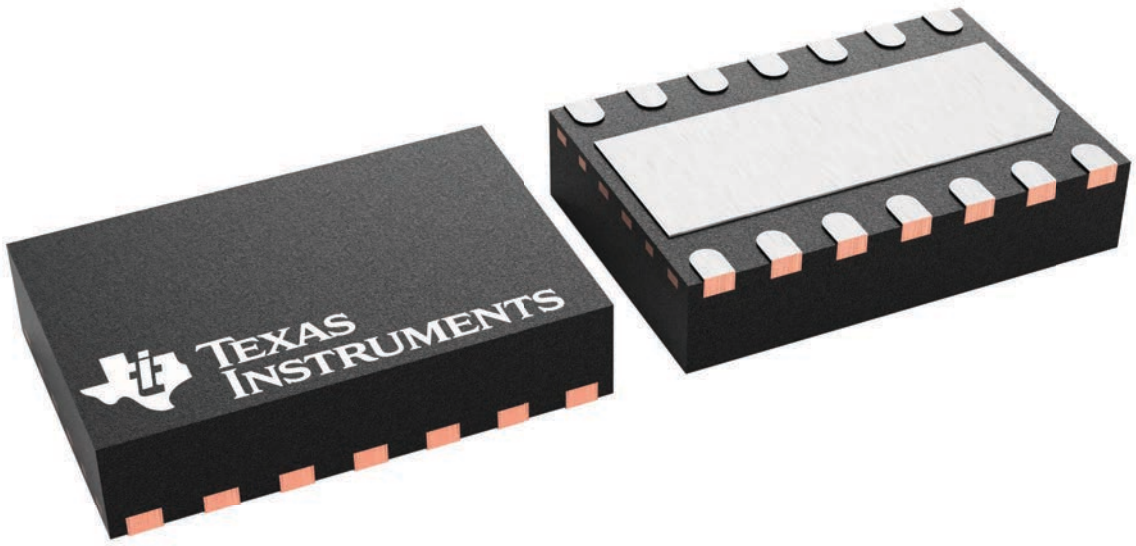
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



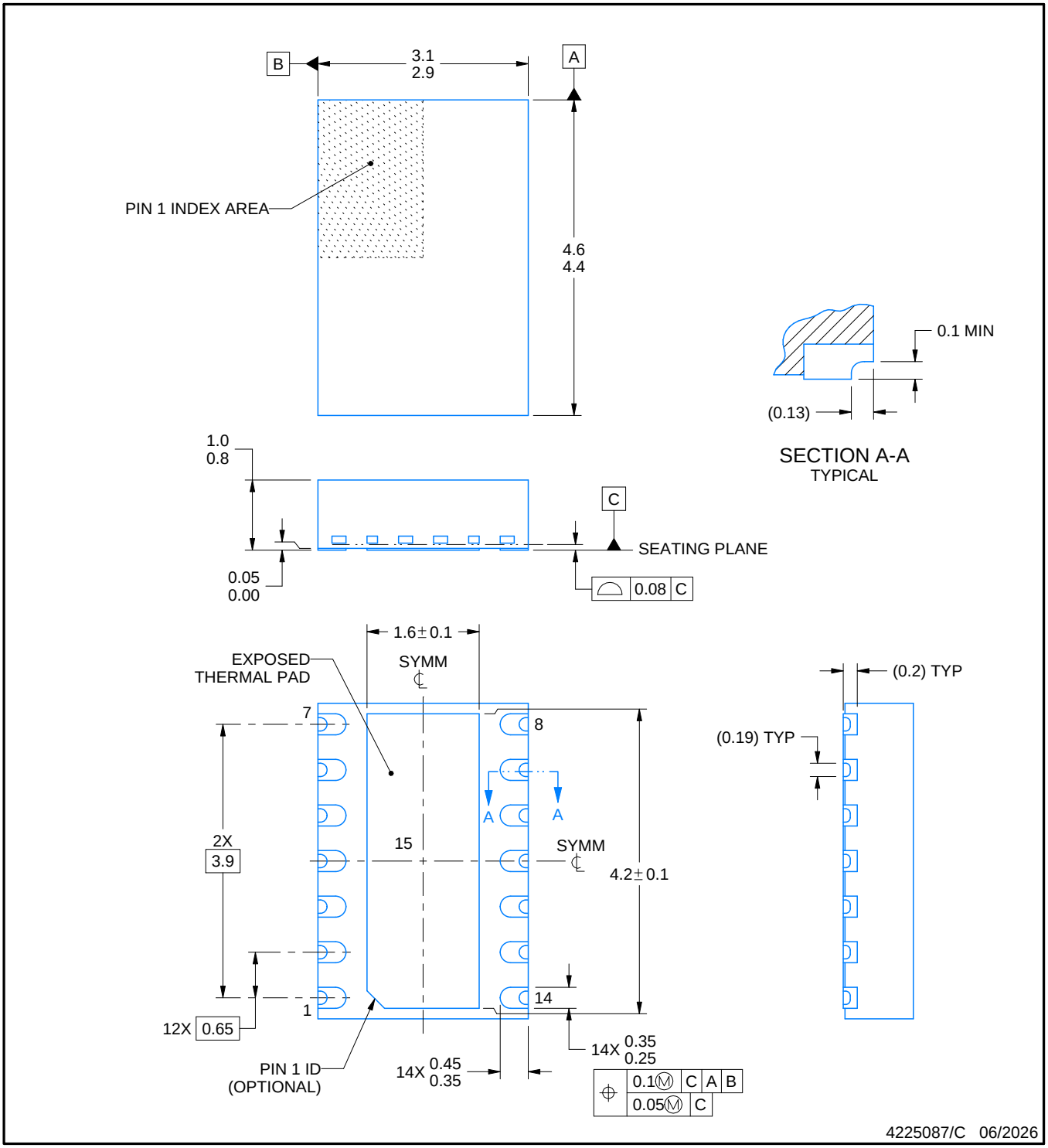
4225088/A

PACKAGE OUTLINE

DMT0014B

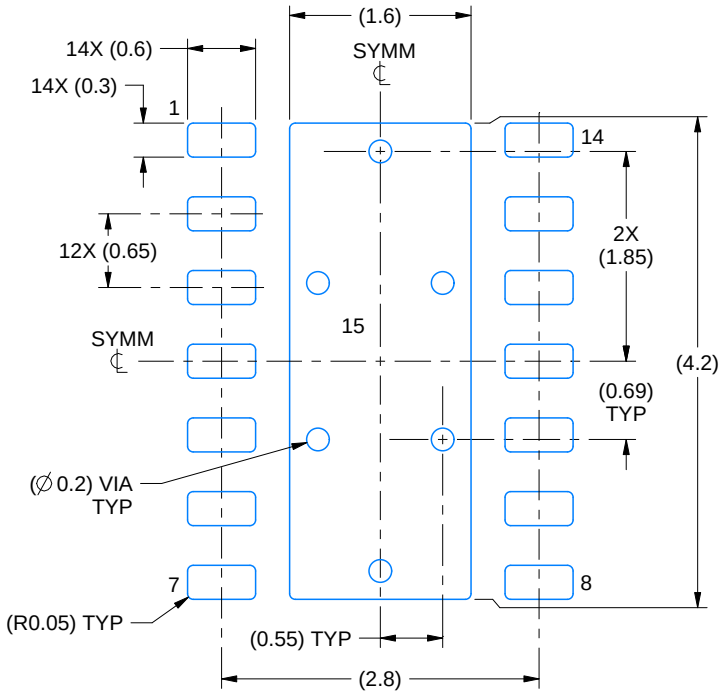
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

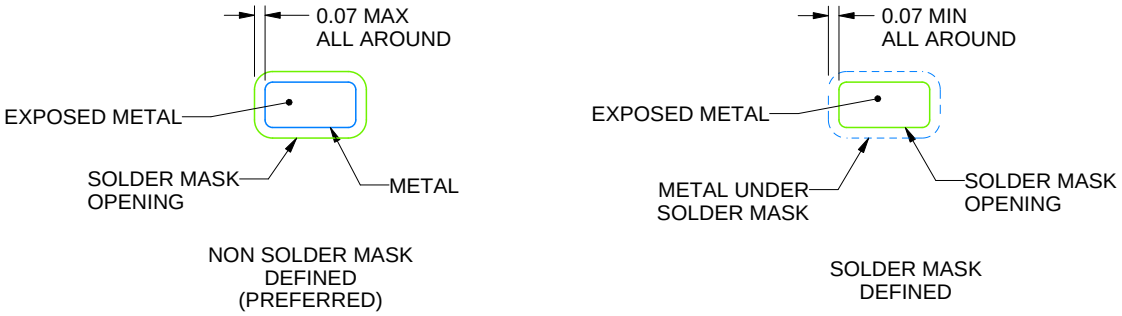


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Exposed side wall metal may vary is shape, size and quantity.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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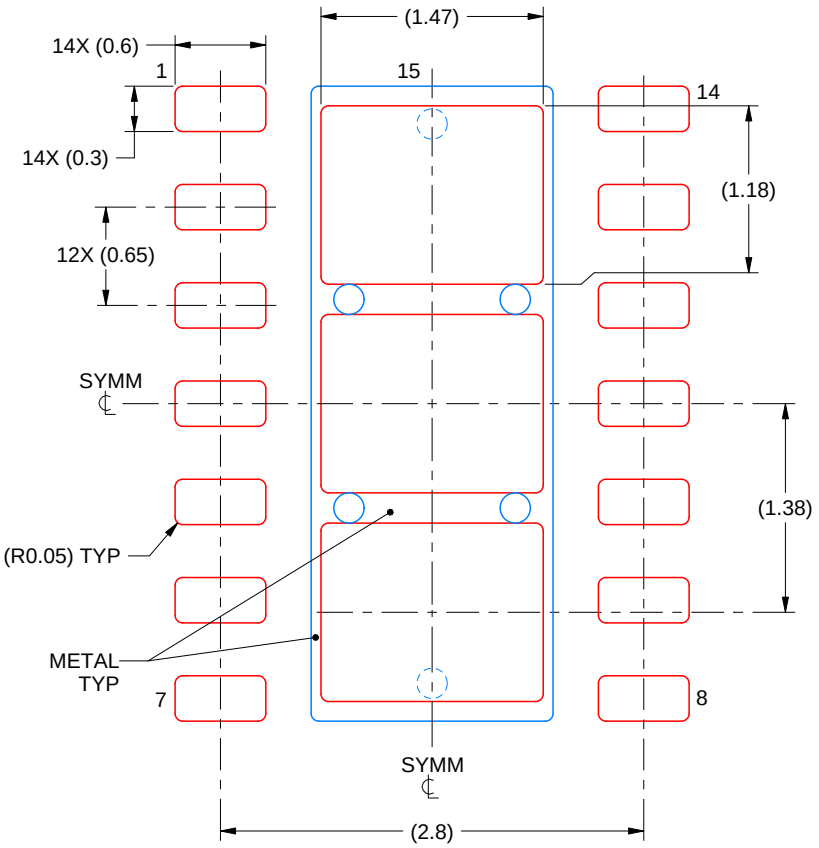
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4225087/C 06/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月