TCAN1057AEV-Q1 具有静音模式的 0 级故障保护 CAN FD 收发器

1 特性

- 符合面向汽车应用的 AEC-Q100（0 级）标准
- 符合 ISO 11898-2:2016 物理层标准要求
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 支持传统 CAN 和经优化的 CAN FD 性能（数据速率为 2、5 和 8Mbps）
  - 具有较短的对称传播延迟时间，可增加时序裕量
- I/O 电压范围支持 1.7V 至 5.5V
- 支持 12V 和 24V 电池应用
- 接收器共模输入电压：±12V
- 保护特性：
  - 总线故障保护：±58V
  - 欠压保护
  - TXD 显性超时 (DTO)
    - 数据速率低至 9.2kbps
  - 热关断保护 (TSD)
- 工作模式：
  - 正常模式
  - 静音模式
- 优化了未上电时的性能
  - 总线和逻辑引脚为高阻抗（运行总线或应用上无负载）
  - 支持热插拔：在总线和 RXD 输出上可实现上电/断电无干扰运行
- 采用 SOIC (8) 封装

2 应用

- 汽车和运输
  - 车身控制模块
  - 汽车网关
  - 高级驾驶辅助系统 (ADAS)
  - 信息娱乐系统

3 说明

TCAN1057AEV-Q1 是一款高速控制器局域网 (CAN) 收发器，符合 ISO 11898-2:2016 高速 CAN 规范的物理层要求。

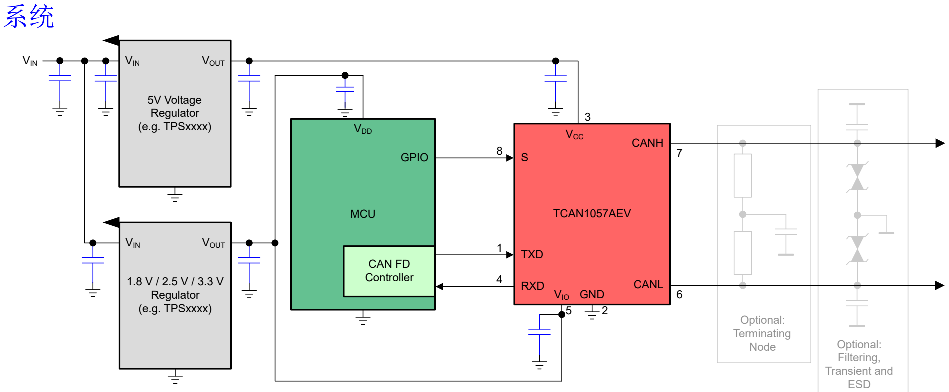
该收发器具有经认证的电磁兼容性 (EMC)，非常适合数据速率高达 5 兆位/秒 (Mbps) 的传统 CAN 和 CAN FD 网络。该器件可以在更简单的网络中实现高达 8Mbps 的速率。收发器支持两种工作模式：正常模式和静音模式。该收发器还具有多种保护和诊断功能，包括热关断 (TSD)、TXD 显性超时 (DTO) 和高达 ±58V 的总线故障保护，并且定义了电源欠压或引脚悬空情况下的失效防护行为。

收发器具有通过 V_{IO} 引脚实现的集成电平转换器，该电平转换器提供内部逻辑电平转换功能，允许将收发器 I/O 直接连接到 1.8V、2.5V、3.3V 或 5V 逻辑电平。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
TCAN1057AEV-Q1	SOIC (D) (8)	4.90mm x 3.91mm

(1) 如需完整的器件型号，请参阅数据表末尾的可订购产品附录。



简化版原理图

English Data Sheet: SLLSFO0

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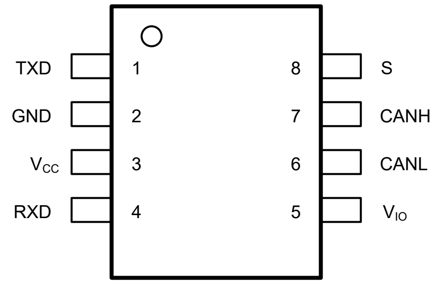
4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2021	*	Initial Release

5 Pin Configuration and Functions



Not to scale

图 5-1. D (SOIC) Package, 8-Pin, Top View

表 5-1. Pin Functions

Pins		Type	Description
No.	**Name**		
1	TXD	Digital Input	CAN transmit data input, integrated pull-up
2	GND	GND	Ground connection
3	V_{CC}	Supply	5-V supply voltage
4	RXD	Digital Output	CAN receive data output, tri-state when powered off
5	V_{IO}	Supply	I/O supply voltage
6	CANL	Bus IO	Low-level CAN bus input/output line
7	CANH	Bus IO	High-level CAN bus input/output line
8	S	Digital Input	Silent mode control input, integrated pull-up

6 Specifications

6.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN Bus I/O voltage	–58	58	V
V_{DIFF}	Max differential voltage between CANH and CANL	–45	45	V
V_{Logic_Input}	Logic input terminal voltage	–0.3	6	V
V_{RXD}	RXD output terminal voltage range	–0.3	6	V
$I_{O(RXD)}$	RXD output current	–8	8	mA
T_J	Junction temperature	–40	175	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	HBM classification level 3A for all pins	±4000	V
			HBM classification level 3B for global pins CANH and CANL with respect to GND	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings Table — IEC Specifications

				VALUE	UNIT
V_{ESD}	System level electrostatic discharge	CAN bus terminals (CANH and CANL) to GND	Unpowered contact discharge per ISO10605 [1]	±8000	V
			SAE J2962-2 per ISO 10605 Powered contact Discharge [2]	±8000	V
			SAE J2962-2 per ISO 10605 Powered air Discharge [2]	±15000	V
V_{Tran}	Transient voltage per ISO 7637-2[3]		Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	Transient voltage per ISO 7637-3[4]		DCC slow transient pulse	±30	V

(1) Tested according to IEC 62228-3:2019 CAN Transceivers.
(2) Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM approved independent third party, EMC report available upon request.
(3) Tested according to IEC 62228-3:2019 CAN Transceivers.
(4) Tested according to SAE J2962-2.

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IO}	Supply voltage for I/O level shifter	1.7		5.5	V
$I_{OH(RXD)}$	RXD terminal high-level output current	–1.5			mA
$I_{OL(RXD)}$	RXD terminal low-level output current			1.5	mA
T_A	Operating ambient temperature	-40		150	℃

6.5 Thermal Characteristics

THERMAL METRIC[1]		TCAN1057AEV-Q1 D (SOIC)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.5	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.9	℃/W
Ψ_{JT}	Junction-to-top characterization parameter	19.3	℃/W
Ψ_{JB}	Junction-to-board characterization parameter	70.2	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	--	℃/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Supply Characteristics

Over recommended operating conditions with T_A = -40℃ to 150℃ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current Normal mode	Dominant	TXD = 0 V, S = 0 V, R_L = 60 Ω, C_L = open; See 图 7-1		45	70	mA
			TXD = 0 V, S = 0 V, R_L = 50 Ω, C_L = open; See 图 7-1		49	80	mA
		Recessive	TXD = V_{IO}, S = 0 V, R_L = 50 Ω, C_L = open; See 图 7-1		4.5	7.5	mA
		Dominant with bus fault	TXD = 0 V, S = 0 V, CANH = CANL = ±25 V, R_L = open, C_L = open; See 图 7-1			130	mA
	Supply current Silent mode		TXD = S = V_{IO}, R_L = 50 Ω, C_L = open; See 图 7-1			2.1	mA
I_{IO}	I/O supply current Normal mode	Dominant	S = 0 V, TXD = 0 V RXD floating		125	300	µA
		Recessive	TXD = V_{IO} , S = 0 V RXD floating		25	48	µA
UV_{CC}	Rising undervoltage detection on V_{CC} for protected mode				4.2	4.4	V
	Falling undervoltage detection on V_{CC} for protected mode			3.5	4	4.25	V
$V_{HYS(UVCC)}$	Hysteresis voltage on UV_{CC}				200		mV
UV_{VIO}	Rising undervoltage detection on V_{IO}				1.56	1.65	V
	Falling undervoltage detection on V_{IO}			1.4	1.51	1.59	V
$V_{HYS(UVIO)}$	Hysteresis voltage on UV_{IO}				40		mV

6.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Average power dissipation Normal mode	V_{CC} = 5 V, V_{IO} = 1.8 V, T_J= 27°C, R_L = 60 Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		95		mW
		V_{CC} = 5 V, V_{IO} = 3.3 V, T_J= 27°C, R_L = 60 Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		95		mW
		V_{CC} = 5 V, V_{IO} = 5 V, T_J= 27°C, R_L = 60 Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		95		mW
		V_{CC} = 5.5 V, V_{IO} = 1.8 V, T_A= 150°C, R_L = 60 Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		120		mW
		V_{CC} = 5.5 V, V_{IO} = 3.3 V, T_A= 150°C, R_L = 60 Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		120		mW
		V_{CC} = 5.5 V, V_{IO} = 5 V, T_A= 150°C, R_L = 60 Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		120		mW
T_{TSD}	Thermal shutdown temperature		175	195	210	°C
$T_{TSD(HYS)}$	Thermal shutdown hysteresis			12		°C

6.8 Electrical Characteristics

Over recommended operating conditions with T_A = -40℃ to 150℃ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{O(DOM)}$	Dominant output voltage Normal mode	CANH	S = 0 V, TXD = 0 V 50 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = open; See 图 7-2	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(REC)}$	Recessive output voltage Normal or silent mode	CANH and CANL	S = 0 V, TXD = V_{IO} R_L = open (no load), R_{CM} = open See 图 7-2	2	0.5 V_{CC}	3	V
V_{SYM}	Driver symmetry $(V_{O(CANH)} + V_{O(CANL)})/V_{CC}$		S = 0 V, TXD = 250 kHz, 1 MHz, 2.5 MHz R_L = 60 Ω, C_{SPLIT} = 4.7 nF, C_L = open, R_{CM} = open; See 图 7-2 and 图 9-2	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry $(V_{CC} - V_{O(CANH)} - V_{O(CANL)})$		S = 0 V R_L = 60 Ω, C_L = open; See 图 7-2	–400		400	mV
$V_{OD(DOM)}$	Differential output voltage Normal mode Dominant	CANH - CANL	S = 0 V, TXD = 0 V 50 Ω ≤ R_L ≤ 65 Ω, C_L = open; See 图 7-2	1.5		3	V
			S = 0 V, TXD = 0 V 45 Ω ≤ R_L ≤ 70 Ω, C_L = open; See 图 7-2	1.4		3.3	V
			S = 0 V, TXD = 0 V R_L = 2240 Ω, C_L = open; See 图 7-2	1.5		5	V
$V_{OD(REC)}$	Differential output voltage Normal mode Recessive	CANH - CANL	S = 0 V, TXD = V_{IO} R_L = 60 Ω, C_L = open; See 图 7-2	–120		12	mV
			S = 0 V, TXD = V_{IO} R_L = open, C_L = open; See 图 7-2	–50		50	mV

6.8 Electrical Characteristics (continued)

Over recommended operating conditions with T_A = -40℃ to 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OS(SS\_DOM)}$	Short-circuit steady-state output current, dominant Normal mode	S = 0 V, TXD = 0 V $V_{(CANH)}$ = -15 V to 40 V, CANL = open; See 图 7-7	–115			mA
		S = 0 V, TXD = 0 V $V_{(CAN\_L)}$ = -15 V to 40 V, CANH = open; See 图 7-7			115	mA
$I_{OS(SS\_REC)}$	Short-circuit steady-state output current, recessive Normal mode	S = 0 V, TXD = V_{IO} –27 V ≤ V_{BUS} ≤ 32 V, where V_{BUS} = CANH = CANL; See 图 7-7	–5		5	mA
Receiver Electrical Characteristics						
V_{IT}	Input threshold voltage Normal and silent mode	S = 0 V, -12 V ≤ V_{CM} ≤ 12 V; See 图 7-3 and 表 8-5	500		900	mV
V_{DOM}	Dominant state differential input voltage range Normal and silent mode	S = 0 V, -12 V ≤ V_{CM} ≤ 12 V; See 图 7-3 and 表 8-5	0.9		9	V
V_{REC}	Recessive state differential input voltage range Normal and silent mode	S = 0 V, -12 V ≤ V_{CM} ≤ 12 V; See 图 7-3 and 表 8-5	-4		0.5	V
V_{HYS}	Hysteresis voltage for input threshold Normal mode	S = 0 V, -12 V ≤ V_{CM} ≤ 12 V; See 图 7-3 and 表 8-5		115		mV
V_{CM}	Common-mode range Normal and silent mode	See 图 7-3 and 表 8-5	–12		12	V
$I_{LKG(IOFF)}$	Unpowered bus input leakage current	CANH = CANL = 5 V, V_{CC} = V_{IO} = GND			5	μA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{IO}			20	pF
C_{ID}	Differential input capacitance				10	pF
R_{ID}	Differential input resistance	TXD = V_{IO}, S = 0 V, -12 V ≤ V_{CM} ≤ 12 V	40		90	kΩ
R_{IN}	Single-ended input resistance (CANH or CANL)		20		45	kΩ
$R_{IN(M)}$	Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	$V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5 V	–1		1	%
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage		0.7 V_{IO}			V
V_{IL}	Low-level input voltage				0.3 V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	μA
I_{IL}	Low-level input leakage current	TXD = 0 V V_{CC}= V_{IO} = 5.5 V	–200	-100	–20	μA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V V_{CC}= V_{IO} = 0 V	–1	0	1	μA
C_I	Input capacitance	V_{IN} = 0.4×sin(2×π×2×10^6×t)+2.5 V		5		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level output voltage	I_O = –1.5 mA See 图 7-3	0.8 V_{IO}			V
V_{OL}	Low-level output voltage	I_O = 1.5mA See 图 7-3			0.2 V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5 V V_{CC} = V_{IO} = 0 V	–1	0	1	μA
S Terminal (Silent Mode Input)						
V_{IH}	High-level input voltage		0.7 V_{IO}			V
V_{IL}	Low-level input voltage				0.3 V_{IO}	V
I_{IH}	High-level input leakage current	V_{CC} = V_{IO} = S = 5.5 V	–2		2	μA
I_{IL}	Low-level input leakage current	S = 0 V V_{CC} = V_{IO} = 5.5 V,	–20		–2	μA
$I_{LKG(OFF)}$	Unpowered leakage current	S = 5.5V V_{CC} = V_{IO} = 0 V	–1	0	1	μA

6.9 Switching Characteristics

Over recommended operating conditions with T_A = -40℃ to 150℃ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay Driver input (TXD) to receiver output (RXD), recessive to dominant	S = 0 V, V_{IO} = 2.8 V to 5.5 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See 图 7-4		125	210	ns
$t_{PROP(LOOP1)}$	Total loop delay Driver input (TXD) to receiver output (RXD), recessive to dominant	S = 0 V, V_{IO} = 1.7 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See 图 7-4		165	255	ns
$t_{PROP(LOOP2)}$	Total loop delay Driver input (TXD) to receiver output (RXD), dominant to recessive	S = 0 V, V_{IO} = 2.8 V to 5.5 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See 图 7-4		150	210	ns
$t_{PROP(LOOP2)}$	Total loop delay Driver input (TXD) to receiver output (RXD), dominant to recessive	S = 0 V, V_{IO} = 1.7 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See 图 7-4		180	255	ns
t_{MODE}	Mode change time, from normal to silent or from silent to normal	See 图 7-5			20	μs
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	S = 0 V R_L = 60 Ω, C_L = 100 pF; See 图 7-2		80		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			70		ns
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)			14		ns
t_R	Differential output signal rise time			25		ns
t_F	Differential output signal fall time			50		ns
t_{TXD_DTO}	Dominant timeout	S = 0 V R_L = 60 Ω, C_L = 100 pF; See 图 7-6	1.2		4.0	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)	S = 0 V $C_{L(RXD)}$ = 15 pF; See 图 7-3		81		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)			66		ns
t_R	RXD output signal rise time			10		ns
t_F	RXD output signal fall time			10		ns
FD Timing Characteristics						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 500 ns	S = 0 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$; See 图 7-4	450		525	ns
	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 200 ns		160		205	ns
	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 125 ns[(1)]		85		130	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins $t_{BIT(TXD)}$ = 500 ns		410		540	ns
	Bit time on RXD output pins $t_{BIT(TXD)}$ = 200 ns		130		210	ns
	Bit time on RXD output pins $t_{BIT(TXD)}$ = 125 ns[(1)]		75		135	ns
Δt_{REC}	Receiver timing symmetry $t_{BIT(TXD)}$ = 500 ns		-50		20	ns
	Receiver timing symmetry $t_{BIT(TXD)}$ = 200 ns		-40		10	ns
	Receiver timing symmetry $t_{BIT(TXD)}$ = 125 ns[(1)]		-40		10	ns

(1) Measured during characterization and not an ISO 11898-2:2016 parameter.

7 Parameter Measurement Information

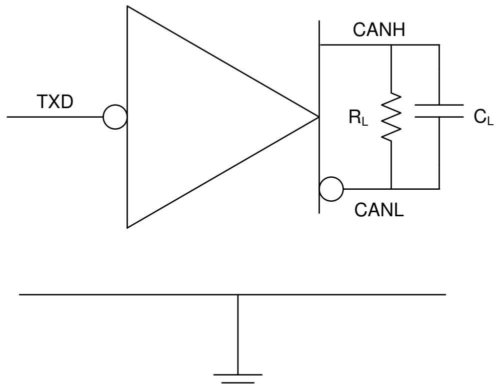


图 7-1. I_{CC} Test Circuit

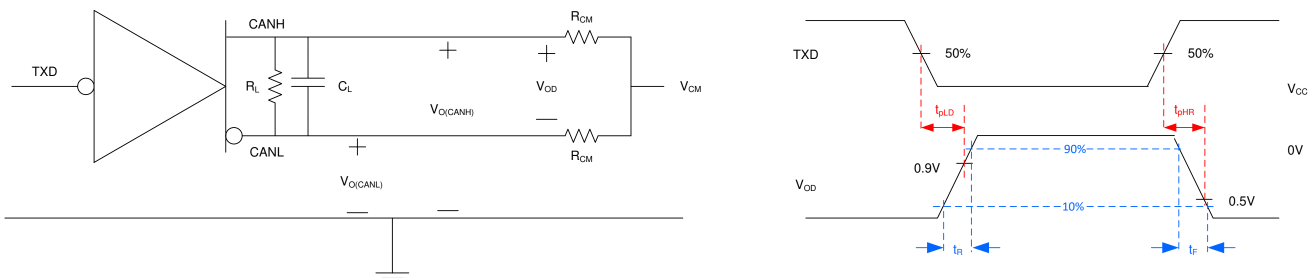


图 7-2. Driver Test Circuit and Measurement

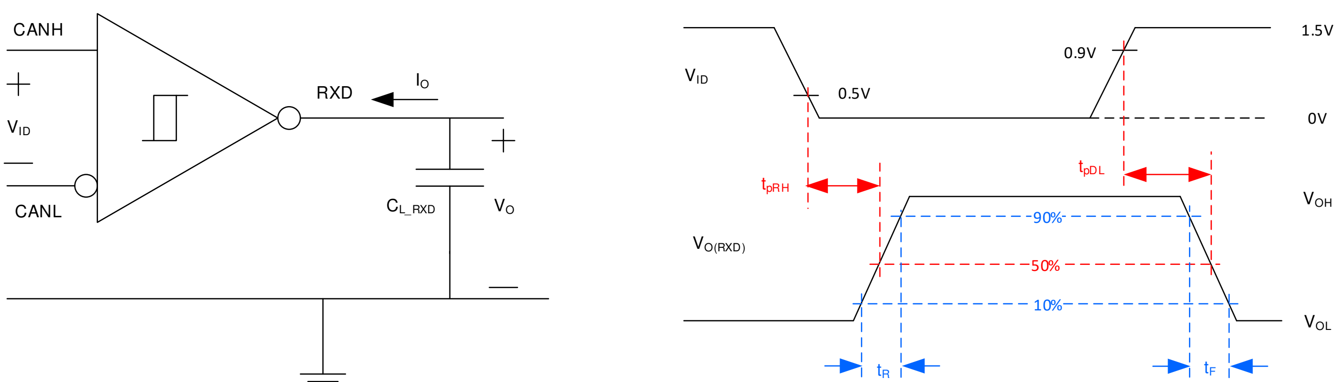


图 7-3. Receiver Test Circuit and Measurement

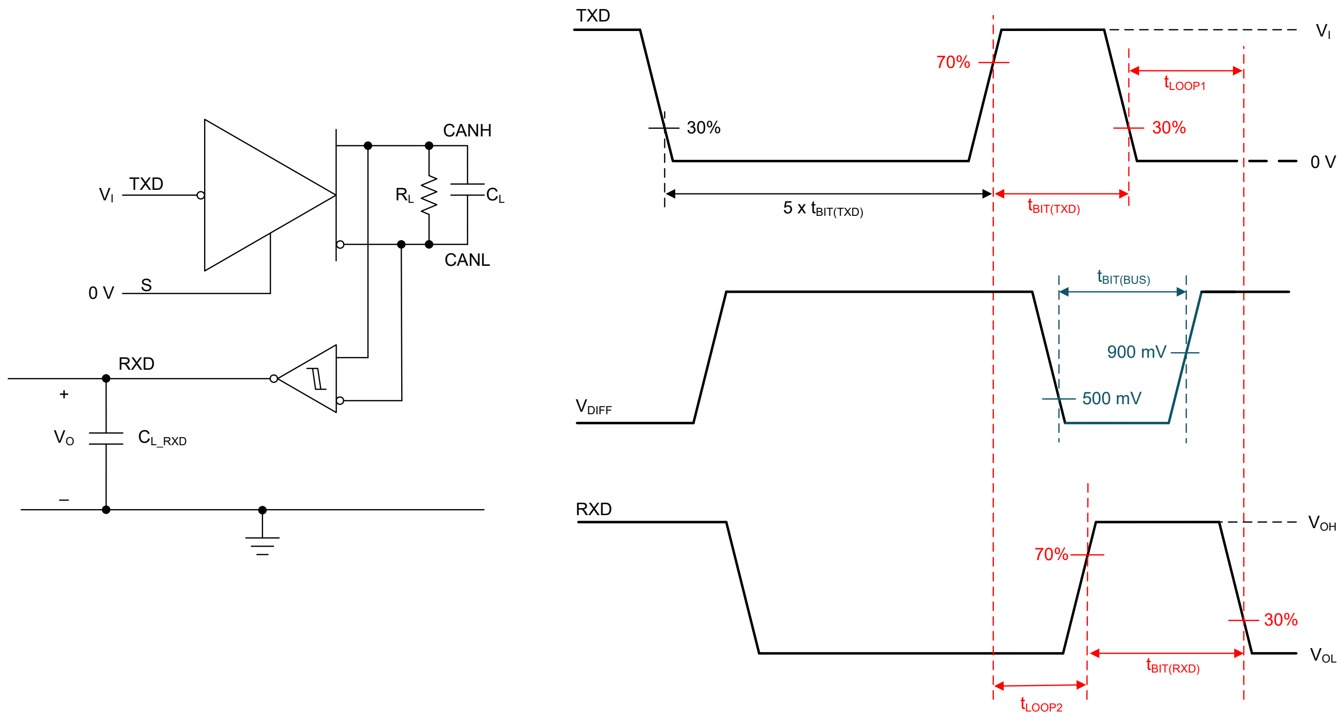


图 7-4. Transmitter and Receiver Timing Test Circuit and Measurement

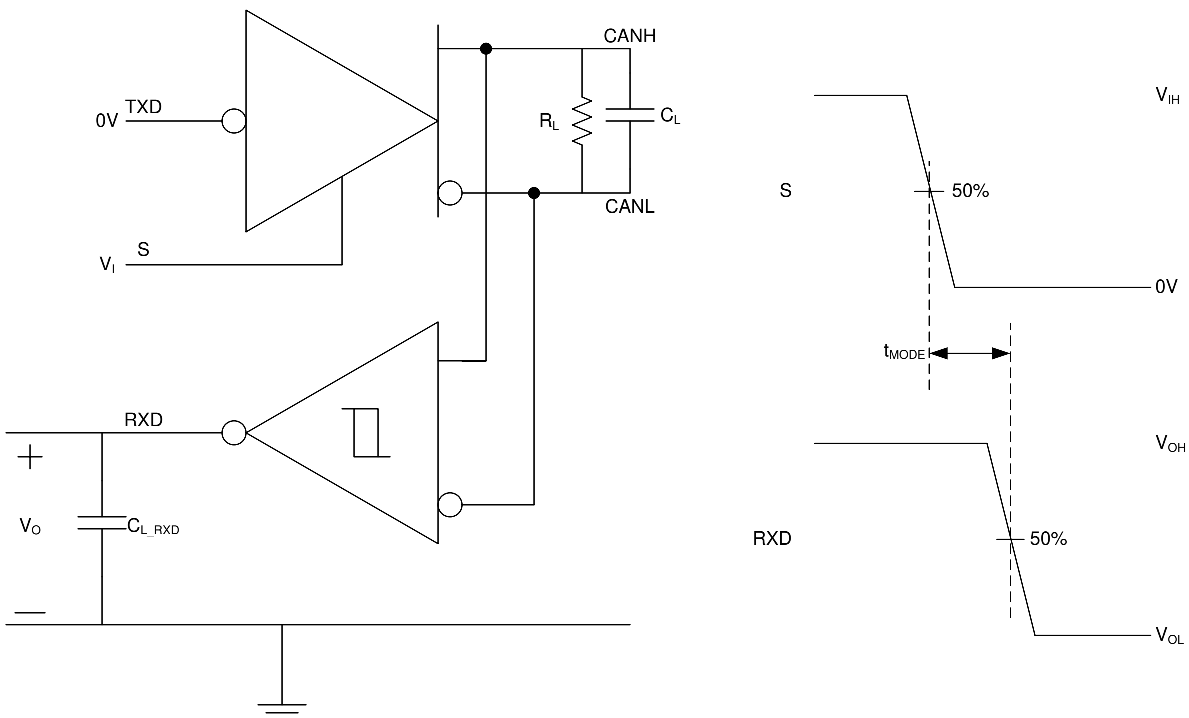


图 7-5. t_{MODE} Test Circuit and Measurement

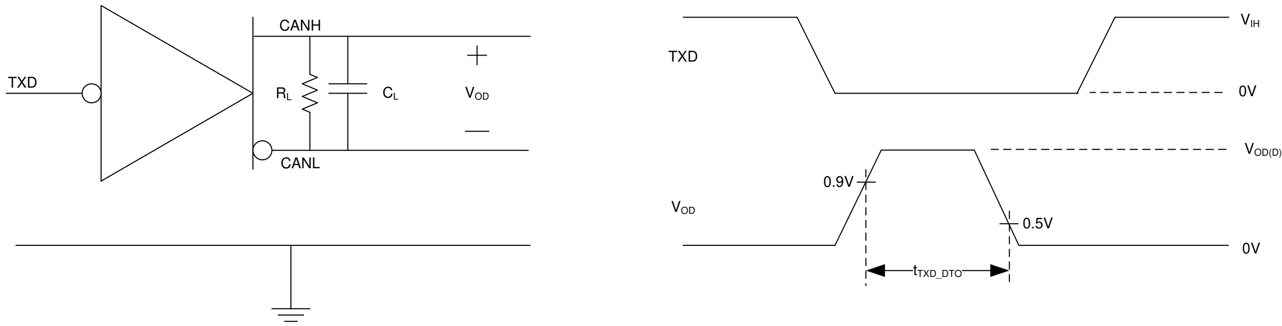


图 7-6. TXD Dominant Timeout Test Circuit and Measurement

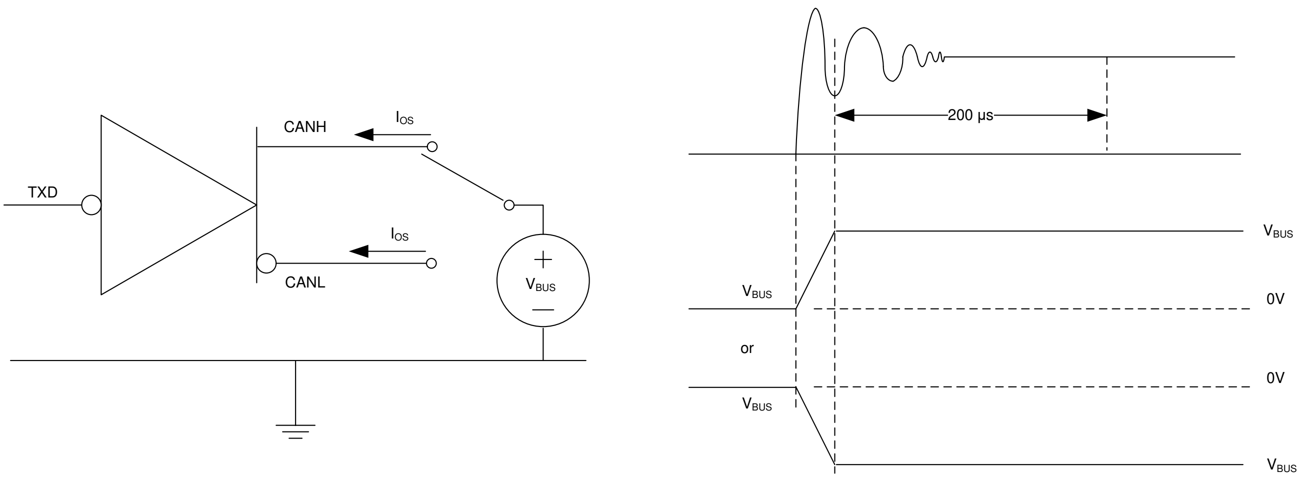


图 7-7. Driver Short-Circuit Current Test and Measurement

8 Detailed Description

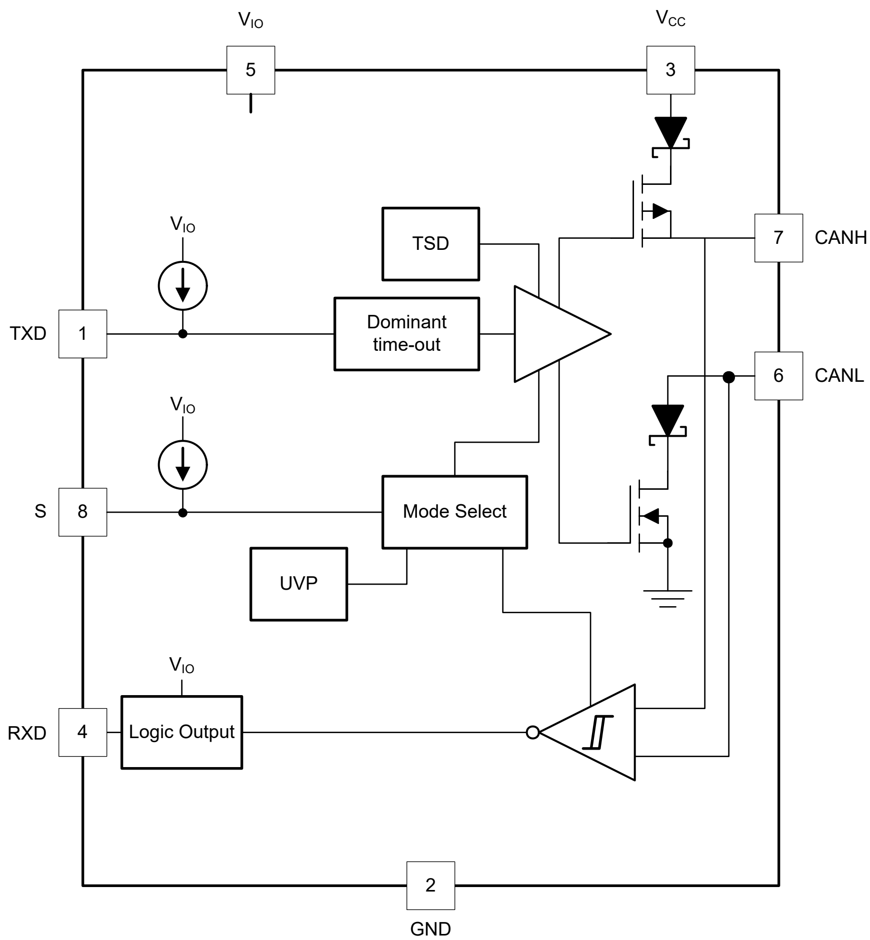
8.1 Overview

The TCAN1057AEV-Q1 meets or exceeds the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The device has been certified to the requirements of ISO 11898-2:2016 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceiver provides a number of different protection features making it ideal for the stringent automotive system requirements while also supporting CAN FD data rates up to 8 Mbps.

The device supports the following CAN standards:

- CAN transceiver physical layer standards:
  - ISO 11898-2:2016 High speed medium access unit
  - ISO 11898-5:2007 High speed medium access unit with low-power mode
  - SAE J2284-1: High Speed CAN (HSC) for Vehicle Applications at 125 kbps
  - SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
  - SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps
  - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 2 Mbps
  - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 5 Mbps
- EMC requirements:
  - IEC 62228-3 EMC evaluation of transceivers - CAN transceivers
  - SAE J2962-2 Communication Transceivers Qualification Requirements – CAN
- Conformance Test requirements:
  - ISO 16845-2 Road vehicles – Controller area network (CAN) conformance test plan Part 2: High-speed medium access unit conformance test plan

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Pin Description

8.3.1.1 TXD

The TXD input is a logic-level signal from a CAN controller to the transceiver, and is referenced to V_{IO} .

8.3.1.2 GND

GND is the ground pin of the transceiver, it must be connected to the PCB ground.

8.3.1.3 V_{CC}

V_{CC} provides the 5-V power supply to the CAN transceiver.

8.3.1.4 RXD

The RXD output is a logic-level signal from the transceiver to the CAN controller, referenced to V_{IO}. RXD is only driven once V_{IO} is present.

8.3.1.5 V_{IO}

The V_{IO} pin is the input source for the integrated level shifter which provides the transceiver I/O voltage. The V_{IO} pin should be connected to the controller's I/O voltage source.

8.3.1.6 CANH and CANL

These are the CAN high and CAN low differential bus pins. These pins are connected to the CAN transmitter and receiver internally.

8.3.1.7 S (Silent)

The S pin is an input pin used for silent mode control of the transceiver. The S pin can be supplied from either the controller or from a static system voltage source. If normal mode is the only intended mode of operation then the S pin can be tied directly to system GND using a pull-down resistor. If silent mode is the only intended mode of operation than the S pin can be tied directly to a static system voltage source using a pull-up resistor.

8.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See 图 8-1.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ through the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes can transmit a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

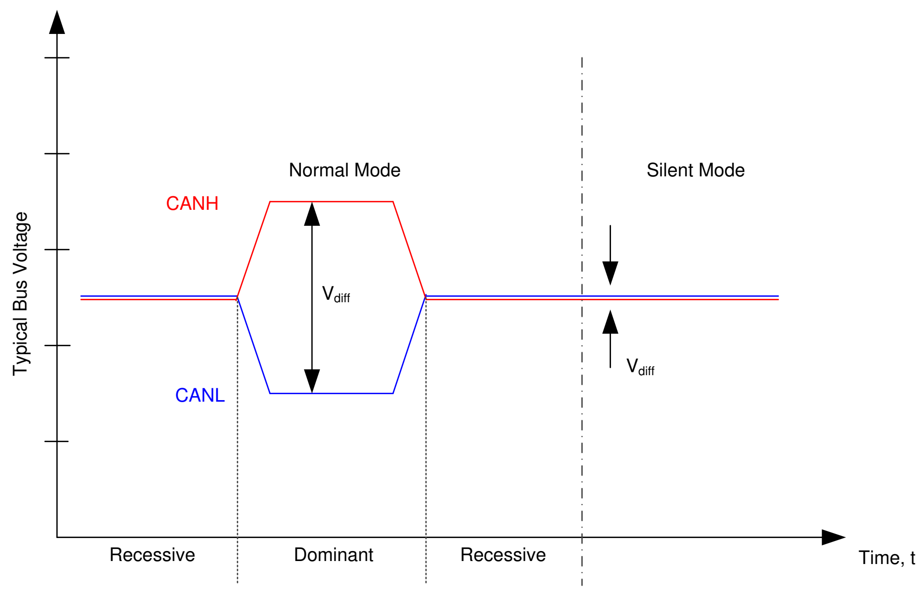


图 8-1. Bus States

8.3.3 TXD Dominant Timeout (DTO)

During normal mode, which is the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, therefore clearing the dominant time out. The receiver remains active and biased to $V_{CC}/2$ and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. To calculate the minimum transmitted data rate use 方程式 1.

$$\text{Minimum Data Rate} = 11\text{ bits} / t_{TXD\_DTO} = 11\text{ bits} / 1.2\text{ ms} = 9.2\text{ kbps} \quad (1)$$

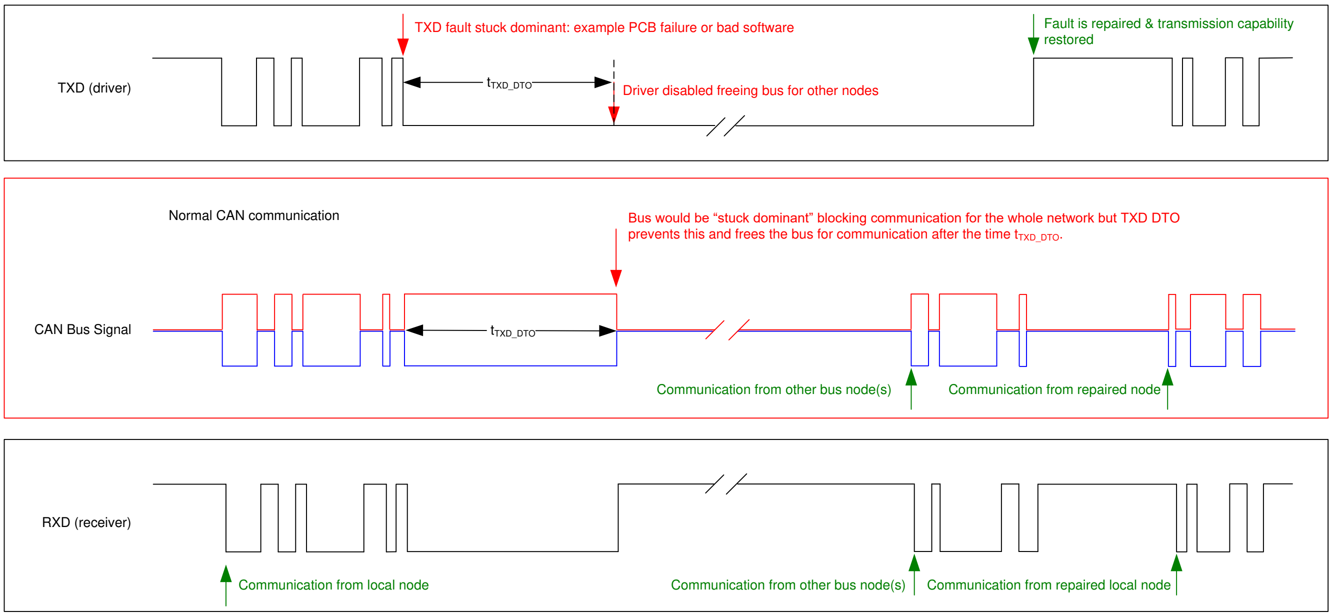


图 8-2. Example Timing Diagram for TXD Dominant Timeout

8.3.4 CAN Bus Short-Circuit Current Limiting

The device has several protection features that limit the short-circuit current when a CAN bus line is shorted. These features include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, therefore the short-circuit current is viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common mode choke for the CAN design, the $I_{OS(AVG)}$ should be used, which is the average current rating. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. These features ensure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using 方程式 2.

$$I_{OS(AVG)} = \%\ Transmit \times [(\%\ REC\_Bits \times I_{OS(SS)\_REC}) + (\%\ DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%\ Receive \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short-circuit current

This short-circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceivers V_{CC} supply.

8.3.5 Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to $V_{CC}/2$ during a TSD fault and the receiver to RXD path remains operational. The device TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

8.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

表 8-1. Undervoltage Lockout - TCAN1057AEV-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	S = V_{IO}: Silent mode	High impedance Weak pull-down to ground(1)	Recessive
		S = GND: Protected mode		
> UV_{VCC}	< UV_{VIO}	Protected		High impedance
< UV_{VCC}	< UV_{VIO}	Protected		High impedance

(1) V_{CC} = GND, see $I_{LKG(OFF)}$

Once the undervoltage condition is cleared and t_{MODE} has expired the device transitions to normal mode and the host controller can send and receive CAN traffic again.

8.3.7 Unpowered Device

If the device is unpowered, it is designed as an ideal passive or no load to the CAN bus . The bus pins are designed to have low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so they do not load other circuits which can remain powered.

8.3.8 Floating Pins

The device has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used, an adequate external pull-up resistor must be chosen. This ensures that the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See 表 8-2 for details on pin bias conditions.

表 8-2. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD toward recessive to prevent bus blockage or TXD DTO triggering
S	Pull-up	Weakly biases S towards low-power silent mode to prevent excessive system power

8.4 Device Functional Modes

8.4.1 Operating Modes

The device has two main operating modes: normal mode and silent mode. Operating mode selection is made by applying a high or low level to the S pin.

表 8-3. Operating Modes

S	Device Mode	Driver	Receiver	RXD Pin
High	Silent mode	Disabled	Enabled	Mirrors bus state
Low	Normal mode	Enabled	Enabled	

8.4.2 Normal Mode

This is the normal operating mode of the device. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins. The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

8.4.3 Silent Mode

In silent mode the CAN driver is disabled and the high-speed CAN receiver is enabled. CAN communication is unidirectional into the device where the receiver is translating the differential signal from CANH and CANL to a digital output on RXD. The power consumption of the TCAN1057AEV-Q1 is reduced in silent mode due to the CAN driver being disabled.

8.4.4 Driver and Receiver Function

The digital input and output levels for the device are CMOS levels with respect to V_{IO}.

表 8-4. Driver Function Table

Device Mode	TXD Input(1)	Bus Outputs		Driven Bus State(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Silent	X	High impedance	High impedance	Biased recessive

(1) X = irrelevant
(2) For bus state see 图 8-1

表 8-5. Receiver Function Table Normal and Silent Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal or Silent	$V_{ID} \geqslant 0.9$ V	Dominant	Low
	0.5 V < V_{ID} < 0.9 V	Undefined	Undefined
	$V_{ID} \leqslant 0.5$ V	Recessive	High
Any	Open ($V_{ID} \approx 0$ V)	Open	High

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.2 Typical Application

图 9-1 shows a typical configuration for 5 V system using the device. The bus termination is shown for illustrative purposes.

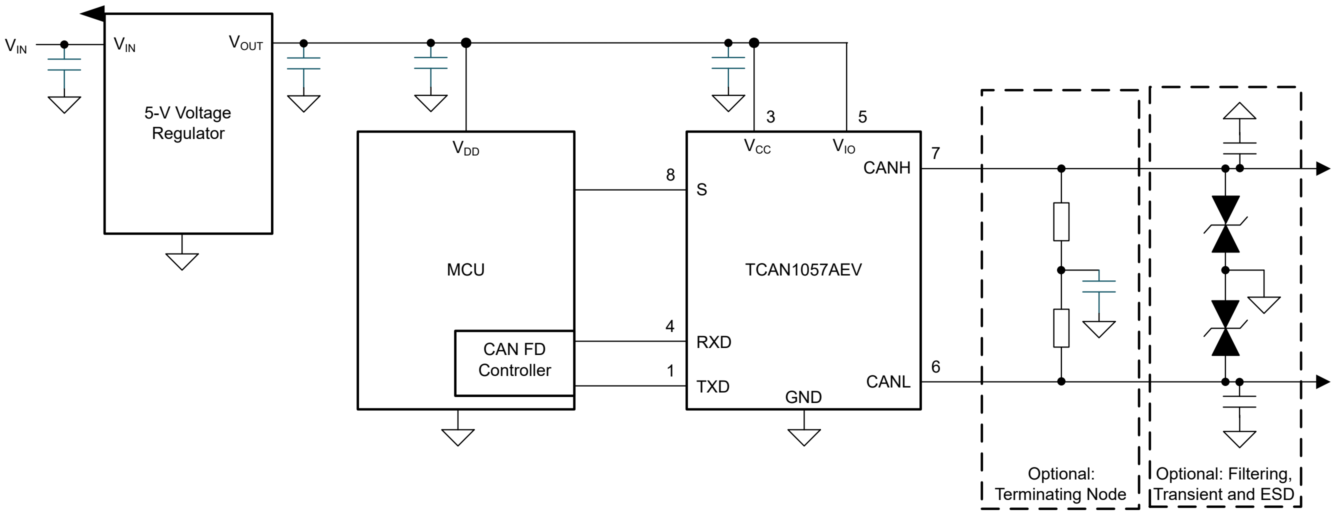


图 9-1. Transceiver Application Using 5 V I/O Connections

9.2.1 Design Requirements

9.2.1.1 CAN Termination

Termination may be a single 120-Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see 图 9-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

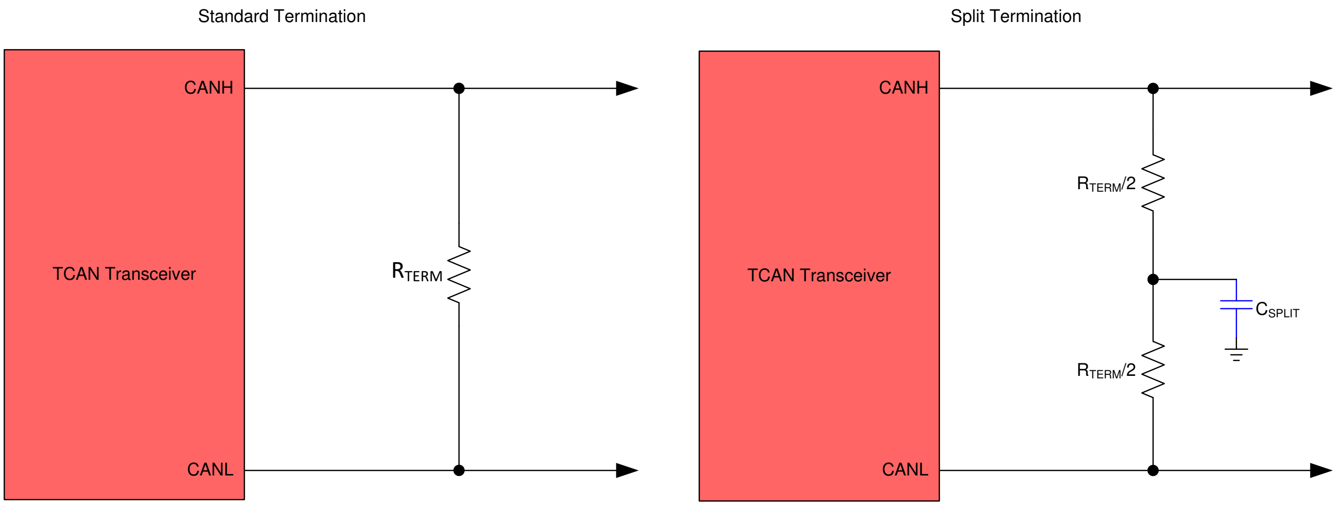


图 9-2. CAN Bus Termination Concepts

9.2.2 Detailed Design Procedures

9.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 meters. However, longer cables, longer stub lengths, and many more nodes to a bus can be achieved with careful design. . A high number of nodes requires a transceiver with high input impedance such as the TCAN1057AEV-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN1057AEV-Q1 family is specified to meet the 1.5-V requirement down to 50 Ω and is specified to meet 1.4-V differential output at 45 Ω bus load. The differential input resistance of the transceiver is a minimum of 40 kΩ. If 100 transceivers are in parallel on a bus, this is equivalent to a 400-Ω differential load in parallel with the nominal 60 Ω bus termination which gives a total bus load of approximately 52 Ω. Therefore, the TCAN1057AEV-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length can be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

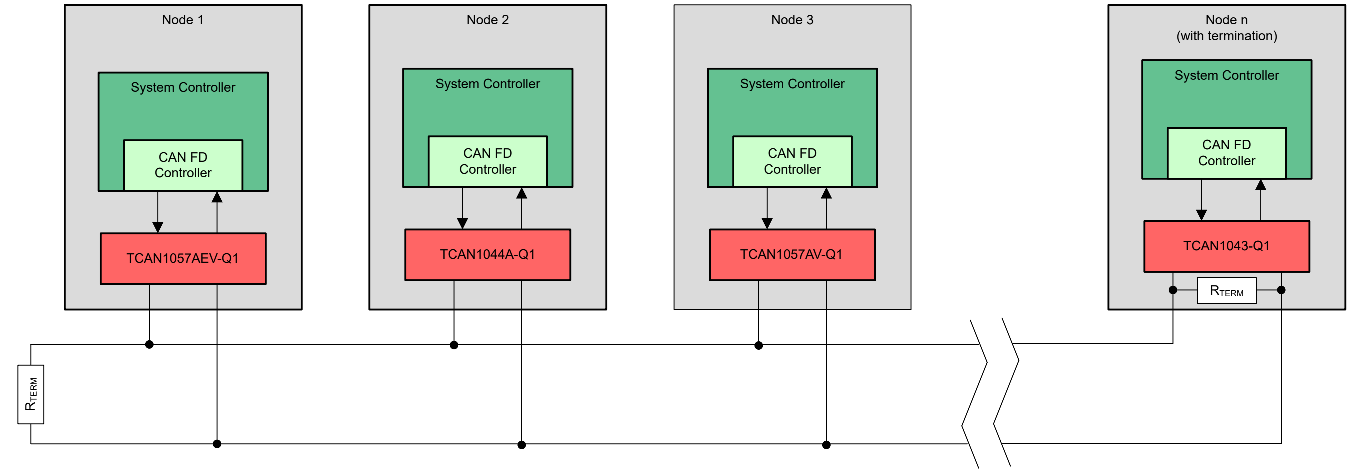
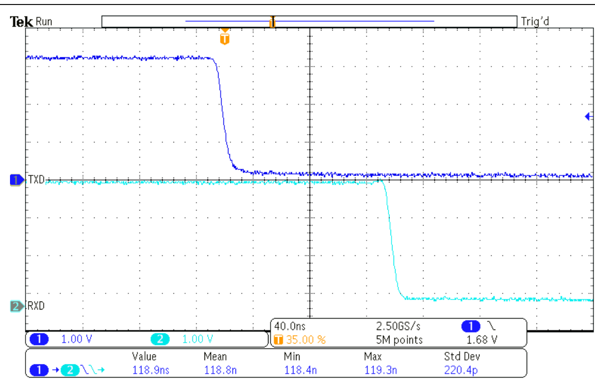


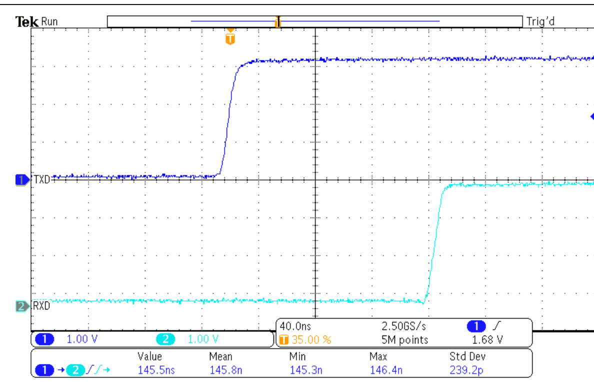
图 9-3. Typical CAN Bus

9.2.3 Application Curves



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

图 9-4. $t_{PROP(LOOP1)}$



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

图 9-5. $t_{PROP(LOOP2)}$

9.2.4 System Examples

图 9-6 shows a typical configuration for 1.8 V, 2.5 V, or 3.3 V systems using the TCAN1057AEV-Q1. The bus termination is shown for illustrative purposes.

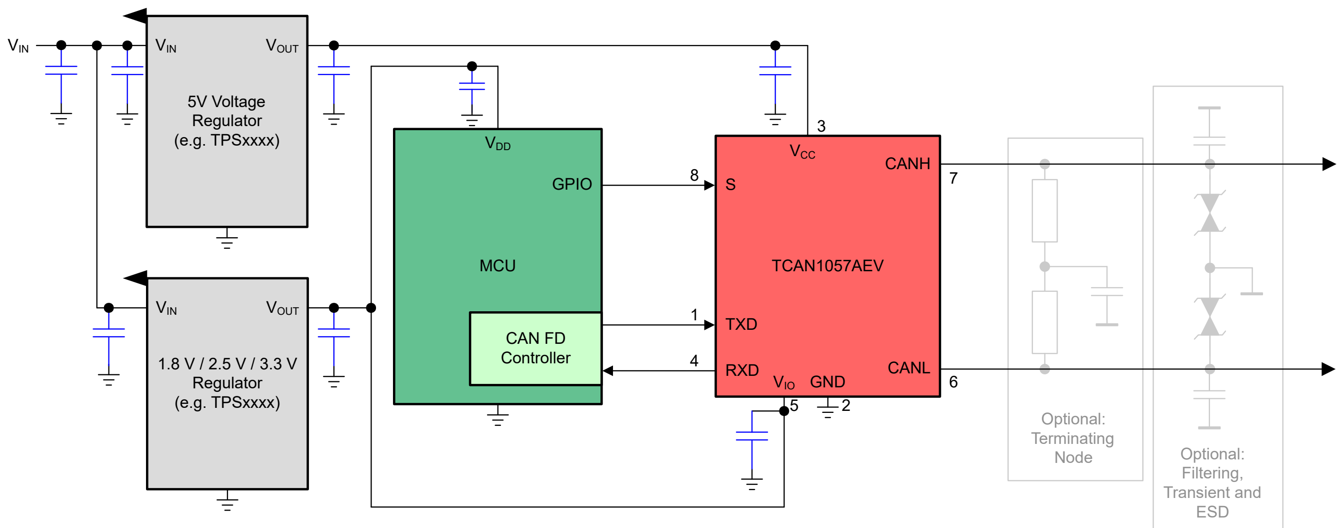


图 9-6. Typical Transceiver Application Using 1.8 V, 2.5 V, 3.3 V IO Connections

10 Power Supply Recommendations

The TCAN1057AEV-Q1 transceiver is designed to operate with a main V_{CC} input voltage supply range between 4.5 V and 5.5 V. The TCAN1057AEV-Q1 implements an I/O level shifting supply input, V_{IO}, designed for a range between 1.7 V and 5.5 V. It is important that both supply inputs are well regulated. In addition to the power supply filtering capacitance, a decoupling capacitance that is typically 100 nF should be placed near the CAN transceiver's V_{CC} and V_{IO} supply pins.

11 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high-frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

11.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows an optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors must be placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

备注

High-frequency current follows the path of least impedance, not the path of least resistance.

- This layout example shows how to implement split termination on the CAN node. The termination is split into two resistors, R4 and R5, with the center or split tap of the termination connected to ground through capacitor C3. Split termination provides common-mode filtering for the bus. See CAN Termination, CAN Bus Short Circuit Current Limiting, and 方程式 2 for information on termination concepts and required power rating for the termination resistors.

11.2 Layout Example

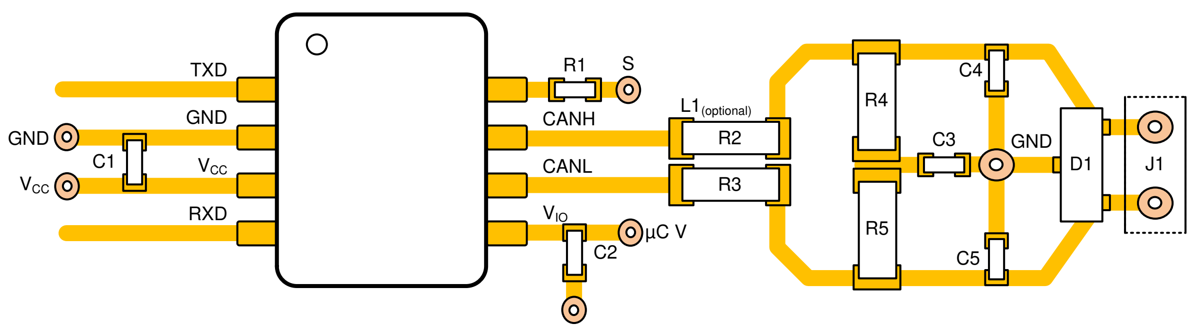


图 11-1. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

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12.5 Electrostatic Discharge Caution

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1057AEVDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	57AEV
TCAN1057AEVDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	57AEV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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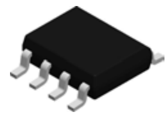
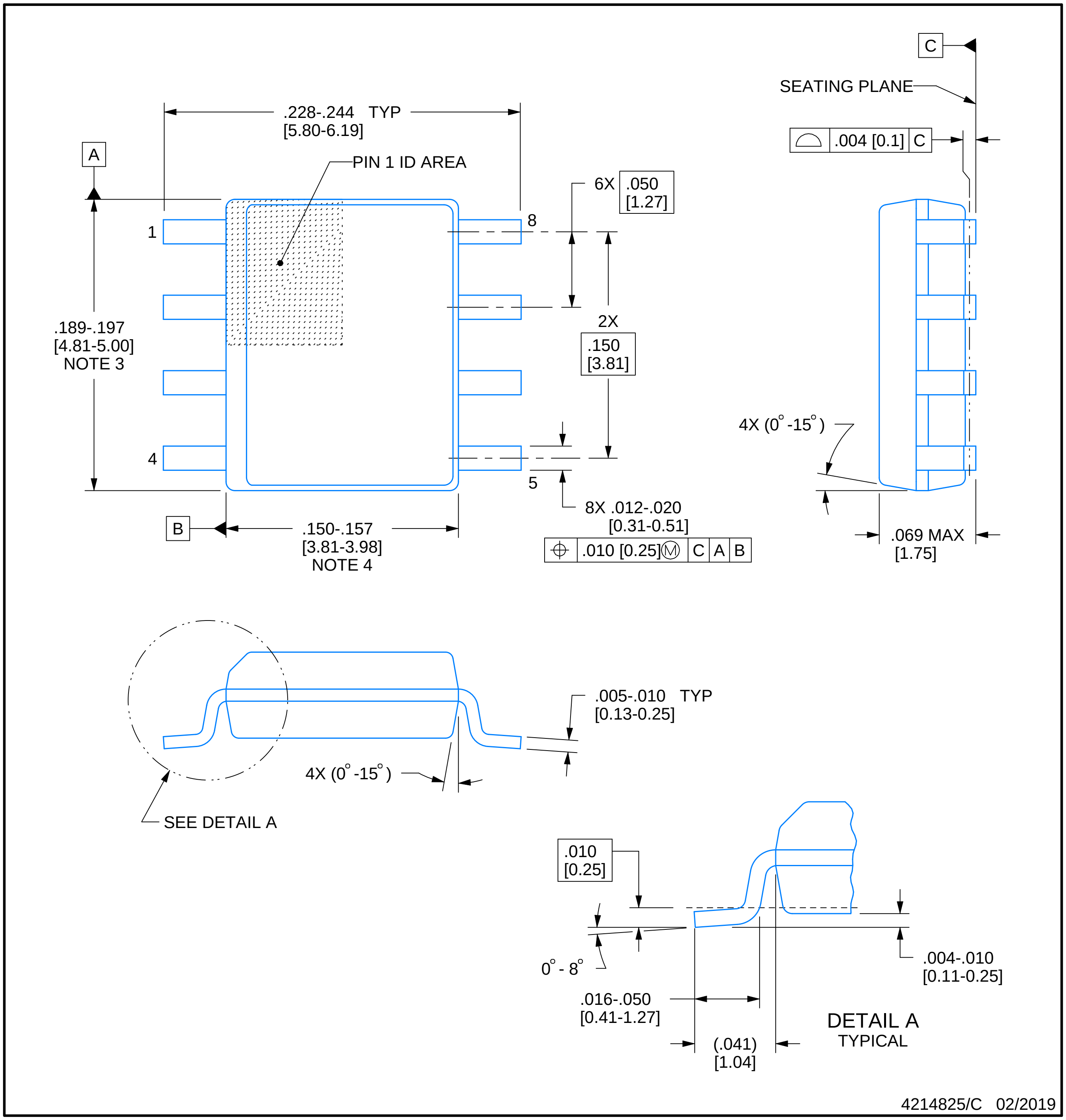


PACKAGE OUTLINE

D0008A

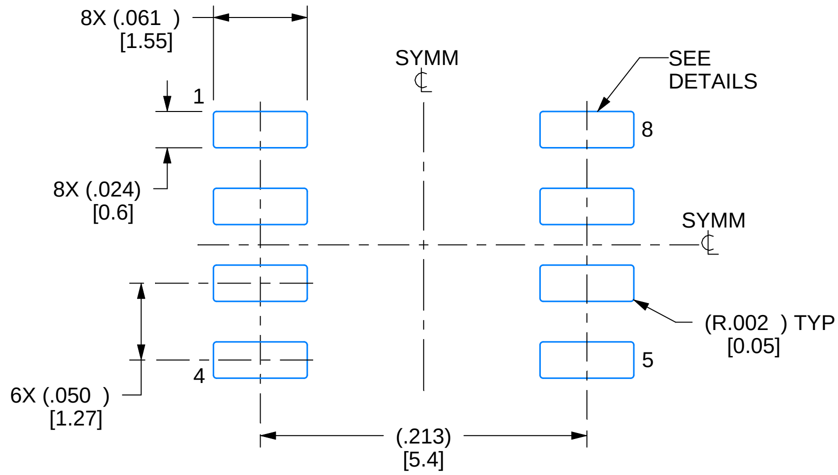
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

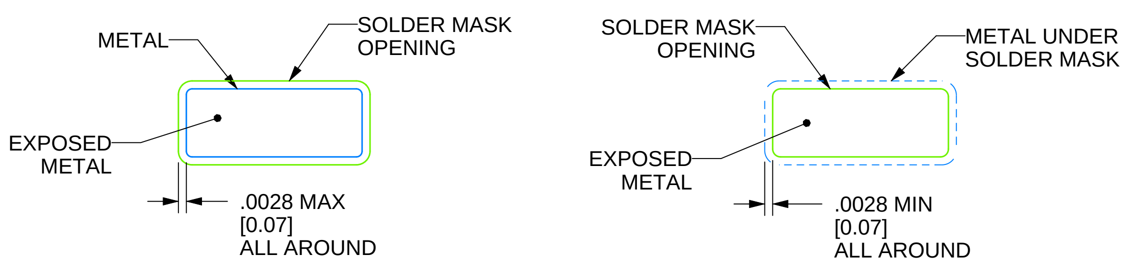


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

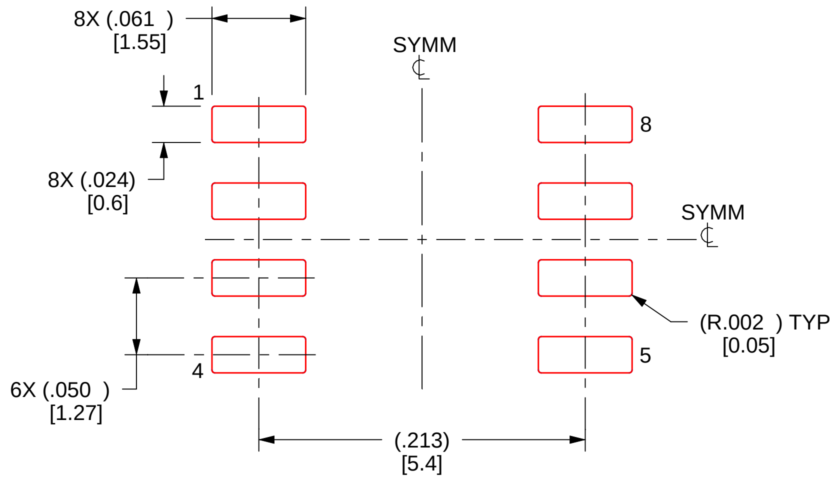
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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