TDC7201 适用于激光雷达、测距仪 和 ADAS 中飞行时间应用的时间-数字转换器

1 特性

- 分辨率：55ps
- 标准偏差：35ps
- 测量范围:
  - 独立模式 1：12ns 至 2000ns
  - 独立模式 2：250ns 至 8ms
  - 组合模式：0.25ns 至 8ms
- 低运行功耗：2.7mA
- 最多支持 10 个 STOP 信号
- 自主多周期平均模式，可实现低功耗
- 电源电压：2V 至 3.6V
- 工作温度范围：-40°C 至 +85°C
- 用于寄存器访问的串行外设接口 (SPI) 接口

2 应用

- 测距仪
- 激光雷达
- 无人机和机器人
- 高级驾驶员辅助系统 (ADAS)
- 冲突检测系统
- 流量计

3 说明

TDC7201 设计为与采用飞行时间技术的超声波、激光和雷达测距设备搭配使用。TDC7201 内置有两个时间数字转换器 (TDC)，可用于测量 4 厘米到数千米范围内的距离，而且架构非常简单，无需使用昂贵的现场可编程门阵列 (FPGA) 或处理器。

每个 TDC 均可执行秒表功能，测量 START 脉冲与多达 5 个 STOP 脉冲之间的时间间隔（飞行时间，即 TOF）。利用这两个 TDC，可以同时且单独测量两对 START 和 STOP 引脚，从而提高时间测量设计的灵活性。

该器件内置自校准时基，可对时间和温度偏差进行补偿。这一自校准功能使得时间数字转换器能够获得皮秒级精度。这一精度使得 TDC7201 非常适合测距 应用。

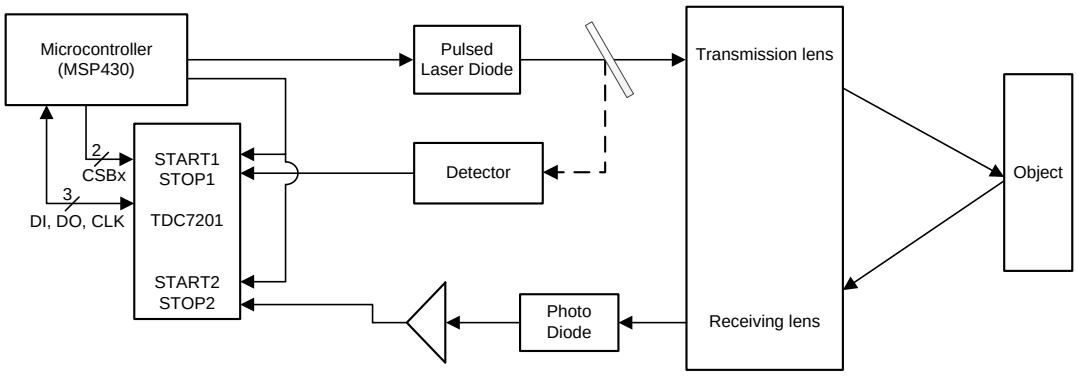
当 TDC7201 器件置于自主多周期平均模式下时，可降低系统功耗，非常适合电池供电式流量计。在该模式下，主器件会进入休眠模式以实现节能并在测量序列完成后由 TDC 中断唤醒。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TDC7201	nFBGA (25)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化的激光雷达应用框图



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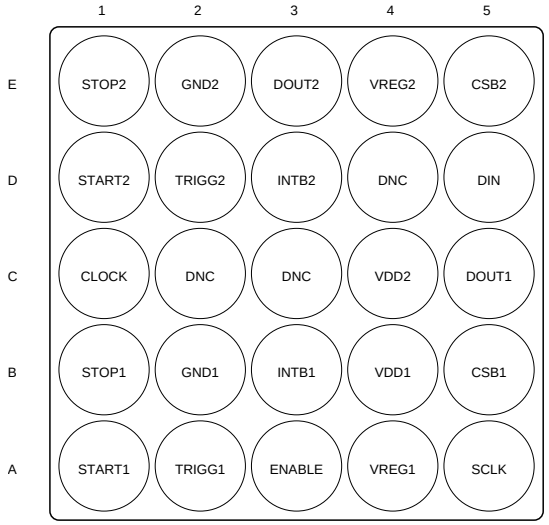
4 修订历史记录

日期	修订版本	注释
2016 年 5 月	*	最初发布版本。

5 Pin Configuration and Functions

ZAX Package
25-Pin nFBGA
Bottom View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	START1	Input	START signal for TDC1
A2	TRIGG1	Output	Trigger output signal for TDC1
A3	ENABLE	Input	Enable signal to TDC
A4	VREG1	Output	LDO output terminal for external decoupling cap
A5	SCLK	Input	SPI clock
B1	STOP1	Input	STOP signal for TDC1
B2	GND1	Ground	Ground
B3	INTB1	Output	Interrupt to MCU for TDC1, active low (open drain)
B4	VDD1	Power	Supply input
B5	CSB1	Input	SPI chip select for TDC1, active low
C1	CLOCK	Input	Clock input to TDC
C2	DNC	—	Do not connect
C3	DNC	—	Do not connect
C4	VDD2	Power	Supply input
C5	DOUT1	Output	SPI data output for TDC1
D1	START2	Input	START signal for TDC2
D2	TRIGG2	Output	Trigger output signal for TDC2
D3	INTB2	Output	Interrupt to MCU for TDC2, active low (open drain)
D4	DNC	—	Do not connect
D5	DIN	Input	SPI data input
E1	STOP2	Input	STOP signal for TDC2
E2	GND2	Ground	Ground
E3	DOUT2	Output	SPI data output for TDC2
E4	VREG2	Output	LDO output terminal for external decoupling cap
E5	CSB2	Input	SPI chip select for TDC2, active low

6 Specifications

6.1 Absolute Maximum Ratings

at T_A = 25°C , VDD1 = VDD2 = 3.3 V, GND1 = GND2 = 0 V (unless otherwise noted).(1)(2)(3)(4)(5)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.3	3.9	V
V_I	Voltage on VREG1, VREG2 pins	–0.3	1.65	V
	Terminal input voltage on any other pin	–0.3	V_{DD} + 0.3	
V_{DIFF_IN}	|Voltage differential| between any two input terminals		3.9	V
$V_{IN\_GND\_VDD}$	|Voltage differential| between any input terminal and GND or VDD		3.9	V
I_I	Input current at any pin	–5	5	mA
T_A	Ambient temperature	–40	125	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Pins VDD1 and VDD2 must be tied together at the board level and supplied from the same source.
(5) When the terminal input voltage (V_I) at any pin exceeds power supplies (V_I < GND or V_I > VDD), the current at that pin must not exceed 5 mA (source or sink), and the voltage (V_I) at the pin must not exceed 3.9 V.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

At T_A = 25°C , VDD1 = VDD2 = 3.3 V, GND1 = GND2 = 0 V (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2		3.6	V
V_I	Terminal voltage	0		VDD	V
V_{IH}	Voltage input high	0.7 × VDD		3.6	V
V_{IL}	Voltage input low	0		0.3 × VDD	V
F_{CALIB_CLK}	Frequency (reference or calibration clock)	1 (1)	8	16	MHz
t_{CLOCK}	Time period (reference or calibration clock)	62.5	125	1000	ns
$DUTY_{CLOCK}$	Input clock duty cycle		50%		
TIMING REQUIREMENTS: Measurement Mode 1(1)(2)(3)					
$T1_{Min\_STARTSTOP}$	Minimum time between start and stop signal	12			ns
$T1_{Max\_STARTSTOP}$	Maximum time between start and stop signal		2000		ns
$T1_{Min\_STOPSTOP}$	Minimum time between 2 stop signals	67			ns
$T1_{Max\_LASTSTOP}$	Maximum time between start and last stop signal		2000		ns
TIMING REQUIREMENTS: Measurement Mode 2(1)(2)(3)					
$T2_{Min\_STARTSTOP}$	Minimum time between start and stop signal	2 × t_{CLOCK}			s
$T2_{Max\_STARTSTOP}$	Maximum time between start and stop signal			(2^{16}-2) × t_{CLOCK}	s
$T2_{Min\_STOPSTOP}$	Minimum time between 2 stop signals	2 × t_{CLOCK}			s
$T2_{Max\_LASTSTOP}$	Maximum time between start and last stop signal			(2^{16}-2) × t_{CLOCK}	s

(1) Specified by design.
(2) Applies to both pairs of START1, STOP1 and START2, STOP2 pins.
(3) Minimum time between 2 stop signals applies to 2 stop signals on the same TDC.

Recommended Operating Conditions (continued)

At T_A = 25°C , VDD1 = VDD2 = 3.3 V, GND1 = GND2 = 0 V (unless otherwise noted).

		MIN	NOM	MAX	UNIT
TIMING REQUIREMENTS: ENABLE INPUT					
T_{REN}	Rise time for enable signal (20% to 80%)		1 to 100		ns
T_{FEN}	Fall time for enable signal (20% to 80%)		1 to 100		ns
TIMING REQUIREMENTS: START1, STOP1, CLOCK, START2, STOP2					
T_{RST}, T_{FST}	Maximum rise, fall time for START, STOP signals (20% to 80%)		1		ns
T_{RXCLK}, T_{FXCLK}	Maximum rise, fall time for external CLOCK (20% to 80%)		1		ns
TIMING REQUIREMENTS: TRIGG1, TRIGG2					
$T_{TRIG1START1}$	Time from TRIG1 to START1	5			ns
$T_{TRIG2START2}$	Time from TRIG2 to START2	5			ns
TIMING REQUIREMENTS: Measurement Mode 1 Combined Operation(4)					
$T1_{STARTSTOP\_Comb\_Min}$	Minimum time between START and STOP signal combined		0.25		ns
TEMPERATURE					
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		85	°C

(4) TDC7201 device in combined measurement mode where START1 and START2 are connected together:
(a) A common REFERENCE_START signal is applied to START1 and START2 at least 12 ns before occurrence of actual START and STOP signals in Mode 1 (and at least 2 × t_{CLOCK} before occurrence of actual Start and Stop signals in Mode 2).
(b) Start signal is connected to STOP1
(c) Stop signal is connected to STOP2
(d) Two time periods T1 (REFERENCE_START to Start) and T2 (REFERENCE_START to Stop) are measured and their difference (T2-T1) is the time between Start to Stop

6.4 Thermal Information

THERMAL METRIC(1)		TDC7201 ZAX (nFBGA) 25 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	155.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	109.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	114.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	110.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C , VDD1 = VDD2 = 3.3 V, GND1 = GND2 = 0 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TDC CHARACTERISTICS						
LSB	Resolution	Single shot measurement		55		ps
T_{ACC-2}	Accuracy (Mode 2)(1)	CLOCK = 8 MHz, Jitter (RMS) < 1 ps, Stability < 5 ppm		28		ps
T_{STD-2}	Standard Deviation (Mode 2)	Measured time = 100 µs		50		ps
		Measured time = 1 µs		35		ps
OUTPUT CHARACTERISTICS: TRIGG1, TRIGG2, INTB1, INTB2, DOUT1, DOUT2						
V_{OH}	Output voltage high	Isource = –2 mA	2.31	2.95		V
V_{OL}	Output voltage low	Isink = 2 mA		0.35	0.99	V
INPUT CHARACTERISTICS: START1, STOP1, START2, STOP2, CSB1, CSB2						
C_{in}	Input capacitance(2)			4		pF
INPUT CHARACTERISTICS: ENABLE, CLOCK, DIN, SCLK						
C_{in}	Input capacitance(2)			8		pF
POWER CONSUMPTION(3) (see *Measurement Mode 1* and *Measurement Mode 2*)						
I_{sh}	Shutdown current	EN = LOW		0.6		µA
I_{QA}	Quiescent Current A	EN = HIGH; TDC running		2.7		mA
I_{QB}	Quiescent Current B	EN = HIGH; TDC OFF, Clock Counter running		140		µA
I_{QC}	Quiescent Current C	EN = HIGH; measurement stopped, SPI communication only		175		µA
I_{QD}	Quiescent Current D	EN = HIGH, TDC OFF, counter stopped, no communication		100		µA

(1) Accuracy is defined as the systematic error in the output signal; the error of the device excluding noise.
(2) Specified by design.
(3) Sum of TDC1 and TDC2 values

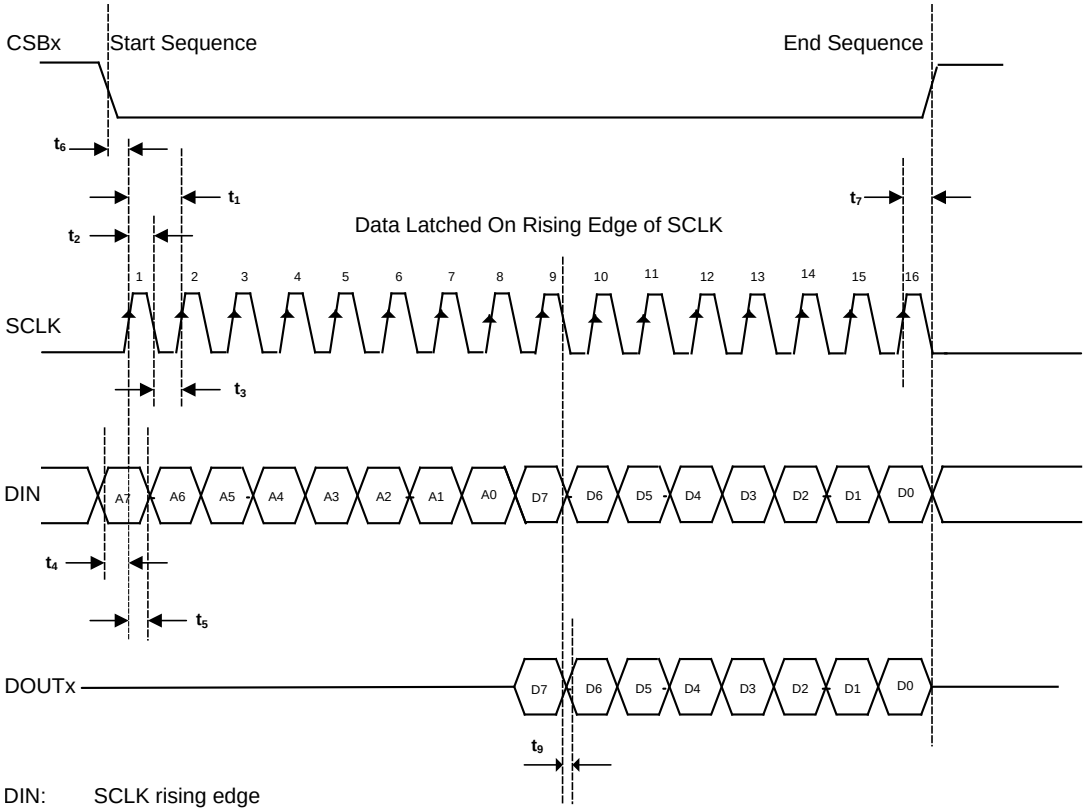
6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
TIMING REQUIREMENTS: START1, STOP1, START2, STOP2, CLOCK					
PW_{START}	Pulse width for Start Signal	10			ns
PW_{STOP}	Pulse width for Stop Signal	10			ns
SERIAL INTERFACE TIMING CHARACTERISTICS (VDD = 3.3 V, f_{SCLK} = 25 MHz) (See Figure 1)					
f_{SCLK}	SCLK frequency			25	MHz
t_1	SCLK period	40			ns
SERIAL INTERFACE TIMING CHARACTERISTICS (VDD = 3.3 V, f_{SCLK} = 20 MHz) (See Figure 1)					
t_1	SCLK period	50			ns
t_2	SCLK High Time	16			ns
t_3	SCLK Low Time	16			ns
t_4	DIN setup time	5			ns
t_5	DIN hold time	5			ns
t_6	CSB1 or CSB2 fall to SCLK rise	6			ns
t_7	Last SCLK rising edge to CSB1 or CSB2 rising edge	6			ns
t_8	Minimum pause time (CSB high)	40			ns
t_9	Clk fall to DOUT1 or DOUT2 bus transition			12	ns

6.7 Switching Characteristics

T_A = 25°C , VDD1 = VDD2 = 3.3 V, GND1 = GND2 = 0 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE UP TIME						
T_{WAKEUP_PERIOD}	Time to be ready for measurement	LSB within 0.3% of settled value		300		µs



DIN: SCLK rising edge
DOUTx: SCLK falling edge

Figure 1. SPI Register Access: 8 Bit Register Example

6.8 Typical Characteristics

At T_A = 25°C , VDD1 = VDD2 = 3.3 V, GND1 = GND2 = 0 V, CLOCK = 8 MHz, CALIBRATION2_PERIODS = 10, AVG_CYCLES = 1 Measurement, NUM_STOP = Single STOP, Measurement Mode 2 (unless otherwise noted).

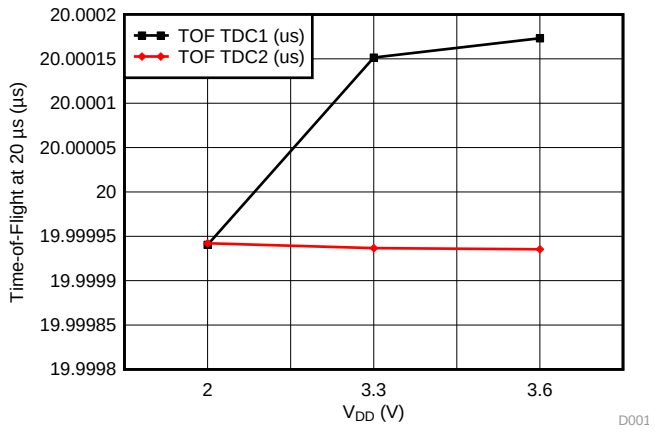


Figure 2. Time-of-Flight (TOF) vs VDD (Measurement Mode 2)

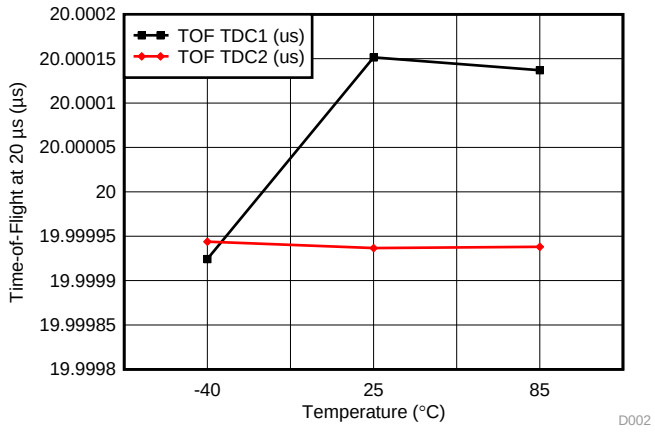


Figure 3. TOF vs Temperature (Measurement Mode 2)

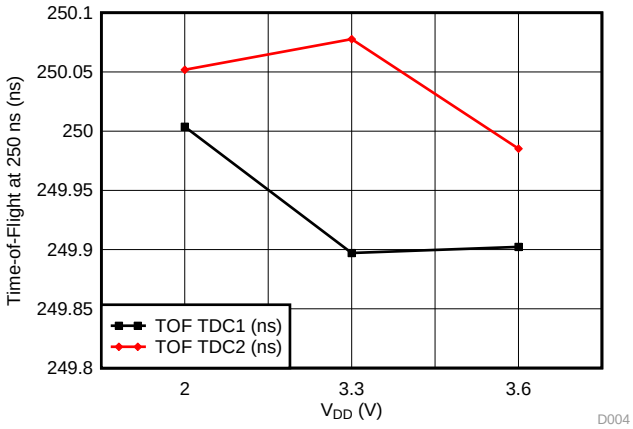


Figure 4. TOF vs VDD (Measurement Mode 1)

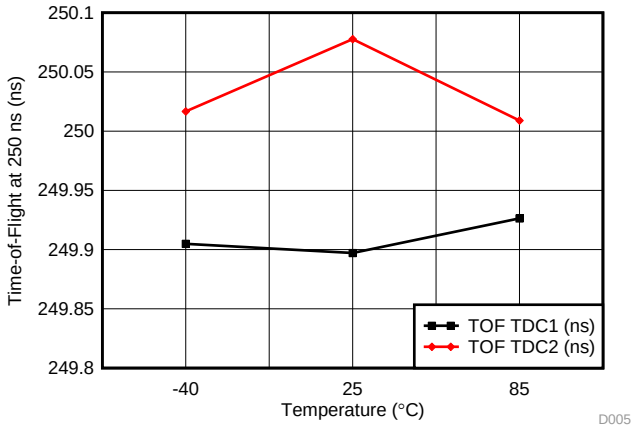


Figure 5. TOF vs Temperature (Measurement Mode 1)

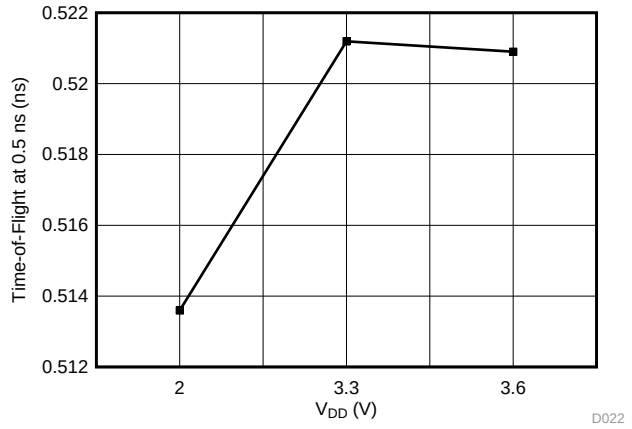


Figure 6. TOF vs. VDD (Mode 1 Combined Operation)

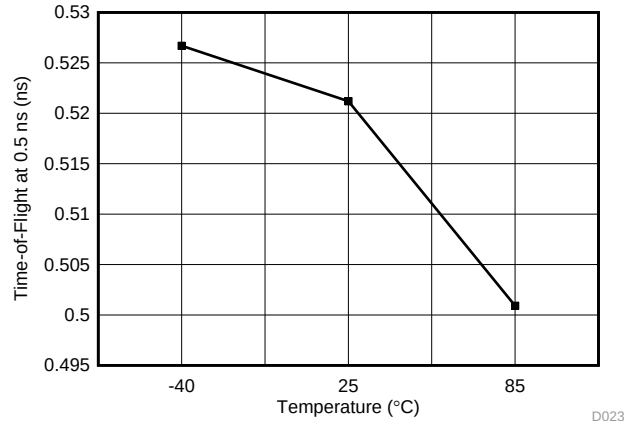


Figure 7. TOF vs. Temperature (Mode 1 Combined Operation)

Typical Characteristics (continued)

At T_A = 25°C , VDD1 = VDD2 = 3.3 V, GND1 = GND2 = 0 V, CLOCK = 8 MHz, CALIBRATION2_PERIODS = 10, AVG_CYCLES = 1 Measurement, NUM_STOP = Single STOP, Measurement Mode 2 (unless otherwise noted).

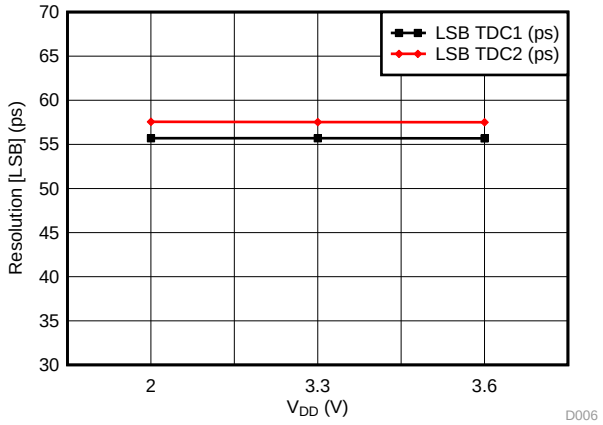


Figure 8. Resolution (LSB) vs VDD

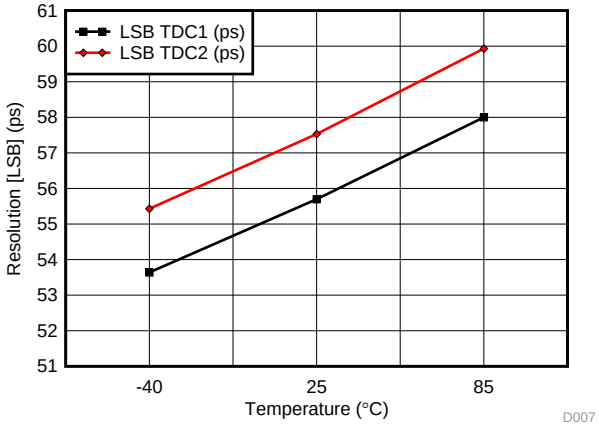


Figure 9. Resolution (LSB) vs Temperature

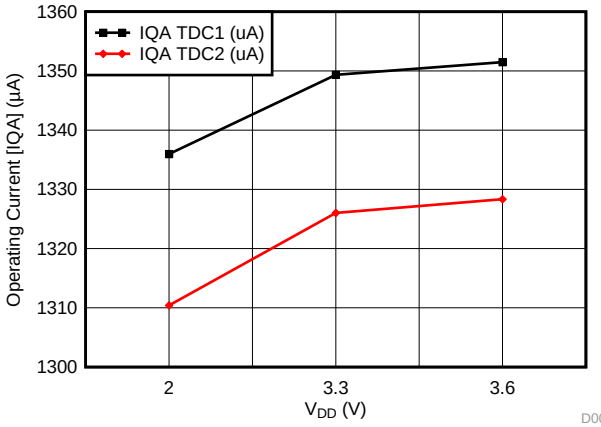


Figure 10. Operating Current (IQA) vs VDD

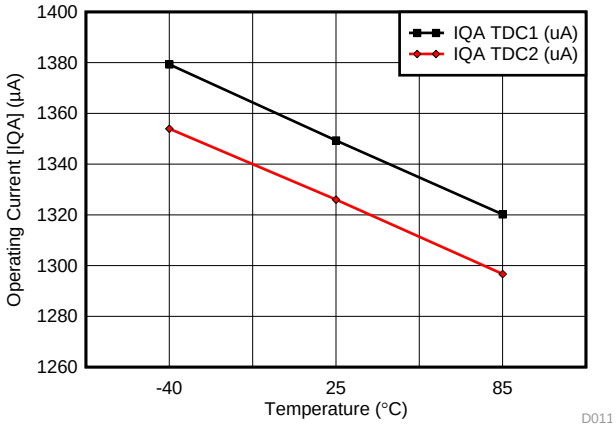


Figure 11. Operating Current (IQA) vs Temperature

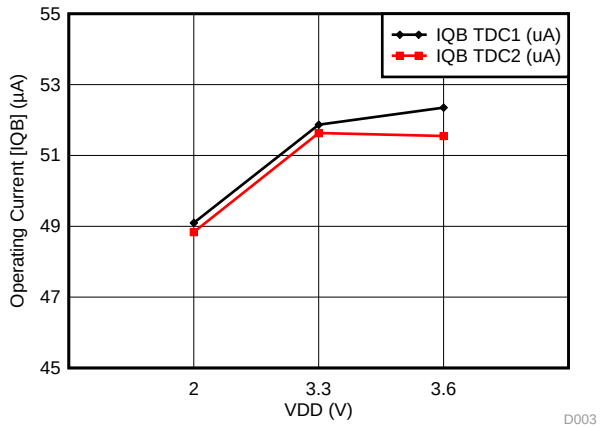


Figure 12. Operating Current (IQB) vs VDD

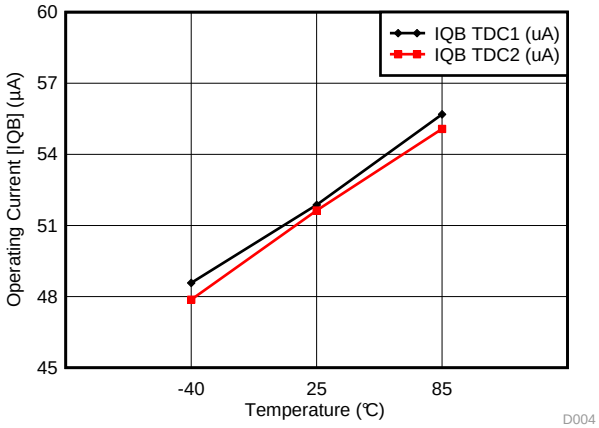


Figure 13. Operating Current (IQB) vs Temperature

Typical Characteristics (continued)

At T_A = 25°C , VDD1 = VDD2 = 3.3 V, GND1 = GND2 = 0 V, CLOCK = 8 MHz, CALIBRATION2_PERIODS = 10, AVG_CYCLES = 1 Measurement, NUM_STOP = Single STOP, Measurement Mode 2 (unless otherwise noted).

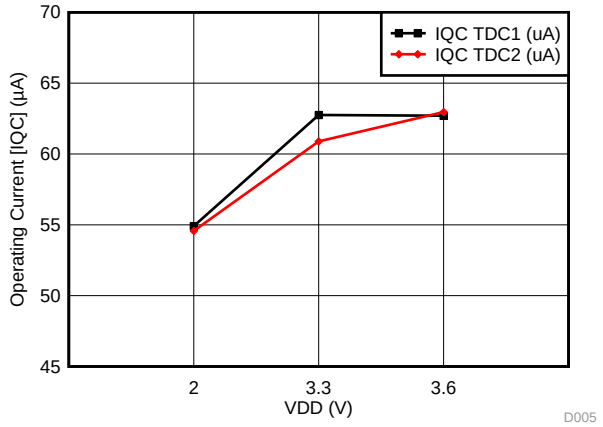


Figure 14. Operating Current (IQC) vs VDD

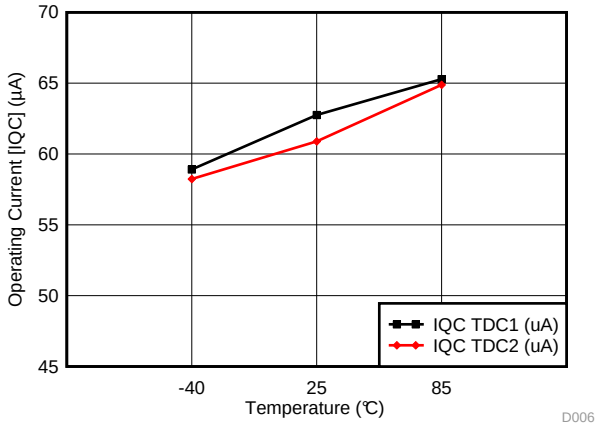


Figure 15. Operating Current (IQC) vs Temperature

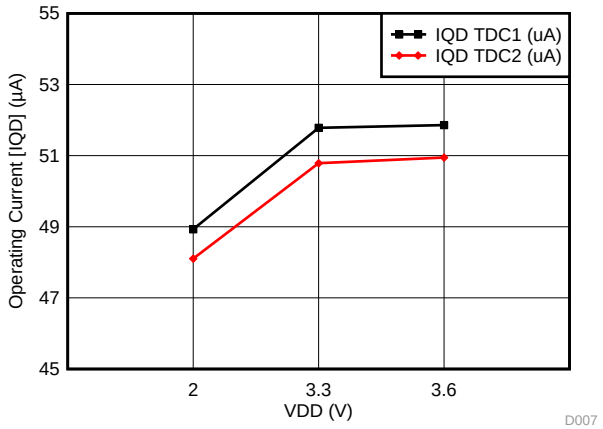


Figure 16. Operating Current (IQD) vs VDD

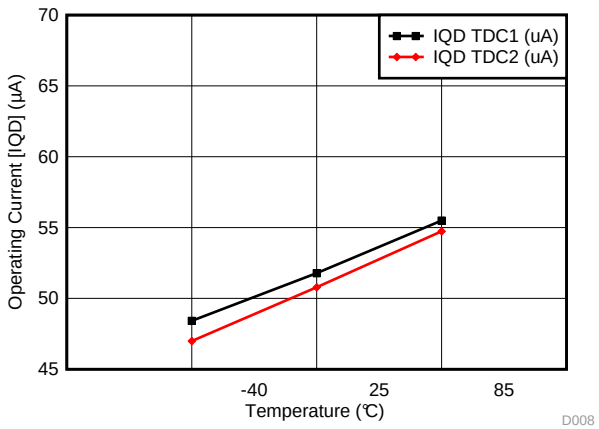


Figure 17. Operating Current (IQD) vs Temperature

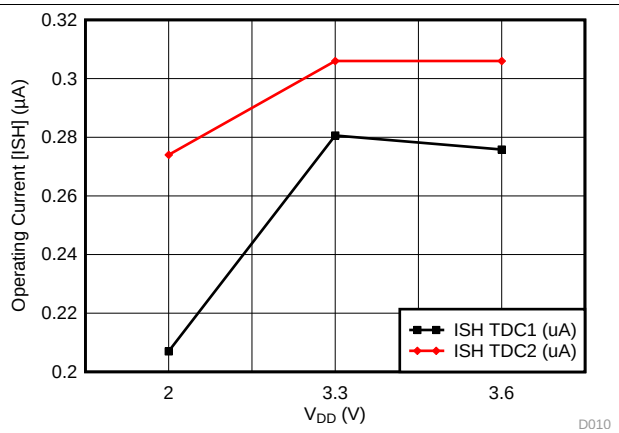


Figure 18. Shutdown Current (ISH) vs VDD

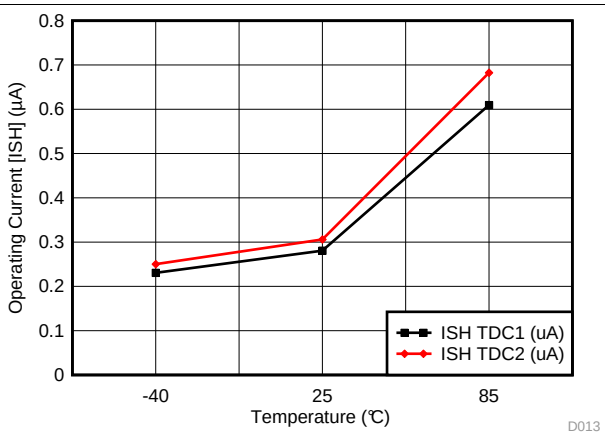


Figure 19. Shutdown Current (ISH) vs Temperature

7 Detailed Description

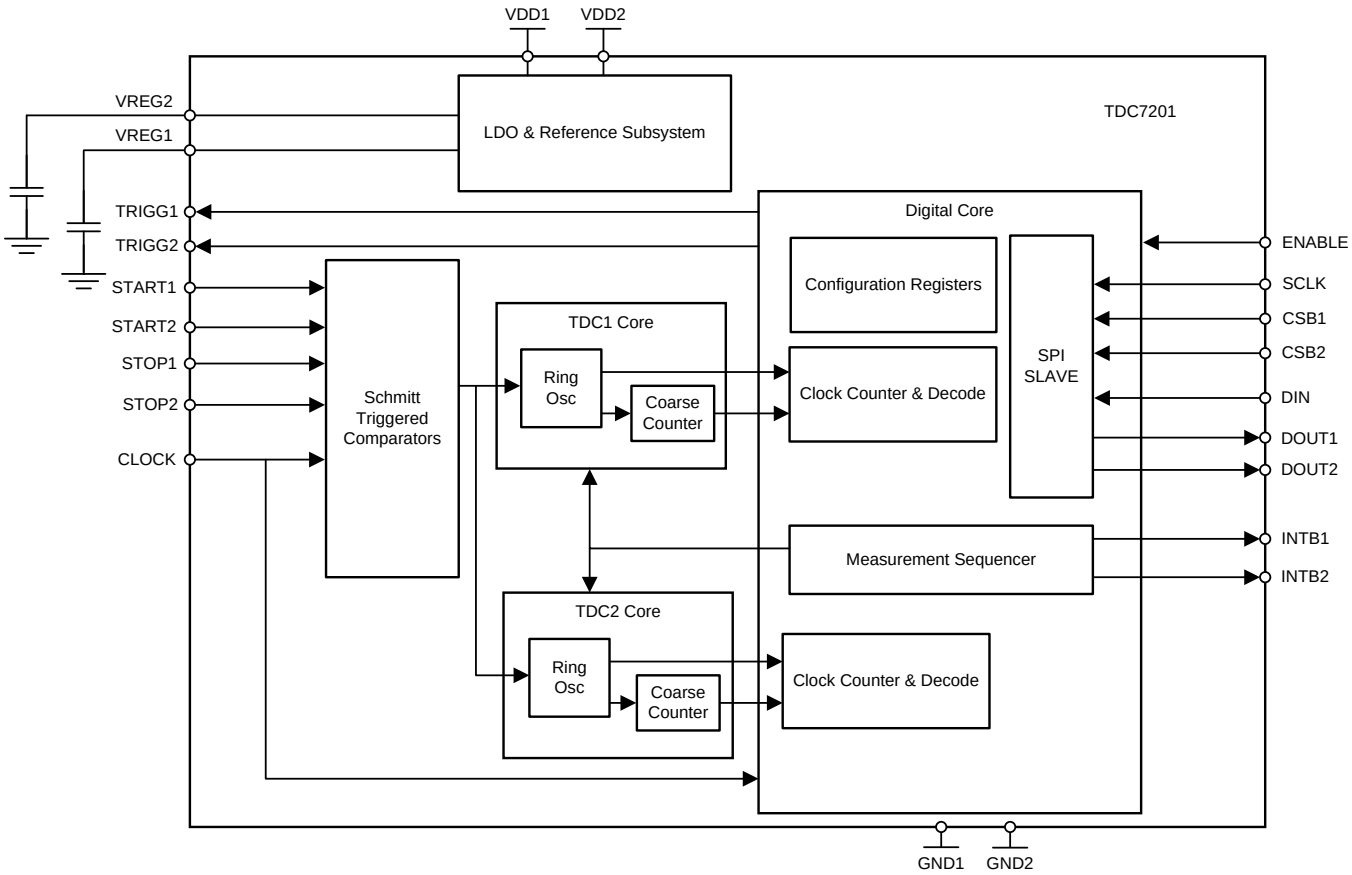
7.1 Overview

The TDC7201 has two built-in TDCs with the capability to simultaneously and individually measure time delay on two pairs of START and STOP pins. Each TDC is a stopwatch that measures time between a single event (edge on START pin) and multiple subsequent events (edge on STOP pin). An event from a START pulse to a STOP pulse is also known as time-of-flight, or TOF for short. The TDC has an internal time base that is used to measure time with accuracy in the order of picoseconds. This accuracy makes the TDC7201 ideal for applications such as drones and range finders, which require high accuracy in the picoseconds range.

NOTE

In rest of the documentation, we use TDCx to refer each TDC of the TDC7201, where x = 1, 2. Also, the prefix TDCx is used in register names to identify the TDC the register belongs to. Further the associated START, STOP, TRIGG, CSB, DOUT, and INTB pins of TDCx are represented as STARTx, STOPx, TRIGGx, CSBx, DOUTx, and INTBx.

7.2 Functional Block Diagram



NOTE

Do not tie together VREG1 and VREG2.

7.3 Feature Description

7.3.1 LDO

The LDO (low-dropout) is an internal supply voltage regulator for the TDC7201. Each of the two TDC cores of the TDC7201 has its own dedicated LDO. No external circuitry needs to be connected to the output of this regulator other than the mandatory external decoupling capacitor on VREG1 and VREG2.

Recommendations for the decoupling capacitor parameters:

- Type: ceramic
- Capacitance: 0.4 µF to 2.7 µF (1 µF typical). If using a capacitor value outside the recommended range, the part may malfunction and can be damaged.
- ESR: 100 mΩ (maximum)

7.3.2 CLOCK

The TDC7201 needs an external reference clock connected to the CLOCK pin. This external clock input serves as the reference clock for both TDCs of the TDC7201. The external CLOCK is used to calibrate the internal time base accurately and therefore, the measurement accuracy is heavily dependent on the external CLOCK accuracy. This reference clock is also used by all digital circuits inside the device; thus, CLOCK has to be available and stable at all times when the device is enabled (ENABLE = HIGH).

Figure 20 shows the typical effect of the external CLOCK frequency on the measurement uncertainty. With a reference clock of 1 MHz, the standard deviation of a set of measurement results is approximately 243 ps. As the reference clock frequency is increased, the standard deviation (or measurement uncertainty) reduces. Therefore, using a reference clock of 16 MHz is recommended for optimal performance.

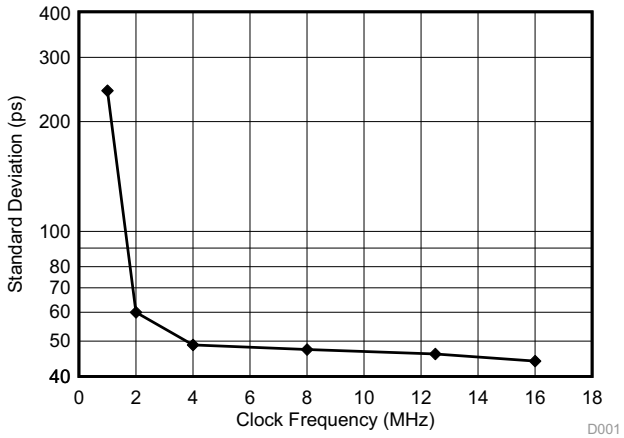


Figure 20. Standard Deviation vs CLOCK

7.3.3 Counters

7.3.3.1 Coarse and Clock Counters Description

Time measurements by each TDCx of the TDC7201 rely on two counters: the Coarse Counter and the Clock Counter. The Coarse Counter counts the number of times the ring oscillator (the TDCx's core time measurement mechanism) wraps, which is used to generate the results in the TDCx_TIME1 to TDCx_TIME6 registers.

The Clock Counter counts the number of integer clock cycles between START and STOP events and is used in *Measurement Mode 2* only. The results for the Clock Counter are displayed in the TDCx_CLOCK_COUNT1 to TDCx_CLOCK_COUNT5 registers.

7.3.3.2 Coarse and Clock Counters Overflow

Once the coarse counter value has reached the corresponding value of the Coarse Counter Overflow registers, then its interrupt bit will be set to 1. In other words, if (TDCx_TIMEn / 63) ≥ COARSE_CNTR_OVF, then COARSE_CNTR_OVF_INT = 1 (this interrupt bit is located in the TDCx_INT_STATUS register).

Feature Description (continued)

TDCx_COARSE_CNTR_OVF = (TDCx_COARSE_CNTR_OVF_H x 2^8 + TDCx_COARSE_CNTR_OVF_L), where TDCx_TIMEn refers to the TDCx_TIME1 to TDCx_TIME6 registers.

Similarly, once the clock counter value has reached the corresponding value of the Clock Counter Overflow registers, then its interrupt bit will be set to 1. In other words, if TDCx_CLOCK_COUNTn > TDCx_CLOCK_CNTR_OVF, then CLOCK_CNTR_OVF_INT = 1 (this interrupt bit is located in the INT_STATUS register).

TDCx_CLOCK_CNTR_OVF = (TDCx_CLOCK_CNTR_OVF_H × 2^8 + TDCx_CLOCK_CNTR_OVF_L), where TDCx_CLOCK_COUNTn refers to the TDCx_CLOCK_COUNT1 to TDCx_CLOCK_COUNT5 registers.

As soon as there is an overflow detected, the running measurement will be terminated immediately.

7.3.3.3 Clock Counter STOP Mask

The values in the Clock Counter STOP Mask registers define the end of the mask window. The Clock Counter STOP Mask value will be referred to as TDCx_CLOCK_CNTR_STOP_MASK = (TDCx_CLOCK_CNTR_STOP_MASK_H x 2^8 + TDCx_CLOCK_CNTR_STOP_MASK_L).

The Clock Counter is started by the first rising edge of the external CLOCK after the START signal (see Figure 23). All STOP signals occurring before the value set by the TDCx_CLOCK_CNTR_STOP_MASK registers will be ignored. This feature can be used to help suppress wrong or unwanted STOP trigger signals.

For example, assume the following values:

- The first time-of-flight (TOF1), which is defined as the time measurement from the START to the 1st STOP = 19 µs.
- The second time-of-flight (TOF2), which is defined as the time measurement from the START to the 2nd STOP = 119 µs.
- CLOCK = 8 MHz

In this example, the TDC7201 will provide a TDCx_CLOCK_COUNT1 of approximately 152 (19 µs / t_{CLOCK}), and TDCx_CLOCK_COUNT2 of approximately 952 (119 µs / t_{CLOCK}). If the user sets TDCx_CLOCK_CNTR_STOP_MASK anywhere between 152 and 952, then the 1st STOP will be ignored and 2nd STOP will be measured.

The Clock Counter Overflow value (TDCx_CLOCK_CNTR_OVF_H × 2^8 + TDCx_CLOCK_CNTR_OVF_L) should always be higher than the Clock Counter STOP Mask value (TDCx_CLOCK_CNTR_STOP_MASK_H × 2^8 + TDCx_CLOCK_CNTR_STOP_MASK_L). Otherwise, the Clock Counter Overflow Interrupt will be set before the STOP mask time expires, and the measurement will be halted.

7.3.3.4 ENABLE

The ENABLE pin is used as a reset to all digital circuits in the TDC7201. Therefore, it is essential that the ENABLE pin sees a positive edge after the device has powered up. It is also important to ensure that there are no transients (such as glitches) on the ENABLE pin; such glitches could cause the device to reset

7.4 Device Functional Modes

7.4.1 Calibration

The time measurements performed by each TDCx of the TDC7201 are based on an internal time base which is represented as the LSB value of the TDCx_TIME1 to TDCx_TIME6 results registers. The typical LSB value can be seen in *Electrical Characteristics*. However, the actual value of the LSB can vary depending on environmental variables (temperature, systematic noise, and so forth). This variation can introduce significant error into the measurement result. There is also an offset error in the measurement due to certain internal delays in the device.

In order to compensate for these errors and to calculate the actual LSB value, calibration needs to be performed. The TDCx calibration consists of two measurement cycles of the external CLOCK. The first is a measurement of a single clock cycle period of the external clock; the second measurement is for the number of external CLOCK periods set by the CALIBRATION2_PERIODS in the TDCx_CONFIG2 register. The results from the calibration measurements are stored in the TDCx_CALIBRATION1 and TDCx_CALIBRATION2 registers.

Device Functional Modes (continued)

The two-point calibration is used to determine the actual LSB in real time in order to convert the TDCx_TIME1 to TDCx_TIME6 results from number of delays to a real TOF number. Calibration is automatic and performed every time after a measurement and before measurement completion interrupt is sent to the MCU through INTBx pin. Only if a measurement is interrupted (for example, due to counter overflow or missing STOP signal), calibration is not performed. As discussed in the next sections, the calibrations will be used for calculating TOF in measurement modes 1 and 2.

7.4.2 Measurement Modes

7.4.2.1 Measurement Mode 1

In measurement mode 1, as shown in Figure 21, each TDCx of the TDC7201 performs the entire counting from START to the last STOP using its internal ring oscillator plus coarse counter. This method is recommended for measuring shorter time durations of < *2000 ns*. TI does not recommend using measurement mode 1 for measuring time > 2000 ns because this decreases accuracy of the measurement (as shown in Figure 22).

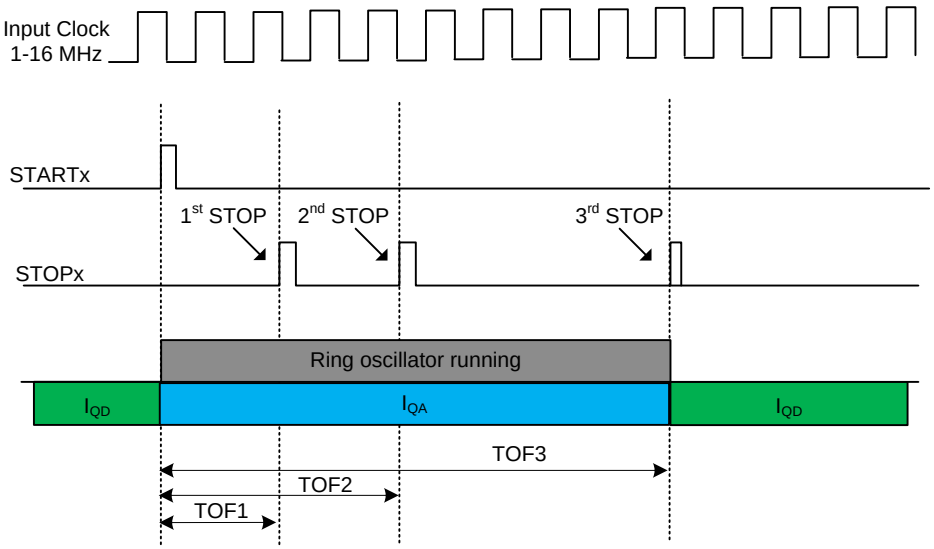


Figure 21. Measurement Mode 1

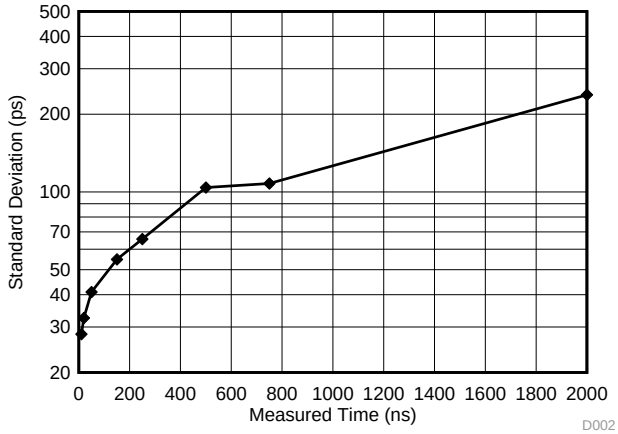


Figure 22. Measurement Mode 1 Standard Deviation vs Measured Time-of-Flight

Device Functional Modes (continued)

7.4.2.1.1 Calculating Time-of-Flight (Measurement Mode 1)

For measurement mode 1, the TOF between the START to the n^{th} STOP can be calculated using Equation 1:

$$TOF_n = (TIME_n)(normLSB)$$

$$normLSB = \frac{(CLOCKperiod)}{(calCount)}$$

$$calCount = \frac{CALIBRATION2 - CALIBRATION1}{(CALIBRATION2\_PERIODS) - 1}$$

where

- TOF_n [sec] = time-of-flight measurement from the START to the n^{th} STOP
- $TIME_n$ = n^{th} TIME measurement given by the TIME1 to TIME6 registers
- normLSB [sec] = normalized LSB value from calibration
- CLOCKperiod [sec] = external CLOCK period
- CALIBRATION1 = TDCx_CALIBRATION1 register value = TDC count for first calibration cycle
- CALIBRATION2 = TDCx_CALIBRATION2 register value = TDC count for second calibration cycle
- CALIBRATION2_PERIODS = setting for the second calibration cycle; located in register TDCx_CONFIG2 (1)

For example, assume the time-of-flight between the START to the 1^{st} STOP is desired, and the following readouts were obtained:

- TDCx_CALIBRATION2 = 21121 (decimal)
- TDCx_CALIBRATION1 = 2110 (decimal)
- CALIBRATION2_PERIODS = 10
- CLOCK = 8 MHz
- TDCx_TIME1 = 4175 (decimal)

Therefore, the calculation for time-of-flight is:

- calCount = (21121 – 2110) / (10 – 1) = 2112.33
- normLSB = (1/8MHz) / (2112.33) = 59.17 ps
- TOF1 = (4175)(5.917 x 10^{-11}) = 247.061 ns

7.4.2.2 Measurement Mode 2

In measurement mode 2, the internal ring oscillator of each TDCx of the TDC7201 is used only to count fractional parts of the total measured time. As shown in Figure 23, the internal ring oscillator starts counting from when it receives the START signal until the first rising edge of the CLOCK. Then, the internal ring oscillator switches off, and the Clock counter starts counting the clock cycles of the external CLOCK input until a STOP pulse is received. The internal ring oscillator again starts counting from the STOP signal until the next rising edge of the CLOCK.

Device Functional Modes (continued)

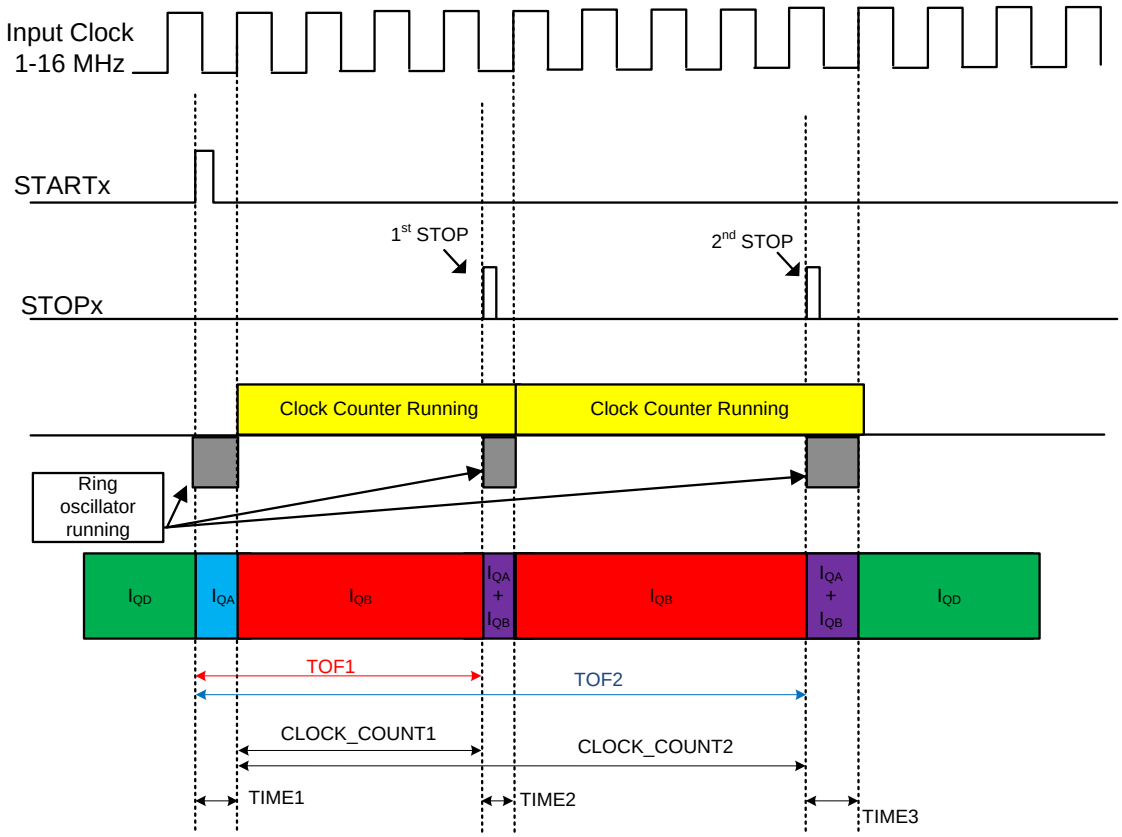


Figure 23. Measurement Mode 2

Device Functional Modes (continued)

7.4.2.2.1 Calculating Time-of-Flight (TOF) (Measurement Mode 2)

The TOF between the START to the n[th] STOP can be calculated using Equation 2:

$$TOF_n = normLSB(TIME1 - TIME_{n+1}) + (CLOCK\_COUNT_n)(CLOCKperiod)$$

$$normLSB = \frac{(CLOCKperiod)}{(calCount)}$$

$$calCount = \frac{CALIBRATION2 - CALIBRATION1}{(CALIBRATION2\_PERIODS) - 1}$$

where

- TOF_n [sec] = time-of-flight measurement from the START to the n[th] STOP
- TIME1 = TDCx_TIME1 register value = time 1 measurement given by the TDC7201 register address 0x10
- $TIME_{(n+1)}$ = $TDCx\_TIME_{(n+1)}$ register value = (n+1) time measurement, where n = 1 to 5 (TDCx_TIME2 to TDCx_TIME6 registers)
- normLSB [sec] = normalized LSB value from calibration
- $CLOCK\_COUNT_n$ = nth clock count, where n = 1 to 5 (TDCx_CLOCK_COUNT1 to TDCx_CLOCK_COUNT5)
- CLOCKperiod [sec] = external CLOCK period
- CALIBRATION1 = TDCx_CALIBRATION1 register value = TDC count for first calibration cycle
- CALIBRATION2 = TDCx_CALIBRATION2 register value = TDC count for second calibration cycle
- CALIBRATION2_PERIODS = setting for the second calibration; located in register TDCx_CONFIG2 (2)

For example, assume the time-of-flight between the START to the 1[st] STOP is desired, and the following readouts were obtained:

- CALIBRATION2 = 23133 (decimal)
- CALIBRATION1 = 2315 (decimal)
- CALIBRATION2_PERIODS = 10
- CLOCK = 8 MHz
- TIME1 = 2147 (decimal)
- TIME2 = 201 (decimal)
- CLOCK_COUNT1 = 318 (decimal)

Therefore, the calculation for time-of-flight is:

$$calCount = \frac{CALIBRATION2 - CALIBRATION1}{(CALIBRATION2\_PERIODS) - 1} = \frac{(23133 - 2315)}{(10 - 1)} = 2313.11$$

$$normLSB = \frac{(CLOCKperiod)}{(calCount)} = \frac{(1/8MHz)}{2313.11} = 54\ ps$$

$$TOF1 = (TIME1)(normLSB) + (CLOCK\_COUNT1)(CLOCKperiod) - (TIME2)(normLSB)$$

$$TOF1 = (2147)\left(5.40 * 10^{-11}\right) + (318)(1/8MHz) - (201)(5.40 * 10^{-11})$$

$$TOF1 = 39.855\mu s \quad (3)$$

Device Functional Modes (continued)

7.4.3 Timeout

For one STOP, each TDCx of the TDC7201 performs the measurement by counting from the START signal to the STOP signal. If no STOP signal is received, either the Clock Counter or Coarse Counter will overflow and will generate an interrupt (see *Coarse and Clock Counters Overflow*). If no START signal is received, the timer waits indefinitely for a START signal to arrive.

For multiple STOPs, each TDCx performs the measurement by counting from the START signal to the last STOP signal. All earlier STOP signals are captured and stored into the corresponding Measurement Results registers (TDCx_TIME1 to TDCx_TIME6, TDCx_CLOCK_COUNT1 to TDCx_CLOCK_COUNT5, TDCx_CALIBRATION1, TDCx_CALIBRATION2). The minimum time required between two consecutive STOP signals is defined in the *Recommended Operating Conditions* table. The device can be programmed to measure up to 5 STOP signals by setting the NUM_STOP bits in the TDCx_CONFIG2 register.

7.4.4 Multi-Cycle Averaging

In the Multi-Cycle Averaging Mode, the TDC7201 will perform a series of measurements on its own and will only send an interrupt to the MCU (for example, MSP430, C2000, and so forth) for wake up after the series has been completed. While waiting, the MCU can remain in sleep mode during the whole cycle (as shown in Figure 24).

Multi-Cycle Averaging Mode Setup and Conditions:

- The number of averaging cycles should be selected (1 to 128). This is done by programming the AVG_CYCLES bit in the TDCx_CONFIG2 register.
- The results of all measurements are reported in the Measurement Results registers (TDCx_TIME1 to TDCx_TIME6, TDCx_CLOCK_COUNT1 to TDCx_CLOCK_COUNT5, TDCx_CALIBRATION1, TDCx_CALIBRATION2 registers). The CLOCK_COUNTn registers should be right shifted by the log2(AVG_CYCLES) before calculating the TOF. For example, if using the multi-cycle averaging mode, Equation 2 should be rewritten as: TOFn = normLSB [TDCx_TIME1 - TDCx_TIME(n+1)] + [TDCx_CLOCK_COUNTn >> log 2 (AVG_CYCLES)] x [CLOCKperiod]
- Following each average cycle, the TDCx generates either a trigger event on the TRIGGx pin after the calibration measurement to commence a new measurement or an interrupt on the INTBx pin, indicating that the averaging sequence has completed.

This mode allows multiple measurements without MCU interaction, thus optimizing power consumption for the overall system.

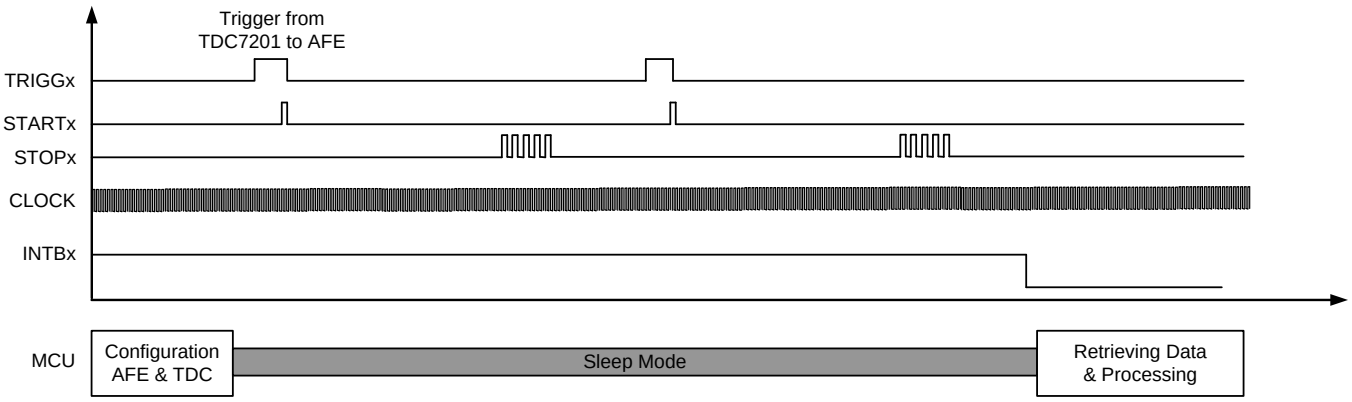


Figure 24. Multi-Cycle Averaging Mode Example with 2 Averaging Cycles and 5 STOP Signals

7.4.5 START and STOP Edge Polarity

In order to achieve the highest measurement accuracy, having the same edge polarity for the START and STOP input signals is highly recommended. Otherwise, slightly different propagation delays due to symmetry shift between the rising and falling edge configuration will impact the measurement accuracy.

Device Functional Modes (continued)

For highest measurement accuracy in measurement mode 2, TI recommends to choose for the START and STOP signal the *rising edge*. This is done by setting the START_EDGE and STOP_EDGE bits in the TDCx_CONFIG1 register to 0.

7.4.6 Measurement Sequence

The TDC7201 has two built-in TDCs with the capability to simultaneously and individually measure time delay on two pairs of START and STOP pins. Each TDCx is a stopwatch that measures time between a single event (edge on STARTx pin) and multiple subsequent events (edge on STOPx pin). The measurement sequence for each TDCx is as follows:

1. After powering up the device, the ENABLE pin needs to be low. There is one low to high transition required while VDD is supplied for correct initialization of the device.

NOTE

Pins VDD1 and VDD2 must be tied together at the board level and supplied from the same source.

2. MCU software requests new TDCx measurements to be initiated through the SPI™ interface.
3. After the start new measurement bit START_MEAS has been set in the TDCx_CONFIG1 register, the TDCx generates a trigger signal on the TRIGGx pin, which is typically used by the corresponding ultrasonic analog-front-end (such as the TDC1000) as start trigger for a measurement (for example, transmit signal for the ultrasonic burst).
4. Immediately after sending the trigger, the TDCx enables the STARTx pin and waits to receive the START pulse edge.
5. After receiving a START, the TDCx resets the TRIGGx pin.
6. The Clock counter is started after the next rising edge of the external clock signal (Measurement Mode 2). The Clock Counter STOP Mask registers (TDCx_CLOCK_CNTR_STOP_MASK_H and TDCx_CLOCK_CNTR_STOP_MASK_L) determine the length of the STOP mask window.
7. After reaching the Clock Counter STOP Mask value, the STOPx pin waits to receive a single or multiple STOP trigger signal from the analog-front-end (for example, detected echo signal of the ultrasonic burst signal).
8. After the last STOP trigger has been received, the TDCx will signal to the MCU through interrupt (INTBx pin) that there are new measurement results waiting in the registers. STARTx, STOPx and TRIGGx pins are disabled (in Multi-Cycle Averaging Mode, the TDCx will start the next cycle automatically by generating a new TRIGG signal). INTBx goes back to high whenever a new measurement is initiated through SPI or when the TDCx_INT_STATUS register bit NEW_MEAS_INT is cleared by writing a 1 to it.

NOTE

INTBx must be utilized to determine TDCx measurement completion; polling the TDCx_INT_STATUS register to determine measurement completion is NOT recommended as it will interfere with the TDCx measurement.

9. After the results are retrieved, the MCU can then start a new measurement with the same register settings. This is done by just setting the START_MEAS bit through SPI. It is not required to drive the ENABLE pin low between measurements.
10. The ENABLE pin can be taken low, if the time duration between measurements is long, and it is desired to put the TDC7201 in its lowest power state. However, upon taking ENABLE high again, the device will come up with its default register settings and will need to be configured through SPI.

The two TDCs of TDC7201 can be used independently to measure TOF. When used independently, the TDCx operation is as explained in the measurement sequence steps above. In this case, each TDCx has dedicated START, STOP inputs and measures their STARTx to STOPx time individually when the START_MEAS bit in the TDCx_CONFIG1 register is set. The MCU has to set up, control, and read the results from the two TDCs individually through the master SPI interface. To set up the registers and read back measurement results of TDCx, MCU needs to perform SPI read and write transactions with corresponding CSBx asserted.

Device Functional Modes (continued)

NOTE

START1, STOP1 and START2, STOP2 inputs can be separate from different sources or can be identical with START1 connected to START2 and STOP1 connected to STOP2. In the latter case, when the TDCx inputs are connected together and the TDCx register setup is identical, then both the TDCs measure the same input in parallel and this can be used to achieve finer resolution. By measuring the same time with both TDCs and taking the average, the LSB resolution is halved.

7.4.7 Wait Times for TDC7201 Startup

The required wait time following the rising edge of the ENABLE pin of the TDC7201 is defined by three key times, as shown in Figure 25. All three times relate to the startup of the TDCx's internal dedicated LDO, which is power gated when the device is disabled for optimal power consumption. The first parameter, $T1_{SPI\_RDY}$, is the time after which the SPI interface is accessible. The second ($T2_{LDO\_SET1}$) parameter and third ($T3_{LDO\_SET2}$) parameter are related to the performance of a measurement made while the internal LDO is settling. The LDO supplies the TDC7201's time measurement device, and a change in voltage on its supply during a measurement translates directly to an inaccuracy. It is therefore recommended to wait until the LDO is settled before time measurement begins.

The first time period relating to the measurement accuracy is $T2_{LDO\_SET1}$, the LDO settling time 1. This is the time after which the LDO has settled to within 0.3% of its final value. A 0.3% error translates to a worst case time error (due to the LDO settling) of 0.3% × t_{CLOCK}, which is 375 ps in the case of an 8-MHz reference clock, or 187.5 ps if a 16-MHz clock is used. Finally, the time $T3_{LDO\_SET2}$ is the time after which the LDO has settled to its final value. For best performance, TI recommends that a time measurement is not started before $T3_{LDO\_SET2}$ to allow the LDO to fully settle. Typical times for these parameters are: $T1_{SPI\_RDY}$ is 100 µs, for $T2_{LDO\_SET1}$ is 300 µs, and for $T3_{LDO\_SET2}$ is 1.5 ms.

Device Functional Modes (continued)

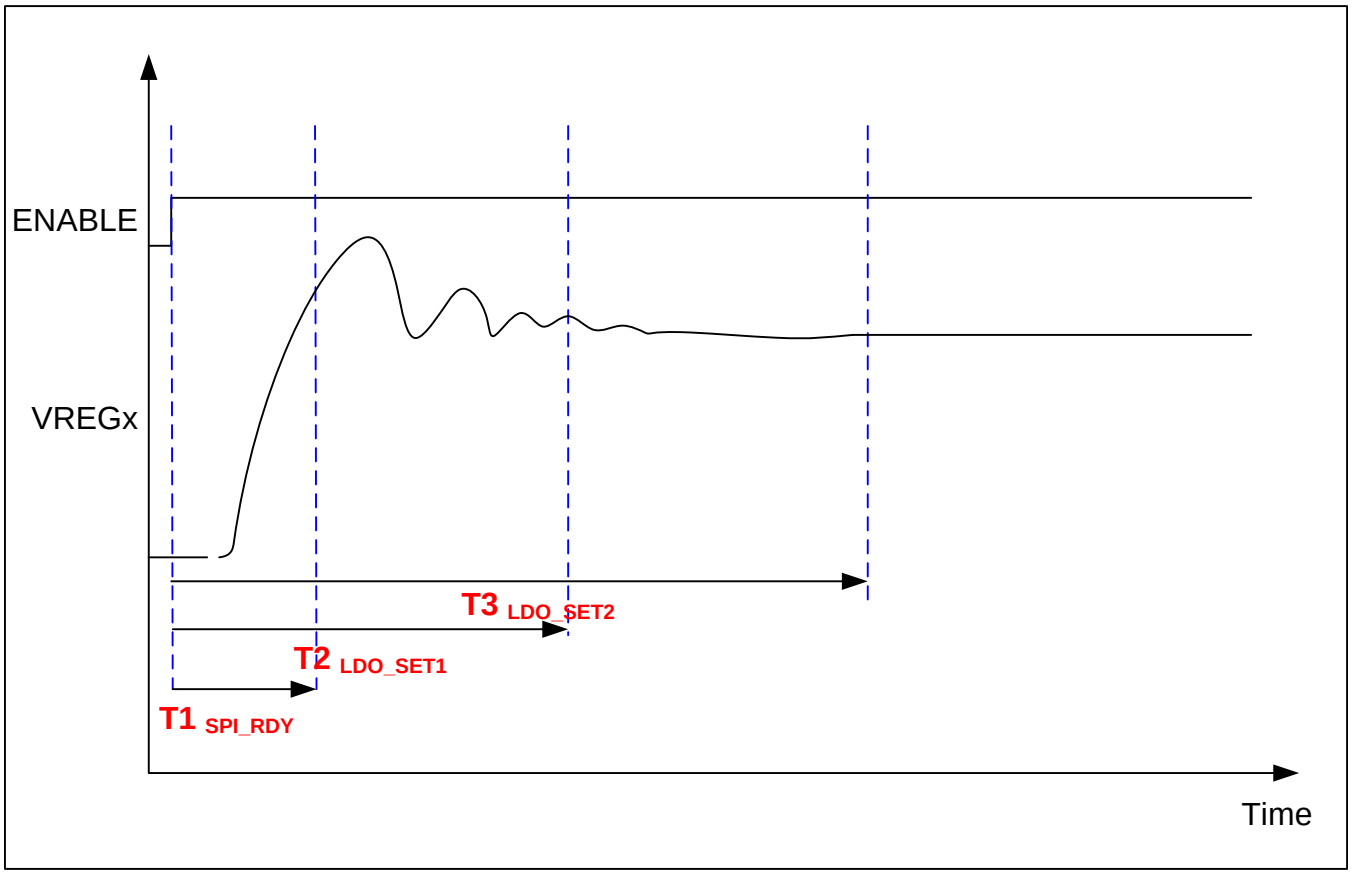


Figure 25. VREGx Startup Time

7.5 Programming

7.5.1 Serial Peripheral Interface (SPI)

The serial interface consists of data input (DIN), data output (DOUTx), serial interface clock (SCLK), and chip select bar (CSBx). The serial interface is used to configure the TDC7201 parameters available in various configuration registers.

The two TDCs of TDC7201 share the serial interface DIN and SCLK pins but support dedicated CSB and DOUT pins. Registers of the TDCx are selected for read/write access when their corresponding dedicated CSBx pin is asserted. By connecting together DOUT1 and DOUT2, a single SPI master interface of the MCU can be used to access both the TDC register sets by asserting the corresponding CSBx. Alternatively, by keeping DOUT1 and DOUT2 separate, data can be read out of the TDCs in parallel using their dedicated DOUTx pins. This doubles the data readout throughput but requires a second dedicated SPI interface of the MCU.

The communication on the SPI bus supports write and read transactions. A write transaction consists of a single write command byte, followed by single data byte. A read transaction consists of a single read command byte followed by 8 or 24 SCLK cycles. The write and read command bytes consist of a 1-bit auto-increment bit, a 1-bit read or write instruction, and a 6-bit register address. Figure 26 shows the SPI protocol for a transaction involving one byte of data (read or write).

Programming (continued)

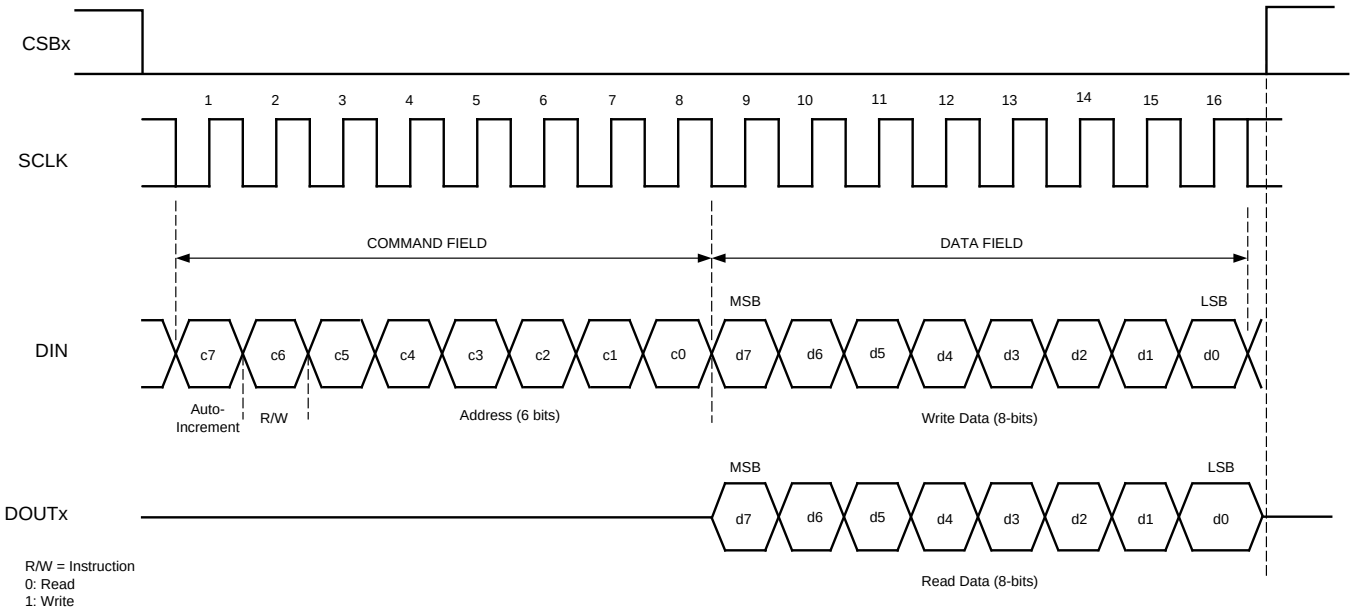


Figure 26. SPI Protocol

7.5.1.1 CSBx

CSBx is an active-low signal and needs to be low throughout a transaction. That is, CSBx should not pulse between the command byte and the data byte of a single transaction.

De-asserting CSBx always terminates an ongoing transaction, even if it is not yet complete. Re-asserting CSBx will always bring the device into a state ready for the next transaction, regardless of the termination status of a previous transaction.

Registers of the TDCx are selected for read/write access when their corresponding dedicated CSBx pin is asserted.

7.5.1.2 SCLK

SPI clock can idle high or low. TI recommends to keep SCLK as clean as possible to prevent glitches from corrupting the SPI frame.

7.5.1.3 DIN

Data In (DIN) is driven by the SPI master by sending the command and the data byte to configure the TDC7201.

7.5.1.4 DOUTx

Data Out (DOUTx) is driven by the TDC7201 when the SPI master initiates a read transaction with CSBx asserted. When the TDC7201 is not being read out, the DOUT pin is in high impedance mode and is undriven.

Registers of the TDCx are selected for read/write access when their corresponding dedicated CSBx pin is asserted. By connecting together DOUT1 and DOUT2, a single SPI master interface of the MCU can be used to access both the TDC register sets by asserting the corresponding CSBx. Alternatively, by keeping DOUT1 and DOUT2 separate, data can be read out of the TDCs in parallel using their dedicated DOUTx pins. This doubles the data readout throughput but requires a second dedicated SPI interface of the MCU.

7.5.1.5 Register Read/Write

Access to the TDCx internal registers can be done through the serial interface formed by pins CSBx (Chip Select - active low), SCLK (serial interface clock), DIN (data input), and DOUTx (data out).

Programming (continued)

Serial shift of bits into the TDCx is enabled when CSBx is low. Serial data DIN is latched (MSB received first, LSB received last) at every rising edge of SCLK when CSBx is active (low). The serial data is loaded into the register with the last data bit SCLK rising edge when CSBx is low. In the case that the word length exceeds the register size, the excess bits are ignored. The interface can work with SCLK frequency from 25 MHz down to very low speeds (a few Hertz) and even with a non-50% duty-cycle SCLK.

The SPI transaction is divided in two main portions:

- Address and Control as shown in Table 1: Auto Increment Mode selection bit, Read/Write bit, Address 6 bits
- Data: 8 bit or 24 bit

When writing to a register with unused bits, these should be set to 0.

Table 1. Address and Control Byte of SPI transaction

Address and Control (A7 - A0)							
A7	A6	A5	A4	A3	A2	A1	A0
Auto Increment	RW	Register Address					
0: OFF 1: ON	Read = 0 Write = 1	00 h up to 3Fh					

7.5.1.6 Auto Increment Mode

When the Auto Increment Mode is OFF, only the register indicated by the Register Address will be accessed, all cycles beyond the register length will be ignored. When the Auto Increment is ON, the register of the Register Address is accessed first, then without interruption, subsequent registers are accessed.

The Auto Increment Mode can be either used to access the configuration (TDCx_CONFIG1 and TDCx_CONFIG2) and status (TDCx_INT_STATUS) registers, or for the Measurement Results registers (TDCx_TIME1 to TDCx_TIME6, TDCx_CLOCK_COUNT1 to TDCx_CLOCK_COUNT5, TDCx_CALIBRATION1, TDCx_CALIBRATION2). As both register block use registers with different length, it is not possible to access all registers of the device within one single access cycle.

7.6 Register Maps

7.6.1 Register Initialization

After power up (VDD supplied, ENABLE Pin low to high transition) the internal registers are initialized with the default value. Disabling the part by pulling ENABLE pin to GND will set the device into total shutdown. As the internal LDO is turned off settings in the register will be lost. The device initializes the registers with default values with the next enable (ENABLE pin to VDD).

Table 2. TDCx_ Register Summary(1)

REGISTER ADDRESS	REGISTER NAME	REGISTER DESCRIPTION	SIZE (BITS)	RESET VALUE
00h	TDCx_CONFIG1	Configuration Register 1	8	00h
01h	TDCx_CONFIG2	Configuration Register 2	8	40h
02h	TDCx_INT_STATUS	Interrupt Status Register	8	00h
03h	TDCx_INT_MASK	Interrupt Mask Register	8	07h
04h	TDCx_COARSE_CNTR_OVF_H	Coarse Counter Overflow Value High	8	FFh
05h	TDCx_COARSE_CNTR_OVF_L	Coarse Counter Overflow Value Low	8	FFh
06h	TDCx_CLOCK_CNTR_OVF_H	CLOCK Counter Overflow Value High	8	FFh
07h	TDCx_CLOCK_CNTR_OVF_L	CLOCK Counter Overflow Value Low	8	FFh
08h	TDCx_CLOCK_CNTR_STOP_MASK_H	CLOCK Counter STOP Mask High	8	00h
09h	TDCx_CLOCK_CNTR_STOP_MASK_L	CLOCK Counter STOP Mask Low	8	00h
10h	TDCx_TIME1	Measured Time 1	24	00_0000h
11h	TDCx_CLOCK_COUNT1	CLOCK Counter Value	24	00_0000h
12h	TDCx_TIME2	Measured Time 2	24	00_0000h
13h	TDCx_CLOCK_COUNT2	CLOCK Counter Value	24	00_0000h
14h	TDCx_TIME3	Measured Time 3	24	00_0000h
15h	TDCx_CLOCK_COUNT3	CLOCK Counter Value	24	00_0000h
16h	TDCx_TIME4	Measured Time 4	24	00_0000h
17h	TDCx_CLOCK_COUNT4	CLOCK Counter Value	24	00_0000h
18h	TDCx_TIME5	Measured Time 5	24	00_0000h
19h	TDCx_CLOCK_COUNT5	CLOCK Counter Value	24	00_0000h
1Ah	TDCx_TIME6	Measured Time 6	24	00_0000h
1Bh	TDCx_CALIBRATION1	Calibration 1, 1 CLOCK Period	24	00_0000h
1Ch	TDCx_CALIBRATION2	Calibration 2, 2/10/20/40 CLOCK Periods	24	00_0000h

(1) Registers of the TDCx are selected for read/write access when their corresponding dedicated CSBx pin is asserted.

7.6.2 TDCx_CONFIG1: TDCx Configuration Register 1 R/W (address = 00h, CSBx asserted) [reset = 0h]

Figure 27. TDCx_CONFIG1 Register

7	6	5	4	3	2	1	0
FORCE_CAL	PARITY_EN	TRIGG_EDGE	STOP_EDGE	START_EDGE	MEAS_MODE		START_MEAS
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3. TDCx_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FORCE_CAL	R/W	0	0: Calibration is automatic and performed every time after a measurement. Only if a measurement is interrupted (for example, due to counter overflow or missing STOP signal), calibration is not performed. 1: Calibration is always performed at the end (for example, after a counter overflow) even if a measurement is interrupted.
6	PARITY_EN	R/W	0	0: Parity bit for Measurement Result Registers* disabled (Parity Bit always 0) 1: Parity bit for Measurement Result Registers enabled (Even Parity) *The Measurement Results registers are the TDCx_TIME1 to TDCx_TIME6, TDCx_CLOCK_COUNT1 to TDCx_CLOCK_COUNT5, TDCx_CALIBRATION1, TDCx_CALIBRATION2 registers.
5	TRIGG_EDGE	R/W	0	0: TRIGG is output as a Rising edge signal 1: TRIGG is output as a Falling edge signal
4	STOP_EDGE	R/W	0	0: Measurement is stopped on Rising edge of STOP signal 1: Measurement is stopped on Falling edge of STOP signal
3	START_EDGE	R/W	0	0: Measurement is started on Rising edge of START signal 1: Measurement is started on Falling edge of START signal
[2:1]	MEAS_MODE	R/W	b00	00: Measurement Mode 1 (for expected time-of-flight < 2000 ns). 01: Measurement Mode 2 (recommended) 10, 11: Reserved for future functionality
0	START_MEAS	R/W	0	Start New Measurement: This bit is cleared when Measurement is Completed. 0: No effect 1: Start New Measurement. Writing a 1 will clear all bits in the Interrupt Status Register and Start the measurement (by generating a TRIGG signal) and will reset the content of all Measurement Results registers (TDCx_TIME1 to TDCx_TIME6, TDCx_CLOCK_COUNT1 to TDCx_CLOCK_COUNT5, TDCx_CALIBRATION1, TDCx_CALIBRATION2) to 0.

7.6.3 TDCx_CONFIG2: TDCx Configuration Register 2 R/W (address = 01h, CSBx asserted) [reset = 40h]

Figure 28. TDCx_CONFIG2 Register

7	6	5	4	3	2	1	0
CALIBRATION2_PERIODS		AVG_CYCLES			NUM_STOP		
R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. TDCx_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
[7:6]	CALIBRATION2_PERIODS	R/W	b01	00: Calibration 2 - measuring 2 CLOCK periods 01: Calibration 2 - measuring 10 CLOCK periods 10: Calibration 2 - measuring 20 CLOCK periods 11: Calibration 2 - measuring 40 CLOCK periods
[5:3]	AVG_CYCLES	R/W	b000	000: 1 Measurement Cycle only (no Multi-Cycle Averaging Mode) 001: 2 Measurement Cycles 010: 4 Measurement Cycles 011: 8 Measurement Cycles 100: 16 Measurement Cycles 101: 32 Measurement Cycles 110: 64 Measurement Cycles 111: 128 Measurement Cycles
[2:0]	NUM_STOP	R/W	b000	000: Single Stop 001: Two Stops 010: Three Stops 011: Four Stops 100: Five Stops 101, 110, 111: No Effect. Single Stop

7.6.4 TDCx_INT_STATUS: Interrupt Status Register (address = 02h, CSBx asserted) [reset = 00h]

Figure 29. TDCx_INT_STATUS Register

7	6	5	4	3	2	1	0
Reserved			MEAS_COMPLETE_FLAG	MEAS_STARTED_FLAG	CLOCK_CNTR_OVF_INT	COARSE_CNTR_OVF_INT	NEW_MEAS_INT
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. TDCx_INT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 5	Reserved	R/W	b000	
4	MEAS_COMPLETE_FLAG	R/W	0	Writing a 1 will clear the status 0: Measurement has not completed 1: Measurement has completed (same information as NEW_MEAS_INT)
3	MEAS_STARTED_FLAG	R/W	0	Writing a 1 will clear the status 0: Measurement has not started 1: Measurement has started (START signal received)
2	CLOCK_CNTR_OVF_INT	R/W	0	Requires writing a 1 to clear interrupt status 0: No overflow detected 1: Clock overflow detected, running measurement will be stopped immediately
1	COARSE_CNTR_OVF_INT	R/W	0	Requires writing a 1 to clear interrupt status 0: No overflow detected 1: Coarse overflow detected, running measurement will be stopped immediately
0	NEW_MEAS_INT	R/W	0	Requires writing a 1 to clear interrupt status 0: Interrupt not detected 1: Interrupt detected – New Measurement has been completed

7.6.5 TDCx_INT_MASK: TDCx Interrupt Mask Register R/W (address = 03h, CSBx asserted) [reset = 07h]

Figure 30. TDCx_INT_MASK Register

7	6	5	4	3	2	1	0
Reserved					CLOCK_CNTR _OVF_MASK	COARSE_CNTR _OVF_MASK	NEW_MEAS _MASK
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. TDCx_INT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7 - 3	Reserved	R/W	b0'0000	
2	CLOCK_CNTR_OVF_MASK	R/W	1	0: CLOCK Counter Overflow Interrupt disabled 1: CLOCK Counter Overflow Interrupt enabled
1	COARSE_CNTR_OVF_MASK	R/W	1	0: Coarse Counter Overflow Interrupt disabled 1: Coarse Counter Overflow Interrupt enabled
0	NEW_MEAS_MASK	R/W	1	0: New Measurement Interrupt disabled 1: New Measurement Interrupt enabled

A disabled interrupt will no longer be visible on the device pin (INTB). The interrupt bit in the TDCx_INT_STATUS register will still be active.

7.6.6 TDCx_COARSE_CNTR_OVF_H: Coarse Counter Overflow High Value Register (address = 04h, CSBx asserted) [reset = FFh]

Figure 31. TDCx_COARSE_CNTR_OVF_H Register

7	6	5	4	3	2	1	0
COARSE_CNTR_OVF_H							
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. TDCx_COARSE_CNTR_OVF_H Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	COARSE_CNTR_OVF_H	R/W	FFh	Coarse Counter Overflow Value, upper 8 Bit

7.6.7 TDCx_COARSE_CNTR_OVF_L: TDCx Coarse Counter Overflow Low Value Register (address = 05h, CSBx asserted) [reset = FFh]

Figure 32. TDCx_COARSE_CNTR_OVF_L Register

7	6	5	4	3	2	1	0
COARSE_CNTR_OVF_L							
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. TDCx_COARSE_CNTR_OVF_L Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	COARSE_CNTR_OVF_L	R/W	FFh	Coarse Counter Overflow Value, lower 8 Bit Note: Do not set COARSE_CNTR_OVF_L to 1.

7.6.8 TDCx_CLOCK_CNTR_OVF_H: Clock Counter Overflow High Register (address = 06h, CSBx asserted) [reset = FFh]

Figure 33. TDCx_CLOCK_CNTR_OVF_H Register

7	6	5	4	3	2	1	0
CLOCK_CNTR_OVF_H							
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. TDCx_CLOCK_CNTR_OVF_H Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK_CNTR_OVF_H	R/W	FFh	CLOCK Counter Overflow Value, upper 8 Bit

7.6.9 TDCx_CLOCK_CNTR_OVF_L: Clock Counter Overflow Low Register (address = 07h, CSBx asserted) [reset = FFh]

Figure 34. TDCx_CLOCK_CNTR_OVF_L Register

7	6	5	4	3	2	1	0
CLOCK_CNTR_OVF_L							
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. TDCx_CLOCK_CNTR_OVF_L Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK_CNTR_OVF_L	R/W	FFh	CLOCK Counter Overflow Value, lower 8 Bit

7.6.10 TDCx_CLOCK_CNTR_STOP_MASK_H: CLOCK Counter STOP Mask High Value Register (address = 08h, CSBx asserted) [reset = 00h]

Figure 35. TDCx_CLOCK_CNTR_STOP_MASK_H Register

7	6	5	4	3	2	1	0
CLOCK_CNTR_STOP_MASK_H							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. TDCx_CLOCK_CNTR_STOP_MASK_H Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK_CNTR_STOP_MASK_H	R/W	00h	CLOCK Counter STOP Mask, upper 8 Bit

7.6.11 TDCx_CLOCK_CNTR_STOP_MASK_L: CLOCK Counter STOP Mask Low Value Register (address = 09h, CSBx asserted) [reset = 00h]

Figure 36. TDCx_CLOCK_CNTR_STOP_MASK_L Register

7	6	5	4	3	2	1	0
CLOCK_CNTR_STOP_MASK_L							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. TDCx_CLOCK_CNTR_STOP_MASK_L Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLOCK_CNTR_STOP_MASK_L	R/W	00h	CLOCK Counter STOP Mask, lower 8 Bit

7.6.12 TDCx_TIME1: Time 1 Register (address: 10h, CSBx asserted) [reset = 00_0000h]

Figure 37. TDCx_TIME1 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	TIME1: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. TDCx_TIME1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-0	TIME1	R	00 0000h	23 bits, TIME1 measurement result

7.6.13 TDCx_CLOCK_COUNT1: Clock Count Register (address: 11h, CSBx asserted) [reset = 00_0000h]

Figure 38. TDCx_CLOCK_COUNT1 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit								CLOCK_COUNT1															
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. TDCx_CLOCK_COUNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-16	Not Used	R	00h	7 bits, these bits will be used in Multi-Cycle Averaging Mode in order to allow higher averaging results.
15-0	CLOCK_COUNT1	R	0000h	16 bits, CLOCK_COUNT1 measurement result

7.6.14 TDCx_TIME2: Time 2 Register (address: 12h, CSBx asserted) [reset = 00_0000h]

Figure 39. TDCx_TIME2 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	TIME2: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. TDCx_TIME2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity Bit	R	0	Parity Bit
22-0	TIME2	R	00 0000h	23 bits, TIME2 measurement result

7.6.15 TDCx_CLOCK_COUNT2: Clock Count Register (address: 13h, CSBx asserted) [reset = 00_0000h]

Figure 40. TDCx_CLOCK_COUNT2 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit								CLOCK_COUNT2															
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. TDCx_CLOCK_COUNT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity Bit
22-16	Not Used	R	00h	7 bits, these bits will be used in Multi-Cycle Averaging Mode in order to allow higher averaging results.
15-0	CLOCK_COUNT2	R	0000h	16 bits, CLOCK_COUNT2 measurement result

7.6.16 TDCx_TIME3: Time 3 Register (address: 14h, CSBx asserted) [reset = 00_0000h]

Figure 41. TDCx_TIME3 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	TIME3: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. TDCx_TIME3 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity Bit
22-0	TIME3	R	00 0000h	23 bits, TIME3 measurement result

7.6.17 TDCx_CLOCK_COUNT3: Clock Count Registers (address: 15h, CSBx asserted) [reset = 00_0000h]

Figure 42. TDCx_CLOCK_COUNT3 Count Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit								CLOCK_COUNT3															
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. TDCx_CLOCK_COUNT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity bit
22-16	Not Used	R	00h	7 bits, these bits will be used in Multi-Cycle Averaging Mode in order to allow higher averaging results.
15-0	CLOCK_COUNT3	R	0000h	16 bits, CLOCK_COUNT3 measurement result

7.6.18 TDCx_TIME4: Time 4 Register (address: 16h, CSBx asserted) [reset = 00_0000h]

Figure 43. TDCx_TIME4 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	TIME4: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. TDCx_TIME4 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity Bit
22-0	TIME4	R	00 0000h	23 bits, TIME4 measurement result

7.6.19 TDCx_CLOCK_COUNT4: Clock Count Register (address: 17h, CSBx asserted) [reset = 00_0000h]

Figure 44. TDCx_CLOCK_COUNT4 Count Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	CLOCK_COUNT4																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. TDCx_CLOCK_COUNT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity bit
22-16	Not Used	R	00h	7 bits, these bits will be used in Multi-Cycle Averaging Mode in order to allow higher averaging results.
15-0	CLOCK_COUNT4	R	0000h	16 bits, CLOCK_COUNT4 measurement result

7.6.20 TDCx_TIME5: Time 5 Register (address: 18h, CSBx asserted) [reset = 00_0000h]

Figure 45. TDCx_TIME5 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	TIME5: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. TDCx_TIME5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity Bit
22-0	TIME5	R	00 0000h	23 bits, TIME5 measurement result

7.6.21 TDCx_CLOCK_COUNT5: Clock Count Register (address: 19h, CSBx asserted) [reset = 00_0000h]

Figure 46. TDCx_CLOCK_COUNT5 Count Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	CLOCK_COUNT5																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. TDCx_CLOCK_COUNT5 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity bit
22-16	Not Used	R	00h	7 bits, these bits will be used in Multi-Cycle Averaging Mode in order to allow higher averaging results.
15-0	CLOCK_COUNT5	R	0000h	16 bits, CLOCK_COUNT5 measurement result

7.6.22 TDCx_TIME6: Time 6 Register (address: 1Ah, CSBx asserted) [reset = 00_0000h]

Figure 47. TDCx_TIME6 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	TIME6: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. TDCx_TIME6 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity bit	R	0	Parity Bit
22-0	TIME6	R	00 0000h	23 bits, TIME6 measurement result

7.6.23 TDCx_CALIBRATION1: Calibration 1 Register (address: 1Bh, CSBx asserted) [reset = 00_0000h]

Figure 48. TDCx_CALIBRATION1 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	CALIBRATION1: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. TDCx_CALIBRATION1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity BIt	R	0	Parity Bit
22-0	CALIBRATION1	R	00 0000h	23 bits, Calibration 1 measurement result

7.6.24 TDCx_CALIBRATION2: Calibration 2 Register (address: 1Ch, CSBx asserted) [reset = 00_0000h]

Figure 49. TDCx_CALIBRATION2 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Parity Bit	CALIBRATION2: 23 bit integer value (Bit 22: MSB, Bit 0: LSB)																						
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. TDCx_CALIBRATION2 Register Field Descriptions

Bit	Field	Type	Reset	Description
23	Parity BIt	R	0	Parity Bit
22-0	CALIBRATION2	R	00 0000h	23 bits, Calibration 2 measurement result

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TDC7201 is targeted for the TOF measurement of laser pulses. Laser based time-of-flight applications demand picosecond accuracy plus the ability to measure very short durations. The TDC7201 is highly suited for such applications with its wide measurement range of 0.25 ns to 8 ms and high accuracy of 28 ps. It has a single shot resolution of 55 ps which is equivalent to 0.825 cm.

8.2 Typical Application

The TDC7201 can be used in TOF laser range finders to measure distance to a target. Besides surveying and navigation, distance measurement using TOF laser range finders is used for collision avoidance and safety in a number of systems like drones, robotics, and autonomous vehicles. A block diagram of TOF laser range finders is shown in Figure 50. The system consists of a laser pulse emitter or transmitter, an echo receiver, and a TDC. In this system, TDC7201 can measure the round trip time between a light pulse emission and its echo from the target. The light pulse transmitter triggers the TDC7201 measurement by providing the start input and the receiver stops the TDC7201. Using the equation $D = C \times TOF / 2$, where C is the speed of light, the distance D to the target can be calculated once the TOF is known. A TOF of 0.67 ns is equivalent to 10 cm range and 1 cm accuracy corresponds to 67 ps.

Typical Application (continued)

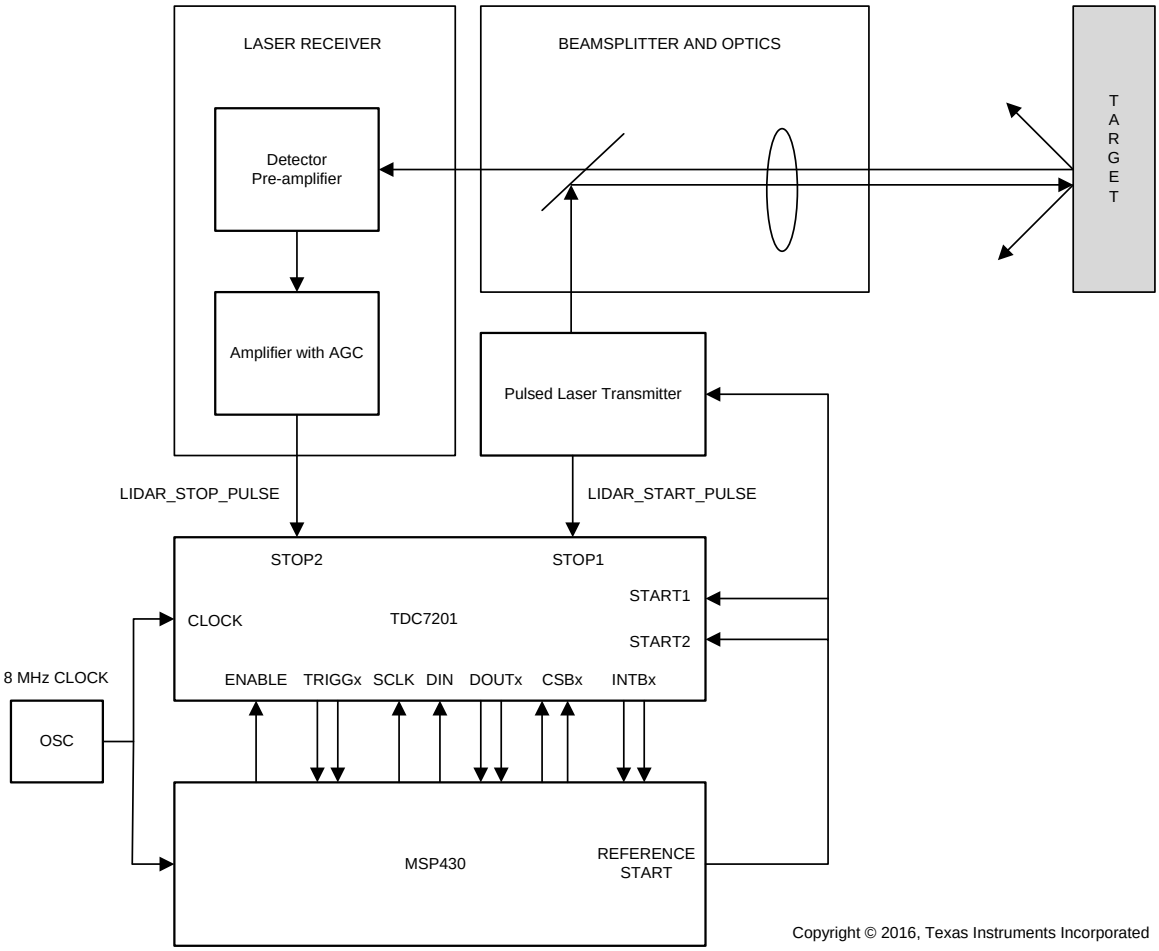


Figure 50. TDC7201 Based TOF Laser Range Finder Block Diagram

8.2.1 Design Requirements

The TOF measurement design is driven by the extreme low measurement range and high accuracy constraints. The TDC7201 has two built-in TDCs to achieve a low measurement range of 4 cm (equivalent to a 0.25 ns TOF). The TDC7201 with its single shot resolution of 55 ps (which is equivalent to 0.825 cm) and built-in averaging of up to 128 samples can enable applications to achieve millimeter or even sub-millimeter precision.

8.2.2 Detailed Design Procedure

8.2.2.1 Measuring Time Periods Less Than 12 ns Using TDC7201

The minimum time measurable in measurement mode 1 is 12 ns. It is feasible to do measurements down to 0.25 ns using the TDC7201 in what is called combined measurement mode. In combined measurement mode, START1 and START2 are connected together:

- A common REFERENCE_START signal is applied to START1 and START2 at least 12 ns before occurrence of actual Start and Stop signals
- TOF Start (LIDAR_START) signal is connected to STOP1
- TOF Stop signal (LIDAR_STOP) is connected to STOP2
- Two time periods T1 (REFERENCE_START to LIDAR_START) and T2 (REFERENCE_START to LIDAR_STOP) are measured and their difference T3 = (T2 - T1) is the required TOF

Typical Application (continued)

An illustration of this combined measurement mode is shown in Figure 51 and Figure 52. It is necessary that the REFERENCE_START pulse is generated at least 12 ns before the LIDAR_START pulse. The REFERENCE_START could be generated by the MCU or by some other timing circuit.

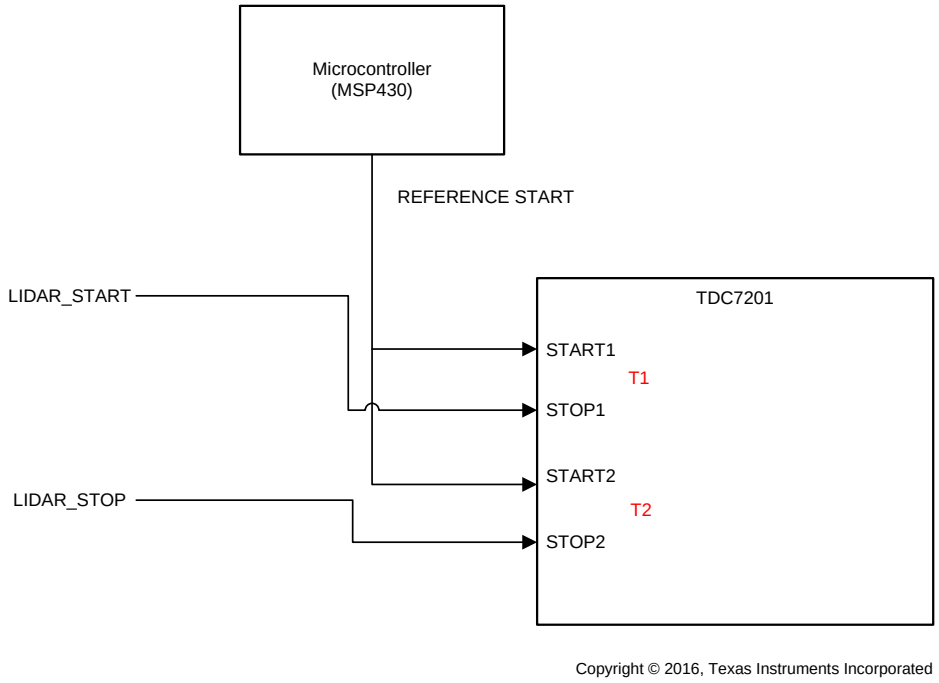


Figure 51. Short Time Measurement Setup

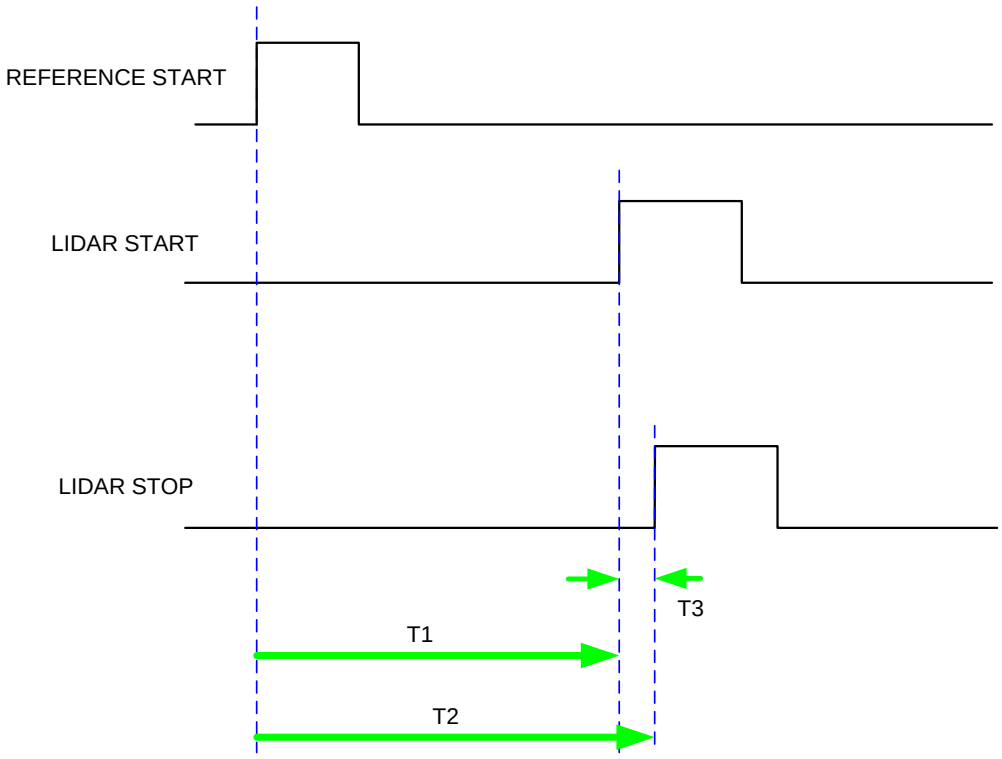


Figure 52. TDC7201 Short Time Measurement Timing

Typical Application (continued)

8.2.3 Application Curves

Figure 53 and Figure 54 show a TOF measurement of 0.25ns using the TDC7201 in combined measurement mode. A Tektronix DTG5078 based test setup was used to generate the TDC7201 START, STOP inputs.

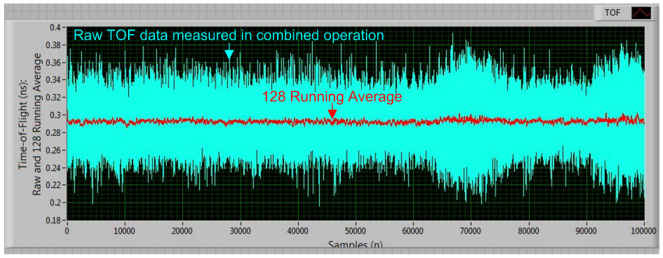


Figure 53. TDC7201 Combined TOF Measurement Data: Raw and 128 x Running Average

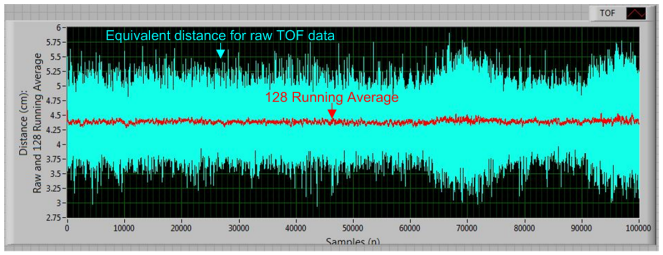


Figure 54. TDC7201 Combined TOF Measurement Data: Equivalent Distance for Raw and 128 x Running Average

8.3 CLOCK Recommendations

A stable, known reference clock is crucial to the ability to measure time, regardless of the time measuring device. Two parameters of a clock source primarily affect the ability to measure time: accuracy and jitter. The following subsection will discuss recommendations for the CLOCK in order to increase accuracy and reduce jitter.

8.3.1 CLOCK Accuracy

CLOCK sources are typically specified with an accuracy value as the clock period is not exactly equal to the nominal value specified. For example, an 8-MHz clock reference may have a 20-ppm accuracy. The true value of the clock period therefore has an error of ±20 ppm, and the real frequency is in the range 7.99984 MHz to 8.00016 MHz [8 MHz ± (8 MHz) x ($20/10^6$)].

If the clock accuracy is at this boundary, but the reference time used to calculate the time of flight relates to the nominal 8-MHz clock period, then the time measured will be affected by this error. For example, if the time period measured is 50 µs, and the 8-MHz reference clock has +50 ppm of error in frequency, but the time measured refers to the 125-ns period (1/8 MHz), then the 50 µs time period will have an error of 50 µs x 50/1000000 = 2.5 ns.

In summary, a clock inaccuracy translates proportionally to a time measurement error.

8.3.2 CLOCK Jitter

Clock jitter introduces uncertainty into a time measurement, rather than inaccuracy. As shown in Figure 55, the jitter accumulates on each clock cycle so the uncertainty associated to a time measurement is a function of the clock jitter and the number of clock cycles measured.

Clock_Jitter_Uncertainty = $(\sqrt{n}) \times (\theta_{JITTER})$, where n is the number of clock cycles counted, and θ_{JITTER} is the cycle-to-cycle jitter of the clock.

For example, if the time measured is 50 µs using an 8-MHz reference clock, n = 50 µs/(1/8 MHz) = 400 clock cycles. If the RMS cycle-to-cycle jitter, θ_{JITTER} = 10 ps, then the RMS uncertainty introduced in a single measurement is in the order of $(\sqrt{n}) \times (\theta_{JITTER})$ = 200 ps.

Because the effect of jitter is random, averaging or accumulating time results reduces the effect of the uncertainty introduced. If the time is measured m times and the result is averaged, then the uncertainty is reduced to: Clock_Jitter_Uncertainty = $(\sqrt{n}) \times (\theta_{JITTER}) / (\sqrt{m})$.

For example, if 64 averages are performed in the example above, then the jitter-related uncertainty is reduced to 25 ps RMS.

CLOCK Recommendations (continued)

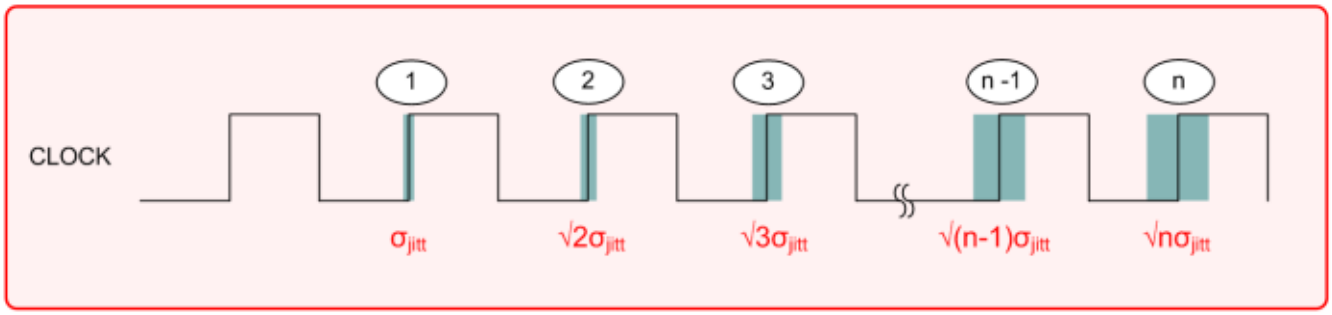


Figure 55. CLOCK Jitter

9 Power Supply Recommendations

The analog circuitry of the TDC7201 is designed to operate from an input voltage supply range between 2 V and 3.6 V. TI recommends to place a 100-nF ceramic bypass capacitor to ground as close as possible to the VDD pins. In addition, an electrolytic or tantalum capacitor with value greater than 1 µF is recommended. The bulk capacitor does not need to be in close vicinity with the TDC7201 and could be close to the voltage source terminals or at the output of the voltage regulators powering the TDC7201.

10 Layout

10.1 Layout Guidelines

- In a 4-layer board design, the recommended layer stack order from top to bottom is: signal, ground, power and signal.
- Bypass capacitors should be placed in close proximity to the VDD pins.
- The length of the START and STOP traces from the TDC7201 to the AFE or MCU should be matched to prevent uneven signal delays. Also, avoid unnecessary via-holes on these traces and keep the routing as short and direct as possible to minimize parasitic capacitance on the PCB.
- Route the SPI signal traces close together. Place a series resistor at the source of DOUT (close to the TDC7201) and series resistors at the sources of DIN, SCLK, and CSB (close to the master MCU).

10.2 Layout Example

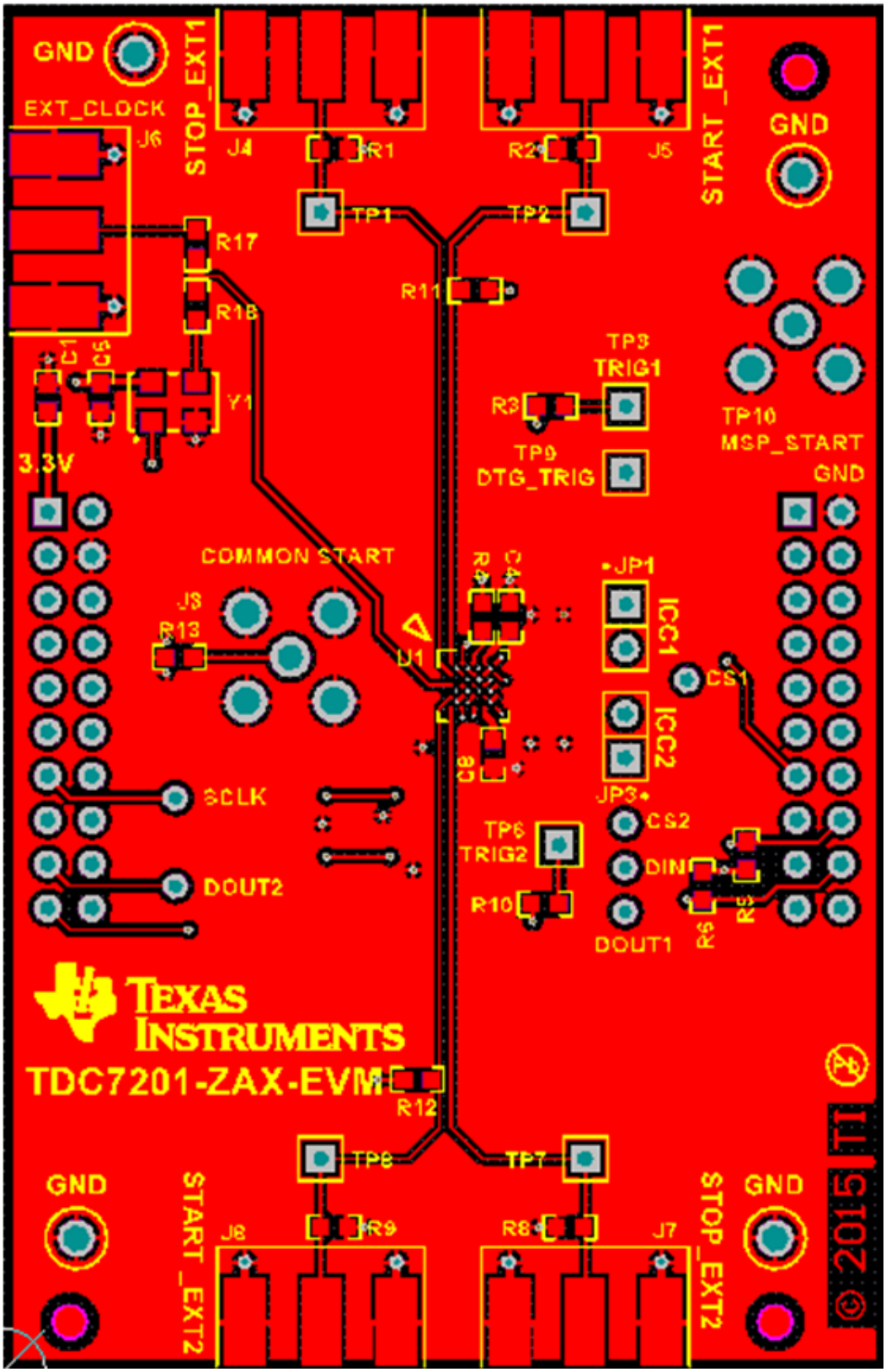


Figure 56. TDC7201EVM Layout

11 器件和文档支持

11.1 文档支持

11.1.1 Third-Party Products Disclaimer

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11.1.2 相关文档

相关文档请参见以下部分：

- 《TDC7200 数据表》（文献编号：SNAS647）
- TDC7200 产品文件夹
- 《TDC1000 数据表》（文献编号：SNAS648）
- TDC1000 产品文件夹

11.2 社区资源

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11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TDC7201ZAXR	ACTIVE	NFBGA	ZAX	25	2000	RoHS & Green	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	TDC7201	Samples
TDC7201ZAXT	OBSOLETE	NFBGA	ZAX	25		TBD	Call TI	Call TI	-40 to 85	TDC7201	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

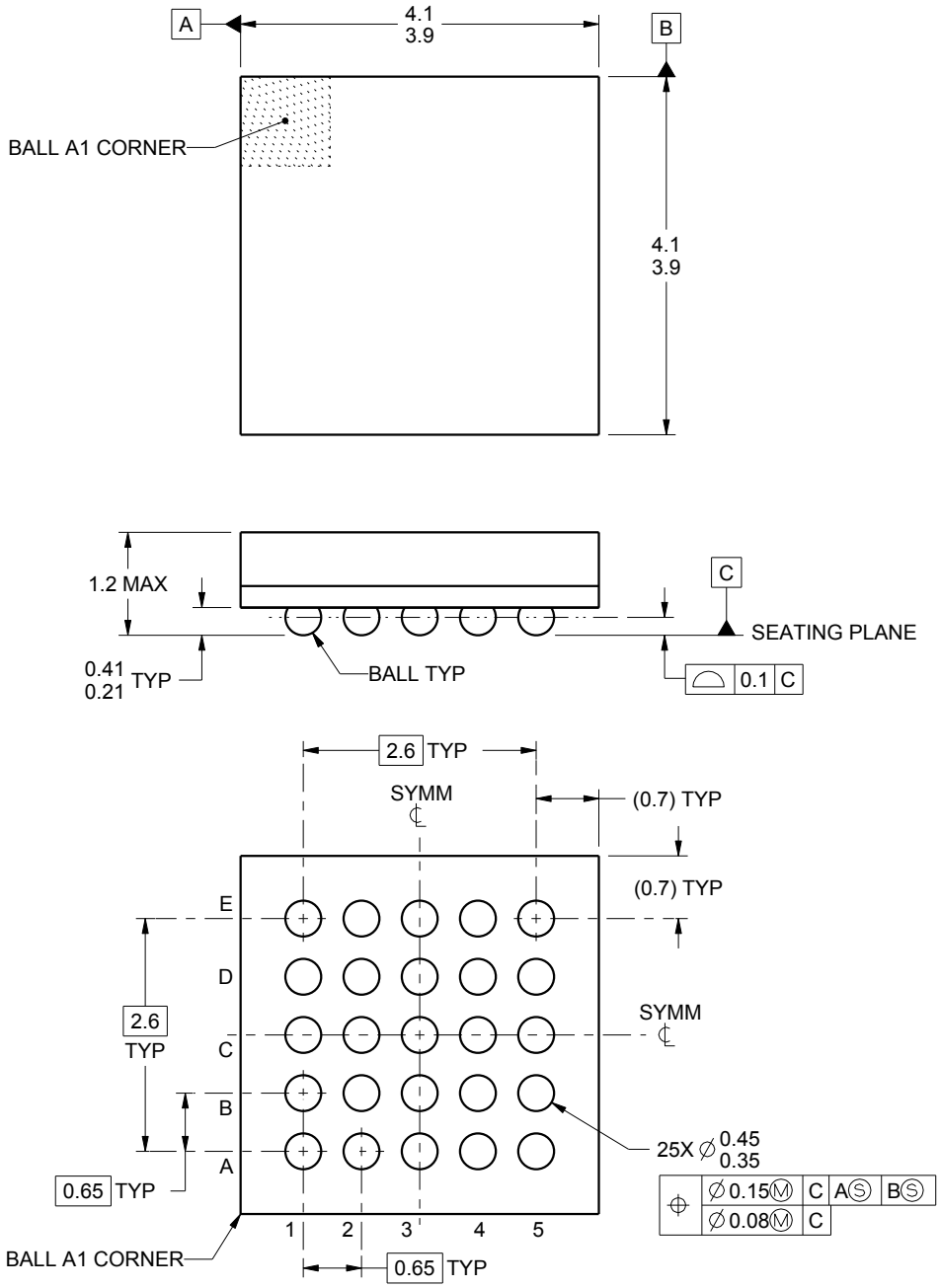
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

ZAX0025A

NFBGA - 1.2 mm max height

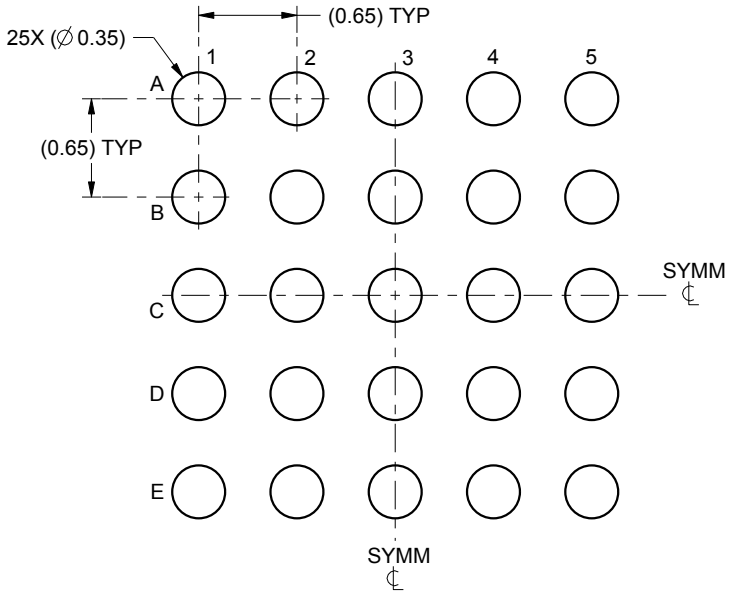
PLASTIC BALL GRID ARRAY



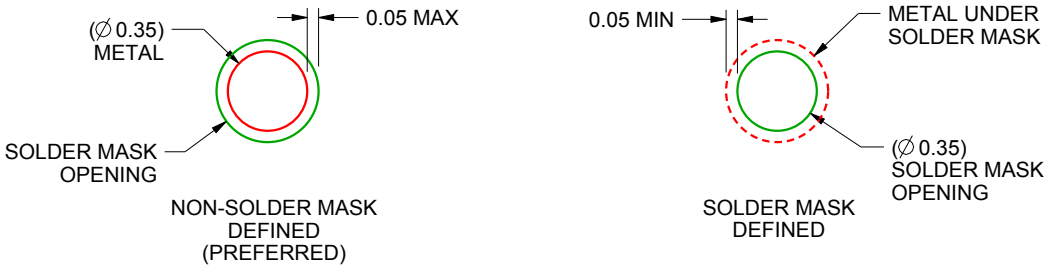
4222623/A 11/20/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:20X

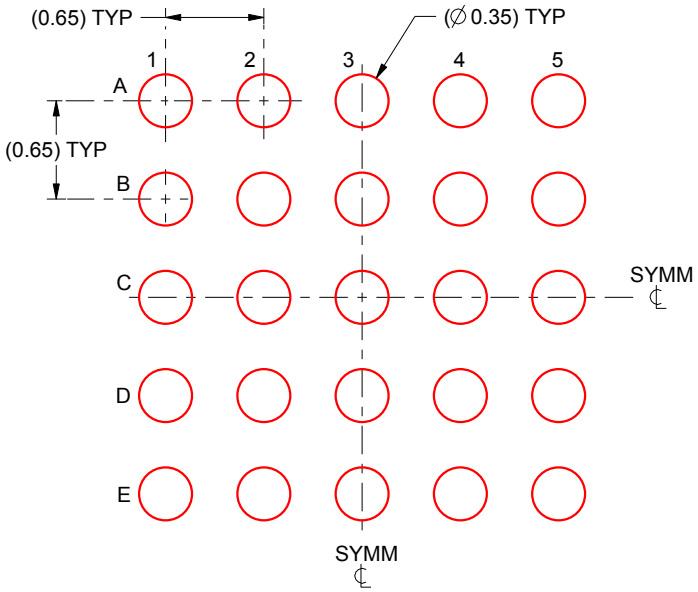


SOLDER MASK DETAILS
NOT TO SCALE

4222623/A 11/20/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:20X

4222623/A 11/20/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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