TFP410 TI PanelBus™ 数字发送器

1 特性

- 符合数字可视接口 (DVI) 技术规范 [1]
- 支持高达 165MHz 的像素速率（包括 60Hz 时的 1080p 和 WUXGA）
- 通用图形控制器接口：
  - 12 位、双边沿和 24 位、单边沿输入模式
  - 可调 1.1V 至 1.8V 和标准 3.3V CMOS 输入信号电平
  - 全差分和单端输入时钟模式
  - 标准 Intel 12 位数字视频端口，与 Intel™ 81x 芯片组兼容
- 增强型 PLL 抗噪性能：
  - 片上稳压器和旁路电容器，可降低系统成本
- 增强的抖动性能：
  - 无 HSYNC 抖动异常
  - 数据相关抖动可忽略不计
- 可使用 I^2C 串行接口进行编程
- 通过热插拔和接收器检测来监控检测
- 单个 3.3V 电源运行
- 采用 TI PowerPAD™ 封装的 64 引脚 TQFP
- TI 先进的 0.18μm EPIC-5™ CMOS 工艺技术
- 与 Sil164 DVI 发送器引脚兼容 [1]

2 应用

- DVD
- 蓝光™
- 高清投影仪
- DVI/HDMI 发送器 [2]

3 说明

TFP410 器件是德州仪器 (TI) 的 PanelBus™ 平板显示产品，是符合 DVI 1.0 标准的全系列端到端解决方案的一部分，面向 PC 和消费类电子产品行业。

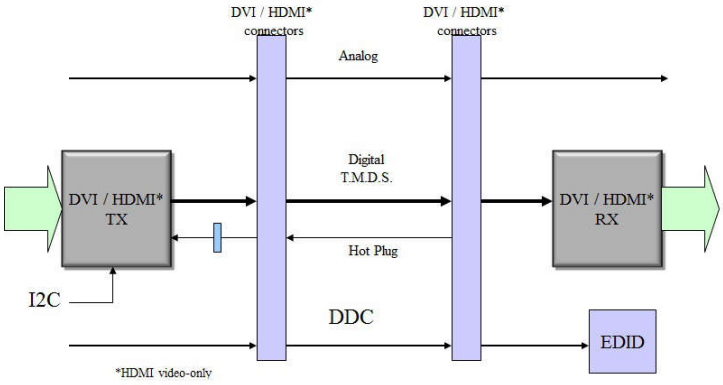
TFP410 器件提供了一个通用接口，可以无缝连接到常用的图形控制器。该通用接口的一些优势包括可选总线宽度、可调信号电平以及差分和单端时钟。1.1V 至 1.8V 可调数字接口提供了一条与 12 位或 24 位接口无缝连接的低 EMI 高速总线。DVI 接口以 24 位真彩像素格式支持高达 165MHz 的 UXGA 平板显示器分辨率。

TFP410 器件将 PanelBus 电路创新与 TI 先进的 0.18 μm EPIC-5 CMOS 工艺技术和 TI 的超低接地电感 PowerPAD 封装相结合，从而得到一个紧凑的 64 引脚 TQFP 封装，提供可靠、低电流、低噪声、高速数字接口解决方案。

封装信息

器件型号	封装(1)	封装尺寸 (2)
TFP410	PAP（HTQFP，64）	12mm x 12mm

(1) 有关更多信息，请参阅节 10
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



典型的 HDMI 接口

[1] 数字可视接口 (DVI) 规范是数字显示工作组 (DDWG) 制定的行业标准，用于数字显示器的高速数字连接，已被业界主要 PC 和消费电子产品制造商采用。TFP410 符合 DVI 修订版 1.0 技术规范。
[2] 仅 HDMI 视频

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

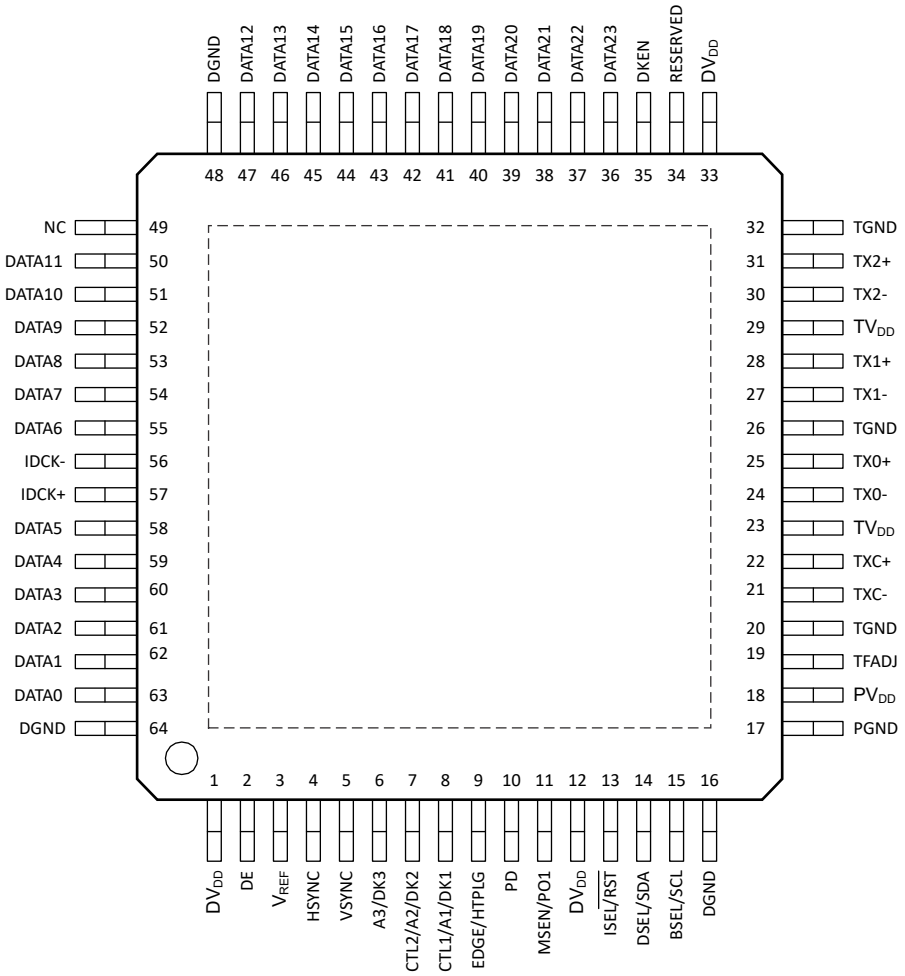


图 4-1. PAP Package, 64 Pin HTQFP (Top View)

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表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
INPUT			
DATA[23:12]	36–47	I	The upper 12 bits of the 24-bit pixel bus In 24-bit, single-edge input mode (BSEL = high), this bus inputs the top half of the 24-bit pixel bus. In 12-bit, dual-edge input mode (BSEL = low), these bits are not used to input pixel data. In this mode, the state of DATA[23:16] is input to the I^2C register CFG. This allows 8 bits of user configuration data to be read by the graphics controller through the I^2C interface (see 节 6.6). Note: All unused data inputs should be tied to GND or V_{DD}.
DATA[11:0]	50–55, 58–63	I	The lower 12 bits of the 24-bit pixel bus/12-bit pixel bus input In 24-bit, single-edge input mode (BSEL = high), this bus inputs the bottom half of the 24-bit pixel bus. In 12-bit, dual-edge input mode (BSEL = low), this bus inputs 1/2 a pixel (12 bits) at every latch edge (both rising and falling) of the clock.
IDCK– IDCK+	56 57	I	Differential clock input. The TFP410 supports both single-ended and fully differential clock input modes. In the single-ended clock input mode, the IDCK+ input (pin 57) should be connected to the single-ended clock source and the IDCK− input (pin 56) should be tied to GND. In the differential clock input mode, the TFP410 uses the crossover point between the IDCK+ and IDCK– signals as the timing reference for latching incoming data DATA[23:0], DE, HSYNC, and VSYNC. The differential clock input mode is only available in the low signal swing mode.
DE	2	I	Data enable. As defined in DVI 1.0 specification, the DE signal allows the transmitter to encode pixel data or control data on any given input clock cycle. During active video (DE = high), the transmitter encodes pixel data, DATA[23:0]. During the blanking interval (DE = low), the transmitter encodes HSYNC, VSYNC and CTL[3:1].
HSYNC	4	I	Horizontal sync input
VSYNC	5	I	Vertical sync input
A3/DK3 CTL2/A2/DK2 CTL1/A1/DK1	6 7 8	I	The operation of these three multifunction inputs depends on the settings of the ISEL (pin 13) and DKEN (pin 35) inputs. All three inputs support 3.3V CMOS signal levels and contain weak pulldown resistors so that if left unconnected they default to all low. When the I^2C bus is disabled (ISEL = low) and the de-skew mode is disabled (DKEN = low), pins 7 and 8 become the control inputs, CTL[2:1], which can be used to send additional information across the DVI link during the blanking interval (DE = low). Pin 6 is not used. When the I^2C bus is disabled (ISEL = low) and the de-skew mode is enabled (DKEN = high), these three inputs become the de-skew inputs DK[3:1], used to adjust the setup and hold times of the pixel data inputs DATA[23:0], relative to the clock input IDCK±. When the I^2C bus is enabled (ISEL = high), these three inputs become the 3 LSBs of the I^2C target address, A[3:1].
CONFIGURATION/PROGRAMMING			
MSEN/PO1	11	O	Monitor sense/programmable output 1. The operation of this pin depends on whether the I^2C interface is enabled or disabled. This pin has an open-drain output and is only 3.3V tolerant. An external 5kΩ pullup resistor connected to V_{DD} is required on this pin. When I^2C is disabled (ISEL = low), a high level indicates a powered on receiver is detected at the differential outputs. A low level indicates a powered on receiver is not detected. This function is only valid in dc-coupled systems. When I^2C is enabled (ISEL = high), this output is programmable through the I^2C interface (see the I^2C register descriptions section).
ISEL/ $\overline{\text{RST}}$	13	I	I^2C interface select/I^2C RESET (active low, asynchronous) If ISEL is high, then the I^2C interface is active. Default values for the I^2C registers can be found in the see 节 6.6. If ISEL is low, then I^2C is disabled and the chip configuration is specified by the configuration pins (BSEL, DSEL, EDGE, VREF) and state pins (PD, DKEN). If ISEL is brought low and then back high, the I^2C state machine is reset. The register values are changed to their default values and are not preserved from before the reset.

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表 4-1. Pin Functions（续）

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BSEL/SCL	15	I	Input bus select/I²C clock input. The operation of this pin depends on whether the I²C interface is enabled or disabled. This pin is only 3.3V tolerant. When I²C is disabled (ISEL = low), a high level selects 24-bit input, single-edge input mode. A low level selects 12-bit input, dual-edge input mode. When I²C is enabled (ISEL = high), this pin functions as the I²C clock input (see 节 6.6). In this configuration, this pin has an open-drain output that requires an external 5kΩ pullup resistor connected to V_{DD}.
DSEL/SDA	14	I/O	DSEL/I²C data. The operation of this pin depends on whether the I²C interface is enabled or disabled. This pin is only 3.3V tolerant. When I²C is disabled (ISEL = low), this pin is used with BSEL and V_{REF} to select the single-ended or differential input clock mode (see 表 6-1). When I²C is enabled (ISEL = high), this pin functions as the I²C bidirectional data line. In this configuration, this pin has an open-drain output that requires an external 5kΩ pullup resistor connected to V_{DD}.
EDGE/HTPLG	9	I	Edge select/hot plug input. The operation of this pin depends on whether the I²C interface is enabled or disabled. This input is 3.3V tolerant only. When I²C is disabled (ISEL = low), a high level selects the primary latch to occur on the rising edge of the input clock IDCK+. A low level selects the primary latch to occur on the falling edge of the input clock IDCK+. This is the case for both single-ended and differential input clock modes. When I²C is enabled (ISEL = high), this pin is used to monitor the hot plug detect signal. When used for *hot-plug* detection, this pin requires a series 1kΩ resistor.
DKEN	35	I	Data de-skew enable. The de-skew function can be enabled either through I²C or by this pin when I²C is disabled. When de-skew is enabled, the input clock to data setup/hold time can be adjusted in discrete trim increments. The amount of trim per increment is defined by $t_{(STEP)}$. When I²C is disabled (ISEL = low), a high level enables de-skew with the trim increment determined by pins DK[3:1] (see 节 6.4.2). A low level disables de-skew and the default trim setting is used. When I²C is enabled (ISEL = high), the value of DKEN and the trim increment are selected through I²C. In this configuration, the DKEN pin should be tied to either GND or V_{DD} to avoid a floating input.
V_{REF}	3	I	Input reference voltage. Selects the swing range of the digital data inputs (DATA[23:0], DE, HSYNC, VSYNC, and IDCK±). For high-swing 3.3V input signal levels, V_{REF} should be tied to V_{DD}. For low-swing input signal levels, V_{REF} should be set to half of the maximum input voltage level. See 节 5.3 for the allowable range for V_{REF}. The desired V_{REF} voltage level is typically derived using a simple voltage-divider circuit.
$\overline{PD}$	10	I	Power down (active low). In the powerdown state, only the digital I/O buffers and I²C interface remain active. When I²C is disabled (ISEL = low), a high level selects the normal operating mode. A low level selects the powerdown mode. When I²C is enabled (ISEL = high), the power-down state is selected through I²C. In this configuration, the $\overline{PD}$ pin should be tied to GND. Note: The default register value for $\overline{PD}$ is low, so the device is in powerdown mode when I²C is first enabled or after an I²C RESET.
RESERVED			
RESERVED	34	I	This pin is reserved and must be tied to GND for normal operation.
DVI DIFFERENTIAL SIGNAL OUTPUT PINS			
TX0+ TX0−	25 24	O	Channel 0 DVI differential output pair. TX0± transmits the 8-bit blue pixel data during active video andHSYNC and VSYNC during the blanking interval.
TX1+ TX1−	28 27	O	Channel 1 DVI differential output pair. TX1± transmits the 8-bit green pixel data during active video and CTL[1] during the blanking interval.
TX2+ TX2−	31 30	O	Channel 2 DVI differential output pair. TX2± transmits the 8-bit red pixel data during active video and CTL[3:2] during the blanking interval.

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表 4-1. Pin Functions（续）

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
TXC+ TXC−	22 21	O	DVI differential output clock.
TFADJ	19	I	Full-scale adjust. This pin controls the amplitude of the DVI output voltage swing, determined by the value of the pullup resistor R_{TFADJ} connected to TV_{DD}.
POWER AND GROUND PINS			
DV_{DD}	1, 12, 33	Power	Digital power supply. Must be set to 3.3V nominal.
PV_{DD}	18	Power	PLL power supply. Must be set to 3.3V nominal.
TV_{DD}	23, 29	Power	Transmitter differential output driver power supply. Must be set to 3.3V nominal.
DGND	16, 48, 64	Ground	Digital ground
PGND	17	Ground	PLL ground
TGND	20, 26, 32	Ground	Transmitter differential output driver ground
NC	49	NC	No connection required. If connected, tie high.

(1) I = input, O = output, NC = no conection, P = power, G = ground

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
DV_{DD}, PV_{DD}, TV_{DD}	Supply voltage range	– 0.5	4	V
	Input voltage, logic/analog signals	– 0.5	4	V
R_T	External DVI single-ended termination resistance		0 to open circuit	Ω
	External TFADJ resistance, RTFADJ		300 to open circuit	Ω
	Case temperature for 10 seconds		260	°C
	JEDEC latch-up (EIA/JESD78)		100	mA
T_{stg}	Storage temperature		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	DVI pins	±4000	V
			All other pins	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage (DV_{DD}, PV_{DD}, TV_{DD})		3.0	3.3	3.6	V
V_{REF}	Input reference voltage	Low-swing mode	0.55	$V_{DDQ}/2$(1)	0.9	V
		High-swing mode			DV_{DD}	V
AV_{DD}	DVI termination supply voltage(2)	DVI receiver	3.14	3.3	3.46	V
R_T	DVI Single-ended termination resistance(3)	DVI receiver	45	50	55	Ω
$R_{(TFADJ)}$	TFADJ resistor for DVI-compliant $V_{(SWING)}$ range	400mV = $V_{(SWING)}$ = 600mV	505	510	515	Ω
T_A	Operating free-air temperature range		0	25	70	°C

(1) V_{DDQ} defines the maximum low-level input voltage, it is not an actual input voltage.
(2) AV_{DD} is the termination supply voltage of the DVI link.
(3) R_T is the single-ended termination resistance at the receiver end of the DVI link.

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5.4 Thermal Information

THERMAL METRIC[1]		TFP410 PAP 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	11.3	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	11.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	

(1) For more information about traditional and new thermal metrics, *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC SPECIFICATIONS						
V_{IH}	High-level input voltage (Data, DE, VSYNC, HSYNC, and IDCK+/- CMOS inputs)	$V_{REF} = DV_{DD}$	$0.7V_{DD}$			V
		$0.5V \leqslant V \leqslant 0.95V$	$V_{REF} + 0.2$			
	High-level input voltage (all other CMOS inputs)		$0.7V_{DD}$			
V_{IL}	Low-level input voltage (Data, DE, VSYNC, HSYNC, and IDCK+/- CMOS inputs)	$V_{REF} = DV_{DD}$			$0.3V_{DD}$	V
		$0.5V \leqslant V \leqslant 0.95V$			$V_{REF} - 0.2$	
	Low-level input voltage (all other CMOS inputs)				$0.3V_{DD}$	
V_{OH}	High-level digital output voltage (open-drain output)	V_{DD} = 3V, I_{OH} = 20 µA	2.4			V
V_{OL}	Low-level digital output voltage (open-drain output)	V_{DD} = 3.6V, I_{OL} = 4mA			0.4	V
I_{IH}	High-level input current	V_I = 3.6V			±25	µA
I_{IL}	Low-level input current	V_I = 0			±25	µA
V_H	DVI single-ended high-level output voltage	AV_{DD} = 3.3V ± 5%, R_T [1] = 50 Ω ± 10%, R_{TFADJ} = 510 Ω ± 1%	$AV_{DD} - 0.01$		$AV_{DD} + 0.01$	V
V_L	DVI single-ended low-level output voltage		$AV_{DD} - 0.6$		$AV_{DD} - 0.4$	V
V_{SWING}	DVI single-ended output swing voltage		400		600	mV_{P-P}
V_{OFF}	DVI single-ended standby/off output voltage		$AV_{DD} - 0.01$		$AV_{DD} + 0.01$	V
I_{PD}	Power-down current[3]			200	500	µA
I_{IDD}	Normal power supply current	Worst-case pattern[2]		200	250	mA
AC SPECIFICATIONS						
$f_{(IDCK)}$	IDCK frequency		25		165	MHz
t_r	DVI output rise time (20-80%)[4]	$f_{(IDCK)}$ = 165MHz	75		240	ps
t_f	DVI output fall time (20-80%)[4]		75		240	ps
$t_{sk(D)}$	DVI output intra-pair + to − differential skew[5], see 图 5-4			50		ps
t_{ojit}	DVI output clock jitter, max.[6]				150	ps
$t_{(STEP)}$	De-skew trim increment	DKEN = 1		350		ps

(1) R_T is the single-ended termination resistance at the receiver end of the DVI link
(2) Black and white checkerboard pattern, each checker is one pixel wide.
(3) Assumes all inputs to the transmitter are not toggling.
(4) Rise and fall times are measured as the time between 20% and 80% of signal amplitude.
(5) Measured differentially at the 50% crossing point using the IDCK+ input clock as a trigger.
(6) Relative to input clock (IDCK).

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5.6 Timing Requirements

			MIN	NOM	MAX	UNIT
$t_{(pixel)}$	Pixel time period(1)		6.06		40	ns
$t_{(IDCK)}$	IDCK duty cycle		30%		70%	
$t_{(ijit)}$	IDCK clock jitter tolerance			2		ns
$t_{sk(CC)}$	DVI output inter-pair or channel-to-channel skew (2), see 图 5-2	$f_{(IDCK)}$ = 165MHz			1.2	ns
$t_{su(IDF)}$	Data, DE, VSYNC, HSYNC setup time to IDCK+ falling edge, see 图 5-2	Single edge (BSEL=1, DSEL=0, DKEN=0, EDGE=0)	1.2			ns
$t_{h(IDF)}$	Data, DE, VSYNC, HSYNC hold time to IDCK+ falling edge, see 图 5-2		1.3			ns
$t_{su(IDR)}$	Data, DE, VSYNC, HSYNC setup time to IDCK+ rising edge, see 图 5-2	Single edge (BSEL=1, DSEL=0, DKEN=0, EDGE=1)	1.2			ns
$t_{h(IDR)}$	Data, DE, VSYNC, HSYNC hold time to IDCK+ rising edge, see 图 5-2		1.3			ns
$t_{su(ID)}$	Data, DE, VSYNC, HSYNC setup time to IDCK+ falling/rising edge, see 图 5-3	Dual edge(BSEL=0, DSEL=1, DKEN=0)	0.9			ns
$t_{h(ID)}$	Data, DE, VSYNC, HSYNC hold time to IDCK+ falling/rising edge, see 图 5-3	Dual edge (BSEL=0, DSEL=1, DKEN=0)	1			ns

(1) $t_{(pixel)}$ is the pixel time defined as the period of the TXC output clock. The period of IDCK is equal to $t_{(pixel)}$.
(2) Measured differentially at the 50% crossing point using the IDCK+ input clock as a trigger.

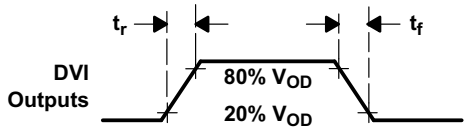


图 5-1. Rise and Fall Time for DVI Outputs

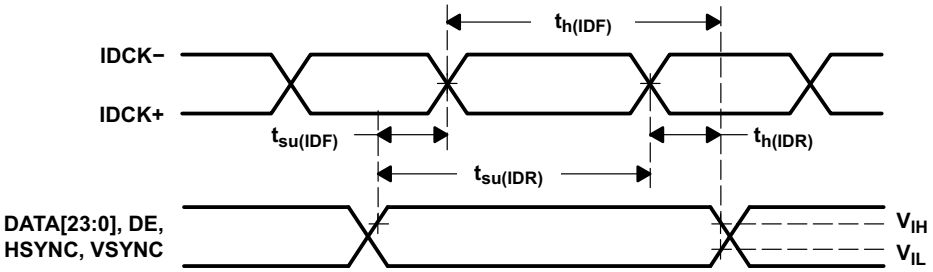


图 5-2. Control and Single-Edge-Data Setup/Hold Time to IDCK±

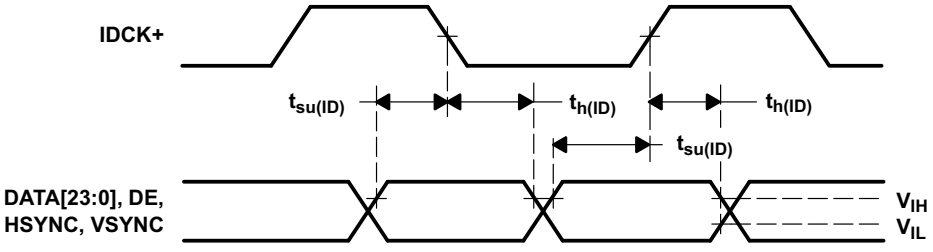


图 5-3. Dual Edge Data Setup/Hold Times to IDCK+

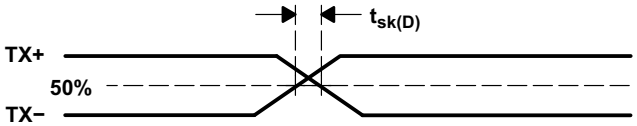


图 5-4. Analog Output Intra-Pair ± Differential Skew

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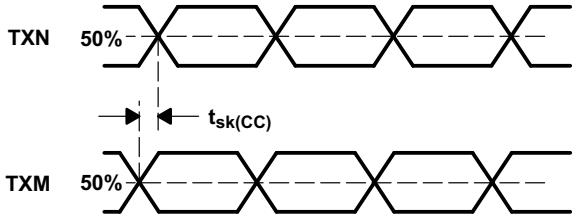


图 5-5. Analog Output Channel-to-Channel Skew

5.7 Typical Characteristics

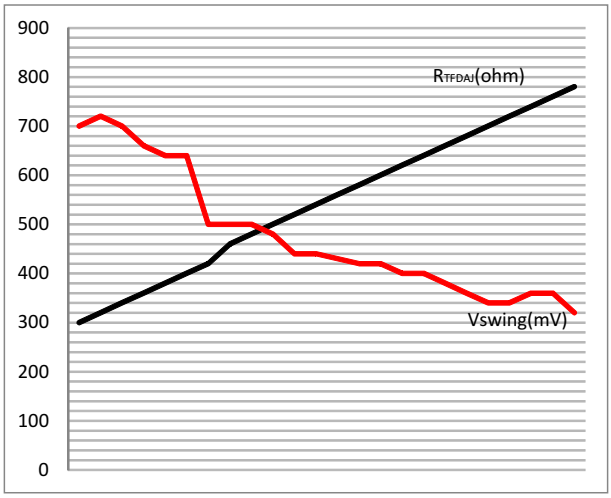


图 5-6. R_{TFDAJ} vs V_{swing}

6 Detailed Description

6.1 Overview

The TFP410 is a DVI-compliant digital transmitter that is used in digital host monitor systems to T.M.D.S. encode and serialize RGB pixel data streams. TFP410 supports resolutions from VGA to WUXGA (and 1080p) and can be controlled in two ways:

1. Configuration and state pins
2. The programmable I^2C serial interface (see 表 6-1)

The host in a digital display system, usually a PC or consumer electronics device, contains a DVI-compatible transmitter such as the TI TFP410 that receives 24-bit pixel data along with appropriate control signals. The TFP410 encodes the signals into a high speed, low voltage, differential serial bit stream optimized for transmission over a twisted-pair cable to a display device. The display device, usually a flat-panel monitor, requires a DVI compatible receiver like the TI TFP401 to decode the serial bit stream back to the same 24-bit pixel data and control signals that originated at the host. This decoded data can then be applied directly to the flat panel drive circuitry to produce an image on the display. Because the host and display can be separated by distances up to 5 meters or more, serial transmission of the pixel data is preferred (see 节 *6.3.1*, 节 *6.3.2*, and 节 *6.3.3*).

The TFP410 integrates a high-speed digital interface, a T.M.D.S. encoder, and three differential T.M.D.S. drivers. Data is driven to the TFP410 encoder across 12 or 24 data lines, along with differential clock pair and sync signals. The flexibility of the TFP410 allows for multiple clock and data formats that enhance system performance.

The TFP410 also has enhanced PLL noise immunity, an enhancement accomplished with on-chip regulators and bypass capacitors.

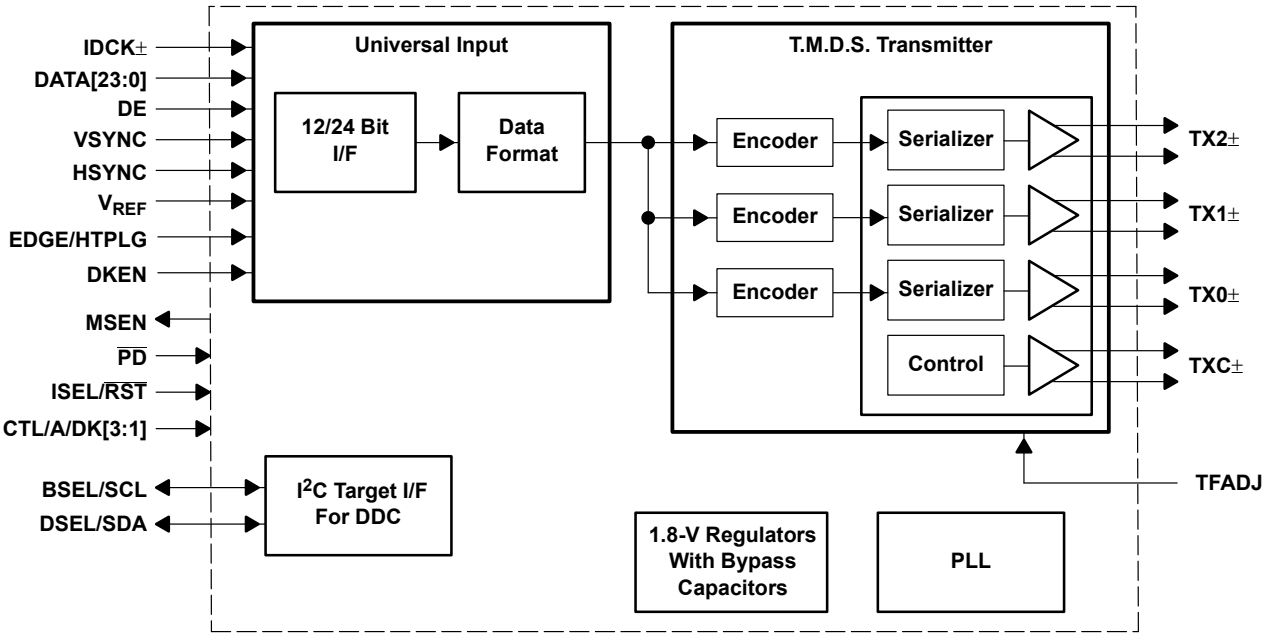
The TFP410 is versatile and highly programmable to provide maximum flexibility for the user. An I^2C host interface is provided to allow enhanced configurations in addition to power-on default settings programmed by pin-strapping resistors.

The TFP410 offers monitor detection through receiver detection, or hot-plug detection when I^2C is enabled. The monitor detection feature allows the user enhanced flexibility when attaching to digital displays or receivers (see 节 *6.4.3* and the see 节 *6.6*).

The TFP410 has a data de-skew feature allowing the users to *de-skew* the input data with respect to the IDCK± (see 节 *6.4.2*).

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6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 T.M.D.S. Pixel Data and Control Signal Encoding

For transition minimized differential signaling (T.M.D.S.), only one of two possible T.M.D.S. characters for a given pixel is transmitted at a given time. The transmitter keeps a running count of the number of ones and zeros previously sent and transmits the character that minimizes the number of transitions and approximates a dc balance of the transmission line. Three T.M.D.S. channels are used to transmit RGB pixel data during the active video interval (DE = High). These same three channels are also used to transmit HSYNC, VSYNC, and three control signals, CTL[3:1], during the inactive display or blanking interval (DE = Low). The following table maps the transmitted output data to the appropriate T.M.D.S. output channel in a DVI-compliant system.

INPUT PINS (VALID FOR DE = High)	T.M.D.S. OUTPUT CHANNEL	TRANSMITTED PIXEL DATA ACTIVE DISPLAY (DE = High)
DATA[23:16]	Channel 2 (TX2 ±)	Red[7:0]
DATA[15:8]	Channel 1 (TX1 ±)	Green[7:0]
DATA[7:0]	Channel 0 (TX0 ±)	Blue[7:0]
INPUT PINS (VALID FOR DE = Low)	**T.M.D.S. OUTPUT CHANNEL**	**TRANSMITTED CONTROL DATA BLANKING INTERVAL (DE = Low)**
CTL2(1)	Channel 2 (TX2 ±)	CTL[2]
CTL1 (1)	Channel 1 (TX1 ±)	CTL[1]
HSYNC, VSYNC	Channel 0 (TX0 ±)	HSYNC, VSYNC

(1) The TFP410 encodes and transfers the CTL[2:1] inputs during the vertical blanking interval. CTL3 is reserved for HDCP and is always encoded as 0. The CTL[2:1] inputs are reserved for future use. When DE = high, CTL and SYNC pins must be held constant.

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6.3.2 Universal Graphics Controller Interface Voltage Signal Levels

The universal graphics controller interface can operate in the following two distinct voltage modes:

- The high-swing mode where standard 3.3V CMOS signaling levels are used.
- The low-swing mode where adjustable 1.1V to 1.8V signaling levels are used.

To select the high-swing mode, the V_{REF} input pin must be tied to the 3.3V power supply.

To select the low-swing mode, the V_{REF} must be 0.55 to 0.95V.

In the low-swing mode, V_{REF} is used to set the midpoint of the adjustable signaling levels. The allowable range of values for V_{REF} is from 0.55V to 0.9V. The typical approach is to provide this from off chip by using a simple voltage-divider circuit. The minimum allowable input signal swing in the low-swing mode is V_{REF} ±0.2V. In low-swing mode, the V_{REF} input is common to all differential input receivers.

6.3.3 Universal Graphics Controller Interface Clock Inputs

The universal graphics controller interface of the TFP410 supports both fully differential and single-ended clock input modes. In the differential clock input mode, the universal graphics controller interface uses the crossover point between the IDCK+ and IDCK− signals as the timing reference for latching incoming data (DATA[23:0], DE, HSYNC, and VSYNC). Differential clock inputs provide greater common-mode noise rejection. The differential clock input mode is only available in the low-swing mode. In the single-ended clock input mode, the IDCK+ input (Pin 57) should be connected to the single-ended clock source and the IDCK− input (Pin 56) should be tied to GND.

The universal graphics controller interface of the TFP410 provides selectable 12-bit dual-edge, and 24-bit single-edge, input clocking modes. In the 12-bit dual-edge, the 12-bit data is latched on each edge of the input clock. In the 24-bit single-edge mode, the 24-bit data is latched on the rising edge of the input clock when EDGE = 1 and the falling edge of the input clock when EDGE = 0.

DKEN and DK[3:1] allow the user to compensate the skew between IDCK± and the pixel data and control signals. See 表 6-10 for details.

6.4 Device Functional Modes

6.4.1 Universal Graphics Controller Interface Modes

表 6-1 is a tabular representation of the different modes for the universal graphics controller interface. The 12-bit mode is selected when BSEL=0 and the 24-bit mode when BSEL=1. The 12-bit mode uses dual-edge clocking and the 24-bit mode uses single-edge clocking. The EDGE input is used to control the latching edge in 24-bit mode, or the primary latching edge in 12-bit mode. When EDGE=1, the data input is latched on the rising edge of the input clock; and when EDGE=0, the data input is latched on the falling edge of the input clock. A fully differential input clock is available only in the low-swing mode. Single-ended clocking is not recommended in the low-swing mode as this decreases common-mode noise rejection.

Note that BSEL, DSEL, and EDGE are determined by register CTL_1_MODE when I^2C is enabled (ISEL=1) and by input pins when I^2C is disabled (ISEL=0).

表 6-1. Universal Graphics Controller Interface Options (Tabular Representation)

V_{REF}	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK EDGE	CLOCK MODE
0.55V – 0.9V	0	0	0	12-bit	Dual-edge	Falling	Differential(1) (2)
0.55V – 0.9V	0	0	1	12-bit	Dual-edge	Falling	Single-ended
0.55V – 0.9V	0	1	0	12-bit	Dual-edge	Rising	Differential(1) (2)
0.55V – 0.9V	0	1	1	12-bit	Dual-edge	Rising	Single-ended
0.55V – 0.9V	1	0	0	24-bit	Single-edge	Falling	Single-ended
0.55V – 0.9V	1	0	1	24-bit	Single-edge	Falling	Differential(1) (3)
0.55V – 0.9V	1	1	0	24-bit	Single-edge	Rising	Single-ended
0.55V – 0.9V	1	1	1	24-bit	Single-edge	Rising	Differential(1) (3)

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表 6-1. Universal Graphics Controller Interface Options (Tabular Representation)（续）

V_{REF}	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK EDGE	CLOCK MODE
DV_{DD}	0	0	X	12-bit	Dual-edge	Falling	Single-ended(4)
DV_{DD}	0	1	X	12-bit	Dual-edge	Rising	Single-ended(4)
DV_{DD}	1	0	X	24-bit	Single-edge	Falling	Single-ended(4)
DV_{DD}	1	1	X	24-bit	Single-edge	Rising	Single-ended(4)

(1) The differential clock input mode is only available in the low signal swing mode (that is, $V_{REF} \leqslant 0.9V$).
(2) The TFP410 does not support a 12-bit dual-clock, single-edge input clocking mode.
(3) The TFP410 does not support a 24-bit single-clock, dual-edge input clocking mode.
(4) In the high-swing mode ($V_{REF} = DV_{DD}$), DSEL is a don’t care; therefore, the device is always in the single-ended latch mode.

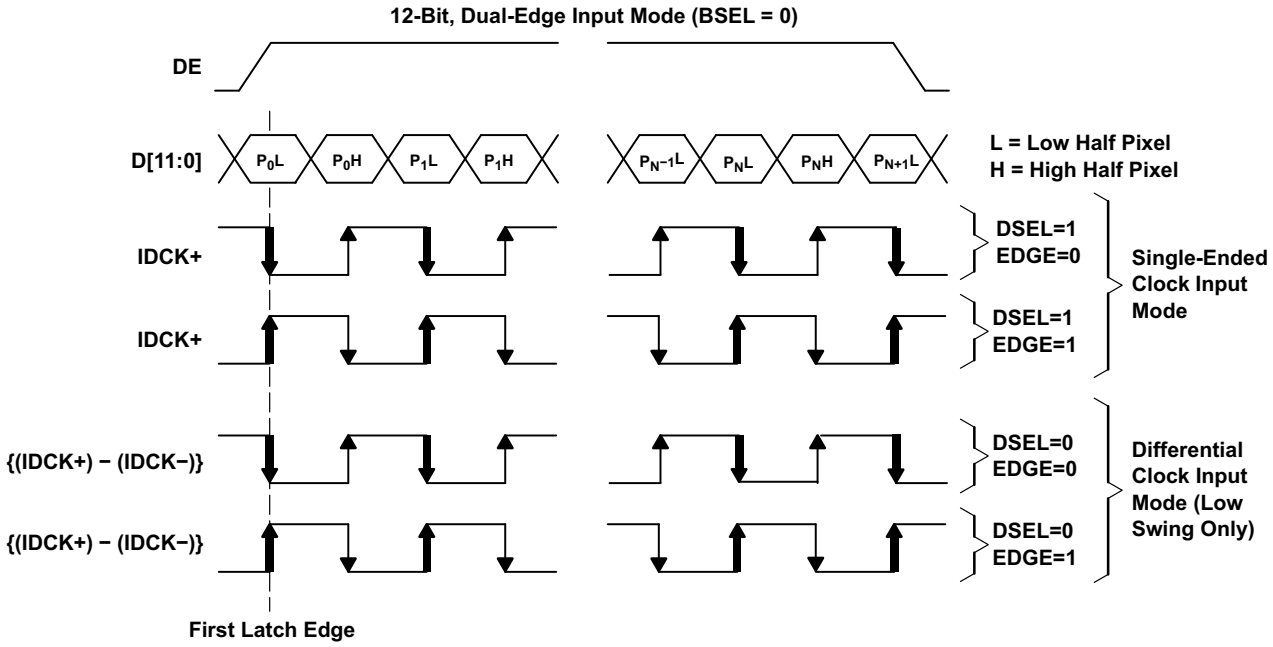


图 6-1. Universal Graphics Controller Interface Options for 12-Bit Mode (Graphical Representation)

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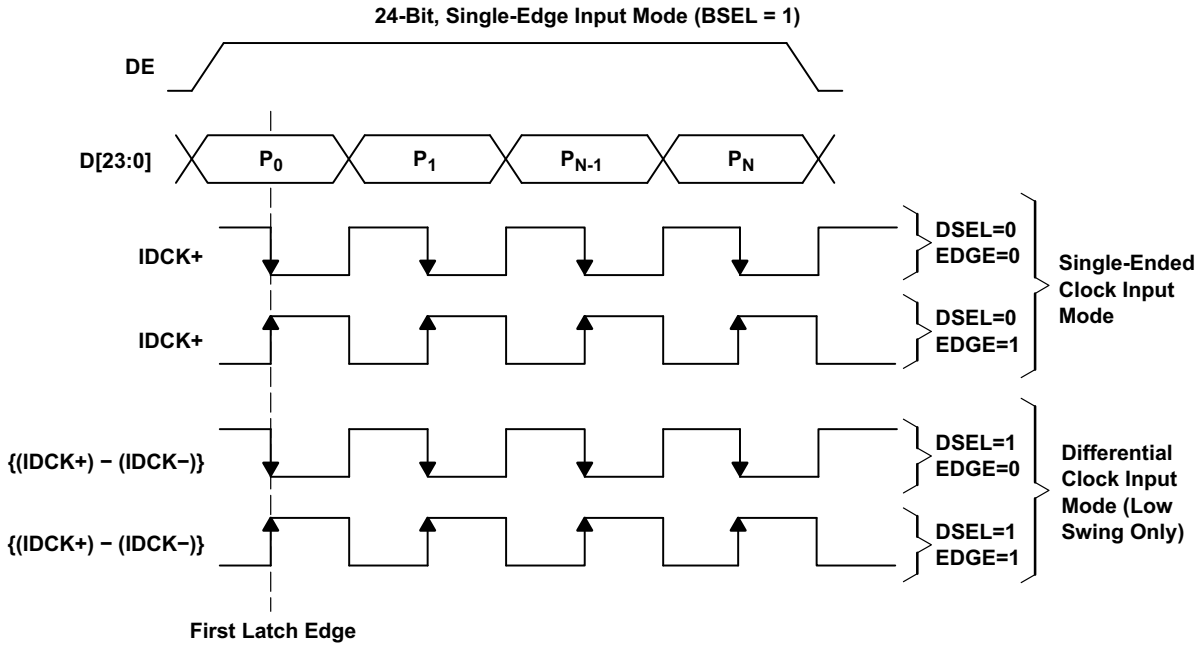


图 6-2. Universal Graphics Controller Interface Options for 24-Bit Mode (Graphical Representation)

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表 6-2. 12-Bit Mode Data Mapping

PIN NAME	P0		P1		P2	
	P0L	P0H	P1L	P1H	P2L	P2H
	LOW	HIGH	LOW	HIGH	LOW	HIGH
D11	G0[3]	R0[7]	G1[3]	R1[7]	G2[3]	R2[7]
D10	G0[2]	R0[6]	G1[2]	R1[6]	G2[2]	R2[6]
D9	G0[1]	R0[5]	G1[1]	R1[5]	G2[1]	R2[5]
D8	G0[0]	R0[4]	G1[0]	R1[4]	G2[0]	R2[4]
D7	B0[7]	R0[3]	B1[7]	R1[3]	B2[7]	R2[3]
D6	B0[6]	R0[2]	B1[6]	R1[2]	B2[6]	R2[2]
D5	B0[5]	R0[1]	B1[5]	R1[1]	B2[5]	R2[1]
D4	B0[4]	R0[0]	B1[4]	R1[0]	B2[4]	R2[0]
D3	B0[3]	G0[7]	B1[3]	G1[7]	B2[3]	G2[7]
D2	B0[2]	G0[6]	B1[2]	G1[6]	B2[2]	G2[6]
D1	B0[1]	G0[5]	B1[1]	G1[5]	B2[1]	G2[5]
D0	B0[0]	G0[4]	B1[0]	G1[4]	B2[0]	G2[4]

表 6-3. 24-Bit Mode Data Mapping

PIN NAME	P0	P1	P2	PIN NAME	P0	P1	P2
D23	R0[7]	R1[7]	R2[7]	D11	G0[3]	G1[3]	G2[3]
D22	R0[6]	R1[6]	R2[6]	D10	G0[2]	G1[2]	G2[2]
D21	R0[5]	R1[5]	R2[5]	D9	G0[1]	G1[1]	G2[1]
D20	R0[4]	R1[4]	R2[4]	D8	G0[0]	G1[0]	G2[0]
D19	R0[3]	R1[3]	R2[3]	D7	B0[7]	B1[7]	B2[7]
D18	R0[2]	R1[2]	R2[2]	D6	B0[6]	B1[6]	B2[6]
D17	R0[1]	R1[1]	R2[1]	D5	B0[5]	B1[5]	B2[5]
D16	R0[0]	R1[0]	R2[0]	D4	B0[4]	B1[4]	B2[4]
D15	G0[7]	G1[7]	G2[7]	D3	B0[3]	B1[3]	B2[3]
D14	G0[6]	G1[6]	G2[6]	D2	B0[2]	B1[2]	B2[2]
D13	G0[5]	G1[5]	G2[5]	D1	B0[1]	B1[1]	B2[1]
D12	G0[4]	G1[4]	G2[4]	D0	B0[0]	B1[0]	B2[0]

6.4.2 Data De-skew Feature

The de-skew feature allows adjustment of the input setup/hold time. Specifically, the input data DATA[23:0] can be latched slightly before or after the latching edge of the clock IDCK± depending on the amount of de-skew desired. When de-skew enable (DKEN) is enabled, the amount of de-skew is programmable by setting the three bits DK[3:1]. When disabled, a default de-skew setting is used. To allow maximum flexibility and ease of use, DKEN and DK[3:1] are accessed directly through configuration pins when I^2C is disabled, or through registers of the same name when I^2C is enabled. When using I^2C mode, the DKEN pin should be tied to ground to avoid a floating input.

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The input setup/hold time can be varied with respect to the input clock by an amount $t_{(CD)}$ given by the formula in 方程式 1.

$$t_{(CD)} = (DK[3:1] - 4) \times t_{(STEP)} \quad (1)$$

where

- $t_{(STEP)}$ is the adjustment increment amount
- DK[3:1] is a number from 0 to 7 represented as a 3-bit binary number
- $t_{(CD)}$ is the cumulative de-skew amount

(DK[3:1]-4) is simply a multiplier in the range {-4,-3,-2,-1, 0, 1, 2, 3} for $t_{(STEP)}$. Therefore, data can be latched in increments from 4 times the value of $t_{(STEP)}$ before the latching edge of the clock to 3 times the value of $t_{(STEP)}$ after the latching edge. Note that the input clock is not changed, only the time when data is latched with respect to the clock.

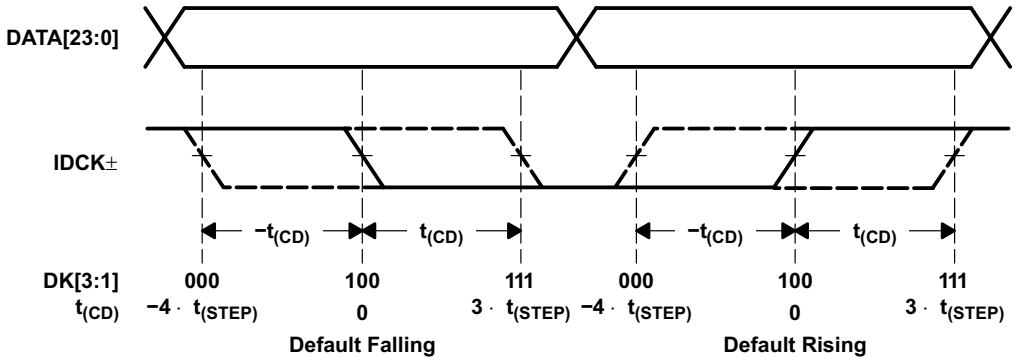


图 6-3. A Graphical Representation of the De-Skew Function

6.4.3 Hot Plug/Unplug (Auto Connect/Disconnect Detection)

TFP410 supports hot plug/unplug (auto connect/disconnect detection) for the DVI link. The receiver sense input (RSEN) bit indicates if a DVI receiver is connected to TXC+ and TXC－. The HTPLG bit reflects the current state of the HTPLG pin connected to the monitor via the DVI connector. When I^2C is disabled (ISEL=0), the RSEN value is available on the MSEN pin. When I2C is enabled, the connection status of the DVI link and HTPLG sense pins are provided by the CTL_2_MODE register. The MSEL bits of the CTL_2_MODE register can be used to program the MSEN to output the HTPLG value, the RSEN value, an interrupt, or be disabled.

The source of the interrupt event is selected by TSEL in the CTL_2_MODE register. An interrupt is generated by a change in status of the selected signal. The interrupt status is indicated in the MDI bit of CTL_2_MODE and can be output via the MSEN pin. The interrupt continues to be asserted until a 1 is written to the MDI bit, resetting the bit back to 0. Writing 0 to the MDI bit has no effect.

6.4.4 Device Configuration and I^2C RESET Description

The TFP410 device configuration can be programmed by several different methods to allow maximum flexibility for the user’s application. Device configuration is controlled depending on the state of the ISEL/ $\overline{RST}$ pin, configuration pins (BSEL, DSEL, EDGE, V_{REF}) and state pins ($\overline{PD}$, DKEN). I^2C bus select and I^2C RESET (active low) are shared functions on the ISEL/ $\overline{RST}$ pin, which operates asynchronously.

Holding ISEL/ $\overline{RST}$ low causes the device configuration to be set by the configuration pins (BSEL, DSEL, EDGE, and V_{REF}) and state pins ($\overline{PD}$, DKEN). The I^2C bus is disabled.

Holding ISEL/ $\overline{RST}$ high causes the chip configuration to be set based on the configuration bits (BSEL, DSEL, EDGE) and state bits ($\overline{PD}$, DKEN) in the I^2C registers. The I^2C bus is enabled.

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Momentarily bringing ISEL/ $\overline{\text{RST}}$ low and then back high while the device is operating in normal or power-down mode will RESET the I^2C registers to their default values. The device configuration will be changed to the default power-up state with I^2C enabled. After power up, the device must be reset. It is suggested that this pin be tied to the system reset signal, which is low during power up and is then asserted high after all the power supplies are fully functional.

6.4.5 DE Generator

The TFP410 contains a DE generator that can be used to generate an internal DE signal when the original data source does not provide one. There are several I^2C programmable values that control the DE generator (see 图 6-4). DE_GEN in the DE_CTL register enables this function. When enabled, the DE pin is ignored.

DE_TOP and DE_LIN are line counts used to control the number of lines after VSYNC goes active that DE is enabled, and the total number of lines that DE remains active, respectively. The polarity of VSYNC must be set by VS_POL in the DE_CTL register.

DE_DLY and DE_CNT are pixel counts used to control the number of pixels after HSYNC goes active that DE is enabled, and the total number of pixels that DE remains active, respectively. The polarity of HSYNC must be set by HS_POL in the DE_CTL register.

The TFP410 also counts the total number of HSYNC pulses between VSYNC pulses, and the total number of pixels between HSYNC pulses. These values, the total vertical and horizontal resolutions, are available in V_RES and H_RES, respectively. These values are available at all times, whether or not the DE generator is enabled.

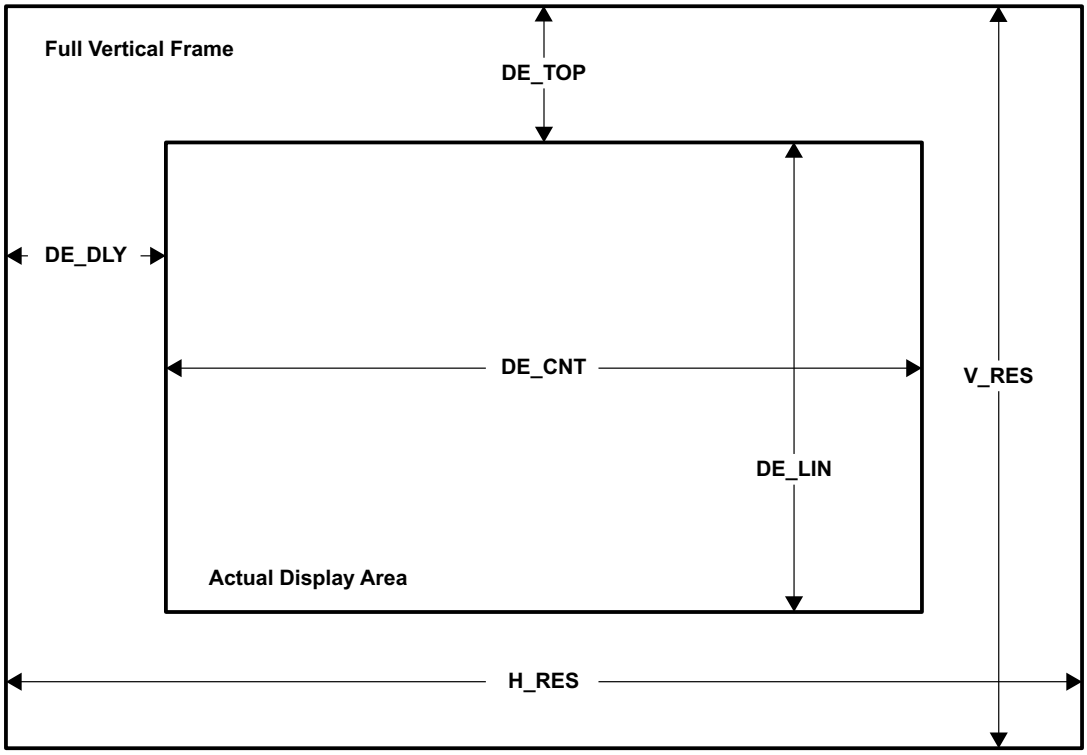


图 6-4. DE Generator Register Functions

6.5 Programming

6.5.1 I²C Interface

The I²C interface is used to access the internal TFP410 registers. This two-pin interface consists of the SCL clock line and the SDA serial data line. The basic I²C access cycles are shown in 图 6-5 and 图 6-6.

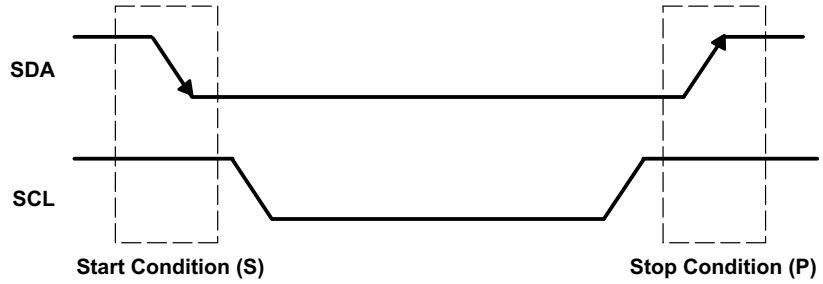


图 6-5. I²C Start and Stop Conditions

The basic access write cycle consists of the following:

1. A start condition
2. A target address cycle
3. A sub-address cycle
4. Any number of data cycles
5. A stop condition

The basic access read cycle consists of the following:

1. A start condition
2. A target write address cycle
3. A sub-address cycle
4. A restart condition
5. A target read address cycle
6. Any number of data cycles
7. A stop condition

The start and stop conditions are shown in 图 6-5. The high to low transition of SDA while SCL is high defines the start condition. The low to high transition of SDA while SCL is high defines the stop condition. Each cycle, data or address, consists of 8 bits of serial data followed by one acknowledge bit generated by the receiving device. Thus, each data/address cycle contains 9 bits as shown in 图 6-6.

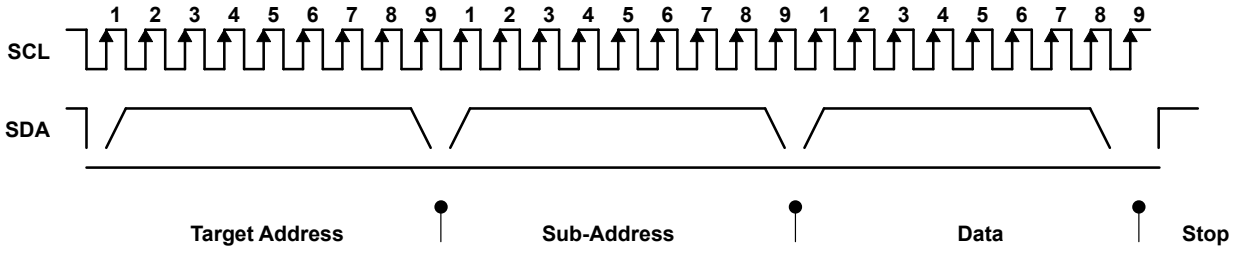


图 6-6. I²C Access Cycles

Following a start condition, each I²C device decodes the target address. The TFP410 responds with an acknowledge by pulling the SDA line low during the ninth clock cycle if it decodes the address as its address. During subsequent sub-address and data cycles, the TFP410 responds with acknowledge as shown in 图 6-7. The sub-address is auto-incremented after each data cycle.

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The transmitting device must not drive the SDA signal during the acknowledge cycle so that the receiving device may drive the SDA signal low. The controller indicates a not acknowledge condition ($\overline{A}$) by keeping the SDA signal high just before it asserts the stop condition (P). This sequence terminates a read cycle as shown in 图 6-8.

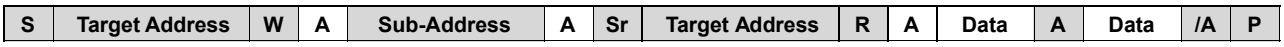
The target address consists of 7 bits of address along with 1 bit of read/write information (read = 1, write = 0) as shown below in 图 6-6 and 图 6-7. For the TFP410, the selectable target addresses (including the R/W bit) using A[3:1] are 0x70, 0x72, 0x74, 0x76, 0x78, 0x7A, 0x7C, and 0x7E for write cycles and 0x71, 0x73, 0x75, 0x77, 0x79, 0x7B, 0x7D, and 0x7F for read cycles.



Where:



图 6-7. I²C Write Cycle



Where:

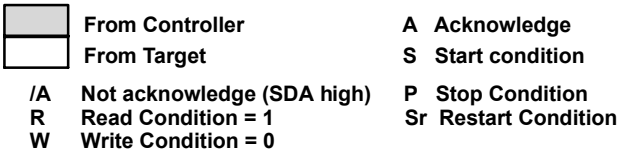


图 6-8. I²C Read Cycle

6.6 Register Maps

The TFP410 is a standard I²C target device. All the registers can be written and read through the I²C interface (unless otherwise specified). The TFP410 target machine supports only byte read and write cycles. Page mode is not supported. The 8-bit binary address of the I²C machine is 0111 A3A2A1X, where A[3:1] are pin programmable or set to 000 by default. The I²C base address of the TFP410 is dependent on A[3:1] (pins 6, 7 and 8 respectively) as shown below.

A[3:1]	WRITE ADDRESS (Hex)	READ ADDRESS (Hex)
000	70	71
001	72	73
010	74	75
011	76	77
100	78	79
101	7A	7B
110	7C	7D
111	7E	7F

REGISTER	RW	SUB-ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VEN_ID	R	00	VEN_ID[7:0]							
	R	01	VEN_ID[15:8]							

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REGISTER	RW	SUB-ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DEV_ID	R	02	DEV_ID[7:0]							
	R	03	DEV_ID[15:8]							
REV_ID	R	04	REV_ID[7:0]							
RESERVED	R	05-07	Reserved							
CTL_1_MODE	RW	08	RSVD	TDIS	VEN	HEN	DSEL	BSEL	EDGE	PD
CTL_2_MODE	RW	09	VLOW	MSEL			TSEL	RSEN	HTPLG	MDI
CTL_3_MODE	RW	0A	DK			DKEN	CTL			RSVD
CFG	R	0B	CFG							
RESERVED	RW	0C-31	Reserved							
DE_DLY	RW	32	DE_DLY[7:0]							
DE_CTL	RW	33	RSVD	DE_GEN	VS_POL	HS_POL	RSVD			DE_DLY[8]
DE_TOP	RW	34	RSVD	DE_DLY[6:0]						
RESERVED	RW	35	Reserved							
DE_CNT	RW	36	DE_CNT[7:0]							
	RW	37	Reserved					DE_CNT[10:8]		
DE_LIN	RW	38	DE_LIN[7:0]							
	RW	39	Reserved					DE_LIN[10:8]		
H_RES	R	3A	H_RES[7:0]							
	R	3B	Reserved					H_RES[10:8]		
V_RES	R	3C	V_RES[7:0]							
	R	3D	Reserved					V_RES[10:8]		
RESERVED	R	3E–FF								

6.6.1 VEN_ID Register (Sub-Address = 01–00) [reset = 0x014C]

图 6-9. VEN_ID Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VEN_ID[15:8]								VEN_ID[7:0]							

表 6-4. VEN_ID Field Descriptions

Bit	Field	Type	Description
15:8	VEN_ID	R	These read-only registers contain the 16-bit Texas Instruments vendor ID. VEN_ID is hardwired to 0x014C.
7:0	VEN_ID	R	

6.6.2 DEV_ID Register (Sub-Address = 03 – 02) [reset = 0x0410]

图 6-10. DEV_ID Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV_ID[15:8]								DEV_ID[7:0]							

表 6-5. DEV_ID Register Field Descriptions

Bit	Field	Type	Description
15:8	DEV_ID	R	These read-only registers contain the 16-bit device ID for the TFP410. DEV_ID is hardwired to 0x0410.
7:0	DEV_ID	R	

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6.6.3 REV_ID Register (Sub-Address = 04) [reset = 0x00]

图 6-11. REV_ID Register

7	6	5	4	3	2	1	0
REV_ID[7:0]							

表 6-6. REV_ID Register Field Descriptions

Bit	Field	Type	Description
7:0	REV_ID	R	This read-only register contains the revision ID.

6.6.4 Reserved Register (Sub-Address = 07 – 05) [reset = 0x641400]

图 6-12. Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED[15:8]								RESERVED[7:0]							

表 6-7. Reserved Field Descriptions

Bit	Field	Type	Description
15:8	RESERVED	Read Only	—
7:0	RESERVED	Read Only	—

6.6.5 CTL_1_MODE (Sub-Address = 08) [reset = 0xBE]

图 6-13. CTL_1_MODE Register

7	6	5	4	3	2	1	0
RSVD	TDIS	VEN	HEN	DSEL	BSEL	EDGE	$\overline{PD}$

表 6-8. CTL_1_MODE Field Descriptions

Bit	Field	Type	Description
7	RSVD	R/W	Reserved
6	TDIS	R/W	This read/write register contains the T.M.D.S. disable mode 0: T.M.D.S. circuitry enable state is determined by PD. 1: T.M.D.S. circuitry is disabled.
5	VEN	R/W	This read/write register contains the vertical sync enable mode. 0: VSYNC input is transmitted as a fixed low 1: VSYNC input is transmitted in its original state
4	HEN	R/W	This read/write register contains the horizontal sync enable mode. 0: HSYNC input is transmitted as a fixed low 1: HSYNC input is transmitted in its original state
3	DSEL	R/W	This read/write register is used in combination with BSEL and VREF to select the single-ended or differential input clock mode. In the high-swing mode, DSEL is a don’t care because IDCK is always single-ended.
2	BSEL	R/W	This read/write register contains the input bus select mode. 0: 12-bit operation with dual-edge clock 1: 24-bit operation with single-edge clock
1	EDGE	R/W	This read/write register contains the edge select mode. 0: Input data latches to the falling edge of IDCK+ 1: Input data latches to the rising edge of IDCK+
0	$\overline{PD}$	R/W	This read/write register contains the power-down mode. 0: Power down (default after RESET) 1: Normal operation

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6.6.6 CTL_2_MODE Register (Sub-Address = 09) [reset = 0x00]

图 6-14. CTL_2_MODE Register

7	6	5	4	3	2	1	0
VLOW	MSEL[3:1]			TSEL	RSEN	HTPLG	MDI

表 6-9. CTL_2_MODE Field Descriptions

Bit	Field	Type	Description
7	VLOW	R/W	This read only register indicates the VREF input level. 0: This bit is a logic level (0) if the VREF analog input selects high-swing inputs 1: This bit is a logic level (1) if the VREF analog input selects low-swing inputs
6:4	MSEL[3:1]	R/W	This read/write register contains the source select of the monitor sense output pin. 000: Disabled. MSEN output high 001: Outputs the MDI bit (interrupt) 010: Outputs the RSEN bit (receiver detect) 011: Outputs the HTPLG bit (hot plug detect)
3	TSEL	R/W	This read/write register contains the interrupt generation source select. 0: Interrupt bit (MDI) is generated by monitoring RSEN 1: Interrupt bit (MDI) is generated by monitoring HTPLG
2	RSEN	R/W	This read only register contains the receiver sense input logic state, which is valid only for dc-coupled systems. 0: A powered-on receiver is not detected 1: A powered-on receiver is detected (that is, connected to the DVI transmitter outputs)
1	HTPLG	R/W	This read only register contains the hot plug detection input logic state. 0: Logic level detected on the EDGE/HTPLG pin (pin 9) 1: High level detected on the EDGE/HTPLG pin (pin 9)
0	MDI	R/W	This read/write register contains the monitor detect interrupt mode. 0: Detected logic level change in detection signal (to clear, write one to this bit) 1: Logic level remains the same

6.6.7 CTL_3_MODE Register (Sub-Address = 0A) [reset = 0x80]

图 6-15. CTL_3_MODE Register

7	6	5	4	3	2	1	0
DK[3:1]			DKEN	RSVD	CTL[2:1]		RSVD

表 6-10. CTL_3_MODE Register Field Descriptions

Bit	Field	Type	Description
7:5	DK[3:1]	RW	This read/write register contains the de-skew setting, each increment adjusts the skew by t(STEP). 000: Step 1 (minimum setup/maximum hold) 001: Step 2 010: Step 3 011: Step 4 100: Step 5 (default) 101: Step 6 110: Step 7 111: Step 8 (maximum setup/minimum hold)
4	DKEN	RW	This read/write register controls the data de-skew enable. 0: Data de-skew is disabled, the values in DK[3:1] are not used 1: Data de-skew is enabled, the de-skew setting is controlled through DK[3:1]
3	RSVD	RW	—
2:1	CTL[2:1]	RW	This read/write register contains the values of the two CTL[2:1] bits that are output on the DVI port during the blanking interval.
0	RSVD	RW	—

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6.6.8 CFG Register (Sub-Address = 0B)

图 6-16. CFG Register

7	6	5	4	3	2	1	0
CFG[7:0]							

表 6-11. CFG Register Field Descriptions

Bit	Field	Type	Description
7:0 (D[23:16])	CFG	Read Only	This read-only register contains the state of the inputs D[23:16]. These pins can be used to provide the user with selectable configuration data through the I^2C bus.

6.6.9 RESERVED Register (Sub-Address = 0E – 0C) [reset = 0x97D0A9]

图 6-17. RESERVED Register

7	6	5	4	3	2	1	0
RESERVED							

表 6-12. RESERVED Register Field Descriptions

Bit	Field	Type	Description
7:0	RESERVED	R/W	—

6.6.10 DE_DLY Register (Sub-Address = 32) [reset = 0x00]

图 6-18. DE_DLY Register

7	6	5	4	3	2	1	0
DE_DLY[7:0]							

表 6-13. DE_DLY Field Descriptions

Bit	Field	Type	Description
7:0	DE_DLY	R/W	This read/write register defines the number of pixels after HSYNC goes active that DE is generated, when the DE generator is enabled. The value must be less than or equal to (2047 - DE_CNT)

6.6.11 DE_CTL Register (Sub-Address = 33) [reset = 0x00]

图 6-19. DE_CTL Register

7	6	5	4	3	2	1	0
Reserved	DE_GEN	VS_POL	HS_POL	Reserved			DE_DLY[8]

表 6-14. DE_CTL Register Field Descriptions

Bit	Field	Type	Description
7	Reserved	R/W	—
6	DE_GEN	R/W	This read/write register enables the internal DE generator. 0: DE generator is disabled. Signal required on DE pin 1: DE generator is enabled. DE pin is ignored.
5	VS_POL	R/W	This read/write register sets the VSYNC polarity. 0: VSYNC is considered active low. 1: VSYNC is considered active high. Line counts are reset on the VSYNC active edge.
4	HS_POL	R/W	This read/write register sets the HSYNC polarity. 0: HSYNC is considered active low. 1: HSYNC is considered active high. Pixel counts are reset on the HSYNC active edge.
1:3	Reserved	R/W	—
0	DE_DLY[8]	R/W	This read/write register contains the top bit of DE_DLY.

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6.6.12 DE_TOP Register (Sub-Address = 34) [reset = 0x00]

图 6-20. DE_TOP Register

7	6	5	4	3	2	1	0
DE_TOP[7:0]							

表 6-15. DE_TOP Register Field Descriptions

Bit	Field	Type	Description
7:0	DE_TOP	R/W	This read/write register defines the number of pixels after VSYNC goes active that DE is generated, when the DE generator is enabled.

6.6.13 DE_CNT Register (Sub-Address = 37 – 36) [reset = 0x0000]

图 6-21. DE_CNT Register

7	6	5	4	3	2	1	0
DE_CNT[7:0]							
Reserved						DE_CNT[10:8]	

表 6-16. DE_CNT Register Field Descriptions

Bit	Field	Type	Description
10:8	DE_CNT	R/W	These read/write registers define the width of the active display, in pixels, when the DE generator is enabled. The value must be less than or equal to (2047 - DE_DLY).
7:0	DE_CNT	R/W	

6.6.14 DE_LIN Register (Sub-Address = 39 – 38) [reset = 0x0000]

图 6-22. DE_LIN Register

7	6	5	4	3	2	1	0
DE_LIN[7:0]							
Reserved						DE_LIN[10:8]	

表 6-17. DE_LIN Register Field Descriptions

Bit	Field	Type	Description
10:8	DE_LIN	R/W	These read/write registers define the height of the active display, in lines, when the DE generator is enabled.
7:0	DE_LIN	R/W	

6.6.15 H_RES Register (Sub-Address = 3B–3A)

图 6-23. H_RES Register

7	6	5	4	3	2	1	0
H_RES[7:0]							
Reserved						H_RES[10:8]	

表 6-18. H_RES Register Field Descriptions

Bit	Field	Type	Description
10:8	H_RES	Read Only	These read-only registers return the number of pixels between consecutive HSYNC pulses.
7:0	H_RES	Read Only	

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6.6.16 V_RES Register (Sub-Address = 3D−3C)

图 6-24. V_RES Register

7	6	5	4	3	2	1	0
V_RES[7:0]							
Reserved					V_RES[10:8]		

表 6-19. V_RES Register Field Descriptions

Bit	Field	Type	Description
10:8	V_RES	Read Only	These read-only registers return the number of lines between consecutive VSYNC pulses.
7:0	V_RES	Read Only	

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7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

7.1 Application Information

The TFP410 is a DVI-compliant digital transmitter that is used in digital host monitor systems to T.M.D.S. encode and serialize RGB pixel data streams. TFP410 supports resolutions from VGA to WUXGA (and 1080p). The host in a digital display system, usually a PC or consumer electronics device, contains a DVI-compatible transmitter such as the TI TFP410 that receives 24-bit pixel data along with appropriate control signals. The TFP410 encodes the signals into a high speed, low voltage, differential serial bit stream optimized for transmission over a twisted-pair cable to a display device such as the TFP401.

7.2 Typical Application

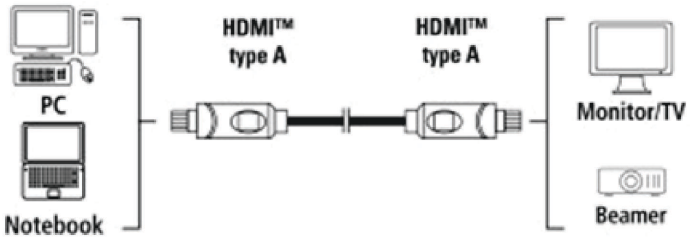


图 7-1. Typical Application for the TFP410 Device

7.2.1 Design Requirements

PARAMETER	VALUE
Power supply	3.3V dc at 1 A
Input clock	Single-ended
Input clock frequency range	25MHz — 165MHz
Output format	24 bits/pixel
Input clock latching	Rising edge
I^2C EEPROM support	No
De-skew	No

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7.2.2 Detailed Design Procedure

7.2.2.1 Data and Control Signals

The trace length of data and control signals out of the receiver should be kept as close to equal as possible. Trace separation should be approximately 5 times the height. As a general rule, traces also should be less than 2.8” if possible (longer traces can be acceptable).

Delay = 85 × SQRT × er (2)

where

- er = 4.35; relative permativity of 50% resin FR-4 at 1 GHz
- Delay = 177 pS/in

Length of rising edge = Tr(ps) / Delay; Tr = 3 ns (3)

where

- = 3000 ps / 177 ps per inch
- = 16.9 inches

Length of rising edge / 6 = Max length of trace for lumped circuit. (4)

16.9 / 6 = 2.8 inches (5)

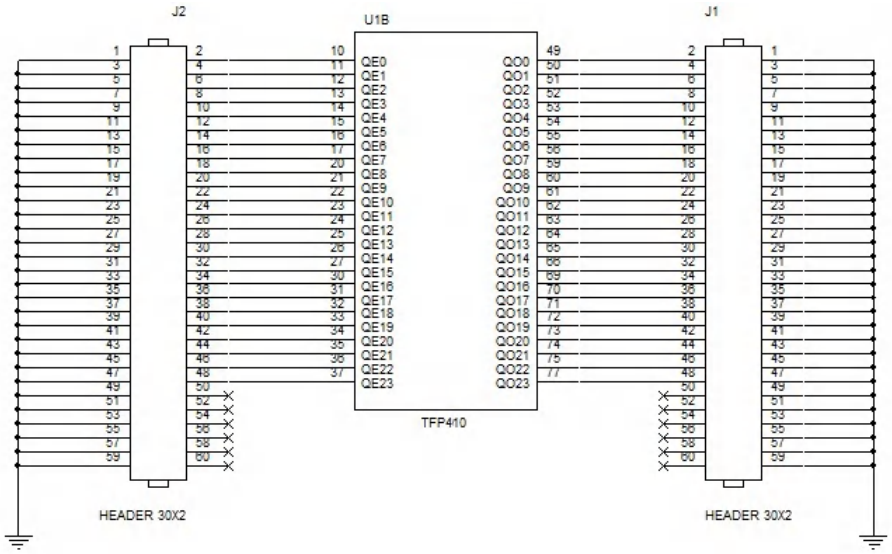


图 7-2. Data Signals

7.2.2.2 Configuration Options

The TFP410 can be configured in several modes depending on the required input format, for example 1 byte/clock, 2 bytes/clock, falling/rinsing clock edge.

Refer to 表 6-1 for more information about configuration options.

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7.2.2.3 Power Supplies Decoupling

Digital, analog, and PLL supplies must be decoupled from each other to avoid electrical noise on the PLL and the core.

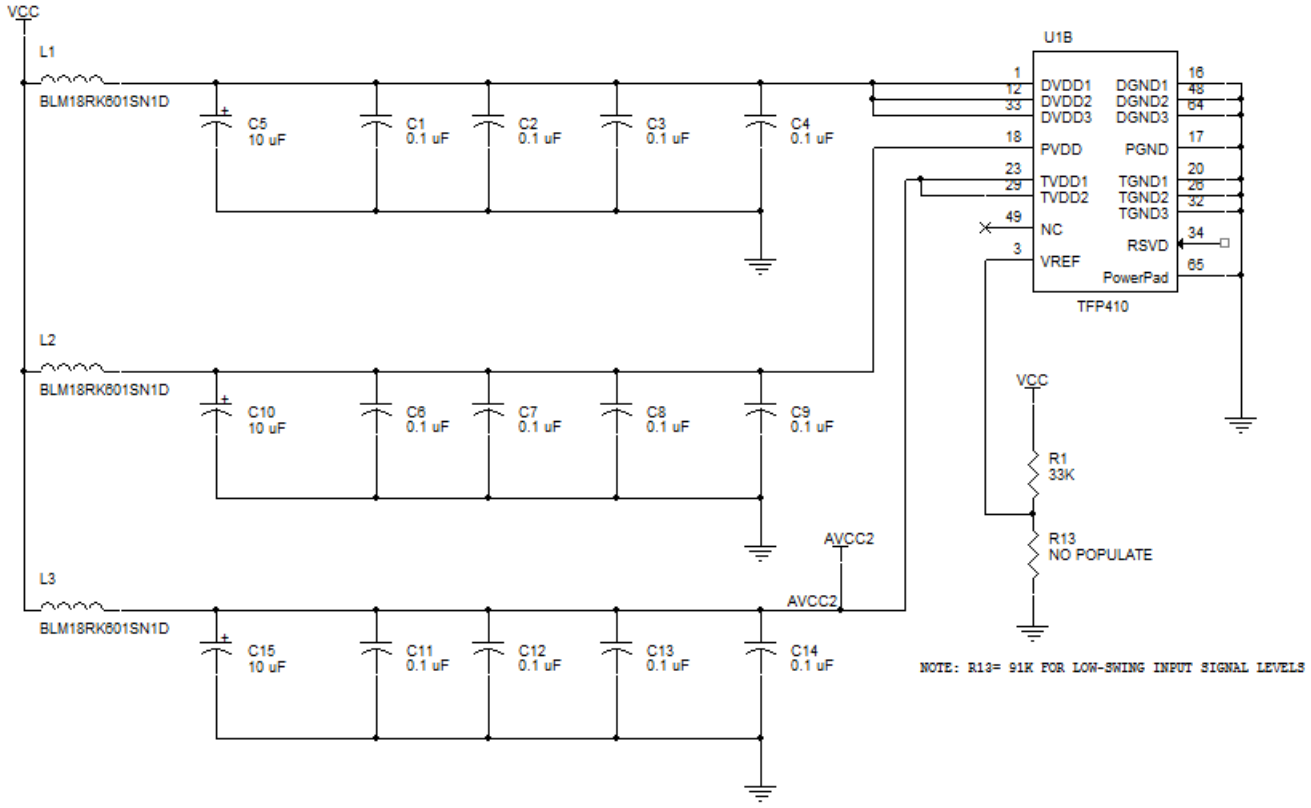


图 7-3. Power Decoupling

7.2.3 Application Curves

Sometimes the Panel does not support the same format as the GPU (graphics processor unit). In these cases the user must decide how to connect the unused bits.

图 7-4 and 图 7-5 show the mismatches between the 18-bit GPU and a 24-bit LCD where “x” and “y” represent the 2 LSB of the Panel.

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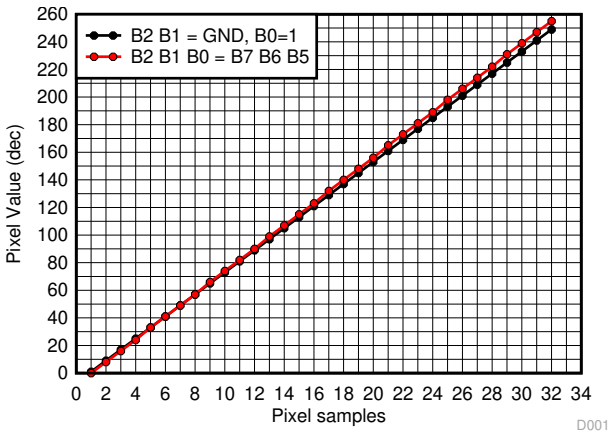


图 7-4. 16b GPU to 24b LCD

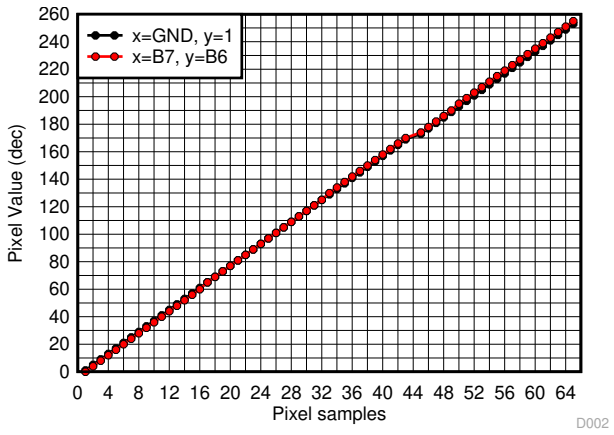


图 7-5. 18b GPU to 24b LCD

7.3 Power Supply Recommendations

Use solid ground planes. Tie ground planes together with as many vias as is practical. This will provide a desirable return path for current. Each supply should be on separate split power planes, where each power plane should be as large an area as possible. Connect PanelBus receiver power and ground pins and all bypass caps to appropriate power or ground plane with via. Vias should be as fat and short as practical, the goal is to minimize the inductance.

7.3.1 DVDD

Place one 0.01µF capacitor as close as possible between each DVDD device pins and ground. A 22µF tantalum capacitor should be placed between the supply and 0.01µF capacitors. A ferrite bead should be used between the source and the 22µF capacitor.

7.3.2 TVDD

Place one 0.01µF capacitor as close as possible between each TVDD device pins and ground. A 22µF tantalum capacitor should be placed between the supply and 0.01µF capacitors. A ferrite bead should be used between the source and the 22µF capacitor.

7.3.3 PVDD

Place three 0.01µF capacitors in parallel as close as possible between the PVDD device pin and ground. A 22µF tantalum capacitor should be placed between the supply and 0.01µF capacitors. A ferrite bead should be used between the source and the 22µF capacitor.

7.4 Layout

7.4.1 Layout Guidelines

7.4.1.1 Layer Stack

The pinout of Texas Instruments' High Speed Interface (HSI) devices features differential signal pairs and the remaining signals comprise the supply rails, VCC and ground, and lower-speed signals, such as control pins. As an example, consider a device X which is a repeater/re-driver, so both inputs and outputs are high-speed differential signals. These guidelines can be applied to other high-speed devices such as drivers, receivers, multiplexers, and so on.

A minimum of four layers is required to accomplish a low-EMI PCB design. Layer stacking should be in the following order (top-to-bottom): high-speed differential signal layer, ground plane, power plane and control signal layer.

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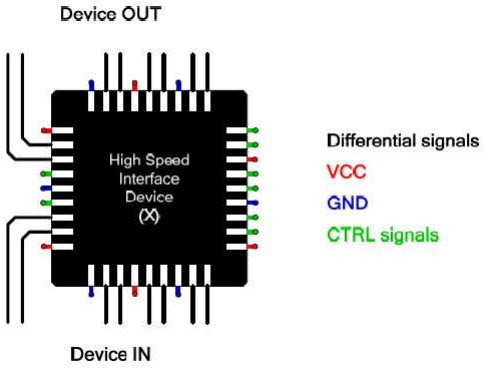


图 7-6. PCB Stack Up

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7.4.1.2 Routing High-Speed Differential Signal Traces (RxC-, RxC+, Rx0-, Rx0+, Rx1-, Rx1+, Rx2-, Rx2+)

Trace impedance should be controlled for optimal performance. Each differential pair should be equal in length and symmetrical and should have equal impedance to ground with a trace separation of 2 times to 4 times the height. A differential trace separation of 4 times the height yields about 6% cross-talk (6% effect on impedance).

We recommend that differential trace routing should be side-by-side, though it is not important that the differential traces be tightly coupled together, because tight coupling is not achievable on PCB traces. Typical ratios on PCBs are only 20% to 50%; 99.9% is the value of a well balanced twisted pair cable. Each differential trace should be as short as possible (< 2 inches is preferable) with no 90° angles. These high-speed transmission traces should be on layer 1, which is the top layer.

RxC-, RxC+, Rx0-, Rx0+, Rx1-, Rx1+, Rx2-, Rx2+ signals all route directly from the DVI connector pins to the device, no external components are needed.

7.4.1.3 DVI Connector

Clear-out holes for connector pins should leave space between pins to allow continuous ground through the pin field. Allow enough spacing in ground plane around signal pins vias however, keep enough copper between vias to allow for ground current to flow between the vias. Avoid creating a large ground plane slot around the entire connector, because minimizing the via capacitance is the goal.

7.4.2 Layout Example

DVI connector trace matching is shown in 图 7-7.

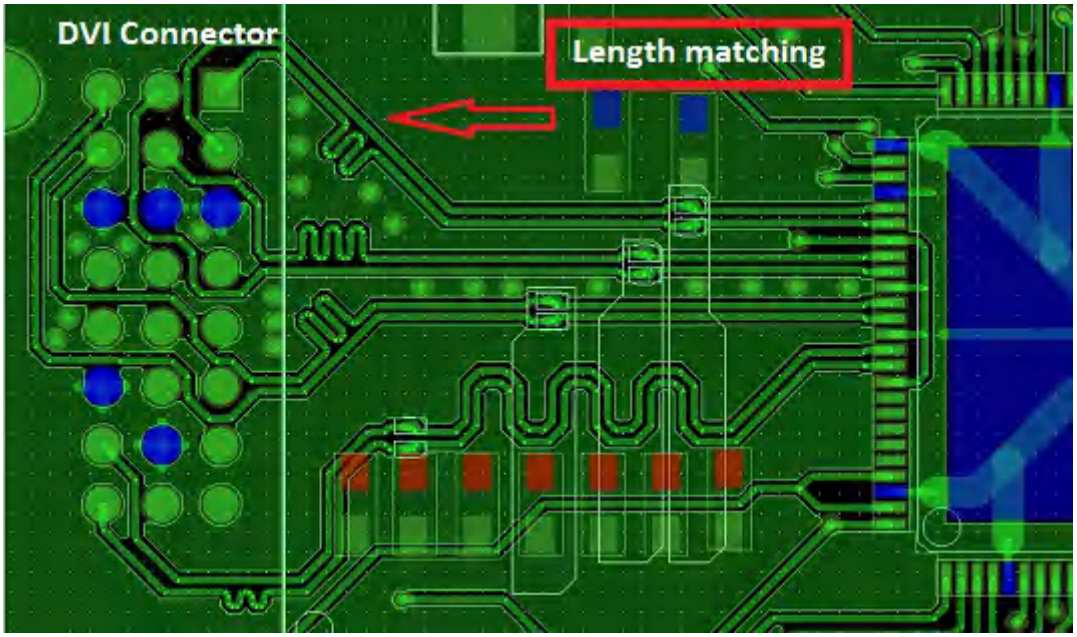


图 7-7. DVI Signal Routing

Keep the data lines as far as possible from each other as shown in 图 7-8.

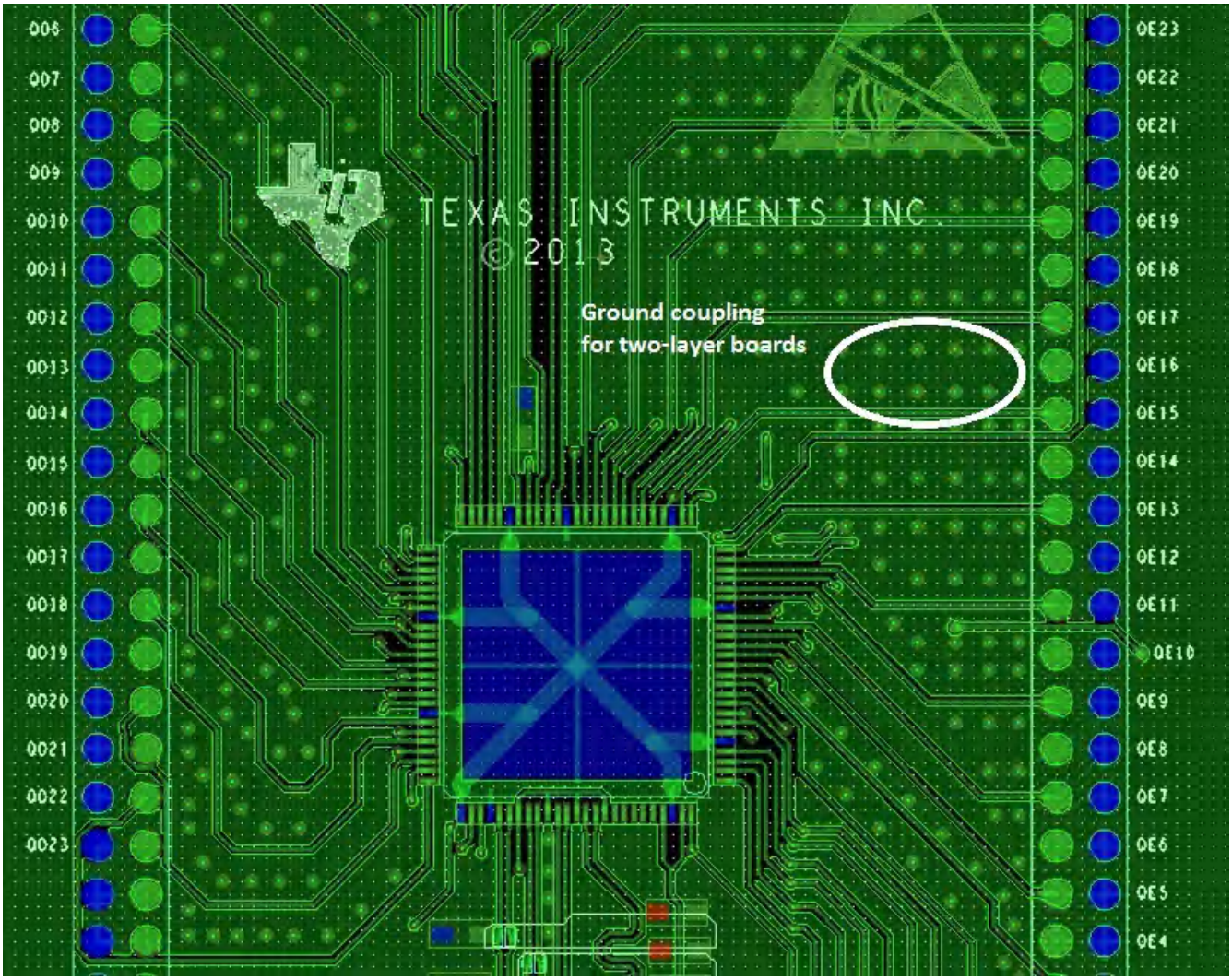


图 7-8. Data Signal Routing

Connect the thermal pad to ground as shown in 图 7-9.

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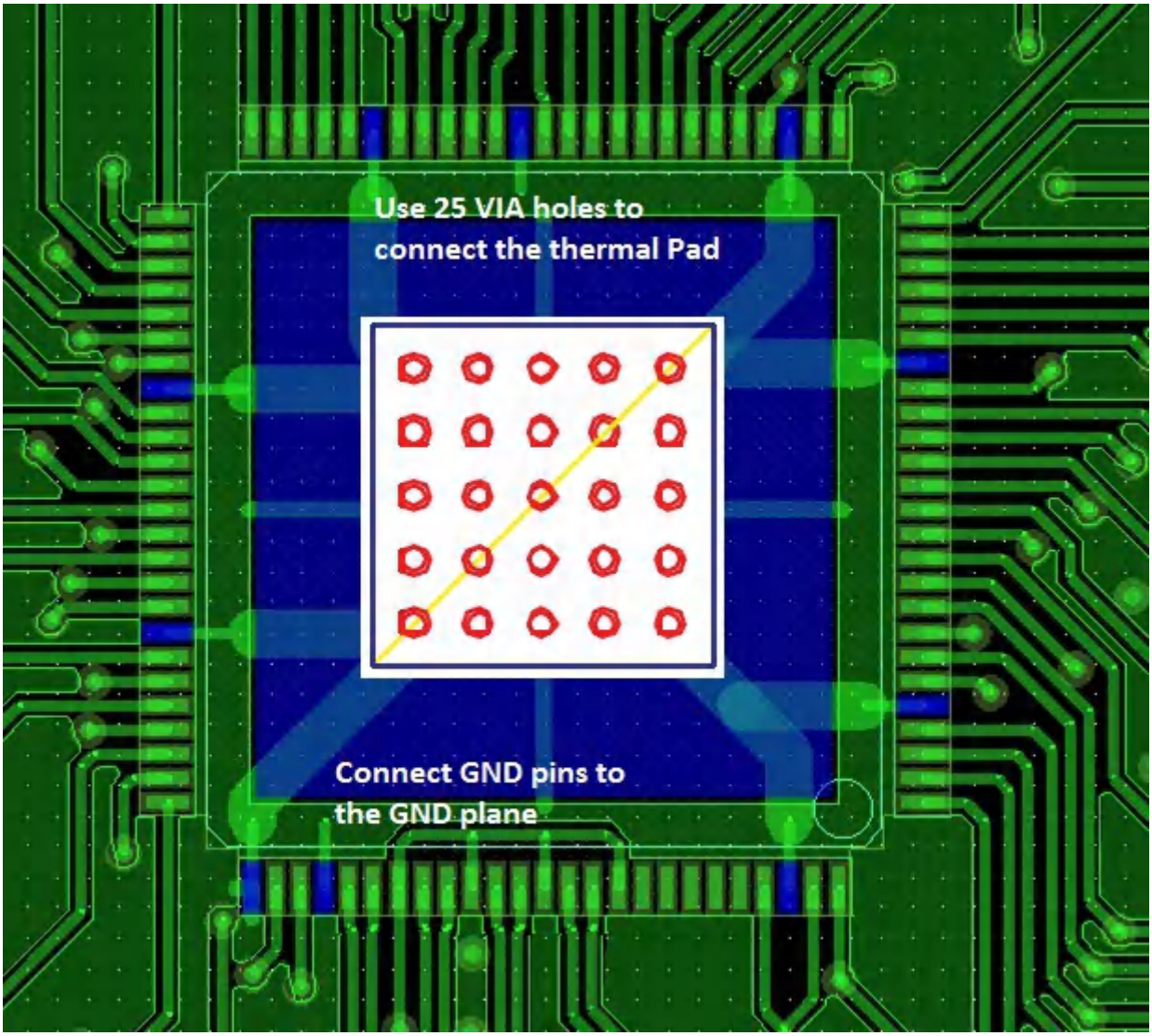


图 7-9. Ground Routing

7.4.3 TI PowerPAD 64-Pin HTQFP Package

The TFP410 is available in TI’s thermally enhanced 64-pin TQFP PowerPAD package. The PowerPAD package is a 10mm × 10mm × 1.0mm TQFP outline with 0.5mm lead-pitch. The PowerPAD package has a specially designed die mount pad that offers improved thermal capability over typical TQFP packages of the same outline. The TI 64-pin TQFP PowerPAD package offers a backside solder plane that connects directly to the die mount pad for enhanced thermal conduction. For thermal considerations, soldering the backside of the TFP410 to the application board is not required because the device power dissipation is well within the package capability when not soldered.

Soldering the backside of the device to the PCB ground plane is recommended for electrical considerations. Because the die pad is electrically connected to the chip substrate and hence chip ground, connecting the back side of the PowerPAD package to a PCG ground plane provides a low-inductance, low-impedance connection to help improve EMI, ground bounce, and power supply noise performance.

表 7-1 contains the thermal properties of the TI 64-pin TQFP PowerPAD package. The 64-pin TQFP non-PowerPAD package is included only for reference.

表 7-1. TI 64-Pin TQFP (10mm × 10mm × 1.0mm) / 0.5mm Lead-Pitch

PARAMETER		WITHOUT PowerPAD™	PowerPAD™ NOT CONNECTED TO PCB THERMAL PLANE	PowerPAD™ CONNECTED TO PCB THERMAL PLANE(1)
$R_{\theta JA}$	Thermal resistance, junction-to-ambient(1) (2)	75.83°C/W	42.20°C/W	21.47°C/W
$R_{\theta JC}$	Thermal resistance, junction-to-case (1) (2)	7.80°/W	0.38°C/W	0.38°C/W
P_D	Power handling capabilities of package (1) (2) (3)	0.92 W	1.66 W	3.26 W

(1) Specified with the PowerPAD bond pad on the backside of the package soldered to a 2-oz. Cu plate PCB thermal plane.
(2) Airflow is at 0 LFM (no airflow)
(3) Specified at 150°C junction temperature and 80°C ambient temperature.

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8 Device and Documentation Support

8.1 接收文档更新通知

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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (November 2014) to Revision D (February 2024)	Page
• 在整个数据表中添加了包容性术语	1
• Changed pin 22 from: *TVC* + to: *TXC*+	2
• Updated MSEN pin description from: *when I^2C is disabled (ISEL = low), a low level indicates a powered on receiver is detected at the differential outputs. A high level indicates a powered on receiver is not detected* to: *when I^2C is disabled (ISEL = low), a high level indicates a powered on receiver is detected at the differential outputs. A low level indicates a powered on receiver is not detected.*	2
• Changed pin 6 name from CTL3/A3/DK3 to A3/DK3	2
• Changed from: *When the I2C bus is disabled (ISEL = low) and the de-skew mode is disabled (DKEN = low), these three inputs become the control inputs, CTL[3:1], which can be used to send additional information across the DVI link during the blanking interval (DE = low). The CTL3 input is reserved for HDCP compliant DVI TXs (TFP510) and the CTL[2:1] inputs are reserved for future use.* to: *When the I^2C bus is disabled (ISEL = low) and the de-skew mode is disabled (DKEN = low), pins 7 and 8 become the control inputs, CTL[2:1], which can be used to send additional information across the DVI link during the blanking interval (DE = low). Pin 6 is not used.*	2
• Updated V_{IH} and V_{IL} for Data, DE, VSYNC, HSYNC, and IDCK+/- CMOS inputs and the remaining CMOS inputs	7
• Changed *three user definable control signals, CTL[3:1], during the inactive display or blanking interval* to: *three control signals, CTL[3:1], during the inactive display or blanking interval*	11

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- Changed *the TFP410 encodes and transfers the CTL[3:1] inputs during the vertical blanking interval* to: *the TFP410 encodes and transfers the CTL[2:1] inputs during the vertical blanking interval* 11
- Changed *the CTL3 input is reserved for HDCP compliant DVI TXs and the CTL[2:1] inputs are reserved for future use* to: *CTL3 is reserved for HDCP and is always encoded as 0. The CTL[2:1] inputs are reserved for future use* 11
- Changed RW field for sub-address 0B from RW to R. 19
- Changed CTL_1_MODE register reset value from: *0xFE* to: *0xBE* 21
- Changed in the CTL_3_MODE register, *bit 3 from CTL3 to RSVD* 22
- Added in DE_DLY register *the value must be less than or equal to (2047 - DE_CNT)* 23
- Added in the DE_CNT register *the value must be less than or equal to (2047 - DE_DLY)* 24
- Changed Application Information summary to be focused on TFP410 instead of the TDP401..... 26

Changes from Revision B (May 2011) to Revision C (November 2014)	Page
• 添加了 *ESD 等级* 表、*热性能信息* 表、*典型特性* 部分、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械*、*封装和可订购信息* 部分。	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TFP410PAP	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TFP410PAP
TFP410PAP.A	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TFP410PAP
TFP410PAPG4	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TFP410PAP
TFP410PAPR	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TFP410PAP
TFP410PAPR.A	Active	Production	HTQFP (PAP) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	TFP410PAP

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TFP410 :

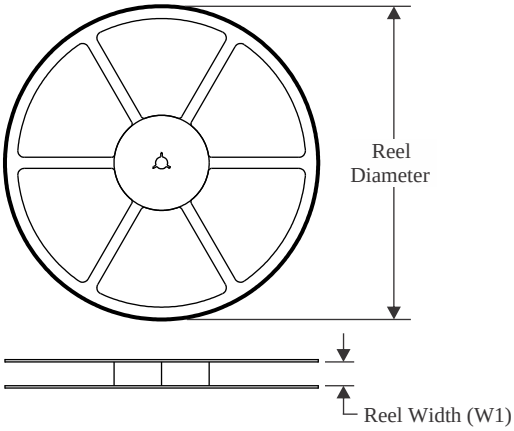
- Enhanced Product : TFP410-EP

NOTE: Qualified Version Definitions:

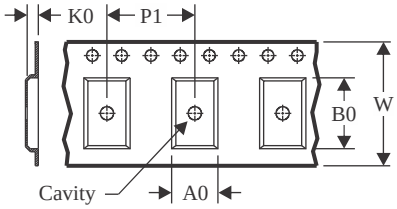
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

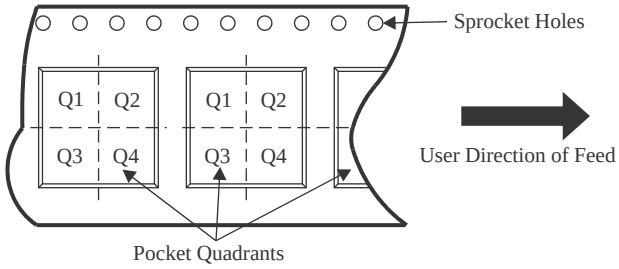


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

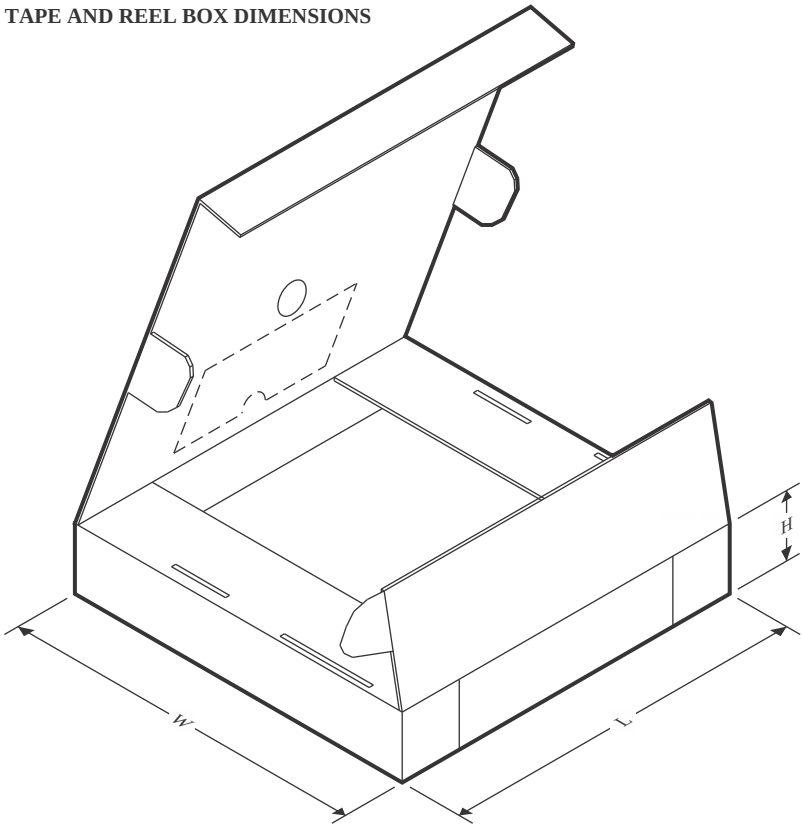
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TFP410PAPR	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

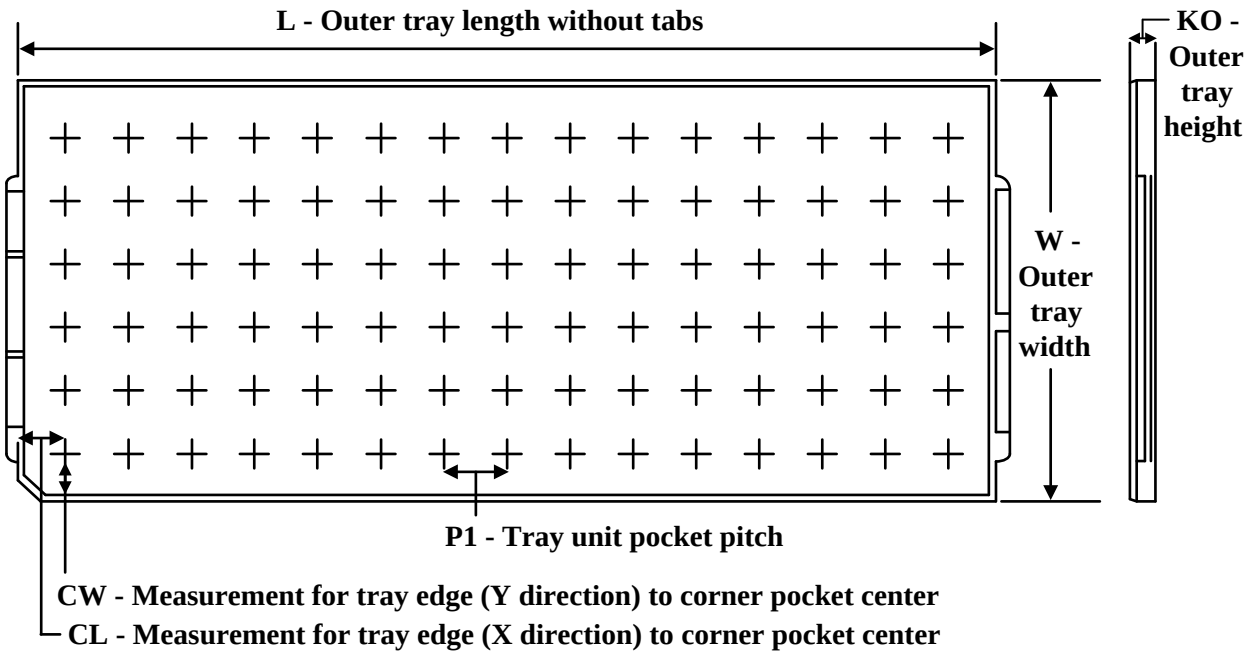
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TFP410PAPR	HTQFP	PAP	64	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TFP410PAP	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
TFP410PAP.A	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
TFP410PAPG4	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

GENERIC PACKAGE VIEW

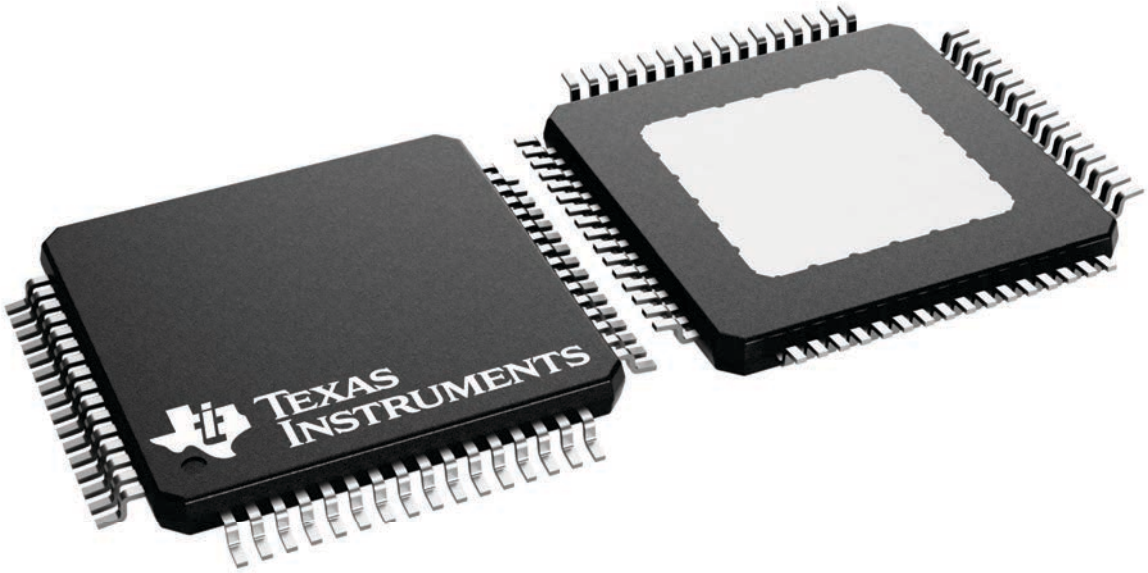
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

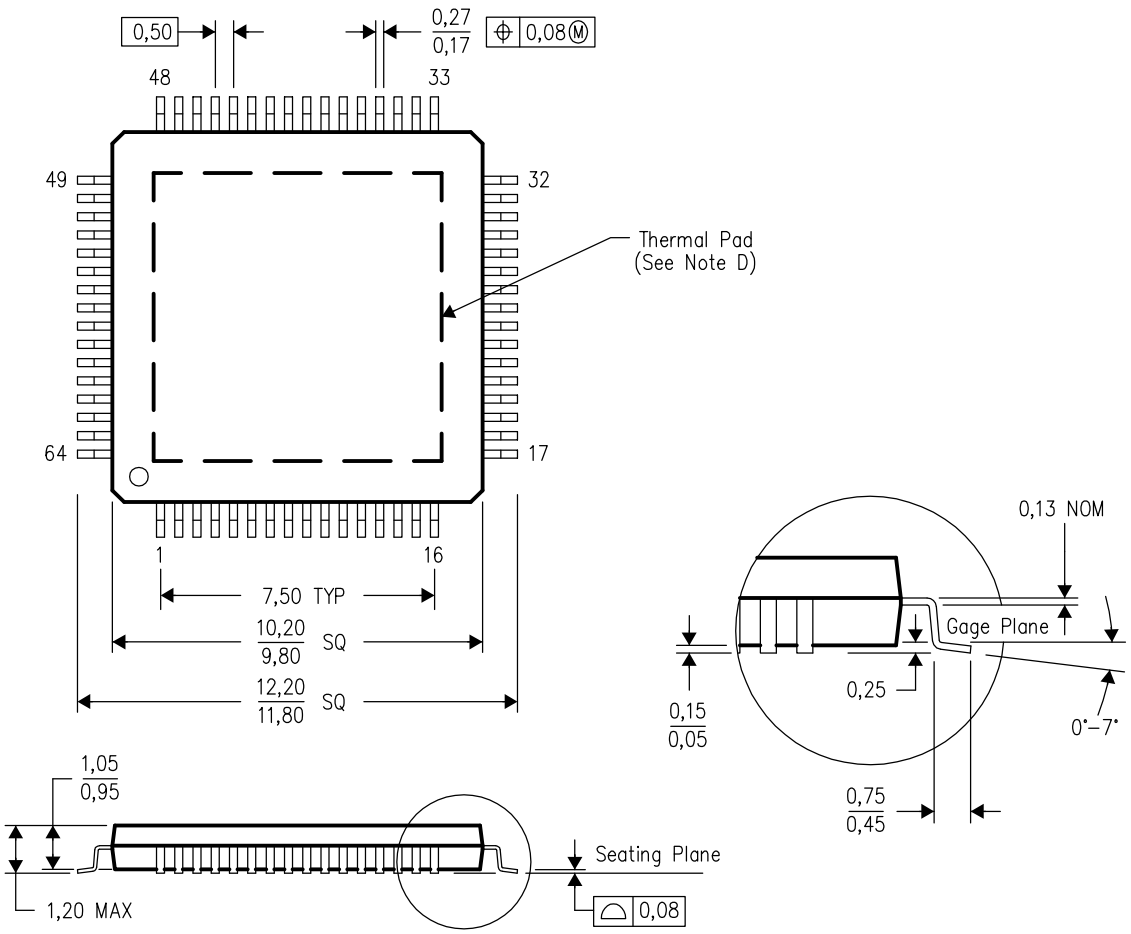
QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226442/A

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

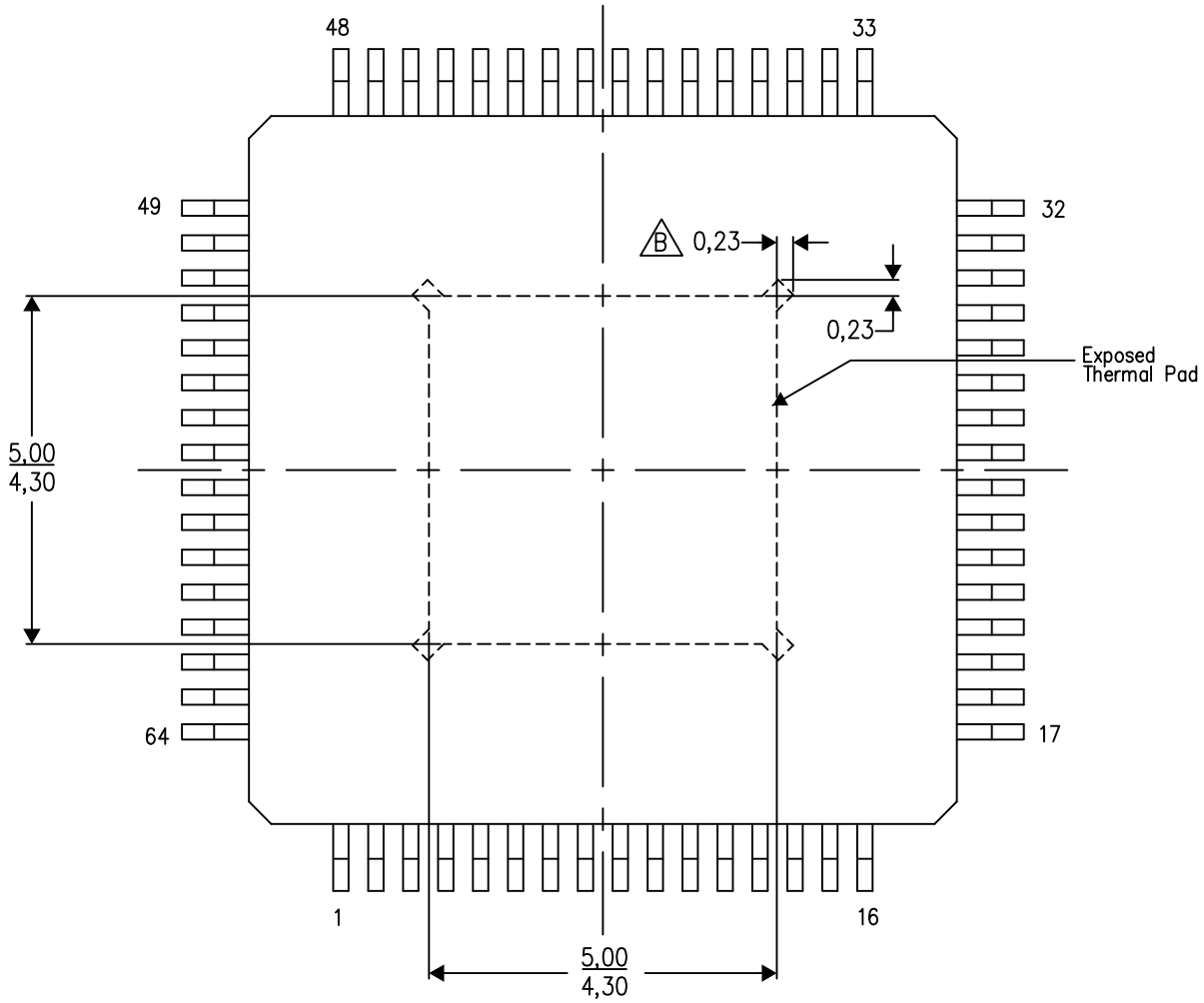
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

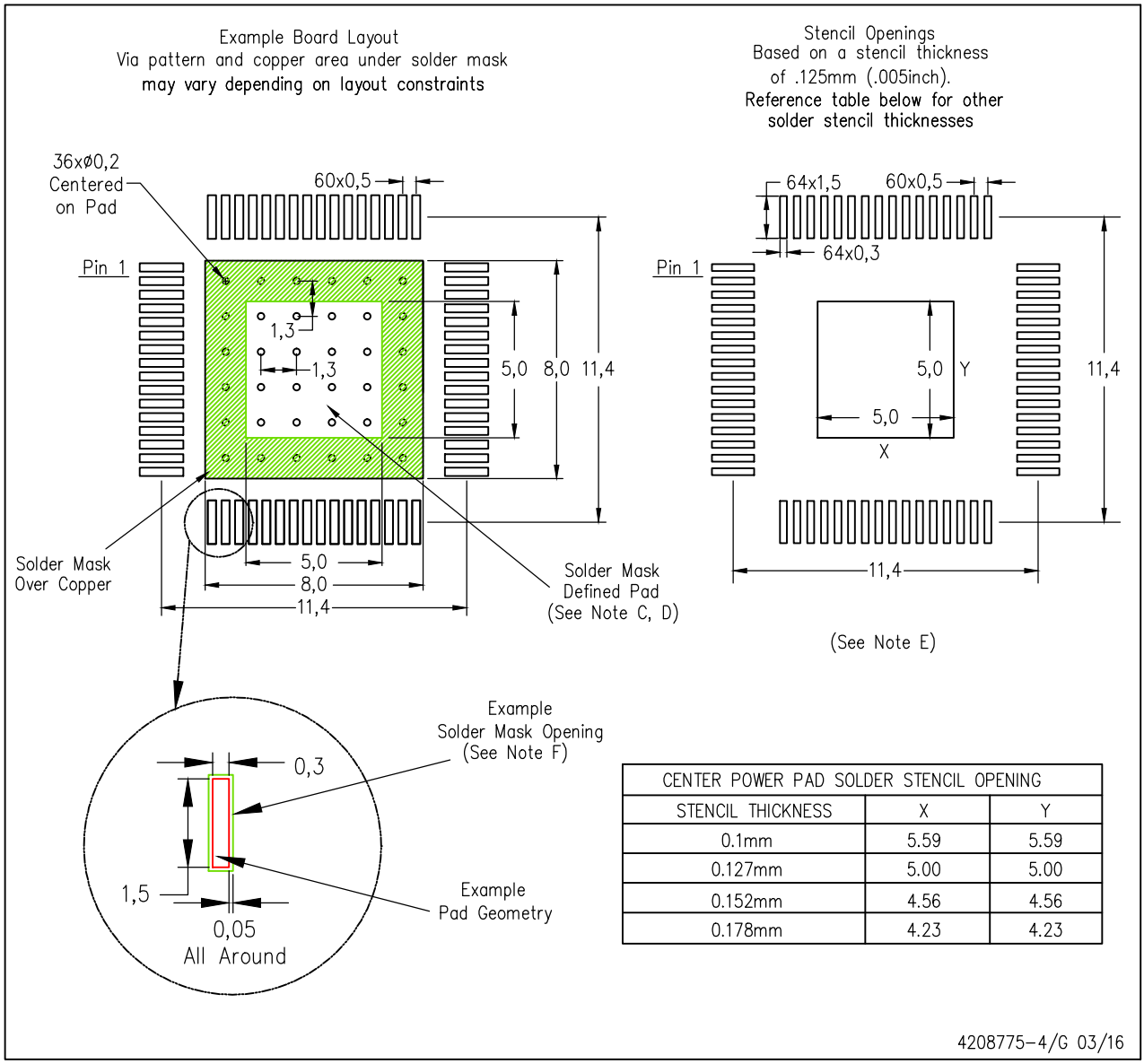
4206326–3/P 05/14

NOTES: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	5.59	5.59
0.127mm	5.00	5.00
0.152mm	4.56	4.56
0.178mm	4.23	4.23

4208775–4/G 03/16

PowerPAD is a trademark of Texas Instruments

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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