《THS413x 高速、低噪声、全差分 I/O 放大器》

1 特性

- 高性能
  - 带宽：170MHz（V_{CC} = ±15V，G = 1V/V）
  - 压摆率：51 V/μs
  - 增益带宽积：215 MHz
  - 失真：–102dBc THD（$2V_{PP}$、250kHz 时）
- 电压噪声
  - 1/f 电压噪声拐角频率：350 Hz
  - 输入基准噪声 1.25nV/√Hz
- 单电源工作电压范围：5 V 至 30 V
- 静态电流（关断）：860μA (THS4130)
- 温度范围：–40°C 至 +85°C
- 封装：PowerPAD™ HVSSOP-8、SOIC-8、VSSOP-8

2 应用

- 单端至差分转换
- 差分 ADC 驱动器
- 差分抗混叠
- 差分发送器和接收器
- 输出电平转换器
- 医疗超声波

3 说明

THS4130 和 THS4131 器件 (THS413x) 是使用德州仪器 (TI) 先进的高压互补双极工艺制造的全差分输入/输出放大器系列。

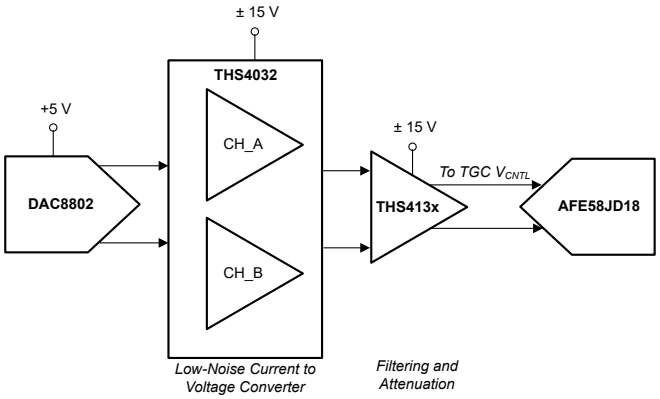
THS413x 使用从输入到输出的真正全差分信号路径，提供高达 ±15V 的高电源电压。这种设计带来了出色的共模噪声抑制能力（800kHz 时为 95dB）和总谐波失真（$2V_{PP}$、250kHz 时为 −102dBc）。高电压差分信号链可通过宽电源电压范围提高裕量和动态范围，而无需为差分信号的每个极性添加单独的放大器。

THS413x 具有 –40°C 至 +85°C 的宽额定运行温度范围。

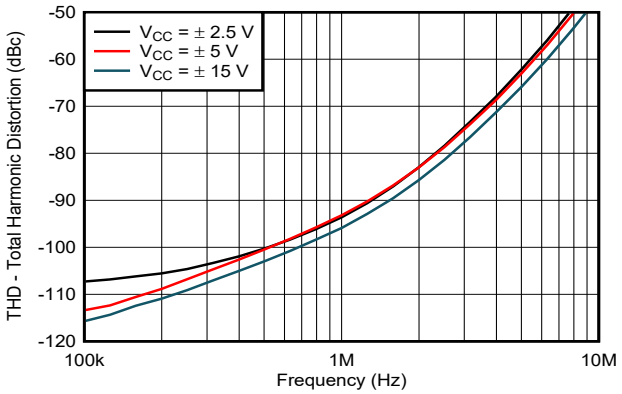
器件信息

器件型号(1)	关断引脚	封装(2)
THS4130	是	D（SOIC，8）、DGK（VSSOP，8）、DGN（HVSSOP，8）
THS4131	否	

(1) 请参阅*器件比较表*。
(2) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



适用于超声波的时间增益控制 DAC 参考设计



V_{OUT} = $2V_{PP}$

总谐波失真与频率间的关系

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision K (August 2022) to Revision L (August 2023) **Page**

- Changed MSOP and MSOP-PowerPad to VSSOP and HVSSOP in Thermal Information table.....4
- Changed thermal specifications for DGN package in *Thermal Information* table.....4
- Changed the Electrical Characteristics section to combine both Electrical Characteristics tables into one table with improved small-signal bandwidth, slew rate, settling time, total harmonic distortion (THD), spurious-free dynamic range (SFDR), voltage noise, offset voltage drift, output swing, and quiescent current parameters for the DGN package.....5
- Changed input current noise typical from 1.3 pA/ √ Hz to 1.7 pA/ √ Hz for DGN package.....5
- Changed common-mode input offset voltage maximum from 3.5 mV to 5.5 mV for DGN package.....5
- Changed maximum input bias current from 6 µA to 15.4 µA for DGN package.....5
- Changed single input resistance parameter into seperate common-mode and differential input resistance parameters for DGN package.....5
- Changed *Typical Characteristics: THS413xD, THS413xDGK* title to *Typical Characteristics* and deleted obsolete *Typical Characteristics: THS413xDGN* section; all plots now in one section.....7

Changes from Revision J (March 2022) to Revision K (August 2022) **Page**

- Updated thermal specifications for DGK package in *Thermal Information* table.....4
- Changed title of *Electrical Characteristics: THS413xD* to *Electrical Characteristics: THS413xD, THS413xDGK* 5
- Changed title of *Typical Characteristics: THS413xD* to *Typical Characteristics: THS413xD, THS413xDGK* 7

5 Device Comparison Table

T_A	D (SOIC, 8)	DGK (VSSOP, 8)	DGN (HVSSOP, 8)
0°C to +70°C	THS4130CD	THS4130CDGK	THS4130CDGN
	THS4131CD	THS4131CDGK	THS4131CDGN
–40°C to +85°C	THS4130ID	THS4130IDGK	THS4130IDGN
	THS4131ID	THS4131IDGK	THS4131IDGN

6 Pin Configuration and Functions

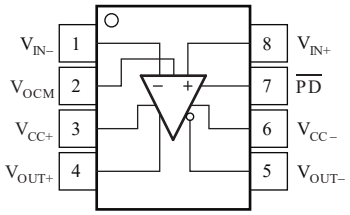


图 6-1. D Package, 8-Pin SOIC, DGK Package, 8-pin VSSOP, DGN Package, 8-Pin HVSSOP THS4130 (Top View)

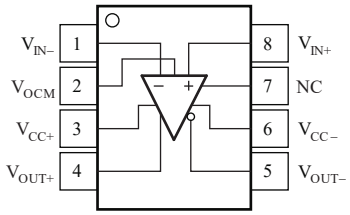


图 6-2. D Package, 8-Pin SOIC, DGK Package, 8-pin VSSOP, DGN Package, 8-Pin HVSSOP THS4131 (Top View)

表 6-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	THS4130	THS4131		
NC	—	7	—	No connect
$\overline{PD}$	7	—	I	Active low power-down pin
V_{CC+}	3	3	I/O	Positive supply voltage pin
V_{CC-}	6	6	I/O	Negative supply voltage pin
V_{IN-}	1	1	I	Negative input pin
V_{OCM}	2	2	I	Common mode input pin
V_{OUT+}	4	4	O	Positive output pin
V_{OUT-}	5	5	O	Negative output pin
V_{IN+}	8	8	I	Positive input pin
Thermal Pad	Thermal Pad	Thermal Pad	—	Thermal pad. DGN (HVSSOP) package only. For the best thermal performance, connect the thermal pad to a large copper plane. This pad is electrically isolated from the die so the pad can be connected to any pin on the package.

(1) I = input, O = output.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage		$-V_{CC}$	$+V_{CC}$	V
V_{CC-} to V_{CC+}	Supply voltage			33	V
	Supply turn on and turn off dV/dT(2)			1.7	V/µs
I_O	Output current(3)			150	mA
V_{ID}	Differential input voltage		−1.5	1.5	V
I_{IN}	Continuous input current			10	mA
T_J	Junction temperature			150	°C
	Junction temperature, continuous operation, long-term reliability(4)			125	°C
T_A	Ambient temperature	C-suffix	0	70	°C
		I-suffix	−40	85	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Stay below this specification to make sure that the edge-triggered ESD absorption devices across the supply pins remain off.
(3) Some of the THS413x packages incorporate a thermal pad on the underside of the chip. This thermal pad acts as a heat sink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature which can permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about using the PowerPAD integrated circuit package.
(4) The maximum junction temperature for continuous operation is limited by package constraints. Operation greater than this temperature can result in reduced reliability, reduced lifetime of the device, or both.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Dual supply	±2.5		±15	V
		Single supply	5		30	
T_A	Operating free-air temperature	C-suffix device	0		70	°C
		I-suffix device	−40		85	

7.4 Thermal Information

THERMAL METRIC(1)		THS413x			UNIT
		D (SOIC)	DGK (VSSOP)	DGN (HVSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.3	147.3	57.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.3	37.9	76.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.8	83.2	30.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.5	0.9	4.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.0	81.6	29.9	°C/W

THERMAL METRIC[1]		THS413x			UNIT
		D (SOIC)	DGK (VSSOP)	DGN (HVSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	14.3	°C/W

(1) For information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

at V_{CC} = ±5 V, gain = 1 V/V, R_F = 390 Ω, R_L = 800 Ω, and T_A = +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
SSBW	Small-signal bandwidth (–3 dB)	V_I = 63 mV_{PP}, gain = 1, R_F = 390 Ω, single-ended input, differential output	V_{CC} = 5 V		165		MHz
			V_{CC} = ±5 V		166		
			V_{CC} = ±15 V		170		
		V_I = 63 mV_{PP}, gain = 2, R_F = 750 Ω, single-ended input, differential output	V_{CC} = 5 V		97		
			V_{CC} = ±5 V		98		
			V_{CC} = ±15 V		100		
SR	Slew rate[2]				67		V/µs
t_s	Settling time	To 0.1%	Step voltage = 2 V, gain = 1		39		ns
		To 0.01%	Step voltage = 2 V, gain = 1		61		
DISTORTION PERFORMANCE							
THD	Total harmonic distortion	V_{CC} = 5 V, V_O = 2 V_{PP}, differential input/output	f = 250 kHz		–101		dBc
			f = 1 MHz		–87		
		V_{CC} = ±5 V, V_O = 2 V_{PP}, differential input/output	f = 250 kHz		–100		
			f = 1 MHz		–87		
		V_{CC} = ±15 V, V_O = 2 V_{PP}, differential input/output	f = 250 kHz		–102		
			f = 1 MHz		–88		
		V_{CC} = ±5 V, V_O = 4 V_{PP}, differential input/output	f = 250 kHz		–94		
			f = 1 MHz		–79		
		V_{CC} = ±15 V, V_O = 4 V_{PP}, differential input/output	f = 250 kHz		–95		
			f = 1 MHz		–80		
SFDR	Spurious-free dynamic range	V_O= 2 V_{PP}, f = 250 kHz, differential input/output	V_{CC} = ±2.5		103		dBc
			V_{CC} = ±5		106		
			V_{CC} = ±15		108		
		V_O = 4 V_{PP}, f = 250 kHz, differential input/output	V_{CC} = ±5		98		
			V_{CC} = ±15		100		
IMD3	Third intermodulation distortion	$V_{I(PP)}$ = 4 V, F_1 = 3 MHz, F_2 = 3.5 MHz			–53		dBc
OIP3	Third-order intercept	$V_{I(PP)}$ = 4 V, F_1 = 3 MHz, F_2 = 3.5 MHz			41.5		dB
NOISE PERFORMANCE							
V_n	Input voltage noise	f = 10 kHz			1.25		nV/√Hz
I_n	Input current noise	f = 10 kHz			1.7		pA/√Hz
DC PERFORMANCE							
A_{OL}	Open-loop gain	T_A = 25°C		71	78		dB
		T_A = full range		69			
V_{OS}	Input offset voltage	T_A = 25°C			±0.2	2	mV
		T_A = full range[1]				3	

7.5 Electrical Characteristics（续）

at V_{CC} = ±5 V, gain = 1 V/V, R_F = 390 Ω, R_L = 800 Ω, and T_A = +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Common-mode input offset voltage	Referred to V_{OCM}			0.2	5.5	mV
	Input offset voltage drift	T_A = full range(1)			2		µV/°C
I_{IB}	Input bias current	T_A = full range(1)			5	15.4	µA
I_{OS}	Input offset current	T_A = full range(1)			100	500	nA
	Input offset current drift				1		nA/°C
INPUT CHARACTERISTICS							
CMRR	Common-mode rejection ratio	T_A = full range(1)		80	95		dB
V_{ICM}	Common-mode input voltage			–3.77 to 4.3	–4 to 4.5		V
R_{I_CM}	Common-mode input resistance	Measured into each input pin			215		MΩ
R_{I_DIFF}	Differential input resistance	Measured into each input pin			10		kΩ
C_{I_CM}	Common-mode input capacitance	Measured into each input pin, closed loop			1.4		pF
C_{I_DIFF}	Differential input capacitance	Measured into each input pin, closed loop			2.5		
OUTPUT CHARACTERISTICS							
R_O	Output resistance	Open loop			41		Ω
	Output voltage swing	V_{CC} = 5 V, R_L = 1 kΩ	T_A = 25°C	1.2 to 3.8	0.9 to 4.1		V
			T_A = full range(1)	1.3 to 3.7	±4		
		V_{CC} = ±5 V, R_L = 1 kΩ	T_A = 25°C	±3.7			
			T_A = full range(1)	±3.6			
		V_{CC} = ±15 V, R_L = 1 kΩ	T_A = 25°C	±11.5	±12.4		
			T_A = full range(1)	±11.2			
I_O	Output current	V_{CC} = 5 V, R_L = 7 Ω	T_A = 25°C	25	45		mA
			T_A = full range	20			
		V_{CC} = ±5 V, R_L = 7 Ω	T_A = 25°C	30	55		
			T_A = full range(1)	28			
		V_{CC} = ±15 V, R_L = 7 Ω	T_A = 25°C	65	85		
			T_A = full range(1)	60			
POWER SUPPLY							
I_{CC}	Quiescent current	V_{CC} = ±5 V	T_A = 25°C		10.4	15	mA
			T_A = full range(1)			16	
		V_{CC} = ±15 V	T_A = 25°C		13		
$I_{CC(SD)}$	Quiescent current (shutdown) (THS4130 only)	$\overline{PD}$ = –5 V	T_A = 25°C		0.86	1.4	mA
			T_A = full range(1)			1.5	
PSRR	Power-supply rejection ratio (dc)		T_A = +25°C	73	98		dB
			T_A = full range(1)	70			

(1) The full range temperature is 0°C to +70°C for the C-suffix device, and –40°C to +85°C for the I-suffix device.
(2) Slew rate is measured from an output level range of 25% to 75%.

7.6 Typical Characteristics

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, gain = +1 V/V, differential input, differential output, and R_L = 800 Ω (unless otherwise noted)

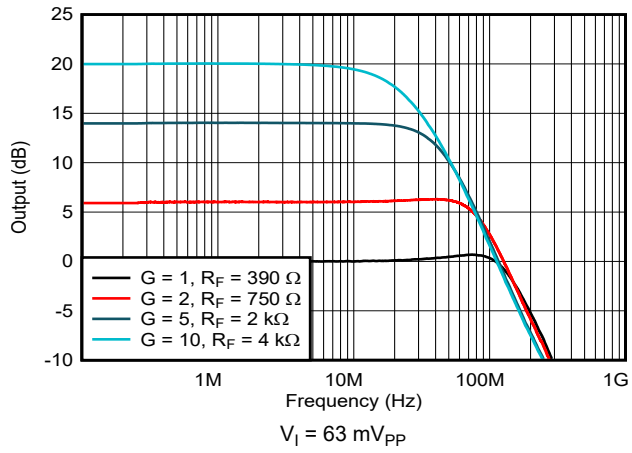


图 7-1. Small-Signal Frequency Response

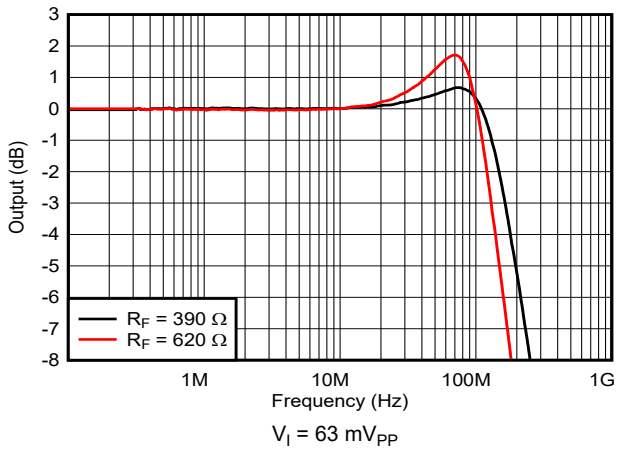


图 7-2. Small-Signal Frequency Response

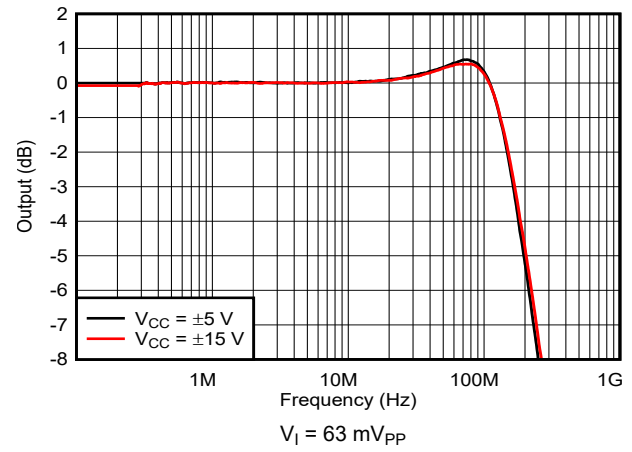


图 7-3. Small-Signal Frequency Response

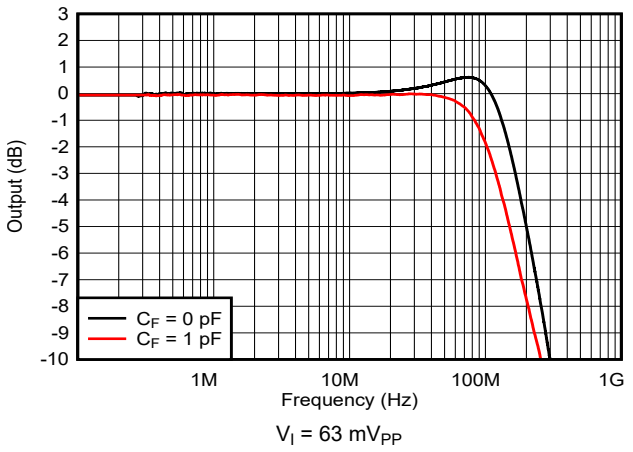


图 7-4. Small-Signal Frequency Response

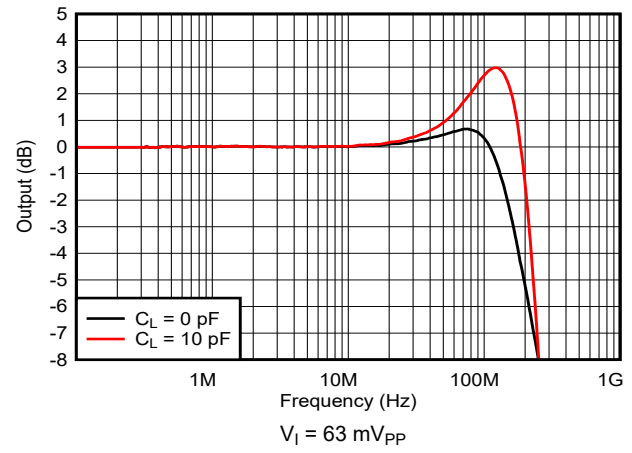


图 7-5. Small-Signal Frequency Response

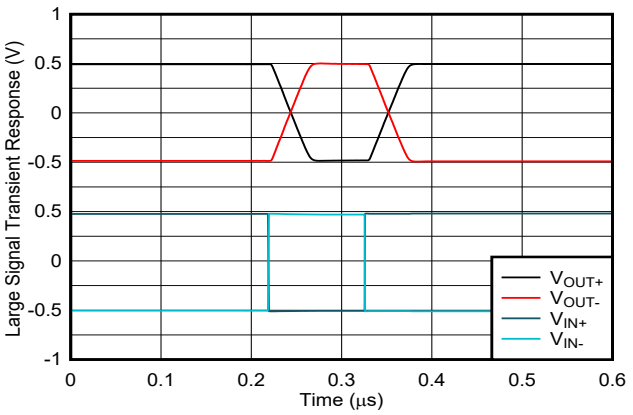
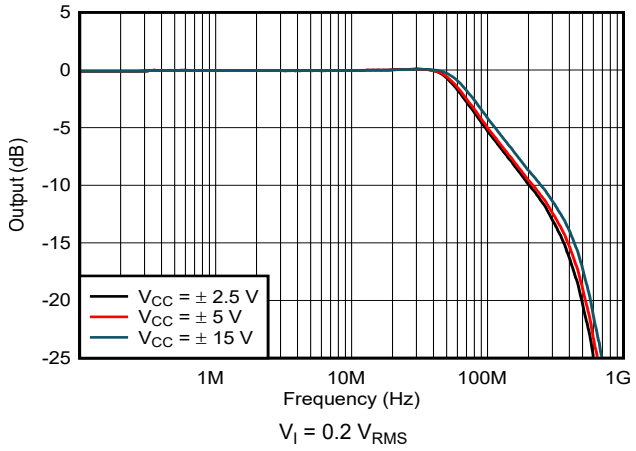


图 7-6. Large-Signal Transient Response (Differential In/Single Out)

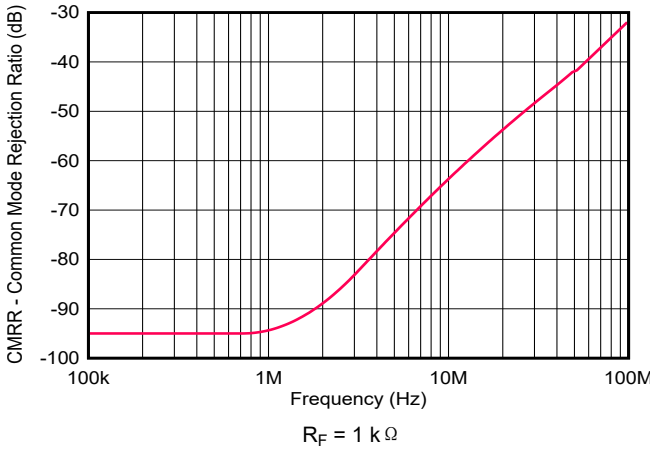
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, gain = +1 V/V, differential input, differential output, and R_L = 800 Ω (unless otherwise noted)



V_I = 0.2 V_{RMS}

图 7-7. Large-Signal Frequency Response



R_F = 1 kΩ

图 7-8. Common-Mode Rejection Ratio vs Frequency

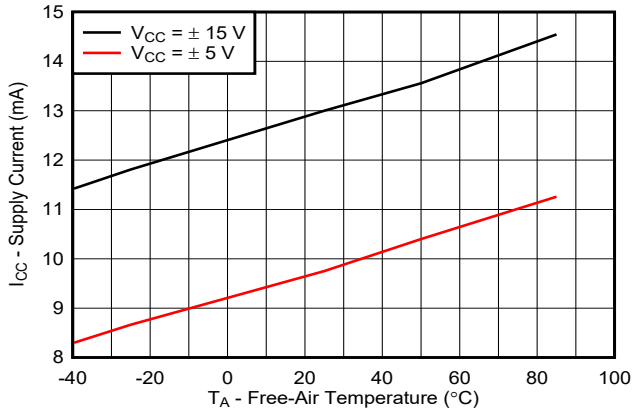


图 7-9. Supply Current vs Free-Air Temperature

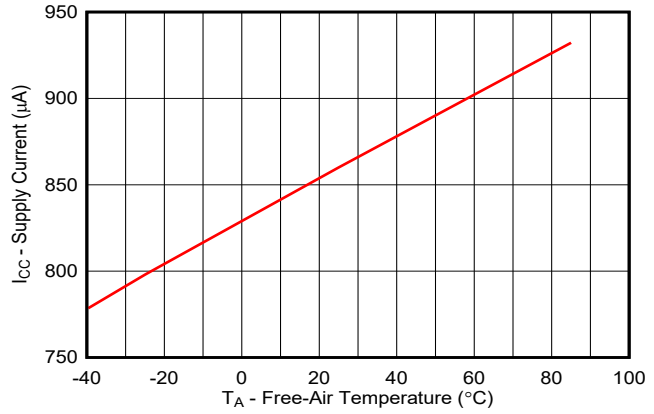


图 7-10. Supply Current vs Free-Air Temperature (Shutdown State)

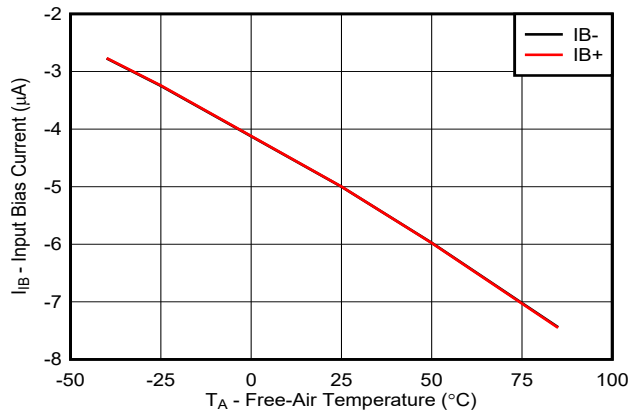
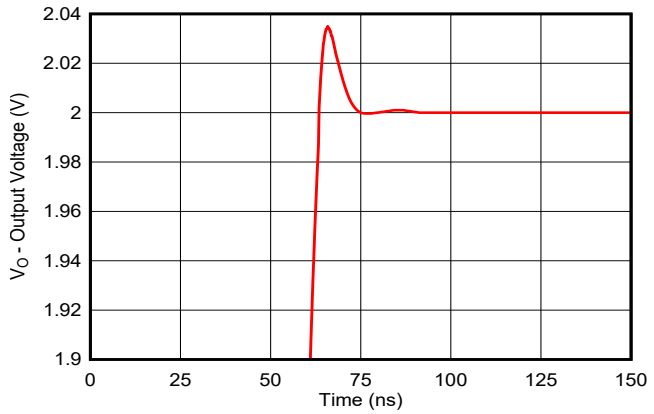


图 7-11. Input Bias Current vs Free-Air Temperature

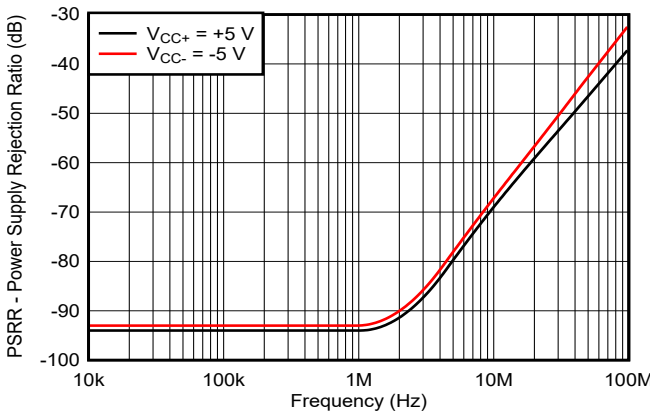


R_F = 510 Ω, C_F= 1 pF, V_{CC}= 5 V, V_O = 4 V_{PP}

图 7-12. Settling Time

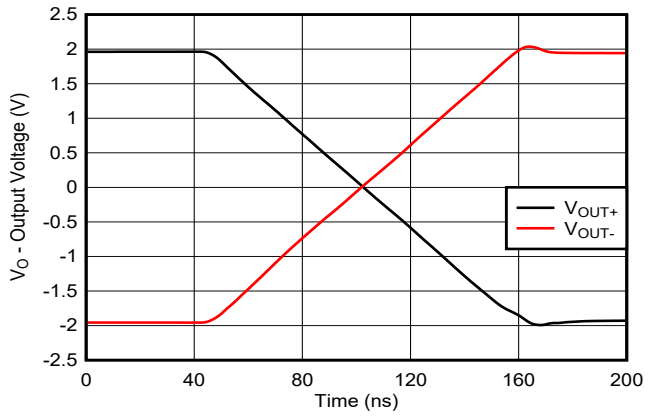
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, gain = +1 V/V, differential input, differential output, and R_L = 800 Ω (unless otherwise noted)



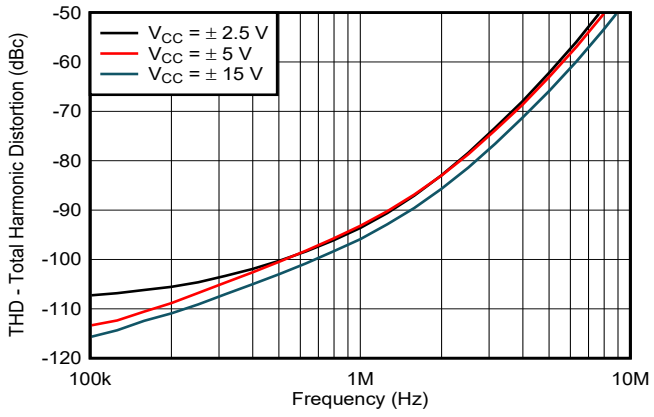
R_F = 330 Ω, R_L = 400 Ω

图 7-13. Power-Supply Rejection Ratio vs Frequency (Differential Out)



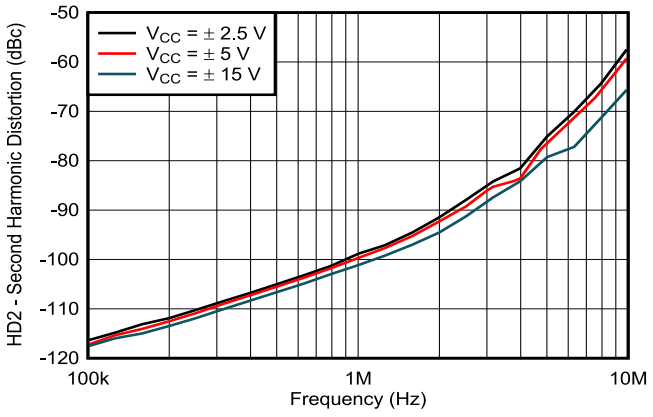
V_{I_Peak} = 2 V, C_L = 10 pF, V_{CC} = ±15 V

图 7-14. Large-Signal Transient Response



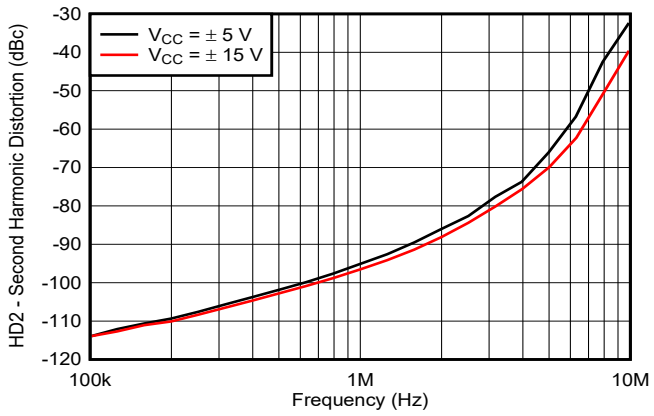
V_{OUT} = 2 V_{PP}

图 7-15. Total Harmonic Distortion vs Frequency



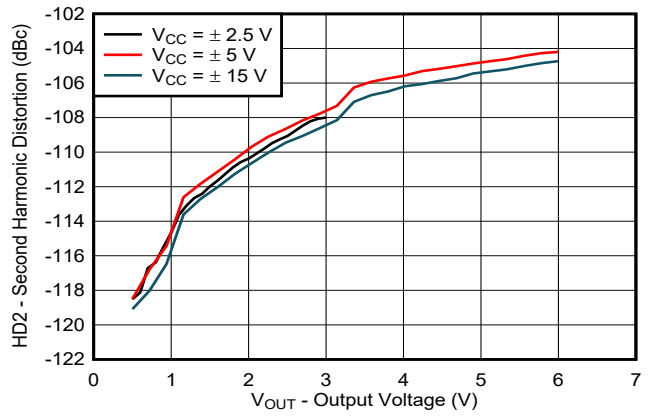
V_{OUT} = 2 V_{PP}, single-ended input, differential output

图 7-16. Second-Harmonic Distortion vs Frequency



V_{OUT} = 4 V_{PP}, single-ended input, differential output

图 7-17. Second-Harmonic Distortion vs Frequency

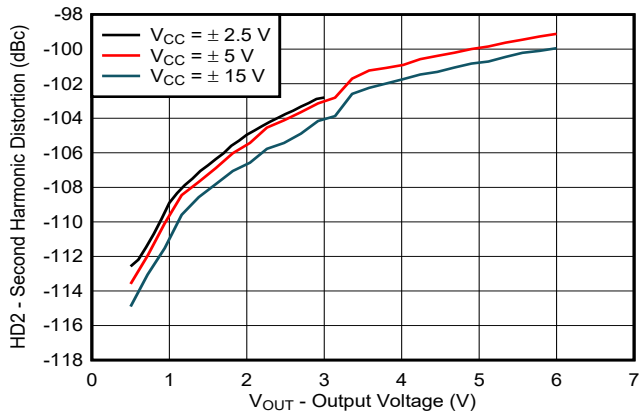


f = 250 kHz, single-ended input, differential output

图 7-18. Second-Harmonic Distortion vs Output Voltage

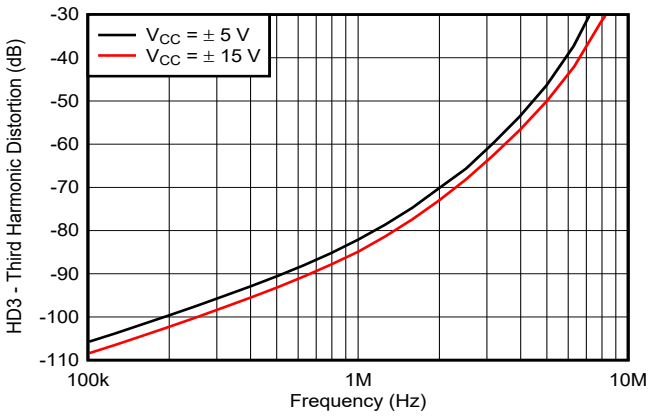
7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, gain = +1 V/V, differential input, differential output, and R_L = 800 Ω (unless otherwise noted)



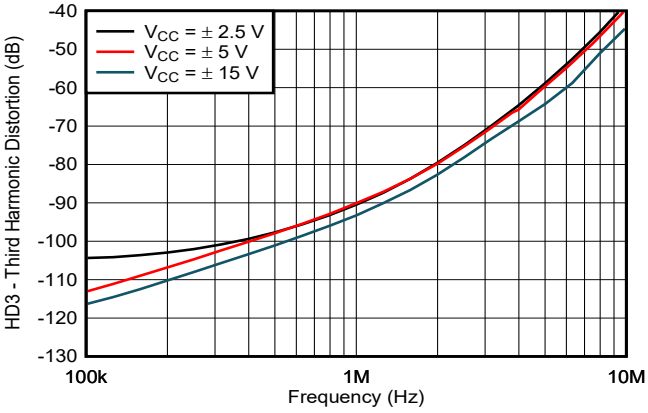
f = 500 kHz, single-ended input, differential output

图 7-19. Second-Harmonic Distortion vs Output Voltage



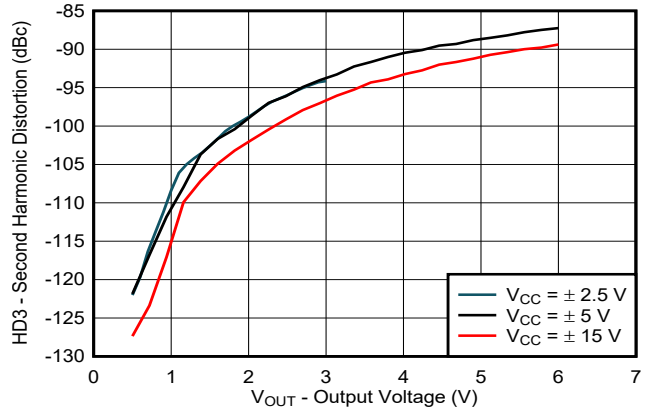
V_{OUT} = 4 V_{PP}, single-ended input, differential output

图 7-20. Third-Harmonic Distortion vs Frequency



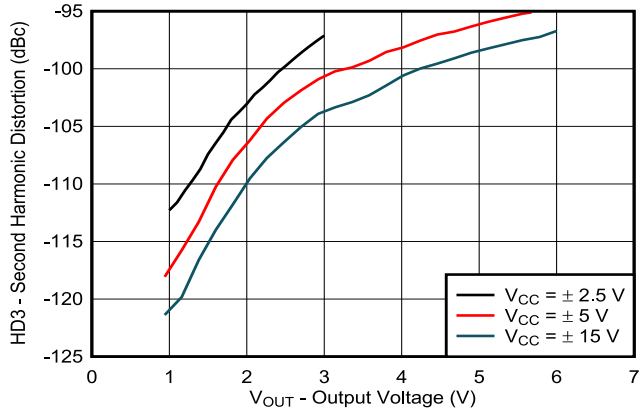
V_{OUT} = 2 V_{PP}, single-ended input, differential output

图 7-21. Third-Harmonic Distortion vs Frequency



f = 500 kHz, single-ended input, differential output

图 7-22. Third-Harmonic Distortion vs Output Voltage



f = 250 kHz, single-ended input, differential output

图 7-23. Third-Harmonic Distortion vs Output Voltage

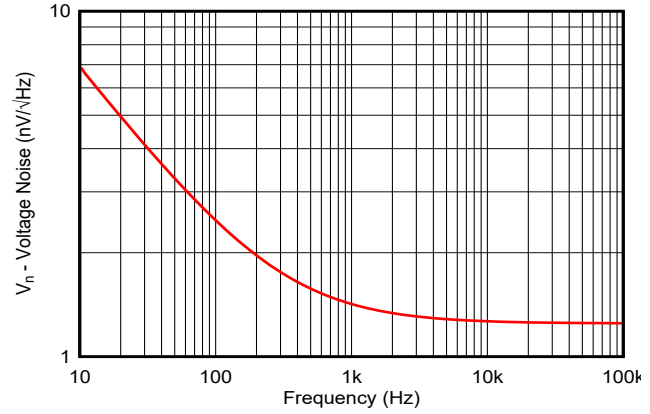


图 7-24. Voltage Noise vs Frequency

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = ±5 V, R_F = 390 Ω, gain = +1 V/V, differential input, differential output, and R_L = 800 Ω (unless otherwise noted)

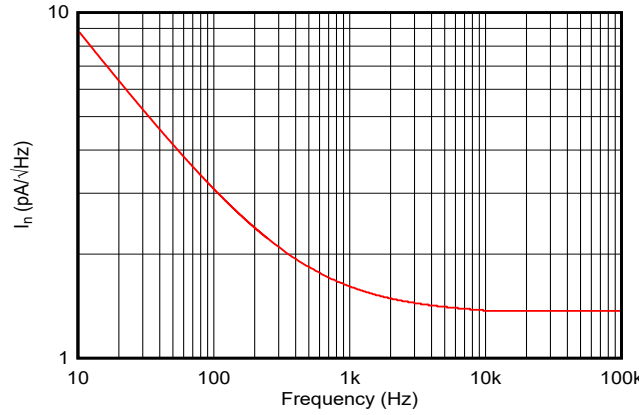
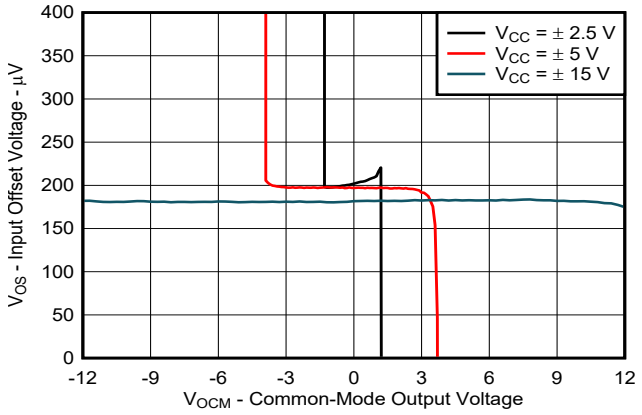
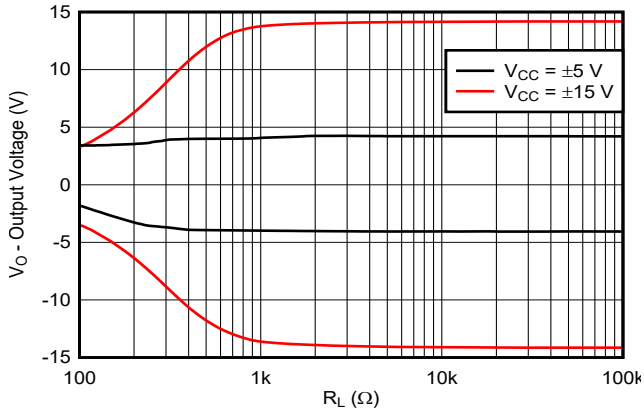


图 7-25. Current Noise vs Frequency



R_F = 1 kΩ

图 7-26. Input Offset Voltage vs Common-Mode Output Voltage



R_F = 1 kΩ, G = 2 V/V

图 7-27. Output Voltage vs Differential Load Resistance

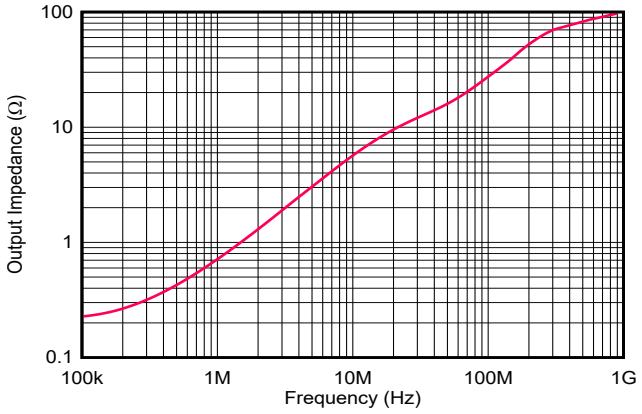


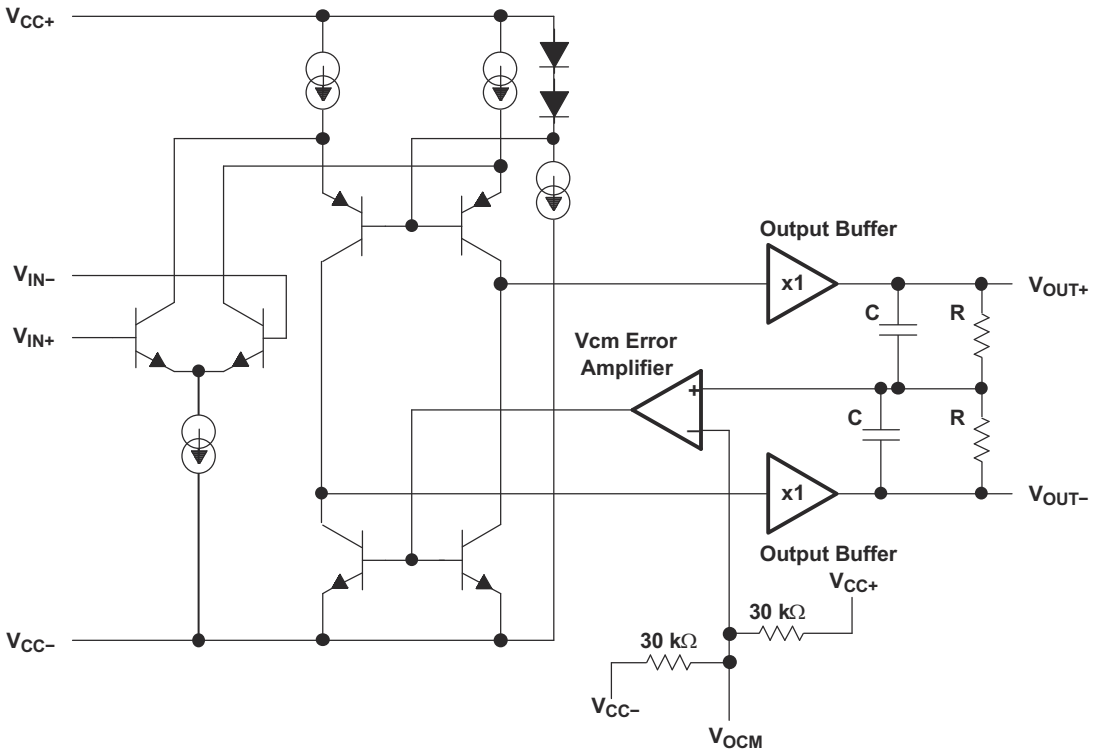
图 7-28. Output Impedance vs Frequency

8 Detailed Description

8.1 Overview

The THS413x devices are fully differential amplifiers (FDAs). Differential signal processing offers a number of performance advantages in high-speed analog signal processing systems, including immunity to external common-mode noise, suppression of even-order nonlinearities, and increased dynamic range. FDAs not only serve as the primary means of providing gain to a differential signal chain, but also provide a monolithic solution for converting single-ended signals into differential signals allowing for easy, high-performance processing. For more information on the basic theory of operation for FDAs, see the *Fully Differential Amplifiers* application note.

8.2 Functional Block Diagram



8.3 Feature Description

图 8-1 and 图 8-2 depict the differences between the operation of the THS413x in two different modes. FDAs can work with either differential or single-ended inputs.

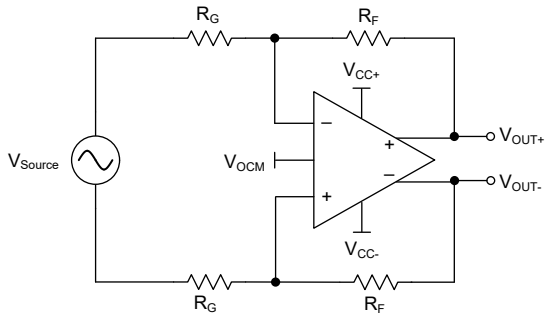


图 8-1. Amplifying Differential Input Signals

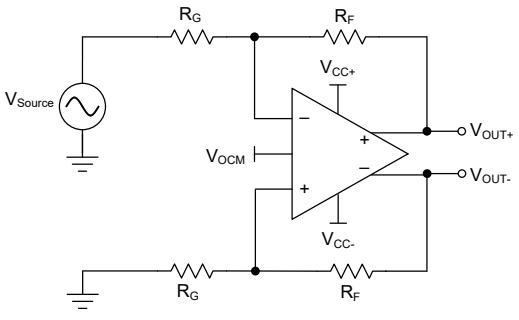


图 8-2. Amplifying Single-ended Input Signals

8.4 Device Functional Modes

8.4.1 Power-Down Mode

Power-down mode is used when power saving is required. The THS4130 power-down ($\overline{PD}$) pin is an active low input. If left unconnected, an internal 250-kΩ resistor to V_{CC+} keeps the device turned on. The threshold voltage for the power-down function is approximately 1.4 V greater than V_{CC-}. Therefore, if the $\overline{PD}$ pin is 1.4 V greater than V_{CC-}, then the device is active. If the $\overline{PD}$ pin is less than 1.4 V greater than V_{CC-}, then the device is off. Pull the pin to V_{CC-} to turn the device off. 图 8-3 shows the simplified version of the power-down circuit. While in power-down mode, the amplifier goes into a high-impedance state. The amplifier output impedance is typically greater than 1 MΩ in power-down mode.

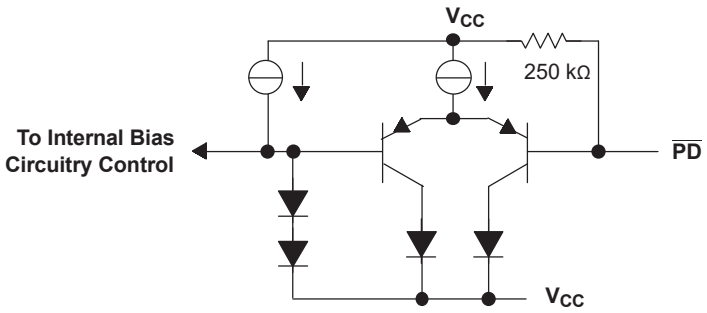
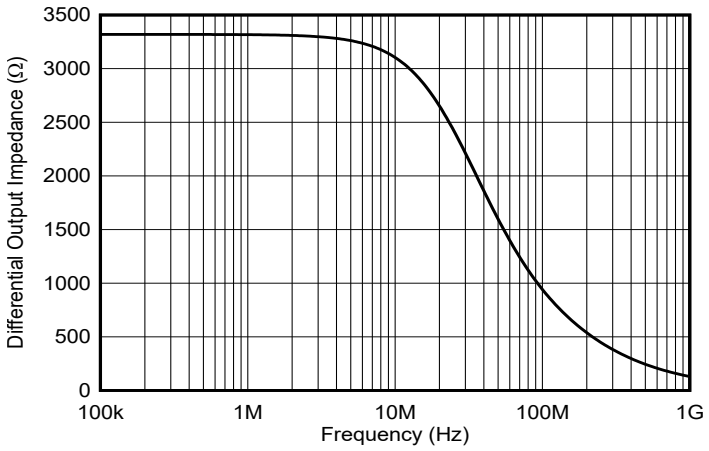


图 8-3. Simplified Power-Down Circuit

Similar to an op amp in an inverting configuration, the output impedance of an FDA is determined by the feedback network configuration. In addition, the THS4130 has an internal 10-kΩ resistor at each output that is tied to the V_{CM} error amplifier (see 节 8.2). The differential output impedance is equal to [(2 × R_F + 2 × R_G) || 20 kΩ]. 图 8-4 shows the closed=loop output impedance of the THS4130 when in power-down.



V_{CC} = ±5 V, gain = 1 V/V, R_F = 1 kΩ, $\overline{PD}$ = V_{CC-}

图 8-4. Output Impedance (in Power-Down) vs Frequency

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.1.1 Output Common-Mode Voltage

The output common-mode voltage pin sets the dc output voltage of the THS413x. A voltage applied to the VOCM pin from a low-impedance source can be used to directly set the output common-mode voltage. If left floating, then the VOCM pin defaults to the mid-rail voltage, defined as:

$$\frac{(V_{CC+}) + (V_{CC-})}{2} \tag{1}$$

To minimize common-mode noise, connect a 0.1-µF bypass capacitor to the VOCM pin. Output common-mode voltage causes additional current to flow in the feedback resistor network. This current is supplied by the output stage of the amplifier; therefore, additional power dissipation is created. For commonly-used feedback resistance values, this current is easily supplied by the amplifier. The additional internal power dissipation created by this current can be significant in some applications and can dictate the use of the HVSSOP package to effectively control self-heating.

9.1.1.1 Resistor Matching

Resistor matching is important in FDAs to maintain good output balance. An ideal differential output signal implies the two outputs of the FDA should be exactly equal in amplitude and shifted 180° in phase. Any imbalance in amplitude or phase between the two output signals results in an undesirable common-mode signal at the output. The output balance error is a measure of how well the outputs are balanced and is defined as the ratio of the output common-mode voltage to the output differential signal.

$$Output\ Balance\ Error = \frac{\left(\frac{V_{OUT+} - V_{OUT-}}{2}\right)}{V_{OUT+} - V_{OUT-}} \tag{2}$$

At low frequencies, resistor mismatch is the primary contributor to output balance errors. Additionally CMRR, PSRR, and HD2 performance diminish if resistor mismatch occurs. Therefore, to optimize performance, use 1% tolerance resistors or better. 表 9-1 provides the recommended resistor values to use for a particular gain.

表 9-1. Recommended Resistor Values

GAIN (V/V)	R_G (Ω)	R_F (Ω)
1	390	390
2	374	750
5	402	2010
10	402	4020

9.1.2 Driving a Capacitive Load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The THS413x have been internally compensated to maximize bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, place a resistor in series with the output of the amplifier, as shown in 图 9-1. A minimum value of 20 Ω works well for most applications. For example, in 50-Ω transmission systems, setting the series resistor value to 50 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

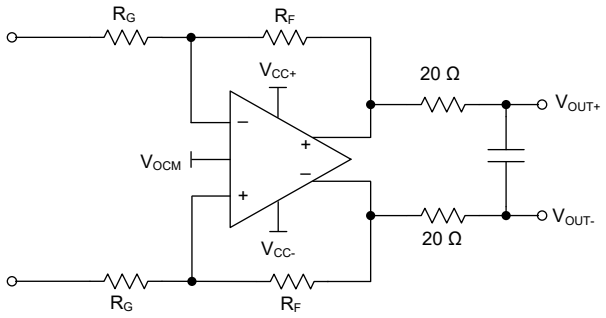


图 9-1. Driving a Capacitive Load

9.1.3 Data Converters

Driving data converters are one of the most popular applications for fully-differential amplifiers. 图 9-2 shows a typical configuration of an FDA attached to a differential analog-to-digital converter (ADC).

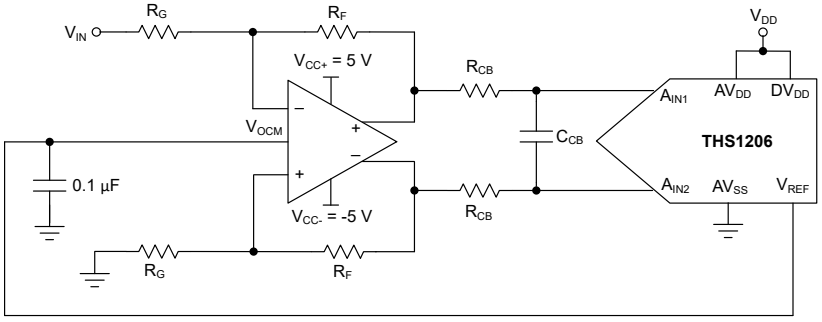


图 9-2. Fully-Differential Amplifier Attached to a Differential ADC

FDAs can operate with a single supply. V_{OCM} defaults to the mid-rail voltage, $V_{CC}/2$. The differential output can be fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{ref}), then connect V_{ref} directly to the V_{OCM} of the amplifier using a bypass capacitor to reduce broadband common-mode noise.

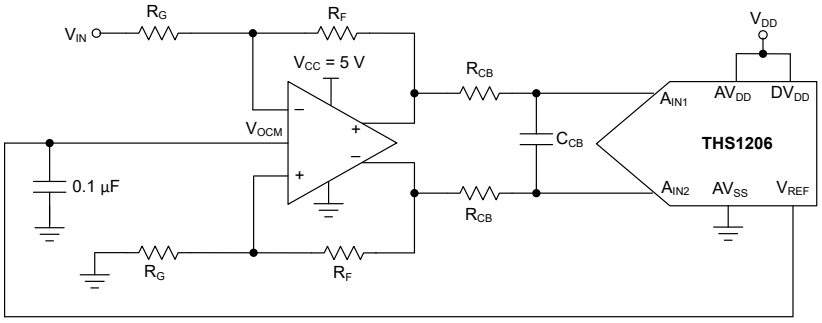


图 9-3. Fully-Differential Amplifier Using a Single Supply

9.1.4 Single-Supply Applications

For proper operation, the input common-mode voltage to the input terminal of the amplifier must not exceed the common-mode input voltage range. However, some single-supply applications can require the input voltage to exceed the common-mode input voltage range. In such cases, to bring the common-mode input voltage within the specifications of the amplifier, the circuit configuration of 图 9-4 is suggested.

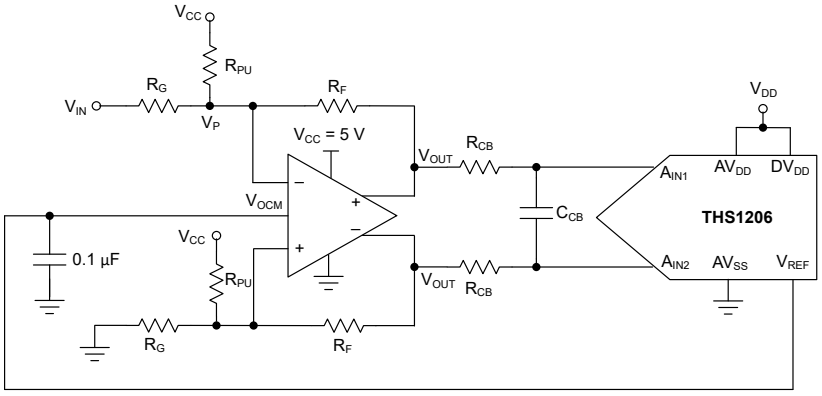


图 9-4. Circuit With Improved Common-Mode Input Voltage

方程式 3 is used to calculate R_{PU}:

$$R_{PU} = \frac{V_P - V_{CC}}{(V_{IN} - V_P)\frac{1}{R_G} + \left(V_{OUT} - V_P\right)\frac{1}{R_F}} \tag{3}$$

9.2 Typical Application

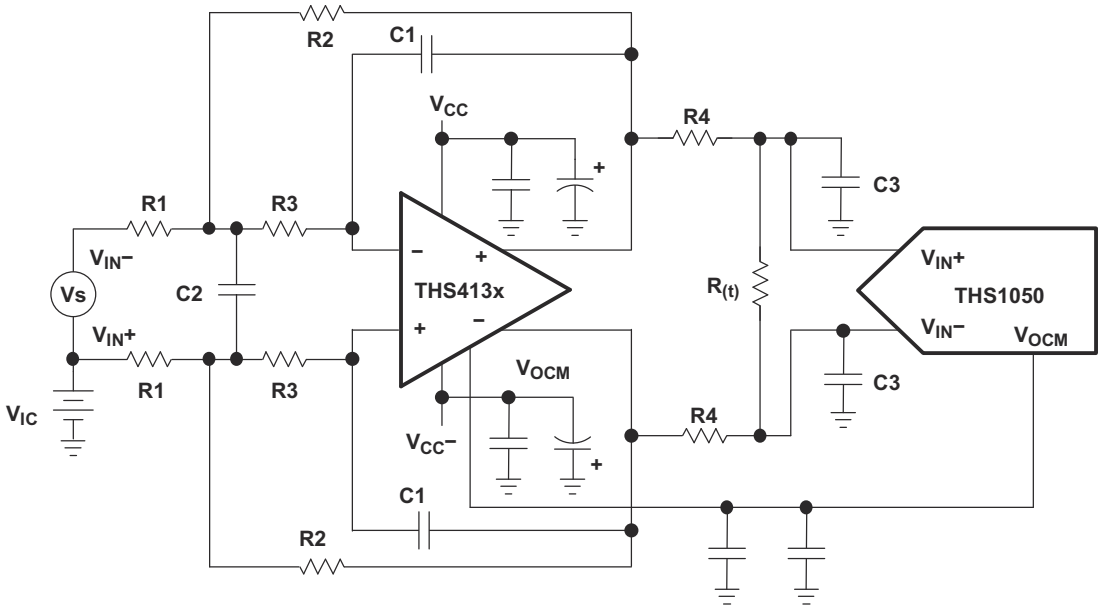


图 9-5. Antialias Filtering

For signal conditioning in ADC applications, make sure to limit the input frequency to the ADC. Low-pass filters can prevent the aliasing of the high-frequency noise with the frequency of operation. This design example shows a method by which the noise can be filtered in the THS413x. 图 9-5 shows the design example for the THS413x in active low-pass filter topology driving an ADC.

9.2.1 Design Requirements

表 9-2 shows example design parameters and values for the typical application design example in 图 9-5.

表 9-2. Design Parameters

DESIGN PARAMETERS	VALUE
Supply voltage	±2.5 V to ±15 V
Amplifier topology	Voltage feedback
Output control	DC-coupled with output common-mode control capability
Filter requirement	500-kHz, multiple-feedback low-pass filter

9.2.2 Detailed Design Procedure

图 9-5 shows a multiple-feedback (MFB) low-pass filter. The transfer function for this filter circuit is:

$$H_d(f) = \left[\frac{K}{-\left[\frac{f}{FSF \times fc}\right]^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1}\right] \times \left[\frac{\frac{Rt}{2R4 + Rt}}{1 + \frac{j2\pi fR4RtC3}{2R4 + Rt}}\right]$$

$$where\ K = \frac{R2}{R1}, FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}}, and\ Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1} \quad (4)$$

K sets the pass-band gain, fc is the cutoff frequency for the filter, FSF is a frequency scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2} \; and \; Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re} \tag{5}$$

where Re is the real part and Im is the imaginary part of the complex pole pair. Setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in:

$$FSF \times fc = \frac{1}{2\pi Rc\sqrt{2 \times mn}} \; and \; Q = \frac{\sqrt{2 \times mn}}{1 + m(1 + K)} \tag{6}$$

Start by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C and calculate R for the desired fc.

9.2.3 Application Curve

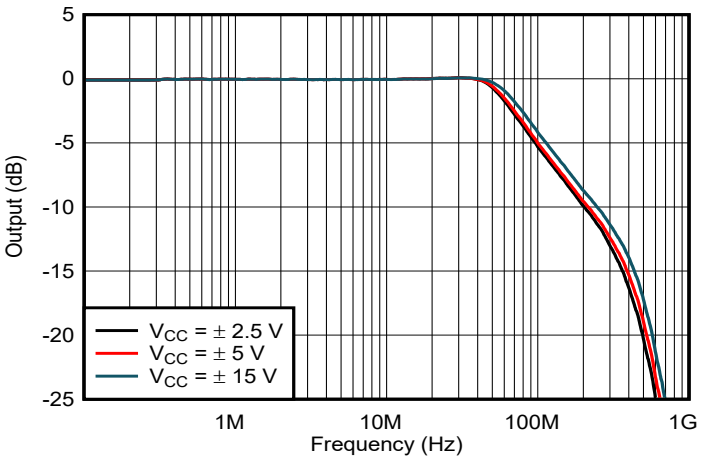


图 9-6. Large-Signal Frequency Response

9.3 Power Supply Recommendations

The THS413x devices are designed to operate on power supplies ranging from ±2.5 V to ±15 V (single-ended supplies of 5 V to 30 V). Use a power-supply accuracy of 5% or better. When operated on a board with high-speed digital signals, make sure to provide isolation between digital signal noise and the analog input pins. The THS413x are connected to power supplies through pin 3 (V_{CC+}) and pin 6 (V_{CC-}). Decouple each supply pin to GND as close to the device as possible with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF. When vias are used to connect the bypass capacitors to a ground plane, configure the vias for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems, two capacitors per supply pin are advised.

To avoid undesirable signal transients, do not power on the THS413x with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

9.4 Layout

9.4.1 Layout Guidelines

To achieve the levels of high-frequency performance of the THS413x devices, follow proper printed-circuit board (PCB) high-frequency design techniques. Following is a general set of guidelines. In addition, a THS413x evaluation board is available to use as a guide for layout or for evaluating device performance.

- Ground planes—Use a ground plane on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling—use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply pin. Sharing the tantalum among several amplifiers is possible depending on the application; however, always use a 0.1-μF ceramic capacitor on the supply pin of every amplifier. In addition, place the 0.1-μF capacitor as close as possible to the supply pin. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. Strive for distances of less than 0.1 inches between the device power pin and the ceramic capacitors.
- Short trace runs or compact part placements—to optimize high-frequency performance, minimize stray series inductance. The best method is to make the circuit layout as compact as possible, thereby minimizing the length of all trace runs. Pay particular attention to the inputs of the amplifier; keep the length as short as possible. This short length helps minimize stray capacitance at the input of the amplifier.

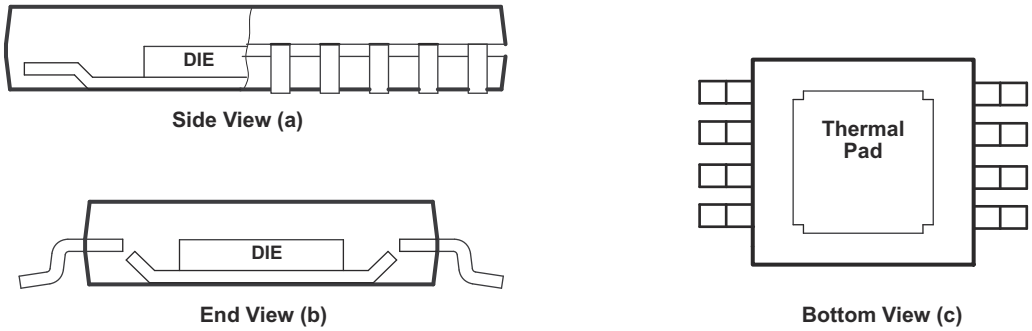
9.4.1.1 PowerPAD™ Integrated Circuit Package Design Considerations

The THS413x is available in a thermally-enhanced DGN package, which is a member of the PowerPAD™ integrated circuit package family. This package is constructed using a downset leadframe upon which the die is mounted (see 图 9-7 **a** and 图 9-7 **b**). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see 图 9-7 **c**). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the previously awkward mechanical methods of using a heat sink.

More complete details of the PowerPAD installation process and thermal management techniques can be found in *PowerPAD Thermally-Enhanced Package* application report. This document can be found on the TI website at www.ti.com by searching for the keyword PowerPAD. The document can also be ordered through your local TI sales office; refer to SLMA002 when ordering.



Note: The thermal pad (PowerPAD) is electrically isolated from all other pins and can be connected to any potential from V_{CC-} to V_{CC+}. Typically, the thermal pad is connected to the ground plane because this plane tends to physically be the largest and is able to dissipate the most amount of heat.

图 9-7. Views of Thermally-Enhanced DGN Package

9.4.2 Layout Example

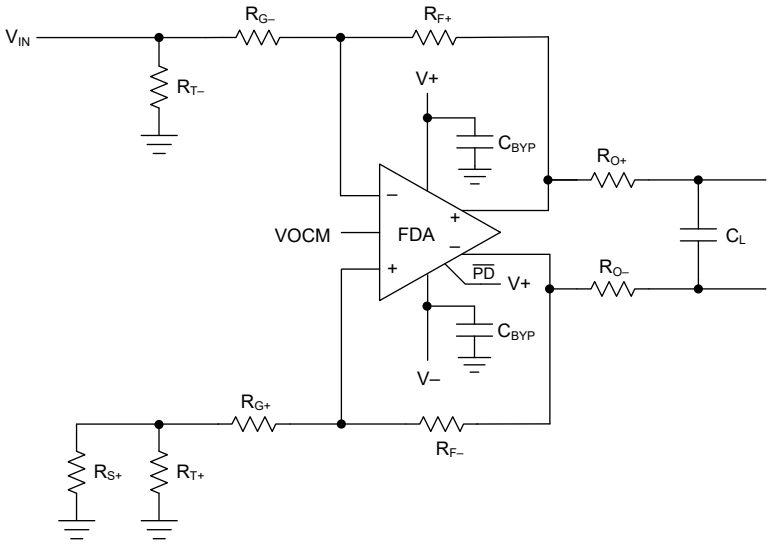


图 9-8. Representative Schematic for Layout

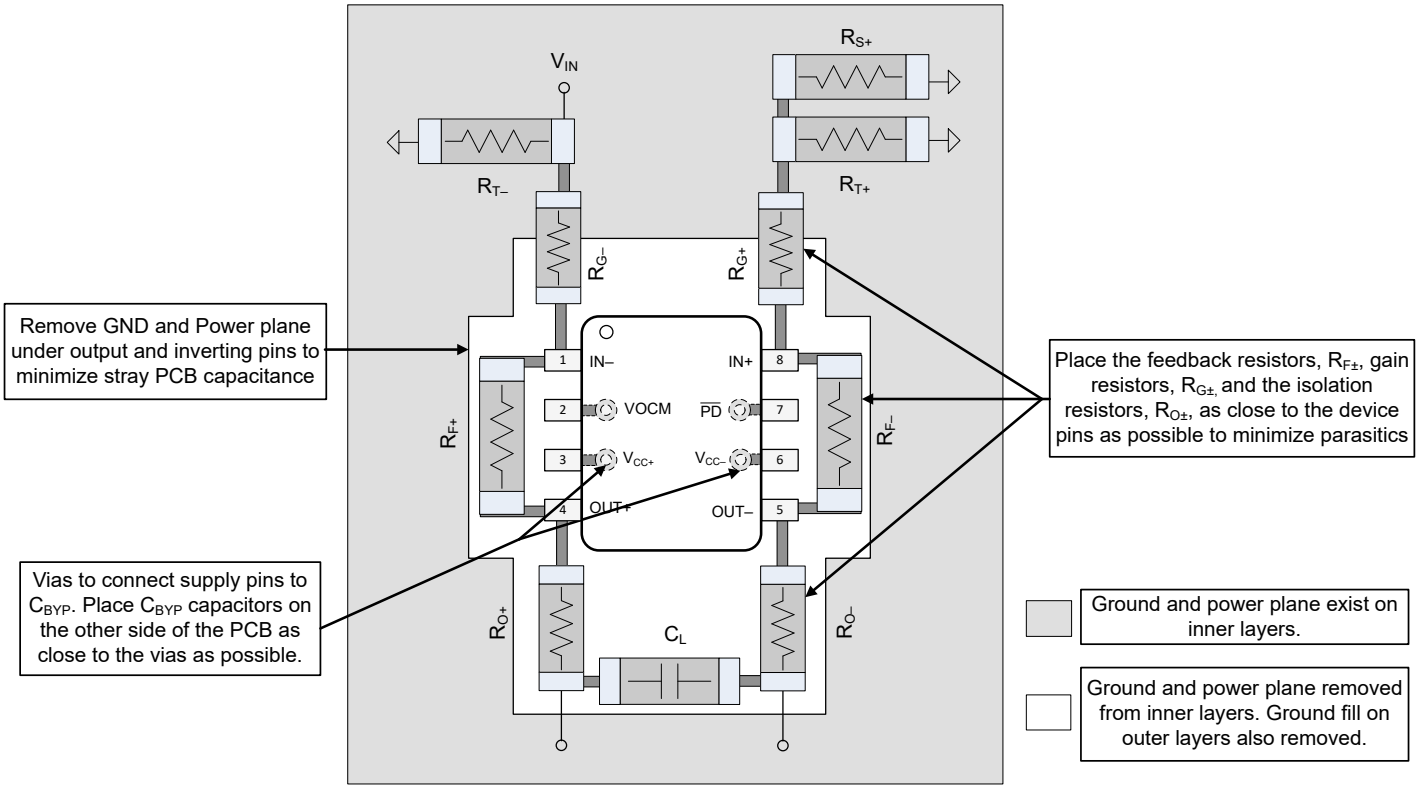


图 9-9. Layout Recommendations

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Design Guide for 2.3 nV/ √Hz, Differential, Time Gain Control (TGC) DAC Reference Design for Ultrasound* design guide
- Texas Instruments, *EVM User's Guide for High-Speed Fully-Differential Amplifier* user's guide
- Texas Instruments, *Fully Differential Amplifiers* application note
- Texas Instruments, *Maximizing Signal Chain Distortion Performance Using High Speed Amplifiers* application note
- Texas Instruments, *PowerPAD Thermally-Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *TI Precision Labs - Fully Differential Amplifiers* video series

10.2 接收文档更新通知

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10.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4130CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	4130C
THS4130CDGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	0 to 70	AOB
THS4130CDGNR	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	0 to 70	AOB
THS4130ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	4130I
THS4130IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASO
THS4130IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASO
THS4130IDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(4130, AOC)
THS4130IDGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(4130, AOC)
THS4130IDGNRG4	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4130
THS4130IDGNRG4.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4130
THS4130IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I
THS4130IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I
THS4130IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I
THS4130IDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I
THS4130IDRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4130I
THS4131CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	4131C
THS4131CDGKR	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	0 to 70	ATQ
THS4131CDGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	0 to 70	AOD
THS4131CDGNR	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	0 to 70	AOD
THS4131CDR	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	4131C
THS4131ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	4131I
THS4131IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP
THS4131IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP
THS4131IDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP
THS4131IDGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP
THS4131IDGKRG4.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASP
THS4131IDGN	Obsolete	Production	HVSSOP (DGN) | 8	-	-	Call TI	Call TI	-40 to 85	AOE
THS4131IDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(4131, AOE)
THS4131IDGNR.B	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(4131, AOE)

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4131IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I
THS4131IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4131I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

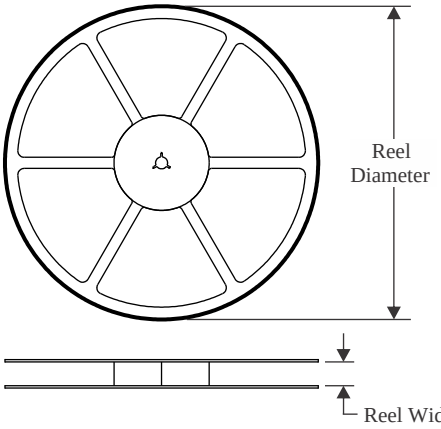
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

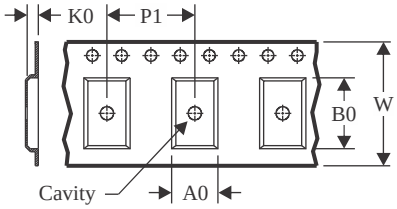
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

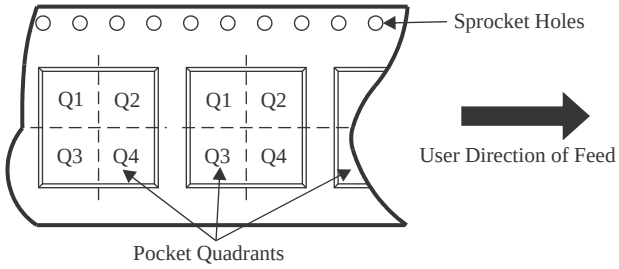


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

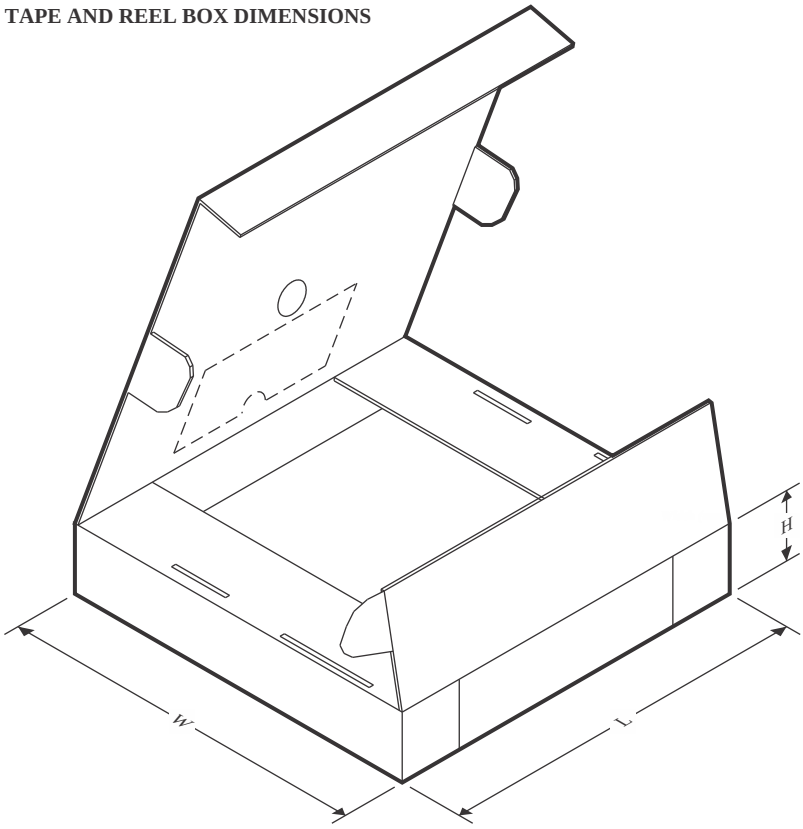
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4130IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THS4130IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDGNRG4	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4130IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4130IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4131IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THS4131IDGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THS4131IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4131IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

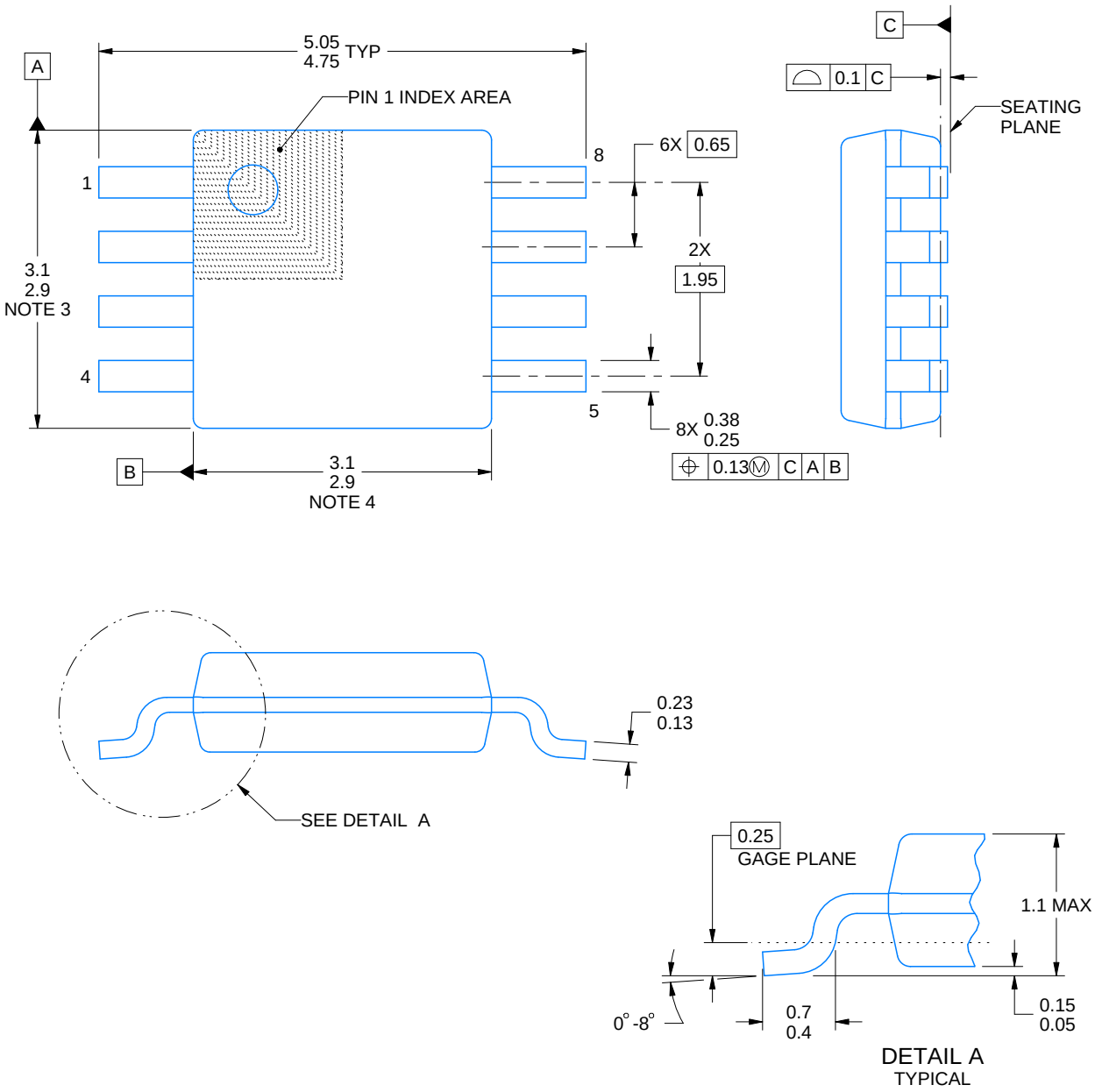
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4130IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THS4130IDGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
THS4130IDGNRG4	HVSSOP	DGN	8	2500	353.0	353.0	32.0
THS4130IDR	SOIC	D	8	2500	353.0	353.0	32.0
THS4130IDRG4	SOIC	D	8	2500	353.0	353.0	32.0
THS4131IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THS4131IDGKRG4	VSSOP	DGK	8	2500	366.0	364.0	50.0
THS4131IDGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
THS4131IDR	SOIC	D	8	2500	353.0	353.0	32.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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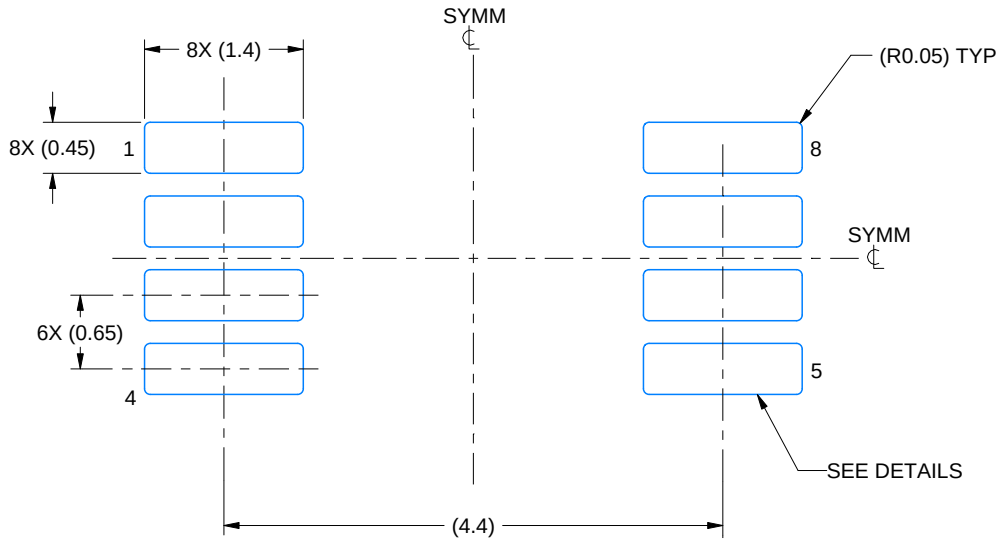
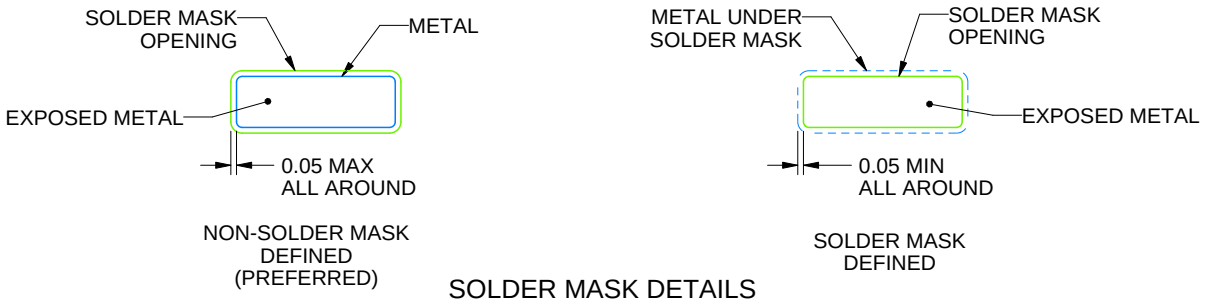
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

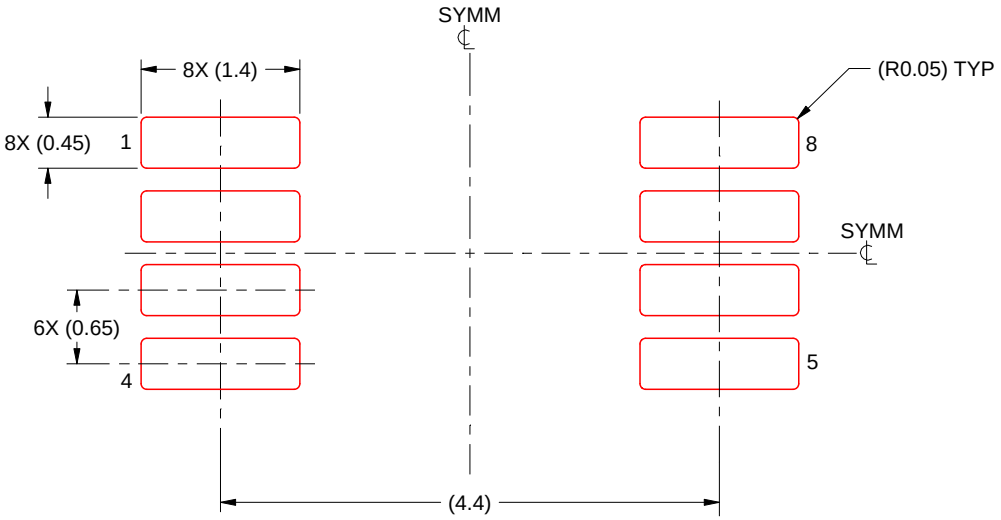


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

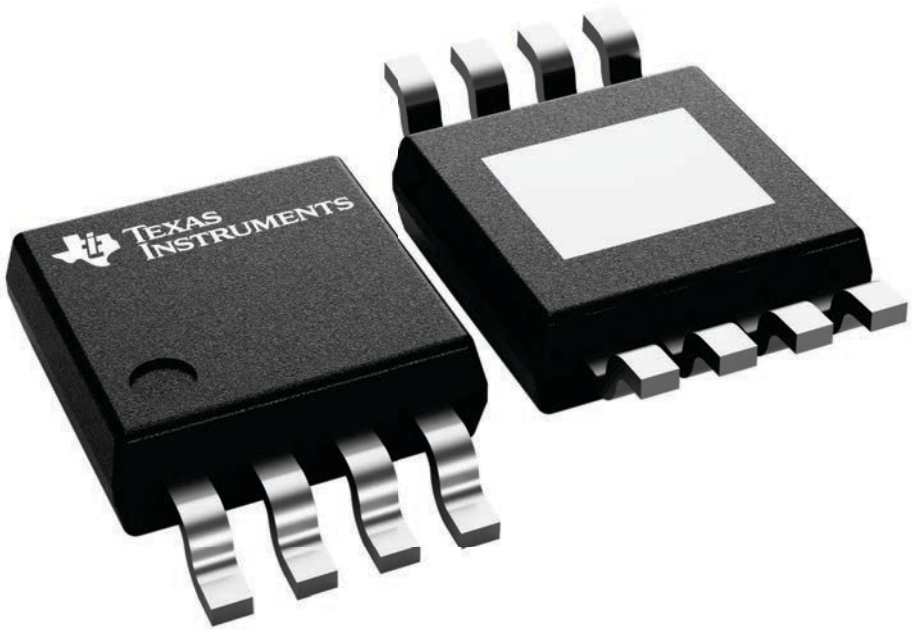
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



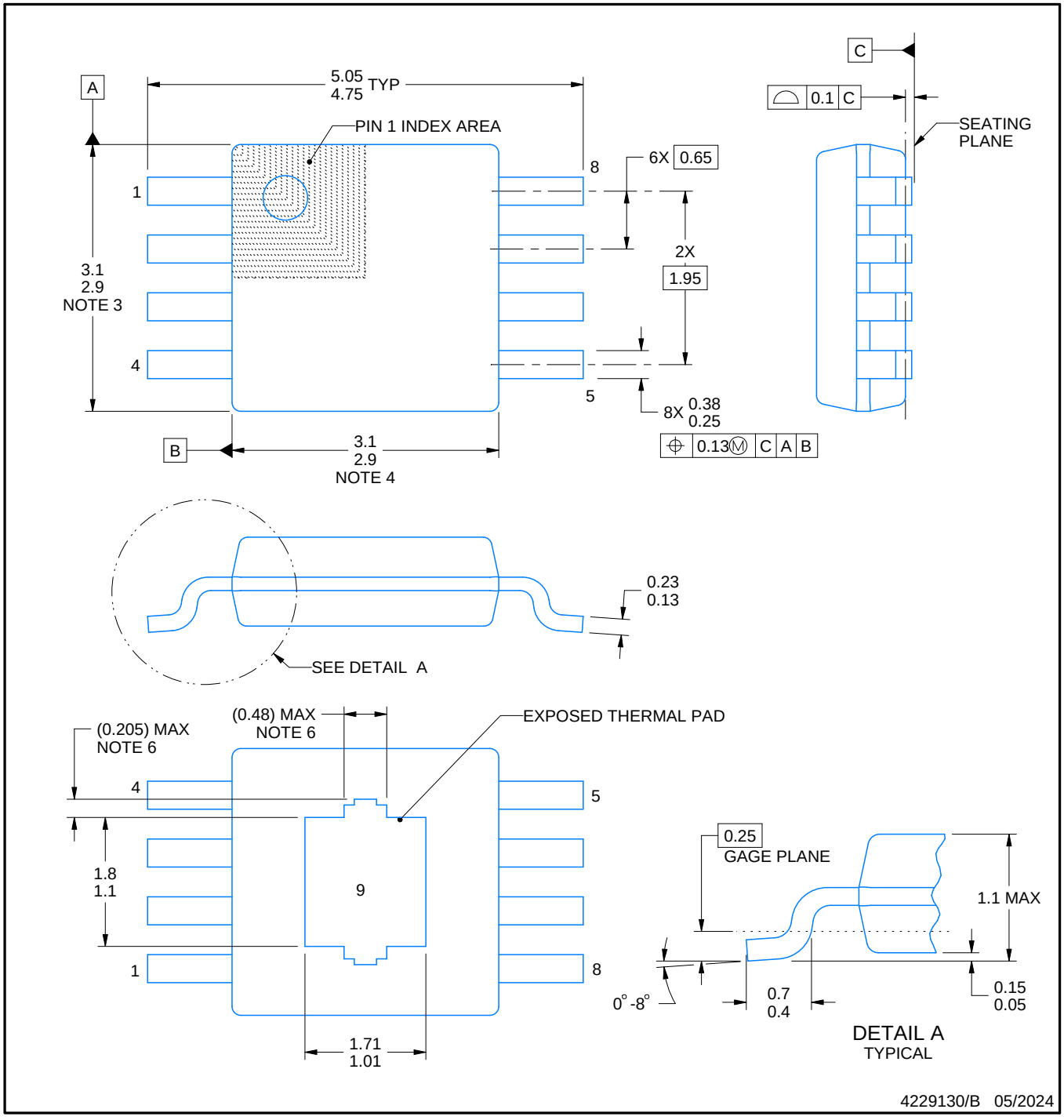
4225482/B

PACKAGE OUTLINE

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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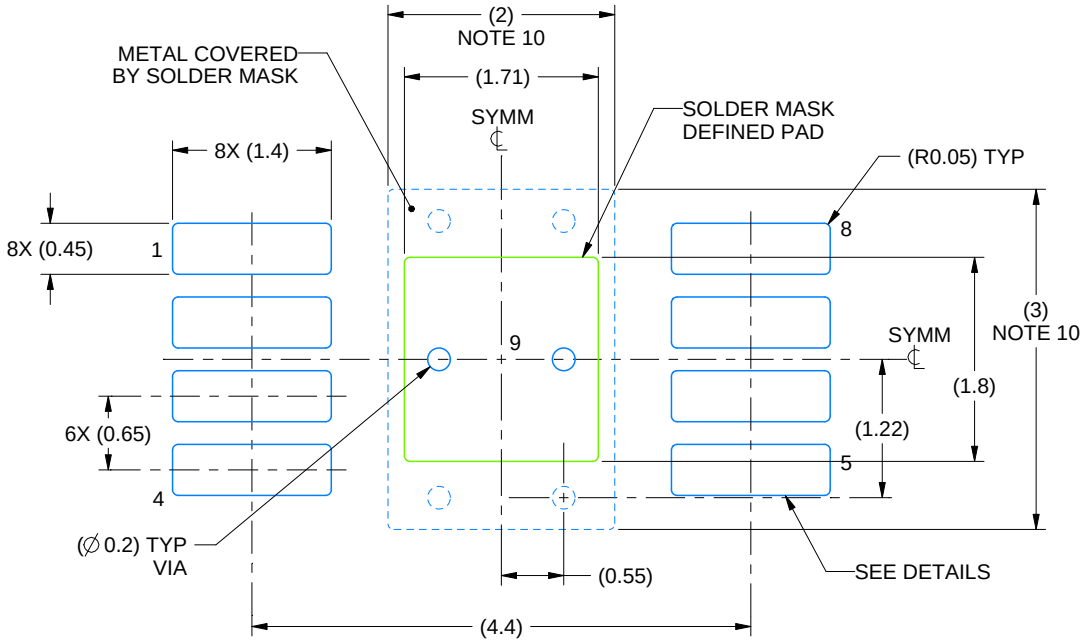
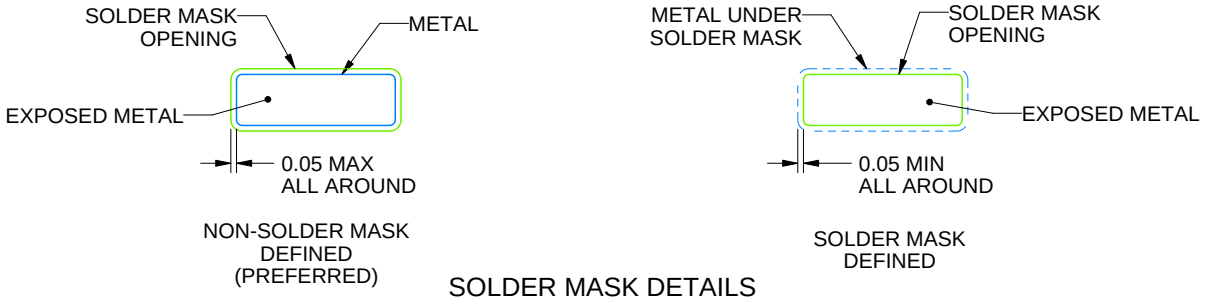
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

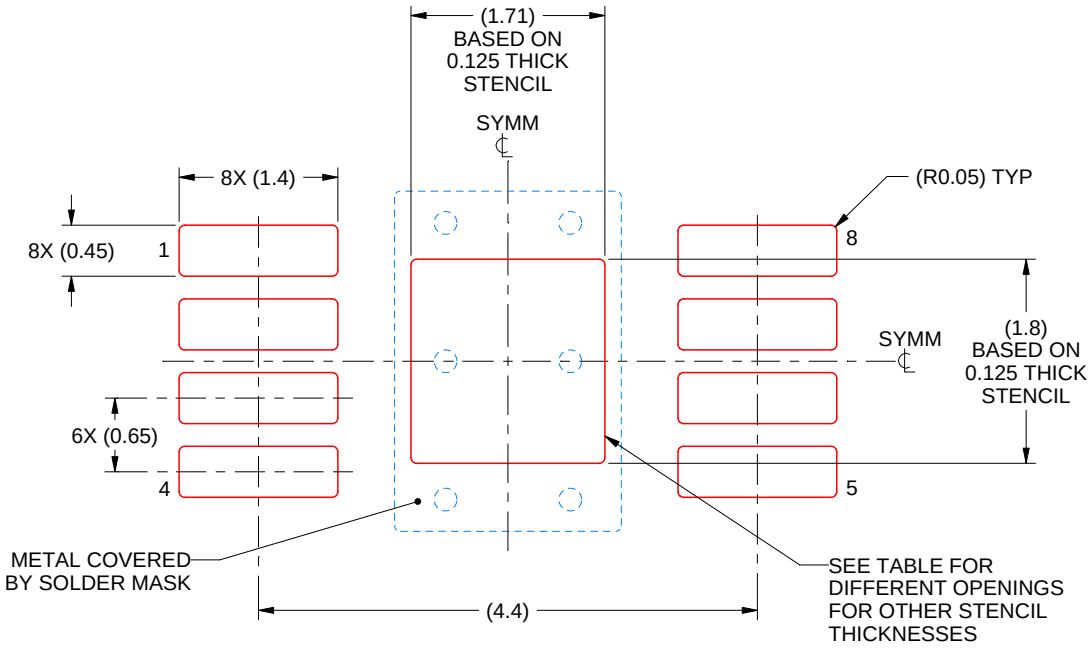


SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



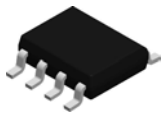
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

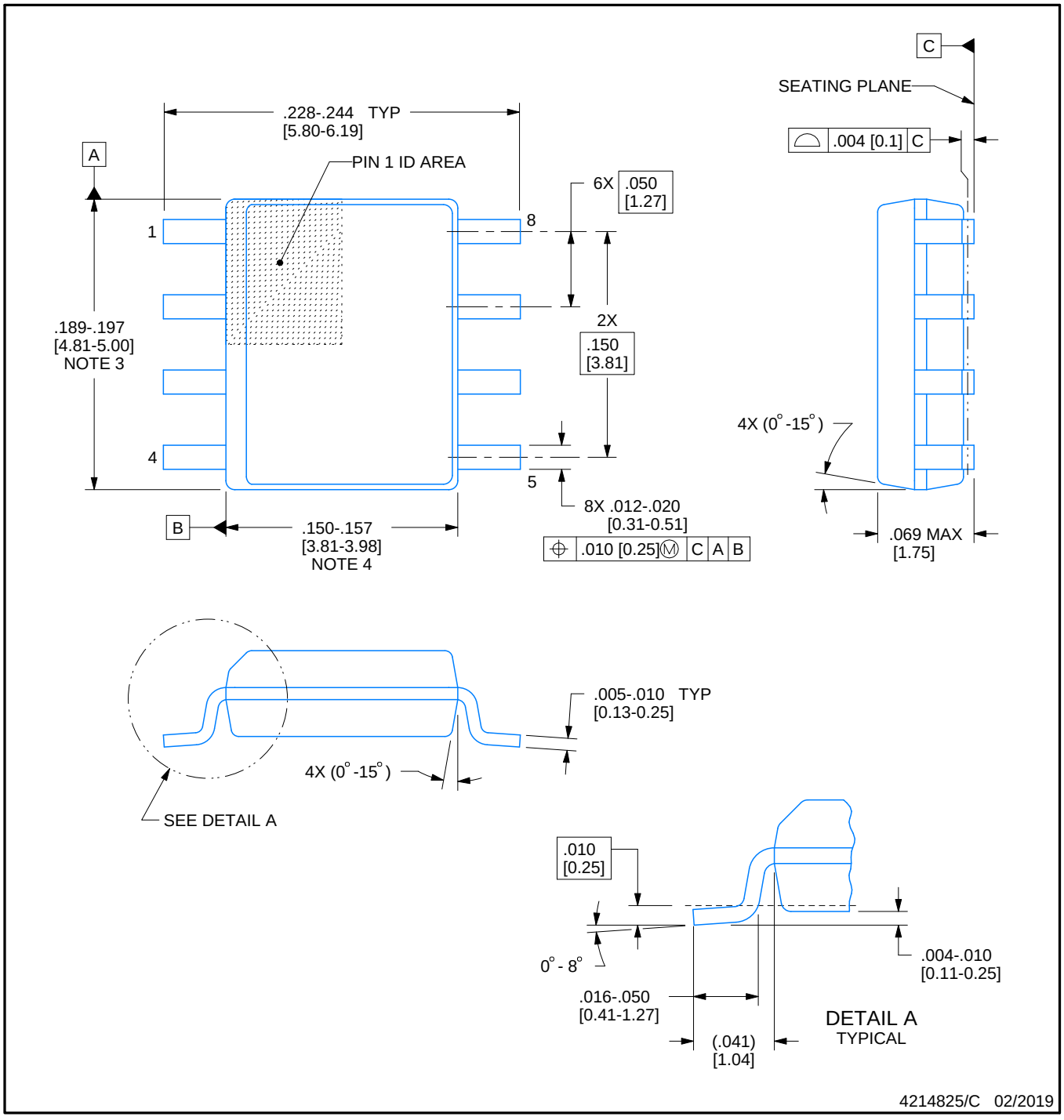


PACKAGE OUTLINE

D0008A

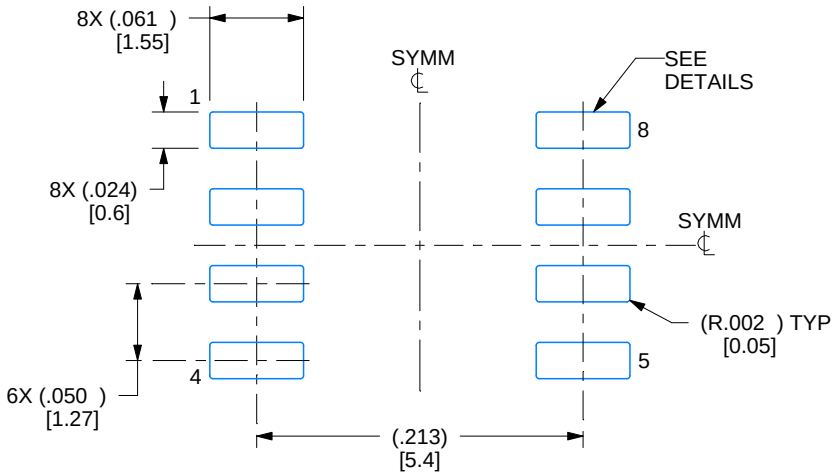
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

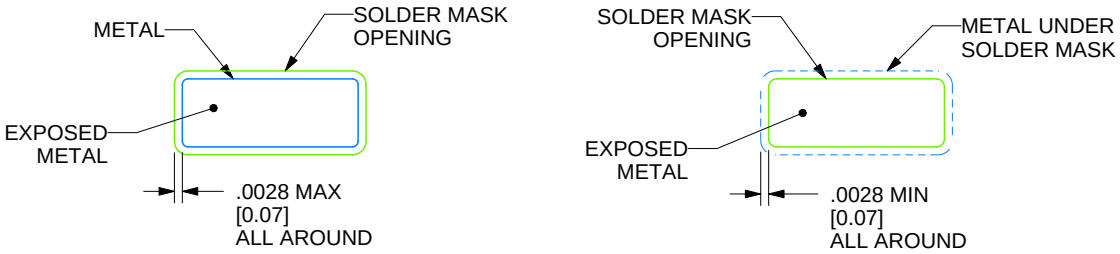


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

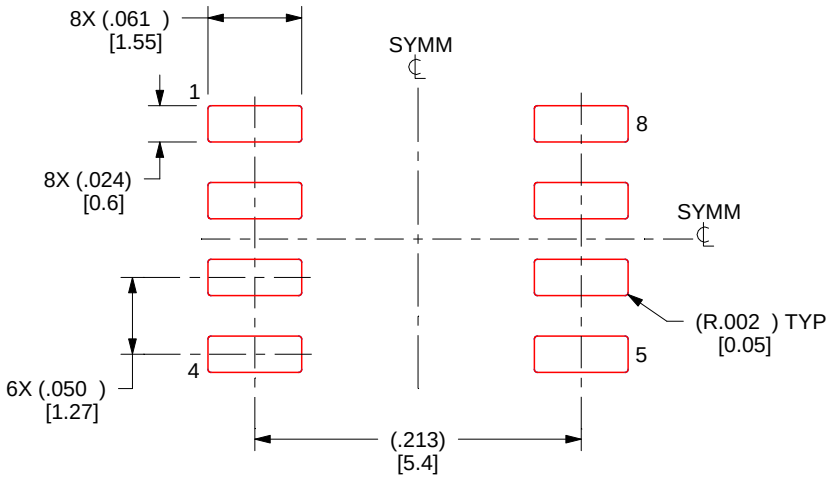
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月