LOW-DISTORTION, HIGH-SPEED, RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

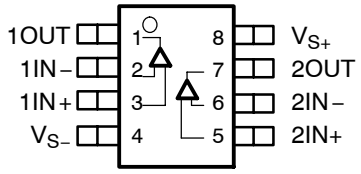
FEATURES

- **Rail-to-Rail Output Swing**
  - **V_O = –4.8/4.8 (R_L = 2 kΩ)**
- **High Speed**
  - **230 MHz Bandwidth (–3 dB, G= 1)**
  - **975 V/μs Slew Rate**
- **Ultra-Low Distortion**
  - **HD2 = –90 dBc (f = 5 MHz, R_L = 499Ω)**
  - **HD3 = –100 dBc (f = 5 MHz, R_L = 499Ω)**
- **High Output Drive, I_O = 100 mA (typ)**
- **Excellent Video Performance**
  - **40 MHz Bandwidth (0.1 dB, G = 2)**
  - **0.007% Differential Gain**
  - **0.007° Differential Phase**
- **Wide Range of Power Supplies**
  - **V_S = 3 V to 15 V**
- **Power-Down Mode (THS4225/6)**
- **Evaluation Module Available**

APPLICATIONS

- **Low-Voltage Analog-to-Digital Converter Preamplifier**
- **Active Filtering**
- **Video Applications**

THS4222
D, DGN, OR DGK PACKAGE
(TOP VIEW)



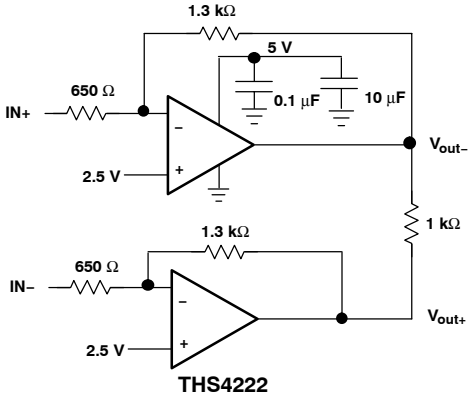
RELATED DEVICES

DEVICE	DESCRIPTION
THS4211	1 GHz, 800 V/μs, Vn = 7 nV/√Hz
THS4271	1.4 GHz, 900 V/μs, Vn = 3 nV/√Hz
OPA354	250 MHz, 150 V/μs, Vn = 6.5 nV/√Hz
OPA690	500 MHz, 1800 V/μs, Vn = 5.5 nV/√Hz

DESCRIPTION

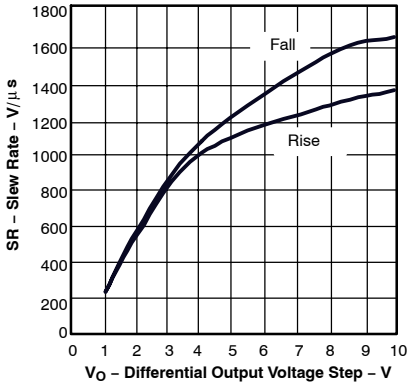
The THS4222 family is a set of rail-to-rail output single, and dual low-voltage, high-output swing, low-distortion high-speed amplifiers ideal for driving data converters, video switching or low distortion applications.This family of voltage feedback amplifiers can operate from a single 15-V power supply down to a single 3-V power supply while consuming only 14 mA of quiescent current per channel. In addition, the family offers excellent ac performance with 230-MHz bandwidth, 975-V/μs slew rate and harmonic distortion (THD) at –90 dBc at 5 MHz.

DIFFERENTIAL DRIVE CIRCUIT



THS4222

SLEW RATE
vs
DIFFERENTIAL OUTPUT VOLTAGE STEP



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNIT
Supply voltage, V_S			16.5 V
Input voltage, V_I			$\pm V_S$
Output current, I_O			100 mA
Differential input voltage, V_{ID}			4 V
Continuous power dissipation			See Dissipation Rating Table
Maximum junction temperature, T_J			150°C
Maximum junction temperature, continuous operation, long term reliability T_J (2)			125°C
Storage temperature range, T_{stg}			–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			300°C
ESD ratings:	HBM	THS4221/5	2500 V
		THS4222/6	3000 V
	CDM		1500 V
	MM	THS4221/5	150 V
		THS4222/6	200 V

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA}(1) (°C/W)	POWER RATING(2)	
			$T_A \le 25°C$	$T_A = 85°C$
DBV (5)	55	255.4	391 mW	156 mW
D (8)	38.3	97.5	1.02 W	410 mW
DGN (8) (3)	4.7	58.4	1.71 W	685 mW
DGK (8)	54.2	260	385 mW	154 mW
DGQ (10) (3)	4.7	58	1.72 W	690 mW

(1) This data was taken using the JEDEC standard High-K test PCB.

(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long term reliability.

(3) The THS422x may incorporate a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the PowerPAD thermally enhanced package.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, (V_{S+} and V_{S-})	Dual supply	±1.35	±7.5	V
	Single supply	2.7	15	
Input common-mode voltage range		V_{S-} + 1.1	V_{S+} – 1.1	V

THS4221 AND THS4225 SINGLE PACKAGE/ORDERING INFORMATION

PACKAGED DEVICES						
PLASTIC SMALL OUTLINE (D)	SOT-23(1)		PLASTIC MSOP(2) PowerPAD™		PLASTIC MSOP(2)	
	(DBV)	SYM	(DGN)	SYM	(DGK)	SYM
THS4221D	THS4221DBV	BFS	THS4221DGN	BFT	THS4221DGK	BHX
THS4225D	—	—	THS4225DGN	BFU	THS4225DGK	BFY

(1) All packages are available taped and reeled. The R suffix standard quantity is 3000. The T suffix standard quantity is 250 (e.g., THS4221DBVT).

(2) All packages are available taped and reeled. The R suffix standard quantity is 2500 (e.g., THS4221DGNR).

PowerPAD is a trademark of Texas Instruments.

THS4222 AND THS4226 DUAL PACKAGE/ORDERING INFORMATION

PACKAGED DEVICES						
PLASTIC SMALL OUTLINE (D)[1]	PLASTIC MSOP PowerPAD™[1]				PLASTIC MSOP™[1]	
	(DGN)	SYM	(DGQ)	SYM	(DGK)	SYM
THS4222D	THS4222DGN	BFO	—	—	THS4222DGK	BHW
—	—	—	THS4226DGQ	BFP	—	—

(1) All packages are available taped and reeled. The R suffix standard quantity is 2500 (e.g., THS4222DGNR).

ELECTRICAL CHARACTERISTICS

V_S = ±5 V, R_L = 499 Ω, and G = 1 unless otherwise noted

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small signal bandwidth	G = 1, P_{IN} = –7 dBm	230				MHz	Typ
	G = 2, P_{IN} = –13 dBm, R_f = 1.3 kΩ	100				MHz	Typ
	G = 5, P_{IN} = –21 dBm, R_f = 2 kΩ	25				MHz	Typ
	G = 10, P_{IN} = –27 dBm, R_f = 2 kΩ	12				MHz	Typ
0.1 dB flat bandwidth	G = 2, P_{IN} = –13 dBm, R_f = 1.3 kΩ	40				MHz	Typ
Gain bandwidth product	G > 10, f = 1 MHz, R_f = 2 kΩ	120				MHz	Typ
Full-power bandwidth	G = 1, V_O = ±2.5 V	65				MHz	Typ
Slew rate	G = –1, V_O = ±2.5 Vpp	990				V/µs	Min
	G = 1, V_O = ±2.5 Vpp	975				V/µs	Min
Settling time to 0.1%	G = –1, V_O = ±2 Vpp	25				ns	Typ
Settling time to 0.01%	G = –1, V_O = ±2 Vpp	52				ns	Typ
Harmonic distortion	G = 1, V_O = 2 V_{PP}, f = 5 MHz						
Second harmonic distortion	R_L = 499 Ω	–90				dBc	Typ
	R_L = 150 Ω	–92				dBc	Typ
Third harmonic distortion	R_L = 499 Ω	–100				dBc	Typ
	R_L = 150 Ω	–96				dBc	Typ
Differential gain (NTSC, PAL)	G = 2, R = 150 Ω	0.007				%	Typ
Differential phase (NTSC, PAL)	G = 2, R = 150 Ω	0.007				°	Typ
Input voltage noise	f = 1 MHz	13				nV/√Hz	Typ
Input current noise	f = 1 MHz	0.8				pA/√Hz	Typ
Crosstalk (dual only)	f = 5 MHz Ch-to-Ch	–90				dB	Typ
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})	V_O = ±2 V	100	80	75	75	dB	Min
Input offset voltage	V_{CM} = 0 V	3	10	16	16	mV	Max
Average offset voltage drift	V_{CM} = 0 V			±20	±20	µV/°C	Typ
Input bias current	V_{CM} = 0 V	0.9	3	5	5	µA	Max
Average offset voltage drift	V_{CM} = 0 V			±10	±10	µV/°C	Typ
Input offset current	V_{CM} = 0 V	100	500	700	700	nA	Max
Average offset current drift	V_{CM} = 0 V			±10	±10	nA/°C	Typ
INPUT CHARACTERISTICS							
Common-mode input range		–4 / 4	–3.9 / 3.9			V	Min
Common-mode rejection ratio	V_{CM} = ±2 V	94	74	69	69	dB	Min
Input resistance		33				MΩ	Typ
Input capacitance	Common-mode / differential	1 / 0.5				pF	Max

ELECTRICAL CHARACTERISTICS

V_S = ±5 V, R_L = 499 Ω, and G = 1 unless otherwise noted

PARAMETER	TEST CONDITIONS		TYP	OVER TEMPERATURE				
			25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX
OUTPUT CHARACTERISTICS								
Output voltage swing	R_L = 499 Ω		–4.7 / 4.7	–4.5 / 4.5	–4.4 / 4.4	–4.4 / 4.4	V	Min
	R_L = 2 kΩ		–4.8 / 4.8				V	Min
Output current (sourcing)	R_L = 10 Ω		100	92	88	88	mA	Min
Output current (sinking)	R_L = 10 Ω		–100	–92	–88	–88	mA	Min
Output impedance	f = 1 MHz		0.02				Ω	Typ
POWER SUPPLY								
Specified operating voltage			±5	±7.5	±7.5	±7.5	V	Max
Maximum quiescent current	Per channel		14	18	20	22	mA	Max
Power supply rejection (±PSRR)			75	62	60	60	dB	Min
POWER-DOWN CHARACTERISTICS								
Maximum power-down current	$\overline{PD}$ ≤ REF +1.0 V, REF = 0 V, Per channel		700	900	1000	1000	µA	Max
Power-down voltage level(1)	REF = 0 V, or V_{S-}	Enable		REF+1.8			V	Min
		Power down		REF+1			V	Max
	REF = V_{S+} or floating	Enable		REF–1			V	Min
		Power down		REF–1.5			V	Max
Turnon time delay	50% of final value		200				ns	Typ
Turnoff time delay	50% of final value		500				ns	Typ
Input impedance			58				Ω	Typ
Isolation	f = 5 MHz		80				dB	Typ

(1) For detail information on the power-down circuit, refer to the powerdown section in the application information of this data sheet.

ELECTRICAL CHARACTERISTICS

V_S = 5 V, R_L = 499 Ω, and G = 1 unless otherwise noted

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small signal bandwidth	G = 1, P_{IN} = –7 dBm	200				MHz	Typ
	G = 2, P_{IN} = –13 dBm, R_f = 1.3 kΩ	100				MHz	Typ
	G = 5, P_{IN} = –21 dBm, R_f = 2 kΩ	25				MHz	Typ
	G = 10, P_{IN} = –27 dBm, R_f = 2 kΩ	12				MHz	Typ
0.1 dB flat bandwidth	G = 2, P_{IN} = –13 dBm, R_f = 1.3 kΩ	50				MHz	Typ
Gain bandwidth product	G > 10, f = 1 MHz, R_f = 2 kΩ	120				MHz	Typ
Full-power bandwidth	G = 1, V_O = ±2 V	40				MHz	Typ
Slew rate	G = –1, V_O = ±2 Vpp	500				V/µs	Min
	G = 1, V_O = ±2 Vpp	550				V/µs	Min
Settling time to 0.1%	G = –1, V_O = ±1 Vpp	27				ns	Typ
Settling time to 0.01%	G = –1, V_O = ±1 Vpp	48				ns	Typ
Harmonic distortion	G = 1, V_O = 2 V_{PP}, f = 5 MHz						
Second harmonic distortion	R_L = 499 Ω	–90				dBc	Typ
	R_L = 150 Ω	–93				dBc	Typ
Third harmonic distortion	R_L = 499 Ω	–89				dBc	Typ
	R_L = 150 Ω	–91				dBc	Typ
Differential gain (NTSC, PAL)	G = 2, R = 150 Ω	0.014				%	Typ
Differential phase (NTSC, PAL)	G = 2, R = 150 Ω	0.011				°	Typ
Input voltage noise	f = 1 MHz	13				nV/√Hz	Typ
Input current noise	f = 1 MHz	0.8				pA/√Hz	Typ
Crosstalk (dual only)	f = 5 MHz Ch-to-Ch	–90				dB	Typ
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})	V_O = 1.5 V to 3.5 V	100	80	75	75	dB	Min
Input offset voltage	V_{CM} = 2.5 V	3	10	16	16	mV	Max
Average offset voltage drift	V_{CM} = 2.5 V			±20	±20	µV/°C	Typ
Input bias current	V_{CM} = 2.5 V	0.9	3	5	5	µA	Max
Average offset voltage drift	V_{CM} = 2.5 V			±10	±10	µV/°C	Typ
Input offset current	V_{CM} = 2.5 V	100	500	700	700	nA	Max
Average offset current drift	V_{CM} = 2.5 V			±10	±10	nA/°C	Typ
INPUT CHARACTERISTICS							
Common-mode input range		1 / 4	1.1 / 3.9			V	Min
Common-mode rejection ratio	V_{CM} = 1.5 V to 3.5 V	96	74	69	69	dB	Min
Input resistance		33				MΩ	Typ
Input capacitance	Common-mode / differential	1 / 0.5				pF	Max
OUTPUT CHARACTERISTICS							
Output voltage swing	R_L = 499 Ω	0.2 / 4.8	0.3 / 4.7	0.4 / 4.6	0.4 / 4.6	V	Min
	R_L = 2 kΩ	0.1 / 4.9				V	Min
Output current (sourcing)	R_L = 10 Ω	95	85	80	80	mA	Min
Output current (sinking)	R_L = 10 Ω	–95	–85	–80	–80	mA	Min
Output impedance	f = 1 MHz	0.02				Ω	Typ

ELECTRICAL CHARACTERISTICS (continued)

V_S = 5 V, R_L = 499 Ω, and G = 1 unless otherwise noted

PARAMETER	TEST CONDITIONS		TYP	OVER TEMPERATURE				
			25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX
POWER SUPPLY								
Specified operating voltage			5	15	15	15	V	Max
Maximum quiescent current	Per channel		12	15	17	19	mA	Max
Power supply rejection (±PSRR)			70	62	60	60	dB	Min
POWER-DOWN CHARACTERISTICS								
Maximum power-down current	$\overline{PD} \le$ REF +1.0 V, REF = 0 V, Per channel		500	750	900	900	µA	Max
Power-down voltage level(1)	REF = 0 V, or V_{S-}	Enable		REF+1.8			V	Min
		Power down		REF+1			V	Max
	REF = V_{S+} or floating	Enable		REF–1			V	Min
		Power down		REF–1.5			V	Max
Turnon time delay	50% of final value		200				ns	Typ
Turnoff time delay	50% of final value		500				ns	Typ
Input impedance			58				Ω	Typ
Isolation	f = 5 MHz		80				dB	Typ

(1) For detail information on the power-down circuit, refer to the powerdown section in the application information of this data sheet.

ELECTRICAL CHARACTERISTICS

V_S = 3.3 V, R_L = 499 Ω, and G = 1 unless otherwise noted

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small signal bandwidth	G = 1, P_{IN} = –7 dBm	200				MHz	Typ
	G = 2, P_{IN} = –13 dBm, R_f = 1 kΩ	100				MHz	Typ
	G = 5, P_{IN} = –21 dBm, R_f = 2 kΩ	15				MHz	Typ
	G = 10, P_{IN} = –27 dBm, R_f = 2 kΩ	12				MHz	Typ
0.1 dB flat bandwidth	G = 2, P_{IN} = –13 dBm, R_f = 1 kΩ	50				MHz	Typ
Gain bandwidth product	G > 10, f = 1 MHz, R_f = 1.5 kΩ	120				MHz	Typ
Full-power bandwidth	G = 1, V_O = 1.3 V to 2 V	50				MHz	Typ
Slew rate	G = –1, V_O = 1.3 V to 2 V	120				V/µs	Min
	G = 1, V_O = 1.3 V to 2V	250				V/µs	Min
Harmonic distortion	G = 2, V_O = 1 V_{PP}, f = 5 MHz						
Second harmonic distortion	R_L = 499 Ω	–80				dBc	Typ
	R_L = 150 Ω	–79				dBc	Typ
Third harmonic distortion	R_L = 499 Ω	–91				dBc	Typ
	R_L = 150 Ω	–92				dBc	Typ
Input voltage noise	f = 1 MHz	13				nV/√Hz	Typ
Input current noise	f = 1 MHz	0.8				pA/√Hz	Typ
Crosstalk (dual only)	f = 5 MHz Ch-to-Ch	–90				dB	Typ
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})	V_O = 1.35 V to 1.95 V	98	80	75	75	dB	Min
Input offset voltage	V_{CM} = 1.65 V	3	10	16	16	mV	Max
Average offset voltage drift	V_{CM} = 1.65 V			±20	±20	µV/°C	Typ
Input bias current	V_{CM} = 1.65 V	0.9	3	5	5	µA	Max
Average offset voltage drift	V_{CM} = 1.65 V			±10	±10	µV/°C	Typ
Input offset current	V_{CM} = 1.65 V	100	500	700	700	nA	Max
Average offset current drift	V_{CM} = 1.65 V			±10	±10	nA/°C	Typ
INPUT CHARACTERISTICS							
Common-mode input range		1 / 2.3	1.1/2.2			V	Min
Common-mode rejection ratio	V_{CM} = 1.35 V to 1.95 V	92	74	69	69	dB	Min
Input resistance		33				MΩ	Typ
Input capacitance	Common-mode / differential	1 / 0.5				pF	Max
OUTPUT CHARACTERISTICS							
Output voltage swing	R_L = 499 Ω	0.15/3.15	0.3/3.0	0.35/2.95	0.35/2.95	V	Min
Output voltage swing	R_L = 2 kΩ	0.1 / 3.2				V	Min
Output current (sourcing)	R_L = 20 Ω	50	45	40	40	mA	Min
Output current (sinking)	R_L = 20 Ω	–50	–45	–40	–40	mA	Min
Output impedance	f = 1 MHz	0.02				Ω	Typ

ELECTRICAL CHARACTERISTICS (continued)

V_S = 3.3 V, R_L = 499 Ω, and G = 1 unless otherwise noted

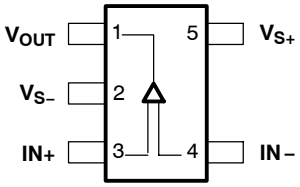
PARAMETER	TEST CONDITIONS		TYP	OVER TEMPERATURE				
			25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX
POWER SUPPLY								
Specified operating voltage			3.3	15	15	15	V	Max
Maximum quiescent current	Per channel		11	13	16	17	mA	Max
Power supply rejection (±PSRR)			65	60	55	55	dB	Min
POWER-DOWN CHARACTERISTICS								
Maximum power-down current	$\overline{PD} \le$ REF +1.0 V, REF = 0 V, Per channel		500	700	800	800	µA	Max
Power-down voltage level(1)	REF = 0 V, or V_{S-}	Enable		REF+1.8			V	Min
		Power down		REF+1			V	Max
	REF = V_{S+} or floating	Enable		REF–1			V	Min
		Power down		REF–1.5			V	Max
Turnon time delay	50% of final value		200				ns	Typ
Turnoff time delay	50% of final value		500				ns	Typ
Input impedance			58				Ω	Typ
Isolation	f = 5 MHz		80				dB	Typ

(1) For detail information on the power-down circuit, refer to the powerdown section in the application information of this data sheet.

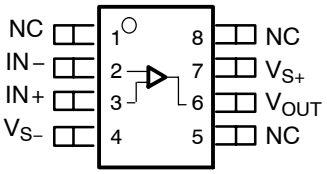
PIN ASSIGNMENTS

NON-POWER DOWN PACKAGE DEVICES

THS4221
DBV PACKAGE
(TOP VIEW)

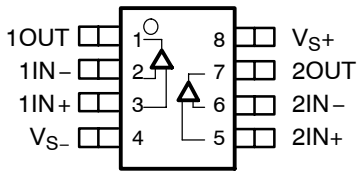


THS4221
D, DGN, OR DGK PACKAGE
(TOP VIEW)



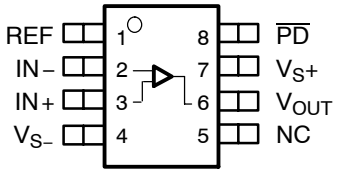
NC – No internal connection

THS4222
D, DGN, OR DGK PACKAGE
(TOP VIEW)



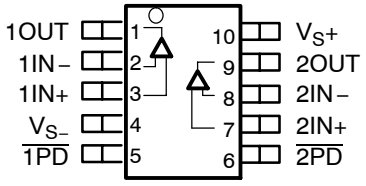
POWER-DOWN PACKAGE DEVICES

THS4225
D, DGN, OR DGK PACKAGE
(TOP VIEW)



NC – No internal connection

THS4226
DGQ PACKAGE
(TOP VIEW)



TYPICAL CHARACTERISTICS

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Input offset voltage vs Case temperature	23
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Power-down quiescent current vs Supply voltage	26
Output impedance in power down vs Frequency	27
Crosstalk vs Frequency	28

SMALL SIGNAL FREQUENCY RESPONSE

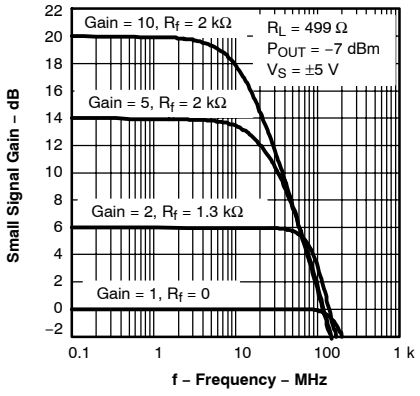


Figure 1

SLEW RATE vs OUTPUT VOLTAGE STEP

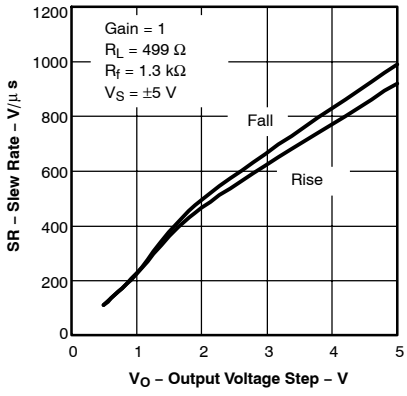


Figure 2

SLEW RATE vs OUTPUT VOLTAGE STEP

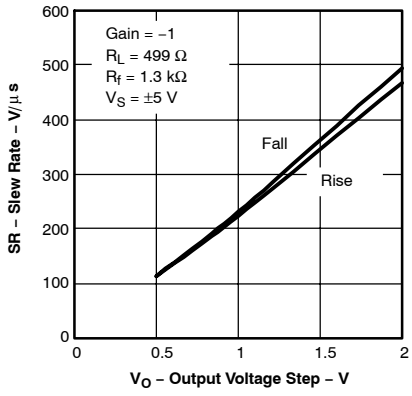


Figure 3

HARMONIC DISTORTION vs FREQUENCY

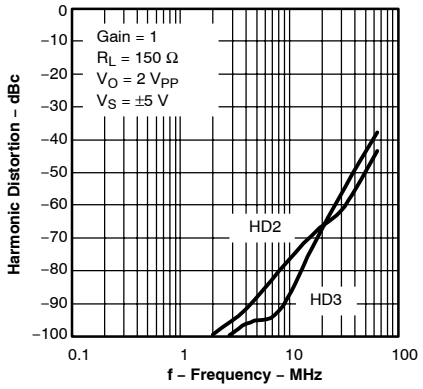


Figure 4

HARMONIC DISTORTION vs FREQUENCY

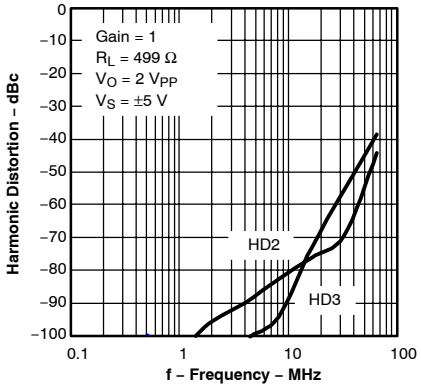


Figure 5

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

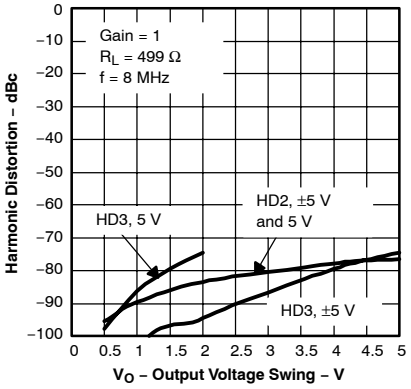


Figure 6

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

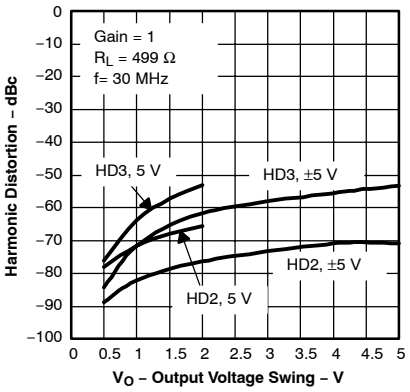


Figure 7

HARMONIC DISTORTION vs FREQUENCY

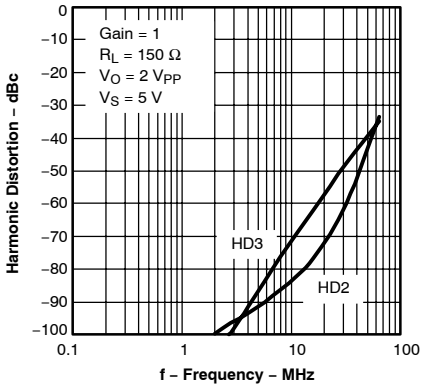


Figure 8

HARMONIC DISTORTION vs FREQUENCY

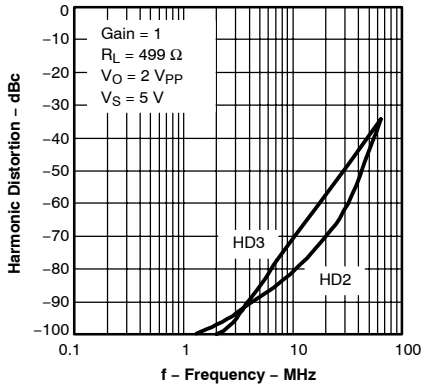


Figure 9

VOLTAGE AND CURRENT NOISE vs FREQUENCY

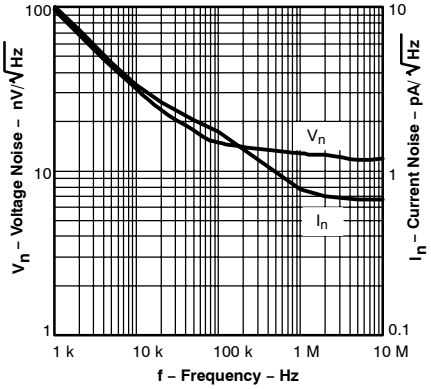


Figure 10

DIFFERENTIAL GAIN vs NUMBER OF LOADS

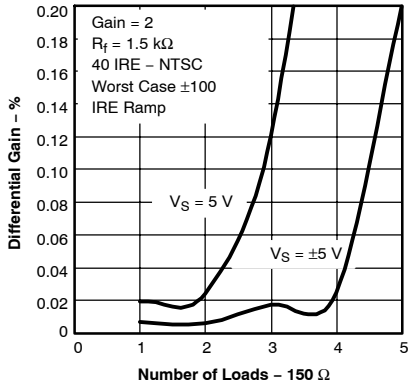


Figure 11

DIFFERENTIAL PHASE vs NUMBER OF LOADS

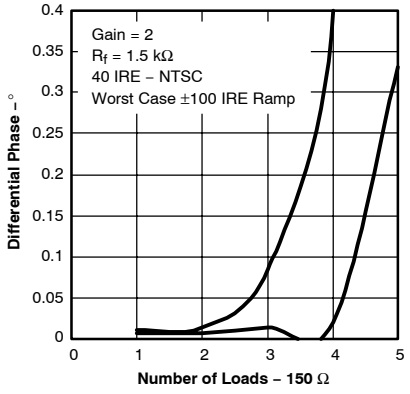


Figure 12

DIFFERENTIAL GAIN vs NUMBER OF LOADS

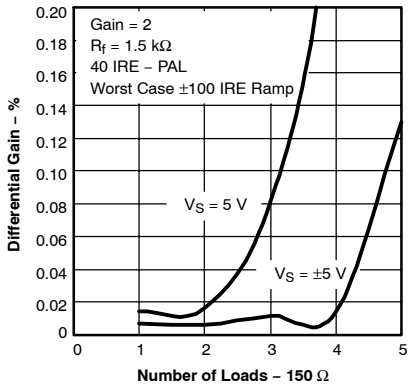


Figure 13

DIFFERENTIAL PHASE vs NUMBER OF LOADS

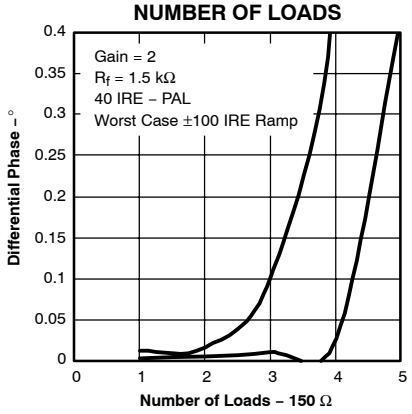


Figure 14

QUIESCENT CURRENT vs SUPPLY VOLTAGE

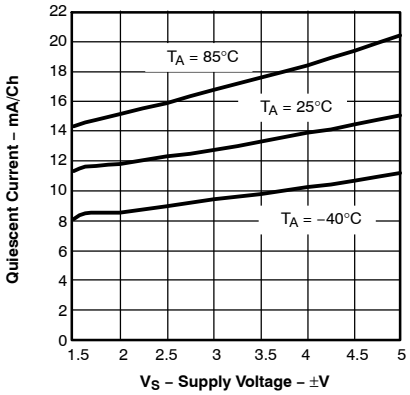


Figure 15

OUTPUT VOLTAGE vs LOAD RESISTANCE

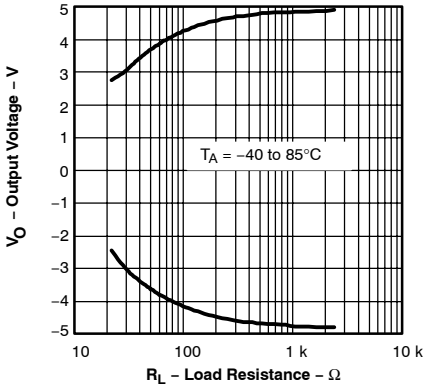


Figure 16

OPEN-LOOP GAIN AND FHASE vs FREQUENCY

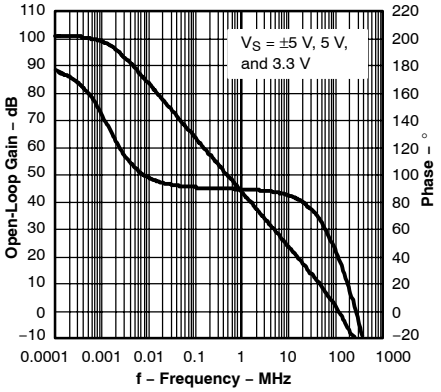


Figure 17

OPEN-LOOP GAIN vs SUPPLY VOLTAGE

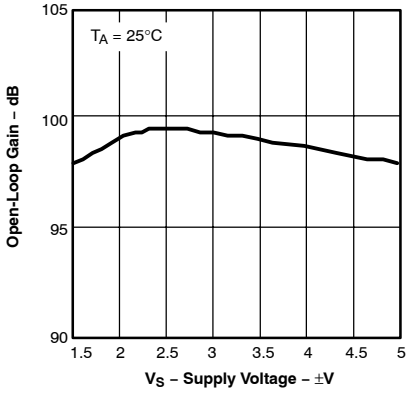


Figure 18

REJECTION RATIO vs FREQUENCY

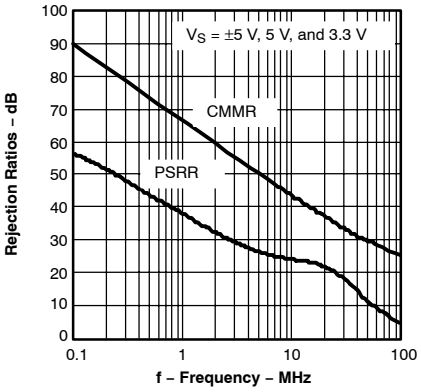


Figure 19

REJECTION RATIO vs CASE TEMPERATURE

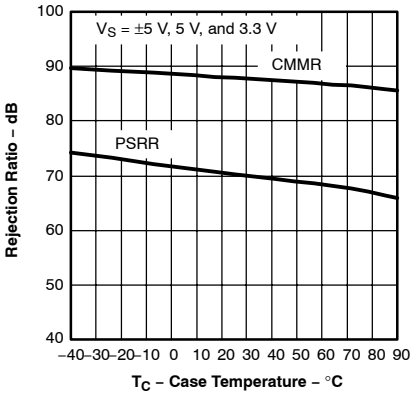


Figure 20

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

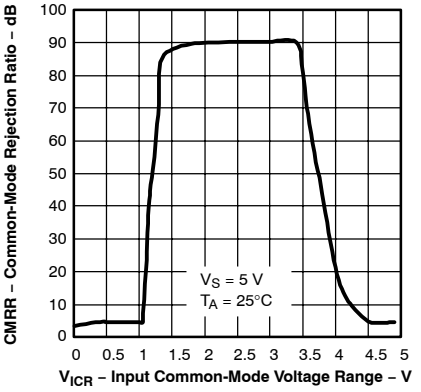


Figure 21

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

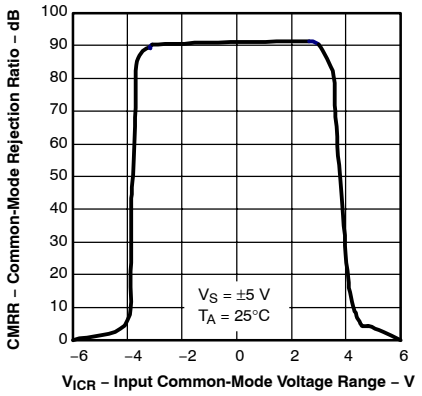


Figure 22

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

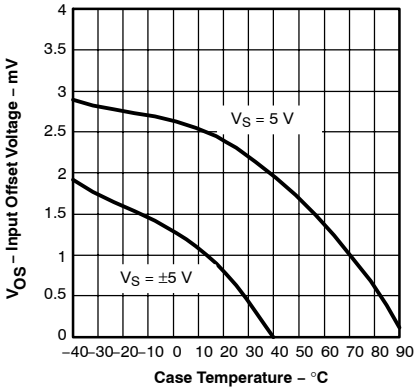


Figure 23

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

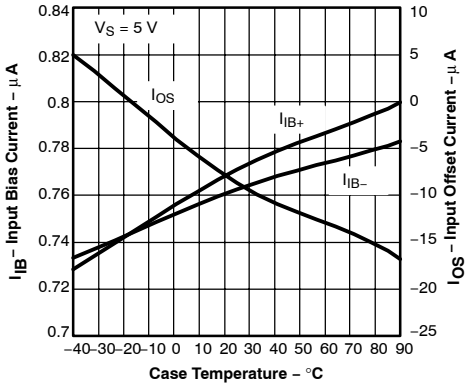


Figure 24

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

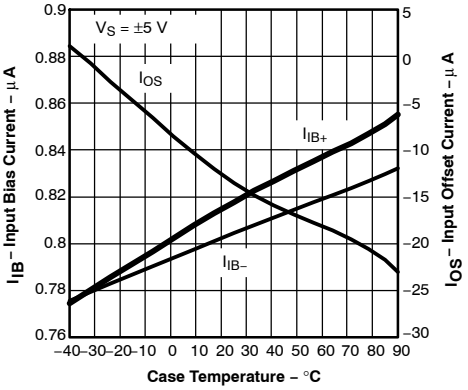


Figure 25

POWER-DOWN QUIESCENT CURRENT vs SUPPLY VOLTAGE

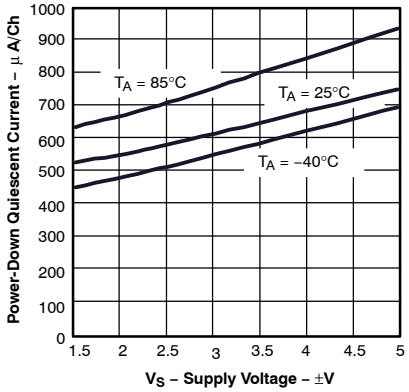


Figure 26

OUTPUT IMPEDANCE IN POWER DOWN vs FREQUENCY

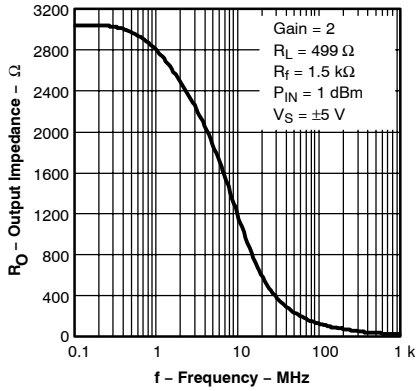


Figure 27

CROSSTALK vs FREQUENCY

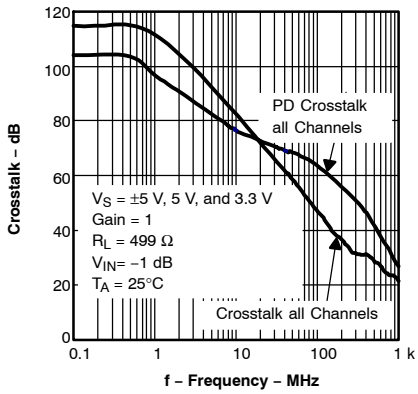


Figure 28

APPLICATION INFORMATION

HIGH-SPEED OPERATIONAL AMPLIFIERS

The THS4222 family of operational amplifiers is a family of single and dual, rail-to-rail output voltage feedback amplifiers. The THS4222 family combines both a high slew rate and a rail-to-rail output stage.

The THS4225 and THS4226 provides a power-down mode, providing the ability to save power when the amplifier is inactive. A reference pin is provided to allow the user the flexibility to control the threshold levels of the power-down control pin.

Applications Section Contents

- Wideband, Noninverting Operation
- Wideband, Inverting Gain Operation
- Single Supply Operation
- Saving Power With Power-Down Functionality and Setting Threshold Levels With the Reference Pin
- Power Supply Decoupling Techniques and Recommendations
- Driving an ADC With the THS4222
- Active Filtering With the THS4222
- An Abbreviated Analysis of Noise in Amplifiers
- Driving Capacitive Loads
- Printed Circuit Board Layout Techniques for Optimal Performance
- Power Dissipation and Thermal Considerations
- Evaluation Fixtures, Spice Models, and Applications Support
- Additional Reference Material
- Mechanical Package Drawings

WIDEBAND, NONINVERTING OPERATION

The THS4222 is a family of unity gain stable rail-to-rail output voltage feedback operational amplifiers, with and without power-down capability, designed to operate from a single 3-V to 15-V power supply.

Figure 29 is the noninverting gain configuration of 2 V/V used to demonstrate the typical performance curves.

Voltage feedback amplifiers, unlike current feedback designs, can use a wide range of resistors values to set their gain with minimal impact on their stability and frequency response. Larger-valued resistors decrease the loading effect of the feedback network on the output of the amplifier, but this enhancement comes at the expense of additional noise and potentially lower bandwidth. Feedback resistor values between 1 kΩ and 2 kΩ are recommended for most situations.

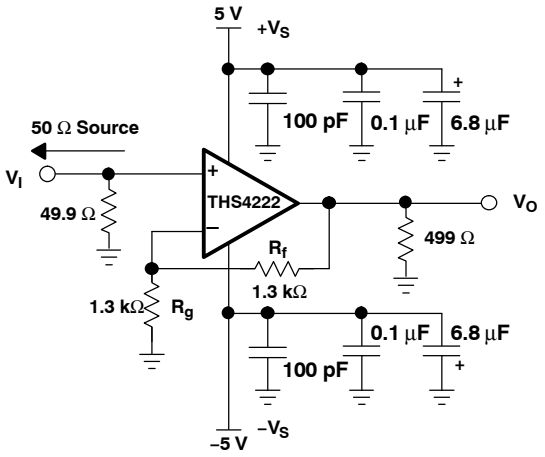


Figure 29. Wideband, Noninverting Gain Configuration

WIDEBAND, INVERTING OPERATION

Since the THS4222 family are general-purpose, wideband voltage-feedback amplifiers, several familiar operational amplifier applications circuits are available to the designer. Figure 30 shows a typical inverting configuration where the input and output impedances and noise gain from Figure 29 are retained in an inverting circuit configuration. Inverting operation is one of the more common requirements and offers several performance benefits. The inverting configuration shows improved slew rates and distortion due to the pseudo-static voltage maintained on the inverting input.

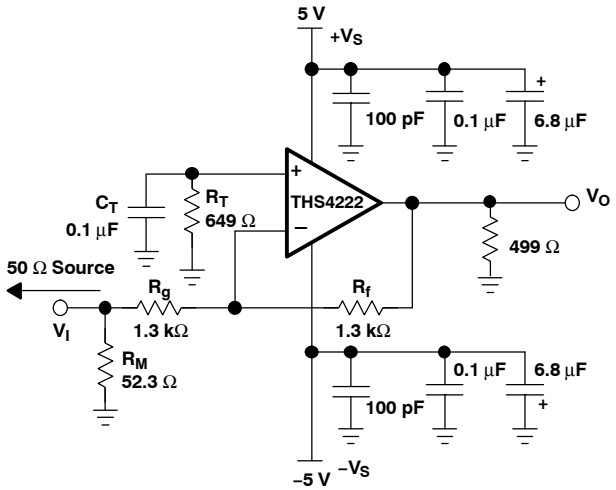


Figure 30. Wideband, Inverting Gain Configuration

In the inverting configuration, some key design considerations must be noted. One is that the gain resistor (R_g) becomes part of the signal channel input impedance. If the input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace, or other transmission line conductors), R_g may be set equal to the required termination value and R_f adjusted to give the desired gain. However, care must be taken when dealing with low inverting gains, as the resultant feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting R_g to 49.9 Ω for input matching eliminates the need for R_M but requires a 100-Ω feedback resistor. This has an advantage of the noise gain becoming equal to 2 for a 50-Ω source impedance—the same as the noninverting circuit in Figure 29. However, the amplifier output now sees the 100-Ω feedback resistor in parallel with the external load. To eliminate this excessive loading, it is preferable to increase both R_g and R_f, values, as shown in Figure 30, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_g and R_M.

The last major consideration to discuss in inverting amplifier design is setting the bias current cancellation resistor on the noninverting input. If the resistance is set equal to the total dc resistance looking out of the inverting terminal, the output dc error, due to the input bias currents, is reduced to (input offset current) multiplied by R_f in Figure 30, the dc source impedance looking out of the inverting terminal is 1.3 kΩ || (1.3 kΩ + 25.6 Ω) = 649 Ω. To reduce the additional high-frequency noise introduced by the resistor at the noninverting input, and power-supply feedback, R_T is bypassed with a capacitor to ground.

SINGLE SUPPLY OPERATION

The THS4222 is designed to operate from a single 3-V to 15-V power supply. When operating from a single power supply, care must be taken to ensure the input signal and amplifier are biased appropriately to allow for the maximum output voltage swing. The circuits shown in Figure 31 demonstrate methods to configure an amplifier in a manner conducive for single supply operation.

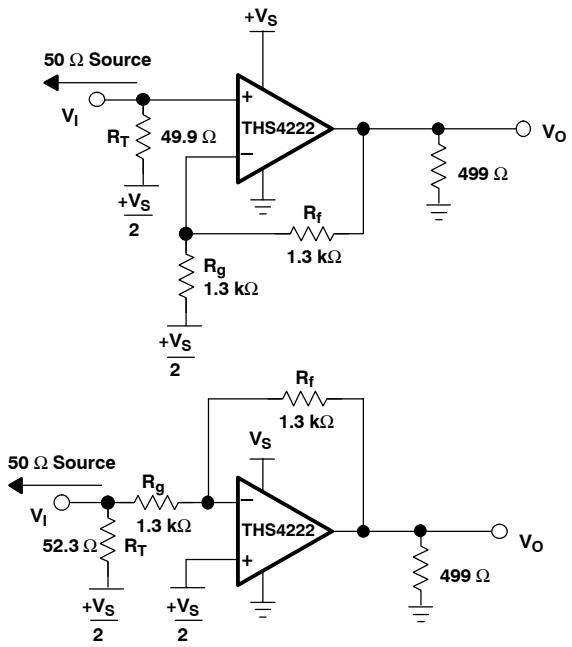


Figure 31. DC-Coupled Single Supply Operation

Saving Power With Power-Down Functionality and Setting Threshold Levels With the Reference Pin

The THS4225 and THS4226 feature a power-down pin ($\overline{PD}$) which lowers the quiescent current from 14 mA/ch down to 700 μA/ch, ideal for reducing system power.

The power-down pin of the amplifiers defaults to the positive supply voltage in the absence of an applied voltage, putting the amplifier in the *power-on* mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be driven towards the negative rail. The threshold voltages for power-on and power-down are relative to the supply rails and given in the specification tables. Above the *Enable Threshold Voltage*, the device is on. Below the *Disable Threshold Voltage*, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high-impedance output. In other words, the power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach 50% of the nominal quiescent current. The time delays are on the order of microseconds because the amplifier moves in and out of the linear mode of operation in these transitions.

Power-Down Reference Pin Operation

In addition to the power-down pin, the THS4225 features a reference pin (REF) which allows the user to control the enable or disable power-down voltage levels applied to the $\overline{PD}$ pin. Operation of the reference pin as it relates to the power-down pin is described below.

In most split-supply applications, the reference pin is connected to ground. In some cases, the user may want to connect it to the negative or positive supply rail. In either case, the user needs to be aware of the voltage level thresholds that apply to the power-down pin. The tables below show examples and illustrate the relationship between the reference voltage and the power-down thresholds.

POWER-DOWN THRESHOLD VOLTAGE LEVELS (REF ≤ Midrail)			
SUPPLY VOLTAGE (V)	REFERENCE PIN VOLTAGE (V)	ENABLE LEVEL (V)	DISABLE LEVEL (V)
±5	GND	≥ 1.8	≤ 1
	–2.5	≥ –0.7	≤ –1.5
	–5	≥ –3.2	≤ –4
5	GND	≥ 1.8	≤ 1
	1	≥ 2.8	≤ 2
	2.5	≥ 4.3	≤ 3.5
3.3	GND	≥ 1.8	≤ 1

In the above table, the threshold levels are derived by the following equations:

REF + 1.8 V for enable
REF + 1 V for disable

Note that in order to maintain these threshold levels, the reference pin can be any voltage between Vs– or GND up to Vs/2 (mid rail).

For 3.3-V operation, the reference pin must be connected to the most negative rail (for single supply this is GND).

POWER-DOWN THRESHOLD VOLTAGE LEVELS (REF > Midrail)			
SUPPLY VOLTAGE (V)	REFERENCE PIN VOLTAGE (V)	ENABLE LEVEL (V)	DISABLE LEVEL (V)
±5	Floating or 5	≥ 4	≤ 3.5
	2.5	≥ 1.5	≤ 1
	1	≥ 0	≤ –0.5
5	Floating or 5	≥ 4	≤ 3.5
	4	≥ 3	≤ 2.5
	3.5	≥ 2.5	≤ 2
3.3	Floating or 3.3	≥ 2.7	≤ 1.8

In the above table, the threshold levels are derived by the following equations:

REF – 1 V for enable
REF – 1.5 V for disable

Note that in order to maintain these threshold levels, the reference pin can be any voltage between (Vs+/2) + 1 V to Vs+ or left floating. The reference pin is internally connected to the positive rail, therefore it can be left floating to maintain these threshold levels.

For 3.3-V operation, the reference pin must be connected to the positive rail or left floating.

The recommended mode of operation is to tie the reference pin to midrail, thus setting the threshold levels to midrail +1.0 V and midrail +1.8 V.

NO. OF CHANNELS	PACKAGES
Single (8-pin)	THS4225D, THS4225DGN

Power Supply Decoupling Techniques and Recommendations

Power supply decoupling is a critical aspect of any high-performance amplifier design process. Careful decoupling provides higher quality ac performance (most notably improved distortion performance). The following guidelines ensure the highest level of performance.

1. Place decoupling capacitors as close to the power supply inputs as possible, with the goal of minimizing the inductance of the path from ground to the power supply.

2. Placement priority should put the smallest valued capacitors closest to the device.

3. Use of solid power and ground planes is recommended to reduce the inductance along power supply return current paths, with the exception of the areas underneath the input and output pins.

4. Recommended values for power supply decoupling include a bulk decoupling capacitor (6.8 to 22 μF), a mid-range decoupling capacitor (0.1 μF) and a high frequency decoupling capacitor (1000 pF) for each supply. A 100 pF capacitor can be used across the supplies as well for extremely high frequency return currents, but often is not required.

APPLICATION CIRCUITS

Driving an Analog-to-Digital Converter With the THS4222

The THS4222 can be used to drive high-performance analog-to-digital converters. Two example circuits are presented below.

The first circuit uses a wideband transformer to convert a single-ended input signal into a differential signal. The differential signal is then amplified and filtered by two THS4222 amplifiers. This circuit provides low intermodulation distortion, suppressed even-order distortion, 14 dB of voltage gain, a 50-Ω input impedance, and a single-pole filter at 25 MHz. For applications without signal content at dc, this method of driving ADCs can be very useful. Where dc information content is required, the THS4500 family of fully differential amplifiers may be applicable.

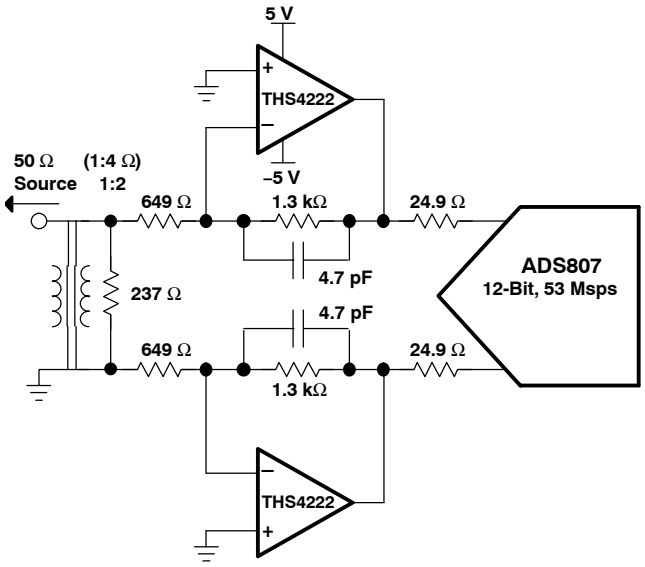
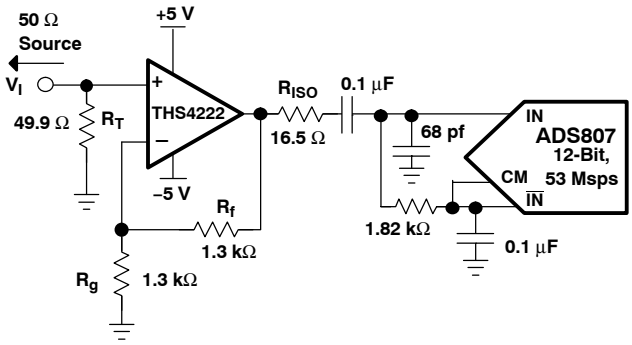


Figure 32. A Linear, Low Noise, High Gain ADC Preamplifier

The second circuit depicts single-ended ADC drive. While not recommended for optimum performance using converters with differential inputs, satisfactory performance can sometimes be achieved with single-ended input drive. An example circuit is shown here for reference.



NOTE: For best performance, high-speed ADCs should be driven differentially. See the THS4500 family of devices for more information.

Figure 33. Driving an ADC With a Single-Ended Input

Active Filtering With the THS4222

High-frequency active filtering with the THS4222 is achievable due to the amplifier's high slew rate, wide bandwidth, and voltage feedback architecture. Several options are available for high-pass, low-pass, bandpass, and bandstop filters of varying orders. A simple two-pole low pass filter is presented here as an example, with two poles at about 25 MHz.

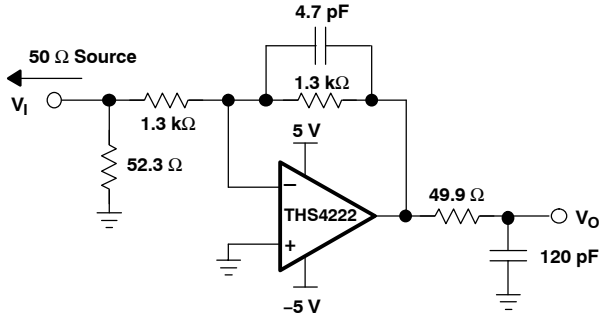


Figure 34. A Two-Pole Active Filter With Two Poles at about 25 MHz

NOISE ANALYSIS

High slew rates, stable unity gain, voltage-feedback operational amplifiers usually achieve their slew rate at the expense of a higher input noise voltage. The input-referred voltage noise, and the two input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 35 shows the amplifier noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

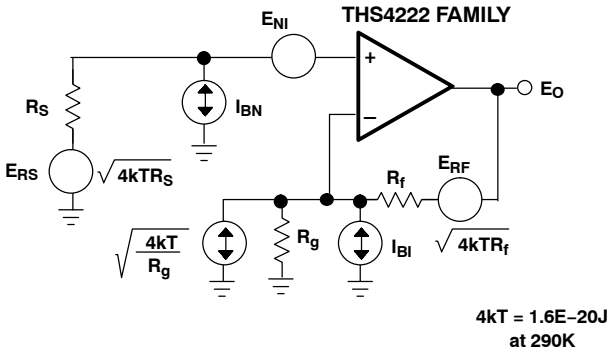


Figure 35. Noise Analysis Model

The total output shot noise voltage can be computed as the square of all squares output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 35:

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_f\right)^2 + 4kTR_fNG} \quad (1)$$

Dividing this expression by the noise gain (NG=(1+ R_f/R_g)) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in equation 2:

$$E_O = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_f}{NG}\right)^2 + \frac{4kTR_f}{NG}} \quad (2)$$

Driving Capacitive Loads

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter, including additional external capacitance, which may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the THS4222 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. When the primary considerations are frequency response flatness, pulse response fidelity, or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

BOARD LAYOUT

Achieving optimum performance with a high frequency amplifier like the THS4222 requires careful attention to board layout parasitics and external component types.

Recommendations that optimize performance include:

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

2. **Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1-μF decoupling capacitors.** At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (2.2-μF to 6.8-μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

3. **Careful selection and placement of external components will preserve the high frequency performance of the THS4222.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wire wound type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place

the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2.0 kΩ, this parasitic capacitance can add a pole and/or a zero below 400 MHz that can effect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations. It has been suggested here that a good starting point for design would be set the R_f be set to 1.3 kΩ for low-gain, noninverting applications. Doing this automatically keeps the resistor noise terms low, and minimize the effect of their parasitic capacitance.

4. **Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs Capacitive Load. Low parasitic capacitive loads (<4 pF) may not need an $R_{(ISO)}$, since the THS4222 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an $R_{(ISO)}$ are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and in fact a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS4222 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of $R_{(ISO)}$ vs Capacitive Load. This setting does not preserve signal integrity or a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

5. **Socketing a high speed part like the THS4222 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create a troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS4222 onto the board.

PowerPAD™ DESIGN CONSIDERATIONS

The THS4222 family is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 36(a) and Figure 36(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 36(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation.

During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the heretofore awkward mechanical methods of heatsinking.

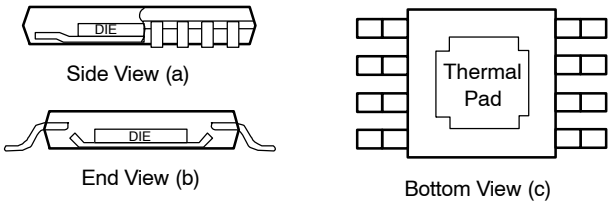


Figure 36. Views of Thermally Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

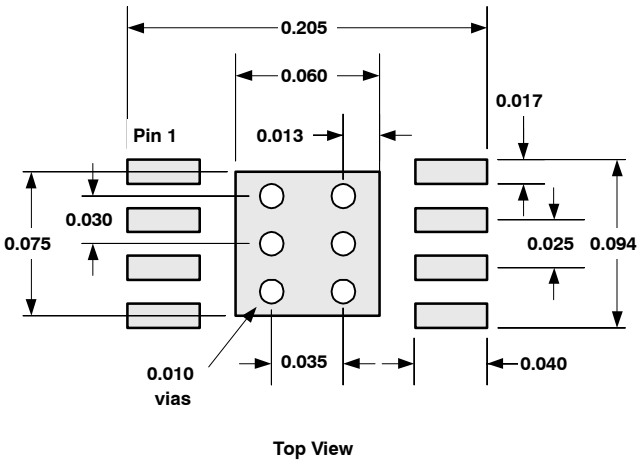


Figure 37. PowerPAD PCB Etch and Via Pattern

PowerPAD PCB LAYOUT CONSIDERATIONS

1. Prepare the PCB with a top side etch pattern as shown in Figure 37. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. They help dissipate the heat generated by the THS4222 family IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This resistance makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS4222 family PowerPAD package should make their connection to the internal ground plane, with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA} , the maximum power dissipation is shown in Figure 38 and is calculated by the equation 5:

$$P_D = \frac{T_{max} - T_A}{\theta_{JA}} \quad (3)$$

where:
P_D = Maximum power dissipation of THS4222 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to the case
θ_{CA} = Thermal coefficient from the case to ambient air (°C/W).

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class AB), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. For a single package, the sum of the RMS output currents and voltages should be used to choose the proper package.

THERMAL ANALYSIS

The THS4222 family of devices does not incorporate automatic thermal shutoff protection, so the designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of 150° C is exceeded.

The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where:
P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the THS4222 family is offered in MSOP with PowerPAD. The thermal coefficient for the MSOP PowerPAD package is substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the two packages. The data for the DGN package assumes a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application notes in the *Additional Reference Material* section at the end of the data sheet.

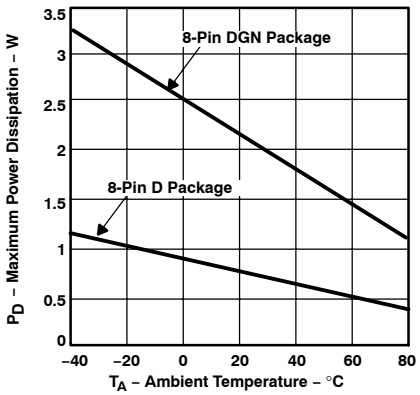


Figure 38. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to consider not only quiescent power dissipation, but also dynamic power dissipation. Often maximum power dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DESIGN TOOLS

Evaluation Fixtures, Spice Models, and Applications Support

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal, evaluation boards have been developed for the THS4222 family of operational amplifiers. The boards are easy to use, allowing for straight-forward evaluation of the device. These evaluation boards can be ordered through the Texas Instruments web site, www.ti.com, or through your local Texas Instruments sales representative. Schematics for the two evaluation boards are shown below with their default component values. Unpopulated footprints are shown to provide insight into design flexibility.

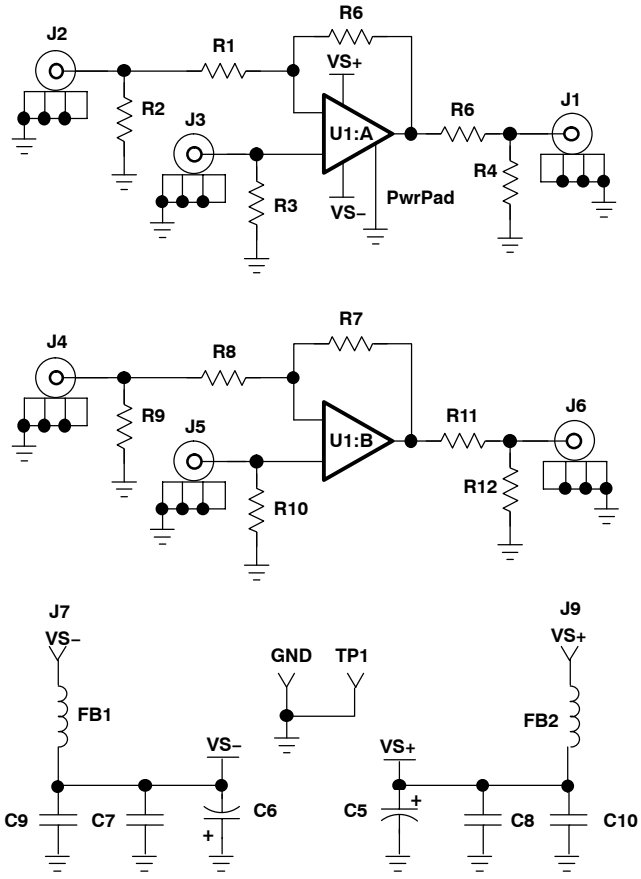


Figure 39. THS4222 EVM Circuit Configuration

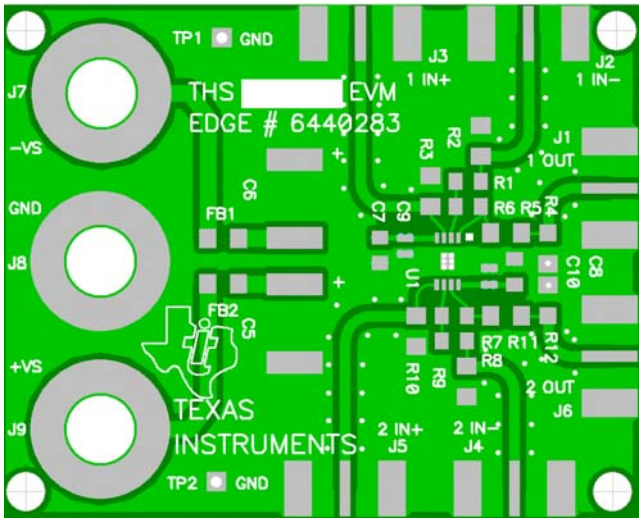


Figure 40. THS4222 EVM Board Layout (Top Layer)

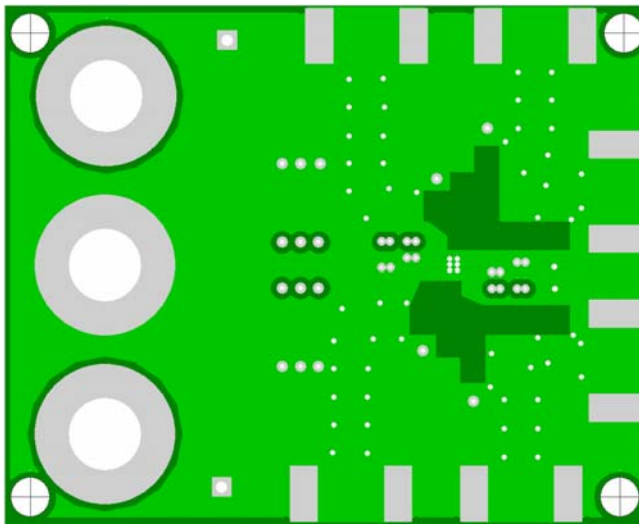


Figure 41. THS4222 EVM Board Layout (2nd Layer, Ground)

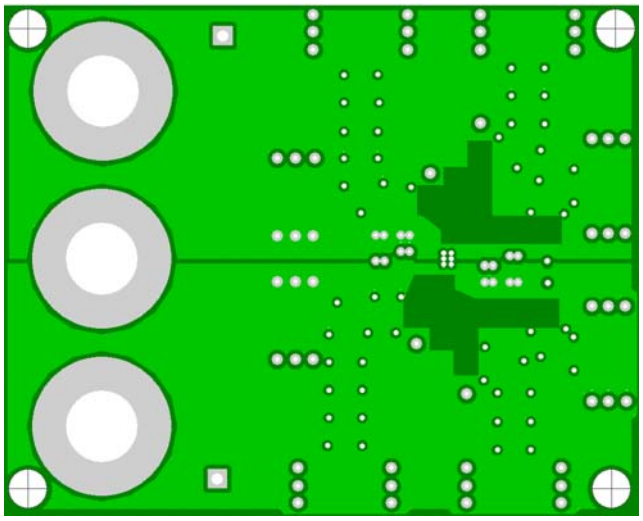


Figure 42. THS4222 EVM Board Layout (3rd Layer, Power)

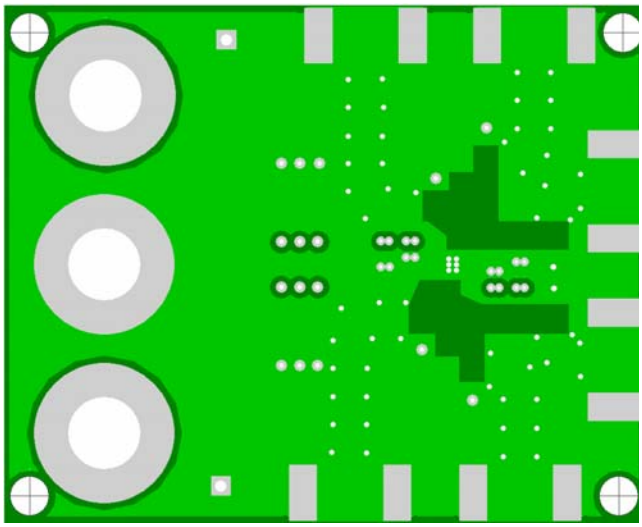


Figure 43. THS4222 EVM Board Layout (Bottom Layer)

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS4222 family is available through the Texas Instruments web site (www.ti.com). The PIC is also available for design assistance and detailed product information. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

ADDITIONAL REFERENCE MATERIAL

- *PowerPAD Made Easy*, application brief (SLMA004)
- *PowerPAD Thermally Enhanced Package*, technical brief (SLMA002)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4221D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4221
THS4221D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4221
THS4221DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFS
THS4221DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFS
THS4221DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFS
THS4221DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFS
THS4221DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
THS4221DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BHX
THS4221DGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BHX
THS4221DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BHX
THS4221DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BHX
THS4221DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFT
THS4221DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFT
THS4222D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4222
THS4222D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4222
THS4222DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BHW
THS4222DGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BHW
THS4222DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BFO
THS4222DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFO
THS4222DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BFO
THS4222DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFO
THS4222DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4222
THS4222DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4222
THS4225D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4225
THS4225D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4225
THS4225DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFY
THS4225DGK.A	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFY
THS4225DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFU
THS4225DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFU

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4226DGQ	Active	Production	HVSSOP (DGQ) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFP
THS4226DGQ.A	Active	Production	HVSSOP (DGQ) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BFP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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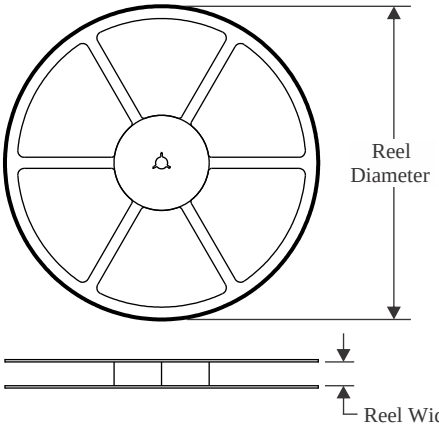
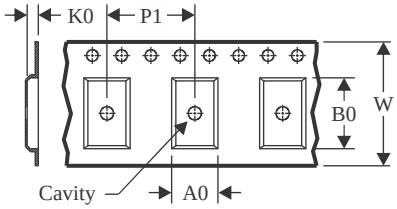
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

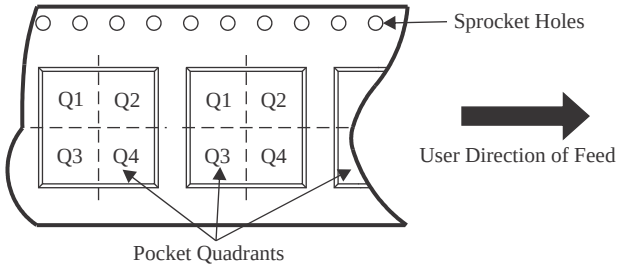


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

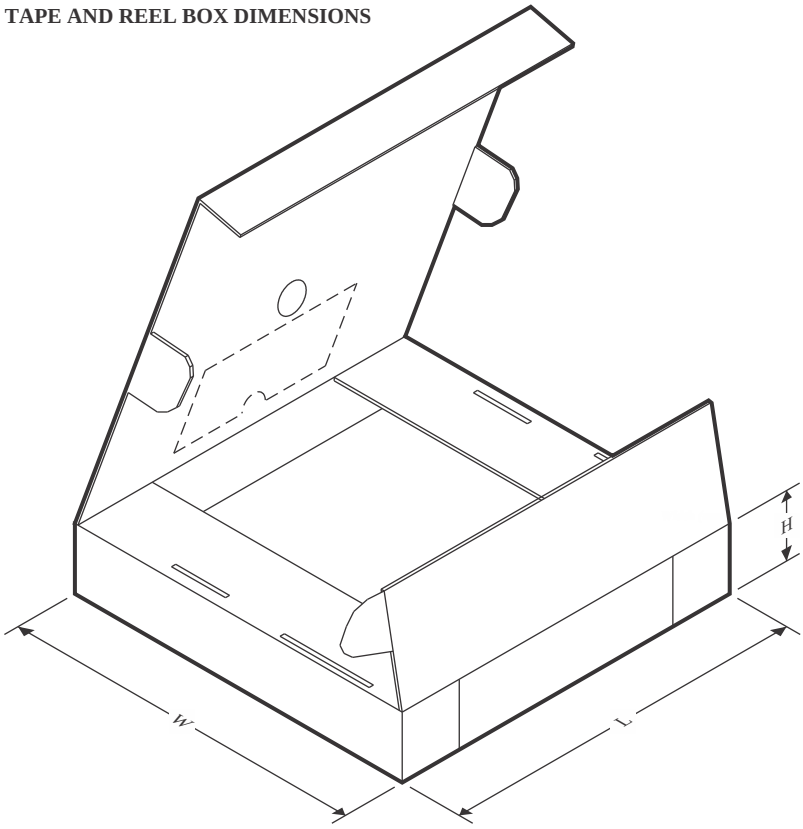
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4221DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
THS4221DBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
THS4221DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4222DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4222DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4222DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

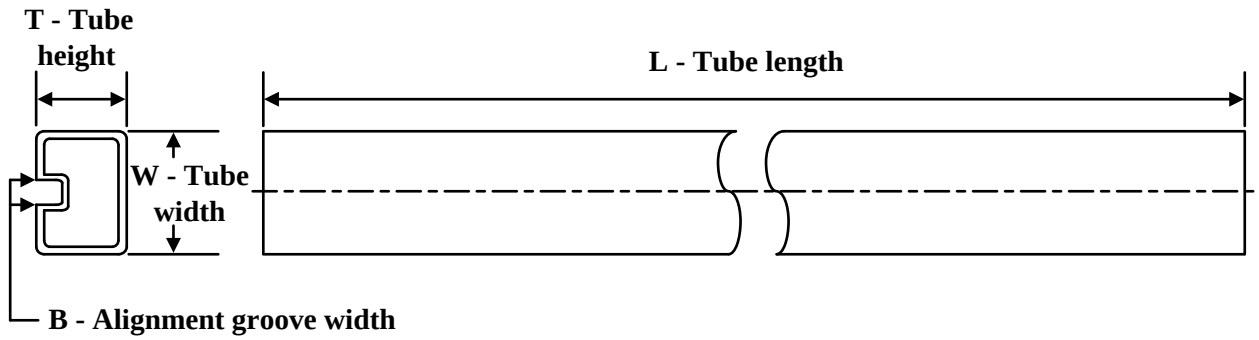
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4221DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
THS4221DBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
THS4221DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4222DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4222DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4222DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

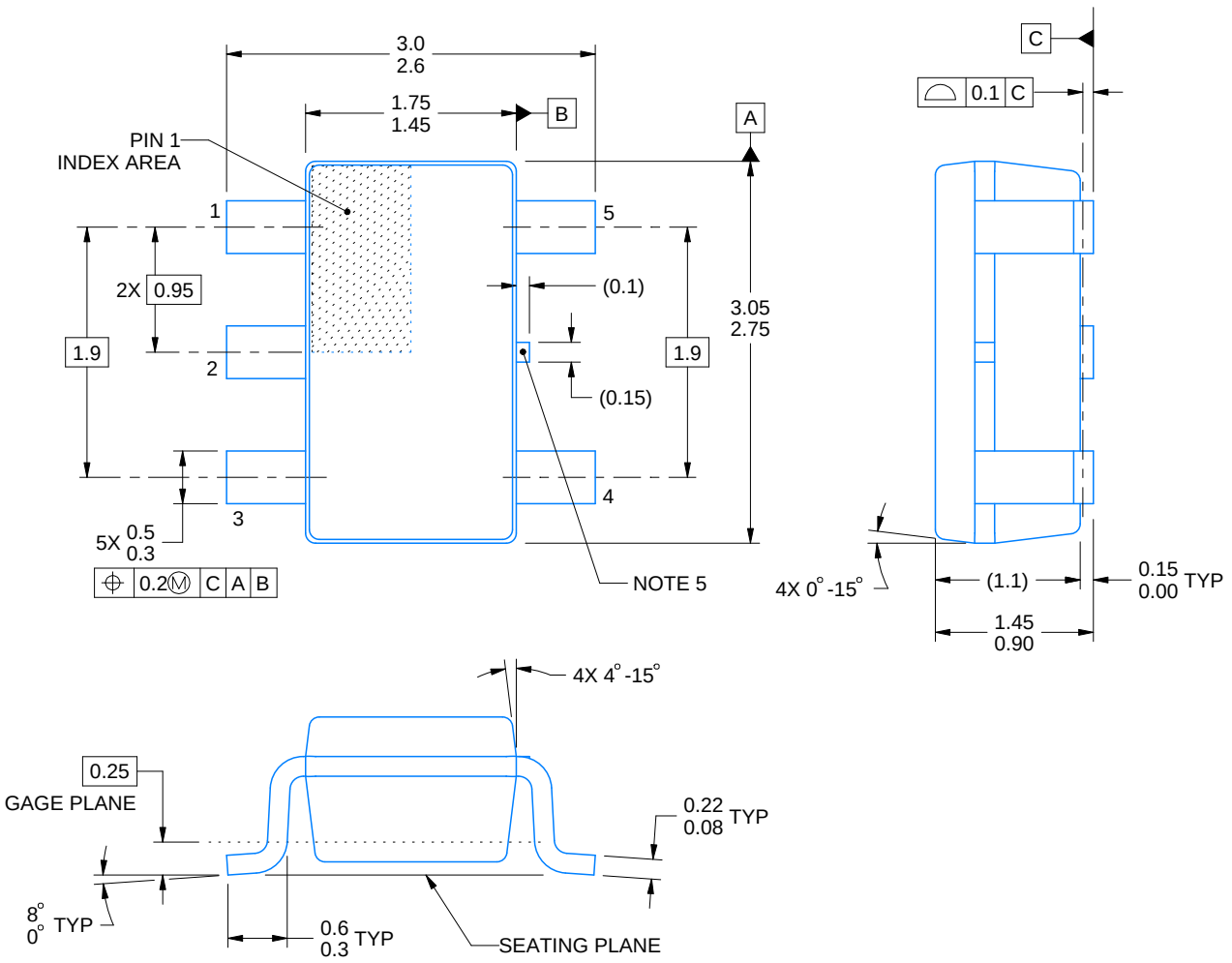
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4221D	D	SOIC	8	75	505.46	6.76	3810	4
THS4221D.A	D	SOIC	8	75	505.46	6.76	3810	4
THS4222D	D	SOIC	8	75	505.46	6.76	3810	4
THS4222D.A	D	SOIC	8	75	505.46	6.76	3810	4
THS4222DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THS4222DGK.A	DGK	VSSOP	8	80	330	6.55	500	2.88
THS4222DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS4222DGN.A	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS4225D	D	SOIC	8	75	505.46	6.76	3810	4
THS4225D.A	D	SOIC	8	75	505.46	6.76	3810	4

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

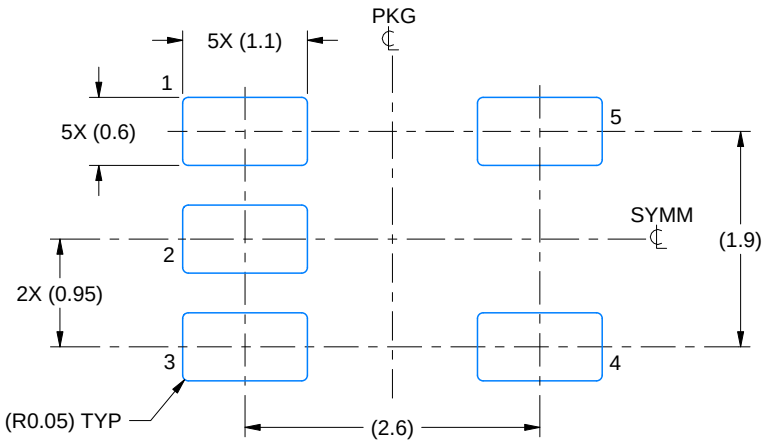
SMALL OUTLINE TRANSISTOR



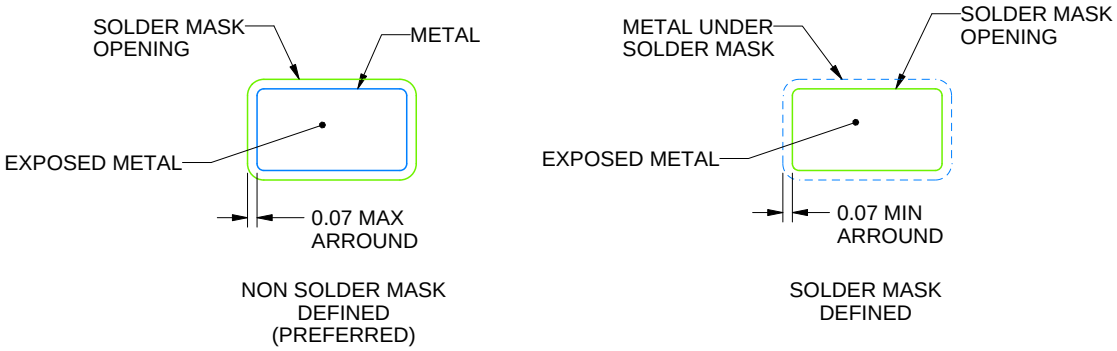
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

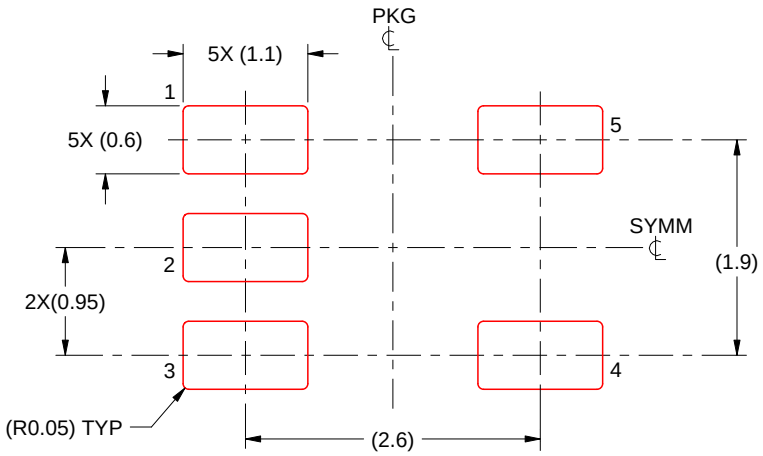


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

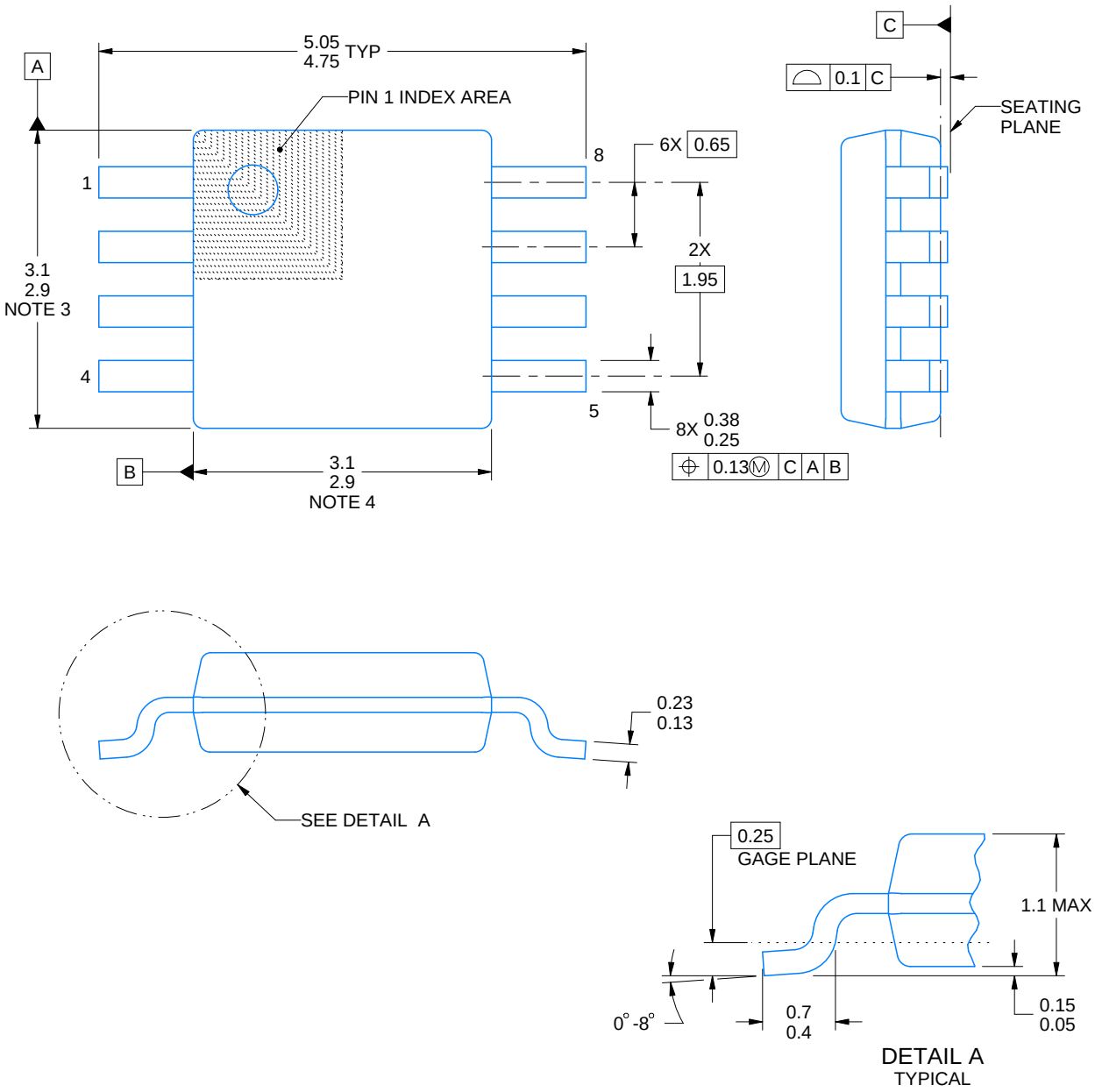
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

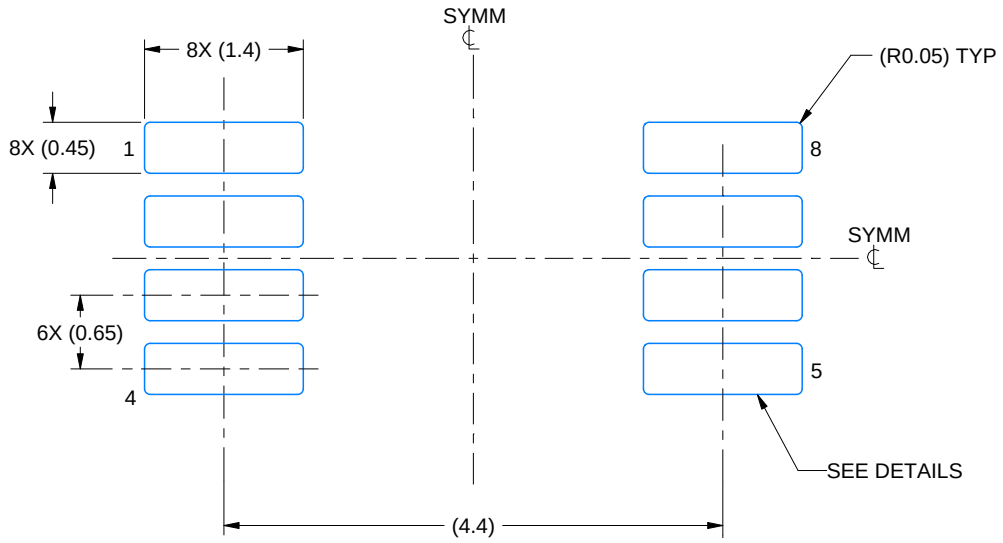
SMALL OUTLINE PACKAGE



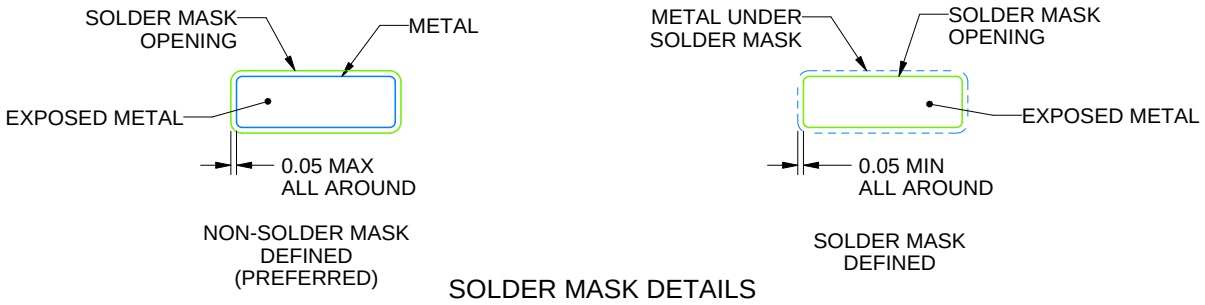
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

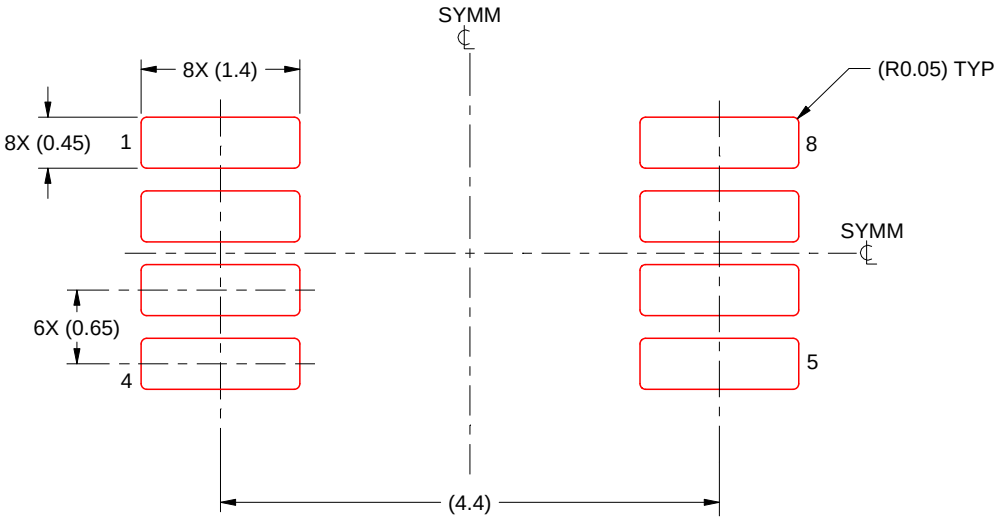


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

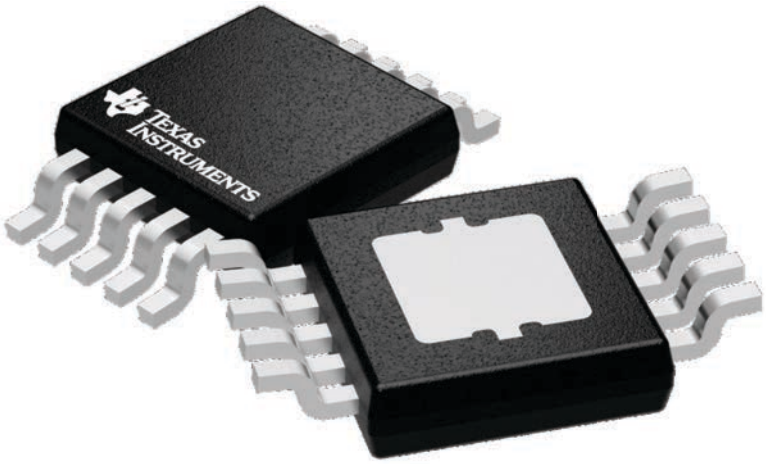
GENERIC PACKAGE VIEW

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

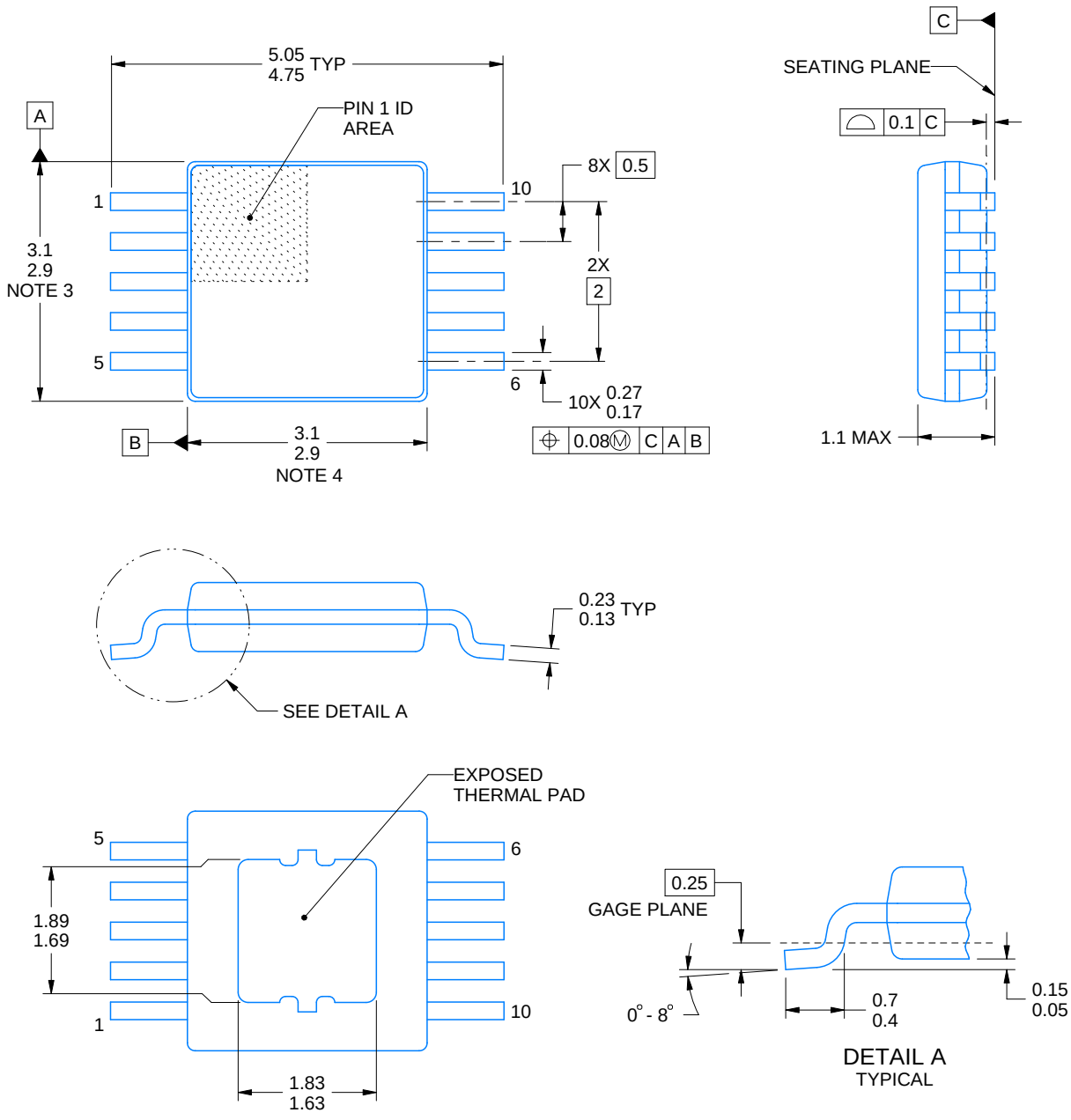
4224775/A

PACKAGE OUTLINE

DGQ0010D

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE

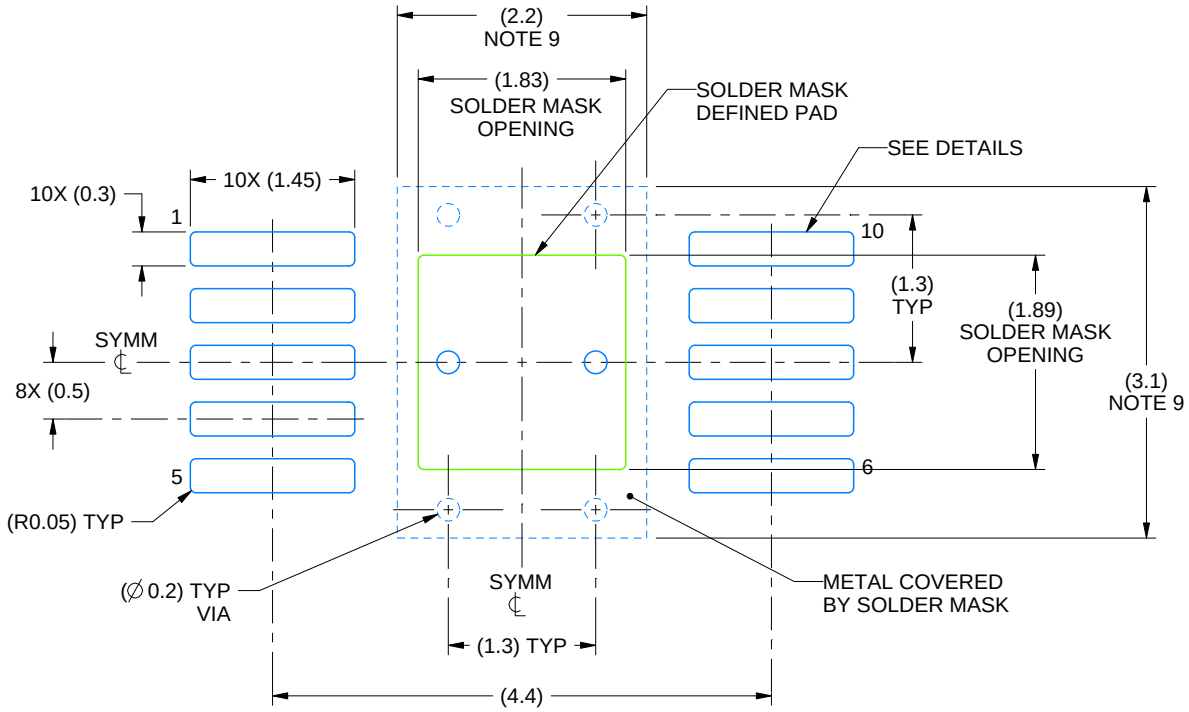


4218842/B 04/2024

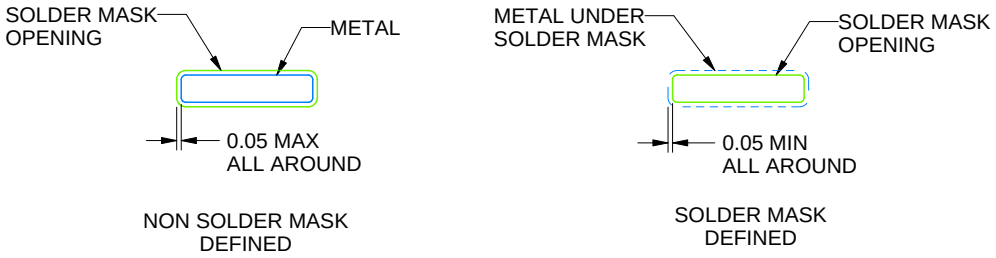
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4218842/B 04/2024

NOTES: (continued)

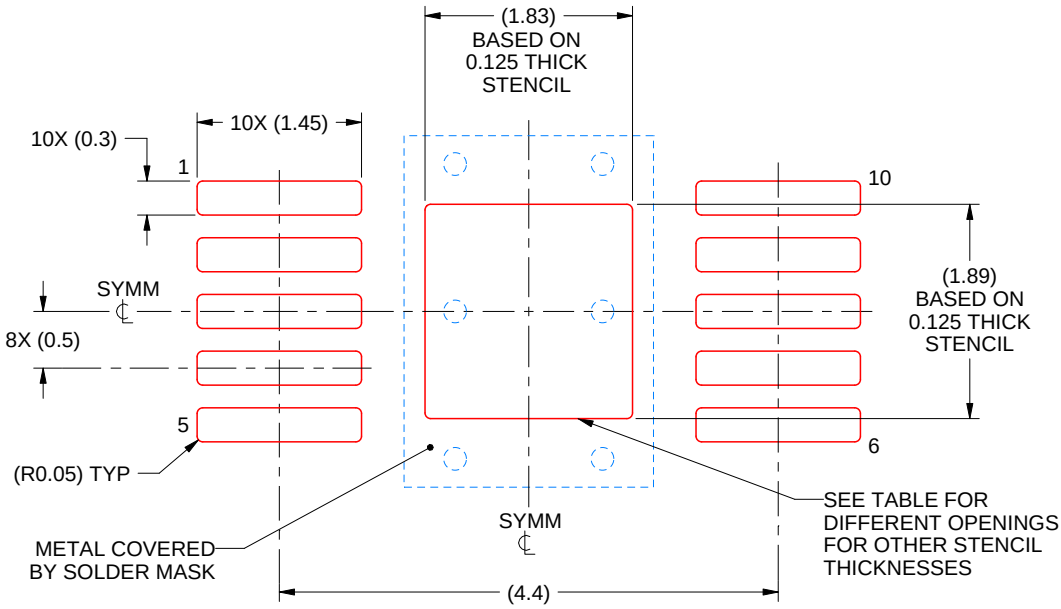
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGQ0010D

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.11
0.125	1.83 X 1.89 (SHOWN)
0.150	1.67 X 1.73
0.175	1.55 X 1.60

4218842/B 04/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

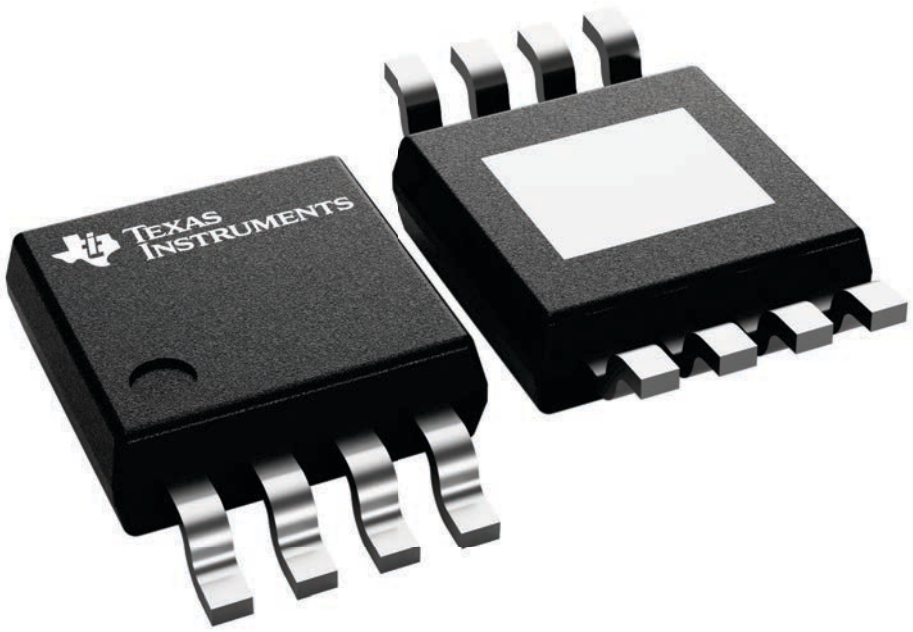
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

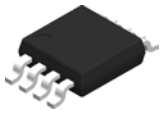
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



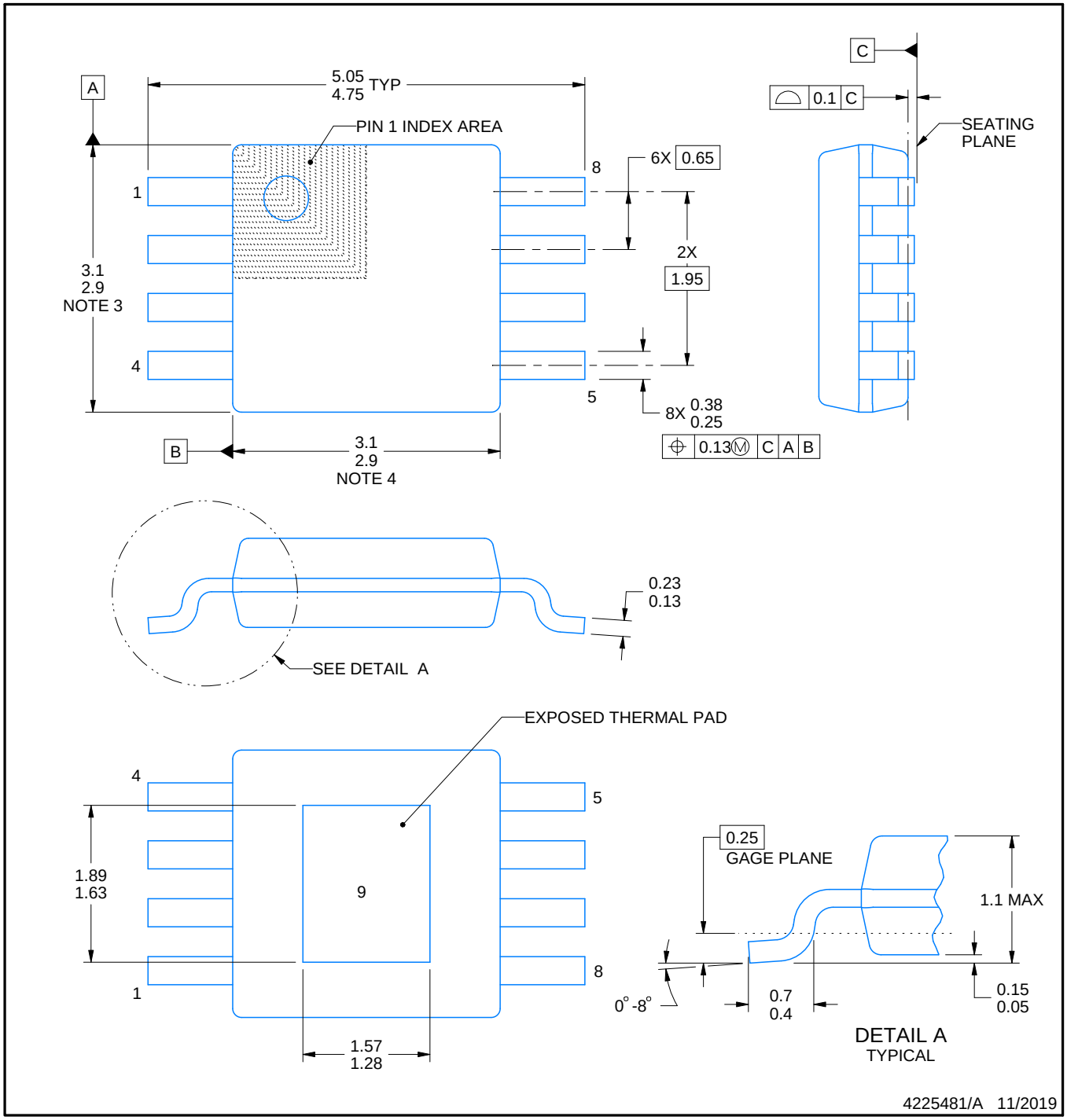
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

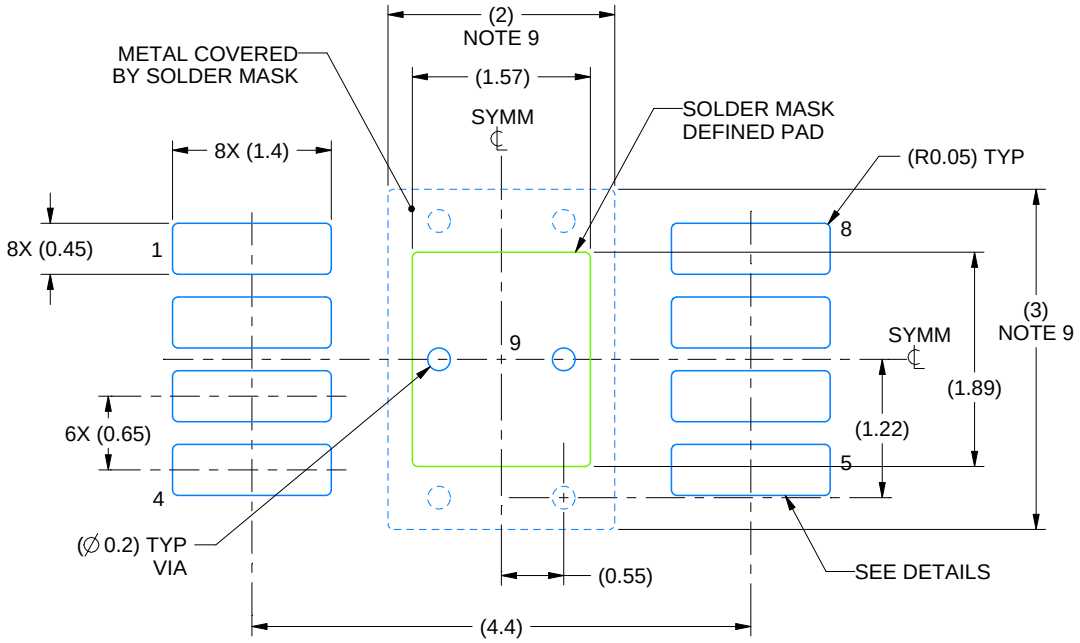
SMALL OUTLINE PACKAGE



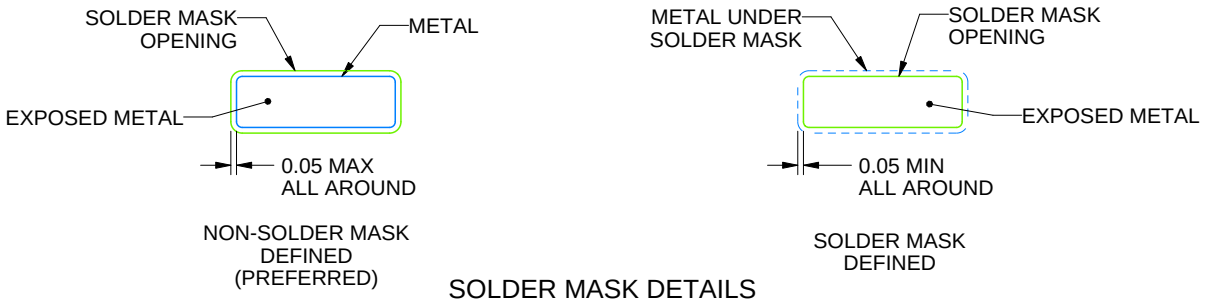
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

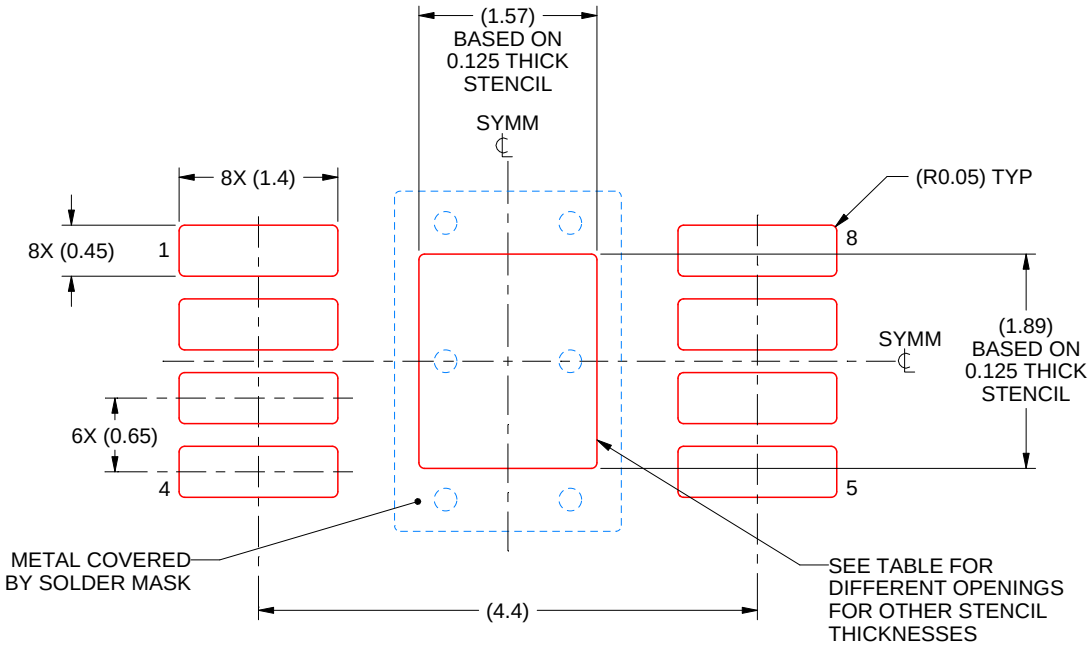


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

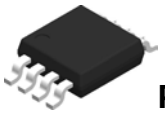
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

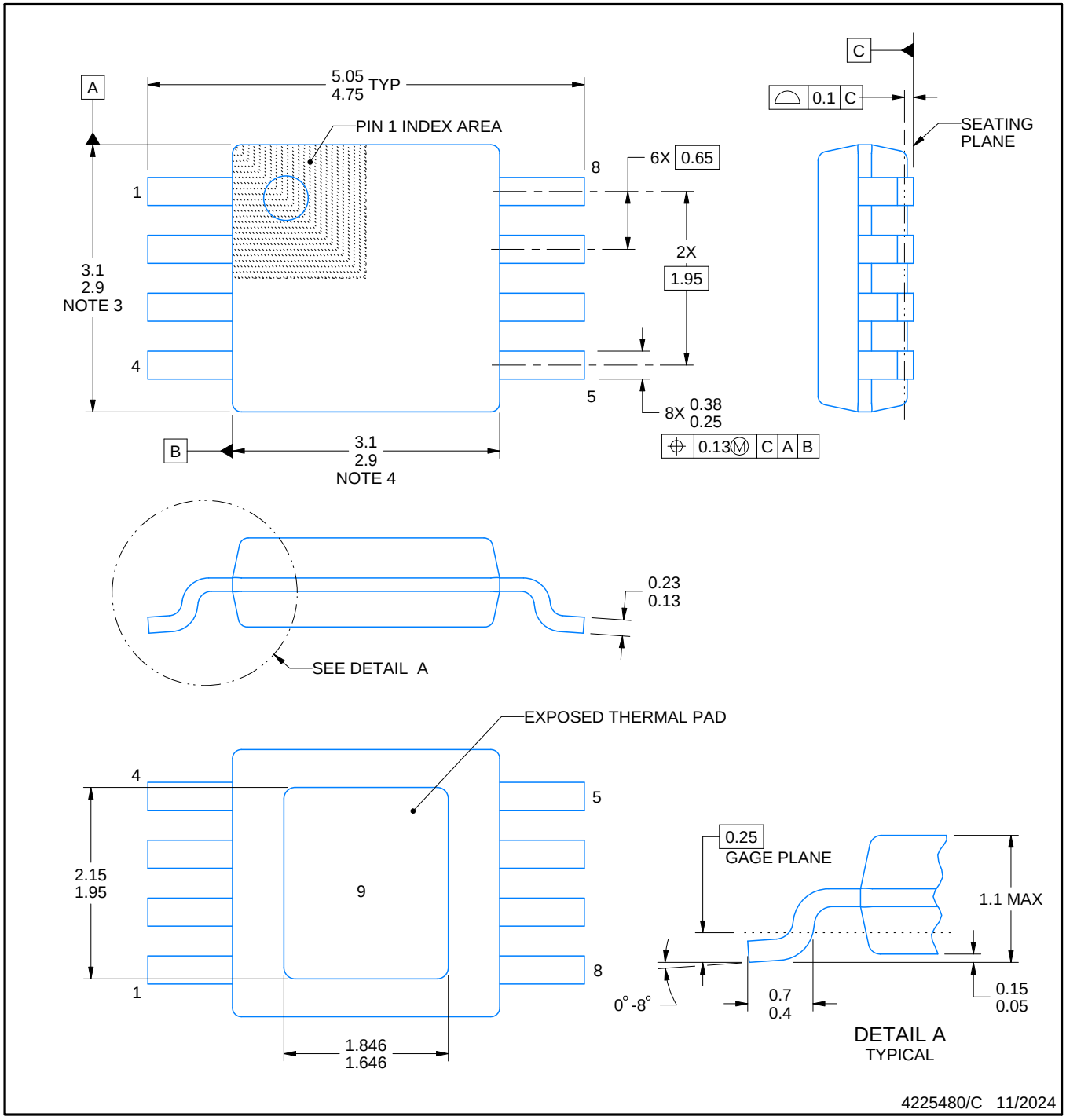
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

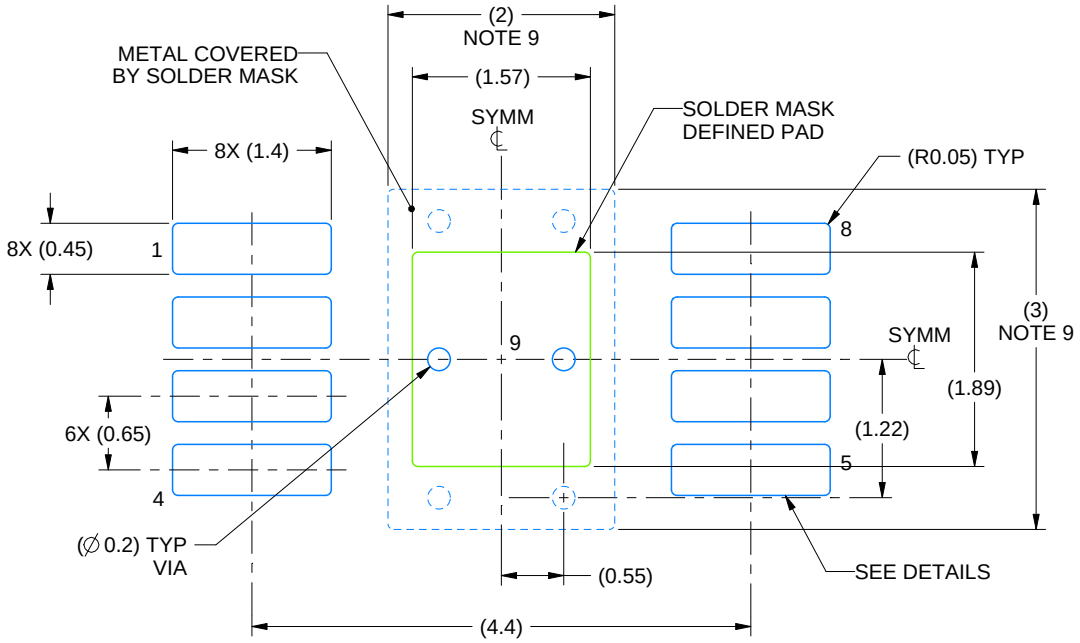
SMALL OUTLINE PACKAGE



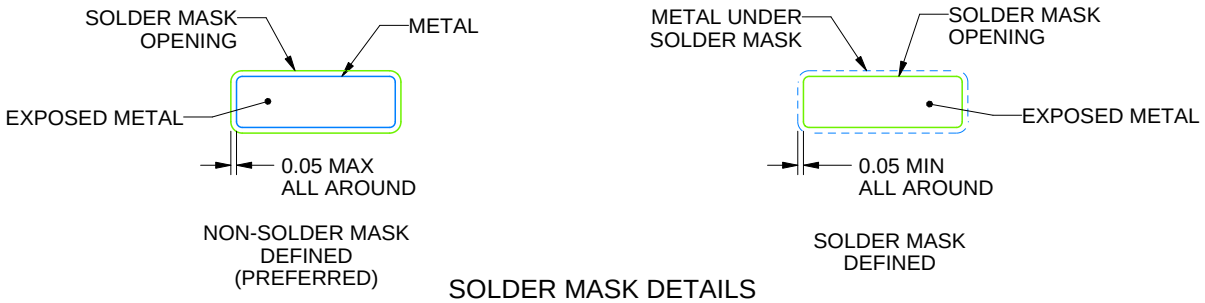
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

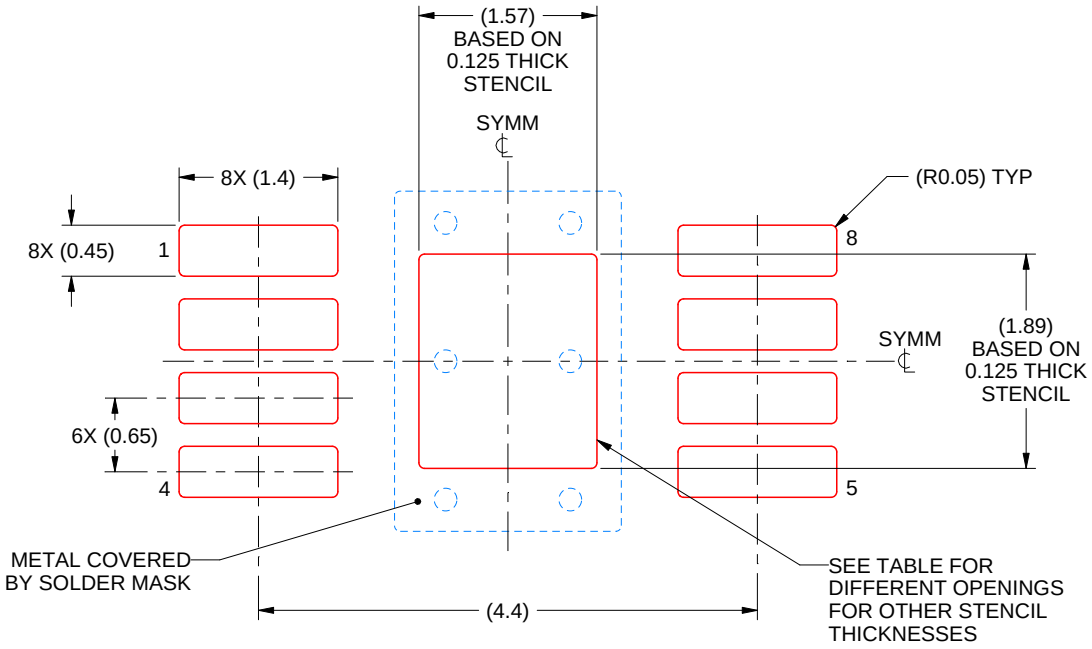


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



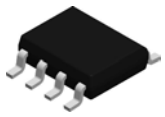
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

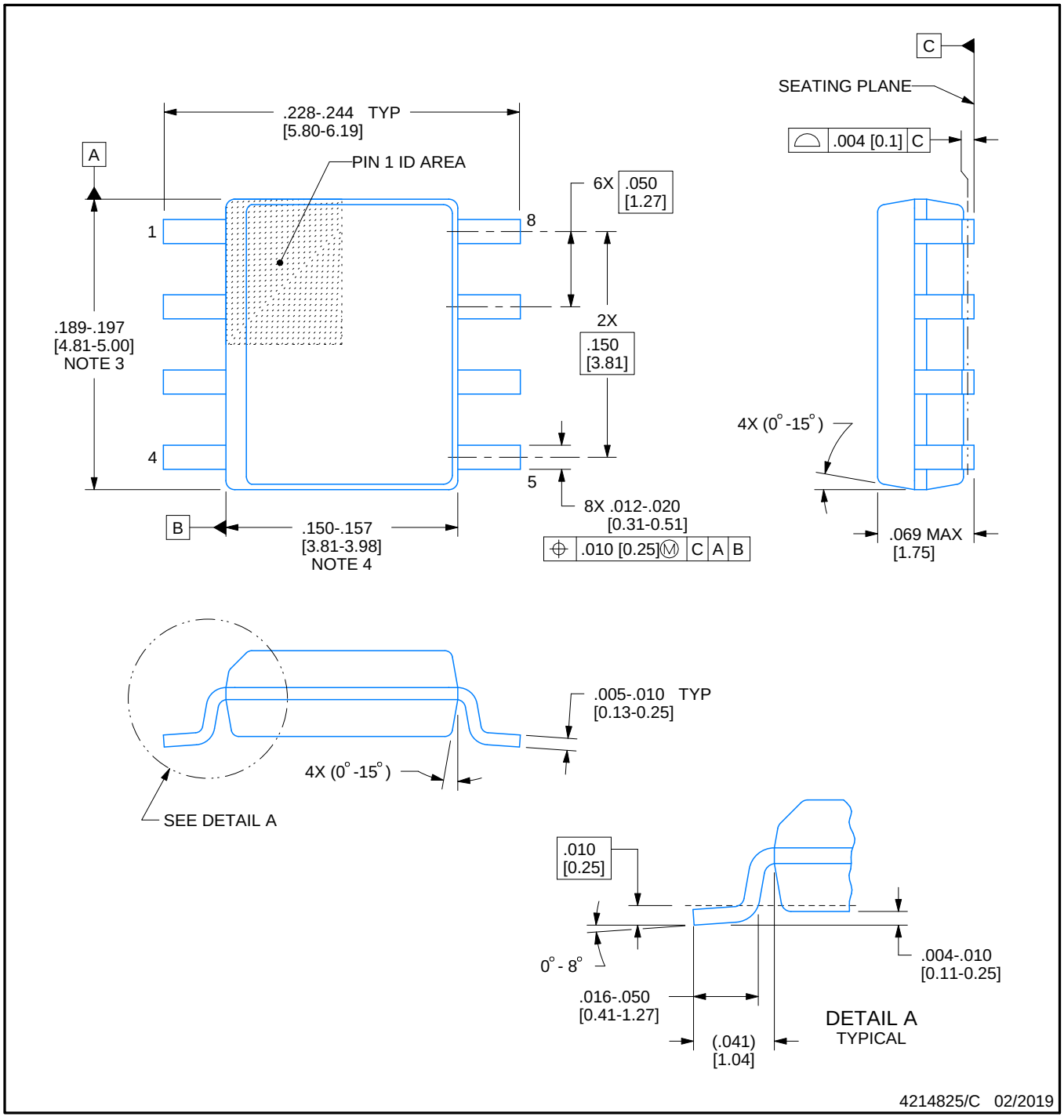


PACKAGE OUTLINE

D0008A

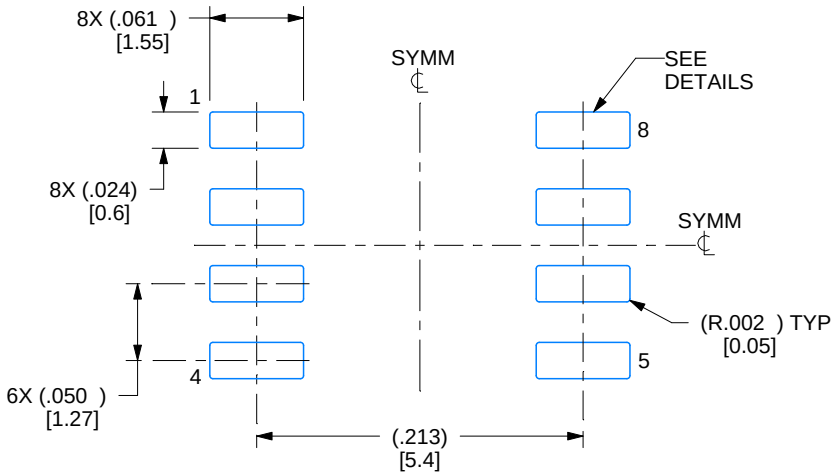
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

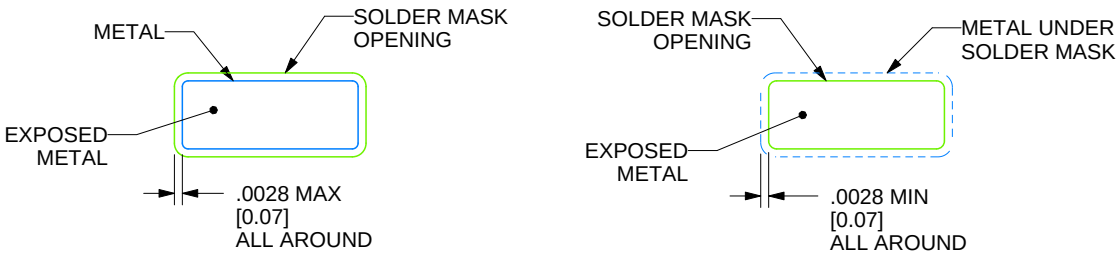


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

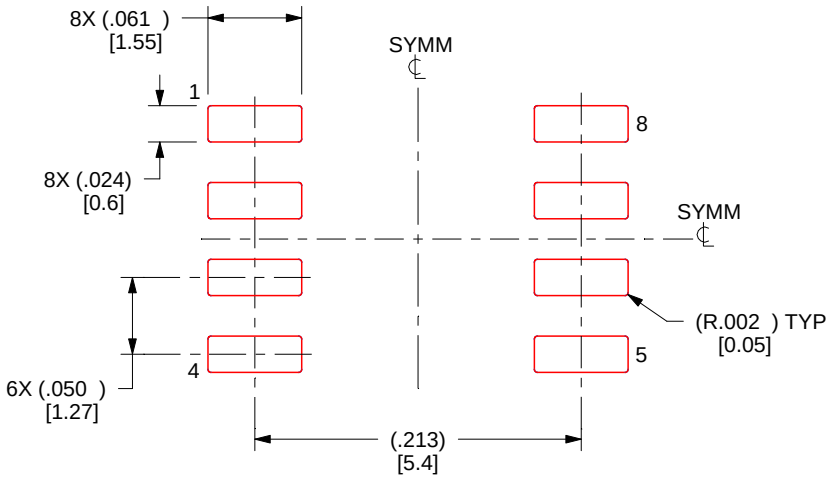
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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