

## 超低功耗、轨到轨输出、全差分放大器

查询样品: **THS4531A**

### 特性

- 超低功耗:
  - 电压: **2.5V 至 5.5V**
  - 电流: **250 $\mu$ A**
  - 省电模式: **0.5 $\mu$ A** (典型值)
- 全差分架构
- 带宽: **36MHz**
- 转换速率: **200V/ $\mu$ s**
- 总谐波失真 (THD): **1kHz (1V<sub>RMS</sub>, R<sub>L</sub>=2k $\Omega$ ) 时为 -120dBc**
- 输入电压噪声: **10nV/ $\sqrt{\text{Hz}}$ (f=1kHz)**
- 高 DC 精度:
  - V<sub>OS</sub>:  **$\pm$ 100 $\mu$ V**
  - V<sub>OS</sub>漂移:  **$\pm$ 3 $\mu$ V/ $^{\circ}$ C (-40 $^{\circ}$ C 至 +125 $^{\circ}$ C)**
  - A<sub>OL</sub>: **114dB**
- 轨到轨输出 (RRO)
- 负电源轨输入 (NRI)
- 输出共模控制

### 应用范围

- 低功耗逐次逼近 (SAR), 三角积分模数转换器 (ADC) 驱动器
- 低功耗、高性能:
  - 差分到差分放大器
  - 单端到差分放大器
- 低功耗、宽带宽差分驱动器
- 低功耗、宽带宽差分信号调节
- 高通道数量和功率密集系统

### 说明

THS4531A 是一款低功耗、完全差分运算放大器, 此放大器具有低于负电源轨和轨到轨输出的输入共模范围。此器件设计用于能耗和功率耗散都十分关键的低功率数据采集系统和高密度应用。

此器件特有精确输出共模控制, 此控制可实现驱动模数转换器 (ADC) 时的 dc 耦合。与低于负电源轨和轨到轨输出的输入共模范围相耦合, 此控制可只使用 2.5V 至 5V 的单电源轻松实现单端接地基准信号源与逐次逼近 (SAR) 的连接和三角积分( $\Delta\Sigma$ ) ADC 的对接。THS4531A 也是一款用于通用、低功率差分信号调节应用的实用工具。

THS4531A 可在介于 -40 $^{\circ}$ C 至 +125 $^{\circ}$ C 的扩展工业温度范围内运行。可提供下列封装选项:

- 8 引脚小外形尺寸集成电路 (SOIC) (微型小外形尺寸 (MSOP)) 和超薄型小外形尺寸 (VSSOP) (D 和 DGK) 封装
- 10 引脚超薄四方扁平无引线封装 (WQFN)(RUN)

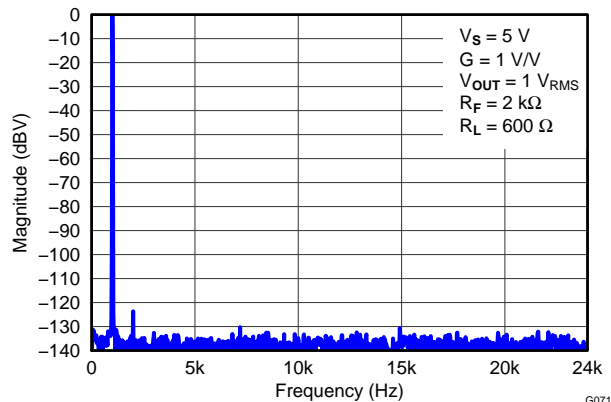


图 1. 音频分析仪上的 1kHz 快速傅里叶变换 (FFT) 幅值频率

表 1. 相关产品

器件	带宽 (BW) (MHz)	I <sub>Q</sub> (mA)	100kHz 下的总谐波失真 (THD)(dBc)	V <sub>N</sub> (nV/ $\sqrt{\text{Hz}}$ )	轨到轨
THS4521	145	1.14	-120	4.6	输出
THS4520	570	15.3	-114	2	输出
THS4121	100	16	-79	5.4	输入/输出
THS4131	150	16	-107	1.3	否



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGING/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	CHANNEL COUNT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
THS4531A	1	SOIC-8	D	–40°C to +125°C	T4531A	THS4531AID	Rails, 75
	1				T4531A	THS4531AIDR	Tape and reel, 2500
	1	VSSOP-8	DGK	–40°C to +125°C	531A	THS4531AIDGK	Rails, 80
	1				531A	THS4531AIDGKR	Tape and reel, 2500
	1	WQFN-10	RUN	–40°C to +125°C	531A	THS4531AIRUNT	Tape and reel, 250
	1				531A	THS4531AIRUNR	Tape and reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS

	VALUE	UNITS
Supply voltage, $V_{S-}$ to $V_{S+}$	5.5	
Input/output voltage, $V_{IN\pm}$ , $V_{OUT\pm}$ , and $V_{OCM}$ pins	$(V_{S-}) - 0.7$ to $(V_{S+}) + 0.7$	V
Differential input voltage, $V_{ID}$	1	V
Continuous output current, $I_O$	50	mA
Continuous input current, $I_i$	0.75	mA
Continuous power dissipation	See Thermal Information	
Maximum junction temperature, $T_J$	150	°C
Operating free-air temperature range, $T_A$	–40 to +125	°C
Storage temperature range, $T_{stg}$	–65 to +150	°C
Electrostatic discharge (ESD) ratings:	Human body model (HBM)	3 kV
	Charge device model (CDM)	500 V

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		THS4531A	THS4531A	THS4531A	UNITS
		SOIC (P)	VSSOP (MSOP) (DGK)	WQFN (RUN)	
		8 PINS	8 PINS	10 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	133	198	163	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance	78	84	66	
$\theta_{JB}$	Junction-to-board thermal resistance	73	120	113	
$\psi_{JT}$	Junction-to-top characterization parameter	26	19	17	
$\psi_{JB}$	Junction-to-board characterization parameter	73	118	113	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

(1) 有关传统和新的热 度量的更多信息，请参阅IC 封装热度量应用报告，[SPRA953](#)。

**ELECTRICAL CHARACTERISTICS:  $V_S = 2.7\text{ V}$** 

Test conditions at  $T_A = 25^\circ\text{C}$ ,  $V_{S+} = 2.7\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2\text{ V}_{PP}$ ,  $R_F = 2\text{ k}\Omega$ ,  $R_L = 2\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, and input and output referenced to mid-supply, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL
AC PERFORMANCE						
Small-signal bandwidth	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 1	34			MHz	C
	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 2	16				
	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 5	6				
	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 10	2.7				
Gain-bandwidth product	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 10	27			MHz	
Large-signal bandwidth	V <sub>OUT</sub> = 2 V <sub>PP</sub> , G = 1	34			MHz	
Bandwidth for 0.1-dB flatness	V <sub>OUT</sub> = 2 V <sub>PP</sub> , G = 1	12			MHz	
Slew rate, rise/fall, 25% to 75%	V <sub>OUT</sub> = 2-V step	190/320			V/μs	
Rise/fall time, 10% to 90%		5.2/6.1			ns	
Settling time to 1%, rise/fall		25/20			ns	
Settling time to 0.1%, rise/fall		60/60				
Settling time to 0.01%, rise/fall		150/110			ns	
Overshoot/undershoot, rise/fall		1/1			%	
2nd-order harmonic distortion		f = 1 kHz, V <sub>OUT</sub> = 1 V <sub>RMS</sub>	−122			
	f = 10 kHz	−127				
	f = 1 MHz	−59				
3rd-order harmonic distortion	f = 1 kHz, V <sub>OUT</sub> = 1 V <sub>RMS</sub>	−130			dBc	
	f = 10 kHz	−135				
	f = 1 MHz	−70				
2nd-order intermodulation distortion	f = 1 MHz, 200-kHz tone spacing, V <sub>OUT</sub> envelope = 2 V <sub>PP</sub>	−83			dBc	
3rd-order intermodulation distortion		−81				
Input voltage noise	f = 1 kHz	10			nV/√Hz	
Voltage noise 1/f corner frequency		45			Hz	
Input current noise	f = 100 kHz	0.25			pA/√Hz	
Current noise 1/f corner frequency		6.5			kHz	
Overdrive recovery time	Overdrive = 0.5 V	65			ns	
Output balance error	V <sub>OUT</sub> = 100 mV, f = 1 MHz	−65			dB	
Closed-loop output impedance	f = 1 MHz (differential)	2.5			Ω	

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## ELECTRICAL CHARACTERISTICS: $V_S = 2.7\text{ V}$ (continued)

Test conditions at  $T_A = 25^\circ\text{C}$ ,  $V_{S+} = 2.7\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2 V_{PP}$ ,  $R_F = 2\text{ k}\Omega$ ,  $R_L = 2\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, and input and output referenced to mid-supply, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL
DC PERFORMANCE						
Open-loop voltage gain ( $A_{OL}$ )		100	113		dB	A
Input-referred offset voltage	$T_A = +25^{\circ}\text{C}$		$\pm 100$	$\pm 400$	$\mu\text{V}$	A
	$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			$\pm 715$		B
	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			$\pm 855$		
	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$			$\pm 1300$		
Input offset voltage drift <sup>(1)</sup>	$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$		$\pm 2$	$\pm 7$	$\mu\text{V}/^{\circ}\text{C}$	B
	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		$\pm 2$	$\pm 7$		
	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		$\pm 3$	$\pm 9$		
Input bias current	$T_A = +25^{\circ}\text{C}$		200	250	nA	A
	$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			275		B
	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			286		
	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$			305		
Input bias current drift <sup>(1)</sup>	$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$		0.45	0.55	nA/ $^{\circ}\text{C}$	B
	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		0.45	0.55		
	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		0.45	0.55		
Input offset current	$T_A = +25^{\circ}\text{C}$		$\pm 5$	$\pm 50$	nA	A
	$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			$\pm 55$		B
	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$			$\pm 57$		
	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$			$\pm 60$		
Input offset current drift <sup>(1)</sup>	$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$		$\pm 0.03$	$\pm 0.1$	nA/ $^{\circ}\text{C}$	B
	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$		$\pm 0.03$	$\pm 0.1$		
	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		$\pm 0.03$	$\pm 0.1$		
INPUT						
Common-mode input low	$T_A = +25^{\circ}\text{C}$ , CMRR > 87 dB		$V_{S-} - 0.2$	$V_{S-}$	V	A
	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$ , CMRR > 87 dB		$V_{S-} - 0.2$	$V_{S-}$		B
Common-mode input high	$T_A = +25^{\circ}\text{C}$ , CMRR > 87 dB	$V_{S+} - 1.2$	$V_{S+} - 1.1$		V	A
	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$ , CMRR > 87 dB	$V_{S+} - 1.2$	$V_{S+} - 1.1$			B
Common-mode rejection ratio		90	116		dB	A
Input impedance common-mode			200    1.2		k $\Omega$    pF	C
Input impedance differential mode			200    1			C
OUTPUT						
Single-ended output voltage: low	$T_A = +25^{\circ}\text{C}$		$V_{S-} + 0.06$	$V_{S-} + 0.2$	V	A
	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$		$V_{S-} + 0.06$	$V_{S-} + 0.2$		B
Single-ended output voltage: high	$T_A = +25^{\circ}\text{C}$	$V_{S+} - 0.2$	$V_{S+} - 0.11$		V	A
	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	$V_{S+} - 0.2$	$V_{S+} - 0.11$			B
Output saturation voltage: high/low			110/60		mV	C
Linear output current drive	$T_A = +25^{\circ}\text{C}$	$\pm 15$	$\pm 22$		mA	A
	$T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	$\pm 15$				B

(1) Input offset voltage drift, input bias current drift, and input offset current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

**ELECTRICAL CHARACTERISTICS:  $V_S = 2.7\text{ V}$  (continued)**

Test conditions at  $T_A = 25^\circ\text{C}$ ,  $V_{S+} = 2.7\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2\text{ V}_{PP}$ ,  $R_F = 2\text{ k}\Omega$ ,  $R_L = 2\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, and input and output referenced to mid-supply, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL
POWER SUPPLY						
Specified operating voltage		2.5		5.5	V	B
Quiescent operating current/ch	$T_A = +25^{\circ}\text{C}$ , $\overline{\text{PD}} = V_{S+}$		230	330	$\mu\text{A}$	A
	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ , $\overline{\text{PD}} = V_{S+}$		270	370		B
Power-supply rejection (PSRR)		87	108		dB	A
POWER DOWN						
Enable voltage threshold	Specified on above 2.1 V			2.1	V	A
Disable voltage threshold	Specified off below 0.7 V	0.7				A
Disable pin bias current	$\overline{\text{PD}} = V_{S-} + 0.5\text{ V}$		50	500	nA	A
Power-down quiescent current	$\overline{\text{PD}} = V_{S-} + 0.5\text{ V}$		0.5	2	$\mu\text{A}$	A
Turn-on time delay	Time from $\overline{\text{PD}} = \text{high}$ to $V_{\text{OUT}} = 90\%$ of final value, $R_L = 200\ \Omega$		650		ns	C
Turn-off time delay	Time from $\overline{\text{PD}} = \text{low}$ to $V_{\text{OUT}} = 10\%$ of original value, $R_L = 200\ \Omega$		20			
OUTPUT COMMON-MODE VOLTAGE CONTROL ( $V_{\text{OCM}}$ )						
Small-signal bandwidth	$V_{\text{OCM}}$ input = 100 mV <sub>PP</sub>		23		MHz	C
Slew rate	$V_{\text{OCM}}$ input = 1 V <sub>STEP</sub>		14		V/ $\mu\text{s}$	C
Gain		0.99	0.996	1.01	V/V	A
Common-mode offset voltage	Offset = output common-mode voltage – $V_{\text{OCM}}$ input voltage		$\pm 1$	$\pm 5$	mV	A
$V_{\text{OCM}}$ input bias current	$V_{\text{OCM}} = (V_{S+} - V_{S-})/2$		$\pm 20$	$\pm 100$	nA	A
$V_{\text{OCM}}$ input voltage range		0.8	0.75 to 1.9	1.75	V	A
$V_{\text{OCM}}$ input impedance			100    1.6		k $\Omega$    pF	C
Default voltage offset from $(V_{S+} - V_{S-})/2$	Offset = output common-mode voltage – $(V_{S+} - V_{S-})/2$		$\pm 3$	$\pm 10$	mV	A

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## ELECTRICAL CHARACTERISTICS: $V_S = 5\text{ V}$

Test conditions at  $T_A = +25^\circ\text{C}$ ,  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2\text{ V}_{PP}$ ,  $R_F = 2\text{ k}\Omega$ ,  $R_L = 2\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, and input and output referenced to mid-supply, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL
AC PERFORMANCE						
Small-signal bandwidth	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 1	36			MHz	C
	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 2	17				
	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 5	6				
	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 10	2.7				
Gain-bandwidth product	V <sub>OUT</sub> = 100 mV <sub>PP</sub> , G = 10	27			MHz	
Large-signal bandwidth	V <sub>OUT</sub> = 2 V <sub>PP</sub> , G = 1	36			MHz	
Bandwidth for 0.1-dB flatness	V <sub>OUT</sub> = 2 V <sub>PP</sub> , G = 1	15			MHz	
Slew rate, rise/fall, 25% to 75%	V <sub>OUT</sub> = 2 V <sub>Step</sub>	220/390			V/μs	
Rise/fall time, 10% to 90%		4.6/5.6			ns	
Settling time to 1%, rise/fall		25/20			ns	
Settling time to 0.1%, rise/fall		60/60			ns	
Settling time to 0.01%, rise/fall		150/110			ns	
Overshoot/undershoot, rise/fall		1/1			%	
2nd-order harmonic distortion		f = 1 kHz, V <sub>OUT</sub> = 1 V <sub>RMS</sub>	−122			
	f = 10 kHz	−128				
	f = 1 MHz	−60				
3rd-order harmonic distortion	f = 1 kHz, V <sub>OUT</sub> = 1 V <sub>RMS</sub>	−130			dBc	
	f = 10 kHz	−137				
	f = 1 MHz	−71				
2nd-order intermodulation distortion	f = 1 MHz, 200-kHz tone spacing, V <sub>OUT</sub> envelope = 2 V <sub>PP</sub>	−85			dBc	
3rd-order intermodulation distortion		−83				
Input voltage noise	f = 1 kHz	10			nV/√Hz	
Voltage noise 1/f corner frequency		45			Hz	
Input current noise	f = 100 kHz	0.25			pA/√Hz	
Current noise 1/f corner frequency		6.5			kHz	
Overdrive recovery time	Overdrive = 0.5 V	65			ns	
Output balance error	V <sub>OUT</sub> = 100 mV, f = 1 MHz	−67			dB	
Closed-loop output impedance	f = 1 MHz (differential)	2.5			Ω	

**ELECTRICAL CHARACTERISTICS:  $V_S = 5\text{ V}$  (continued)**

Test conditions at  $T_A = +25^\circ\text{C}$ ,  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2\text{ V}_{PP}$ ,  $R_F = 2\text{ k}\Omega$ ,  $R_L = 2\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, and input and output referenced to mid-supply, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL
DC PERFORMANCE						
Open-loop voltage gain ( $A_{OL}$ )		100	114		dB	A
Input-referred offset voltage	$T_A = +25^{\circ}\text{C}$		$\pm 100$	$\pm 400$	$\mu\text{V}$	A
	$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$			$\pm 715$		B
	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			$\pm 855$		
	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$			$\pm 1300$		
Input offset voltage drift <sup>(1)</sup>	$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$		$\pm 2$	$\pm 7$	$\mu\text{V}/^{\circ}\text{C}$	B
	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		$\pm 2$	$\pm 7$		
	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$		$\pm 3$	$\pm 9$		
Input bias current	$T_A = +25^{\circ}\text{C}$		200	250	nA	A
	$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$			279		B
	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			292		
	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$			315		
Input bias current drift <sup>(1)</sup>	$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$		0.5	0.65	nA/ $^{\circ}\text{C}$	B
	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		0.5	0.65		
	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$		0.5	0.65		
Input offset current	$T_A = +25^{\circ}\text{C}$		$\pm 5$	$\pm 50$	nA	A
	$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$			$\pm 55$		B
	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			$\pm 57$		
	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$			$\pm 60$		
Input offset current drift <sup>(1)</sup>	$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$		$\pm 0.03$	$\pm 0.1$	nA/ $^{\circ}\text{C}$	B
	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		$\pm 0.03$	$\pm 0.1$		
	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$		$\pm 0.03$	$\pm 0.1$		
INPUT						
Common-mode input: low	$T_A = +25^{\circ}\text{C}$ , CMRR > 87 dB		$V_{S-} - 0.2$	$V_{S-}$	V	A
	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ , CMRR > 87 dB		$V_{S-} - 0.2$	$V_{S-}$		B
Common-mode input: high	$T_A = +25^{\circ}\text{C}$ , CMRR > 87 dB	$V_{S+} - 1.2$	$V_{S+} - 1.1$		V	A
	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ , CMRR > 87 dB	$V_{S+} - 1.2$	$V_{S+} - 1.1$			B
Common-mode rejection ratio		90	116		dB	A
Input impedance common-mode			$200 \parallel 1.2$		$\text{k}\Omega \parallel \text{pF}$	C
Input impedance differential mode			$200 \parallel 1$			C
OUTPUT						
Linear output voltage: low	$T_A = +25^{\circ}\text{C}$		$V_{S-} + 0.1$	$V_{S-} + 0.2$	V	A
	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$		$V_{S-} + 0.1$	$V_{S-} + 0.2$		B
Linear output voltage: high	$T_A = +25^{\circ}\text{C}$	$V_{S+} - 0.25$	$V_{S+} - 0.12$			A
	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	$V_{S+} - 0.25$	$V_{S+} - 0.12$			B
Output saturation voltage: high/low			120/100		mV	C
Linear output current drive	$T_A = +25^{\circ}\text{C}$	$\pm 15$	$\pm 25$		mA	A
	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	$\pm 15$				B

(1) Input offset voltage drift, input bias current drift, and input offset current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

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## ELECTRICAL CHARACTERISTICS: $V_S = 5\text{ V}$ (continued)

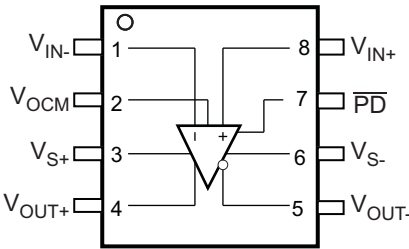
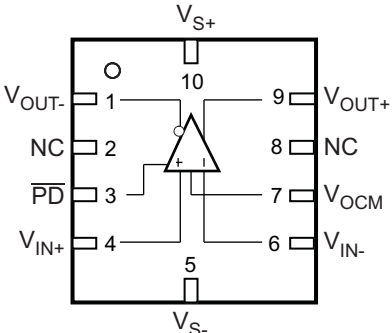
Test conditions at  $T_A = +25^\circ\text{C}$ ,  $V_{S+} = 5\text{ V}$ ,  $V_{S-} = 0\text{ V}$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2\text{ V}_{PP}$ ,  $R_F = 2\text{ k}\Omega$ ,  $R_L = 2\text{ k}\Omega$  differential,  $G = 1\text{ V/V}$ , single-ended input, differential output, and input and output referenced to mid-supply, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL
POWER SUPPLY						
Specified operating voltage		2.5		5.5	V	B
Quiescent operating current/ch	T <sub>A</sub> = 25°C, $\overline{PD} = V_{S+}$		250	350	μA	A
	T <sub>A</sub> = −40°C to 125°C, $\overline{PD} = V_{S+}$		290	390		B
Power-supply rejection (PSRR)		87	108		dB	A
POWER DOWN						
Enable voltage threshold	Specified on above 2.1 V			2.1	V	A
Disable voltage threshold	Specified off below 0.7 V	0.7				A
Disable pin bias current	$\overline{PD} = V_{S-} + 0.5\text{ V}$		50	500	nA	A
Power-down quiescent current	$\overline{PD} = V_{S-} + 0.5\text{ V}$		0.5	2	μA	A
Turn-on time delay	Time from $\overline{PD} = \text{high}$ to V <sub>OUT</sub> = 90% of final value, R <sub>L</sub> = 200 Ω		600		ns	C
Turn-off time delay	Time from $\overline{PD} = \text{low}$ to V <sub>OUT</sub> = 10% of original value, R <sub>L</sub> = 200 Ω		15			
OUTPUT COMMON-MODE VOLTAGE CONTROL (V <sub>OCM</sub> )						
Small-signal bandwidth	V <sub>OCM</sub> input = 100 mV <sub>PP</sub>		24		MHz	C
Slew rate	V <sub>OCM</sub> input = 1 V <sub>STEP</sub>		15		V/μs	C
Gain		0.99	0.996	1.01	V/V	A
Common-mode offset voltage	Offset = output common-mode voltage – V <sub>OCM</sub> input voltage		±1	±5	mV	A
V <sub>OCM</sub> input bias current	V <sub>OCM</sub> = (V <sub>S+</sub> – V <sub>S–</sub> )/2		±20	±120	nA	A
V <sub>OCM</sub> input voltage range		0.95	0.75 to 4.15	4.0	V	A
V <sub>OCM</sub> input impedance			65    0.86		kΩ    pF	C
Default voltage offset from (V <sub>S+</sub> – V <sub>S–</sub> )/2	Offset = output common-mode voltage – (V <sub>S+</sub> – V <sub>S–</sub> )/2		±3	±10	mV	A



## DEVICE INFORMATION

### PIN CONFIGURATIONS

THS4531A	THS4531A
SOIC-8 (D), VSSOP-8 (DGK) PACKAGE (TOP VIEW)	WQFN-10 (RUN) PACKAGE (TOP VIEW)
	

### PIN FUNCTIONS

NUMBER	NAME	DESCRIPTION
<b>THS4531A D, DGK PACKAGE</b>		
1	V <sub>IN-</sub>	Inverted (negative) output feedback
2	V <sub>OCM</sub>	Common-mode voltage input
3	V <sub>S+</sub>	Amplifier positive power-supply input
4	V <sub>OUT+</sub>	Noninverted amplifier output
5	V <sub>OUT-</sub>	Inverted amplifier output
6	V <sub>S-</sub>	Amplifier negative power-supply input. Note V <sub>S-</sub> tied together on multichannel devices.
7	$\overline{\text{PD}}$	Power-down, $\overline{\text{PD}}$ = logic low = low power mode, $\overline{\text{PD}}$ = logic high = normal operation ( <b>PIN MUST BE DRIVEN</b> )
8	V <sub>IN+</sub>	Noninverted amplifier input
<b>THS4531A RUN PACKAGE</b>		
1	V <sub>OUT-</sub>	Inverted amplifier output
2, 8	NC	No internal connection
3	$\overline{\text{PD}}$	Power-down, $\overline{\text{PD}}$ = logic low = low power mode, $\overline{\text{PD}}$ = logic high = normal operation ( <b>PIN MUST BE DRIVEN</b> )
4	V <sub>IN+</sub>	Noninverted amplifier input
5	V <sub>S-</sub>	Amplifier negative power-supply input. Note V <sub>S-</sub> tied together on multichannel devices.
6	V <sub>IN-</sub>	Inverting amplifier input
7	V <sub>OCM</sub>	Common-mode voltage input
9	V <sub>OUT+</sub>	Noninverted amplifier output
10	V <sub>S+</sub>	Amplifier positive power-supply input

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## TYPICAL CHARACTERISTICS: $V_S = 2.7V$

Test conditions unless otherwise noted:  $V_{S+} = 2.7V$ ,  $V_{S-} = 0V$ , CM = open,  $V_{OUT} = 2V_{pp}$ ,  $R_F = 2k\Omega$ ,  $R_L = 2k\Omega$  Differential,  $G = 1V/V$ , Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply unless otherwise noted.

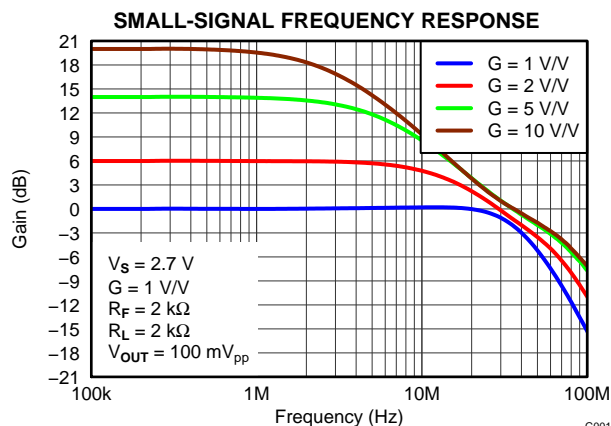


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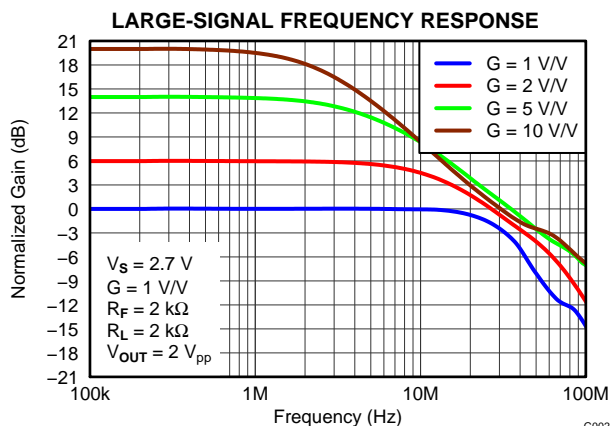


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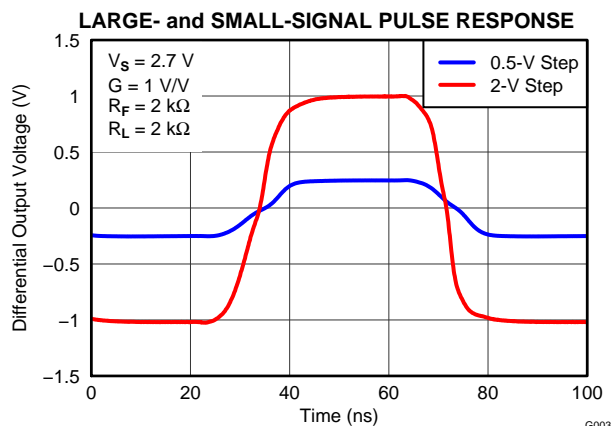


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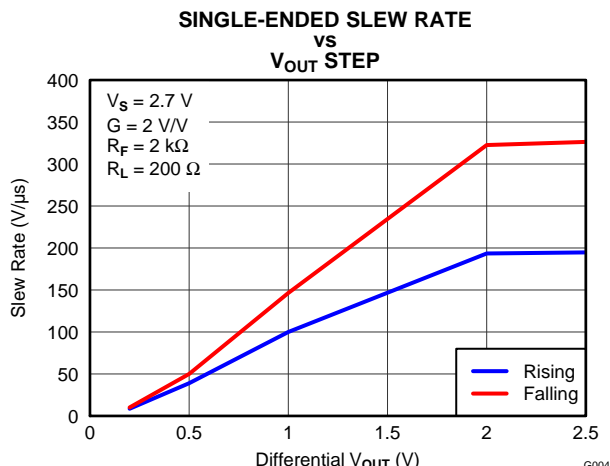


Figure 5.

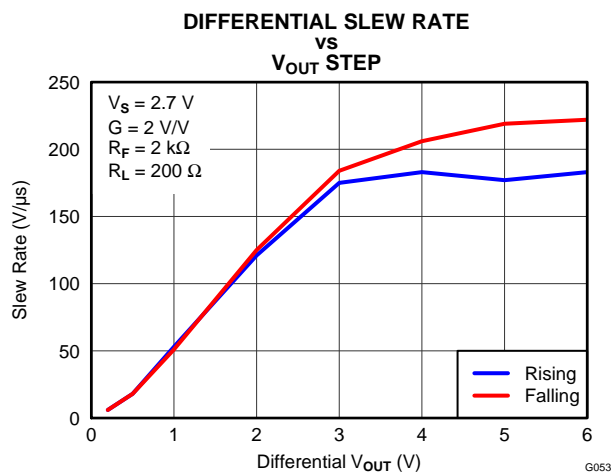


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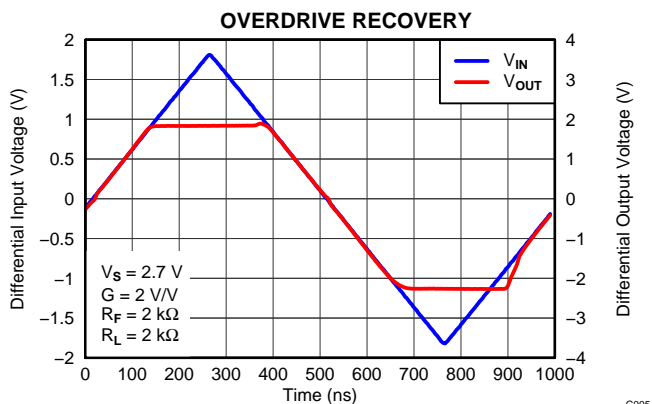
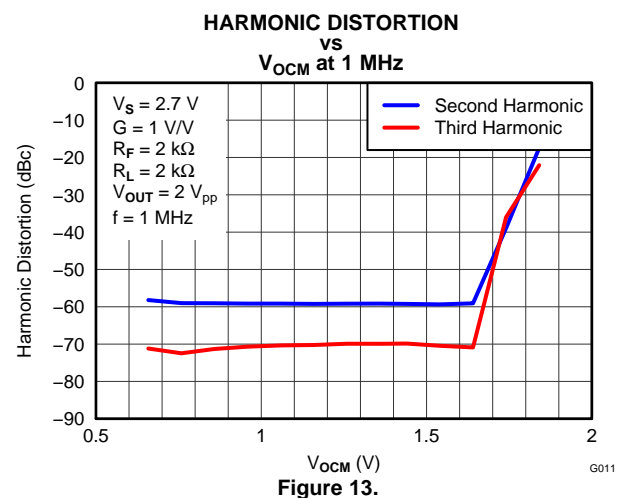
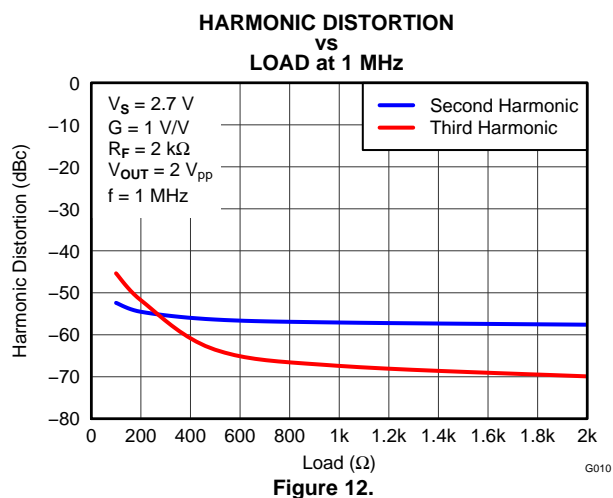
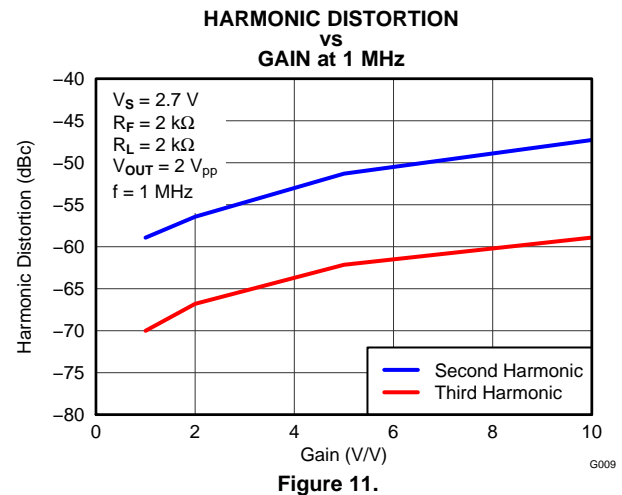
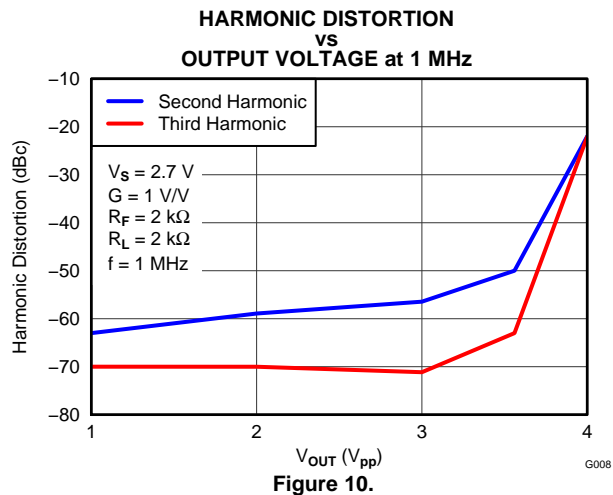
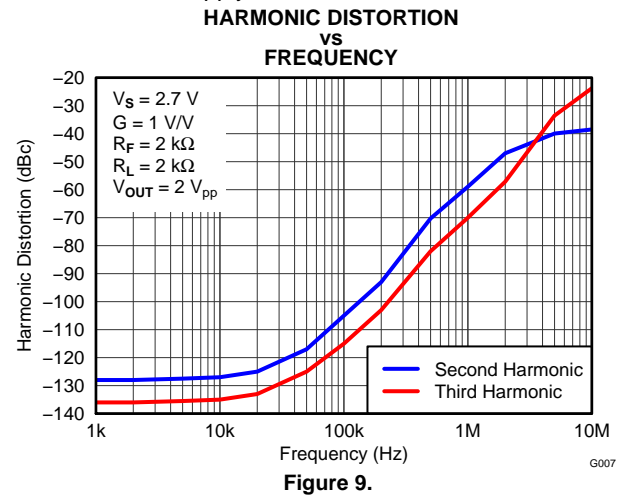
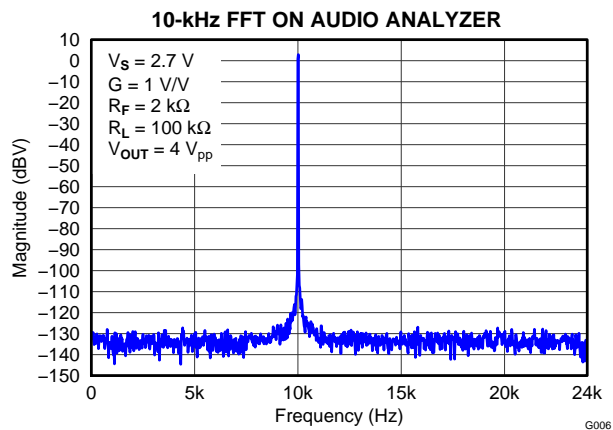


Figure 7.

## TYPICAL CHARACTERISTICS: $V_S = 2.7V$ (continued)

Test conditions unless otherwise noted:  $V_{S+} = 2.7V$ ,  $V_{S-} = 0V$ , CM = open,  $V_{OUT} = 2V_{pp}$ ,  $R_F = 2k\Omega$ ,  $R_L = 2k\Omega$  Differential,  $G = 1V/V$ , Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply unless otherwise noted.



# TYPICAL CHARACTERISTICS: $V_S = 2.7V$ (continued)

Test conditions unless otherwise noted:  $V_{S+} = 2.7V$ ,  $V_{S-} = 0V$ , CM = open,  $V_{OUT} = 2V_{pp}$ ,  $R_F = 2k\Omega$ ,  $R_L = 2k\Omega$  Differential,  $G = 1V/V$ , Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply unless otherwise noted.

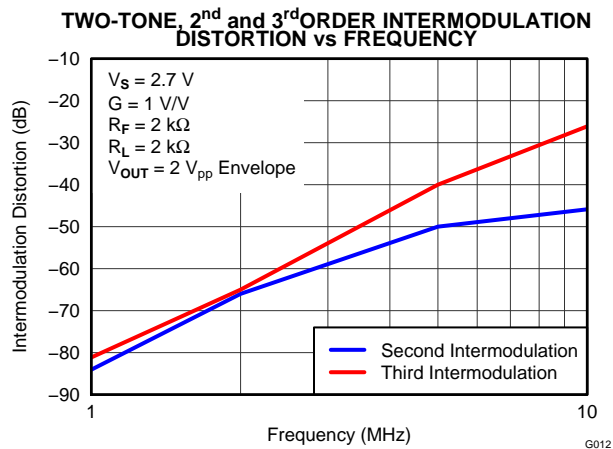


Figure 14.

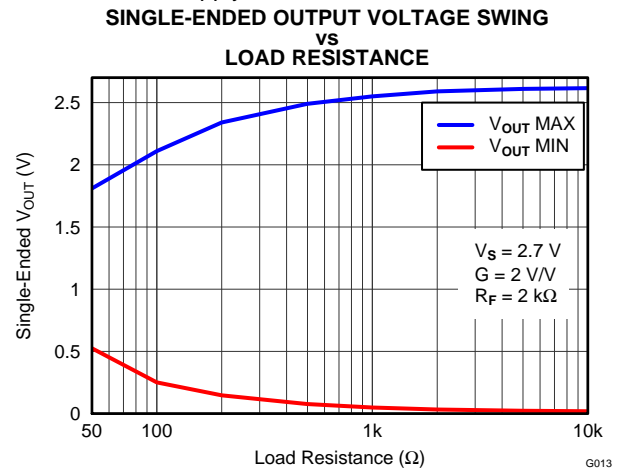


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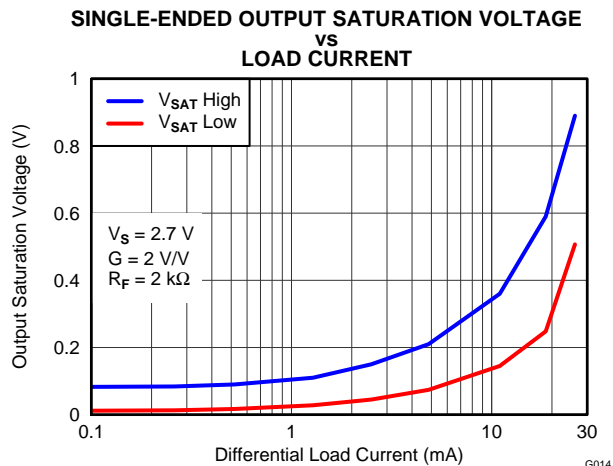


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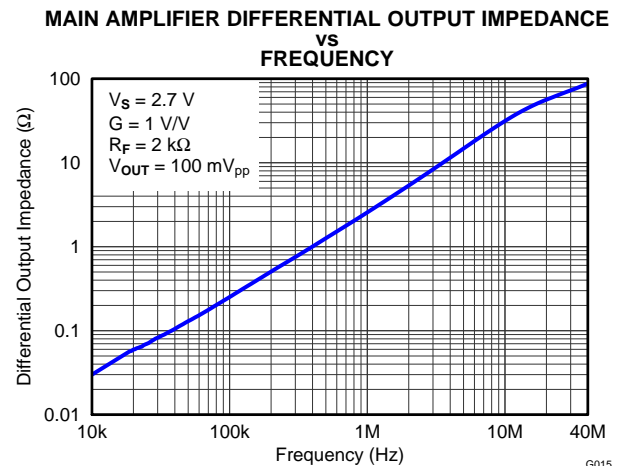


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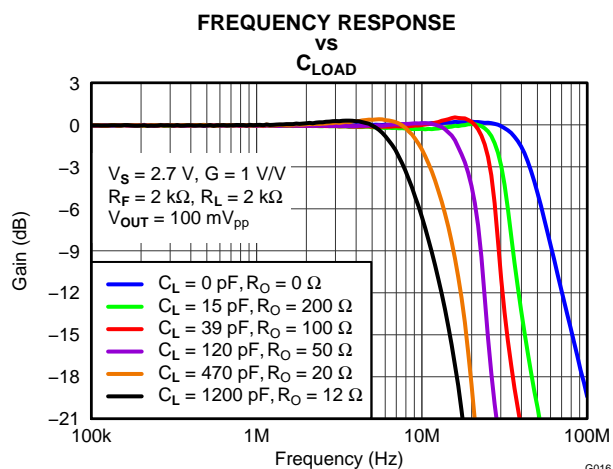


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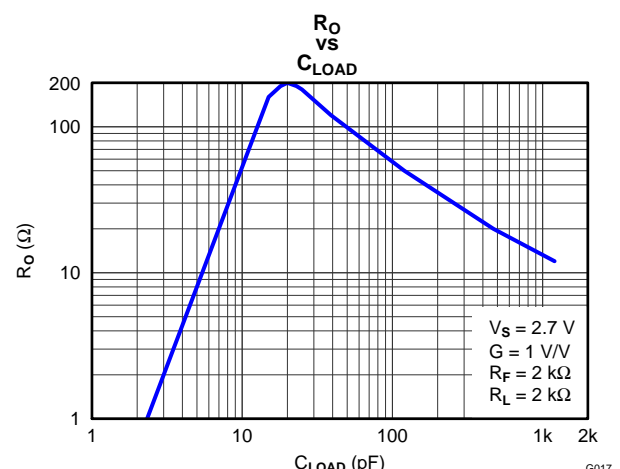
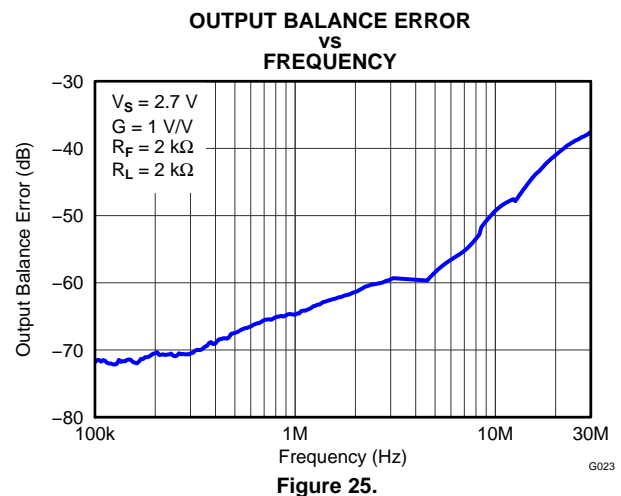
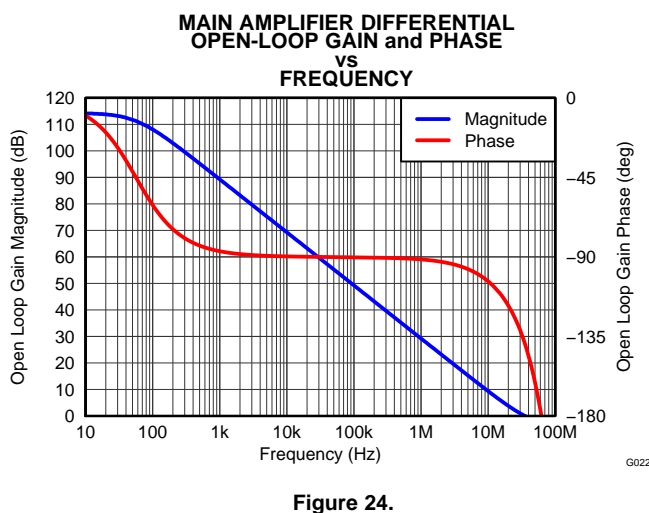
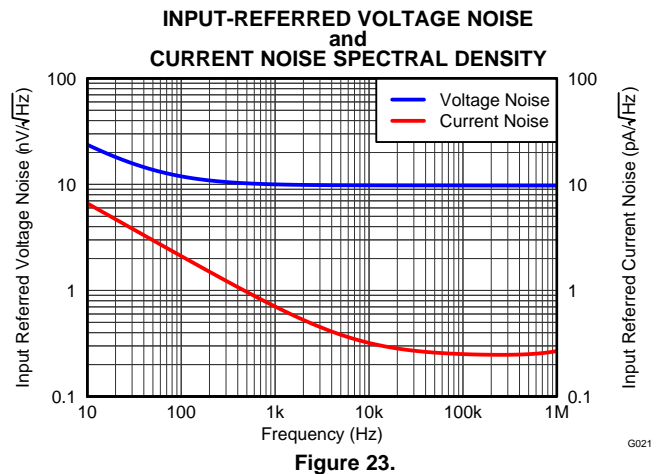
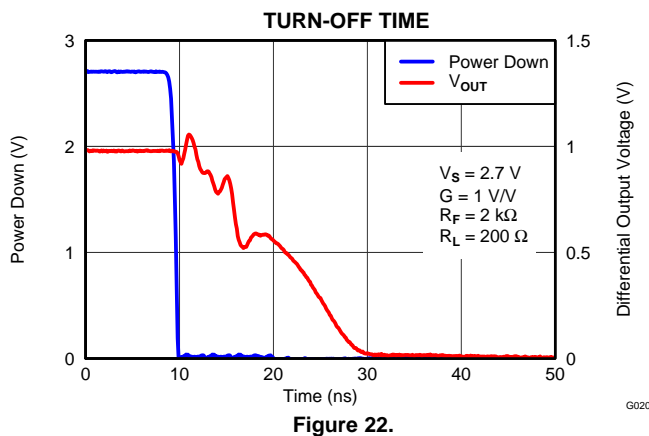
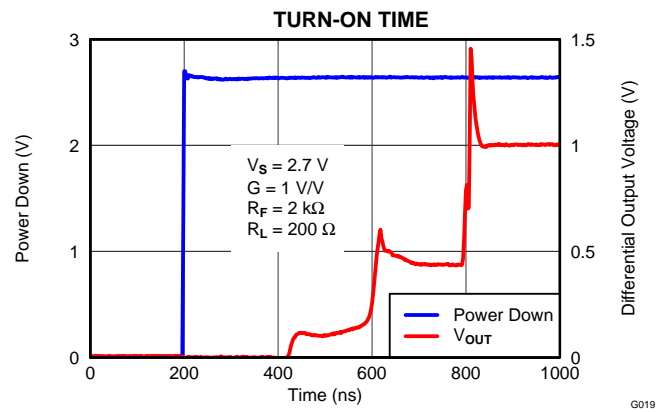
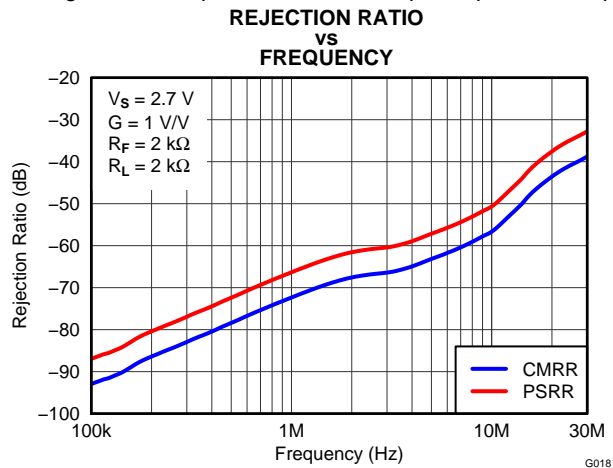


Figure 19.

## TYPICAL CHARACTERISTICS: $V_S = 2.7V$ (continued)

Test conditions unless otherwise noted:  $V_{S+} = 2.7V$ ,  $V_{S-} = 0V$ , CM = open,  $V_{OUT} = 2V_{pp}$ ,  $R_F = 2k\Omega$ ,  $R_L = 2k\Omega$  Differential,  $G = 1V/V$ , Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply unless otherwise noted.



# TYPICAL CHARACTERISTICS: $V_S = 2.7V$ (continued)

Test conditions unless otherwise noted:  $V_{S+} = 2.7V$ ,  $V_{S-} = 0V$ , CM = open,  $V_{OUT} = 2V_{pp}$ ,  $R_F = 2k\Omega$ ,  $R_L = 2k\Omega$  Differential,  $G = 1V/V$ , Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply unless otherwise noted.

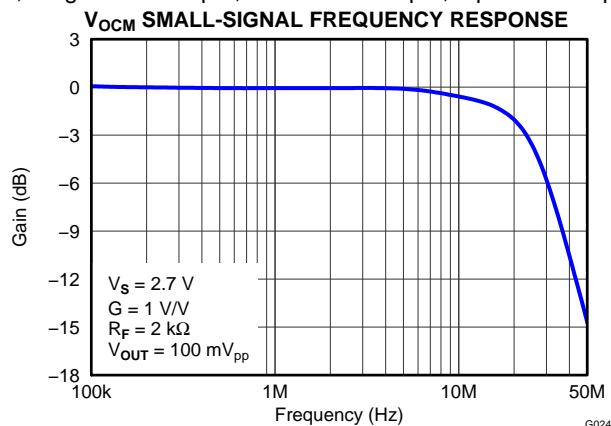


Figure 26.

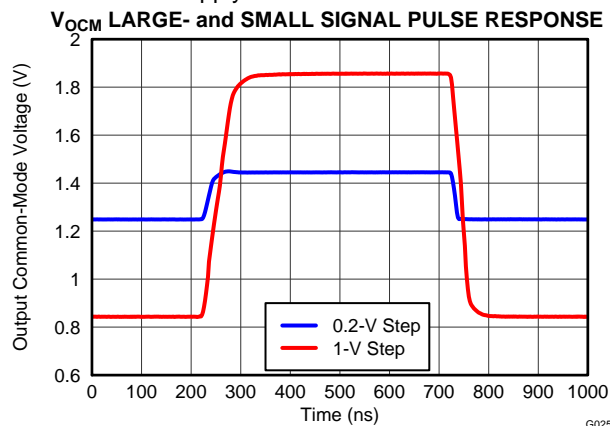


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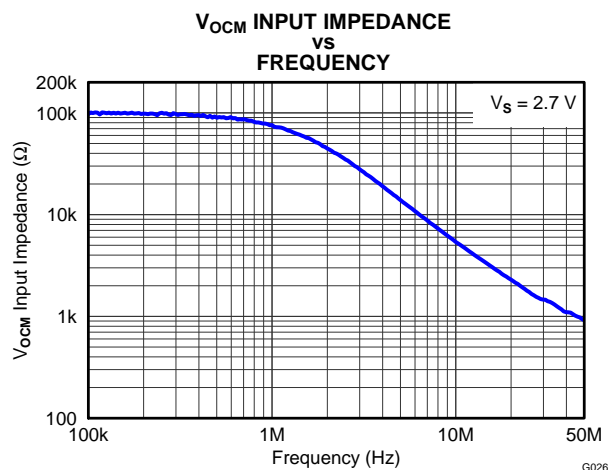


Figure 28.

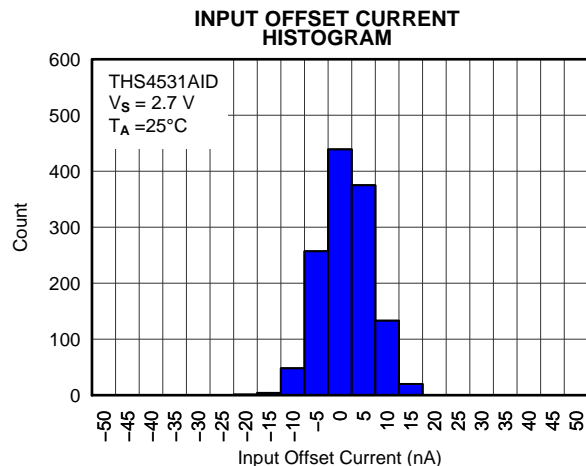


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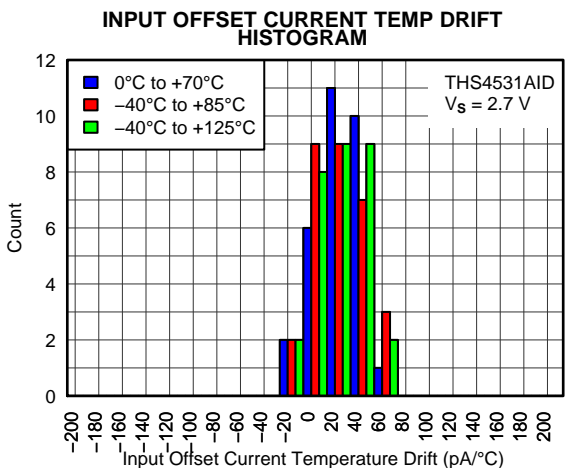


Figure 30.

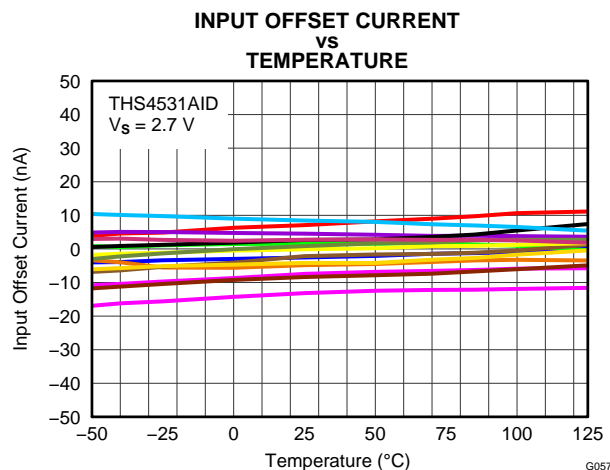


Figure 31.

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## TYPICAL CHARACTERISTICS: $V_S = 2.7V$ (continued)

Test conditions unless otherwise noted:  $V_{S+} = 2.7V$ ,  $V_{S-} = 0V$ , CM = open,  $V_{OUT} = 2V_{pp}$ ,  $R_F = 2k\Omega$ ,  $R_L = 2k\Omega$  Differential, G = 1V/V, Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply unless otherwise noted.

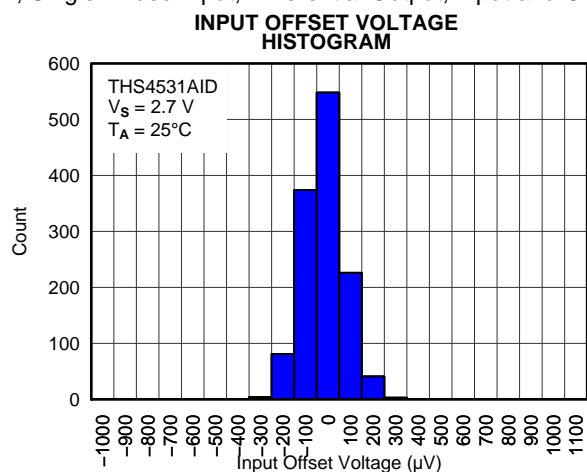


Figure 32.

G058

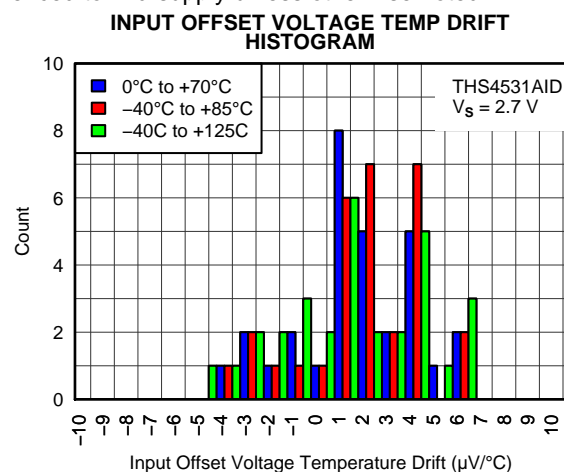


Figure 33.

G059

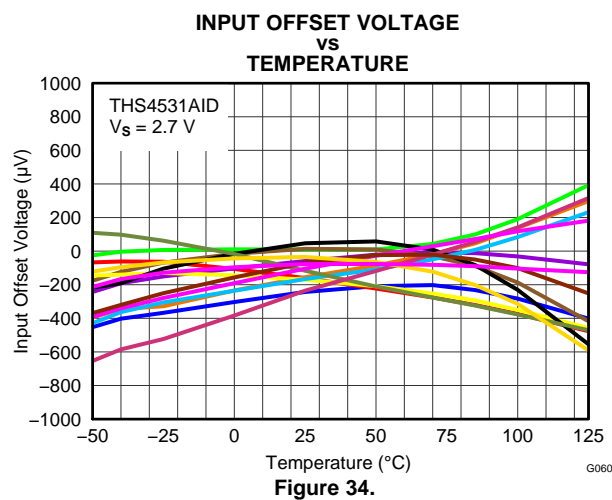


Figure 34.

G060



## TYPICAL CHARACTERISTICS: $V_S = 5V$

Test conditions unless otherwise noted:  $V_{S+} = 5V$ ,  $V_{S-} = 0V$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2V_{pp}$ ,  $R_F = 2k\Omega$ ,  $R_L = 2k\Omega$  Differential,  $G = 1V/V$ , Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply,  $T_A = 25^\circ\text{C}$  unless otherwise noted.

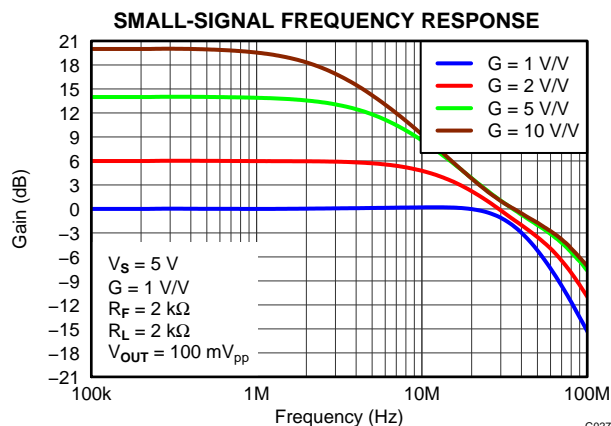


Figure 35.

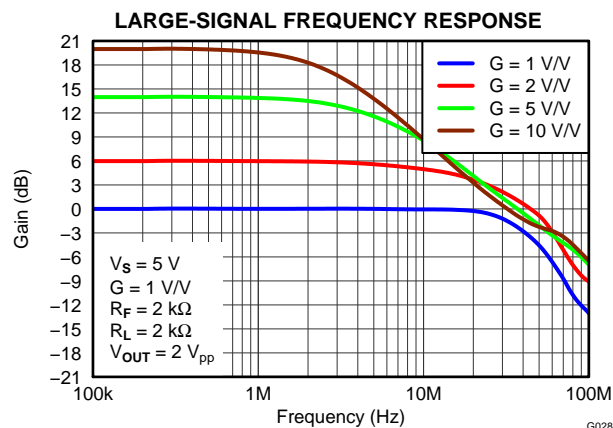


Figure 36.

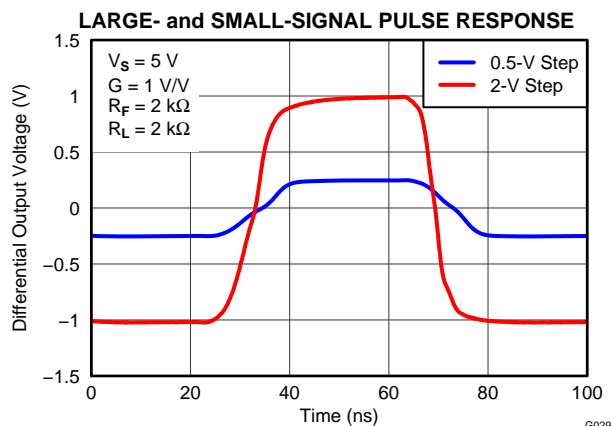


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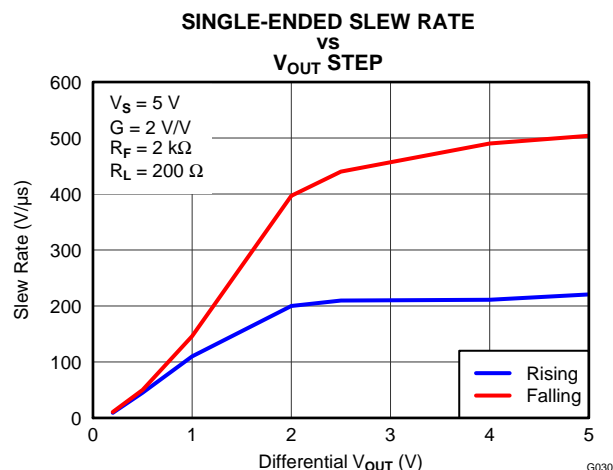


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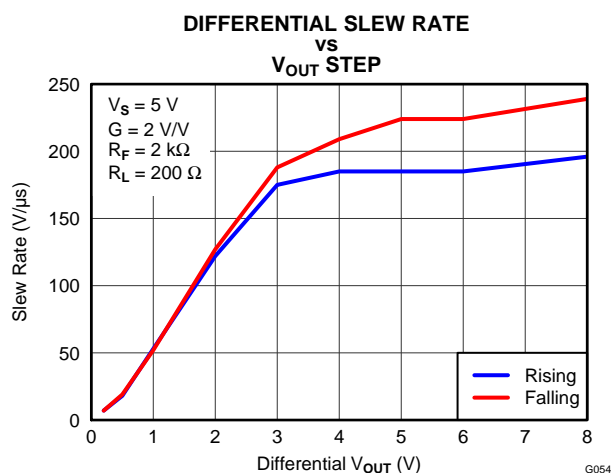


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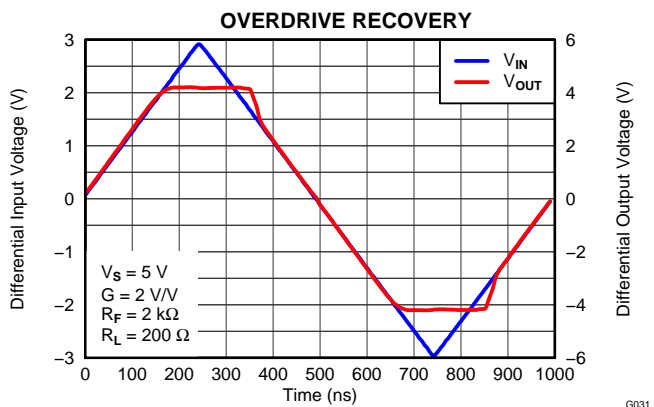
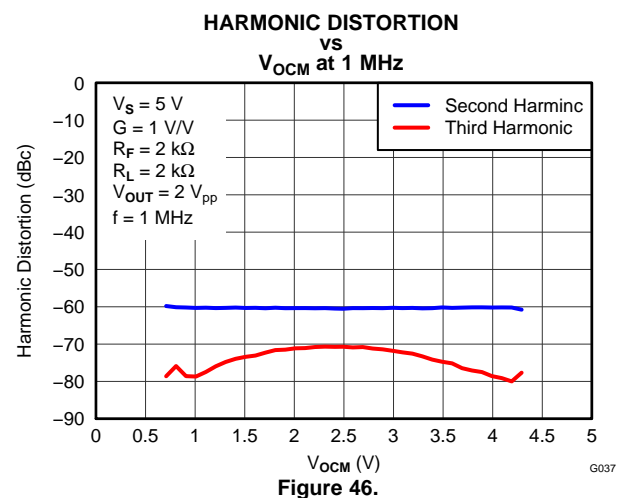
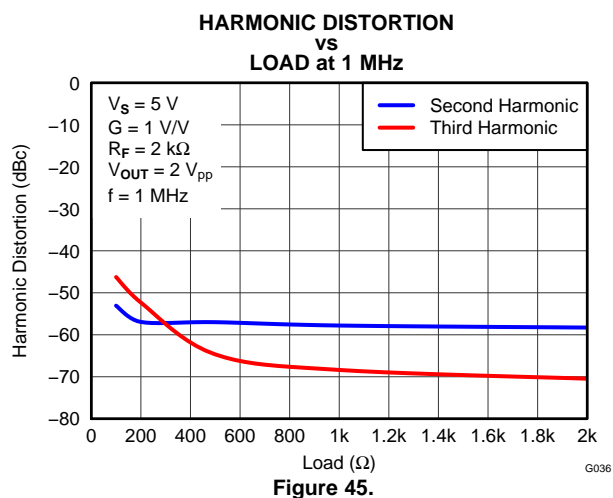
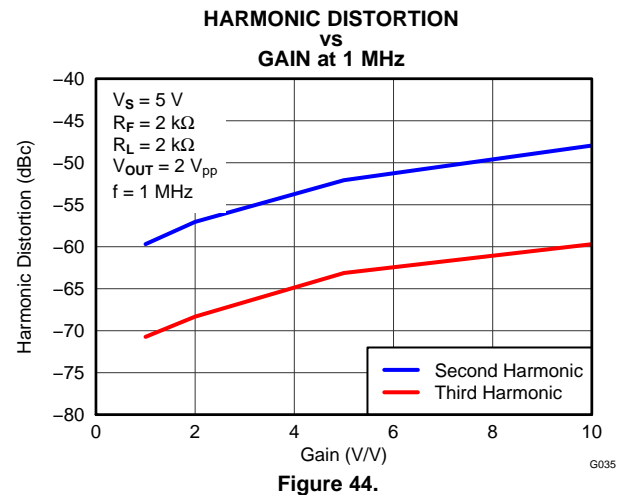
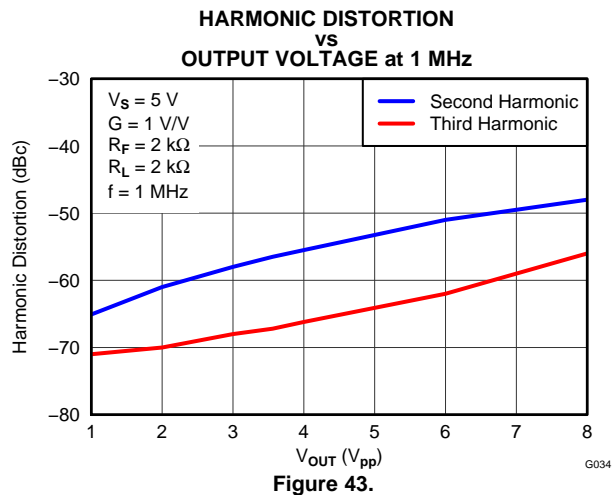
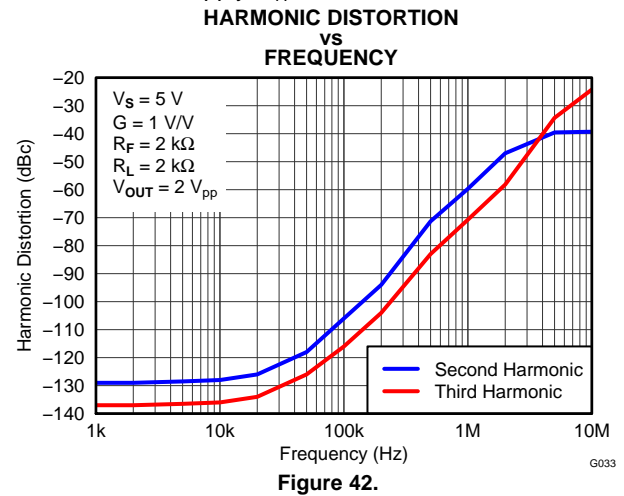
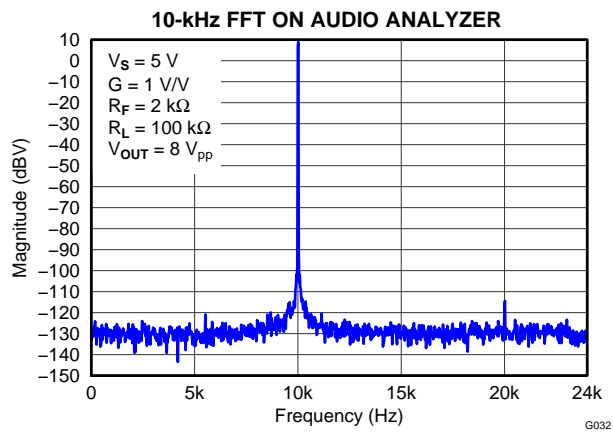


Figure 40.

## TYPICAL CHARACTERISTICS: $V_S = 5V$ (continued)

Test conditions unless otherwise noted:  $V_{S+} = 5V$ ,  $V_{S-} = 0V$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2V_{pp}$ ,  $R_F = 2k\Omega$ ,  $R_L = 2k\Omega$  Differential,  $G = 1V/V$ , Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply,  $T_A = 25^\circ\text{C}$  unless otherwise noted.



## TYPICAL CHARACTERISTICS: $V_S = 5V$ (continued)

Test conditions unless otherwise noted:  $V_{S+} = 5V$ ,  $V_{S-} = 0V$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2V_{pp}$ ,  $R_F = 2k\Omega$ ,  $R_L = 2k\Omega$  Differential,  $G = 1V/V$ , Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply,  $T_A = 25^\circ\text{C}$  unless otherwise noted.

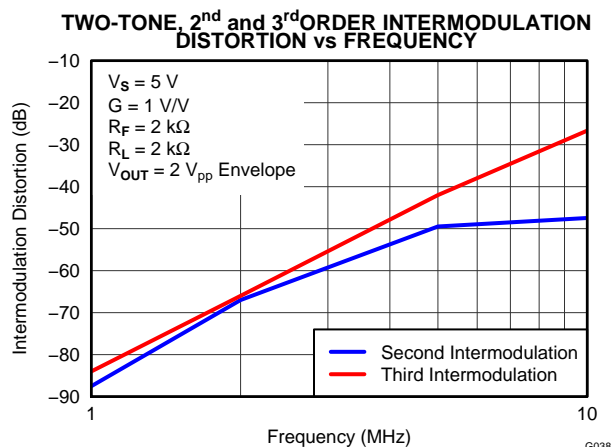


Figure 47.

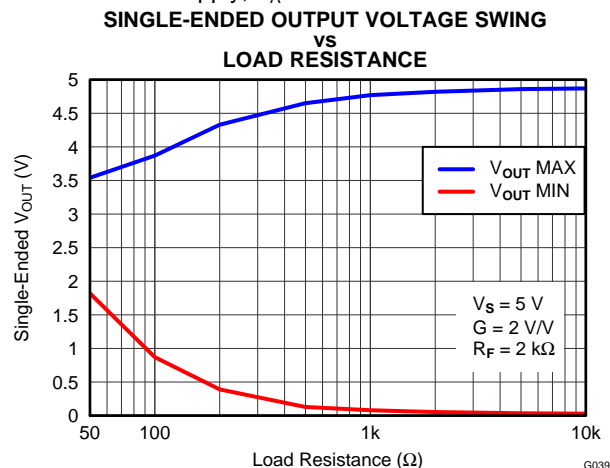


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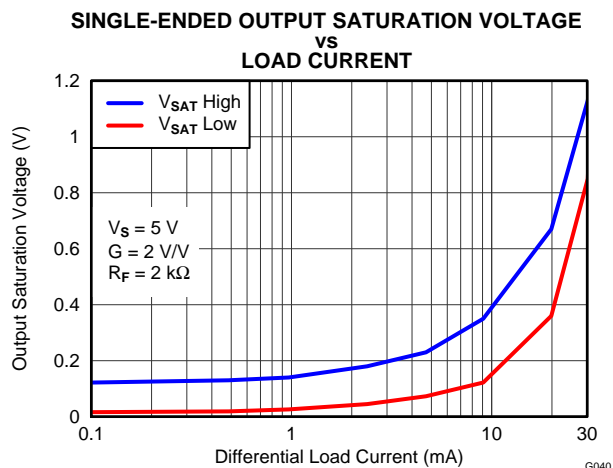


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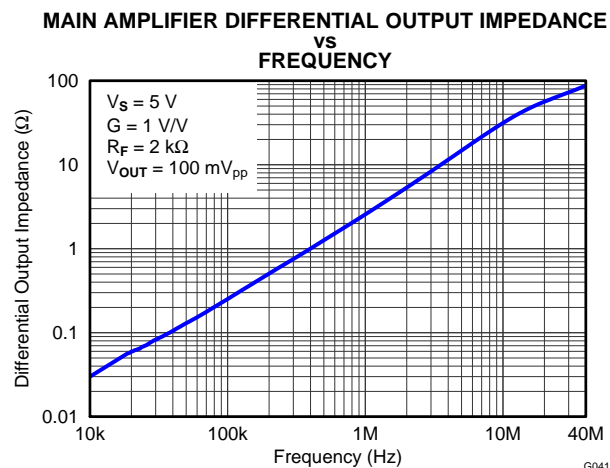


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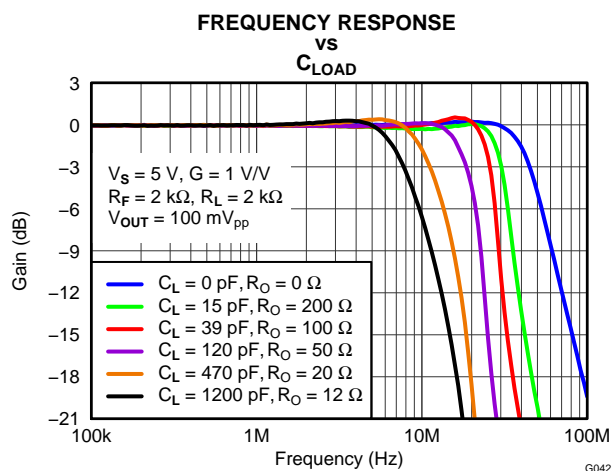


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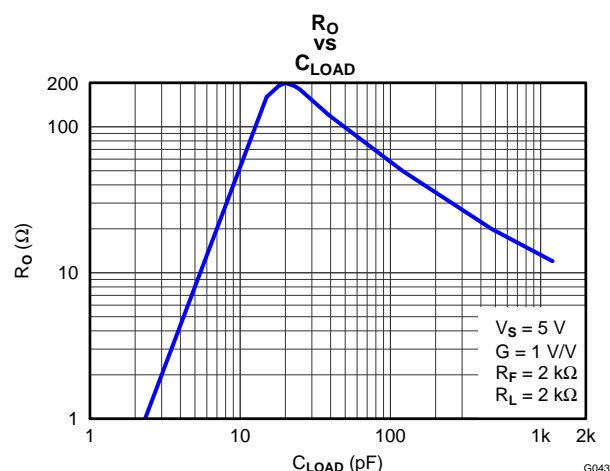
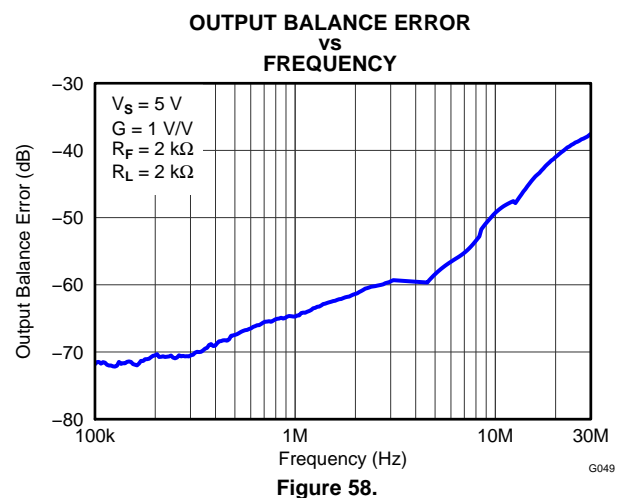
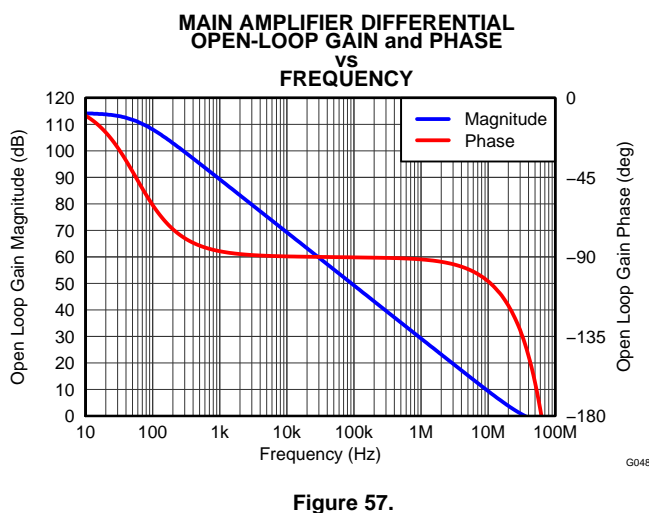
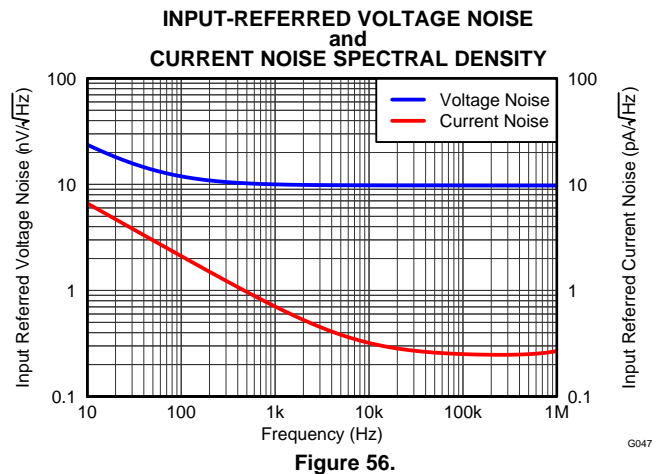
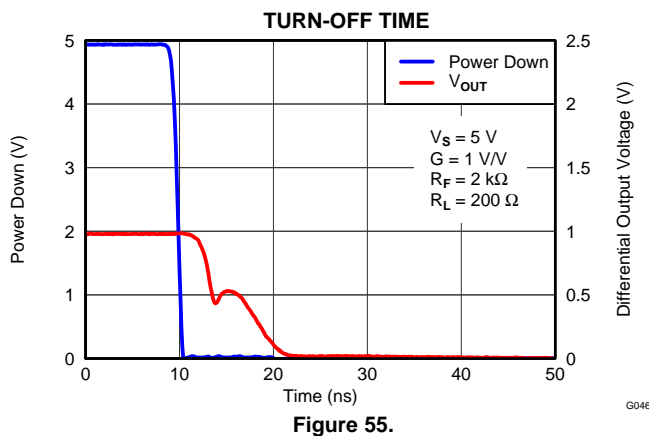
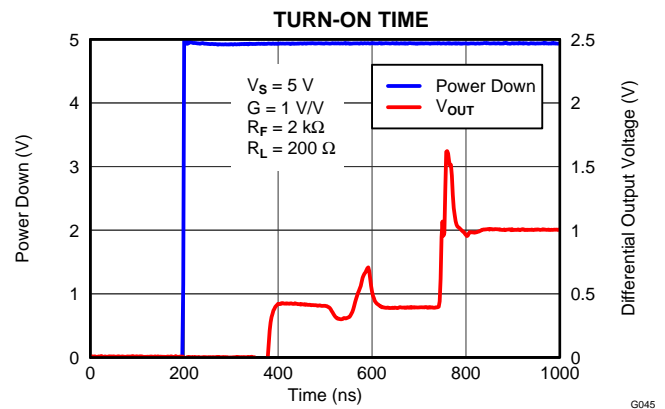
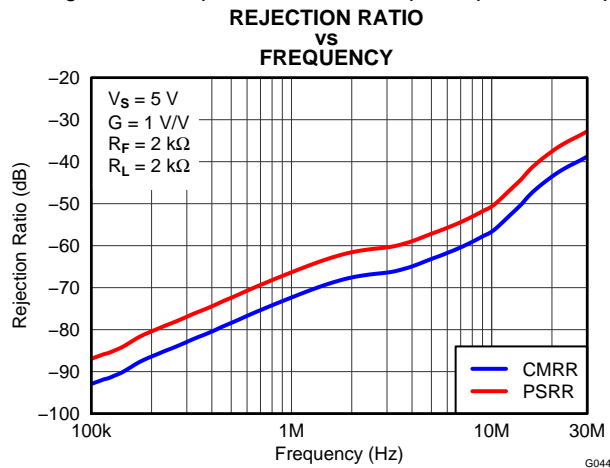


Figure 52.

## TYPICAL CHARACTERISTICS: $V_S = 5V$ (continued)

Test conditions unless otherwise noted:  $V_{S+} = 5V$ ,  $V_{S-} = 0V$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2V_{pp}$ ,  $R_F = 2k\Omega$ ,  $R_L = 2k\Omega$  Differential,  $G = 1V/V$ , Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply,  $T_A = 25^\circ\text{C}$  unless otherwise noted.



# TYPICAL CHARACTERISTICS: $V_S = 5V$ (continued)

Test conditions unless otherwise noted:  $V_{S+} = 5V$ ,  $V_{S-} = 0V$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2V_{pp}$ ,  $R_F = 2k\Omega$ ,  $R_L = 2k\Omega$  Differential,  $G = 1V/V$ , Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply,  $T_A = 25^\circ\text{C}$  unless otherwise noted.

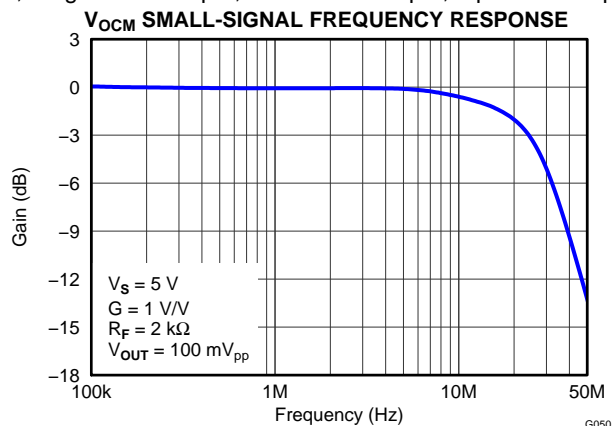


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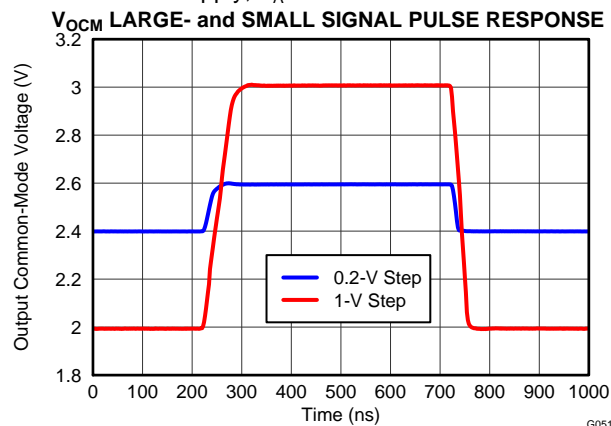


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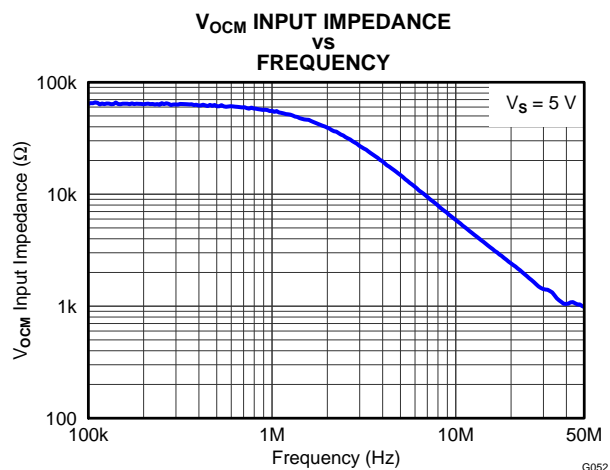


Figure 61.

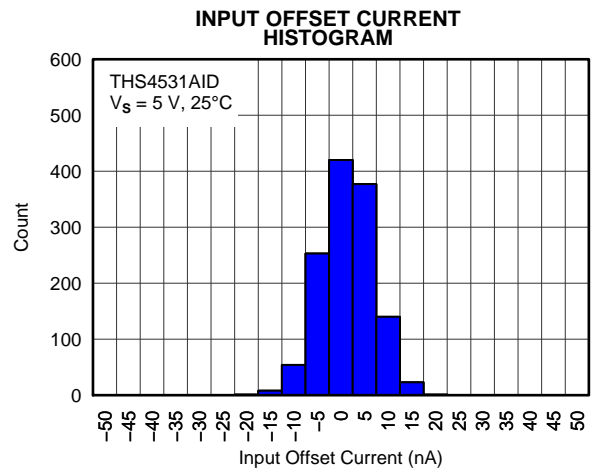


Figure 62.

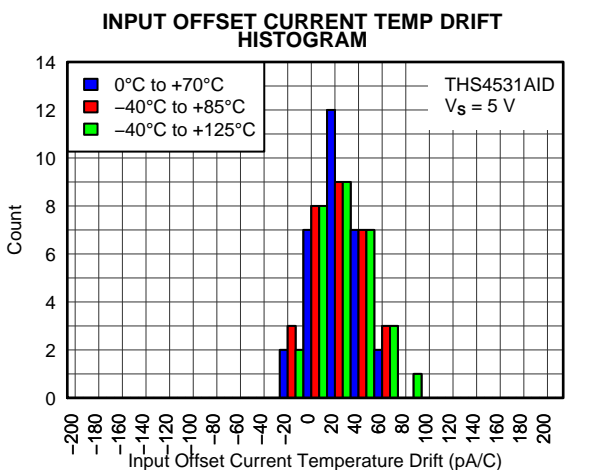


Figure 63.

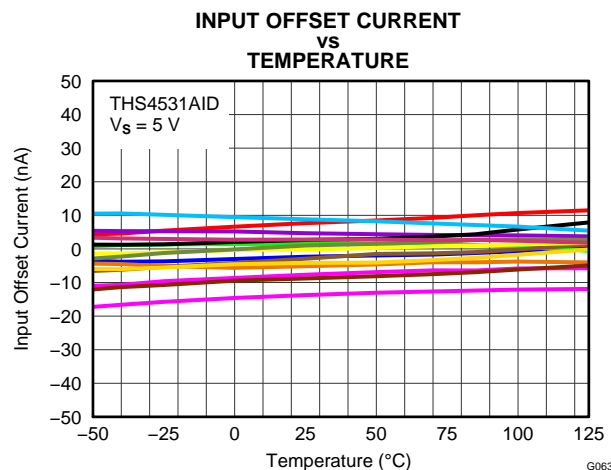


Figure 64.

## TYPICAL CHARACTERISTICS: $V_S = 5V$ (continued)

Test conditions unless otherwise noted:  $V_{S+} = 5V$ ,  $V_{S-} = 0V$ ,  $V_{OCM} = \text{open}$ ,  $V_{OUT} = 2V_{pp}$ ,  $R_F = 2k\Omega$ ,  $R_L = 2k\Omega$  Differential,  $G = 1V/V$ , Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply,  $T_A = 25^\circ\text{C}$  unless otherwise noted.

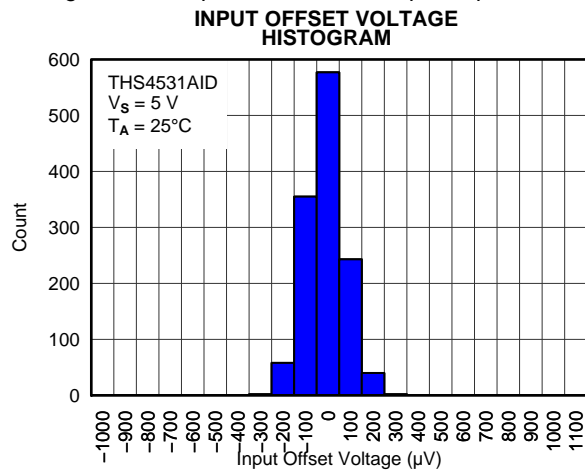


Figure 65.

G064

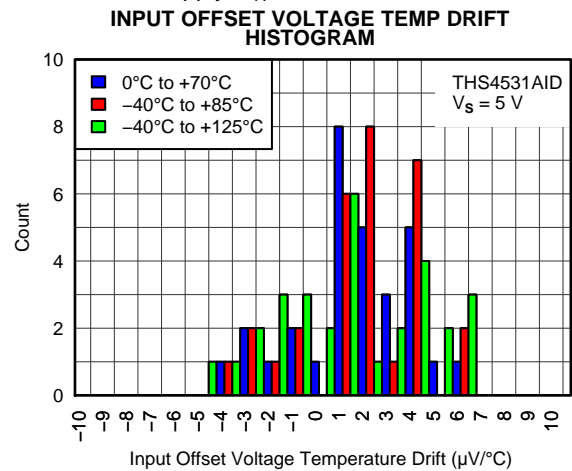


Figure 66.

G065

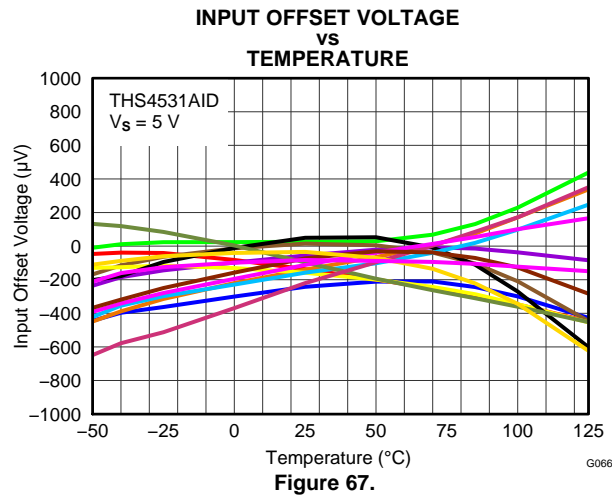


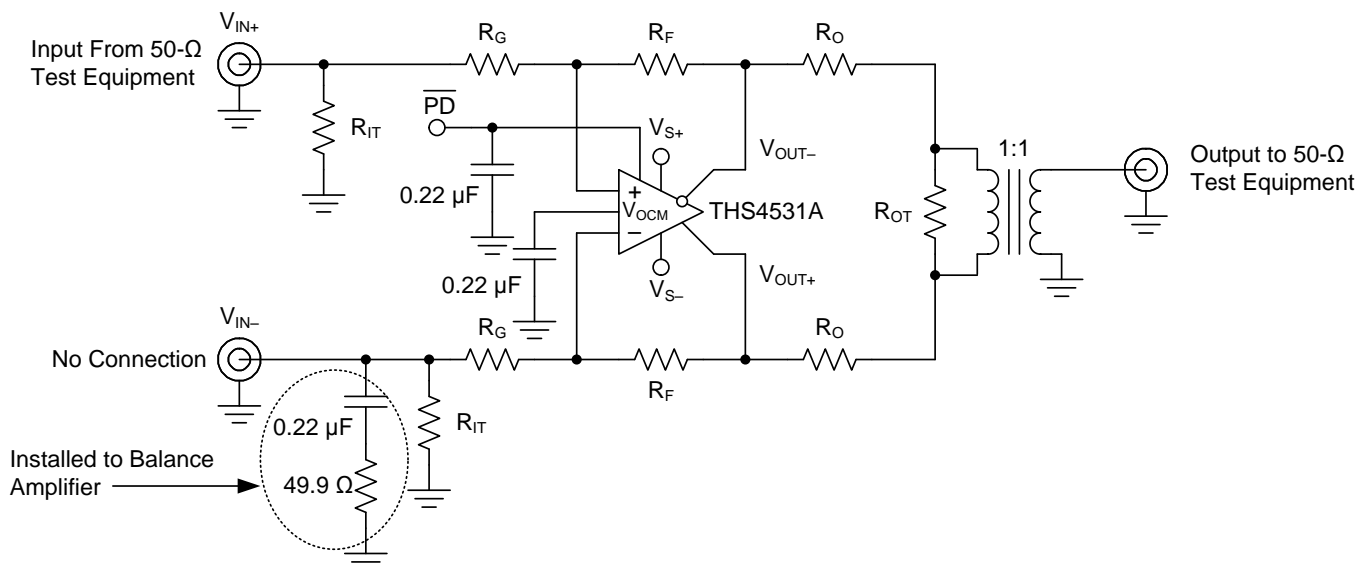
Figure 67.

G066

## APPLICATION INFORMATION

### TYPICAL CHARACTERISTICS TEST CIRCUITS

Figure 68 shows the general test circuit built on the EVM that was used for testing the THS4531A. For simplicity, power supply decoupling is not shown – please see layout in the applications section for recommendations. Depending on the test conditions, component values are changed per Table 2 and Table 3, or as otherwise noted. Some of the signal generators used are ac coupled 50Ω sources and a 0.22μF cap and 49.9Ω resistor to ground are inserted across  $R_{IT}$  on the un-driven or alternate input as shown to balance the circuit. Split-power supply is used to ease the interface to common lab test equipment, but if properly biased, the amplifier can be operated single-supply as described in the applications section with no impact on performance. For most of the tests, the devices are tested with single ended input and a transformer on the output to convert the differential output to single ended because common lab test equipment have single ended inputs and outputs. Performance is the same or better with differential input and differential output.



**Figure 68. General Test Circuit**

**Table 2. Gain Component Values for Single-Ended Input<sup>(1)</sup>**

GAIN	$R_F$	$R_G$	$R_{IT}$
1 V/V	2kΩ	2kΩ	51.1Ω
2 V/V	2kΩ	1kΩ	52.3Ω
5 V/V	2kΩ	392Ω	53.6Ω
10 V/V	2kΩ	187kΩ	57.6Ω

(1) Note components are chosen to achieve gain and 50Ω input termination. Resistor values shown are closest standard values so gains are approximate.

**Table 3. Load Component Values For 1:1 Differential to Single-Ended Output Transformer<sup>(1)</sup>**

$R_L$	$R_O$	$R_{OT}$	ATTEN
100Ω	25Ω	open	6
200Ω	86.6Ω	69.8Ω	16.8
499Ω	237Ω	56.2Ω	25.5
1kΩ	487Ω	52.3Ω	31.8
2kΩ	976Ω	51.1Ω	37.9

(1) Note the total load includes 50Ω termination by the test equipment. Components are chosen to achieve load and 50Ω line termination through a 1:1 transformer. Resistor values shown are closest standard values so loads are approximate.

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Due to the voltage divider on the output formed by the load component values, the amplifier's output is attenuated. The column "Atten" in [Table 3](#) shows the attenuation expected from the resistor divider. When using a transformer at the output as shown in [Figure 68](#), the signal will see slightly more loss due to transformer and line loss, and these numbers will be approximate. The standard output load used for most tests is 2k $\Omega$  with associated 37.9dB of loss.

## Frequency Response, and Output Impedance

The circuit shown in [Figure 68](#) is used to measure the frequency response of the amplifier.

A network analyzer is used as the signal source and the measurement device. The output impedance of the network analyzer is 50 $\Omega$  and is DC coupled.  $R_{IT}$  and  $R_G$  are chosen to impedance match to 50 $\Omega$  and maintain the proper gain. To balance the amplifier, a 49.9 $\Omega$  resistor to ground is inserted across  $R_{IT}$  on the alternate input.

The output is routed to the input of the network analyzer via 50 $\Omega$  coax. For 2k load, 37.9dB is added to the measurement to refer back to the amplifier's output per [Table 3](#).

For output impedance, the signal is injected at  $V_{OUT}$  with  $V_{IN}$  left open. The voltage drop across the 2x  $R_O$  resistors is measured with a high impedance differential probe and used to calculate the impedance seen looking into the amplifier's output.

## Distortion

At 1MHz and above, the circuit shown in [Figure 68](#) is used to measure harmonic, intermodulation distortion, and output impedance of the amplifier.

A signal generator is used as the signal source and the output is measured with a spectrum analyzer. The output impedance of the signal generator is 50 $\Omega$  and is AC coupled.  $R_{IT}$  and  $R_G$  are chosen to impedance match to 50 $\Omega$  and maintain the proper gain. To balance the amplifier, a 0.22 $\mu$ F cap and 49.9 $\Omega$  resistor to ground is inserted across  $R_{IT}$  on the alternate input. A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured and then a high-pass filter is inserted at the output to reduce the fundamental so it does not generate distortion in the input of the spectrum analyzer.

Distortion in the audio band is measured using an audio analyzer. Refer to audio measurement section for detail.

## Slew Rate, Transient Response, Settling Time, Overdrive, Output Voltage, and Turn-On/Off Time

The circuit shown in [Figure 69](#) is used to measure slew rate, transient response, settling time, overdrive recovery, and output voltage swing. Turn on and turn off times are measured with 50 $\Omega$  input termination on the  $\overline{PD}$  input, by replacing the 0.22 $\mu$ F capacitor with 49.9 $\Omega$  resistor.

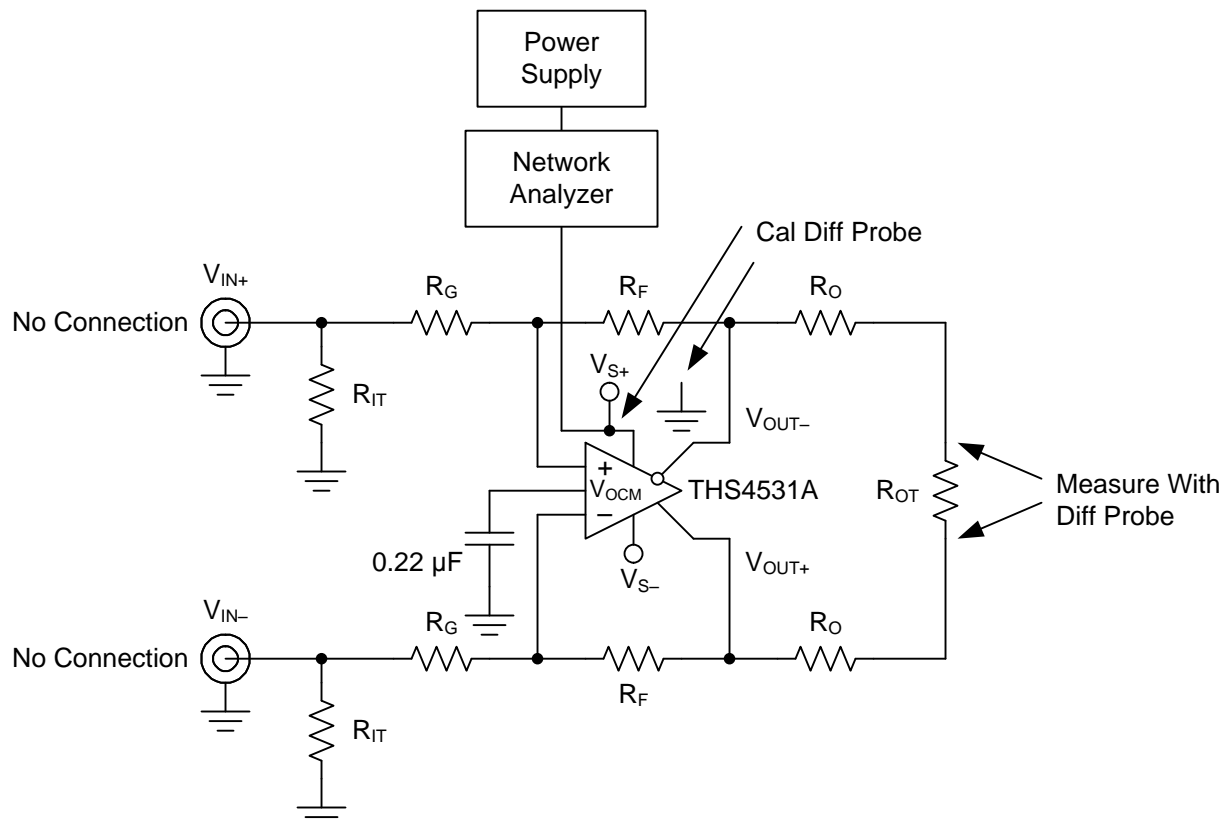




The circuit shown in [Figure 70](#) is used to measure the CMRR. The signal from the network analyzer is applied common-mode to the input.

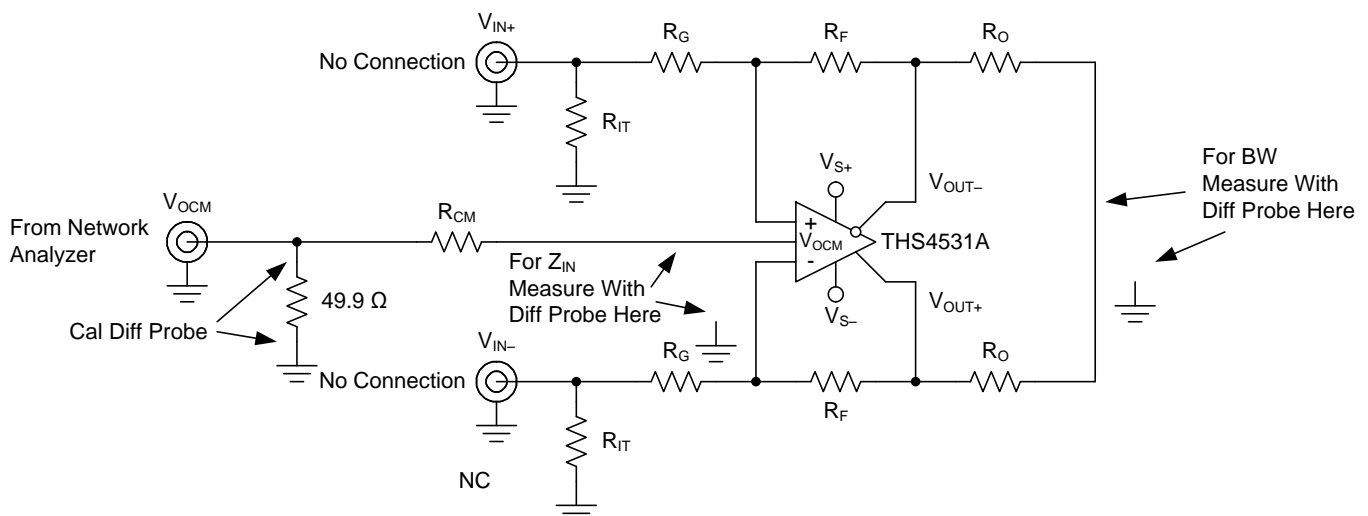


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**Figure 71. PSRR Test Circuit**

### **V<sub>OCM</sub> Input**

The circuit shown in [Figure 72](#) is used to measure the transient response, frequency response and input impedance of the V<sub>OCM</sub> input. For these tests, the cal point is across the 49.9Ω V<sub>OCM</sub> termination resistor. Transient response and frequency response are measured with R<sub>CM</sub> = 0Ω and using a high impedance differential probe at the summing junction of the two R<sub>O</sub> resistors, with respect to ground. The input impedance is measured using a high impedance differential probe at the V<sub>OCM</sub> pin and the drop across R<sub>CM</sub> is used to calculate the impedance seen looking into the amplifier's V<sub>OCM</sub> input.


**Figure 72. V<sub>OCM</sub> Input Test Circuit**

## Balance Error

The circuit shown in Figure 73 is used to measure the balance error of the main differential amplifier. A network analyzer is used as the signal source and the measurement device. The output impedance of the network analyzer is  $50\Omega$  and is DC coupled.  $R_{IT}$  and  $R_G$  are chosen to impedance match to  $50\Omega$  and maintain the proper gain. To balance the amplifier, a  $49.9\Omega$  resistor to ground is inserted across  $R_{IT}$  on the alternate input. The output is measured using a high impedance differential probe at the summing junction of the two  $R_O$  resistors, with respect to ground.

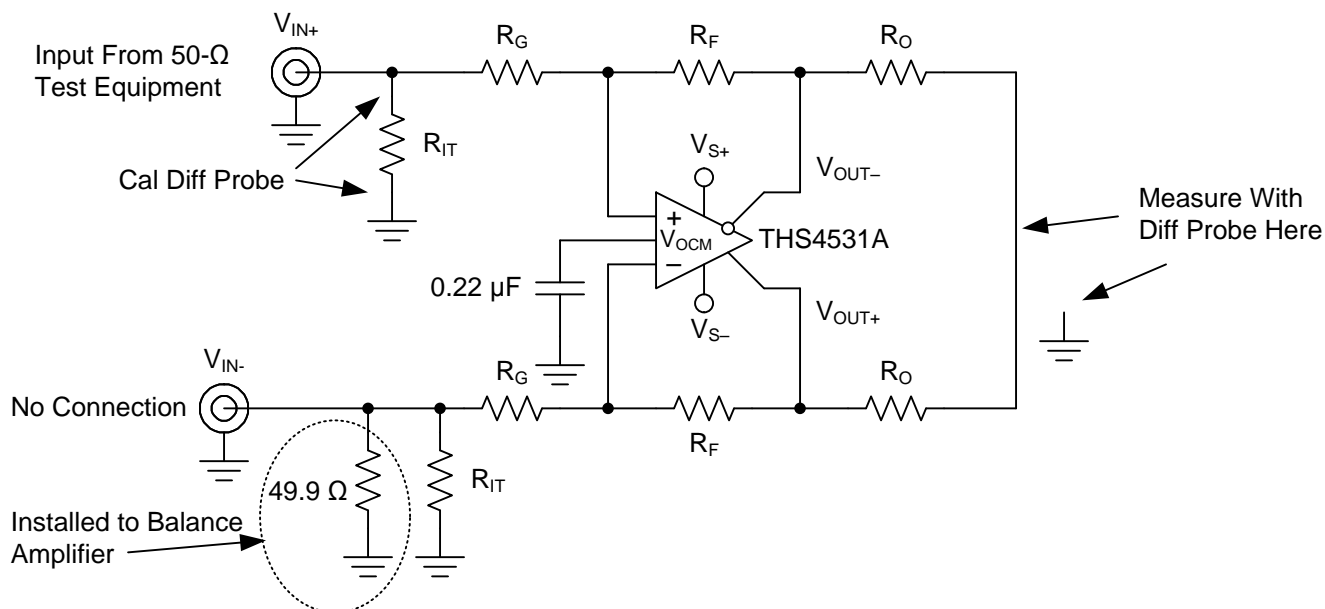


Figure 73. Balance Error Test Circuit

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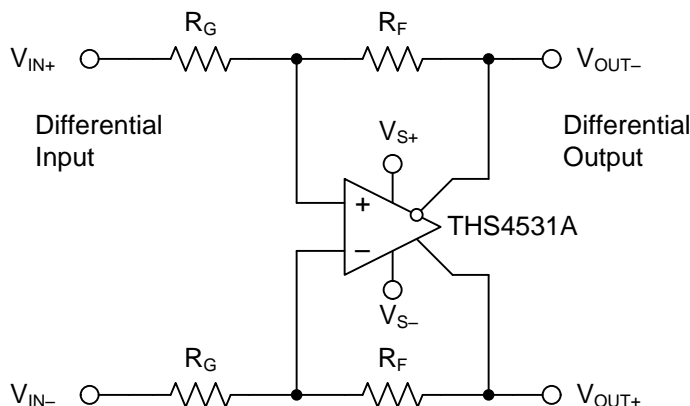
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## APPLICATION CIRCUITS

The following circuits show application information for the THS4531A. For simplicity, power supply decoupling capacitors are not shown in these diagrams – please see the EVM and Layout Recommendations section for recommendations. For more detail on the use and operation of fully differential op amps refer to application report “Fully-Differential Amplifiers” [SLOA054D](#).

### Differential Input to Differential Output Amplifier

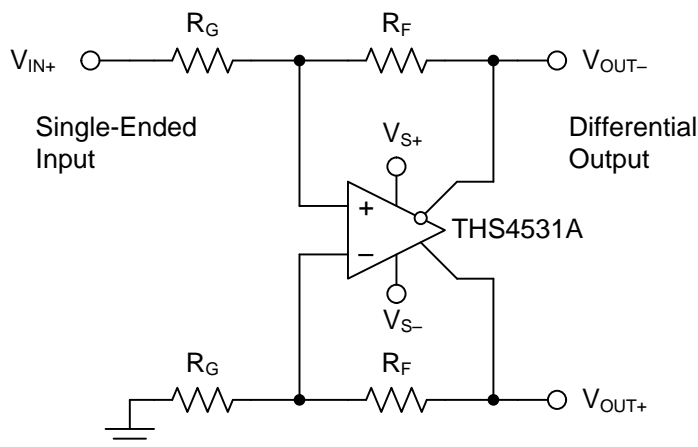
The THS4531A is a fully differential op amp and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in [Figure 74](#) ( $V_{OCM}$  and PD inputs not shown). The gain of the circuit is set by  $R_F$  divided by  $R_G$ .



**Figure 74. Differential Input to Differential Output Amplifier**

### Single-Ended Input to Differential Output Amplifier

The THS4531A can also be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in [Figure 75](#) ( $V_{OCM}$  and PD inputs not shown). The gain of the circuit is again set by  $R_F$  divided by  $R_G$ .



**Figure 75. Single-Ended Input to Differential Output Amplifier**

### Differential Input to Single-Ended Output Amplifier

Fully differential op amps like the THS4531A are not recommended for differential to single-ended conversion. This application is best performed with an instrumentation amplifier or with a standard op amp configured as a classic differential amplifier. See application section of the OPA835 data sheet ([SLOS713](#)).

## Input Common-Mode Voltage Range

The input common-mode voltage of a fully differential op amp is the voltage at the “+ and –” input pins of the op amp.

It is important to not violate the input common-mode voltage range ( $V_{ICR}$ ) of the op amp. Assuming the op amp is in linear operation the voltage across the input pins is only a few millivolts at most. So finding the voltage at one input pin will determine the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by:

$$\left( V_{OUT+} \times \frac{R_G}{R_G + R_F} \right) + \left( V_{IN-} \times \frac{R_F}{R_G + R_F} \right) \quad (1)$$

To determine the  $V_{ICR}$  of the op amp, the voltage at the negative input is evaluated at the extremes of  $V_{OUT+}$ .

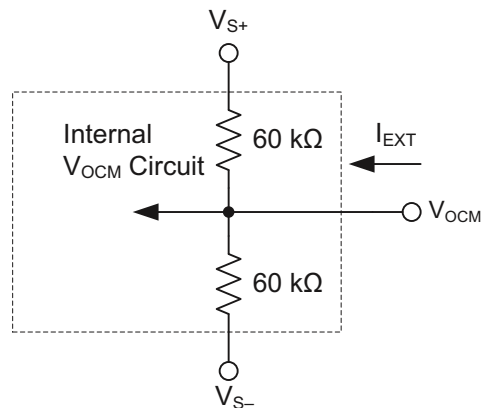
As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

## Setting the Output Common-Mode Voltage

The output common-mode voltage is set by the voltage at the  $V_{OCM}$  pin and the internal circuit works to maintain the output common-mode voltage as close as possible to this voltage. If left unconnected, the output common-mode is set to mid-supply by internal circuitry, which may be over-driven from an external source. [Figure 76](#) is representative of the  $V_{OCM}$  input. The internal  $V_{OCM}$  circuit has about 24MHz of -3dB bandwidth, which is required for best performance, but it is intended to be a DC bias input pin. Bypass capacitors are recommended on this pin to reduce noise. The external current required to overdrive the internal resistor divider is given approximately by the formula:

$$I_{EXT} = \frac{2V_{OCM} - (V_{S+} - V_{S-})}{60k\Omega} \quad (2)$$

where  $V_{OCM}$  is the voltage applied to the  $V_{OCM}$  pin.



**Figure 76. Simplified  $V_{OCM}$  Input Circuit**

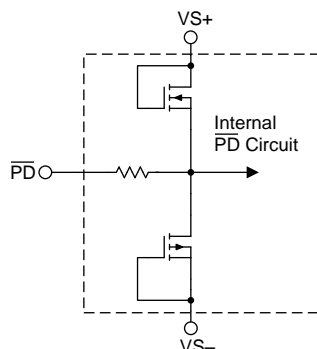
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## Power Down

The power down pin is internally connected to a CMOS stage which must be driven to a minimum of 2.1V to ensure proper high logic.

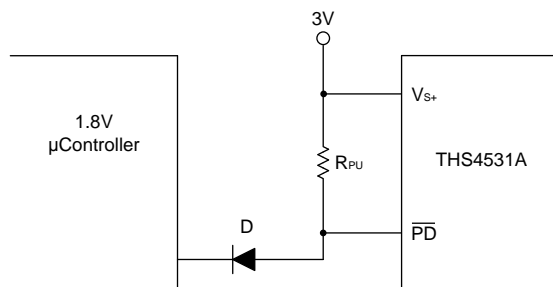


**Figure 77. Simplified Power Down Internal Circuit**

If 1.8V logic is used to drive the pin, a shoot through current of up to 100μA may develop in the digital logic causing the overall quiescent current to exceed the 2μA of maximum disabled quiescent current specified in the electrical characteristics.

In order to properly interface to 1.8V logic with minimal increase in additional current draw, a logic-level translator like the SN74AVC1T45 can be used.

Alternatively, the same function may be achieved using a diode and pull up resistor shown below.



**Figure 78. THS4531A Power Down Interface to 1.8V Logic Microcontroller**

The voltage seen at the power down pin will be a function of the supply voltage, input logic level, and diode drop. As long as the diode is forward biased, the power down voltage will be determined by:

$$V_{PD} = V_L + V_f \quad (3)$$

Where  $V_L$  is the logic level voltage and  $V_f$  is the forward voltage drop across the diode.

This means for 1.8V logic, the forward voltage of the diode should be greater than 0.3V but less than 0.7V in order to keep the power down logic level above 2.1V and less than 0.7V respectively.

For example, if we select 1N914 as the diode with a forward voltage of approximately 0.4V, the translated logic voltages will be 0.4V for disabled operation and 2.2V for enabled operation.

The additional current draw can be determined by:

$$i_{PD} = \frac{V_{CC} - (V_L + V_f)}{R_{PU}} \quad (4)$$

This equation shows that larger values of  $R_{PU}$  result in a smaller additional current. A reasonable value of  $R_{PU}$  may be 500kΩ where we can expect to see an additional current draw of 5.2μA while the device is in operation and 1.6μA when disabled.

## Single-Supply Operation

To facilitate testing with common lab equipment, the THS4531A EVM is built to allow for split-supply operation and most of the data presented in this data sheet was taken with split-supply power inputs. But the device is designed for use with single-supply power operation and can easily be used with single-supply power without degrading the performance. The only requirement is to bias the device properly and the specifications in this data sheet are given for single supply operation.

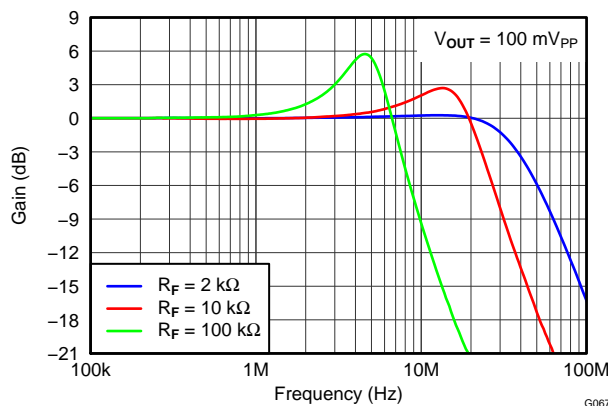
## Low Power Applications and the Effects of Resistor Values on Bandwidth

The THS4531A is designed for the nominal value of  $R_F$  to be 2 k $\Omega$ . This gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. It also loads the amplifier. For example; in gain of 1 with  $R_F = R_G = 2$  k $\Omega$ ,  $R_G$  to ground, and  $V_{OUT+} = 4$ V, 1mA of current will flow through the feedback path to ground. In low power applications, it is desirable to reduce this current by increasing the gain setting resistors values. Using larger value gain resistors has two primary side effects (other than lower power) due to their interaction with the device and PCB parasitic capacitance:

1. Lowers the bandwidth.
2. Lowers the phase margin
  - (a) This will cause peaking in the frequency response.
  - (b) And will cause over shoot and ringing in the pulse response.

Figure 79 shows the small signal frequency response for gain of 1 with  $R_F$  and  $R_G$  equal to 2k $\Omega$ , 10k $\Omega$ , and 100k $\Omega$ . The test was done with  $R_L = 2$ k $\Omega$ . Due to loading effects of  $R_L$ , lower values may reduce the peaking, but higher values will not have a significant effect.

As expected, larger value gain resistors cause lower bandwidth and peaking in the response (peaking in frequency response is synonymous with overshoot and ringing in pulse response).



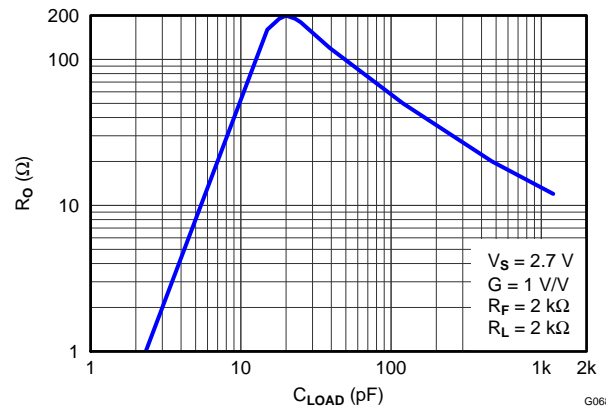
**Figure 79. THS4531A Frequency Response with Various Gain Setting Resistor Values**

## Driving Capacitive Loads

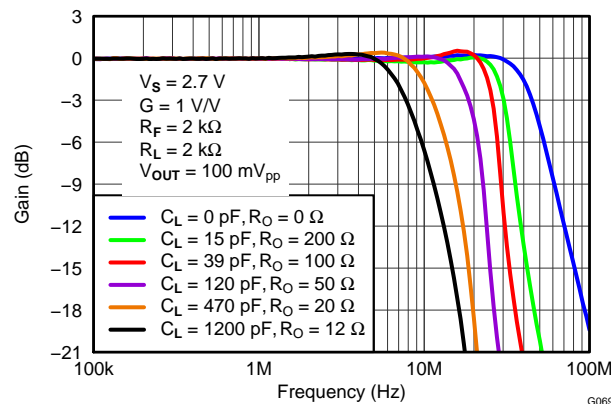
The THS4531A is designed for a nominal capacitive load of 2pF (differentially). When driving capacitive loads greater than this, it is recommended to use small resistors ( $R_O$ ) in series with the output as close to the device as possible. Without  $R_O$ , capacitance on the output will interact with the output impedance of the amplifier causing phase shift in the loop gain of the amplifier that will reduce the phase margin resulting in:

1. Peaking in the frequency response.
2. Overshoot, undershoot, and ringing in the time domain response with a pulse or square-wave signal.
3. May lead to instability or oscillation.

Inserting  $R_O$  will compensate the phase shift and restore the phase margin, but it will also limit bandwidth. The circuit shown in Figure 69 is used to test for best  $R_O$  versus capacitive loads,  $C_L$ , with a capacitance placed differential across the  $V_{OUT+}$  and  $V_{OUT-}$  along with 2k $\Omega$  load resistor, and the output is measure with a differential probe. Figure 80 shows the optimum values of  $R_O$  versus capacitive loads,  $C_L$ , and Figure 81 shows the frequency response with various values. Performance is the same on both 2.7V and 5V supply.



**Figure 80. Recommended Series Output Resistor vs Capacitive Load for Flat Frequency Response**



**Figure 81. Frequency Response for Various  $R_O$  and  $C_L$  Values**

## Audio Performance

The THS4531A provides excellent audio performance with very low quiescent power. To show performance in the audio band, the device was tested with an audio analyzer. THD+N and FFT tests were run at 1V<sub>rms</sub> output voltage. Performance is the same on both 2.7V and 5V supply. [Figure 82](#) is the test circuit used, and [Figure 83](#) and [Figure 84](#) show performance of the analyzer. In the FFT plot the harmonic spurs are at the testing limit of the analyzer, which means the THS4531A is actually much better than can be directly measured. Because the THS4531A distortion performance cannot be directly measured in the audio band it is estimated from measurement in high noise gain configuration correlated with simulation.



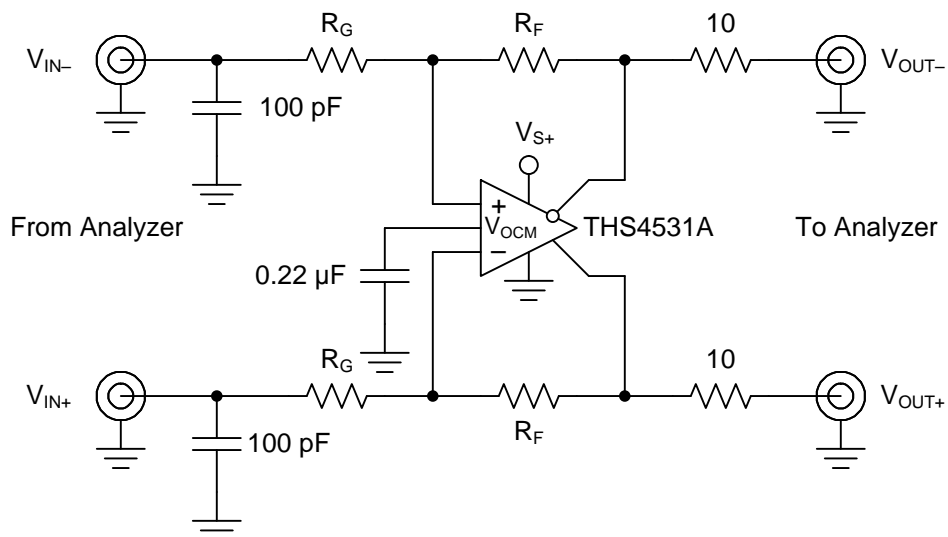


Figure 82. THS4531A Audio Analyzer Test Circuit

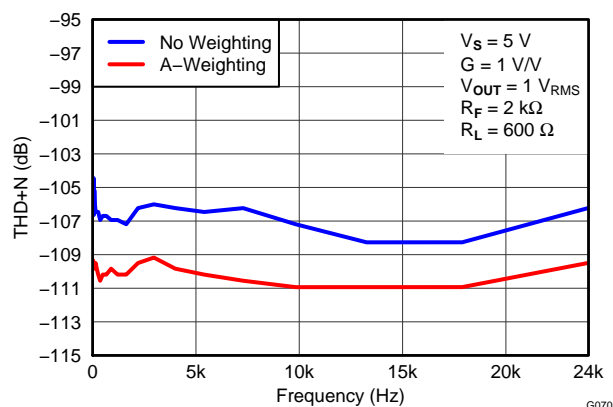


Figure 83. THD+N on Audio Analyzer, 10 Hz to 24 kHz

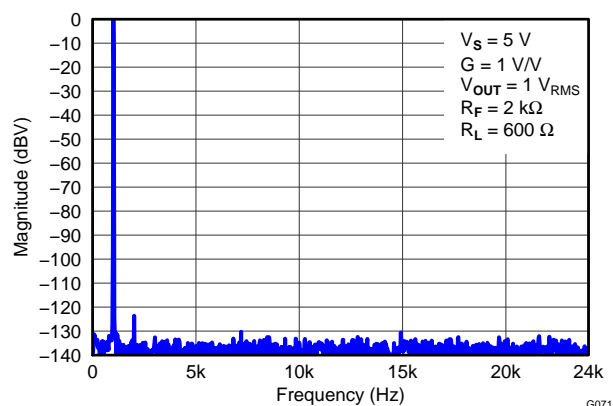


Figure 84. 1kHz FFT Plot on Audio Analyzer

# THS4531A

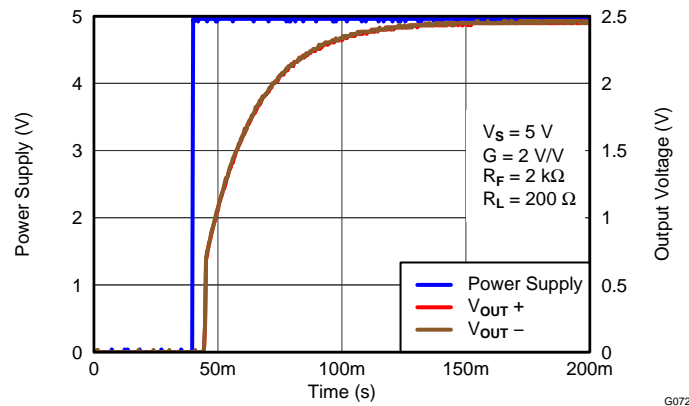
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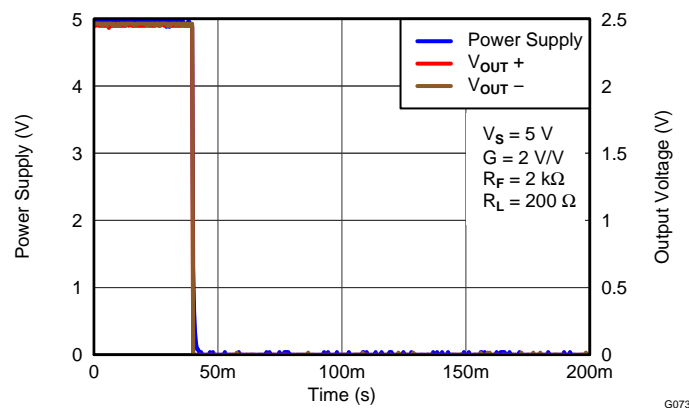
## Audio On/Off Pop Performance

The THS4531A is tested to show on and off pop performance by connecting a speaker between the differential outputs and switching on and off the power supply, and also by using the power down function of the THS4531A. Testing was done with and without tones. During these tests no audible pop could be heard.

With no input tone, Figure 85 shows the voltage waveforms when switching power on to the THS4531A and Figure 86 shows voltage waveforms when turning power off. The transients during power on and off show no audible pop should be heard.



**Figure 85. Power Supply Turn On Pop Performance**



**Figure 86. Power Supply Turn Off Pop Performance**

With no input tone, Figure 87 shows the voltage waveforms using the  $\overline{\text{PD}}$  pin to enable and disable the THS4531A. The transients during power on and off show no audible pop should be heard.

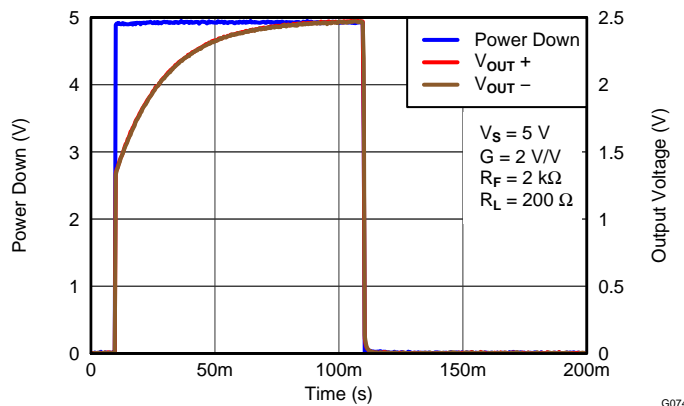


Figure 87.  $\overline{\text{PD}}$  Enable Pop Performance

## AUDIO ADC DRIVER PERFORMANCE: THS4531A AND PCM4204 COMBINED PERFORMANCE

To show achievable performance with a high performance audio ADC, the THS4531A is tested as the drive amplifier for the PCM4204. The PCM4204 is a high-performance, four-channel analog-to-digital (A/D) converter designed for professional and broadcast audio applications. The PCM4204 architecture utilizes a 1-bit delta-sigma modulator per channel incorporating an advanced dither scheme for improved dynamic performance, and supports PCM output data. The PCM4204 provides flexible serial port interface and many other advanced features. Please refer to its data sheet for more information.

The PCM4204 EVM is used to test the audio performance of the THS4531A as a drive amplifier. The standard PCM4204 EVM is provided with 4x OPA1632 fully differential amplifiers, which use the same pin out as the THS4531A. For testing, one of these amplifiers is replaced with a THS4531A device in same package (MSOP), gain changed to 1V/V, and power supply changed to single supply +5V. Figure 88 shows the circuit. With single supply +5V supply the output common-mode of the THS4531A defaults to +2.5V as required at the input of the PCM4204. So the resistor connecting the  $V_{\text{OCM}}$  input of the THS4531A to the input common-mode drive from the PCM4204 is optional and no performance change was noted with it connected or removed. The EVM power connections were modified by connecting positive supply inputs, +15V, +5VA and +5VD, to a +5V external power supply (EXT +3.3 was not used) and connecting -15V and all ground inputs to ground on the external power supply so only one external +5V supply was needed to power all devices on the EVM.

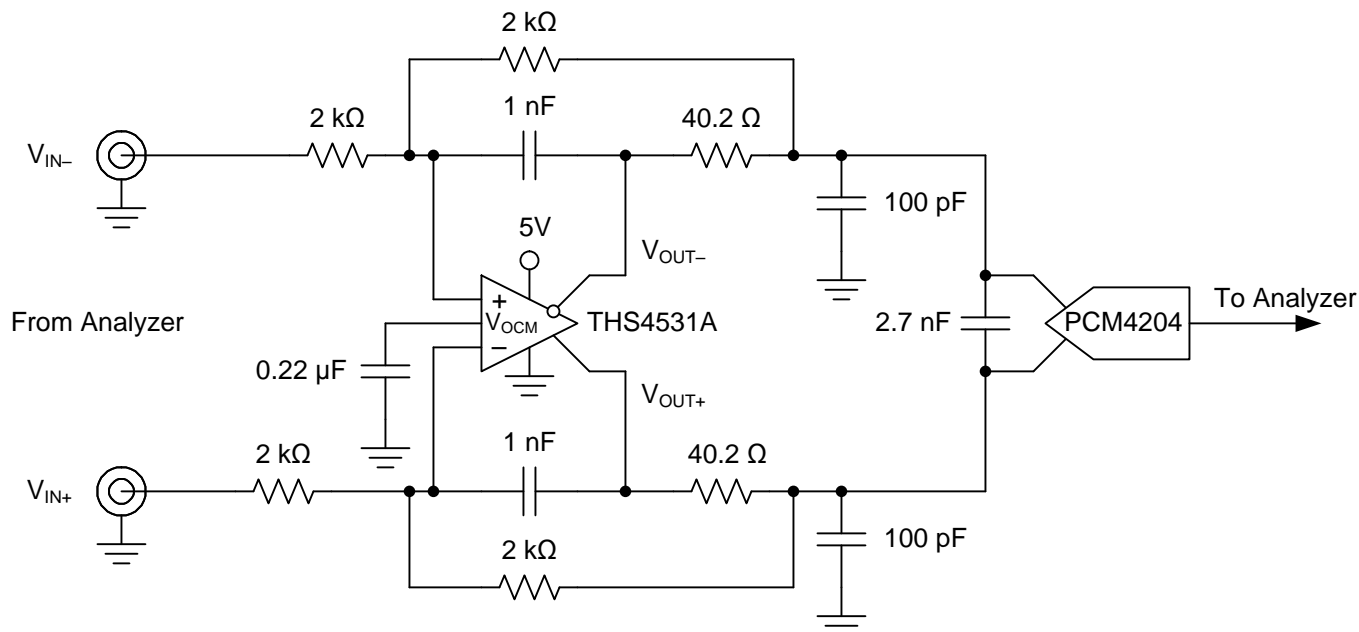


Figure 88. THS4531A and PCM4204 Test Circuit

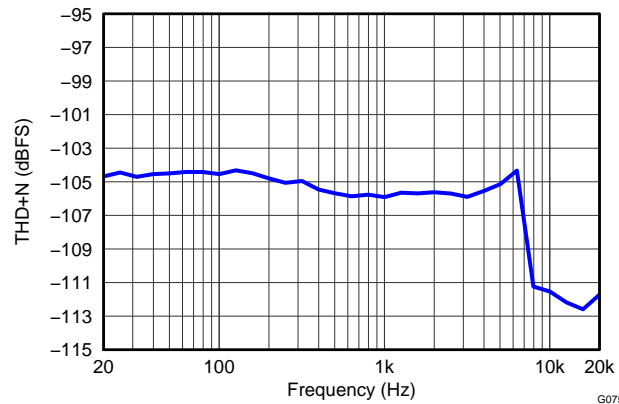
# THS4531A

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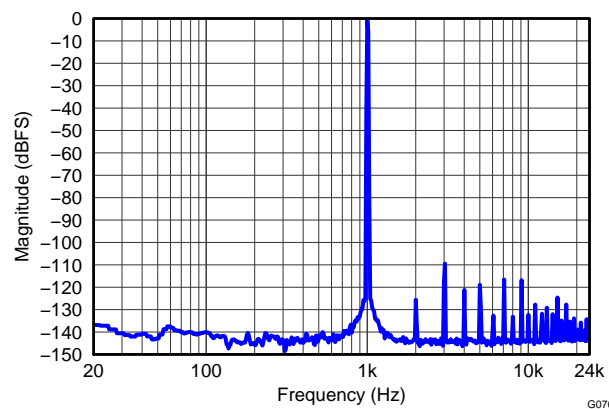
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An audio analyzer is used to provide an analog audio input to the EVM and the PCM formatted digital output is read by the digital input on the analyzer. Data was taken at  $f_s = 96\text{kHz}$ , and audio output uses PCM format. Other data rates and formats are expected to show similar performance in line with that shown in the data sheet.

Figure 89 shows the THD+N vs Frequency with no weighting and Figure 90 shows an FFT with 1kHz input tone. Input signal to the PCM4204 for these tests is -0.5dBFS. Table 4 summarizes results of testing using the THS4531A + PCM4204 versus typical Data Sheet performance, and show it make an excellent drive amplifier for this ADC.



**Figure 89. THS4531A + PCM4204 THD+N vs Frequency with No Weighting**



**Figure 90. THS4531A + PCM4204 1kHz FFT**

**Table 4. 1kHz AC Analysis: Test Circuit versus PCM4204 Data Sheet Typical Specifications ( $f_s = 96\text{kSPS}$ )**

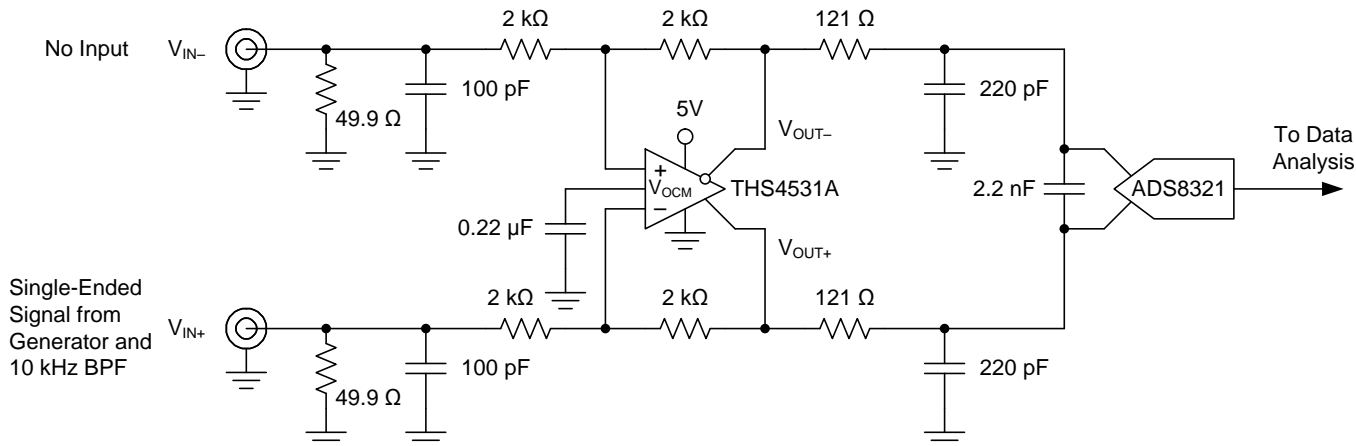
CONFIGURATION	TONE	THD + N
THS4531A + PCM4204	1kHz	-106 dB
PCM4204 Data Sheet (typ)	1kHz	-103 dB

## SAR ADC PERFORMANCE

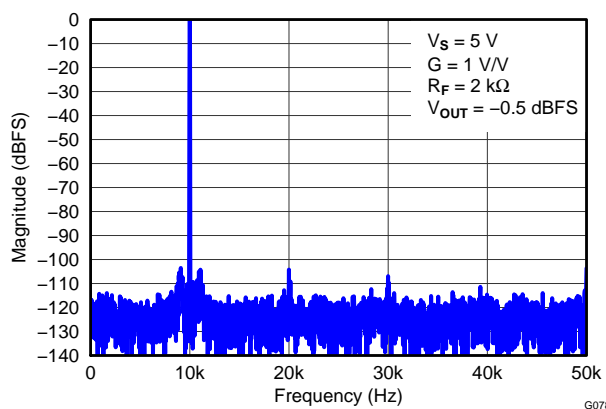
### THS4531A and ADS8321 Combined Performance

To show achievable performance with a high performance SAR ADC, the THS4531A is tested as the drive amplifier for the ADS8321. The ADS8321 is a 16-bit, SAR ADC that offers excellent AC and DC performance, with ultra-low power and small size. The circuit shown in Figure 91 is used to test the performance. Data was taken using the ADS8321 at 100kSPS with input frequency of 10 kHz and signal levels 0.5 dB below full scale. The FFT plot of the spectral performance is in Figure 92. A summary of the FFT analysis results are in Table 5 along with ADS8321 typical data sheet performance at  $f_s = 100\text{kSPS}$ . Please refer to its data sheet for more information.

The standard ADS8321 EVM and THS4531A EVM are modified to implement the schematic in Figure 91 and used to test the performance of the THS4531A as a drive amplifier. With single supply +5V supply the output common-mode of the THS4531A defaults to +2.5V as required at the input of the ADS8321 so the  $V_{OCM}$  input of the THS4531A simply bypassed to GND with 0.22 $\mu$ F capacitor. The summary of results of the FFT analysis versus typical data sheet performance shown in Table 5 show the THS4531A will make an excellent drive amplifier for this ADC.



**Figure 91. THS4531A and ADS8321 Test Circuit**



**Figure 92. THS4531A + ADS8321 1kHz FFT**

**Table 5. 10kHz FFT Analysis Summary**

CONFIGURATION	TONE	SIGNAL	SNR	THD	SINAD	SFDR
THS4531A + ADS8321	10kHz	-0.5 dBFS	87 dBc	-96 dBc	87 dBc	100 dBc
ADS8321 Data Sheet (typ)	10kHz	-0.5 dBFS	87 dBc	-86 dBc	84 dBc	86 dBc

### THS4531A and ADS7945 Combined Performance

To show achievable performance with a high performance SAR ADC, the THS4531A is tested as the drive amplifier for the ADS7945. The ADS7945 is a 14-bit, SAR ADC that offers excellent AC and DC performance, with low power and small size. The circuit shown in Figure 93 is used to test the performance. Data was taken using the ADS7945 at 2MSPS with input frequency of 10 kHz and signal level 0.5 dB below full scale. The FFT plot of the spectral performance is in Figure 94. A summary of the FFT analysis results are in Table 6 along with ADS7945 typical data sheet performance at  $f_s = 2$ MSPS. Please refer to its data sheet for more information.

## THS4531A

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The standard ADS7945 EVM and THS4531A EVM are modified to implement the schematic in Figure 93 and used to test the performance of the THS4531A as a drive amplifier. With single supply +5V supply the output common-mode of the THS4531A defaults to +2.5V as required at the input of the ADS7945 so the  $V_{OCM}$  input of the THS4531A simply bypassed to GND with 0.22 $\mu$ F capacitor. The summary of results of the FFT analysis versus typical data sheet performance shown in Table 6 show the THS4531A will make an excellent drive amplifier for this ADC.

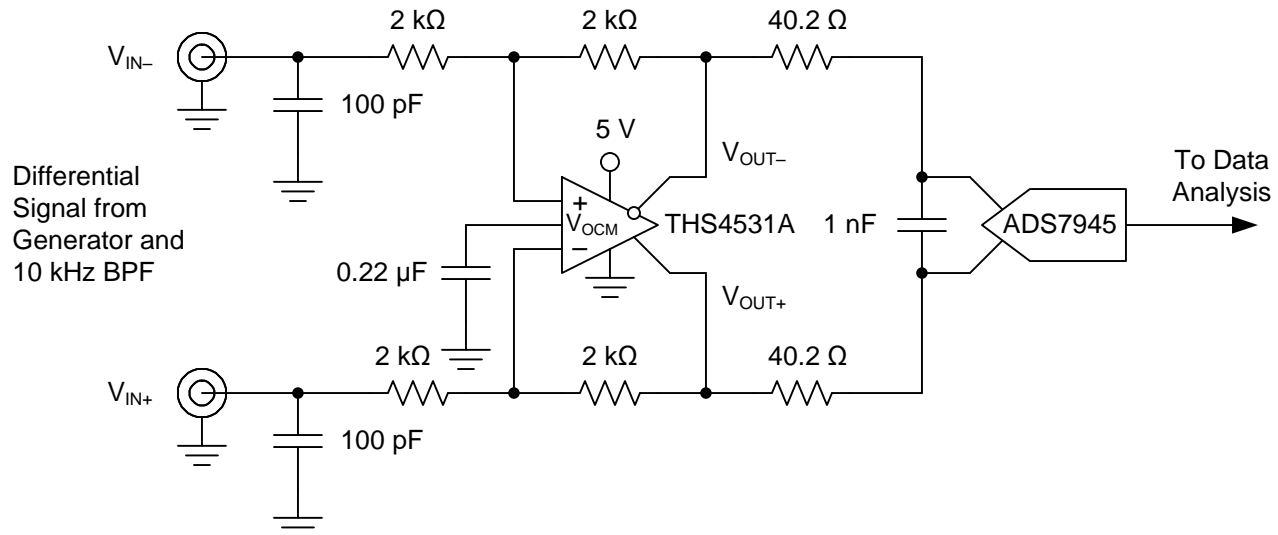


Figure 93. THS4531A and ADS7945 Test Circuit

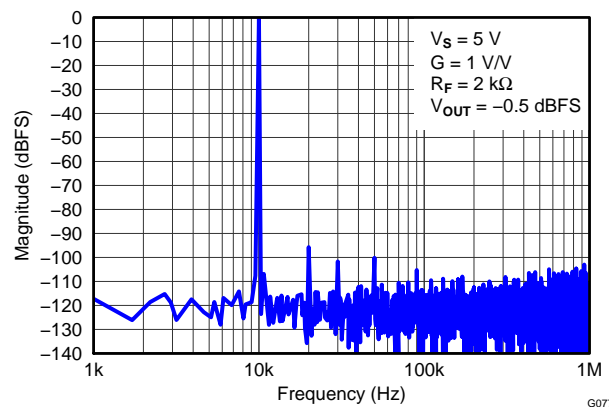


Figure 94. THS4531A and ADS7945 Test Circuit

Table 6. 10kHz FFT Analysis Summary

CONFIGURATION	TONE	SIGNAL	SNR	THD	SFDR
THS4531A + ADS7945	10kHz	-0.5 dBFS	83 dBc	-93 dBc	96 dBc
ADS7945 Data Sheet (typ)	10kHz	-0.5 dBFS	84 dBc	-92 dBc	94 dBc

## EVM AND LAYOUT RECOMMENDATIONS

The THS4531A EVM ([SLOU356](#)) should be used as a reference when designing the circuit board. It is recommended to follow the EVM layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the op amp.
2. The feedback path should be short and direct avoiding vias if possible.
3. Ground or power planes should be removed from directly under the amplifier's input and output pins.
4. A series output resistor is recommended to be placed as near to the output pin as possible. See [Figure 80](#) "Recommended Series Output Resistor vs. Capacitive Load" for recommended values given expected capacitive load of design.
5. A 2.2 $\mu$ F power supply decoupling capacitor should be placed within 2 inches of the device and can be shared with other op amps. For split supply, a capacitor is required for both supplies.
6. A 0.1 $\mu$ F power supply decoupling capacitor should be placed as near to the power supply pins as possible. Preferably within 0.1 inch. For split supply, a capacitor is required for both supplies.
7. The  $\overline{\text{PD}}$  pin uses TTL logic levels referenced to the negative supply voltage ( $V_{\text{S}}$ ). When not used it should be tied to the positive supply to enable the amplifier. When used, it must be actively driven high or low and should not be left in an indeterminate logic state. A bypass capacitor is not required, but can be used for robustness in noisy environments.

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**REVISION HISTORY**

<b>Changes from Original (December 2012) to Revision A</b>	<b>Page</b>
<ul style="list-style-type: none"><li>Changed graph title from "V<sub>OS</sub> OVER TEMPERATURE" to "SMALL-SIGNAL FREQUENCY RESPONSE" .....</li></ul>	<a href="#">17</a>

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## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4531AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T4531A	<a href="#">Samples</a>
THS4531AIDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	531A	<a href="#">Samples</a>
THS4531AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG   SN	Level-2-260C-1 YEAR	-40 to 125	531A	<a href="#">Samples</a>
THS4531AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T4531A	<a href="#">Samples</a>
THS4531AIRUNR	ACTIVE	QFN	RUN	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	531A	<a href="#">Samples</a>
THS4531AIRUNT	ACTIVE	QFN	RUN	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	531A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4531AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4531AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4531AIRUNR	QFN	RUN	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
THS4531AIRUNT	QFN	RUN	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4531AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THS4531AIDR	SOIC	D	8	2500	356.0	356.0	35.0
THS4531AIRUNR	QFN	RUN	10	3000	210.0	185.0	35.0
THS4531AIRUNT	QFN	RUN	10	250	210.0	185.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
THS4531AID	D	SOIC	8	75	506.6	8	3940	4.32
THS4531AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88

## GENERIC PACKAGE VIEW

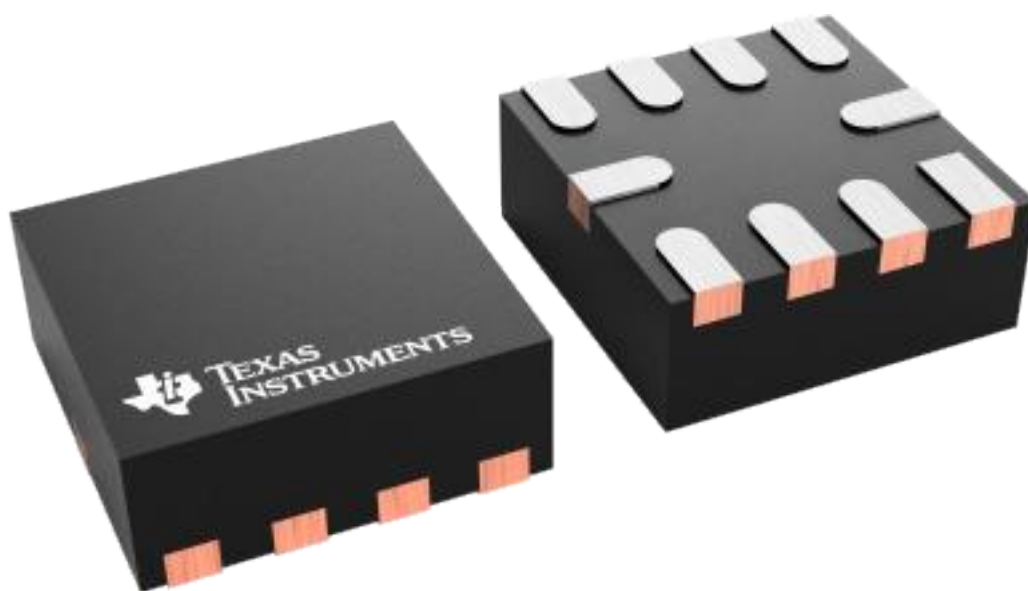
**RUN 10**

**WQFN - 0.8 mm max height**

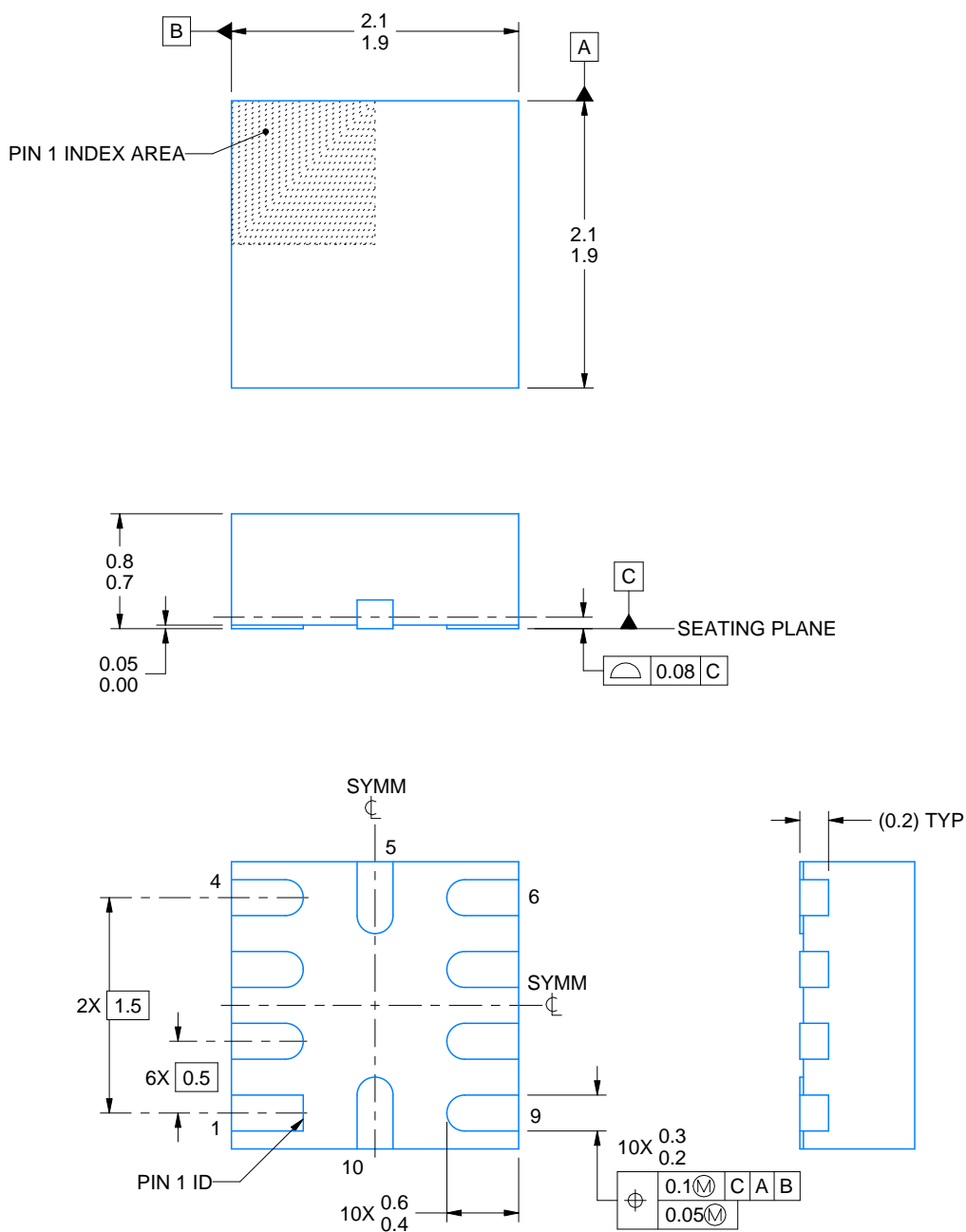
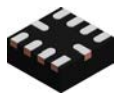
2 X 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4228249/A



4220470/A 05/2020

NOTES:

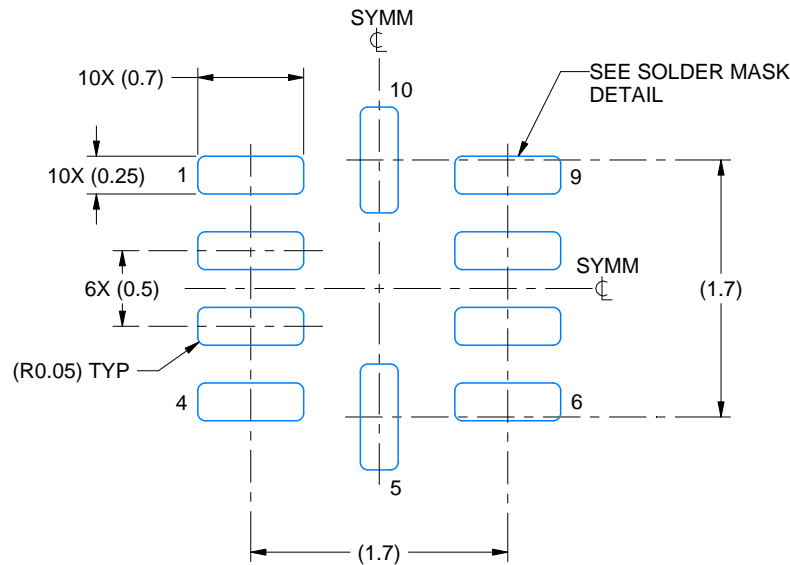
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

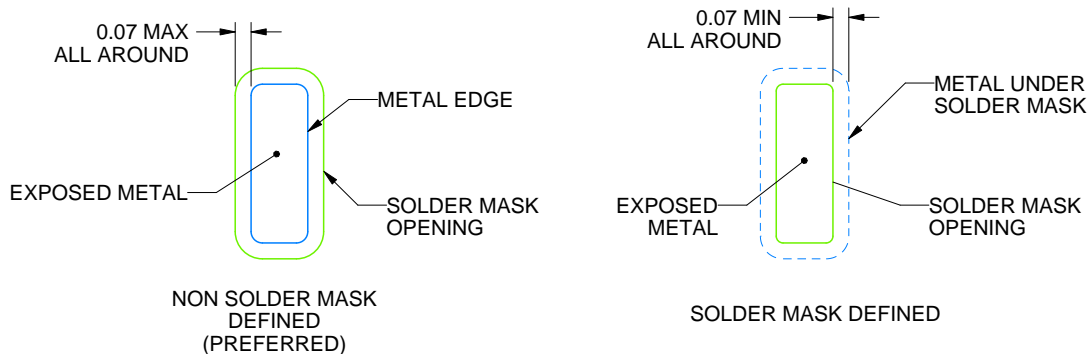
RUN0010A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



SOLDER MASK DETAILS

4220470/A 05/2020

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

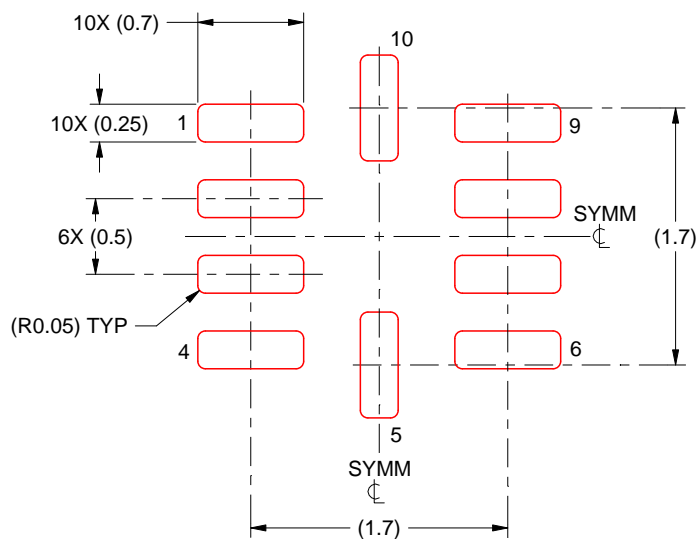


## EXAMPLE STENCIL DESIGN

RUN0010A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

4220470/A 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## DGK (S-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE



## NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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