THS6222 具有共模缓冲器的 8V 至 32V 差分 HPLC 线路驱动器

1 特性

- 电源电压范围 (V_S)：8V 至 32V
- 集成 1/2 Vs 共模缓冲器
- 大信号带宽：195MHz (V_O = 16V_{PP})
- 压摆率（16V 阶跃）：5500V/µs
- 低失真（V_S = 12V，50Ω 负载）：
  - HD2：–80dBc (1MHz)
  - HD3：–90dBc (1MHz)
- 输出电流：338mA（V_S = 12V，25Ω 负载）
- 宽输出摆幅 (V_S = 12V)：
  - 19.4V_{PP}（100Ω 负载）
  - 18.6V_{PP}（50Ω 负载）
- 可调功耗模式：
  - 满偏置模式：19.5mA
  - 中偏置模式：15mA
  - 低偏置模式：10.4mA
  - 低功耗关断模式
  - IADJ 引脚，用于调节偏置电流
- 集成式过热保护
- 升级至 THS6212 以实现高性能

2 应用

- SGCC HPLC 线路驱动器，IEEE 1901.1
- PLC 标准：G.hn、PRIME BPL、G3、PRIME
- HomePlug GreenPHY (HPGP)、ISO 15118
- 智能电表
- 数据集中器
- 电力线通信网关
- 家庭网络 PLC
- 差分 DSL 线路驱动器

3 说明

THS6222 是一款具有电流反馈架构的差分线路驱动器放大器，该器件使用德州仪器 (TI) 专有的高速硅锗 (SiGe) 工艺制造。该器件专用于在驱动重线路负载时需要高线性度的宽带、高速、电力线通信（HPLC、IEEE 1901.1）线路驱动器应用。THS6222 支持 PLC 标准，包括 G3、PRIME、ISO 15118 (HPGP)、G.hn 和 PRIME BPL。通用调制方案：OOK、FSK、OFDM。

THS6222 的独特架构可以尽可能降低静态电流，同时提供极高的线性度。该放大器具有可调的电流引脚 (IADJ)，可设定多种偏置模式的额定电流消耗，从而提供更佳的节能效果，而无需发挥放大器的全部性能。关断偏置模式能够在时分多路复用 (TDM) 系统中进一步降低接收模式下的功耗，同时保持高输出阻抗。集成式 1/2 Vs 共模缓冲器不需要外部元件，从而降低了系统成本并节省了布板空间。

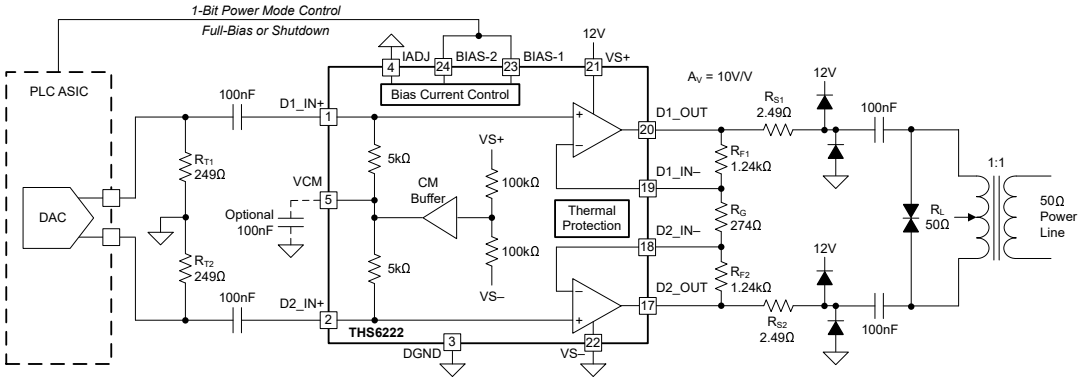
57V_{PP}（100Ω 负载）的宽输出摆幅搭配 32V 电源以及超过 650mA 的电流驱动（25Ω 负载），可提供低失真的宽带动态范围。

THS6222 采用 16 引脚和 24 引脚 VQFN 封装（带有外露散热焊盘），额定工作温度范围为 -40°C 至 +85°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
THS6222	RGT（VQFN，16）	3mm × 3mm
	RHF（VQFN，24）	5mm × 4mm
	YS 裸片（晶圆销售，19）	1261.00µm × 1641.00µm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



采用 THS6222 的典型线路驱动器电路

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

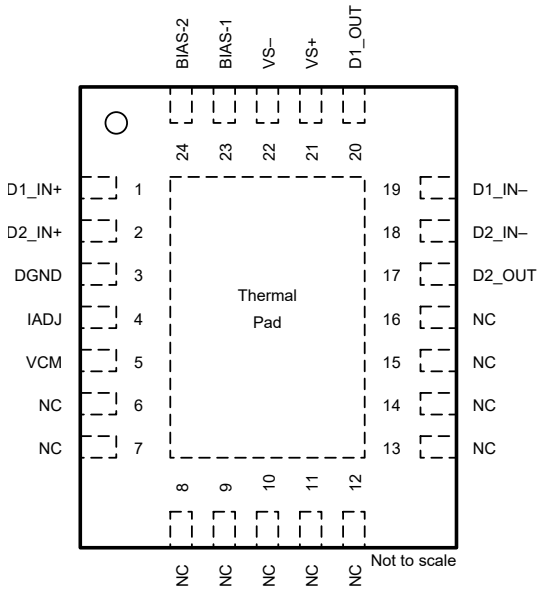


图 4-1. RHF Package,
24-Pin VQFN With Exposed Thermal Pad
(Top View)

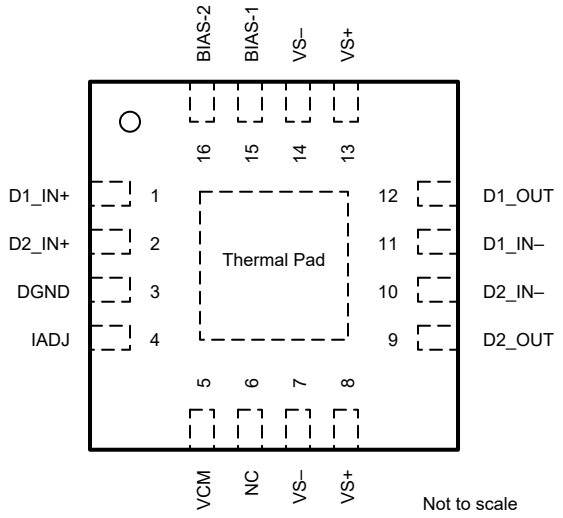


图 4-2. RGT Package,
16-Pin VQFN With Exposed Thermal Pad
(Top View)

表 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	RHF (VQFN)	RGT (VQFN)		
BIAS-1(1)	23	15	Input	Bias mode control, LSB
BIAS-2(1)	24	16	Input	Bias mode control, MSB
D1_IN –	19	11	Input	Amplifier D1 inverting input
D1_IN+	1	1	Input	Amplifier D1 noninverting input
D1_OUT	20	12	Output	Amplifier D1 output
D2_IN –	18	10	Input	Amplifier D2 inverting input
D2_IN+	2	2	Input	Amplifier D2 noninverting input
D2_OUT	17	9	Output	Amplifier D2 output
DGND(2)	3	3	Input	Ground reference for bias control pins
IADJ	4	4	Input	Bias current adjustment pin
NC	6-16	6	—	No internal connection
VCM	5	5	Output	Common-mode buffer output
VS –	22	7, 14	Power	Negative power-supply connection
VS+	21	8, 13	Power	Positive power-supply connection
Thermal Pad	Pad	Pad	Power	Electrically connected to die substrate and VS – . Connect to VS – on the printed circuit board (PCB) for best performance.

(1) The THS6222 defaults to the shutdown (disable) state if a signal is not present on the bias pins.
(2) The DGND pin ranges from VS – to (VS+) – 5V.

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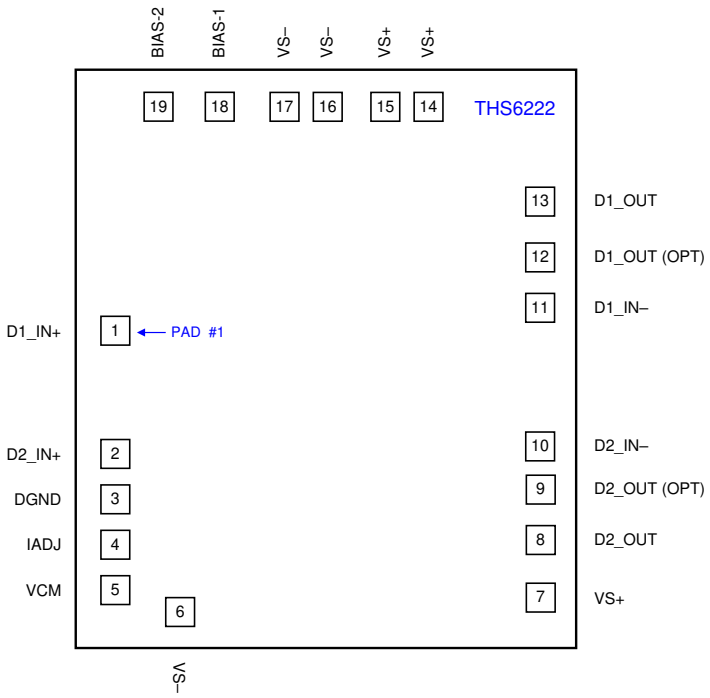


图 4-3. YS Die,
19-Pad Wafer Sale
(Top View)

表 4-2. Bond Pad Functions

PAD		TYPE	DESCRIPTION
NAME	NO.		
BIAS-1(1)	18	Input	Bias mode parallel control, LSB
BIAS-2(1)	19	Input	Bias mode parallel control, MSB
D1_IN –	11	Input	Amplifier D1 inverting input
D1_IN+	1	Input	Amplifier D1 noninverting input
D1_OUT	13	Output	Amplifier D1 output (must be used for D1 output)
D1_OUT (OPT)	12	Output	Optional amplifier D1 output (pad can be left unconnected or connected to pad 13)
D2_IN –	10	Input	Amplifier D2 inverting input
D2_IN+	2	Input	Amplifier D2 noninverting input
D2_OUT	8	Output	Amplifier D2 output (must be used for D2 output)
D2_OUT (OPT)	9	Output	Optional amplifier D2 output (can be left unconnected or connected to pad 8)
DGND(2)	3	Input	Ground reference for bias control pins
IADJ	4	Input	Bias-current adjustment pin
VCM	5	Output	Common-mode buffer output
VS –	6, 16, 17	Power	Negative power-supply connection
VS+	7, 14, 15	Power	Positive power-supply connection
Backside	—	—	Connect to the lowest voltage potential on the die (generally V_{S-})

(1) The THS6222 defaults to the shutdown (disable) state if a signal is not present on the bias pins.
(2) The DGND pin ranges from VS – to (VS+) – 5V.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, $V_S = (V_{S+}) - (V_{S-})$(2)		33	V
V_{BIAS}	Bias control pin voltage, referenced to DGND	0	16.5	V
V_{CM}	Common-mode voltage	See *Common-Mode Buffer*		V
$V_{IN/OUT/IADJ}$	All pins except VS+, VS–, VCM, and BIAS control	$(V_{S-}) - 0.5$	$(V_{S+}) + 0.5$	V
T_J	Maximum junction temperature (under any condition)		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Refer to *Breakdown Supply Voltage* for breakdown test results.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, $V_S = (V_{S+}) - (V_{S-})$	8		32	V
DGND	DGND pin voltage	V_{S-}		$V_{S+} - 5$	V
T_A	Ambient operating air temperature	–40	25	85	°C

5.4 Thermal Information

THERMAL METRIC(1)		THS6222		UNIT
		RHF (VQFN)	RGT (VQFN)	
		24 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.4	48.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35	55.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.3	22.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	1.6	°C/W
Y_{JB}	Junction-to-board characterization parameter	21.2	22.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.3	8.6	°C/W

(1) For more information about thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.5 Electrical Characteristics V_S = 12 V

at $T_A \approx 25°C$, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 50 Ω, series isolation resistor (R_S) = 2.5 Ω each, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, VCM = open, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth	A_V = 5 V/V, R_F = 1.5 kΩ, V_O = 2 V_{PP}			250		MHz
		A_V = 10 V/V, R_F = 1.24 kΩ, V_O = 2 V_{PP}			180		
		A_V = 15 V/V, R_F = 1 kΩ, V_O = 2 V_{PP}			165		
	0.1-dB bandwidth flatness				17		MHz
LSBW	Large-signal bandwidth	V_O = 16 V_{PP}			195		MHz
SR	Slew rate (20% to 80%)	V_O = 16-V step			5500		V/µs
	Rise and fall time (10% to 90%)	V_O = 2 V_{PP}			2.1		ns
HD2	2nd-order harmonic distortion	A_V = 10 V/V, V_O = 2 V_{PP}, R_L = 50 Ω	Full bias, f = 1 MHz		–80		dBc
			Mid bias, f = 1 MHz		–78		
			Low bias, f = 1 MHz		–78		
			Full bias, f = 10 MHz		–61		
			Mid bias, f = 10 MHz		–61		
			Low bias, f = 10 MHz		–61		
HD3	3rd-order harmonic distortion	A_V = 10 V/V, V_O = 2 V_{PP}, R_L = 50 Ω	Full bias, f = 1 MHz		–90		dBc
			Mid bias, f = 1 MHz		–86		
			Low bias, f = 1 MHz		–83		
			Full bias, f = 10 MHz		–69		
			Mid bias, f = 10 MHz		–65		
			Low bias, f = 10 MHz		–62		
e_n	Differential input voltage noise	f ≥ 1 MHz, input-referred, with and without 100 nF noise-decoupling capacitor on VCM pin			2.5		nV/√Hz
i_{n+}	Noninverting input current noise	f ≥ 1 MHz, each amplifier			1.4		pA/√Hz
i_{n-}	Inverting input current noise	f ≥ 1 MHz, each amplifier			18		pA/√Hz
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain				1300		kΩ
	Input offset voltage (each amplifier)				±12		mV
		T_A = –40°C			±16		
		T_A = 85°C			±11		
	Noninverting input bias current				±1		µA
		T_A = –40°C			±1		
		T_A = 85°C			±1		
	Inverting input bias current				±8		µA
		T_A = –40°C			±7		
		T_A = 85°C			±4		

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5.5 Electrical Characteristics V_S = 12 V （续）

at $T_A \approx 25°C$, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 50 Ω, series isolation resistor (R_S) = 2.5 Ω each, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, VCM = open, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
	Common-mode input voltage	Each input with respect to midsupply			±3.0		V
CMRR	Common-mode rejection ratio	Each input			64		dB
		T_A = –40°C			67		
		T_A = 85°C			62		
	Noninverting differential input resistance				10 || 2		kΩ || pF
	Inverting input resistance				43		Ω
COMMON-MODE BUFFER CHARACTERISTICS							
V_{CM-OS}	Common-mode offset voltage	Voltage at V_{CM} with respect to midsupply			±2.5		mV
		T_A = –40°C			±5		
		T_A = 85°C			±1		
	Common-mode voltage noise	With and without 100-nF V_{CM} noise-decoupling capacitor, f ≥ 50 kHz			20		nV/√Hz
	Common-mode output resistance	f = DC	AC-coupled inputs		650		Ω
			DC-coupled inputs		520		Ω
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	R_L = 100 Ω, R_S = 0 Ω			±9.7		V
		R_L = 50 Ω, R_S = 0 Ω			±9.3		
		R_L = 25 Ω, R_S = 0 Ω			±8.4		
I_O	Output current (sourcing and sinking)	R_L = 25 Ω, R_S = 0 Ω, based on V_O specification			±338		mA
	Short-circuit output current				±0.81		A
Z_O	Closed-loop output impedance	f = 1 MHz, differential			0.03		Ω
POWER SUPPLY							
DGND	DGND pin voltage			V_{S-}	0	V_{S+} – 5	V
I_{S+}	Quiescent current	Full bias (BIAS-1 = 0, BIAS-2 = 0)			19.5		mA
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)			15		
		Low bias (BIAS-1 = 0, BIAS-2 = 1)			10.4		
		Bias off (BIAS-1 = 1, BIAS-2 = 1)			1.1		
I_{S-}	Quiescent current	Full bias (BIAS-1 = 0, BIAS-2 = 0)			18.8		mA
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)			14.4		
		Low bias (BIAS-1 = 0, BIAS-2 = 1)			9.8		
		Bias off (BIAS-1 = 1, BIAS-2 = 1)			0.4		
	Current through DGND pin	Full bias (BIAS-1 = 0, BIAS-2 = 0)			0.8		mA
+PSRR	Positive power-supply rejection ratio	Differential			83		dB
–PSRR	Negative power-supply rejection ratio	Differential			83		dB

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5.5 Electrical Characteristics V_S = 12 V （续）

at $T_A \approx 25°C$, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 50 Ω, series isolation resistor (R_S) = 2.5 Ω each, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, VCM = open, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CONTROL						
	Bias control pin voltage	With respect to DGND, T_A = –40°C to +85°C	0	3.3	12	V
	Bias control pin logic threshold	Logic 1, with respect to DGND, T_A = –40°C to +85°C	2.1			V
		Logic 0, with respect to DGND, T_A = –40°C to +85°C			0.8	
	Bias control pin current(1)	BIAS-1, BIAS-2 = 0.5 V (logic 0)		–9.6		µA
		BIAS-1, BIAS-2 = 3.3 V (logic 1)		0.3	1	
	Open-loop output impedance	Off bias (BIAS-1 = 1, BIAS-2 = 1)		70 || 5		MΩ || pF

(1) Current is considered positive out of the pin.

5.6 Electrical Characteristics V_S = 32 V

at $T_A \approx 25°C$, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 100 Ω, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, V_{CM} = open, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth, –3 dB	A_V = 5 V/V, R_F = 1.5 kΩ, V_O = 2 V_{PP}			285		MHz
		A_V = 10 V/V, R_F = 1.24 kΩ, V_O = 2 V_{PP}			205		
	0.1-dB bandwidth flatness				13		MHz
LSBW	Large-signal bandwidth	V_O = 40 V_{PP}			170		MHz
SR	Slew rate (20% to 80% level)	V_O = 40-V step			11,000		V/µs
	Rise and fall time	V_O = 2 V_{PP}			2		ns
HD2	2nd-order harmonic distortion	A_V = 10 V/V, V_O = 2 V_{PP}, R_L = 100 Ω	Full bias, f = 1 MHz		–86		dBc
			Low bias, f = 1 MHz		–79		
			Full bias, f = 10 MHz		–71		
			Low bias, f = 10 MHz		–63		
HD3	3rd-order harmonic distortion	A_V = 10 V/V, V_O = 2 V_{PP}, R_L = 100 Ω	Full bias, f = 1 MHz		–101		dBc
			Low bias, f = 1 MHz		–88		
			Full bias, f = 10 MHz		–80		
			Low bias, f = 10 MHz		–65		
e_n	Differential input voltage noise	f ≥ 1 MHz, input-referred			2.5		nV/√Hz
i_{n+}	Noninverting input current noise (each amplifier)	f ≥ 1 MHz			1.7		pA/√Hz
i_{n-}	Inverting input current noise (each amplifier)	f ≥ 1 MHz			18		pA/√Hz
DC PERFORMANCE							
Z_{OL}	Open-loop transimpedance gain				1500		kΩ
	Input offset voltage				±12		mV
	Input offset voltage drift	T_A = –40°C to +85°C			–40		µV/°C
	Input offset voltage matching	Amplifier A to B			±0.5		mV
	Noninverting input bias current				±1		µA
	Inverting input bias current				±6		µA

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5.6 Electrical Characteristics V_S = 32 V （续）

at $T_A \approx 25°C$, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 100 Ω, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, V_{CM} = open, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Inverting input bias current matching			±8		μA

5.6 Electrical Characteristics V_S = 32 V （续）

at $T_A \approx 25°C$, differential closed-loop gain (A_V) = 10 V/V, differential load (R_L) = 100 Ω, R_F = 1.24 kΩ, R_{ADJ} = 0 Ω, V_{CM} = open, V_O = D1_OUT – D2_OUT, and full bias (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
	Common-mode input voltage	Each input	±11	±12		V
CMRR	Common-mode rejection ratio	Each input	53	65		dB
	Noninverting input resistance			10 || 2		kΩ || pF
	Inverting input resistance			38		Ω
COMMON-MODE BUFFER CHARACTERISTICS						
V_{CM-OS}	Common-mode offset voltage	Voltage at V_{CM} with respect to midsupply		±3.9		mV
	Common-mode voltage noise	With and without 100-nF V_{CM} noise-decoupling capacitor, f ≥ 50 kHz		21		nV/√Hz
	Common-mode output resistance	f = DC		520		Ω
OUTPUT CHARACTERISTICS						
V_O	Output voltage swing(1)	R_L = 100 Ω		±28.5		V
		R_L = 25 Ω		±16.3		
I_O	Output current (sourcing and sinking) (1)	R_L = 25 Ω, based on V_O specification	±580	±665		mA
	Short-circuit output current			1		A
Z_O	Output impedance	f = 1 MHz, differential		0.01		Ω
POWER SUPPLY						
I_{S+}	Quiescent current	Full bias (BIAS-1 = 0, BIAS-2 = 0)		23		mA
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)		17.7		
		Low bias (BIAS-1 = 0, BIAS-2 = 1)		12.2		
		Bias off (BIAS-1 = 1, BIAS-2 = 1)		1.5	1.8	
I_{S-}	Quiescent current	Full bias (BIAS-1 = 0, BIAS-2 = 0)		22		mA
		Mid bias (BIAS-1 = 1, BIAS-2 = 0)		16.7		
		Low bias (BIAS-1 = 0, BIAS-2 = 1)		11.2		
		Bias off (BIAS-1 = 1, BIAS-2 = 1)		0.5	0.8	
	Current through GND pin	Full bias (BIAS-1 = 0, BIAS-2 = 0)		1		mA
+PSRR	Positive power-supply rejection ratio	Differential		83		dB
–PSRR	Negative power-supply rejection ratio	Differential		77		dB
BIAS CONTROL						
	Bias control pin voltage	With respect to DGND, T_A = –40°C to +85°C	0	3.3	16.5	V
	Bias control pin logic threshold	Logic 1, with respect to DGND, T_A = –40°C to +85°C	1.9			V
		Logic 0, with respect to DGND, T_A = –40°C to +85°C			0.8	
	Bias control pin current(2)	BIAS-1, BIAS-2 = 0.5 V (logic 0)	–15	–10		µA
		BIAS-1, BIAS-2 = 3.3 V (logic 1)		0.1	1	

(1) See *Output Voltage and Current Drive* and *图 5-51* for output voltage vs output current characteristics.
(2) Current is considered positive out of the pin.

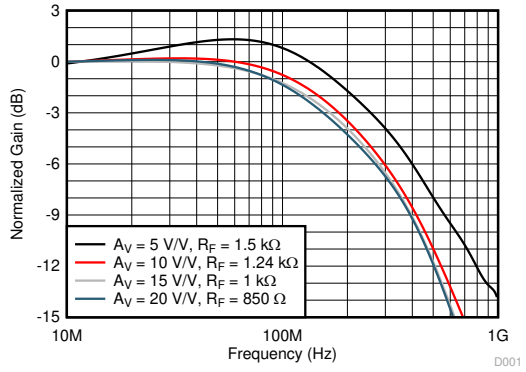
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5.7 Timing Requirements

		MIN	NOM	MAX	UNIT
t_{ON}	Turn-on time delay: time for output to start tracking the input		25		ns
t_{OFF}	Turn-off time delay: time for output to stop tracking the input		275		ns

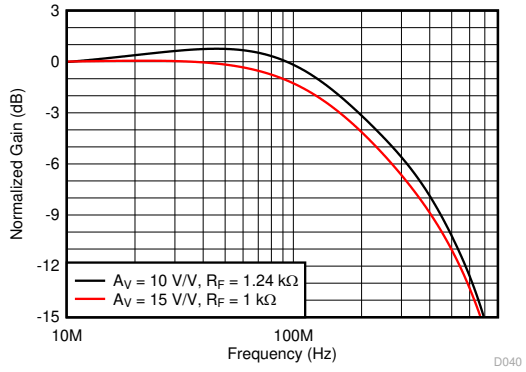
5.8 Typical Characteristics: V_S = 12 V

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



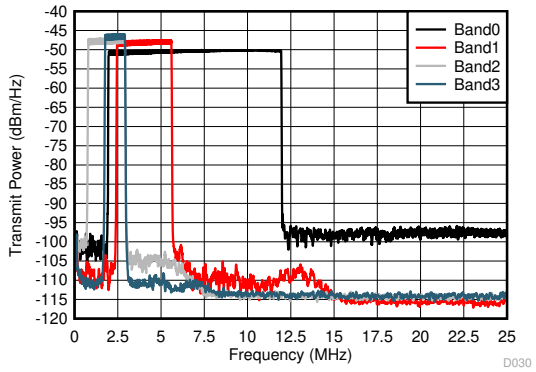
V_O = 2 V_{PP}

图 5-1. Small-Signal Frequency Response



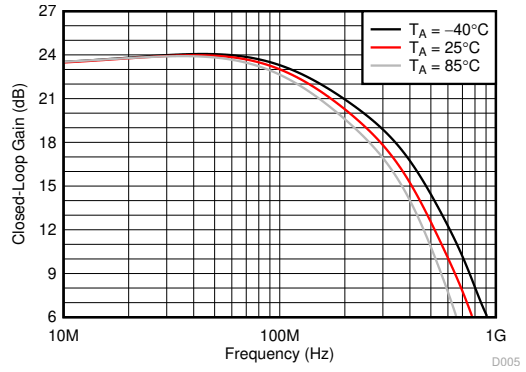
V_O = 16 V_{PP}

图 5-2. Large-Signal Frequency Response



SGCC HPLC profiles, crest factor = 5 V/V, see the *Broadband PLC Line Driving* section for more details.

图 5-3. Out-of-Band Suppression



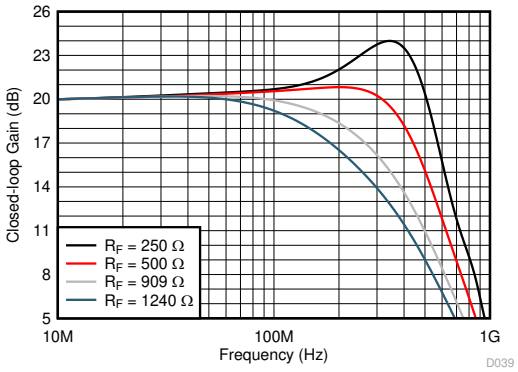
A_V = 15 V/V, V_O = 2 V_{PP}

图 5-4. Small-Signal Frequency Response vs Temperature

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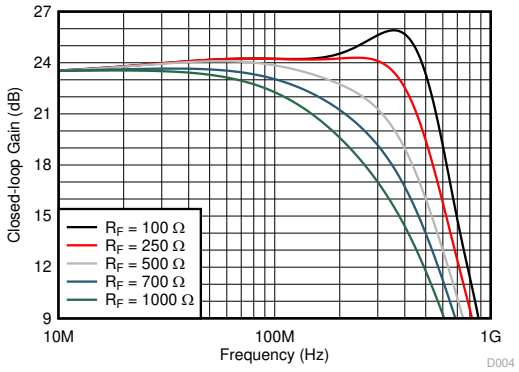
5.8 Typical Characteristics: V_S = 12 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



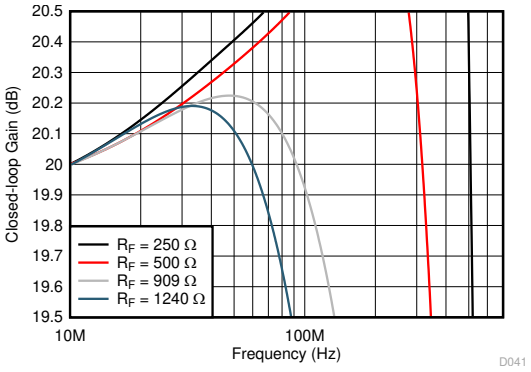
A_V = 10 V/V, V_O = 2 V_{PP}

图 5-5. Small-Signal Frequency Response vs R_F



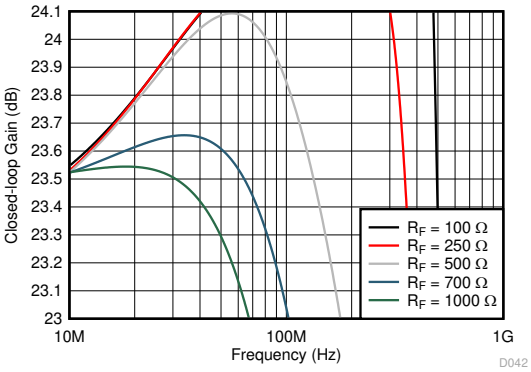
A_V = 15 V/V, V_O = 2 V_{PP}

图 5-6. Small-Signal Frequency Response vs R_F



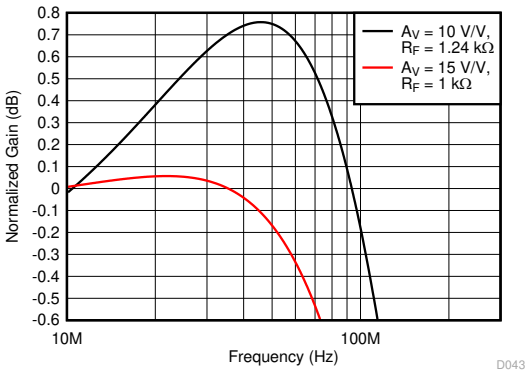
A_V = 10 V/V, V_O = 2 V_{PP}

图 5-7. Small-Signal Gain Flatness vs R_F



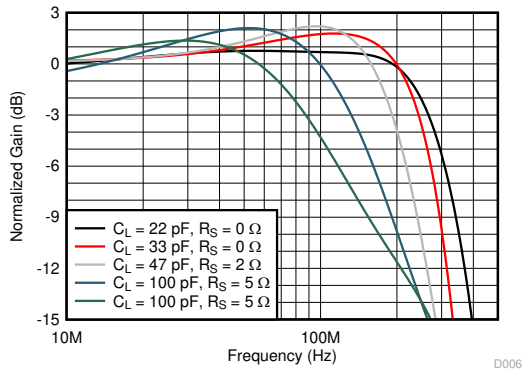
A_V = 15 V/V, V_O = 2 V_{PP}

图 5-8. Small-Signal Gain Flatness vs R_F



V_O = 16 V_{PP}

图 5-9. Large-Signal Gain Flatness



V_O = 100 mV_{PP}

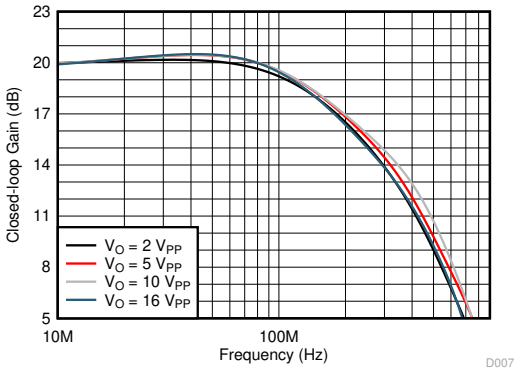
Frequency response is measured at the device output pin before the isolation resistor.

图 5-10. Small-Signal Frequency Response vs C_{LOAD}

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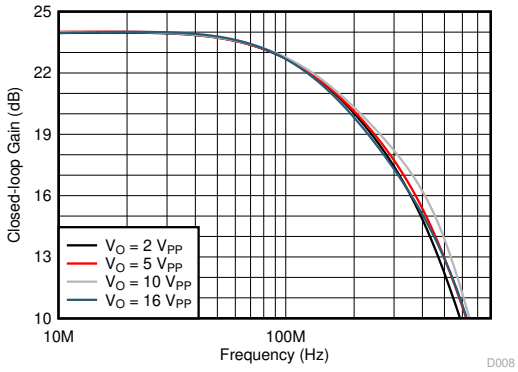
5.8 Typical Characteristics: V_S = 12 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



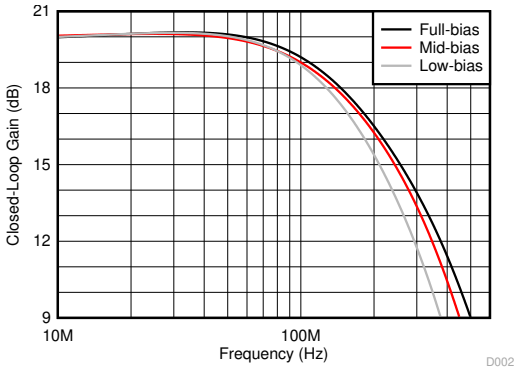
A_V = 10 V/V

图 5-11. Large-Signal Frequency Response vs V_O



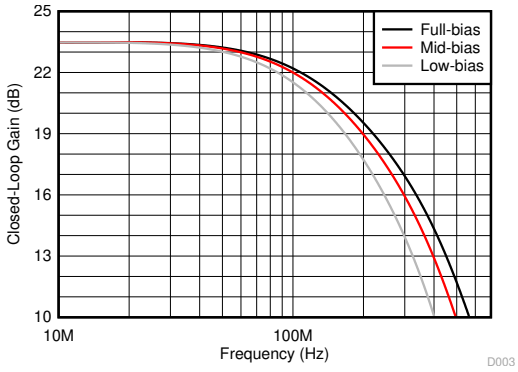
A_V = 15 V/V

图 5-12. Large-Signal Frequency Response vs V_O



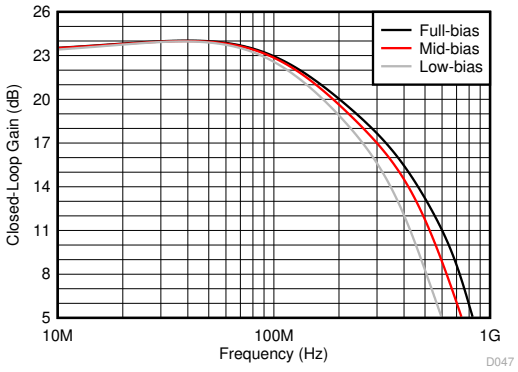
A_V = 10 V/V, V_O = 2 V_{PP}

图 5-13. Small-Signal Frequency Response vs Bias Modes



A_V = 15 V/V, V_O = 2 V_{PP}

图 5-14. Small-Signal Frequency Response vs Bias Modes



A_V = 15 V/V, V_O = 16 V_{PP}

图 5-15. Large-Signal Frequency Response vs Bias Modes

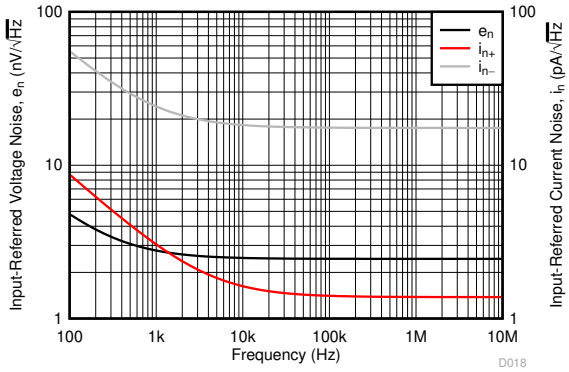
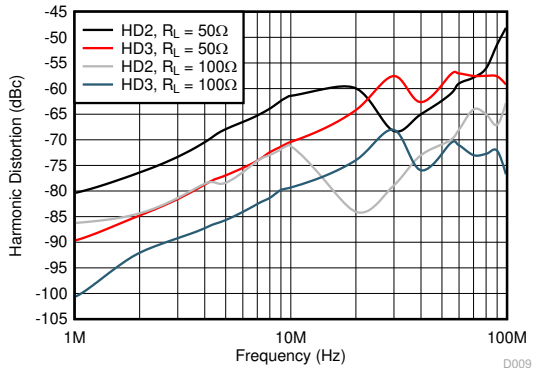


图 5-16. Input Voltage and Current Noise Density vs Frequency

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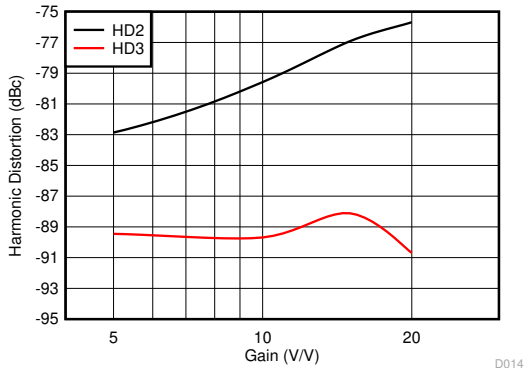
5.8 Typical Characteristics: V_S = 12 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



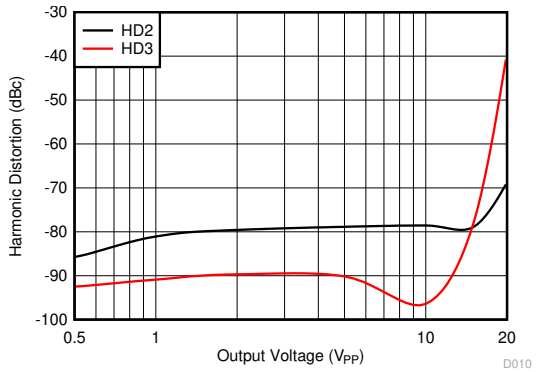
V_O = 2 V_{PP}

图 5-17. Harmonic Distortion vs Frequency



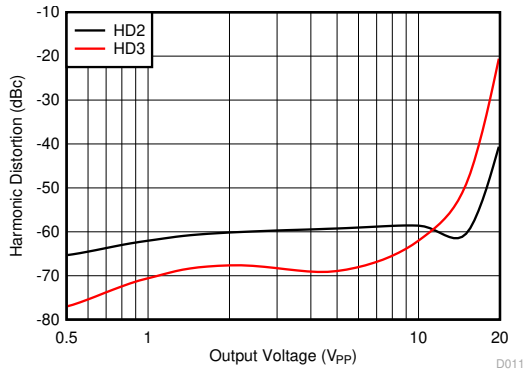
f = 1 MHz, V_O = 2 V_{PP}

图 5-18. Harmonic Distortion vs Gain



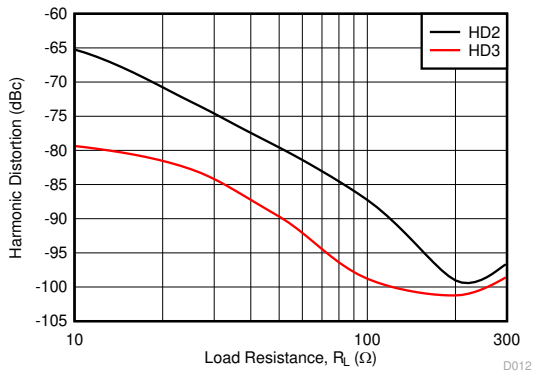
f = 1 MHz, A_V = 10 V/V

图 5-19. Harmonic Distortion vs V_O



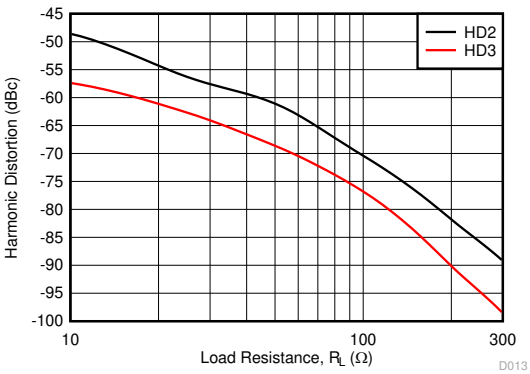
f = 10 MHz, A_V = 10 V/V

图 5-20. Harmonic Distortion vs V_O



f = 1 MHz, V_O = 2 V_{PP}, A_V = 10 V/V

图 5-21. Harmonic Distortion vs R_L



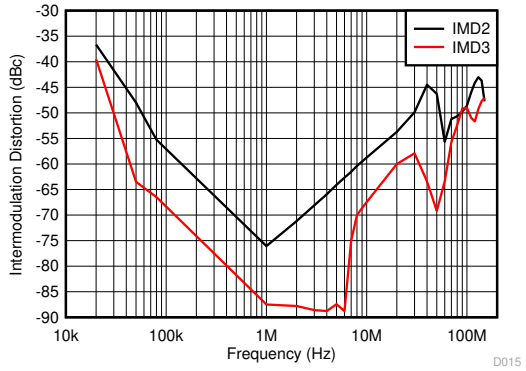
f = 10 MHz, V_O = 2 V_{PP}, A_V = 10 V/V

图 5-22. Harmonic Distortion vs R_L

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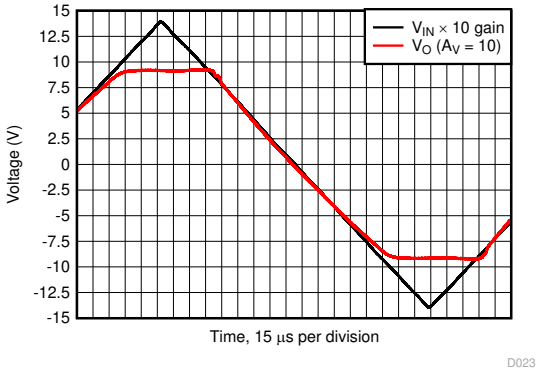
5.8 Typical Characteristics: V_S = 12 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



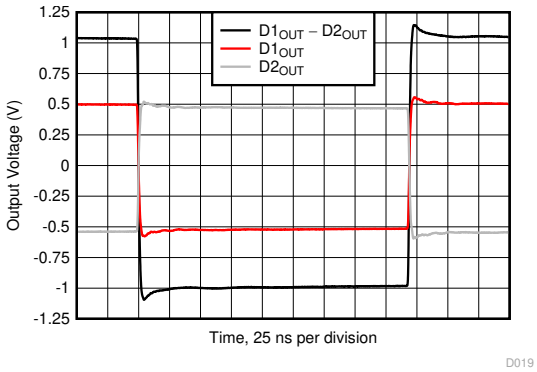
±12.2 kHz tone spacing, V_O = 2 V_{PP} per tone

图 5-23. Intermodulation Distortion vs Frequency



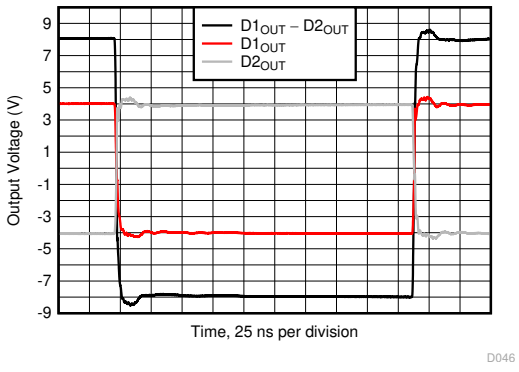
V_{IN} = 2.8-V_{PP} triangular waveform

图 5-24. Overdrive Recovery



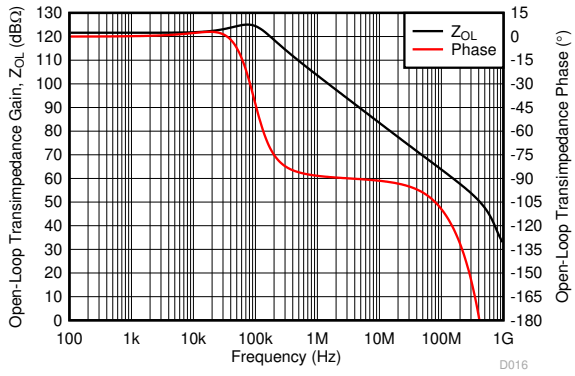
V_O step = 2 V_{PP}

图 5-25. Small-Signal Pulse Response



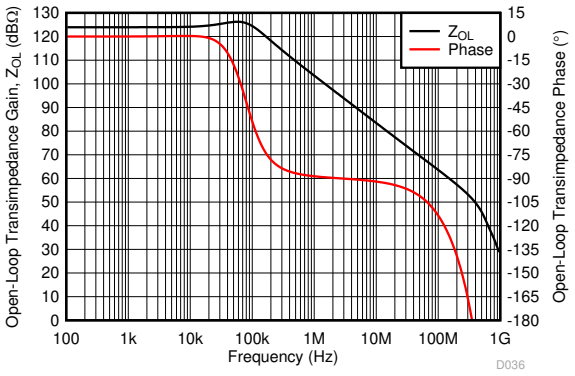
V_O step = 16 V_{PP}

图 5-26. Large-Signal Pulse Response



Full-bias simulation

图 5-27. Open-Loop Transimpedance Gain and Phase vs Frequency



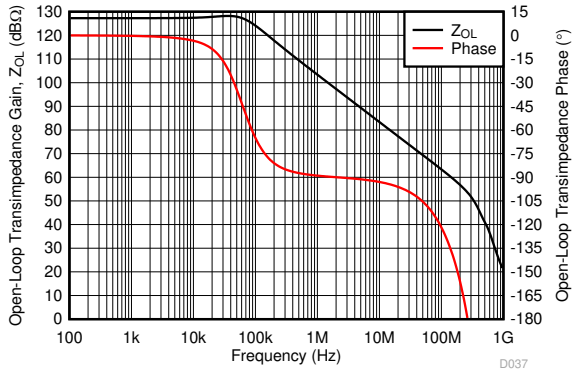
Mid-bias simulation

图 5-28. Open-Loop Transimpedance Gain and Phase vs Frequency

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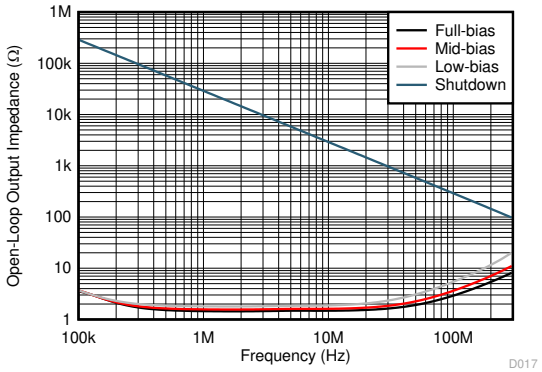
5.8 Typical Characteristics: V_S = 12 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



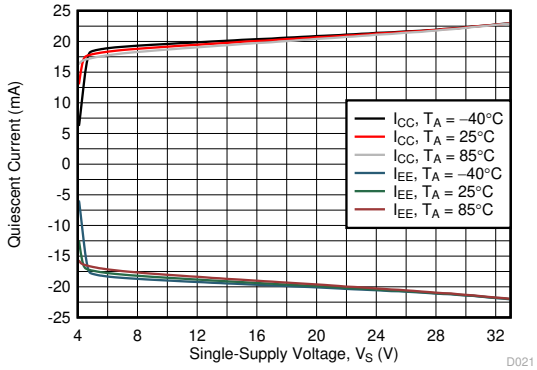
Low-bias simulation

图 5-29. Open-Loop Transimpedance Gain and Phase vs Frequency



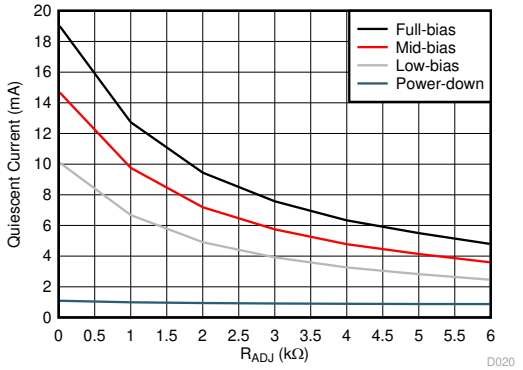
Simulation

图 5-30. Open-Loop Output Impedance vs Frequency



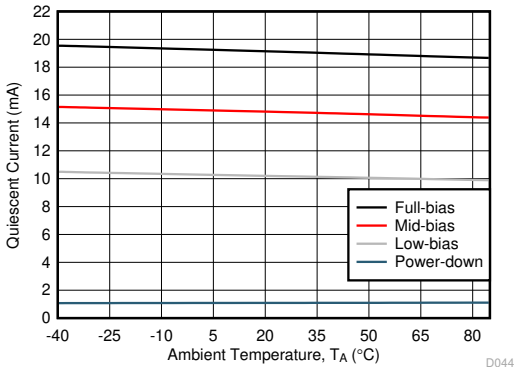
R_L = no load, average of 30 devices

图 5-31. Quiescent Current vs Single-Supply Voltage



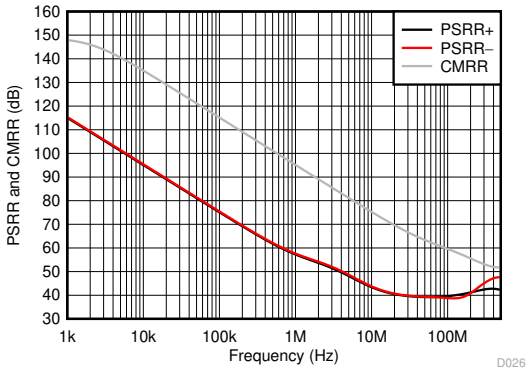
Average of 30 devices

图 5-32. Quiescent Current vs R_{ADJ}



R_L = no load, average of 30 devices

图 5-33. Quiescent Current vs Temperature



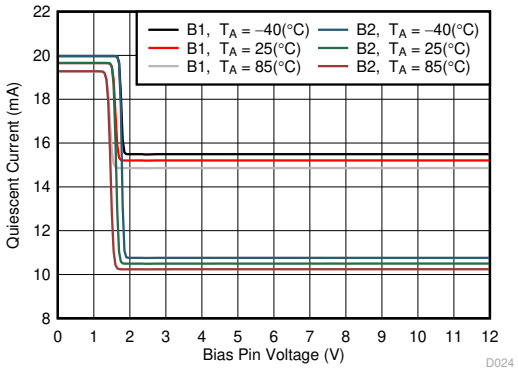
T_J = 50°C, simulation

图 5-34. PSRR and CMRR vs Frequency

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5.8 Typical Characteristics: V_S = 12 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 50 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



B1 = full-bias to mid-bias transition with B2 = DGND, B2 = full-bias to low-bias transition with B1 = DGND, DGND = V_S –

图 5-35. Mode Transition Voltage Threshold

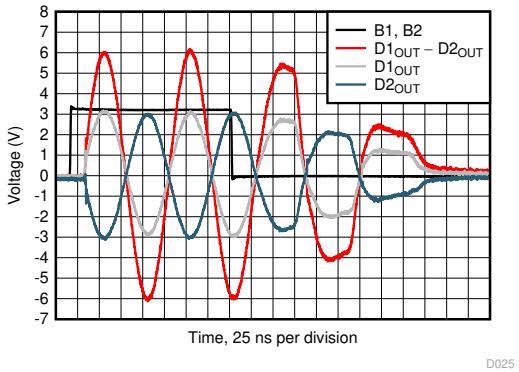
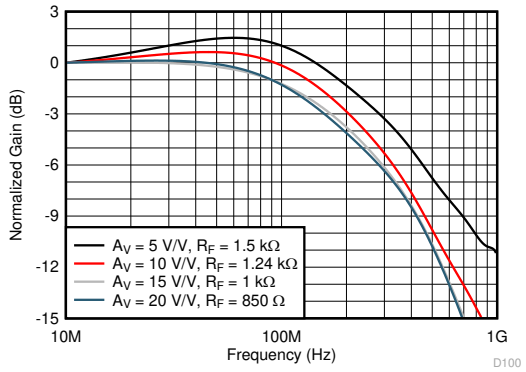


图 5-36. Full-Bias and Shutdown Mode Transition Timing

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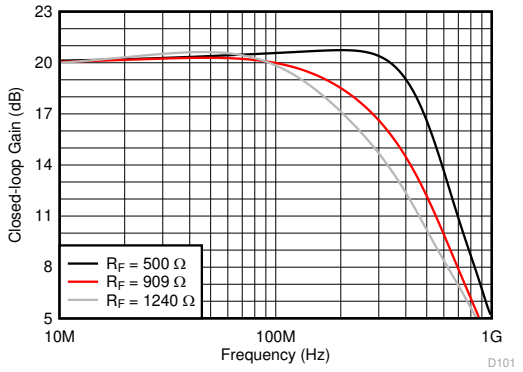
5.9 Typical Characteristics: V_S = 32 V

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 100 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



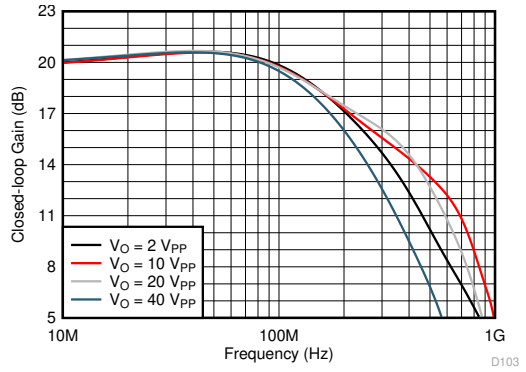
V_O = 2 V_{PP}

图 5-37. Small-Signal Frequency Response



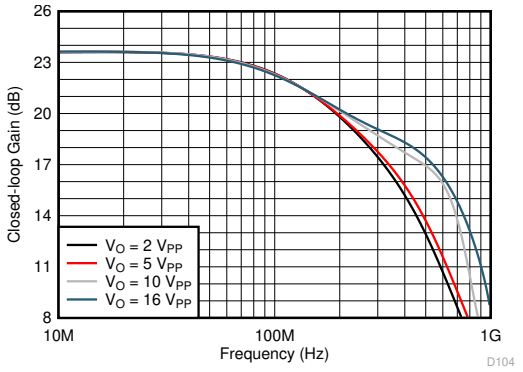
V_O = 2 V_{PP}

图 5-38. Small-Signal Frequency Response vs R_F



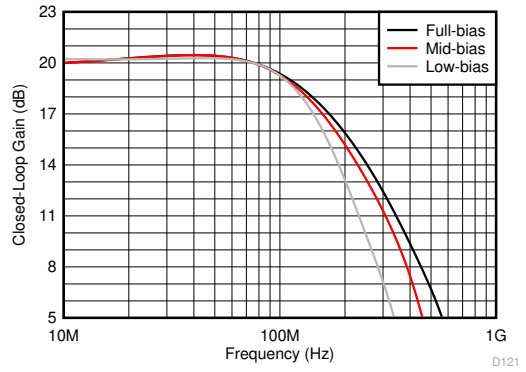
A_V = 10 V/V

图 5-39. Large-Signal Frequency Response vs V_O



A_V = 15 V/V

图 5-40. Large-Signal Frequency Response vs V_O



V_O = 40 V_{PP}

图 5-41. Large-Signal Frequency Response vs Bias Modes

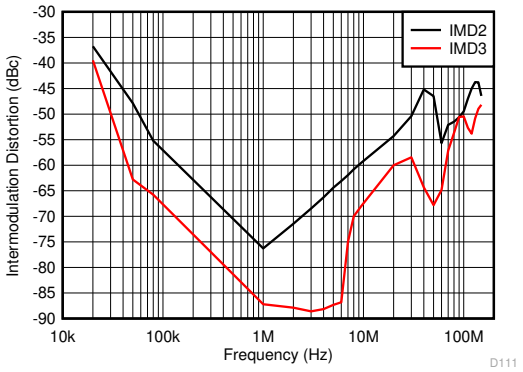
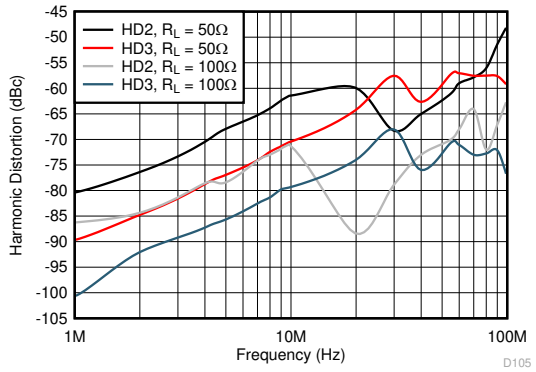


图 5-42. Intermodulation Distortion vs Frequency

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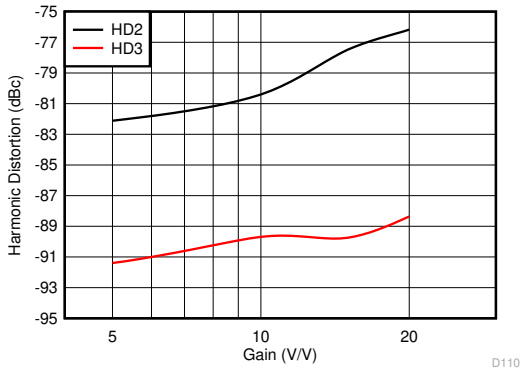
5.9 Typical Characteristics: V_S = 32 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 100 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



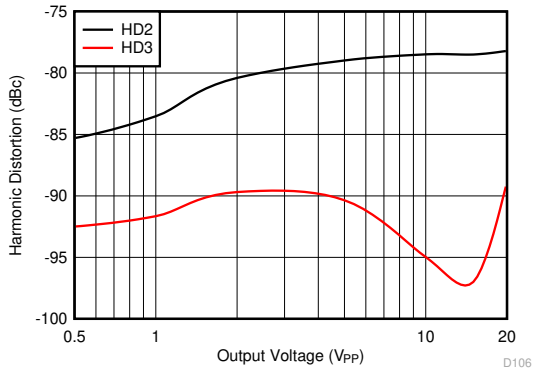
V_O = 2 V_{PP}

图 5-43. Harmonic Distortion vs Frequency



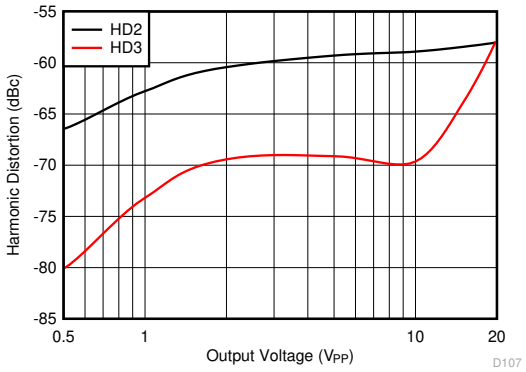
f = 1 MHz, V_O = 2 V_{PP} R_L = 50 Ω

图 5-44. Harmonic Distortion vs Gain



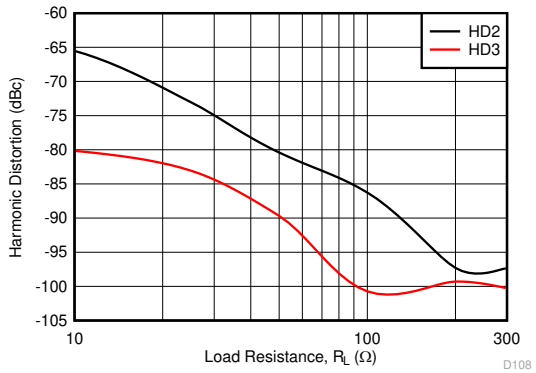
f = 1 MHz, R_L = 50 Ω

图 5-45. Harmonic Distortion vs V_O



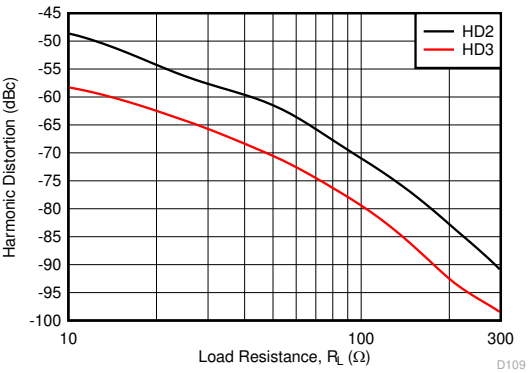
f = 10 MHz, R_L = 50 Ω

图 5-46. Harmonic Distortion vs V_O



f = 1 MHz, V_O = 2 V_{PP}

图 5-47. Harmonic Distortion vs R_L



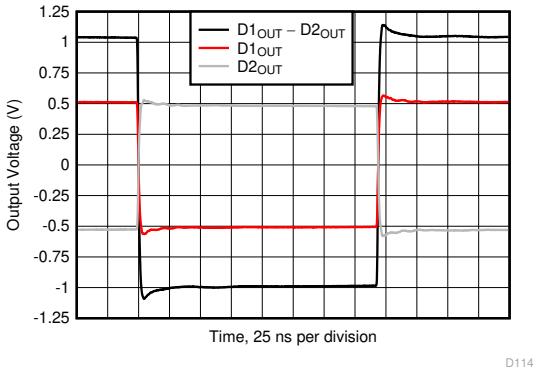
f = 10 MHz, V_O = 2 V_{PP}

图 5-48. Harmonic Distortion vs R_L

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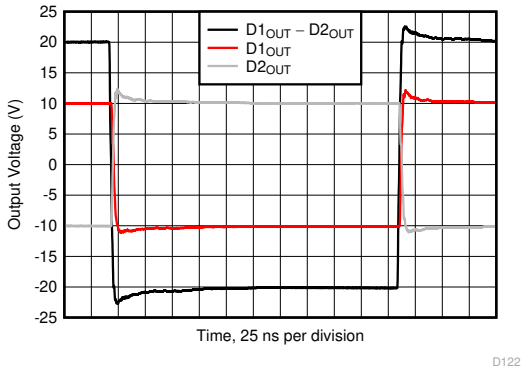
5.9 Typical Characteristics: V_S = 32 V (continued)

at $T_A \approx 25°C$, A_V = 10 V/V, R_F = 1.24 kΩ, R_L = 100 Ω, R_S = 2.5 Ω, R_{ADJ} = 0 Ω, full-bias mode, and VCM = open (unless otherwise noted)



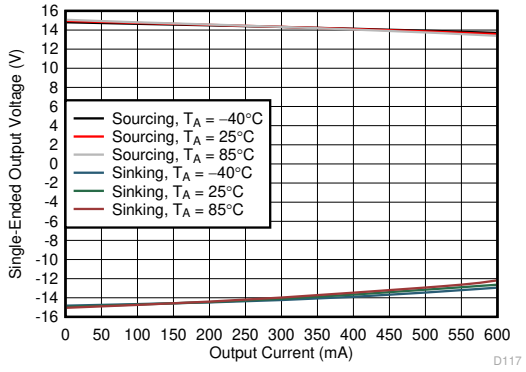
V_O step = 2 V_{PP}

图 5-49. Small-Signal Pulse Response



V_O step = 40 V_{PP}

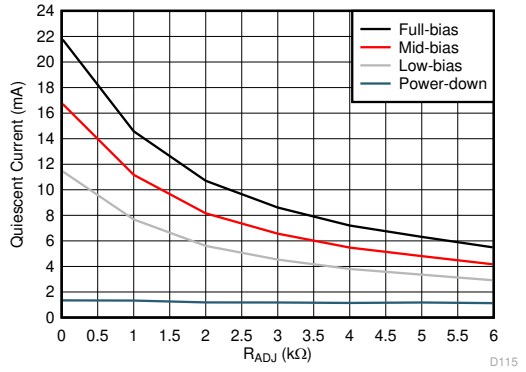
图 5-50. Large-Signal Pulse Response



Average of 30 devices

Output voltage was slammed and I_O was pulsed to maintain T_J as close to T_A as possible.

图 5-51. Single-Ended Output Voltage vs I_O and Temperature



Average of 30 devices

图 5-52. Quiescent Current vs R_{ADJ}

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6 Detailed Description

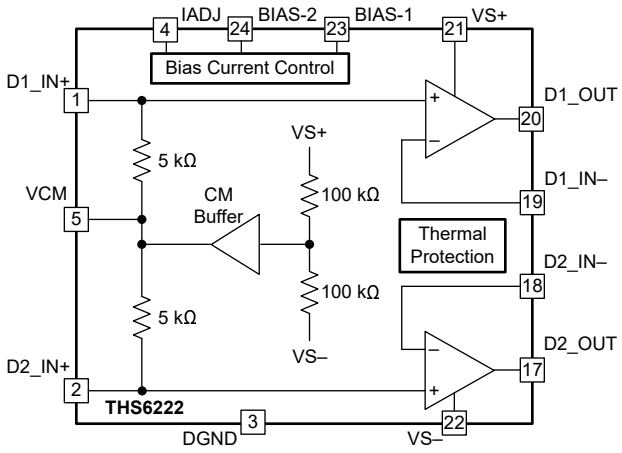
6.1 Overview

The THS6222 is a differential line-driver amplifier with a current-feedback architecture. The device is targeted for use in line-driver applications such as narrow-band and broadband power-line communications (PLC) that are often found in smart-metering and home-networking applications.

The THS6222 is designed as a single-port differential line driver. For the THS6222 to function as a drop-in replacement for the THS6212, tie the thermal pad to VS –. The integrated common-mode buffer featured in the THS6222 reduces the number of external components required for level shifting the input common-mode voltage in PLC applications that are often ac coupled, resulting in space savings on the circuit board and reducing the overall system cost. As a result of the THS6222 architecture, the two current-feedback amplifiers (D1 and D2) cannot be used independently; therefore, always drive these amplifiers differentially.

The architecture of the THS6222 is designed to provide maximum flexibility with adjustable power modes that are selectable based on application performance requirements, and also provide an external current adjustment pin (IADJ) to further optimize the quiescent power of the device. The wide output swing (18.6 V_{PP}) into 50-Ω differential loads with 12-V power supplies and high current drive of the THS6222 make the device an excellent choice for high-power, line-driving applications. By using 32-V power supplies and with good thermal design that keep the device within the safe operating temperature, the THS6222 is capable of swinging 57 V_{PP} into 100-Ω loads.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Common-Mode Buffer

The THS6222 is a differential line driver that features an integrated common-mode buffer. 图 7-2 shows that the most-common line-driving applications for the THS6222 are ac-coupled applications. Therefore, common-mode shift the inputs to confirm the input signals are within the common-mode specifications of the device. To maximize the dynamic range, the common-mode voltage is shifted to midsupply in most ac-coupled applications. With the integrated common-mode buffer, no external components are required to shift the input common-mode voltage. Engineers often choose to connect a noise-decoupling capacitor to the VCM pin. However, as shown in 图 6-1, assuming the circuit is reasonably shielded from external noise sources, no difference in common-mode noise is observed with the 100-nF capacitor or without the capacitor.

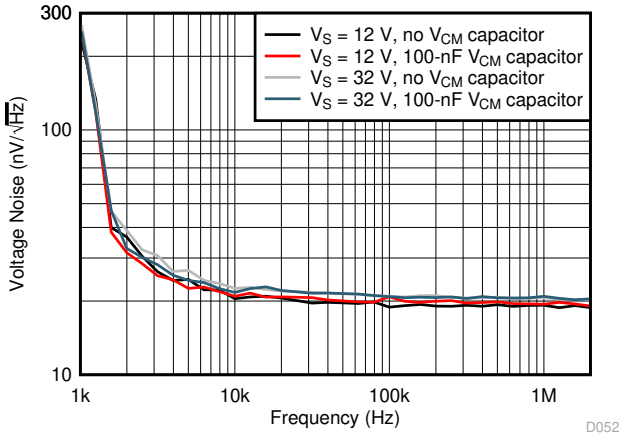


图 6-1. Common-Mode Voltage Noise Density vs Frequency

There are ESD protection diodes in series directly at the output of the common-mode buffer between the internal 520-Ω resistor and the common-mode buffer output. These diodes are referenced to midsupply. Any voltage that is 1.4 V greater or less than the midsupply applied to the VCM pin forward biases the protection diodes. This biasing results in either current flowing into or out of the VCM pin. The current is limited by the 520-Ω resistor in series, but to prevent permanent damage to the device, limit the current to the specifications in the *Absolute Maximum Ratings*.

6.3.2 Thermal Protection and Package Power Dissipation

The THS6222 is designed with thermal protection that automatically puts the device in shutdown mode when the junction temperature reaches approximately 175°C. In this mode, the device behavior is the same as if the bias pins are used to power-down the device. The device resumes normal operation when the junction temperature reaches approximately 145°C. In general, the thermal shutdown condition must be avoided. If and when the thermal protection triggers, thermal cycling occurs where the device repeatedly goes in and out of thermal shutdown until the junction temperature stabilizes to a value that prevents thermal shutdown.

A common technique to calculate the maximum power dissipation that a device can withstand is by using the junction-to-ambient thermal resistance ($R_{\theta JA}$), provided in the *Thermal Information* table. Using the equation power dissipation = (junction temperature, T_J – ambient temperature, T_A) / $R_{\theta JA}$, the amount of power a package can dissipate can be estimated. 图 6-2 illustrates the package power dissipation based on this equation to reach junction temperatures of 125°C and 150°C at various ambient temperatures. The $R_{\theta JA}$ value is determined using industry standard JEDEC specifications and allows ease of comparing various packages. Power greater than that in 图 6-2 can be dissipated in a package by good printed circuit board (PCB) thermal design, using heat sinks, and or active cooling techniques. See the *Thermal Design By Insight, Not Hindsight* application report for an in-depth discussion on thermal design.

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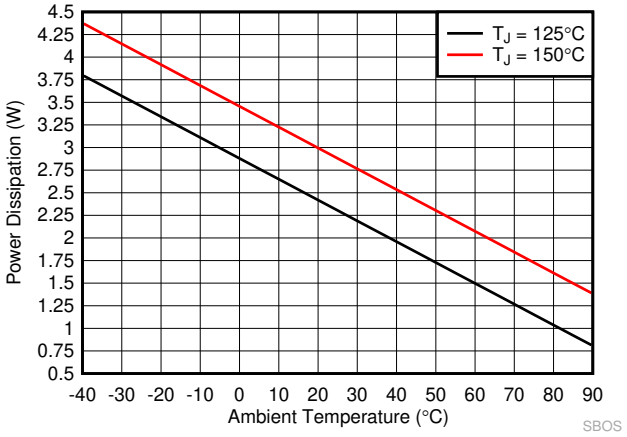
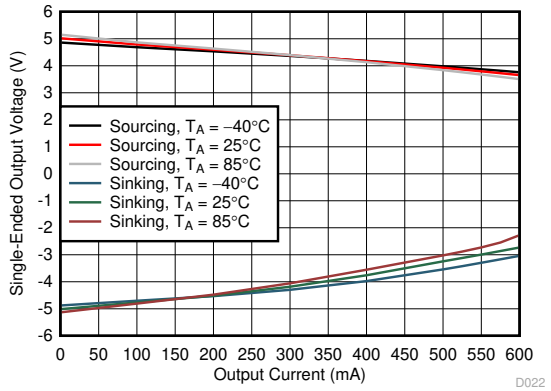


图 6-2. Package Power Dissipation vs Ambient Temperature

6.3.3 Output Voltage and Current Drive

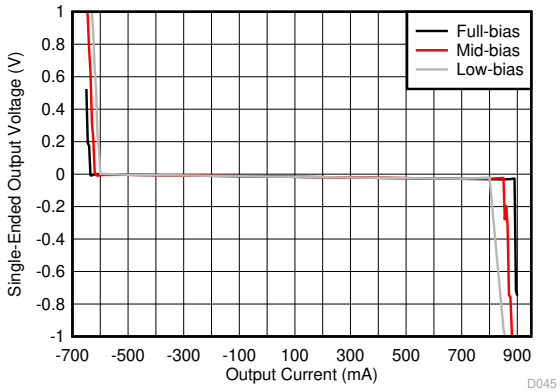
The THS6222 provides output voltage and current capabilities that are unsurpassed in a low-cost, monolithic op amp. Under no load at room temperature, the output voltage typically swings closer than 1.1 V to either supply rail and typically swings to within 1.1 V of either supply with a 100-Ω differential load. The THS6222 can deliver over 350 mA of current with a 25-Ω load.

Good thermal design of the system is important (including use of heat sinks and active cooling methods) if the THS6222 is pushed to the limits of the output drive capabilities. 图 6-3 and 图 6-4 show the output drive of the THS6222 under two different sets of conditions where T_A is approximately equal to T_J. In practical applications, T_J is often much higher than T_A and highly depends on the device configuration, signal parameters, and PCB thermal design. To represent the full output-drive capability of the THS6222 in 图 6-3 and 图 6-4, $T_J \approx T_A$ is achieved by pulsing or sweeping the output current for a duration of less than 100 ms.



V_S = 12 V, $T_J \approx T_A$

图 6-3. Slammed Single-Ended Output Voltage vs I_O and Temperature



V_S = 12 V, $T_J \approx T_A \approx$ 25°C

图 6-4. Linear Single-Ended Output Voltage vs I_O and Temperature

In 图 6-3, the output voltages are differentially slammed to the rail and the output current is single-endedly sourced or sunk using a source measure unit (SMU) for less than 100 ms. The single-ended output voltage of each output is then measured prior to removing the load current. After removing the load current, the outputs are brought back to mid-supply before repeating the measurement for different load currents. This entire process is repeated for each ambient temperature. Under the slammed output voltage condition of 图 6-3, the output transistors are in saturation and the transistors start going into linear operation as the output swing is backed off for a given I_O,

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In 图 6-4, the inputs are floated and the output voltages are allowed to settle to the mid-supply voltage. The load current is then single-endedly swept for sourcing (greater than 0 mA) and sinking (less than 0 mA) conditions and the single-ended output voltage is measured at each current-forcing condition. The current sweep is completed in a few seconds (approximately 3 s to 4 s) so as not to significantly raise the junction temperature (T_J) of the device from the ambient temperature (T_A). The output is not swinging and the output transistors are in linear operation in 图 6-4 until the current drawn exceeds the device capabilities, at which point the output voltage starts to deviate quickly from the no load output voltage.

To maintain maximum output stage linearity, output short-circuit protection is not provided. This absence of short-circuit protection is normally not a problem because most applications include a series-matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin, in most cases, permanently damages the amplifier.

6.3.4 Breakdown Supply Voltage

To estimate the margin beyond the maximum supply voltage specified in the *Absolute Maximum Ratings* table and exercise the robustness of the device, several typical units were tested beyond the specifications in the *Absolute Maximum Ratings* table. 图 6-5 shows the configuration used for the test. The supply voltage, V_S, was swept manually and quiescent current was recorded at each 0.5-V supply voltage increment. 图 6-6 shows the results of the single-supply voltage where the typical units started breaking. Under a similar configuration as the one shown in 图 6-5, a unit was subjected to V_S = 42 V for 168 hours and tested for quiescent current at the beginning and at the end of the test. There was no notable difference in the quiescent current before and after the 168 hours of testing and the device did not show any signs of damage or abnormality.

The primary objective of these tests was to estimate the margins of robustness for typical devices and does not imply performance or maximum limits beyond those specified in the *Absolute Maximum Ratings* and *Recommended Operating Conditions* tables.

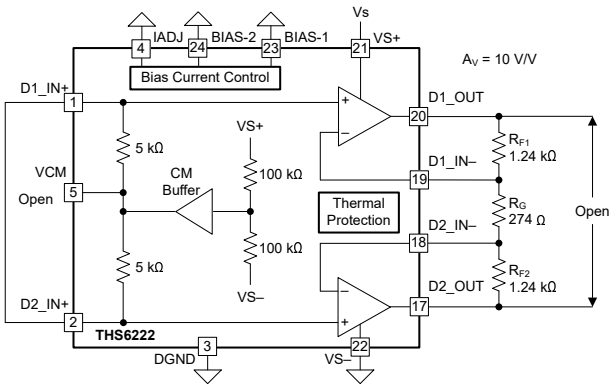


图 6-5. Breakdown Supply Voltage Test Configuration

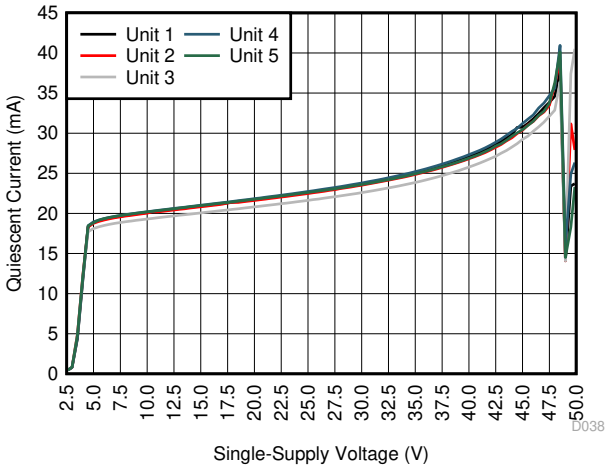


图 6-6. Typical Device Breakdown Supply Voltage (T_A = 27°C)

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6.3.5 Surge Test Results

Line drivers such as the THS6222 often directly interface with power lines through a transformer and various protection components in high-speed power line communications (HPLC) smart-meters and digital subscriber line (DSL) applications. Surge testing is an important requirement for such applications. To validate the performance and surge survivability of the THS6222, the THS6222 circuit configuration shown in 图 6-7 was subjected to a ±4-kV common-mode surge and a ±2-kV differential-mode surge. The common-mode and differential-mode surge voltages were applied at V_{CM} and V_{DIFF}, respectively, in 图 6-7. The 1.2/50-µs surge profile was used per the IEC 61000-4-5 test with R_{EQ} = 42 Ω, as explained in the *TI's IEC 61000-4-x Tests and Procedures* application report. Five devices were tested in full-bias and shutdown modes, and were subjected to the surge five times for each polarity. No device showed any discernible change in quiescent current after being subjected to the surge test, and the out-of-band suppression tests did not show any performance deterioration either; see 图 6-8 through 图 6-11 for the state grid corporation of China (SGCC) HPLC bands.

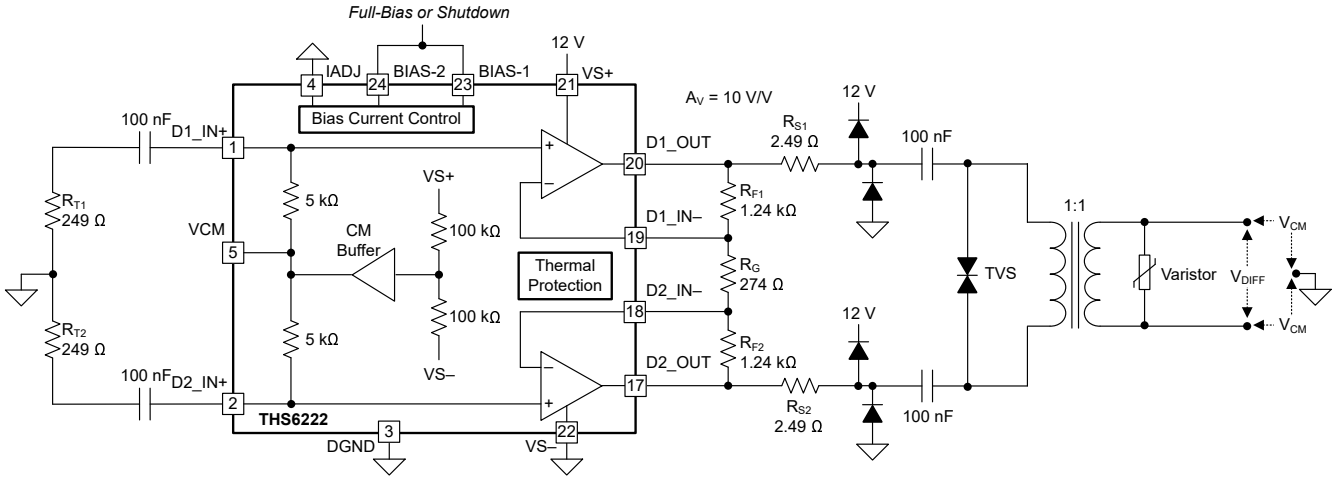


图 6-7. Surge Test Configuration

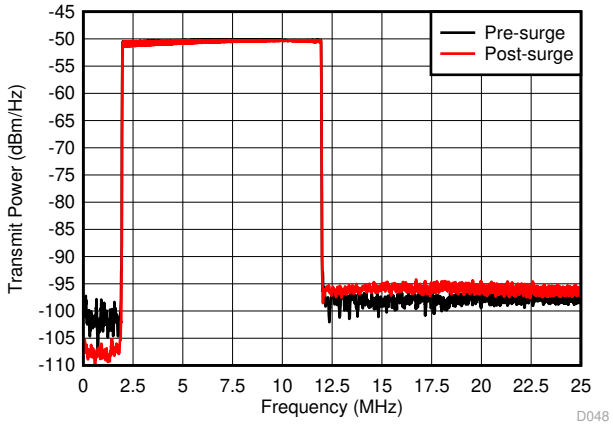


图 6-8. China SGCC HPLC Band0 Pre-Surge and Post-Surge

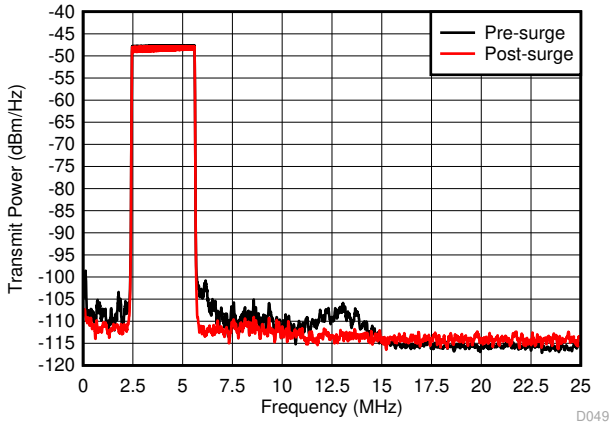


图 6-9. China SGCC HPLC Band1 Pre-Surge and Post-Surge

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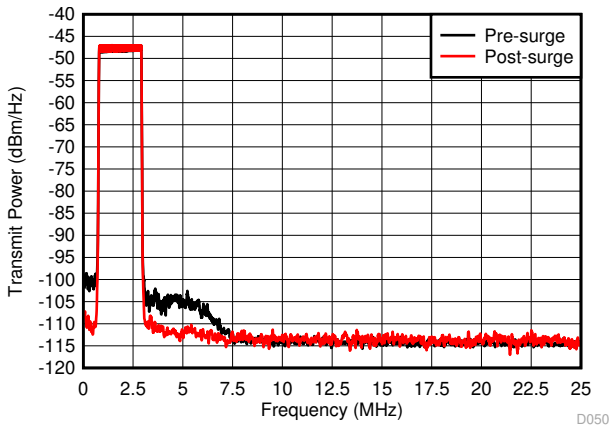


图 6-10. China SGCC HPLC Band2 Pre-Surge and Post-Surge

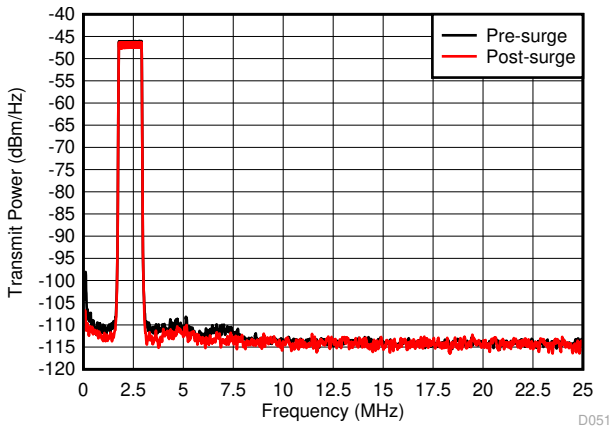


图 6-11. China SGCC HPLC Band3 Pre-Surge and Post-Surge

6.4 Device Functional Modes

The THS6222 has four different functional modes set by the BIAS-1 and BIAS-2 pins. 表 6-1 shows the truth table for the device mode pin configuration and the associated description of each mode.

表 6-1. BIAS-1 and BIAS-2 Logic Table

BIAS-1	BIAS-2	FUNCTION	DESCRIPTION
0	0	Full-bias mode (100%)	Amplifiers on with lowest distortion possible
1	0	Mid-bias mode (75%)	Amplifiers on with power savings and a reduction in distortion performance
0	1	Low-bias mode (50%)	Amplifiers on with enhanced power savings and a reduction of overall performance
1	1	Shutdown mode	Amplifiers off and output is high impedance

If the PLC application requires switching the line driver between all four power modes and if the PLC application-specific integrated circuit (ASIC) has two control bits, then the two control bits can be connected to the bias pins BIAS-1 and BIAS-2 for switching between any of the four power modes. Most PLC applications, however, only require the line driver to switch between one of the three active power modes and the shutdown mode. This type of 1-bit power mode control is illustrated in 图 7-1, where the line driver can be switched between the full-bias and shutdown modes using just one control bit from the PLC ASIC. If switching between the mid-bias or low-bias modes and the shutdown mode is required for the application, then either the BIAS-1 or BIAS-2 pin can be connected to ground and the control pin from the PLC ASIC can be connected to the non-grounded BIAS pin.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The THS6222 is typically used for high output power line-driving applications with various load conditions, as is often the case in power line communications (PLC) applications. In the *Typical Applications* section, the amplifier is presented in a typical, broadband, current-feedback configuration driving a 50 Ω line load; however, the amplifier is also applicable for many different general-purpose and specific line-driving applications beyond what is shown in the *Typical Applications* section.

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7.2 Typical Applications

7.2.1 Broadband PLC Line Driving

The THS6222 provides the exceptional ac performance of a wideband current-feedback op amp with a highly linear, high-power output stage. The low output headroom requirement and high output current drive capability makes the THS6222 an excellent choice for 12 V PLC applications. The primary advantage of a current-feedback op amp such as the THS6222 over a voltage-feedback op amp is that the ac performance (bandwidth and distortion) is relatively independent of signal gain. 图 7-1 shows a typical ac-coupled broadband PLC application circuit where a current-output digital-to-analog converter (DAC) of the PLC application-specific integrated circuit (ASIC) drives the inputs of the THS6222. Though 图 7-1 shows the THS6222 interfacing with a current-output DAC, the THS6222 can just as easily be interfaced with a voltage-output DAC by using much larger terminating resistors, R_{T1} and R_{T2}.

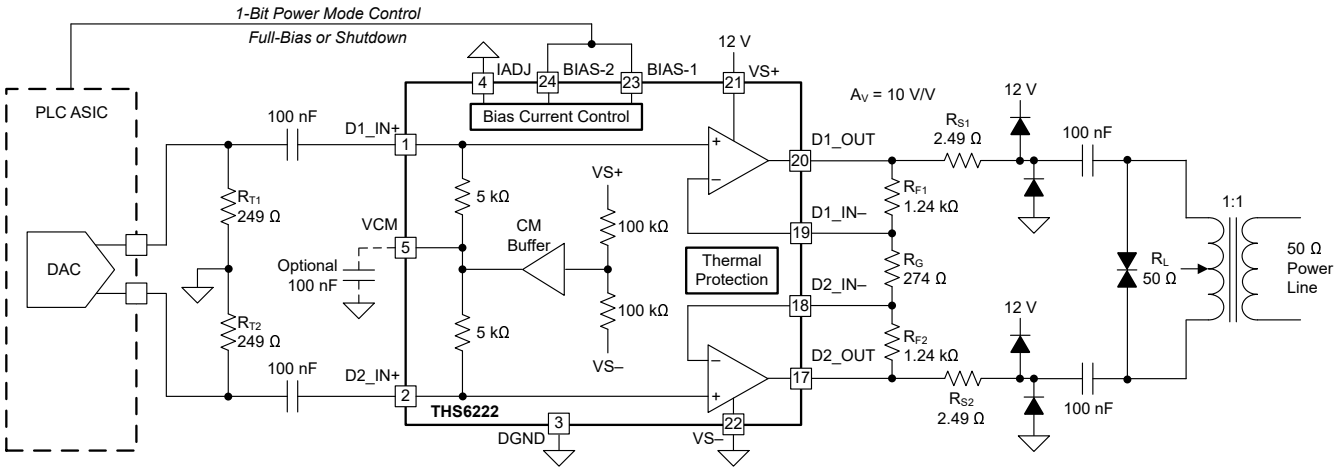


图 7-1. Typical Broadband PLC Configuration

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7.2.1.1 Design Requirements

The main design requirements for an ac-coupled wideband current-feedback operation are to choose power supplies that satisfy the output voltage requirement, and also to use a feedback resistor value that allows for the proper bandwidth while maintaining stability. Use the design requirements shown in 表 7-1 to design a broadband PLC application circuit.

表 7-1. Design Requirements

DESIGN PARAMETER	VALUE
Power supply	12 V, single-supply
Differential gain, A_V	10 V/V
Spectrum profile	China SGCC HPLC band0, band1, band2, and band3
In-band power spectral density	– 50 dBm/Hz
Minimum out-of-band suppression	35 dB

7.2.1.2 Detailed Design Procedure

The closed-loop gain equation for a differential line driver such as the THS6222 is given as $A_V = 1 + 2 \times (R_F / R_G)$, where $R_F = R_{F1} = R_{F2}$. The THS6222 is a current-feedback amplifier and thus the bandwidth of the closed-loop configuration is set by the value of the R_F resistor. This advantage of the current-feedback architecture allows for flexibility in setting the differential gain by choosing the value of the R_G resistor without reducing the bandwidth as is the case with voltage-feedback amplifiers. The THS6222 is designed to provide excellent bandwidth performance with $R_{F1} = R_{F2} = 1.24$ kΩ. To configure the device in a gain of 10 V/V, the R_G resistor is chosen to be 274 Ω. See the TI Precision Labs for more details on how to choose the R_F resistor to optimize the performance of a current-feedback amplifier.

Often, a key requirement for PLC applications is the out-of-band suppression specifications. The in-band frequencies carry the encoded data with a certain power level. The line driver must not generate any spurs beyond a certain power level outside the in-band spectrum. In the design requirements of this application example, the minimum out-of-band suppression specification of 35 dB means there must be no frequency spurs in the out-of-band spectrum beyond the – 80 dBm/Hz power spectral density, considering the in-band power spectral density is – 50 dBm/Hz.

The circuit shown in 图 7-2 measures the out-of-band suppression specification. The minor difference in components between the circuits of 图 7-1 and 图 7-2 does not have any significant impact on the out-of-band suppression results.

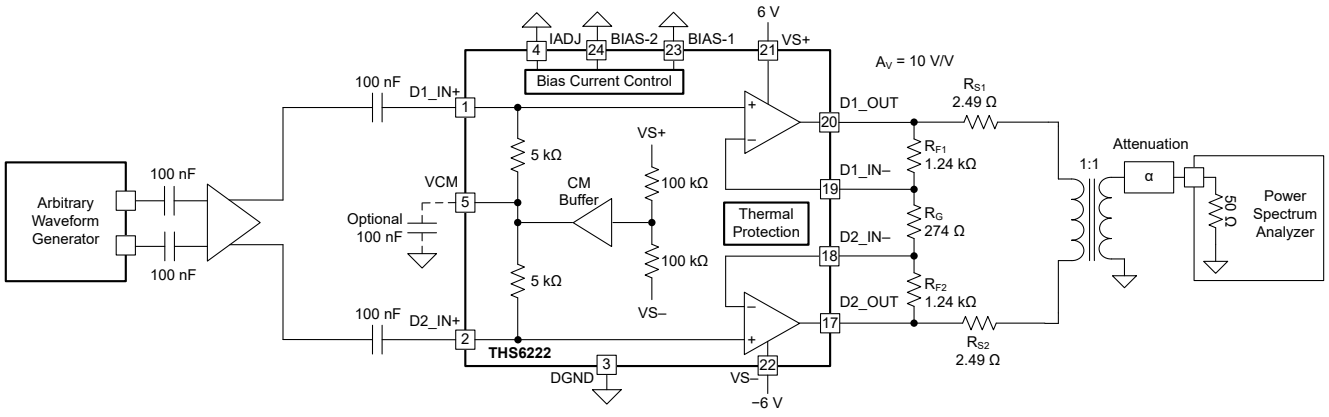


图 7-2. Measurement Test Circuit for Out-of-Band Suppression

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7.2.1.3 Application Curve

图 7-3 shows the out-of-band suppression measurement results of the circuit. Out-of-band suppression is a good indicator of the linearity performance of the device. The results in 图 7-3 show over 40 dB of out-of-band suppression, which is well beyond the 35 dB requirement and indicative of the excellent linearity performance of the THS6222.

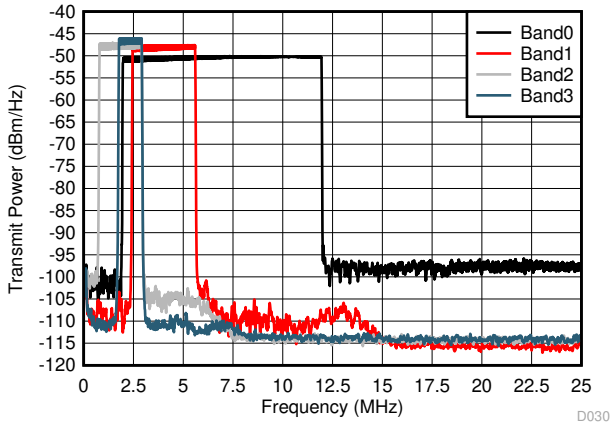


图 7-3. Out-of-Band Suppression

7.3 Best Design Practices

7.3.1 Do

- Include a thermal design at the beginning of the project.
- Use well-terminated transmission lines for all signals.
- Use solid metal layers for the power supplies.
- Keep signal lines as straight as possible.
- Keep the traces carrying differential signals of the same length.

7.3.2 Do Not

- Do not use a lower supply voltage than necessary.
- Do not use thin metal traces to supply power.
- Do not treat the D1 and D2 amplifiers as independent single-ended amplifiers.

7.4 Power Supply Recommendations

The THS6222 supports single-supply and split-supply power supplies, as well as balanced and unbalanced bipolar supplies. The device has a wide supply range of 8 V (– 3 V to +5 V) to 32 V (±16 V). Choose power-supply voltages that allow for adequate swing on both the inputs and outputs of the amplifier to prevent affecting device performance. Operating from a single supply can have numerous advantages. With the negative supply at ground, the errors resulting from the – PSRR term can be minimized. The DGND pin provides the ground reference for the bias control pins. For applications that use split bipolar supplies, care must be taken to design within the DGND voltage specifications and must be within V_{S-} to (V_{S+} – 5 V); the DGND pin must be a minimum bias of 5 V. Thus, the minimum positive supply that can be used in split-supply applications is V_{S+} = 5 V. The negative supply, V_{S-}, can then be set to a voltage anywhere in between – 3 V and – 27 V, as per the *Recommended Operating Conditions* specifications.

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7.5 Layout

7.5.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the THS6222 requires careful attention to board layout parasitic and external component types. The THS6222RHFEVM can be used as a reference when designing the circuit board. Recommendations that optimize performance include:

1. Minimize parasitic capacitance to any ac ground for all signal I/O pins. Parasitic capacitance, particularly on the output and inverting input pins, can cause instability; on the noninverting input, this capacitance can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins must be opened in all ground and power planes around these pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. Minimize the distance (less than 0.25 in, or 6.35 mm) from the power-supply pins to high-frequency 0.1 µF decoupling capacitors. At the device pins, the ground and power plane layout must not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves second-harmonic distortion performance. Larger (2.2 µF to 6.8 µF) decoupling capacitors, effective at lower frequencies, must also be used on the main supply pins. These capacitors can be placed somewhat farther from the device and can be shared among several devices in the same area of the PCB.
3. Careful selection and placement of external components preserves the high-frequency performance of the THS6222. Resistors must be of a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition, axially-leaded resistors can also provide good high-frequency performance.

   Again, keep leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Where double-side component mounting is required, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value, as described in 节 *7.2.1*. Increasing the value reduces the bandwidth, whereas decreasing the value leads to a more peaked frequency response. The 1.24 kΩ feedback resistor used in 节 *5.8* is a good starting point for a gain of 10 V/V design.
4. Connections to other wideband devices on the board can be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50-mils to 100-mils, 0.050-in to 0.100-in, or 1.27-mm to 2.54-mm) must be used, preferably with ground and power planes opened up around them.
5. Socketing a high-speed part such as the THS6222 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, and can make achieving a smooth, stable frequency response almost impossible. Best results are obtained by soldering the THS6222 directly onto the board.
6. Use the V_{S-} plane to conduct the heat out of the package. The package attaches the die directly to an exposed thermal pad on the bottom, and must be soldered to the board. This pad must be connected electrically to the same voltage plane as the most negative supply voltage (V_{S-}) applied to the THS6222. Place as many vias as possible on the thermal pad connection and connect the vias to a heat spreading plane that is at the same potential as V_{S-} on the bottom side of the PCB.

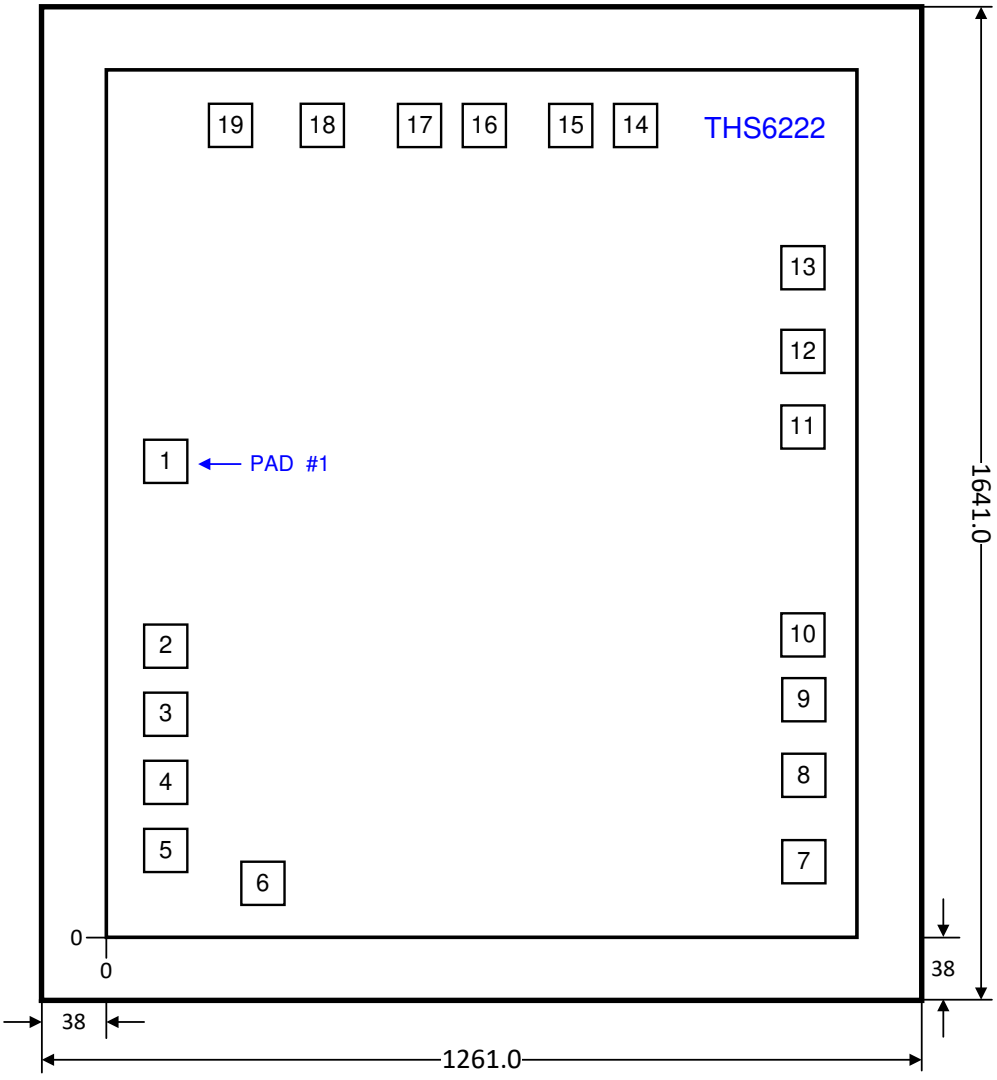
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7.5.1.1 Wafer and Die Information

表 7-2 lists wafer and bond pad information for the YS package.

表 7-2. Wafer and Bond Pad Information

WAFER BACKSIDE FINISH	WAFER THICKNESS	BACKSIDE POTENTIAL	BOND PAD METALLIZATION	BOND PAD DIMENSIONS (X × Y)
Silicon without backgrind	25 mils	Must be connected to the lowest voltage potential on the die (generally V_{S-})	Al	76.0 µm × 76.0 µm



All dimensions are in micrometers (µm).

图 7-4. Die Dimensions

表 7-3 lists the bond pad locations for the YS package. All dimensions are in micrometers (μm).

表 7-3. Bond Pad Locations

PAD NUMBER	PAD NAME	X MIN	Y MIN	X MAX	Y MAX	DESCRIPTION
1	D1_IN+	71.050	878.875	147.050	954.875	Amplifier D1 noninverting input
2	D2_IN+	71.050	525.125	147.050	601.125	Amplifier D2 noninverting input
3	DGND	71.050	384.025	147.050	460.025	Ground reference for bias control pins
4	IADJ	71.050	267.025	147.050	343.025	Bias current adjustment pin
5	VCM	71.050	150.025	147.050	226.025	Common-mode buffer output
6	VS –	209.175	85.925	285.175	161.925	Negative power-supply connection
7	VS+	1007.475	95.500	1083.475	171.500	Positive power-supply connection
8	D2_OUT	1007.475	222.500	1083.475	298.500	Amplifier D2 output (must be used for D2 output)
9	D2_OUT (OPT)	1007.475	369.900	1083.475	445.900	Optional amplifier D2 output (can be left unconnected or connected to pad 8)
10	D2_IN –	1007.475	487.375	1083.475	563.375	Amplifier D2 inverting input
11	D1_IN –	1007.450	919.375	1083.450	995.375	Amplifier D1 inverting input
12	D1_OUT (OPT)	1007.475	1034.100	1083.475	1110.100	Optional amplifier D1 output (pad can be left unconnected or connected to pad 13)
13	D1_OUT	1007.475	1181.500	1083.475	1257.500	Amplifier D1 output (must be used for D1 output)
14	VS+	851.675	1417.950	927.675	1493.950	Positive power-supply connection
15	VS+	718.900	1417.950	794.900	1493.950	Positive power-supply connection
16	VS –	557.375	1417.950	633.375	1493.950	Negative power-supply connection
17	VS –	424.600	1417.950	500.600	1493.950	Negative power-supply connection
18	BIAS-1	293.075	1417.750	369.075	1493.750	Bias mode parallel control, LSB
19	BIAS-2	159.250	1417.750	235.250	1493.750	Bias mode parallel control, MSB

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7.5.2 Layout Examples

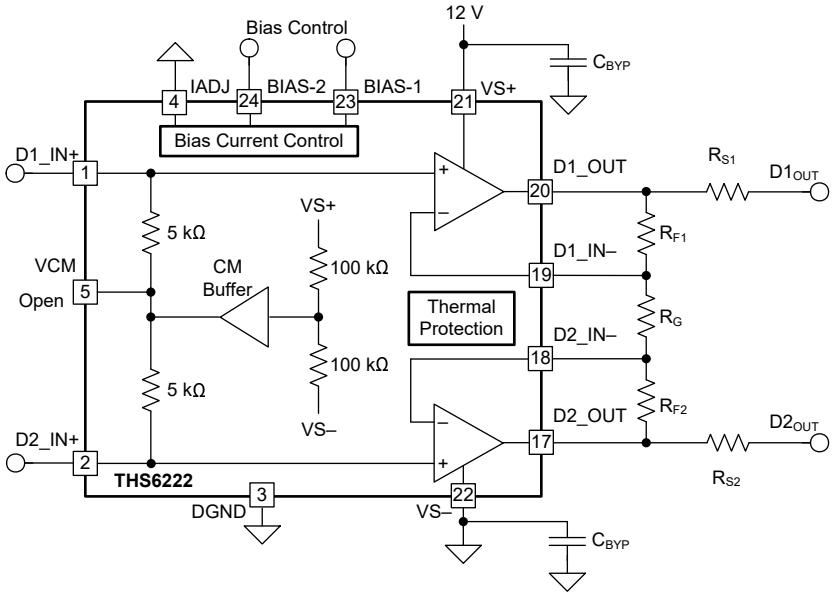


图 7-5. Representative Schematic for the Layout in 图 7-6

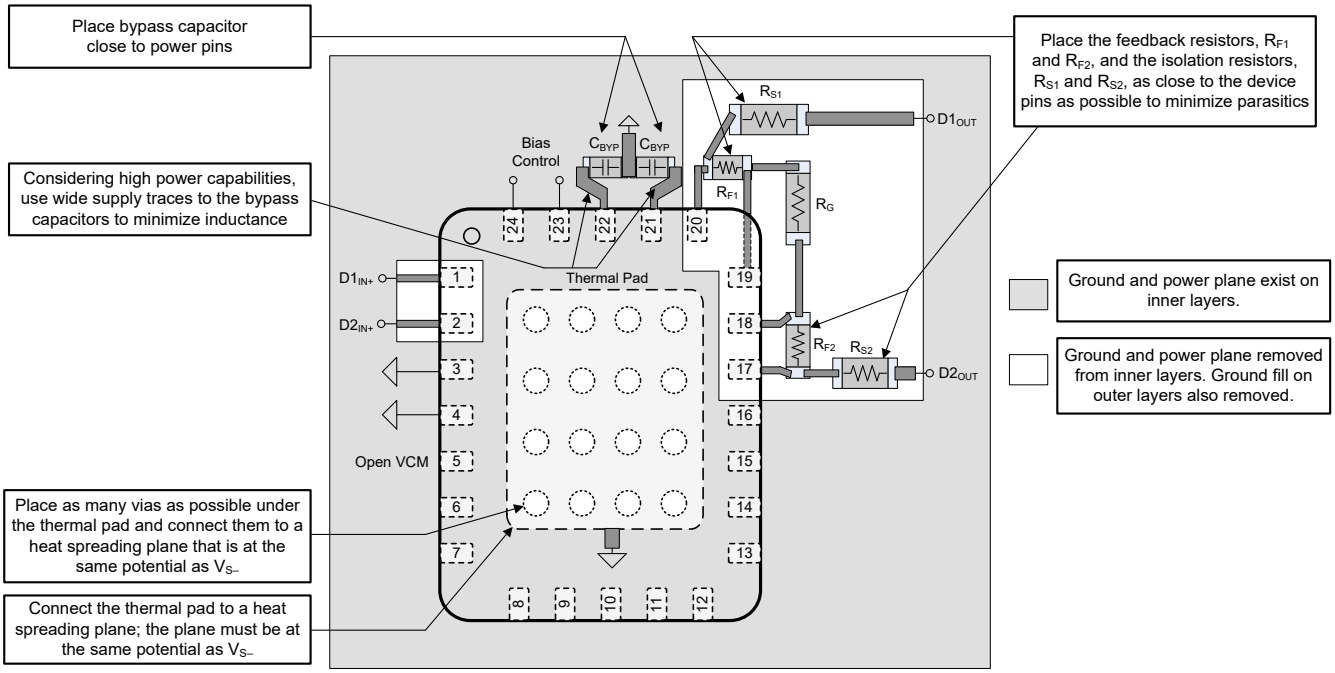


图 7-6. Layout Recommendations

8 Device and Documentation Support

8.1 Development Support

TI Precision Labs

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *THS6212 Differential Broadband PLC Line Driver Amplifier* data sheet
- Texas Instruments, *THS6214 Dual-Port, Differential, VDSL2 Line Driver Amplifiers* data sheet
- Texas Instruments, *Thermal Design By Insight, Not Hindsight* application report
- Texas Instruments, *TI's IEC 61000-4-x Tests and Procedures* application report
- Texas Instruments, *THS6222 Evaluation Module* user's guide

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (October 2024) to Revision F (December 2024)	Page
• 在*应用* 中为 SEO 的 PLC 标准添加了说明	1
• 在*说明* 中为 SEO 的 PLC 标准添加了说明	1
• 更新了首页上的*功能方框图* 以及图 6-5、6-7、7-1、7-2 和 7-5 以修复错误的引脚交换和标签	1

Changes from Revision D (April 2021) to Revision E (October 2024)	Page
• 更新了最后一个*特性* 要点，以阐明与 THS6212 的兼容性	1

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- Deleted maximum junction temperature continuous operation, long-term reliability from *Absolute Maximum Ratings* 5
- Updated drop-in replacement text in *Overview* section..... 21

Changes from Revision C (November 2020) to Revision D (April 2021) **Page**

- Updated the wrong pin diagram image that was tagged incorrectly during system migration.....3

Changes from Revision B (April 2020) to Revision C (November 2020) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式.....1
- 向 *器件信息* 表中添加了 VQFN (16) 封装.....1
- Updated the RHF package in the *Pin Configuration and Functions* section.....3
- Added the RGT package in the *Pin Configuration and Functions* section.....3

Changes from Revision A (December 2019) to Revision B (April 2020) **Page**

- 向 *器件信息* 表添加了晶圆销售封装和本体尺寸（标称值）..... 1
- Added the YS die bondpad and functions..... 3
- Updated Table 1 BIAS-1 and BIAS-2 Logic Table..... 26
- Added Wafer and Die Information section..... 31

Changes from Revision * (August 2019) to Revision A (December 2019) **Page**

- 将器件状态从预告信息更改为生产数据..... 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS6222IRGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	TH6222
THS6222IRGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	TH6222
THS6222IRGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	TH6222
THS6222IRHFR	Active	Production	VQFN (RHF) | 24	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	(THS, THS6222) 6222
THS6222IRHFR.B	Active	Production	VQFN (RHF) | 24	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	(THS, THS6222) 6222
THS6222IRHFT	Active	Production	VQFN (RHF) | 24	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	(THS, THS6222) 6222
THS6222IRHFT.B	Active	Production	VQFN (RHF) | 24	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	(THS, THS6222) 6222
THS6222YS	Active	Production	WAFERSALE (YS) | 0	1 | OTHER	-	Call TI	Call TI	-40 to 85	
THS6222YS.B	Active	Production	WAFERSALE (YS) | 0	1 | OTHER	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

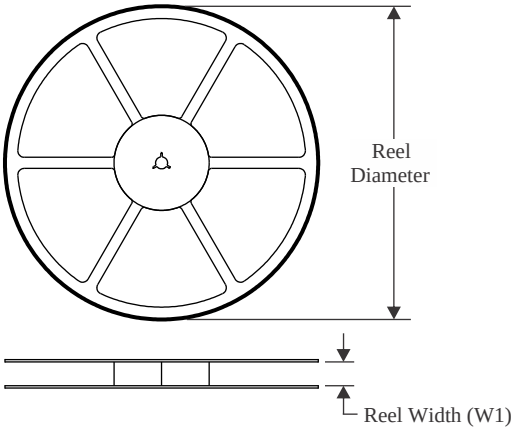
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

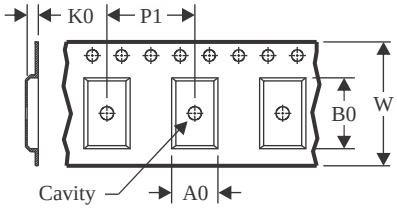
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

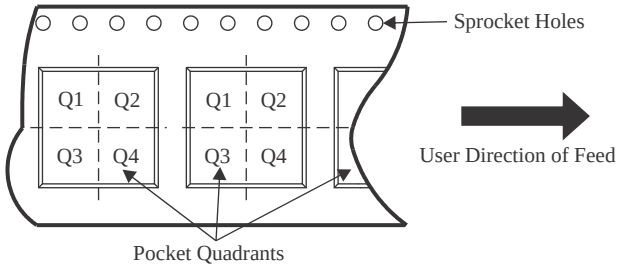


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

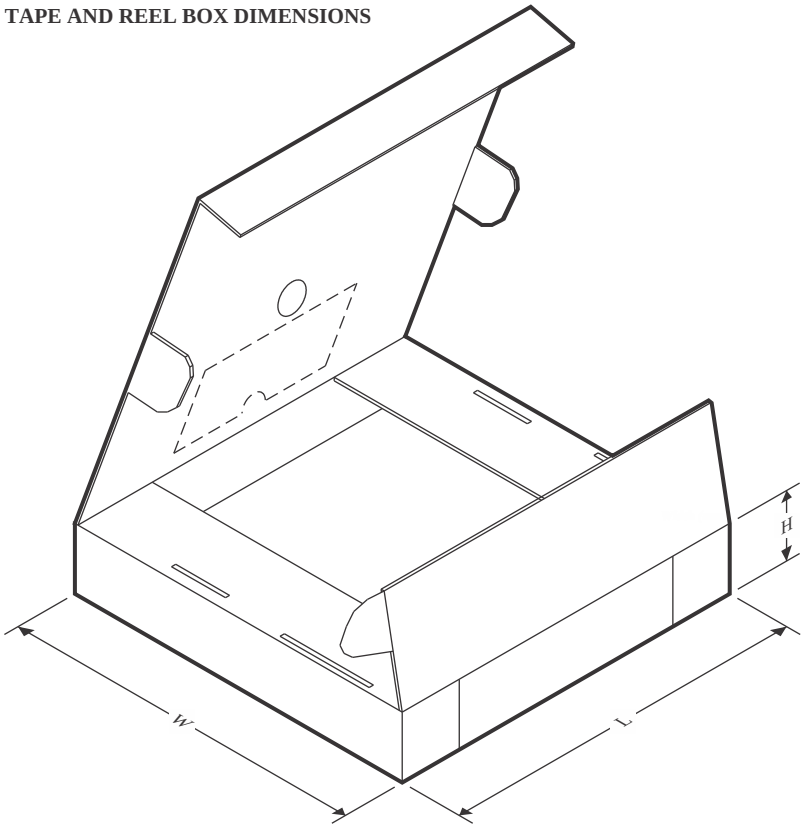
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6222IRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THS6222IRHFR	VQFN	RHF	24	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1
THS6222IRHFT	VQFN	RHF	24	250	180.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

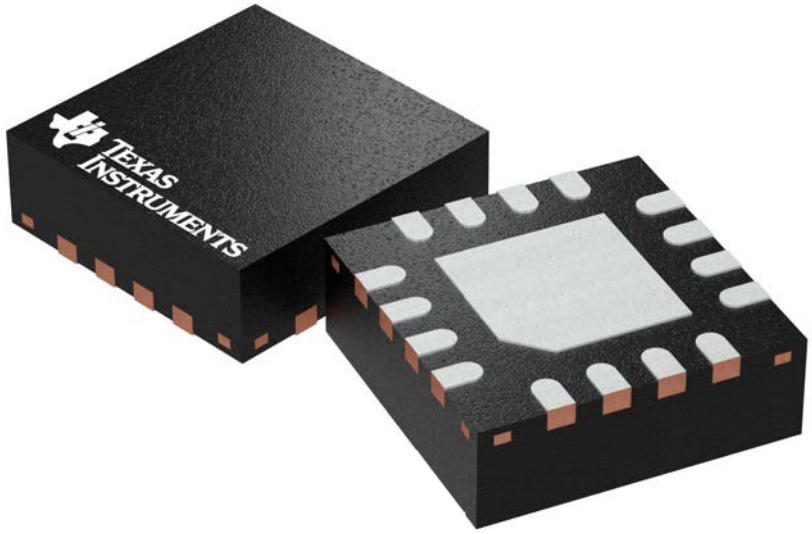


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6222IRGTR	VQFN	RGT	16	3000	360.0	360.0	36.0
THS6222IRHFR	VQFN	RHF	24	3000	356.0	356.0	36.0
THS6222IRHFT	VQFN	RHF	24	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



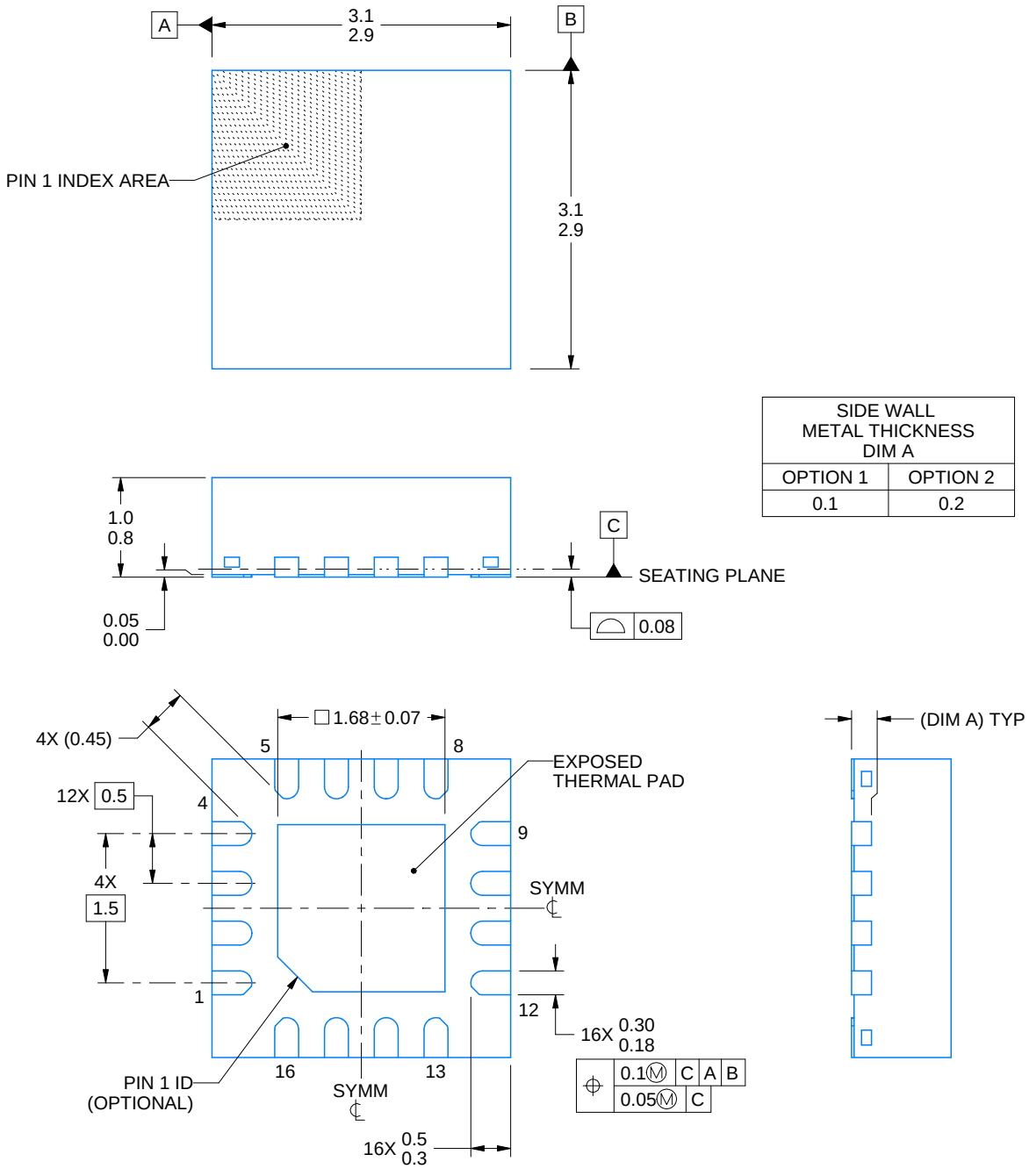
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

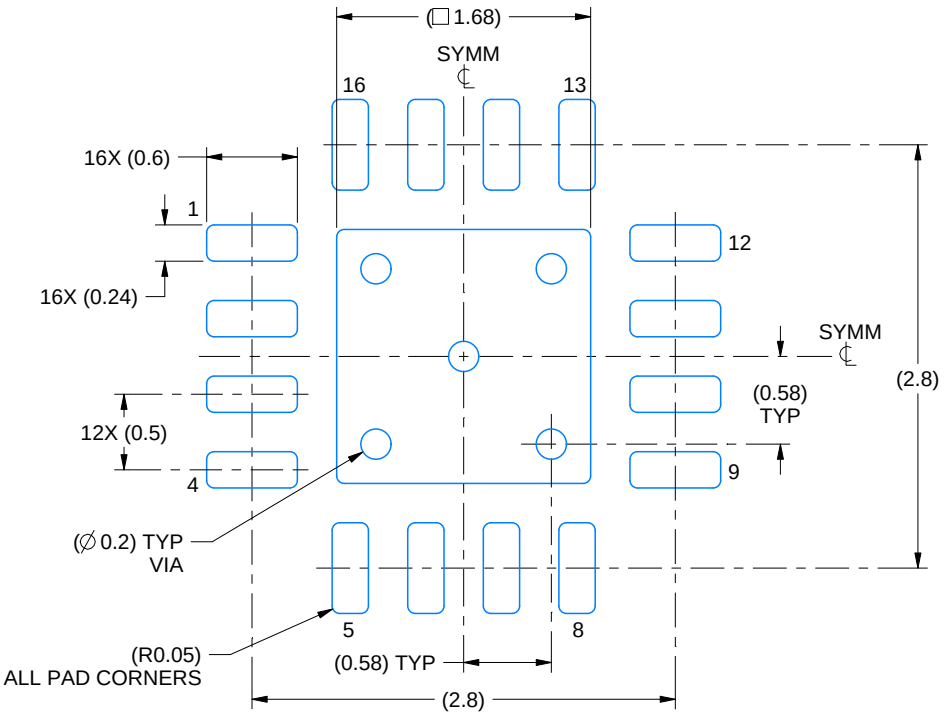
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

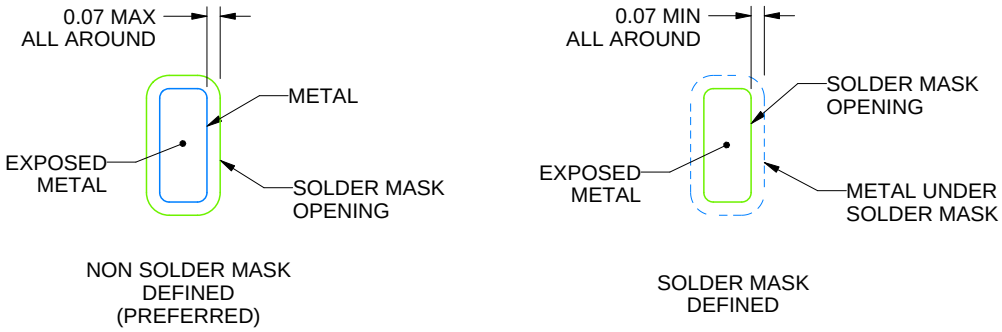


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

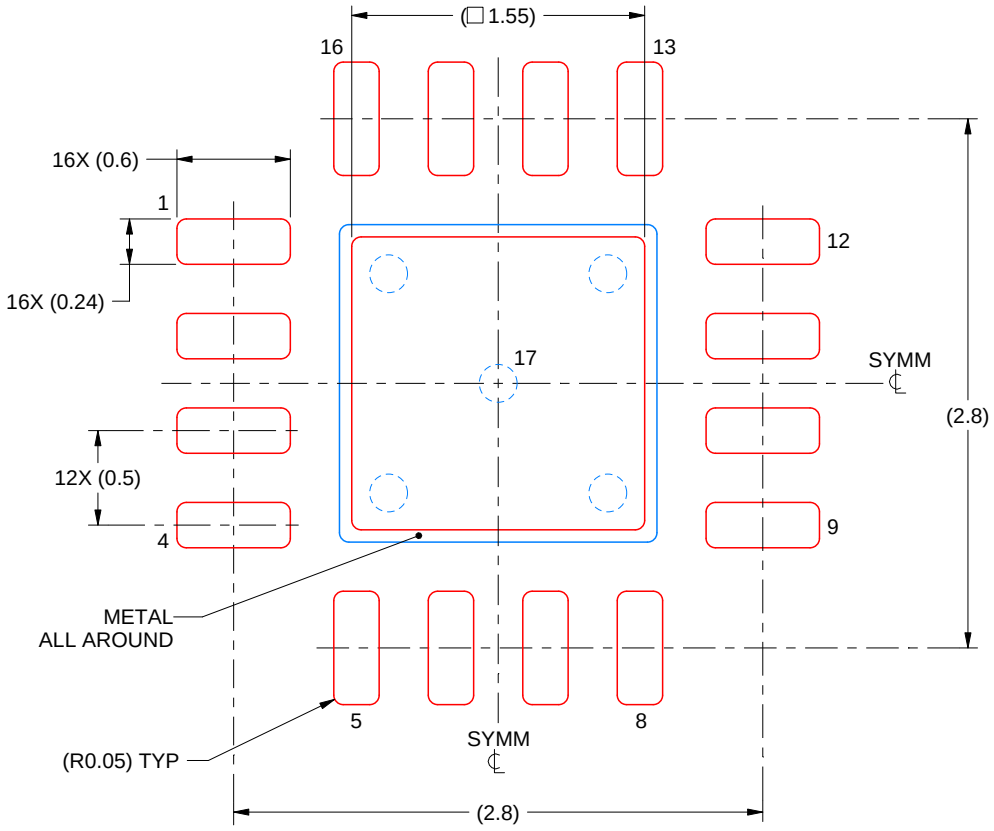


SOLDER MASK DETAILS

4222419/E 07/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

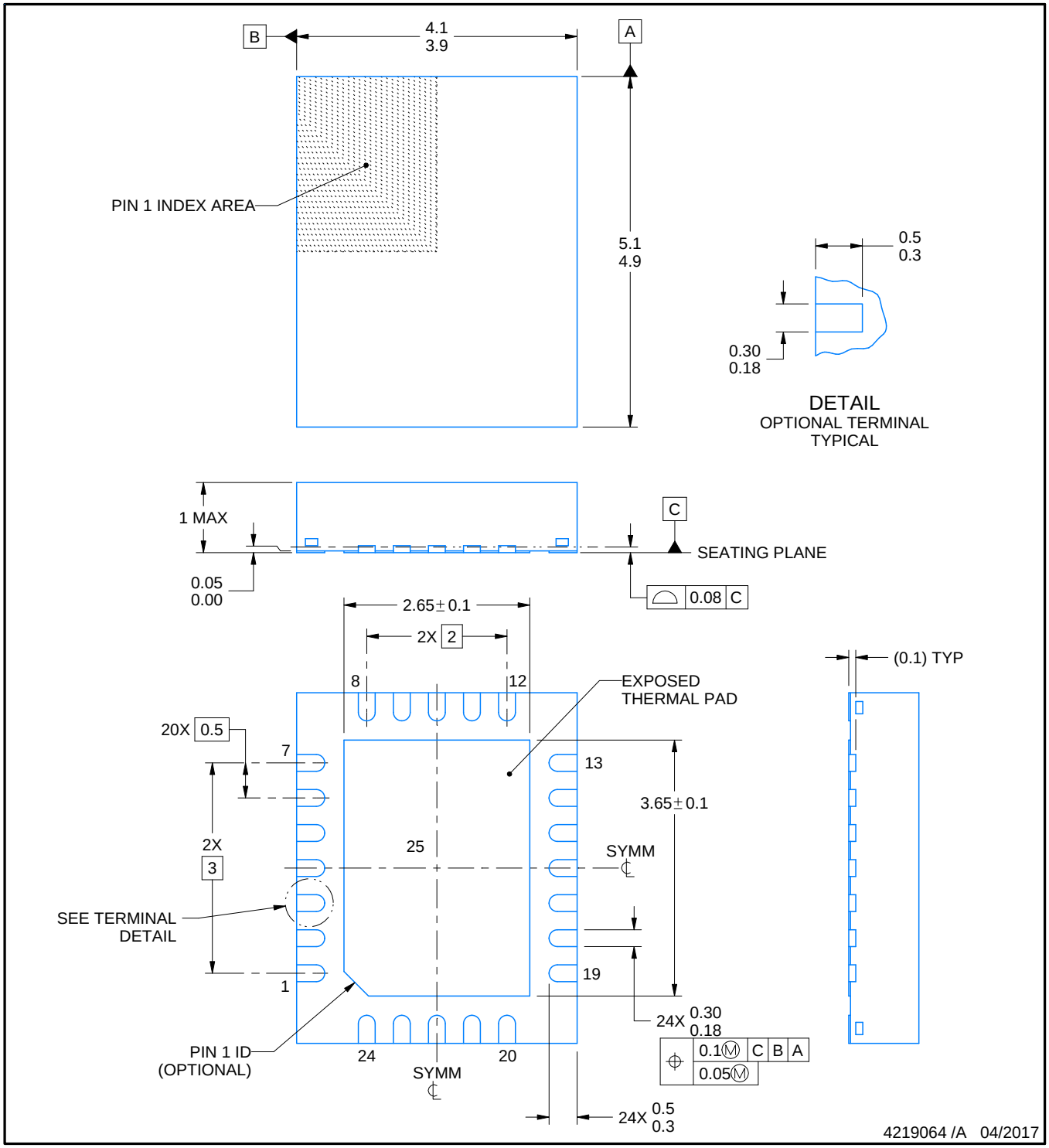
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RHF0024A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

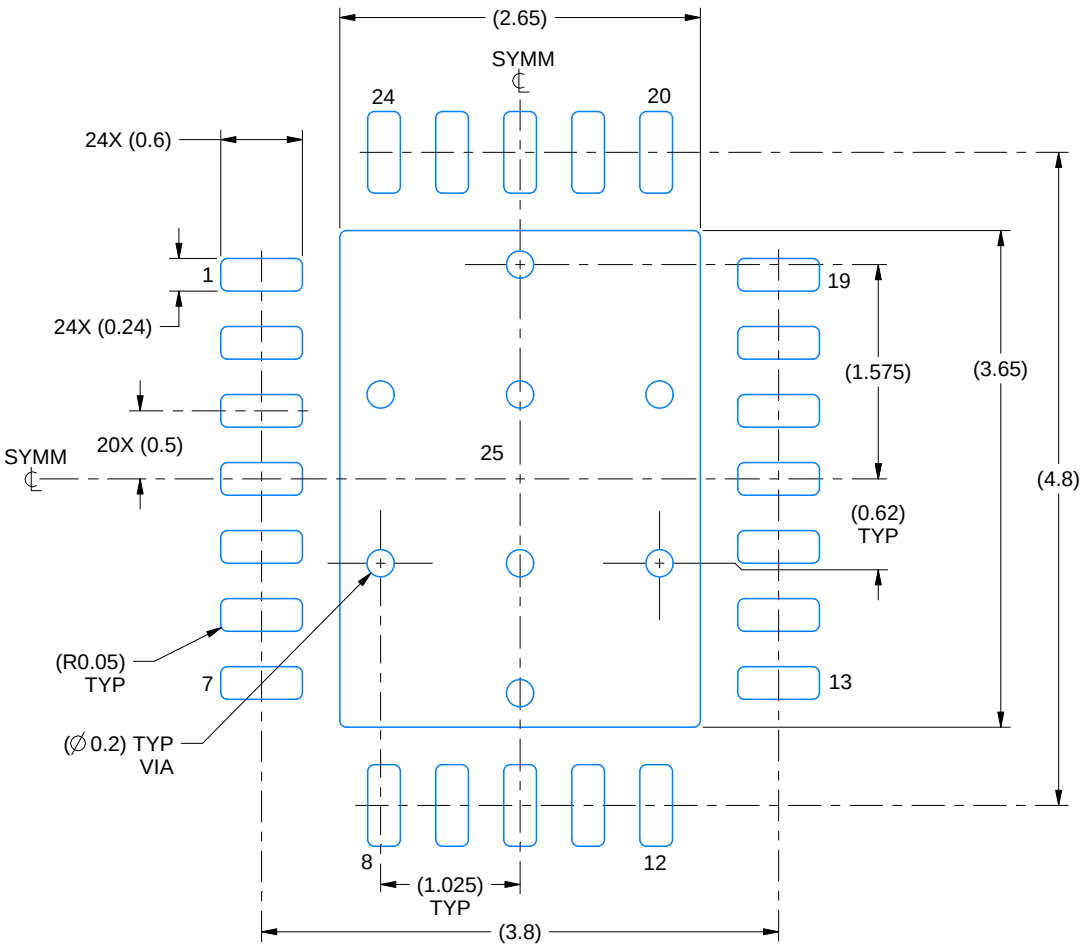
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

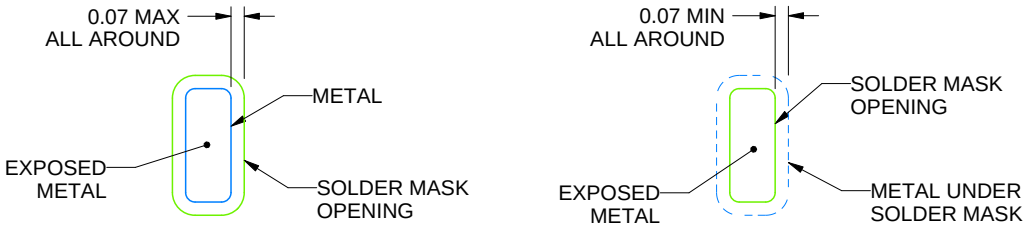
RHF0024A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

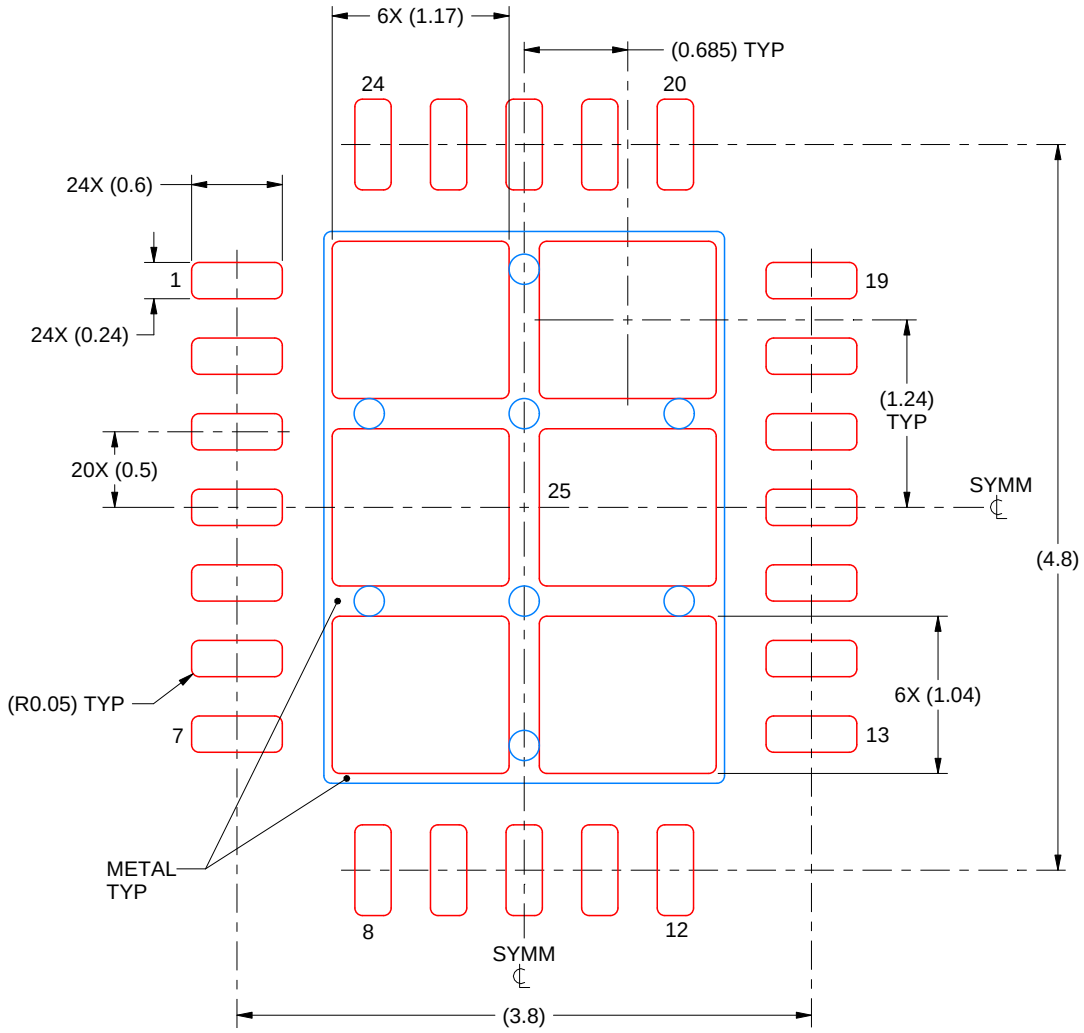


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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