- **Separate Low Noise Preamp and PGA Stages**
- **Shutdown Control**
- **Preamp Features**
  - **Low Voltage Noise . . . 1.7 nV/√Hz**
  - **Accessible Output Pin for External Filtering**
  - **Voltage Feedback, G_{min} = −1, 2**
  - **100 MHz Bandwidth (−3 dB)**
- **PGA Features**
  - **Digitally Programmable Gain**
  - **−22 dB to 20 dB Gain/Attenuation Range**
  - **6 dB Step Resolution**
  - **Output Clamp Protection**
  - **70 MHz Bandwidth (−3 dB)**
  - **175 V/μs Slew Rate**
- **Wide Supply Range ±4.5 V to ±16 V**
- **PowerPAD™ Package for Enhanced Thermal Performance**

description

The THS7001 (single) and THS7002 (dual) are high-speed programmable-gain amplifiers, ideal for applications where load impedance can often vary. Each channel on this device consists of a separate low-noise input preamp and a programmable gain amplifier (PGA). The preamp is a voltage-feedback amplifier offering a low 1.7-nV/√Hz voltage noise with a 100-MHz (−3 dB) bandwidth. The output pin of the preamp is accessible so that filters can be easily added to the amplifier.

The 3-bit digitally-controlled PGA provides a −22-dB to 20-dB attenuation/gain range with a 6-dB step resolution. In addition, the PGA provides both high and low output clamp protection to prevent the output signal from swinging outside the common-mode input range of an analog-to-digital converter. The PGA provides a wide 70-MHz (−3 dB) bandwidth, which remains relatively constant over the entire gain/attenuation range. Independent shutdown control is also provided for power conservation and multiplexing. These devices operate over a wide ±4.5-V to ±16-V supply voltage range.

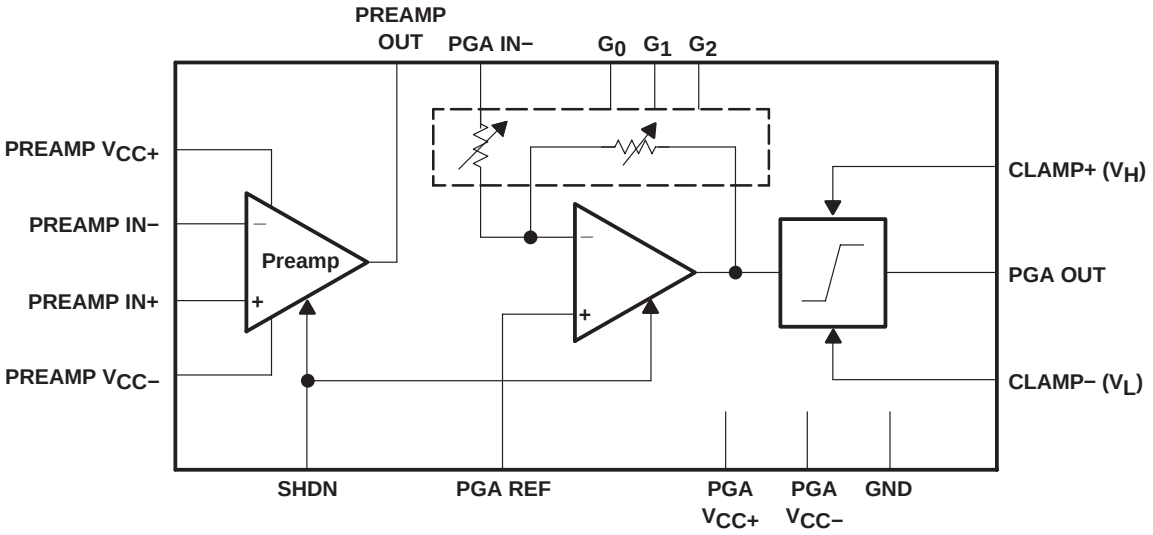

Figure 1. THS7001 Block Diagram

CAUTION: The THS7001 and THS7002 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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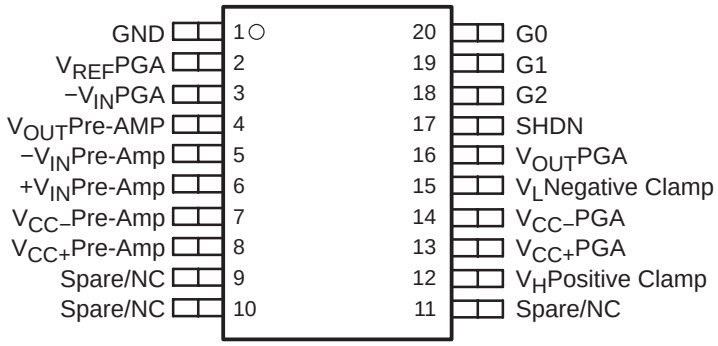
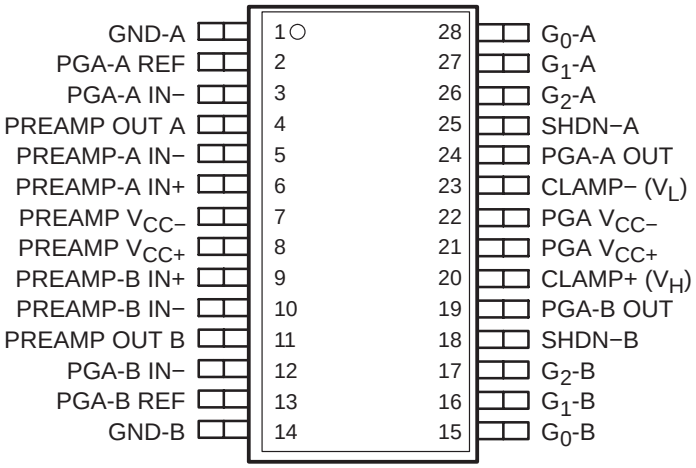
THS7001
PWP PACKAGE
(TOP VIEW)



THS7002
PWP PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES	EVALUATION MODULE
		PowerPAD PLASTIC TSSOP (PWP)	
0°C to 70°C	1	THS7001CPWP	THS7001EVM
	2	THS7002CPWP	THS7002EVM
−40°C to 85°C	1	THS7001IPWP	—
	2	THS7002IPWP	—

block diagram

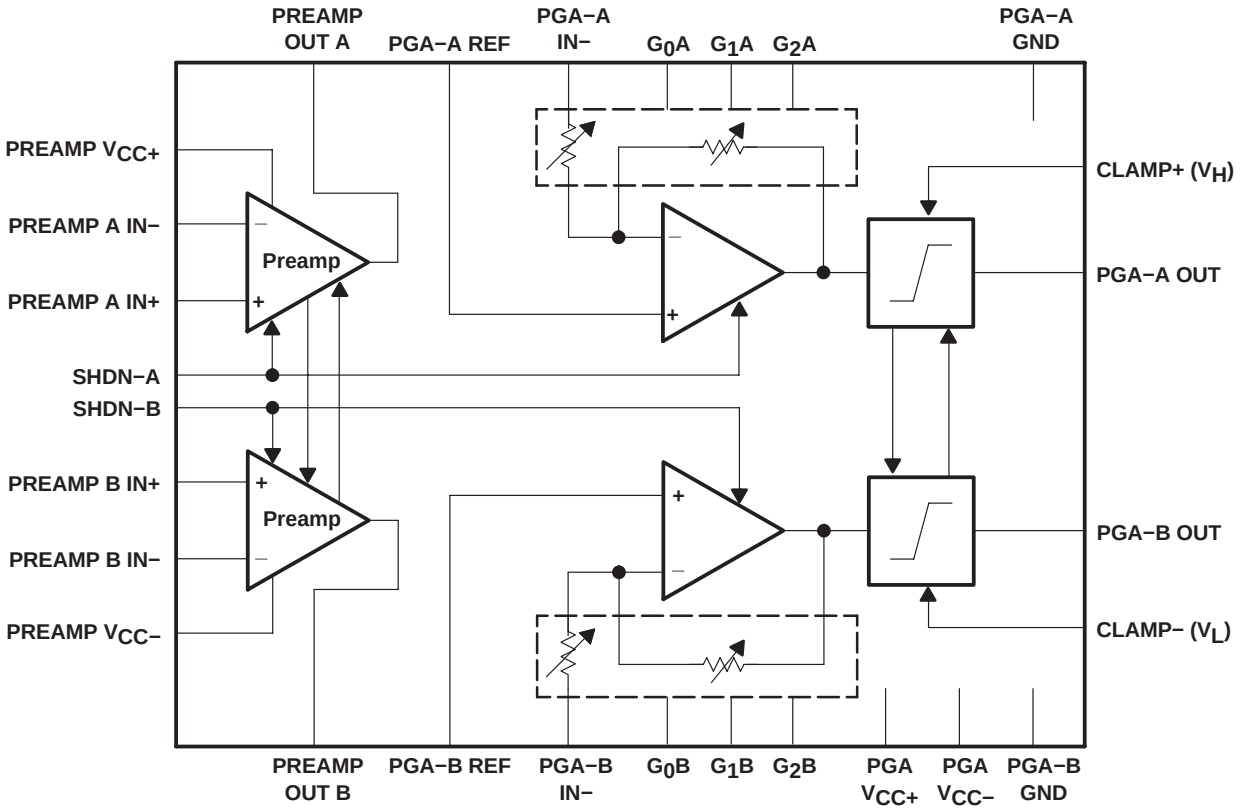


Figure 2. THS7002 Dual Channel PGA

input preamp

To achieve the minimum input equivalent noise required for very small input signals, the input preamp is configured as a classic voltage feedback amplifier with a minimum gain of 2 or −1. The output of the preamp is accessible, allowing for adjustment of gain using external resistors and for external filtering between the preamp and the PGA.

programmable gain amplifier (PGA)

The PGA is an inverting, programmable gain amplifier. The gain is digitally programmable using three control bits (TTL-compatible terminals) that are encoded to provide eight distinct levels of gain/attenuation. Nominal gain/attenuation is shown in Table 1.

Table 1. Nominal Gain/Attenuation

G_2	G_1	G_0	PGA GAIN (dB)	PGA GAIN (V/V)
0	0	0	−22	0.08
0	0	1	−16	0.16
0	1	0	−10	0.32
0	1	1	−4	0.63
1	0	0	2	1.26
1	0	1	8	2.52
1	1	0	14	5.01
1	1	1	20	10.0

output clamping

Output clamping for both upper (V_H) and lower (V_L) levels for the PGAs is provided. There is only one terminal for the positive output clamp and one for the negative output clamp for both channels.

shutdown control

The SHDN terminals allow for powering down the internal circuitry for power conservation or for multiplexing. Separate shutdown controls are available for each channel. The control levels are TTL compatible.

absolute maximum ratings over operating free-air temperature (see Notes 1 and 2)†

Supply voltage, V_{CC} . . . . . ±16.5 V
Input voltage, V_I . . . . . $\pm V_{CC}$
Output current, I_O (preamp) (see Note 1) . . . . . 150 mA
I_O (PGA) (see Note 1) . . . . . 85 mA
Differential input voltage, V_{ID} . . . . . ±4 V
Total continuous power dissipation at (or below) T_A = 25°C (see Note 2): THS7001 . . . . . 3.83 W
THS7002 . . . . . 4.48 W
Maximum junction temperature, T_J . . . . . 150°C
Operating free-air temperature, T_A: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . −40°C to 85°C
Storage temperature, T_{stg} . . . . . −65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The THS7001 and THS7002 incorporates a PowerPAD on the underside of the chip. The PowerPAD acts as a heatsink and must be connected to a thermal dissipation plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which could permanently damage the device. See the *Thermal Information* section of this document for more information about PowerPAD technology.
2. For operation above T_A = 25°C, derate the THS7001 linearly to 2 W at the rate of 30.6 mW/°C and derate the THS7002 linearly to 2.33 W at the rate of 35.9 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Preamp supply voltage, V_{CC+} and V_{CC-}	Split supply	±4.5		±16	V
PGA supply voltage, V_{CC+} and V_{CC-}	Split supply	±4.5‡		±16	V
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	−40		85	°C

‡ PGA minimum supply voltage **must be** less than or equal to preamp supply voltage.

preamp electrical characteristics, G = 2, T_A = 25°C, R_L = 150 Ω, (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Split supply		±4.5		±16.5	V
V_{OM}	Maximum output voltage swing	R_L = 1 kΩ	V_{CC} = ±5 V	±3.6	±3.8		V
			V_{CC} = ±15 V	±13	±13.6		
		R_L = 150 Ω	V_{CC} = ±5 V	±3.5	±3.7		
		R_L = 250 Ω	V_{CC} = ±15 V	±11	±12.6		
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	5	mV
			T_A = full range			7	
	Input offset voltage drift				10		µV/°C
V_{ICR}	Common-mode input voltage range	V_{CC} = ±5 V		±3.8	±4.2		V
		V_{CC} = ±15 V		±13.8	±14		
I_O	Output current (see Note 3)	R_L = 20 Ω	V_{CC} = ±5 V	40	70		mA
			V_{CC} = ±15 V	60	95		
I_{OC}	Short-circuit output current (see Note 3)	V_{CC} = ±15 V			120		mA
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2.5	6	µA
			T_A = full range			8	
I_{IO}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		30	175	nA
			T_A = full range			400	
	Input offset current drift				0.3		nA/°C
CMRR	Common-mode rejection ratio	V_{CC} = ±5 V, V_{IC} = ±2.5 V	T_A = 25°C	80	89		dB
			T_A = full range	78			
		V_{CC} = ±15 V, V_{IC} = ±12 V	T_A = 25°C	80	88		
			T_A = full range	78			
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	85	100		dB
			T_A = full range	80			
R_I	Input resistance				1		MΩ
C_I	Input capacitance				1.5		pF
R_O	Output resistance	Open loop			13		Ω
I_{CC}	Quiescent current (per channel)	V_{CC} = ±5 V	T_A = 25°C		5.5	7	mA
			T_A = full range			8	
		V_{CC} = ±15 V	T_A = 25°C		7	8	
			T_A = full range			9	

† Full range for the THS7001/02C is 0°C to 70°C. Full range for the THS7001/022I is −40°C to 85°C.

NOTE 3: A heatsink may be required to keep the junction temperature below absolute maximum when an output is heavily loaded or shorted. (See absolute maximum ratings and thermal information section.)

preamp operating characteristics, G = 2, T_A = 25°C, R_L = 150 Ω, (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
SR	Slew rate (see Note 4)	G = −1	V_O = ±2 V, V_{CC} = ±5 V		65		V/µs
			V_O = ±10 V, V_{CC} = ±15 V		85		
t_s	Settling time to 0.1%	G = −1, 5 V Step	V_{CC} = ±5 V		85		ns
			V_{CC} = ±15 V		70		
	Settling time to 0.01%		V_{CC} = ±5 V		95		
			V_{CC} = ±15 V		90		
THD	Total harmonic distortion	V_{CC} = ±15 V, $V_{O(PP)}$ = 2V	f_c = 1 MHz, R_L = 250 Ω		−88		dBc
V_n	Input noise voltage	V_{CC} = ±5 V or ±15 V,	f = 10 kHz		1.7		nV/√Hz
I_n	Input noise current	V_{CC} = ±5 V or ±15 V,	f = 10 kHz		0.9		pA/√Hz
BW	Small-signal bandwidth (−3 dB)	$V_{O(PP)}$ = 0.4V, G = 2	V_{CC} = ±5 V		85		MHz
			V_{CC} = ±15 V		100		
	Bandwidth for 0.1 dB flatness	$V_{O(PP)}$ = 0.4V, G = 2	V_{CC} = ±5 V		35		MHz
			V_{CC} = ±15 V		45		
	Full power bandwidth (see Note 5)	V_{CC} = ±5 V,	V_O = 5 $V_{O(PP)}$		4.1		MHz
		V_{CC} = ±15 V,	V_O = 20 $V_{O(PP)}$		1.4		
A_D	Differential gain error	G = 2, 100 IRE, NTSC	V_{CC} = ±5 V		0.02%		
			V_{CC} = ±15 V		0.02%		
ϕ_D	Differential phase error	G = 2, 100 IRE, NTSC	V_{CC} = ±5 V		0.01°		
			V_{CC} = ±15 V		0.01°		
	Open loop gain	V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 1 kΩ	T_A = 25°C	85	89		dB
			T_A = full range	83			
		V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	86	91		
			T_A = full range	84			
	Channel-to-channel crosstalk (THS7002)	V_{CC} = ±5 V or ±15 V,	f = 1 MHz		−85		dB

† Full range for the THS7001/02C is 0°C to 70°C. Full range for the THS7001/02I is −40°C to 85°C.

NOTES: 4. Slew rate is measured from an output level range of 25% to 75%.
5. Full power bandwidth = slew rate/2π $V_{(PP)}$.

shutdown electrical characteristics

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{CC(standby)}$	Standby current, disabled (per channel)	Preamp	$V_{I(SHDN)}$ = 2.5 V	V_{CC} = ±5 V		0.2	0.3	mA
				V_{CC} = ±15 V		0.65	0.8	
		PGA		V_{CC} = ±5 V or ±15 V		0.8	1.2	
$V_{IH(SHDN)}$	Shutdown voltage for power up		V_{CC} = ±5 V or ±15 V,	Relative to GND			0.8	V
$V_{IL(SHDN)}$	Shutdown voltage for power down				2			V
$I_{IH(SHDN)}$	Shutdown input current high		V_{CC} = ±5 V or ±15 V,	$V_{I(SHDN)}$ = 5 V		300	400	µA
$I_{IL(SHDN)}$	Shutdown input current low			$V_{I(SHDN)}$ = 0.5 V		25	50	µA
t_{dis}	Disable time†		V_{CC} = ±5 V or ±15 V,	Preamp and PGA		100		ns
t_{en}	Enable time†		V_{CC} = ±5 V or ±15 V,	Preamp and PGA		1.5		µs

† Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.

PGA electrical characteristics, T_A = 25°C, Gain = 2 dB, R_L = 1 kΩ, (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	Split supply		±4.5‡		±16.5	V
V_{OM}	Maximum output voltage swing	R_L = 1 kΩ	V_{CC} = ±5 V	±3.6	±4.1		V
			V_{CC} = ±15 V	±13.2	±13.8		
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	9	mV
			T_A = full range			11	
	Input offset voltage drift				10		µV/°C
	Reference input voltage range	V_{CC} = ±5 V		±3.8	±4.0		V
		V_{CC} = ±15 V		±13.5	±13.8		
I_{IB}	Input bias current (reference terminal)	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	2	µA
			T_A = full range			3	
I_O	Output current	R_L = 20 Ω	V_{CC} = ±5 V	30	50		mA
I_{OS}	Short-circuit output current				80		mA
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	75	82		dB
			T_A = full range	72			
R_I	Input resistance	Gain = 20 dB			0.27		kΩ
		Gain = −22 dB			3		
R_O	Output resistance	Open loop			20		Ω
I_{CC}	Quiescent supply current (per channel)	V_{CC} = ±5 V	T_A = 25°C		4.8	6	mA
			T_A = full range			7	
		V_{CC} = ±15 V	T_A = 25°C		5	7	
			T_A = full range			8	

† Full range for the THS7001/02C is 0°C to 70°C. Full range for the THS7001/02I is −40°C to 85°C.
‡ PGA minimum supply voltage **must be** less than or equal to preamp supply voltage.

output limiting characteristics

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Clamp accuracy	V_{CC} = ±15 V, V_I = ±10 V, Gain = 2 dB	V_H = 10 V, V_L = −10 V,	T_A = 25°C		±250	±300	mV
			T_A = full range			±350	
	V_{CC} = ±5 V, V_I = ±2.5 V, Gain = 2 dB	V_H = 2 V, V_L = −2 V,	T_A = 25°C		±50	±80	
			T_A = full range			±100	
Clamp overshoot	V_{CC} = ±15 V, V_I = ±10 V,	V_H = 10 V, t_r and t_f = 1 ns	V_L = −10 V,		0.5%		
	V_{CC} = ±5 V, V_I = ±2.5 V,	V_H = 2 V, t_r and t_f = 1 ns	V_L = −2 V,		0.3%		
Overdrive recovery time	V_{CC} = ±15 V, V_I = ±10 V	V_H = 10 V,	V_L = −10 V,		7		ns
	V_{CC} = ±5 V, V_I = ±2.5 V	V_H = 2 V,	V_L = 2 V,		6		
Clamp input bias current	V_O = 3.3 V, V_H = 3.3 V	V_L = 3.3 V,	T_A = 25°C		1	5	µA
			T_A = full range			8	

† Full range for the THS7002C is 0°C to 70°C. Full range for the THS7002I is −40°C to 85°C.

PGA electrical characteristics, T_A = 25°C, Gain = 2 dB, R_L = 1 kΩ, (unless otherwise noted) (continued)

digital gain characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	Relative to GND	2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input current	V_{IH} = 5 V		20	100	nA
I_{IL}	Low-level input current (sink current)	V_{IL} = 0.5 V		0.9	2	µA
t_d	Gain-change delay time†	V_{CC} = ±5 V or ±15 V		2		µs

† Gain-change delay time is the time needed to reach 90% of its final gain value.

PGA operating characteristics, T_A = 25°C, Gain = 2 dB, R_L = 1 kΩ, (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
SR	Slew rate (see Note 4)	V_{CC} = ±5 V,	V_O = ±2.5 V		160		V/µs
		V_{CC} = ±15 V,	V_O = ±10 V		175		
t_s	Settling time to 0.1%	5 V Step	V_{CC} = ±15 V		125		ns
			V_{CC} = ±5 V		120		
THD	Total harmonic distortion	V_{CC} = ±15 V, f_c = 1 MHz,	$V_{O(PP)}$= 2 V, Gain = 8 dB		−69		dBc
BW	Small-signal bandwidth (−3 dB)	Gain = 20 dB, $V_{O(PP)}$ = 0.4 V	V_{CC} = ±15 V		65		MHz
			V_{CC} = ±5 V		60		
		Gain = 2 dB, $V_{O(PP)}$ = 0.4 V	V_{CC} = ±15 V		75		
			V_{CC} = ±5 V		70		
		Gain = −22 dB, $V_{O(PP)}$ = 0.4 V	V_{CC} = ±15 V		80		
			V_{CC} = ±5 V		70		
	Bandwidth for 0.1 dB flatness	Gain = 2 dB, $V_{O(PP)}$ = 0.4 V	V_{CC} = ±15 V		20		MHz
			V_{CC} = ±5 V		18		
	Full power bandwidth (see Note 5)	$V_{O(PP)}$ = 5 V,	V_{CC} = ±5 V		10		MHz
		$V_{O(PP)}$ = 20 V,	V_{CC} = ±15 V		2.8		
A_D	Differential gain error	G = 8 dB, 100 IRE, NTSC, R_L = 150 Ω	V_{CC} = ±5 V		0.04%		
			V_{CC} = ±15 V		0.04%		
ϕ_D	Differential phase error	G = 8 dB, ±100 IRE, NTSC, R_L = 150 Ω	V_{CC} = ±15 V		0.07		°
			V_{CC} = ±5 V		0.09		
	Gain accuracy (see Note 6)	Gain = −22 dB to 20 dB, All 8 steps, V_{CC} = ±5 V or ±15 V	T_A = 25°C	−7.5%	0%	7.5%	
			T_A = full range	−8.5%		8.5%	
	Channel-to-channel gain accuracy (THS7002 only) (see Note 7)	Gain = −22 dB to 20 dB, All 8 steps, V_{CC} = ±5 V or ±15 V	T_A = 25°C	−5.5%	0%	5.5%	
			T_A = full range	−6.5%		6.5%	
V_n	Input referred noise voltage	V_{CC} = ±5 V or ±15 V, f = 10 kHz	Gain = 20 dB		10		nV/√Hz
			Gain = −22 dB		500		
	PGA channel-to-channel crosstalk (THS7002 only)	V_{CC} = ±5 V or ±15 V,	f = 1 MHz		−77		dB

† Full range for the THS7001/02C is 0°C to 70°C. Full range for the THS7001/02I is −40°C to 85°C.

NOTES: 4. Slew rate is measured from an output level range of 25% to 75%.
5. Full power bandwidth = slew rate/2π V_{PEAK}
6. Specified as −100 × (output voltage − (input voltage × gain))/(input voltage × gain)
7. Specified as 100 × (output voltage B− output voltage A)/output voltage A

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

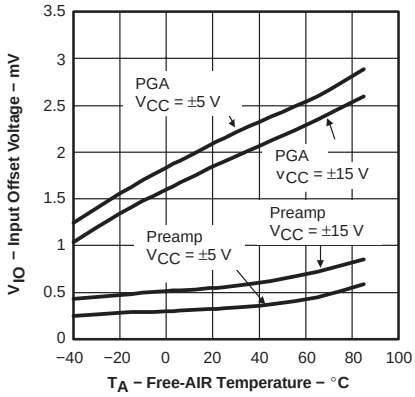


Figure 3

STANDBY SUPPLY CURRENT vs FREE-AIR TEMPERATURE

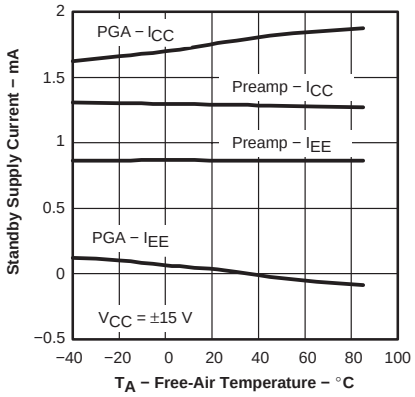


Figure 4

QUIESCENT SUPPLY CURRENT vs FREE-AIR TEMPERATURE

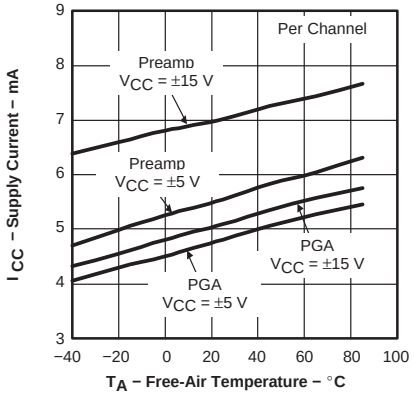


Figure 5

PSRR vs FREQUENCY

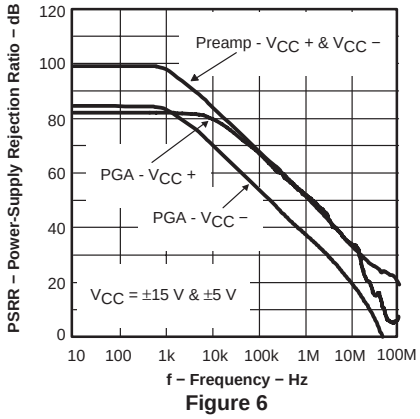


Figure 6

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

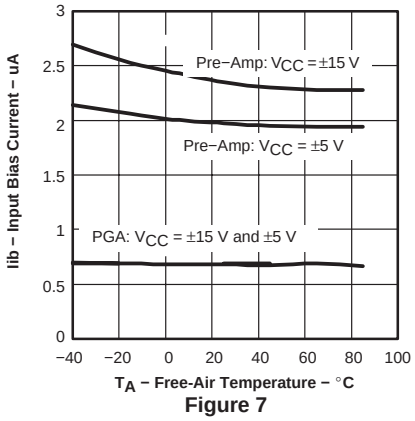


Figure 7

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

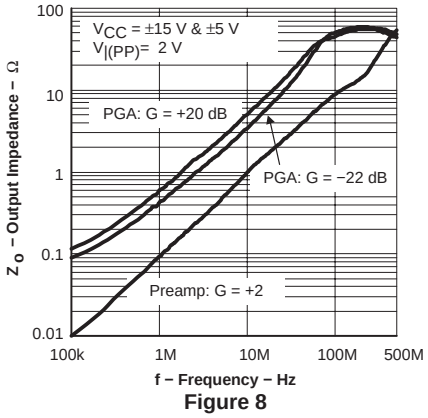


Figure 8

PREAMP INPUT COMMON-MODE VOLTAGE RANGE vs SUPPLY VOLTAGE

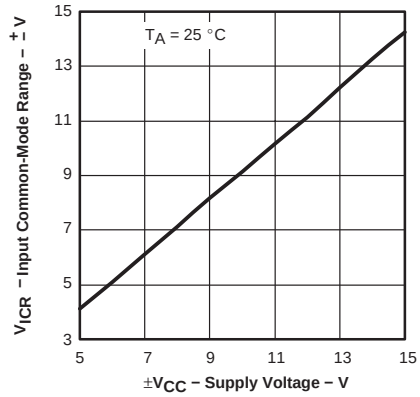


Figure 9

PREAMP OUTPUT VOLTAGE vs SUPPLY VOLTAGE

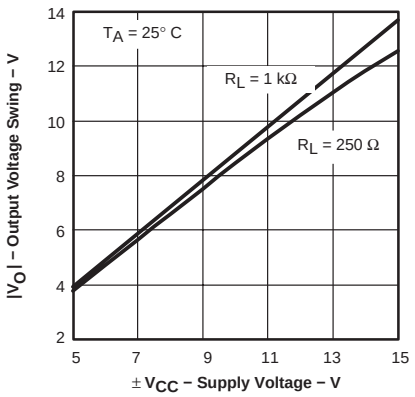


Figure 10

PREAMP CMRR vs FREQUENCY

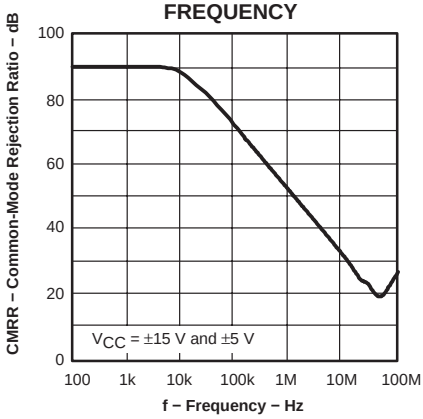


Figure 11

TYPICAL CHARACTERISTICS

PREAMP OPEN LOOP GAIN AND PHASE RESPONSE vs FREQUENCY

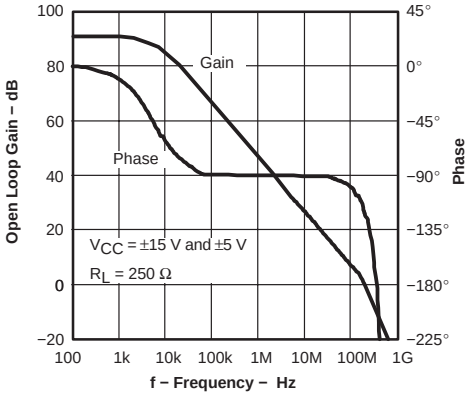


Figure 12

PREAMP INPUT REFERRED VOLTAGE NOISE AND CURRENT NOISE vs FREQUENCY

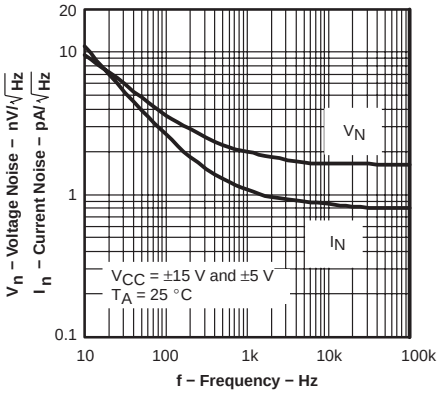


Figure 13

PREAMP OUTPUT AMPLITUDE vs FREQUENCY

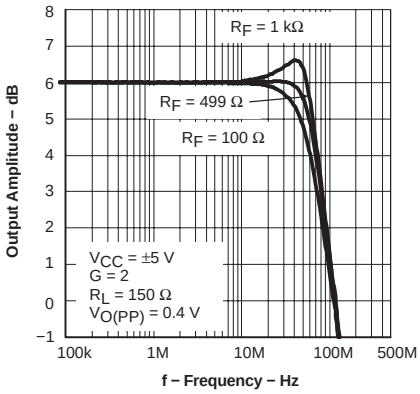


Figure 14

PREAMP OUTPUT AMPLITUDE vs FREQUENCY

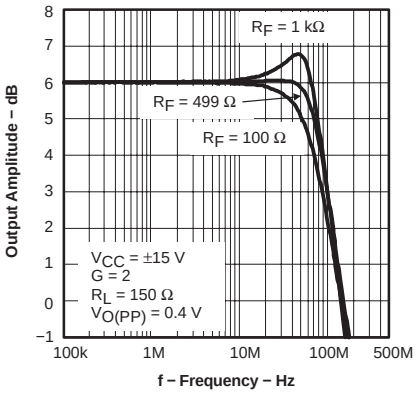


Figure 15

PREAMP OUTPUT AMPLITUDE vs FREQUENCY

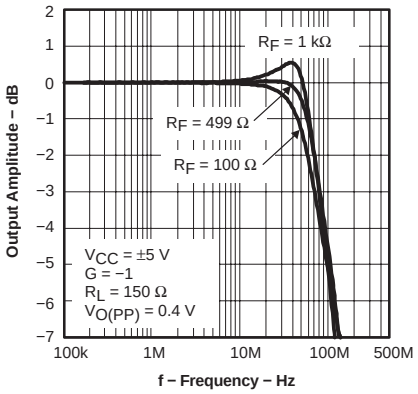


Figure 16

PREAMP OUTPUT AMPLITUDE vs FREQUENCY

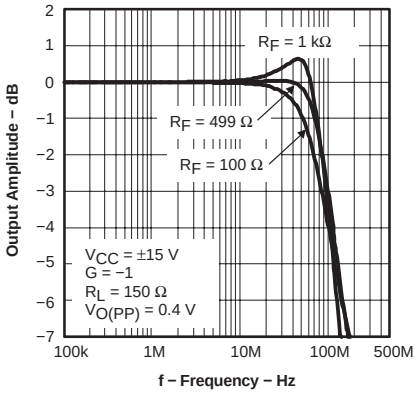


Figure 17

PREAMP OUTPUT AMPLITUDE vs FREQUENCY

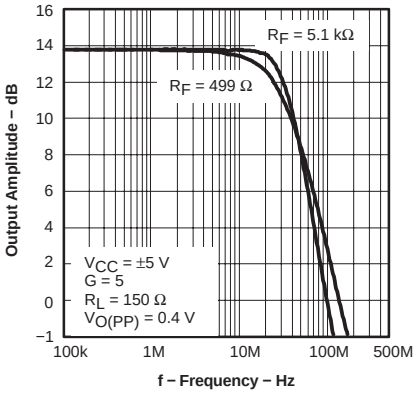


Figure 18

PREAMP OUTPUT AMPLITUDE vs FREQUENCY

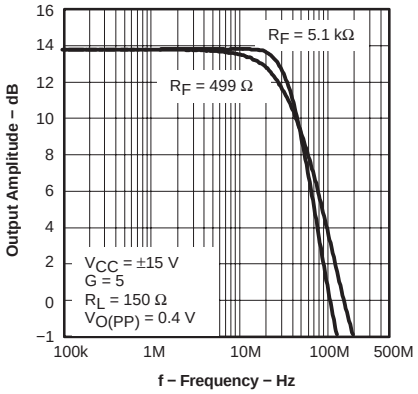


Figure 19

TYPICAL CHARACTERISTICS

PREAMP LARGE AND SMALL SIGNAL FREQUENCY RESPONSE

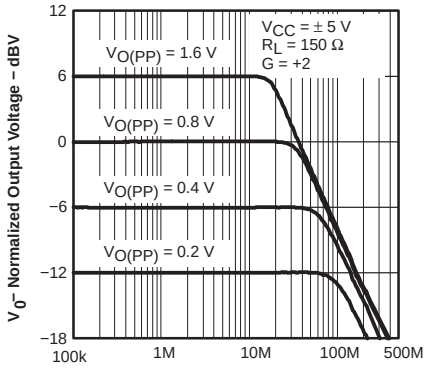


Figure 20

PREAMP LARGE AND SMALL SIGNAL FREQUENCY RESPONSE

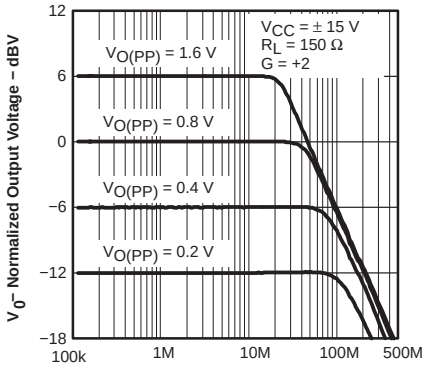


Figure 21

PREAMP HARMONIC DISTORTION vs FREQUENCY

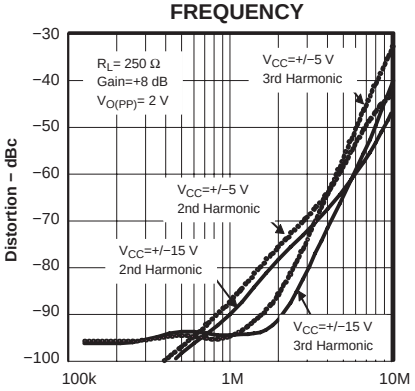


Figure 22

PREAMP HARMONIC DISTORTION vs OUTPUT VOLTAGE

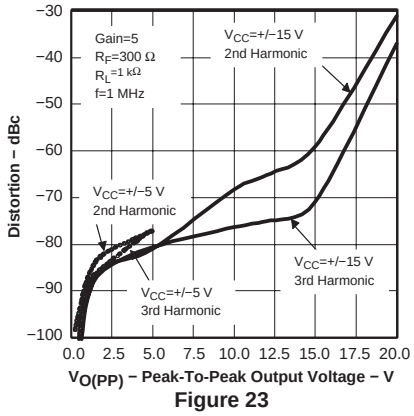


Figure 23

PREAMP SLEW RATE vs FREE-AIR TEMPERATURE

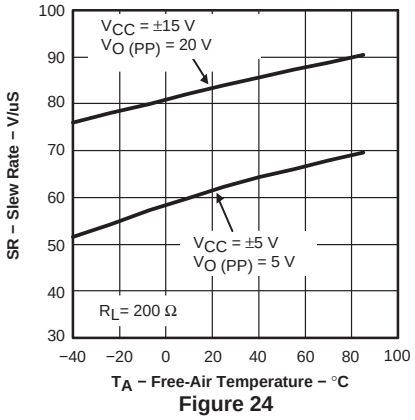


Figure 24

PREAMP 400-mV STEP RESPONSE

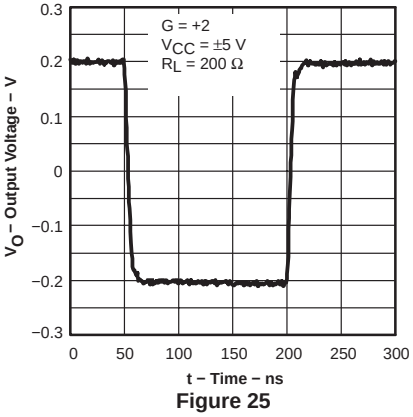


Figure 25

PREAMP 5-V STEP RESPONSE

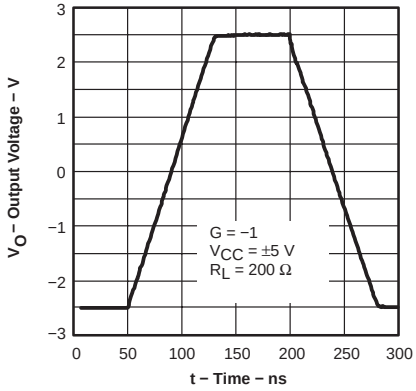


Figure 26

PREAMP 5-V STEP RESPONSE

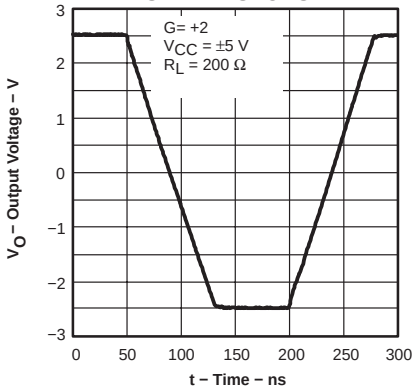


Figure 27

PREAMP 20-V STEP RESPONSE

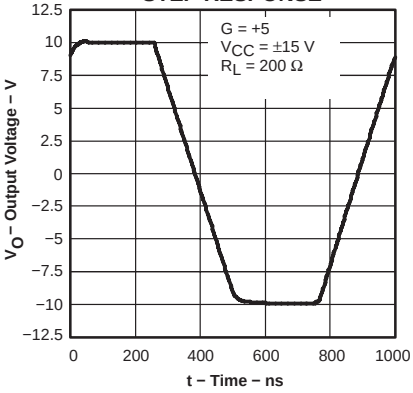


Figure 28

TYPICAL CHARACTERISTICS

THS7002 PREAMP CHANNEL-TO-CHANNEL CROSSTALK

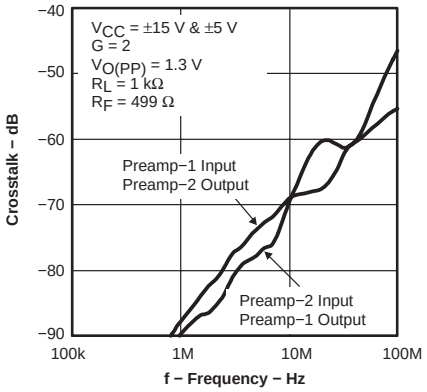


Figure 29

PREAMP-TO-PGA CROSSTALK vs FREQUENCY

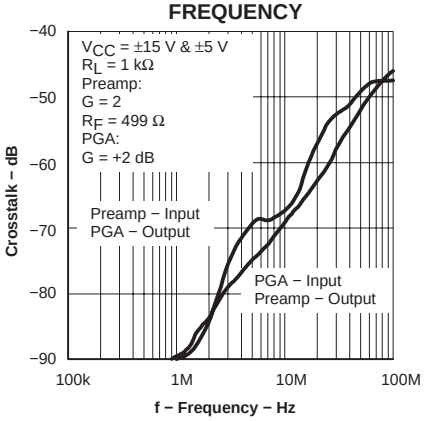


Figure 30

PGA INPUT REFERRED VOLTAGE NOISE vs FREQUENCY

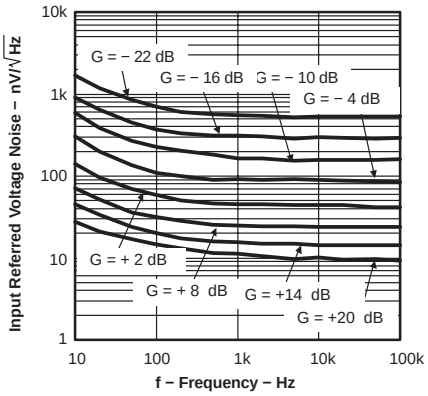


Figure 31

PGA CHANNEL-TO-CHANNEL GAIN ACCURACY vs GAIN SETTING

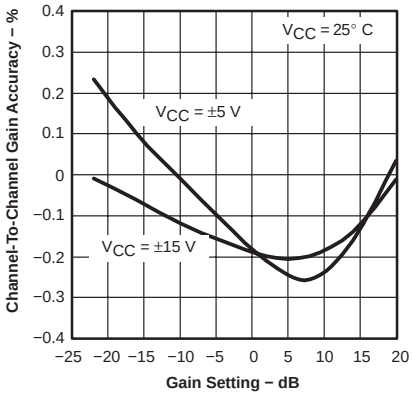


Figure 32

NORMALIZED PGA GAIN ACCURACY vs TEMPERATURE

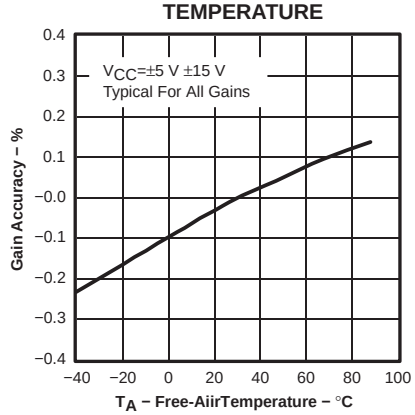


Figure 33

PGA FREQUENCY RESPONSE

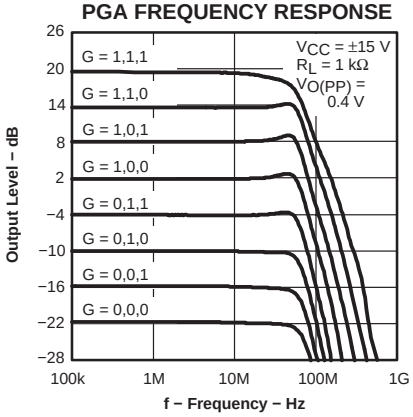


Figure 34

PGA FREQUENCY RESPONSE

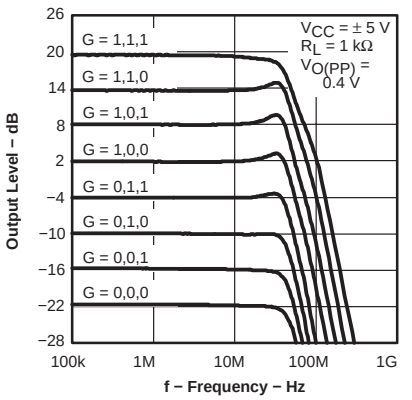


Figure 35

PGA LARGE AND SMALL SIGNAL FREQUENCY RESPONSE

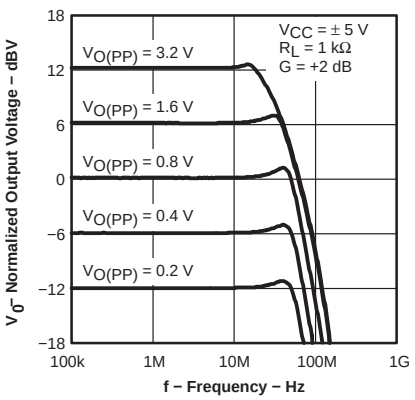


Figure 36

PGA LARGE AND SMALL SIGNAL FREQUENCY RESPONSE

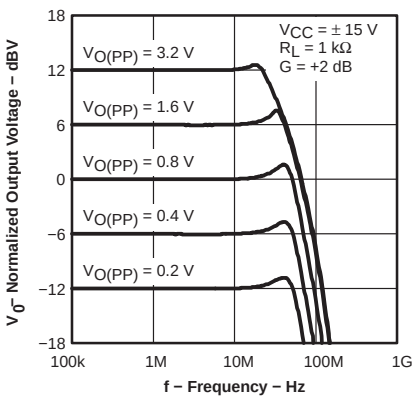


Figure 37

TYPICAL CHARACTERISTICS

PGA HARMONIC DISTORTION vs FREQUENCY

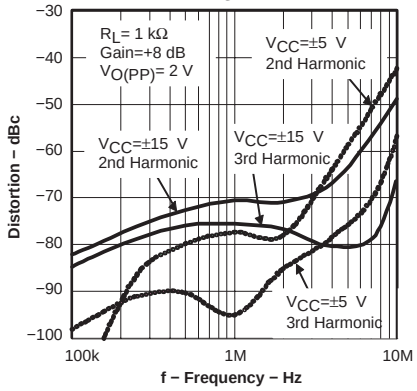


Figure 38

PGA HARMONIC DISTORTION vs OUTPUT VOLTAGE

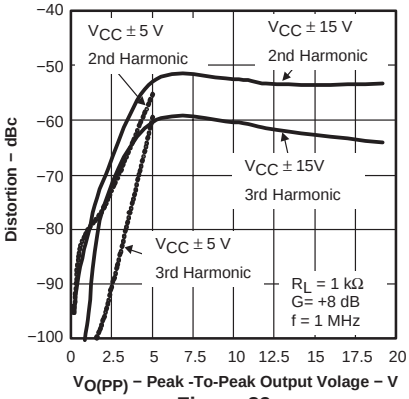


Figure 39

PGA SLEW RATE vs FREE-AIR TEMPERATURE

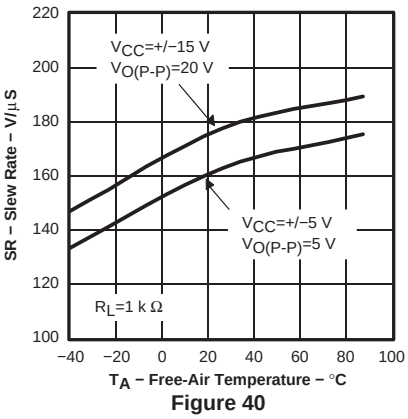


Figure 40

PGA CLAMP ACCURACY vs FREE-AIR TEMPERATURE

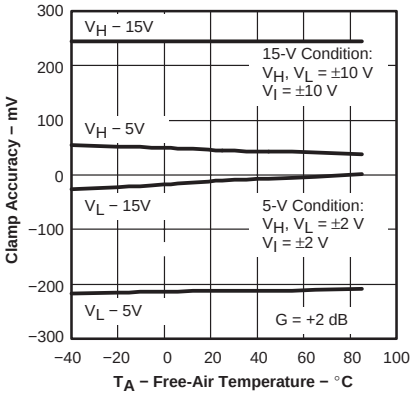


Figure 41

PGA CLAMP RESPONSE

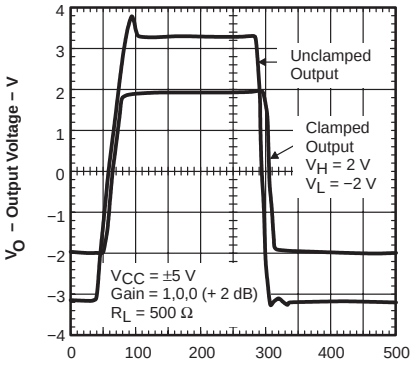


Figure 42

PGA CLAMP RESPONSE

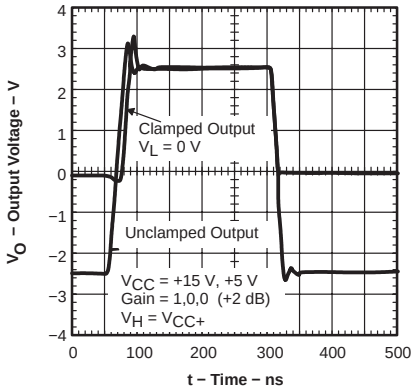


Figure 43

PGA CLAMP RESPONSE

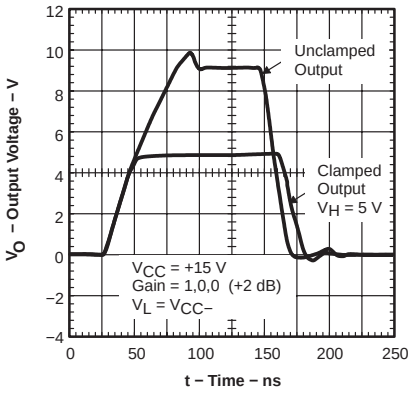


Figure 44

SHUTDOWN ISOLATION vs FREQUENCY

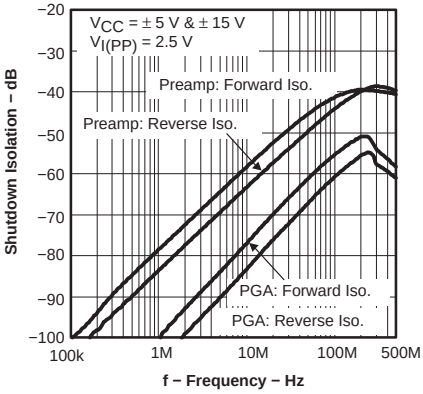


Figure 45

PGA SHUTDOWN RESPONSE

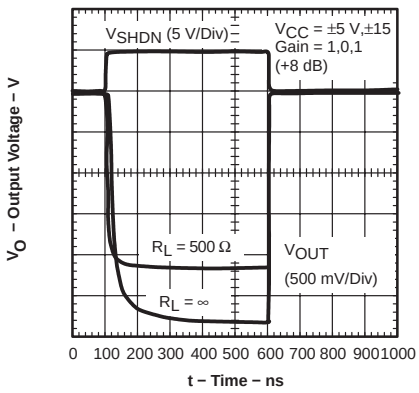


Figure 46

TYPICAL CHARACTERISTICS

PGA SHUTDOWN RESPONSE

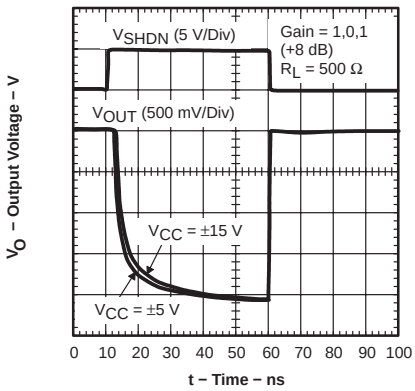


Figure 47

PREAMP SHUTDOWN RESPONSE

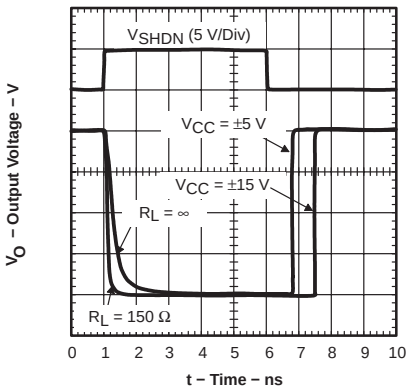


Figure 48

PGA 5-V STEP RESPONSE

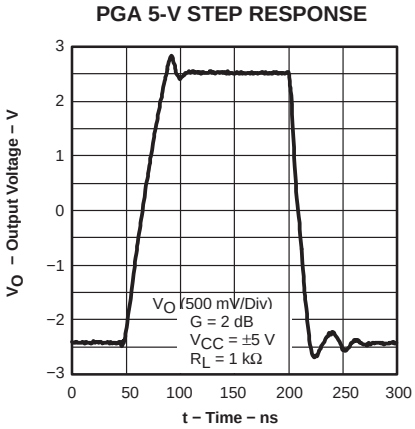


Figure 49

PGA 20-V STEP RESPONSE

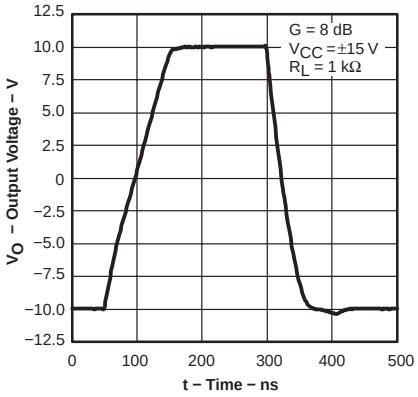


Figure 50

APPLICATION INFORMATION

theory of operation

Each section of the THS7001 and THS7002 consists of a pair of high speed operational amplifiers configured in a voltage feedback architecture. They are built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in exceptionally high performance amplifiers that have a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic of the preamplifiers are shown in Figure 51.

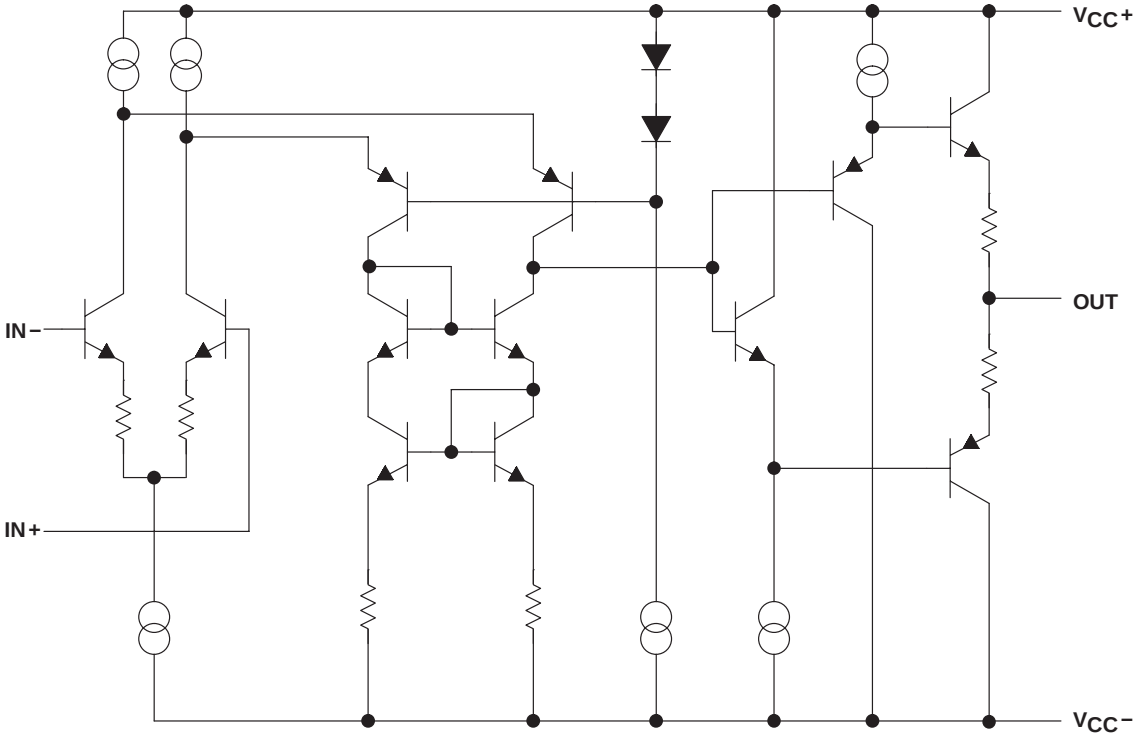


Figure 51. Pre-Amp Simplified Schematic

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true for the preamplifiers, which typically amplify small signals. The noise model is shown in Figure 52. This model includes all of the noise sources as follows:

- e_n = amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = noninverting current noise (pA/$\sqrt{Hz}$)
- IN− = inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

APPLICATION INFORMATION

noise calculations and noise figure (continued)

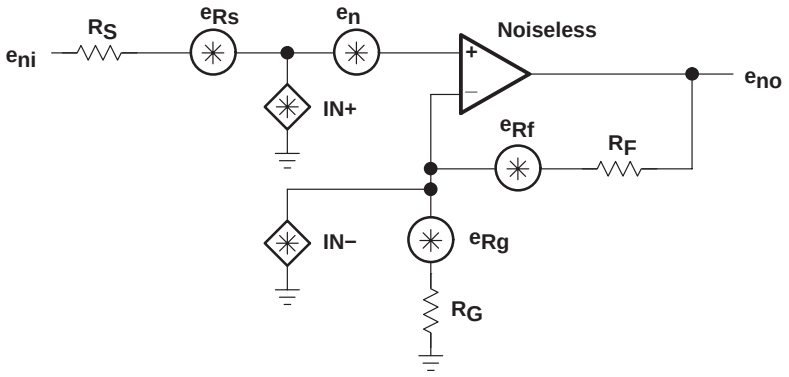


Figure 52. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)} \quad (1)$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)} \quad (2)$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing $R_F + R_G$), the input noise can be reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

By using the low noise preamplifiers as the first element in the signal chain, the input signal's signal-to-noise ratio (SNR) is maintained throughout the entire system. This is because the dominant system noise is due to the first amplifier. This can be seen with the following example:

APPLICATION INFORMATION

noise calculations and noise figure (continued)

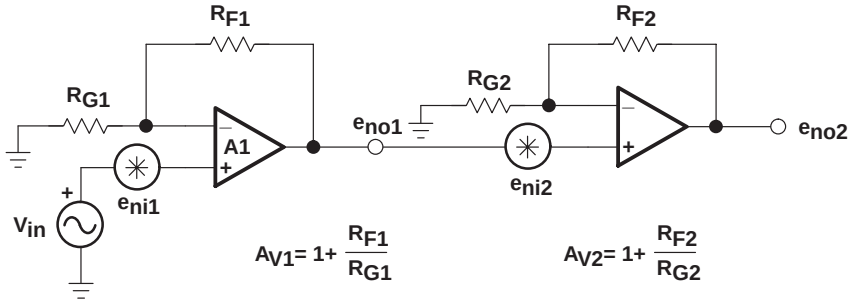


Figure 53. Simplified Composite Amplifier System

The noise due to amplifier 1 (A1) is the same as derived in equations 1 and 2. The composite system noise is calculated as follows:

$$e_{no2} = \sqrt{e_{ni2}^2 + e_{no1}^2} \times A_{V2}$$

$$= \sqrt{e_{ni2}^2 + \left(e_{ni1} A_{V1}\right)^2} \times A_{V2} \quad (3)$$

In a typical system, amplifier 1 (A1) has a large gain (A_{V1}). Because the noise is summed in the RMS method, if the A1 output noise is more than 25% larger than the input noise of amplifier 2, the contribution of amplifier 2's input noise to the composite amplifier output noise can effectively be ignored. This reduces equation 3 down to:

$$e_{no2} \cong e_{ni1} A_{V1} A_{V2} \quad (4)$$

Equation 4 shows that the very first amplifier (the preamplifier) is critical in any low-level signal system. This also shows that practically any noisy amplifier can be used after the preamplifier with minimal SNR degradation.

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{\left(e_{Rs}\right)^2}\right]$$

APPLICATION INFORMATION

noise calculations and noise figure (continued)

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\,kTR_S}\right]$$

Figure 54 shows the noise figure graph for the THS7001 and THS7002.

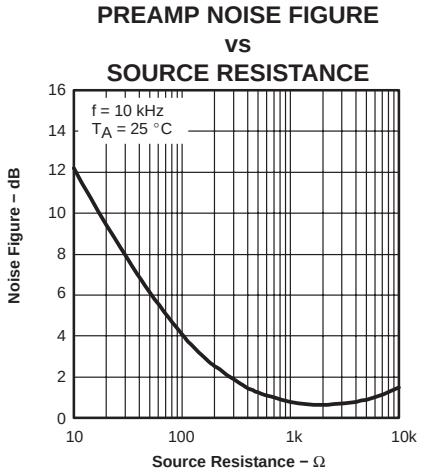


Figure 54. Noise Figure vs Source Resistance

optimizing frequency response for the preamplifiers

Internal frequency compensation of the THS7001 and THS7002 was selected to provide very wide bandwidth performance and still maintain a very low noise floor. In order to meet these performance requirements, the preamplifiers must have a minimum gain of 2 (−1). Because everything is referred to the noninverting terminal of an operational amplifier, the noise gain in a G = −1 configuration is the same as a G = 2 configuration.

One of the keys of maintaining a smooth frequency response, and hence, a stable pulse response, is to pay particular attention to the inverting terminal. Any stray capacitance at this node causes peaking in the frequency response. There are two things that can be done to help minimize this effect. The first is to simply remove any ground planes under the inverting terminal of the amplifier. This also includes the trace that connects to this terminal. Additionally, the length of this trace should be minimized. The capacitance at this node causes a lag in the voltage being fed back due to the charging and discharging of the stray capacitance. If this lag becomes too long, the amplifier will not be able to correctly keep the noninverting terminal voltage at the same potential as the inverting terminal's voltage. Peaking and possibly oscillations can occur if this happens.

APPLICATION INFORMATION

optimizing frequency response for the preamplifiers (continued)

The next thing that helps to maintain a smooth frequency response is to keep the feedback resistor (R_f) and the gain resistor (R_g) values fairly low. These two resistors are effectively in parallel when looking at the ac small-signal response. This is why in a configuration with a gain of 5, a feedback resistor of 5.1 kΩ with a gain resistor of 1.2 kΩ only shows a small peaking in the frequency response. The parallel resistance is less than 1 kΩ. This value, in conjunction with a very small stray capacitance test PCB, forms a zero on the edge of the amplifier's natural frequency response. To eliminate this peaking, all that needs to be done is to reduce the feedback and gain resistances. One other way to compensate for this stray capacitance is to add a small capacitor in parallel with the feedback resistor. This helps to neutralize the effects of the stray capacitance. To keep this zero out of the operating range, the stray capacitance and resistor value's time constant must be kept low. But, as can be seen in Figures 14 − 19, a value too low starts to reduce the bandwidth of the amplifier. Table 1 shows some recommended feedback resistors to be used with the THS7001 and THS7002 preamplifiers.

Table 2. Recommended Feedback Resistors

GAIN	R_f for V_{CC} = ±15 V and ± 5 V
2	499 Ω
−1	499 Ω
5	1 kΩ

PGA gain control

The PGA section of the THS7001 and THS7002 IC allows for digital control of the gain. There are three digital control pins for each side of the PGA (AG0 – AG2, and BG0 – BG2). Standard TTL or CMOS Logic will control these pins without any difficulties. The applied logic levels are referred to the DGND pins of the THS7002. The gain functions are not latched and therefore always rely on the logic at these pins to maintain the correct gain settings. A 3.3 kΩ resistor to ground is usually applied at each input to ensure a fixed logic state. The gain control acts like break-before-make SPDT switches. Because of this action, the PGA will go into an open-loop condition. This may cause the output to behave unpredictably until the switches closes in less than 1.5 μs. Due to the topology of this circuit, the controlling circuitry must be able to sink up to 2 μA of current when 0-V is applied to the gain control pin. A simplified circuit diagram of the gain control circuitry is shown in Figure 55.

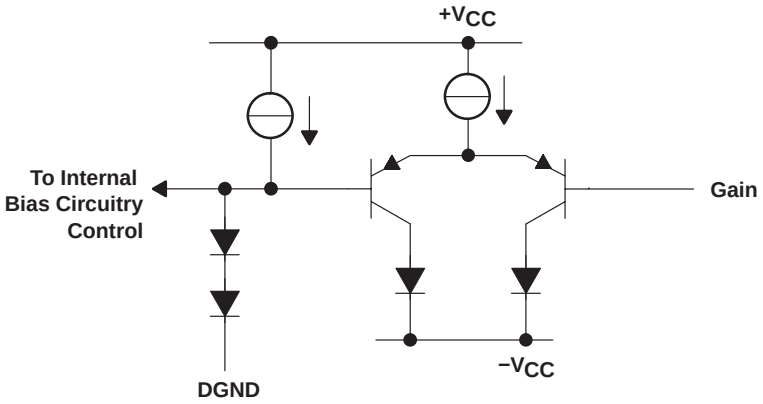


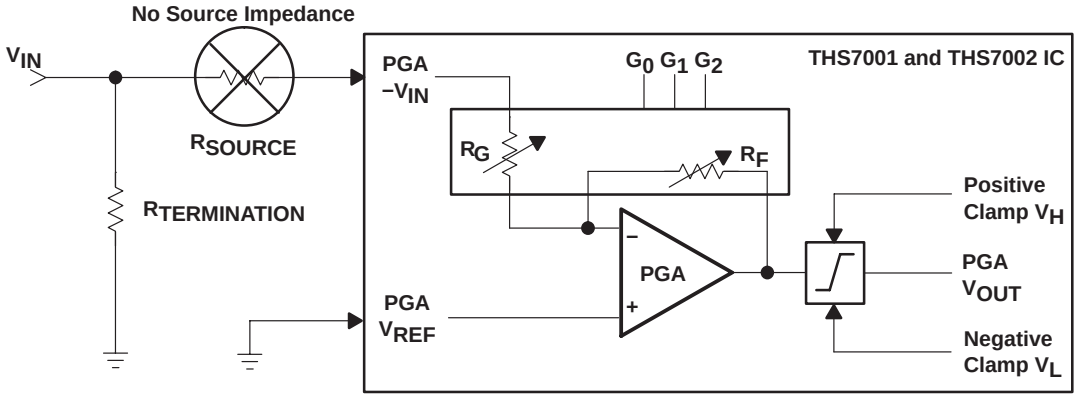
Figure 55. Simplified PGA Gain Control

APPLICATION INFORMATION

PGA gain control (continued)

One aspect of the THS7001 and THS7002 PGA signal inputs is that there are internal variable resistors (R_F and R_G), which set the gain. The resistance of R_G changes from about 270-Ω (Gain = +20 dB) to about 3-kΩ (Gain = −22 dB). Therefore, any source impedance at the input to the PGA amplifiers will cause a gain error to be seen at the output. A buffer/amplifier is highly recommended to directly drive the input of the PGA section to help minimize this effect.

Another thing which should be kept in mind is that when each amplifier's V_{REF} is connected to ground, the internal R_G resistor is connected to a virtual ground. Therefore, if a termination resistor is used on the source side, the total terminating resistance is the parallel combination of the terminating resistance and the internal R_G resistor. This, in conjunction with the series impedance problem mentioned previously, can potentially cause a voltage mismatch between the output of a 50-Ω source and the expected PGA output voltage. These points can be easily seen in the simplified diagram of the THS7001 and THS7002 PGA section (see Figure 56).



$$R_{TOTAL\ TERMINATION} = \frac{R_{TERMINATION} \times \left(R_{SOURCE} + R_G\right)}{R_{TERMINATION} + \left(R_{SOURCE} + R_G\right)}$$

Figure 56. Simplified PGA Section of the THS7001 and THS7002

voltage reference terminal

If a voltage is applied to the PGA's V_{REF} terminal, then the output of the PGA section will amplify the applied reference voltage by one plus the selected gain. Thus, the output gain strictly due to V_{REF} will be from +0.6 dB to +21 dB according to the following formula:

$$\frac{V_{OUT}}{V_{REF}} = 20 \text{ X } \text{Log}_{10}\left[1 + \left(\text{PGA Gain}(V/V)\right)\right]$$

For most configurations, it is recommended that this pin be connected to the signal ground.

APPLICATION INFORMATION

output clamping

Typically, the output of the PGA will directly drive an analog-to-digital converter (ADC). Because of the limited linear input range and saturation characteristics of most ADCs, the PGA's outputs incorporate a voltage clamp. Unlike a lot of clamping amplifiers which clamp only at the input, the THS7001 and THS7002 clamps at the output stage. This insures that the output will always be protected regardless of the Gain setting and the input voltage. The clamps activate almost instantaneously and recover from saturation in less than 7 ns. This can be extremely important when the THS7001 and THS7002 is used to drive some ADCs which have a very long overdrive recovery time. It is also recommended to add a pair of high frequency bypass capacitors to the clamp inputs. These capacitors will help eliminate any ringing which may ocur when a large pulse is applied to the amplifier. This pulse will force the clamp diodes to abruptly turn on, drawing current from the reference voltages. Just like a power supply trace, you must minimize the inductance seen by the clamp pins. The bypass capacitors will supply the sudden current demands when the clamps are suddenly turned on. A simplified clamping circuit diagram is shown in Figure 57.

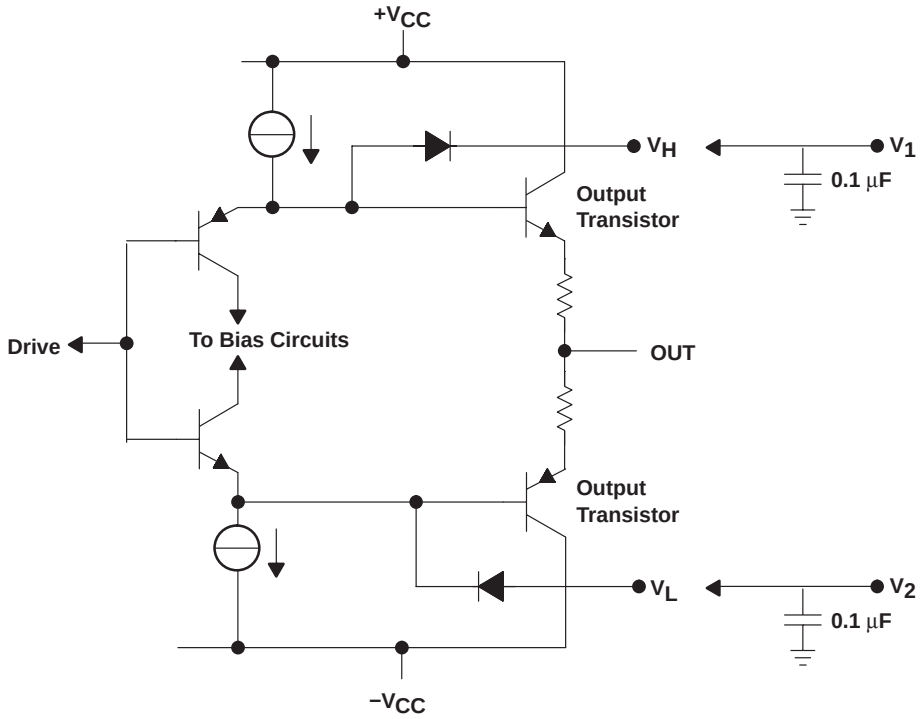


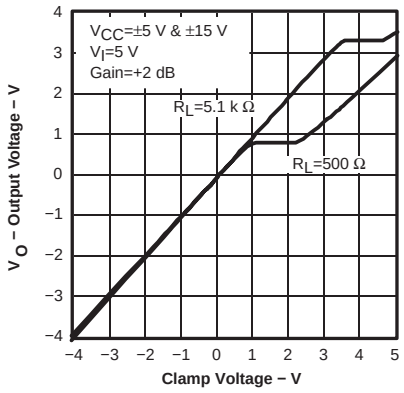
Figure 57. Simplified THS7001 and THS7002 Clamp Circuit

Because the internal clamps utilize the same clamping reference voltages, the outputs of both PGAs on the THS7002 are clamped to the same values. These clamps are typically connected to the power supply pins to allow a full output range. But, they can be connected to any voltage reference desired. The clamping range is limited to $+V_{CC}$ and GND for V_H and $–V_{CC}$ and GND for V_L. It is possible to go beyond GND for each respective clamp, but it is not recommended. This is because this operation relies on the internal bias currents in the Class AB output stage to maintain their linearity. There may also be a chance to reverse bias the PN junctions and possibly cause internal damage to these junctions. But for reference, the graphs in Figure 58 show the output voltage versus the clamping voltage with different loads.

APPLICATION INFORMATION

output clamping (continued)

OUTPUT VOLTAGE vs CLAMP VOLTAGE (V_L)



OUTPUT VOLTAGE vs CLAMP VOLTAGE (V_H)

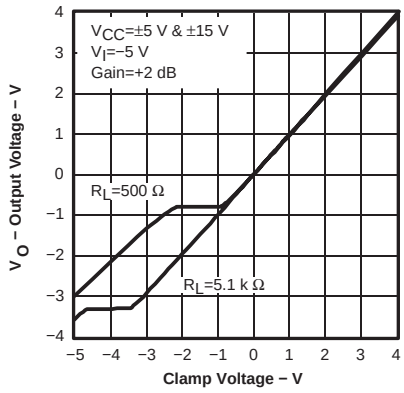
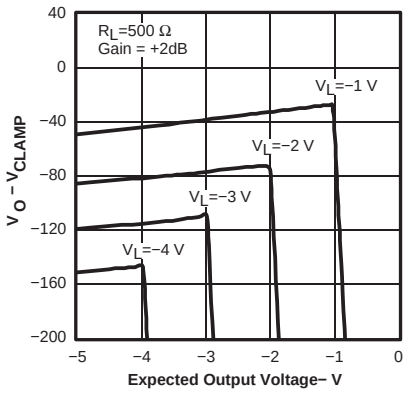


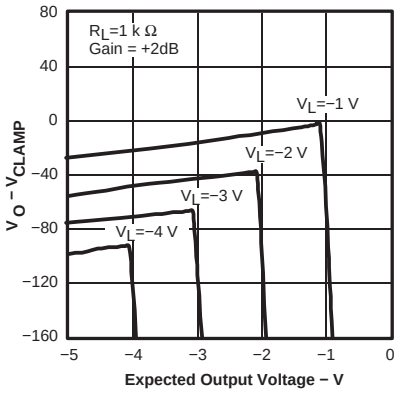
Figure 58. Output Voltage vs Clamp Voltage

The accuracy of this clamp is dependant on the amount of current flowing through the internal clamping diodes. As is typical with all diodes, the voltage drop across this diode increases with current. Therefore, the accuracy of the clamp is highly dependant upon the output voltage, the clamping voltage difference, and the output current. The accuracy of the clamps with different load resistances are shown in Figure 59.

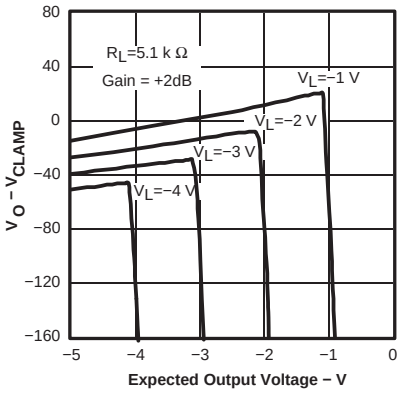
NEGATIVE CLAMP ACCURACY (V_L)



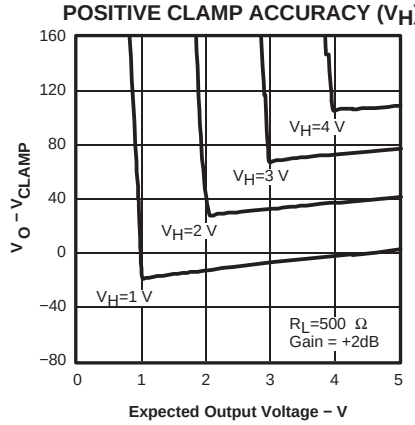
NEGATIVE CLAMP ACCURACY (V_L)



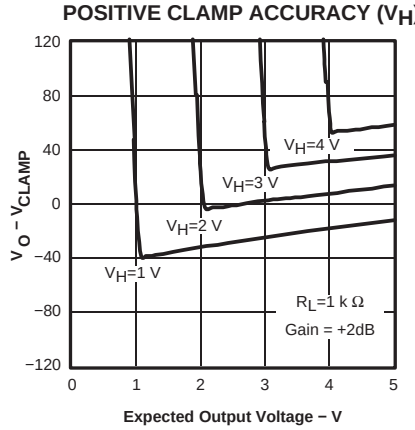
NEGATIVE CLAMP ACCURACY (V_L)



POSITIVE CLAMP ACCURACY (V_H)



POSITIVE CLAMP ACCURACY (V_H)



POSITIVE CLAMP ACCURACY (V_H)

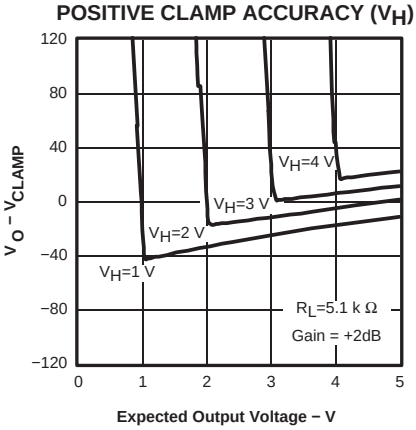


Figure 59. Clamping Accuracy

APPLICATION INFORMATION

shutdown control

There are two shutdown pins which control the shutdown for each half of the THS7002 and one shutdown pin for the THS7001. When the shutdown pins signals are low, the THS7001 and THS7002 is active. But, when a shutdown pin is high (+5 V), a preamplifier and the respective PGA section is turned off. Just like the Gain controls, the shutdown logic is not latched and should always have a signal applied to them. A 3.3-kΩ resistor to ground is usually applied to ensure a fixed logic state. A simplified circuit can be seen in Figure 60.

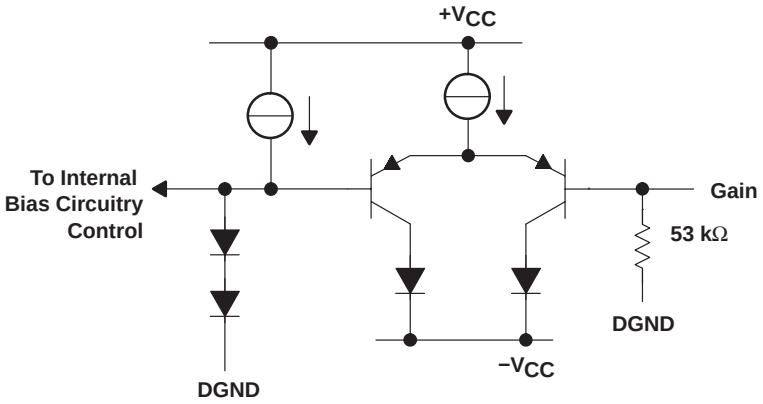


Figure 60. Simplified THS7001 and THS7002 Shutdown Circuit

One aspect of the shutdown feature, which is often over-looked, is that the PGA section will still have an output while in shutdown mode. This is due to the internally fixed R_F and R_G resistors. This effect is true for any amplifier connected as an inverter. The internal circuitry may be powered down and in a high-impedance state, but the resistors are always there. This will then allow the input signal current to flow through these resistors and into the output. The equivalent resistance of R_F and R_G is approximately 3 kΩ. To minimize this effect, a shunt resistor to ground may be utilized, This will act as a classic voltage divider and will reduce the feed-through voltage seen at the PGA output. The drawback to this is the increased load on the PGA while in the active state.

driving a capacitive load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS7001 and THS7002 has been internally compensated to maximize its bandwidth and slew rate performance. When an amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 61. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

APPLICATION INFORMATION

driving a capacitive load (continued)

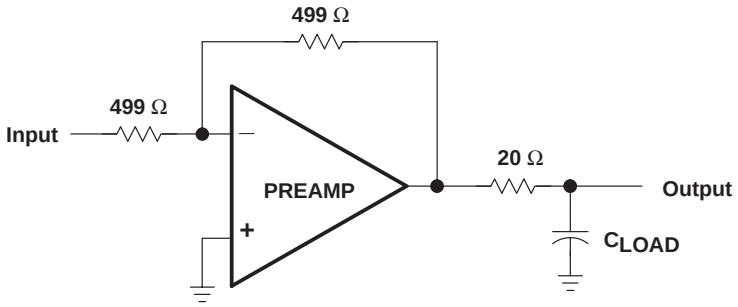
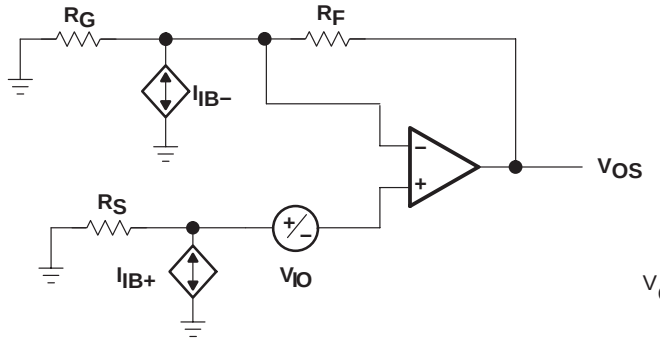


Figure 61. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

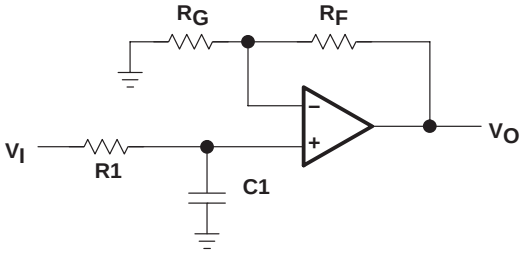


$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_F$$

Figure 62. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the THS7001 and THS7002 preamplifier (see Figure 63).



$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 63. Single-Pole Low-Pass Filter

APPLICATION INFORMATION

general configurations (continued)

If even more attenuation is needed, a multiple-pole filter is required. The Sallen-Key filter can be used for this task. For best results, the THS7001 and THS7002 preamplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

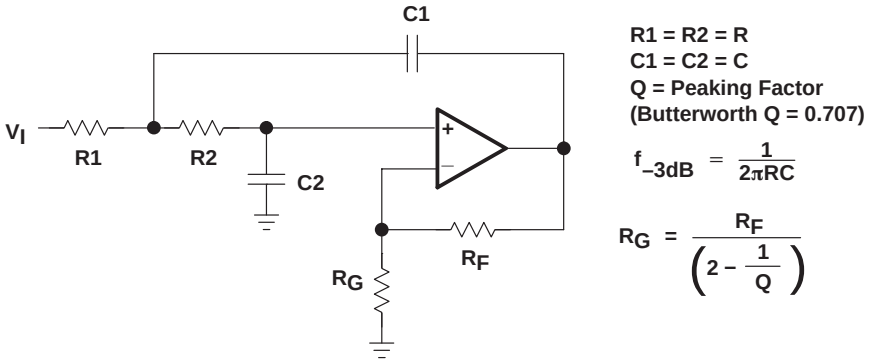


Figure 64. 2-Pole Low-Pass Sallen-Key Filter

ADSL

The ADSL receive band consists of up to 255 separate carrier frequencies each with its own modulation and amplitude level. With such an implementation, it is imperative that signals received off the telephone line have as high a signal-to-noise ratio (SNR) as possible. This is because of the numerous sources of interference on the line. The best way to accomplish this high SNR is to have a low-noise preamplifier on the front-end. It is also important to have the lowest distortion possible to help minimize against interference within the ADSL carriers. The THS7001 and THS7002 was designed with these two priorities in mind.

By taking advantage of the superb characteristics of the complimentary bipolar process (BICOM), the THS7001 and THS7002 offers extremely low noise and distortion while maintaining a high bandwidth. There are some aspects that help minimize distortion in any amplifier. The first is to extend the bandwidth of the amplifier as high as possible without peaking. This allows the amplifier to eliminate any nonlinearities in the output signal. Another thing that helps to minimize distortion is to increase the load impedance seen by the amplifier, thereby reducing the currents in the output stage. This will help keep the output transistors in their linear amplification range and will also reduce the heating effects.

One central-office side terminal circuit implementation, shown in Figure 65, uses a 1:2 transformer ratio. While creating a power and output voltage advantage for the line drivers, the 1:2 transformer ratio reduces the SNR for the received signals. The ADSL standard, ANSI T1.413, stipulates a noise power spectral density of –140 dBm/Hz, which is equivalent to 31.6 nV/$\sqrt{\text{Hz}}$ for a 100 Ω system. Although many amplifiers can reach this level of performance, actual ADSL system testing has indicated that the noise power spectral density may typically be ≤ –150 dBm/Hz, or ≤ 10 nV/$\sqrt{\text{Hz}}$. With a transformer ratio of 1:2, this number reduces to less than 5 nV/$\sqrt{\text{Hz}}$. The THS7002 preamplifiers, with an equivalent input noise of 1.7 nV/$\sqrt{\text{Hz}}$, is an excellent choice for this application. Coupled with a very low 0.9 pA/$\sqrt{\text{Hz}}$ equivalent input current noise and low value resistors, the THS7001 and THS7002 will ensure that the received signal SNR will be as high as possible.

APPLICATION INFORMATION

ADSL (continued)

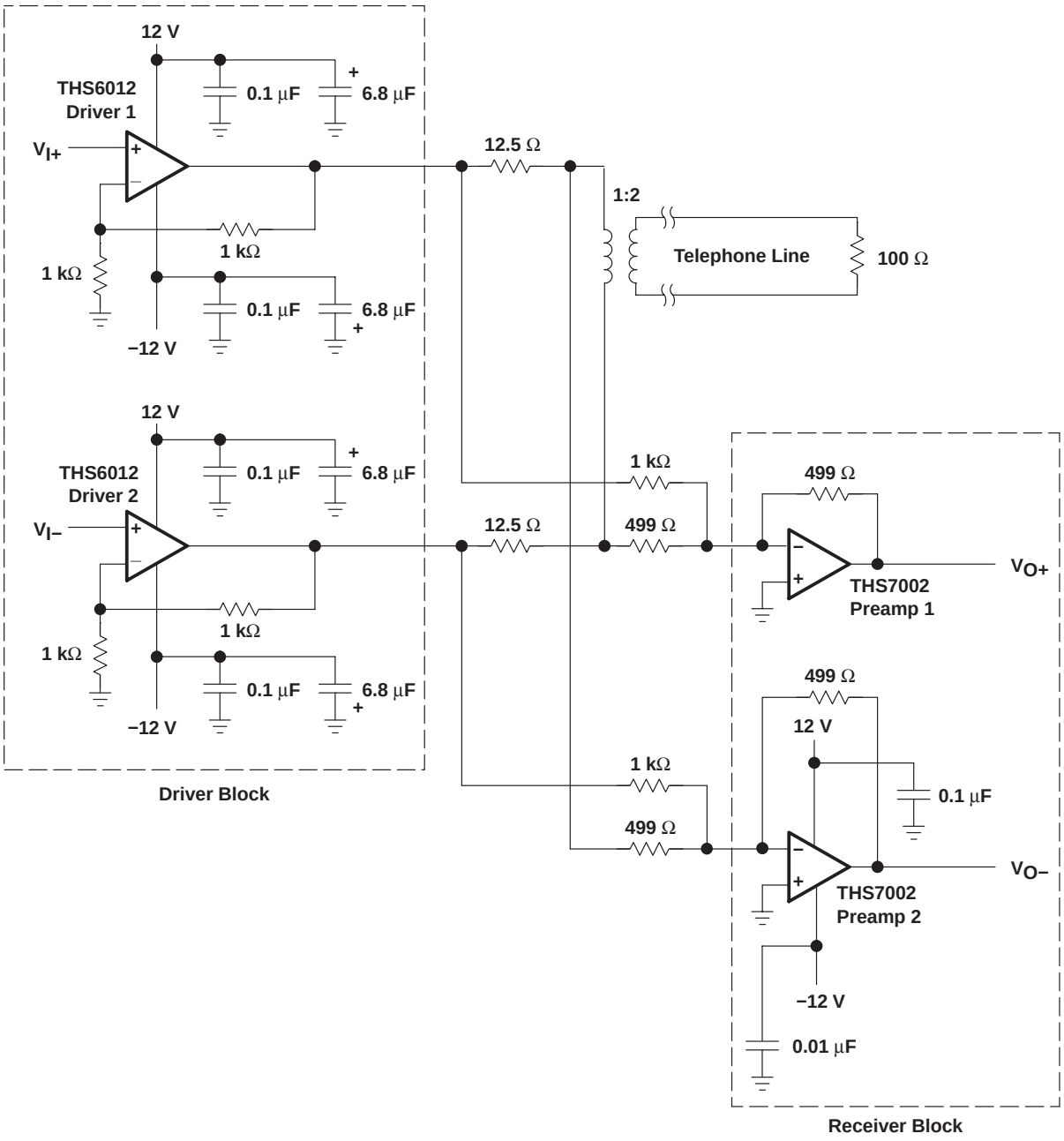


Figure 65. THS7002 Central-Office ADSL Application

APPLICATION INFORMATION

ADSL (continued)

Typically, the outputs of the preamplifiers are carried into a CODEC, which incorporates an analog-to-digital converter (ADC). The problem with this setup is that it only uses fixed gain elements. But, when the client is close to the central office, the gain must be set to receive a high-level signal; or for the opposite, set to receive a low-level signal. To solve this problem, a programmable-gain amplifier (PGA) should be used. The THS7001 and THS7002 PGAs allow the gain of the receiver signals to be varied from −22 dB to 20 dB. By allowing the gains to be controlled with a TTL-compatible signal, it is very easy to integrate the THS7001 and THS7002 into any system.

By having the preamplifier output separate from the PGA input, inserting more amplifiers into the system can be accomplished easily. The functionality of the amplifier is typically as an active fixed gain filter. This is shown in Figure 66.

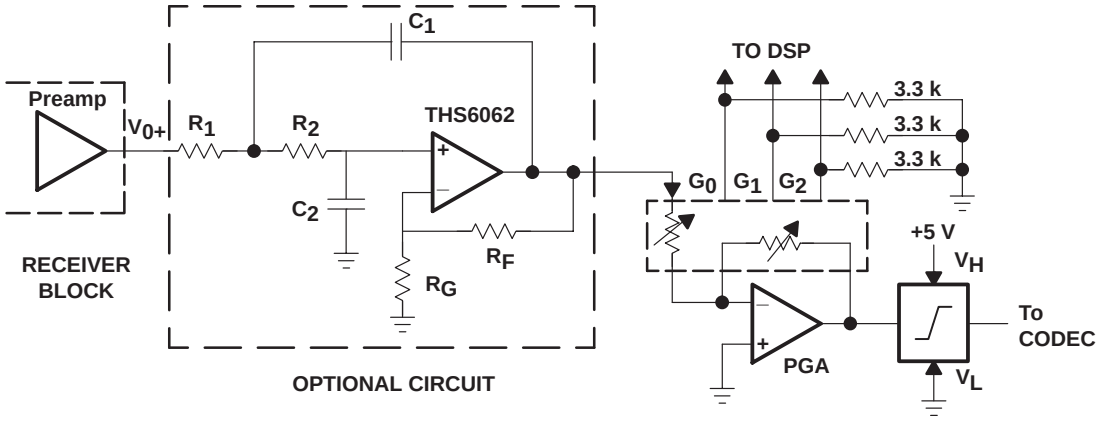


Figure 66. Typical PGA Setup (One Channel)

circuit layout considerations

In order to achieve the levels of high-frequency performance of the THS7001 and THS7002, it is essential that proper printed-circuit board high-frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS7001 and THS7002 evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches (2,54 mm) between the device power terminals and the ceramic capacitors.
- Sockets—Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.

APPLICATION INFORMATION

circuit layout considerations (continued)

- Short trace runs/compact part placements—Optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

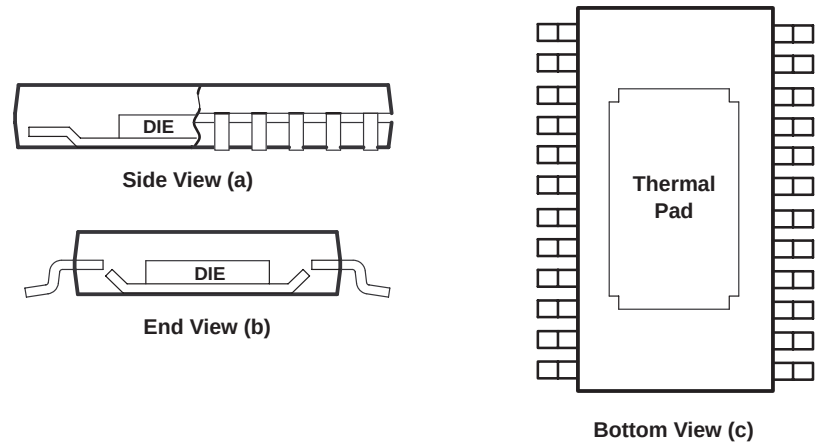
thermal information

The THS7001 and THS7002 is supplied in a thermally-enhanced PWP package, which is a member of the PowerPAD. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 67(a) and Figure 67(b)]. This arrangement exposes the lead frame as a thermal pad on the underside of the package [see Figure 67(c)]. Because this pad has direct contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area requirement and ease of assembly of surface mount with the heretofore awkward mechanical methods of heatsinking.

thermal information (continued)



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 67. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

general PowerPAD design considerations

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

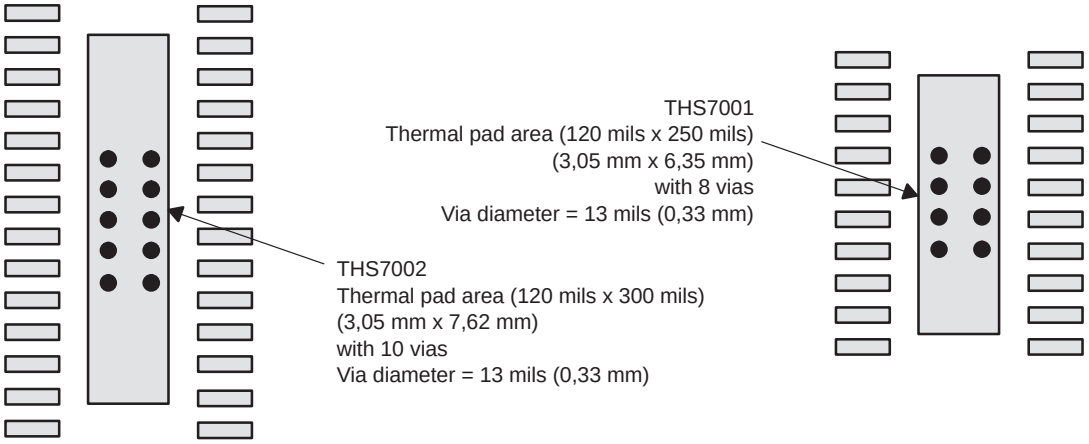


Figure 68. PowerPAD PCB Etch and Via Pattern

1. Prepare the PCB with a top side etch pattern as shown in Figure 68. There should be etch for the leads as well as etch for the thermal pad.
2. Place the thermal transfer holes in the area of the thermal pad. These holes should be 13 mils (0,33 mm) in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the IC. These additional vias may be larger than the 13-mil (0,33 mm) diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the IC package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its thermal transfer holes exposed. The bottom-side solder mask should cover the thermal transfer holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS7001PWP/THS7002PWP IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

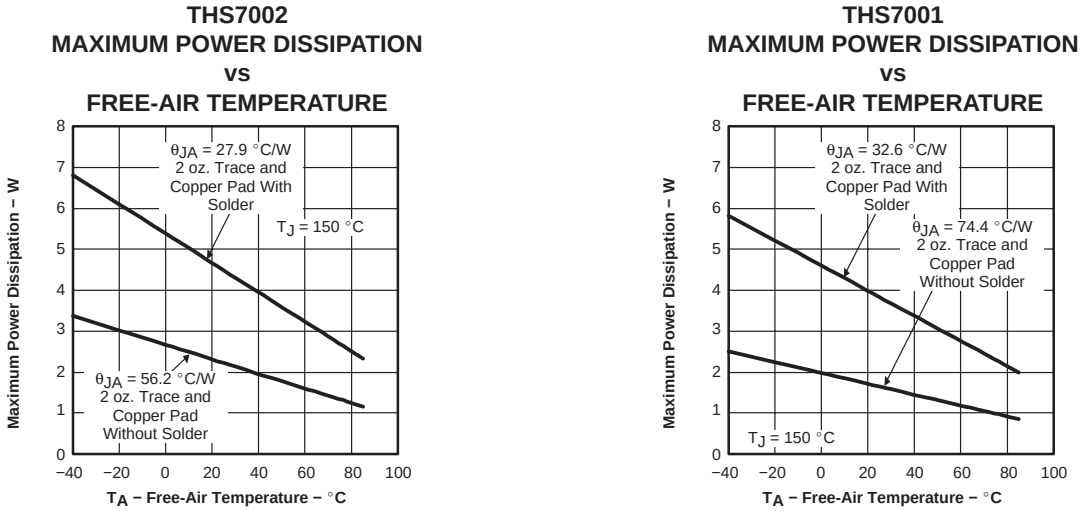
general PowerPAD design considerations (continued)

The actual thermal performance achieved with the THS7001PWP/THS7002PWP in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches (76,2 mm x 76.2 mm), then the expected thermal coefficient, θ_{JA}, is about 32.6°C/W for the THS7001 and 27.9°C/W for the THS7002. For a given θ_{JA}, the maximum power dissipation is shown in Figure 69 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS7001 and THS7002 IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (THS7001 = 1.4°C/W; THS7002 = 0.72°C/W)
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and PCB size = 3”× 3” (76,2 mm x 76,2 mm)

Figure 69. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments technical brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

evaluation board

An evaluation board is available both the THS7001 (literature number SLOP250) and for the THS7002 (literature number SLOP136). These boards has been configured for very low parasitic capacitance in order to realize the full performance of the amplifiers. These EVM’s incorporate DIP switches to demonstrate the full capabilities of the THS7001 and THS7002 independent of any digital control circuitry. For more information, please refer to the *THS7001 EVM User’s Guide* (literature number SLOU057)and the *THS7002 EVM User’s Guide* (literature number SLOU037). To order a evaluation board contact your local TI sales office or distributor.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS7001CPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	THS7001C
THS7001CPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	THS7001C
THS7001CPWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	THS7001C
THS7001CPWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	THS7001C
THS7001IPWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7001I
THS7001IPWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS7001I
THS7002CPWP	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	THS7002C
THS7002CPWP.A	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	0 to 70	THS7002C
THS7002IPWP	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	THS7002I
THS7002IPWP.A	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	THS7002I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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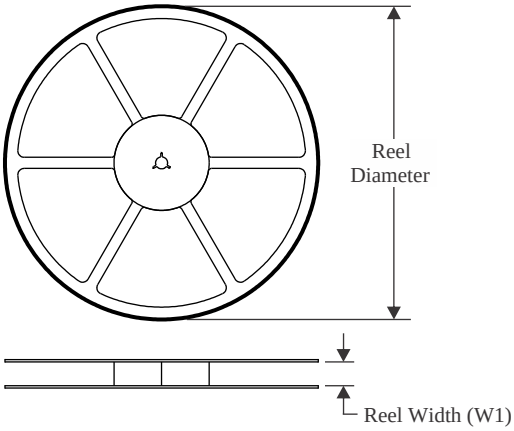
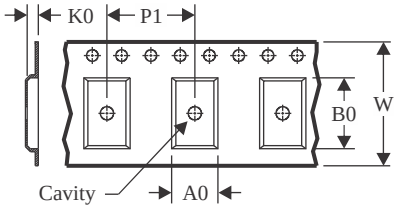
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

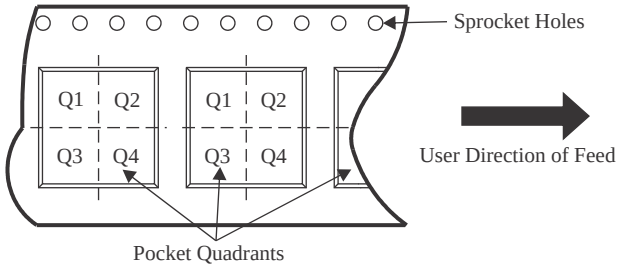


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

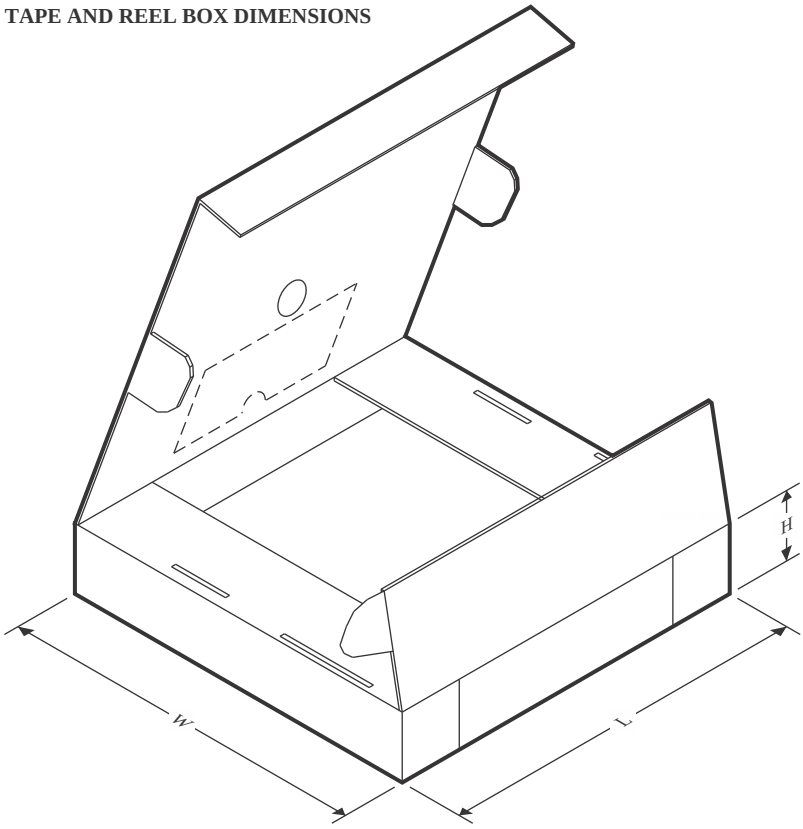
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7001CPWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

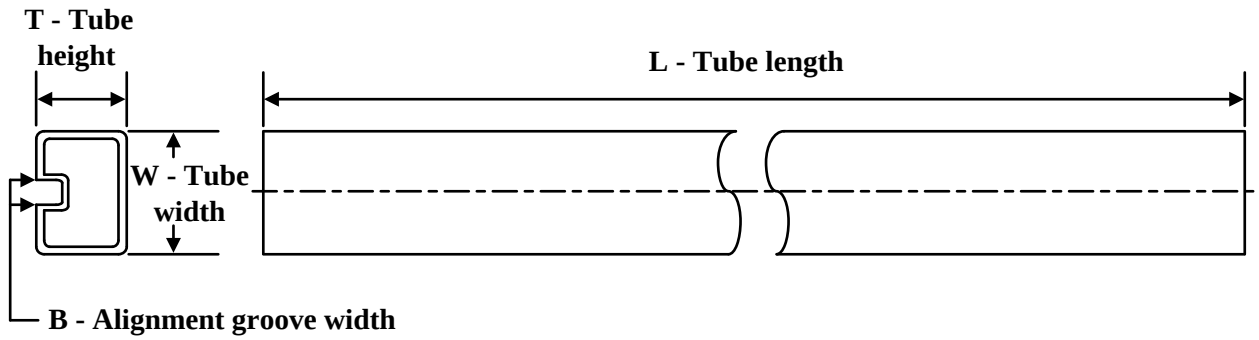
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7001CPWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS7001CPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
THS7001CPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
THS7001IPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
THS7001IPWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
THS7002CPWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
THS7002CPWP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5
THS7002IPWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
THS7002IPWP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

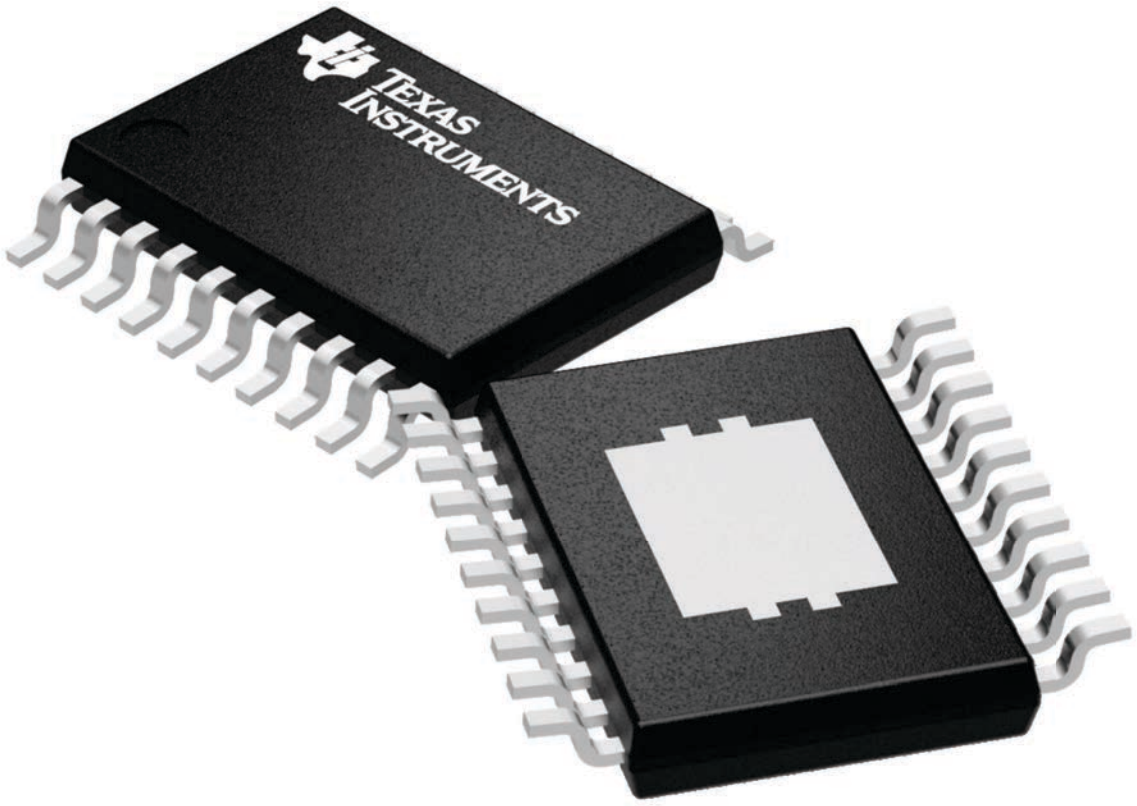
PWP 20

HTSSOP - 1.2 mm max height

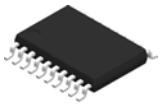
6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

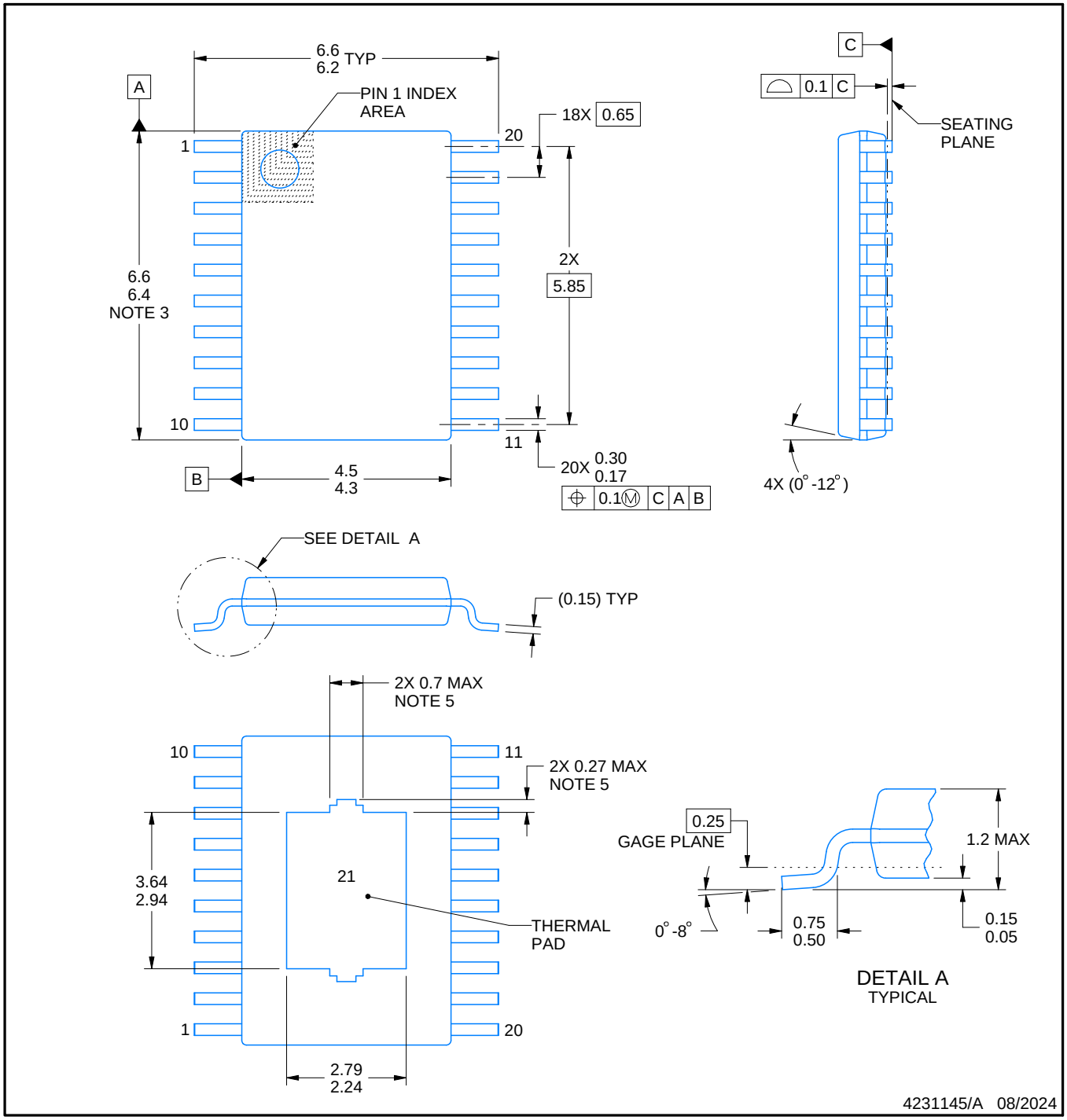


PACKAGE OUTLINE

PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

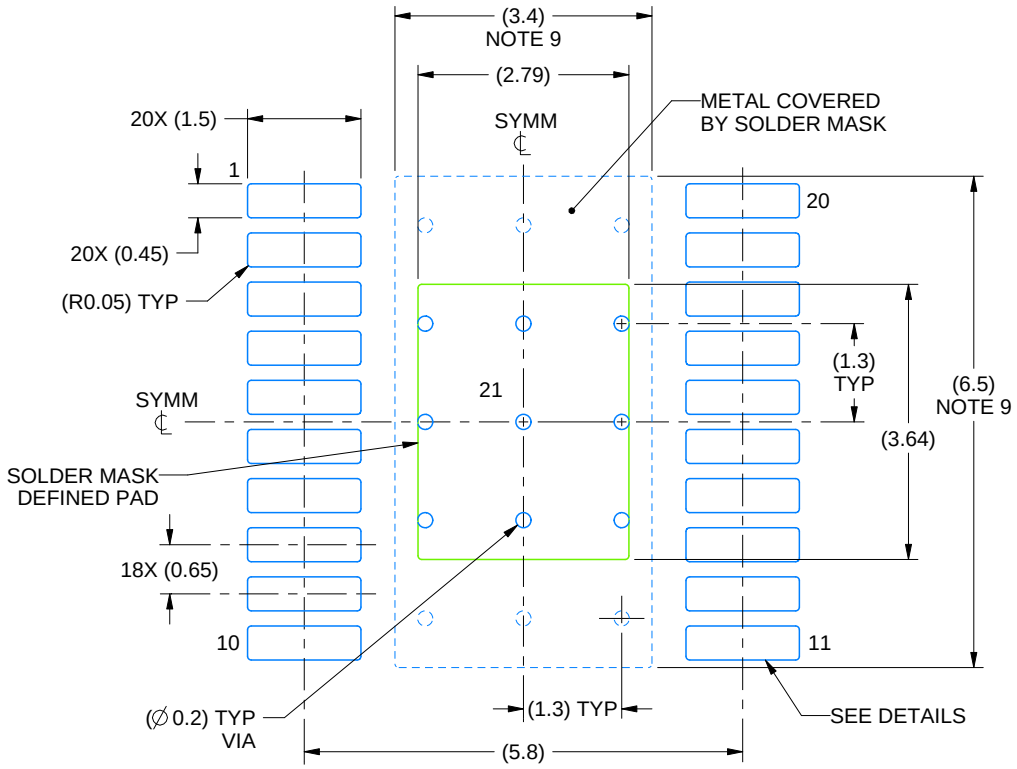
SMALL OUTLINE PACKAGE



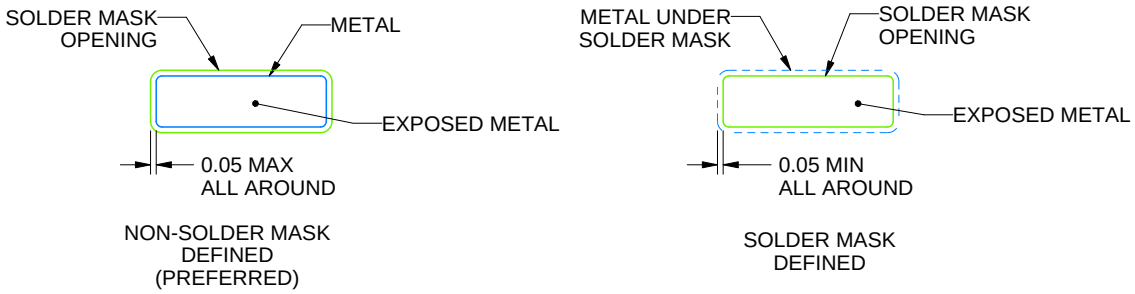
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

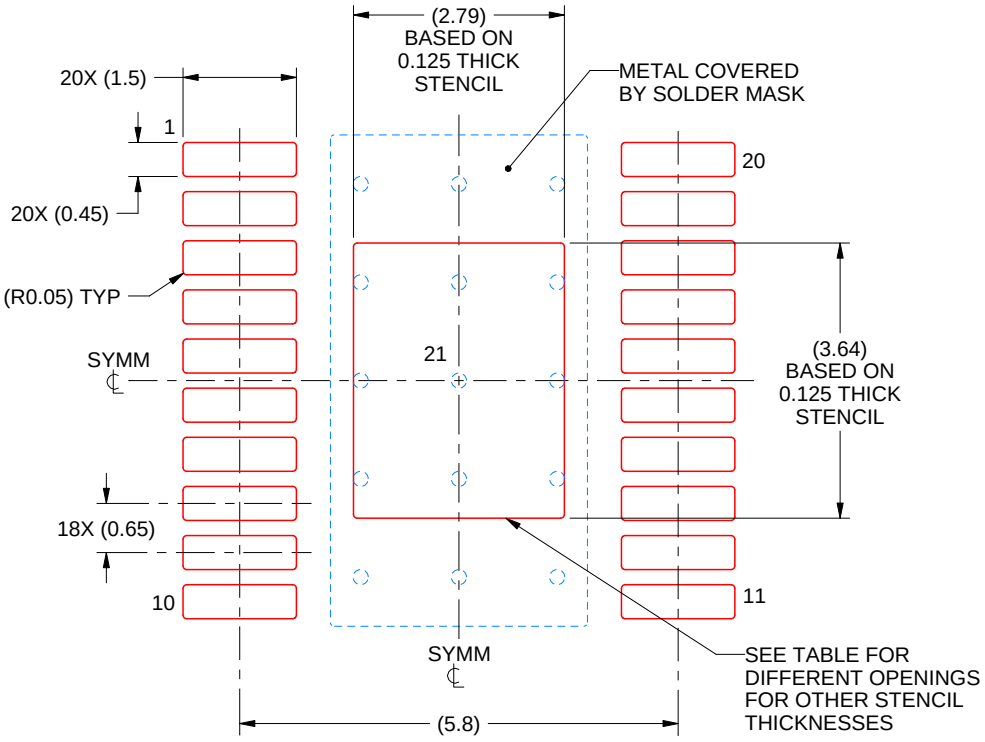


SOLDER MASK DETAILS

4231145/A 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.12 X 4.07
0.125	2.79 X 3.64 (SHOWN)
0.15	2.55 X 3.32
0.175	2.36 X 3.08

4231145/A 08/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

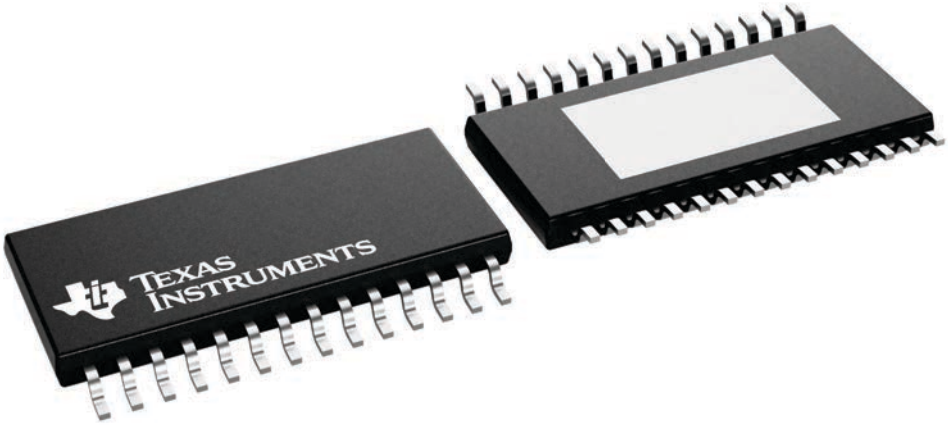
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

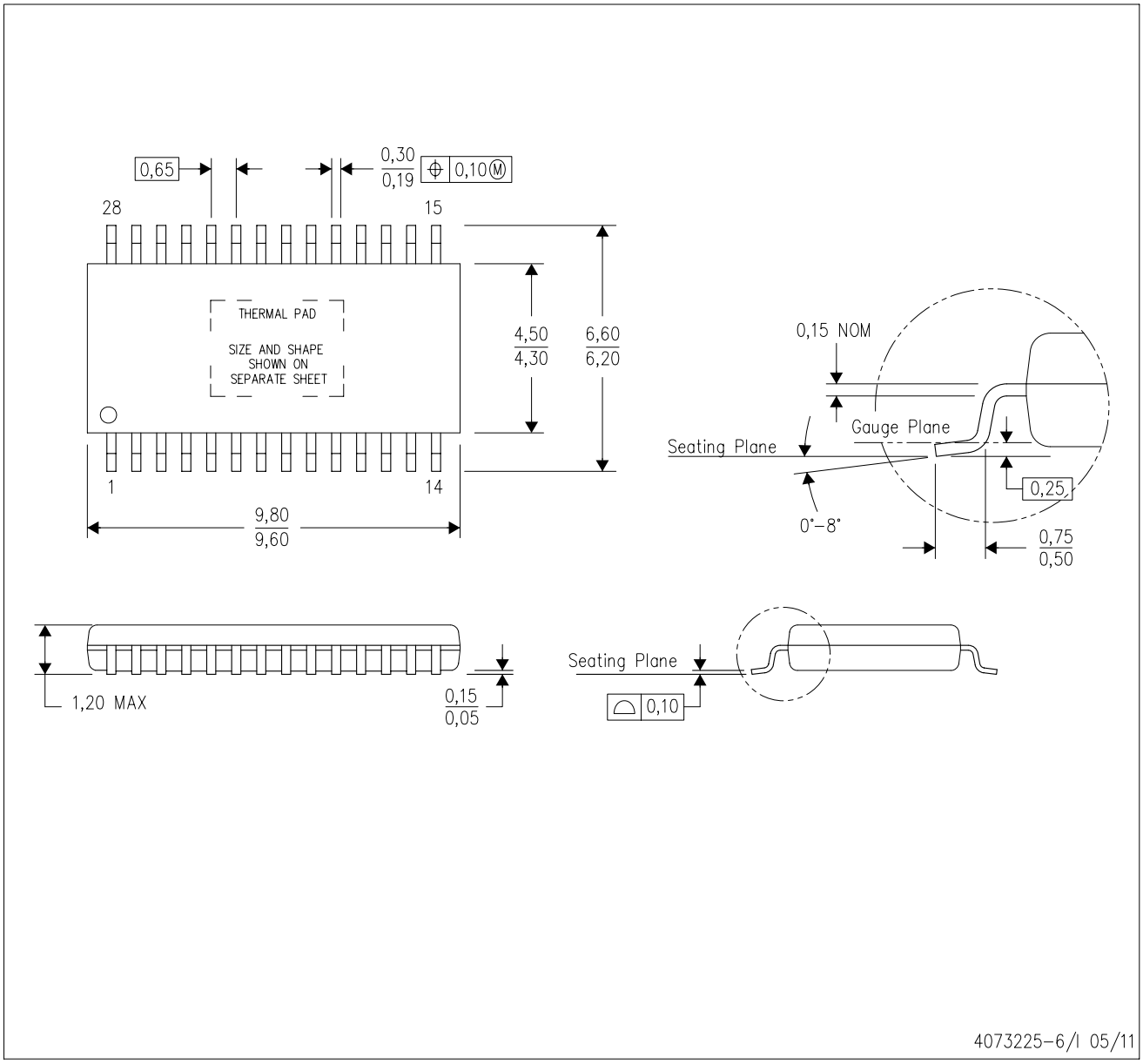
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

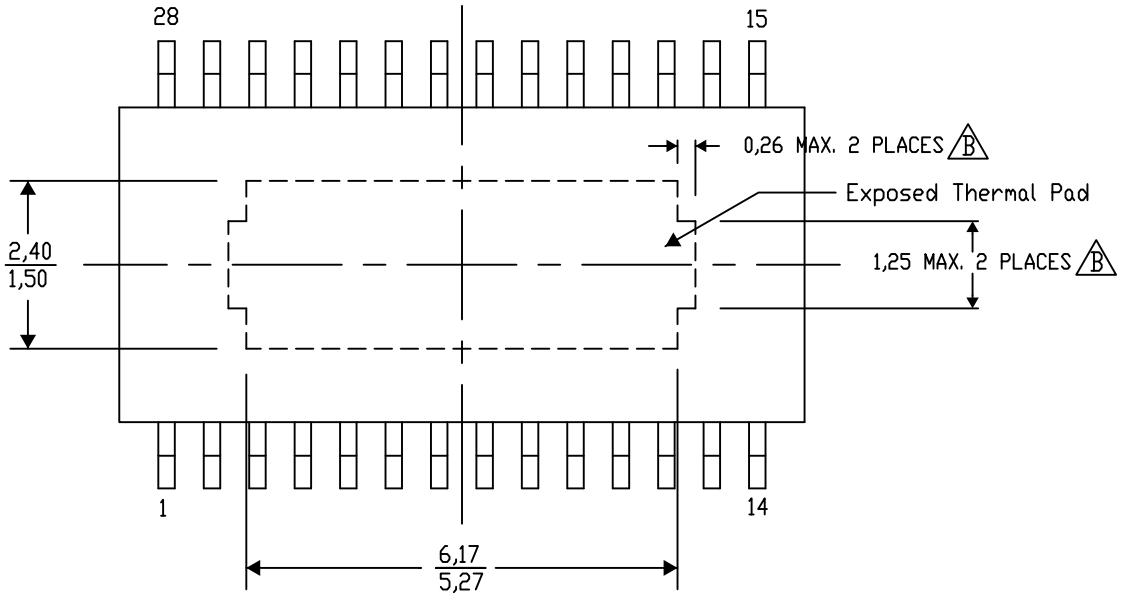
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

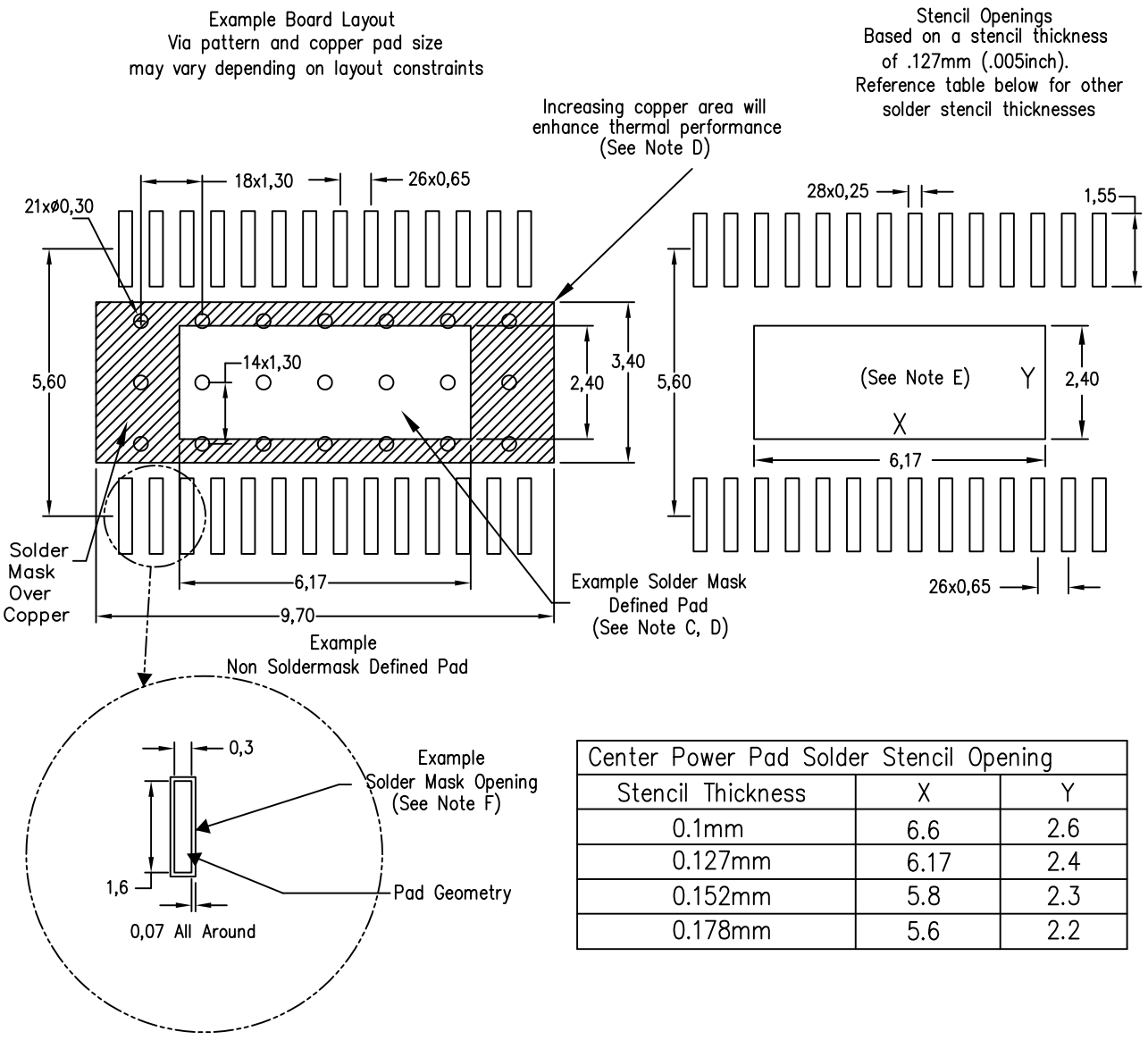
4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609–19/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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