High-Slew-Rate, Single-Supply Operational Amplifier

1 Features

- Wide gain-bandwidth product: 4.5MHz
- Fast settling time 2µs to 0.1%
- Wide-range single-supply operation: 4V to 36V
- Wide input common-mode range includes ground (V_{CC-})
- Output short-circuit protection

2 Description

Quality, low-cost fabrication with remarkable design concepts is employed for the TL3472 operational amplifier. This device offers 4.5MHz of gain-bandwidth product, and fast settling time. Although the TL3472 can be operated from split supplies, device is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential (V_{CC-}). This device exhibits high input resistance, low input offset voltage, and high gain. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

Package Information

PART NUMBER(1)	PACKAGE(1)	PACKAGE SIZE
TL3472	D (SOIC, 8)	4.9mm × 3.9mm
	P (PDIP, 8)	9.5mm x 6.35mm

(1) For all available packages, see the orderable addendum at the end of the data sheet

Table of Contents

3 Pin Configuration and Functions

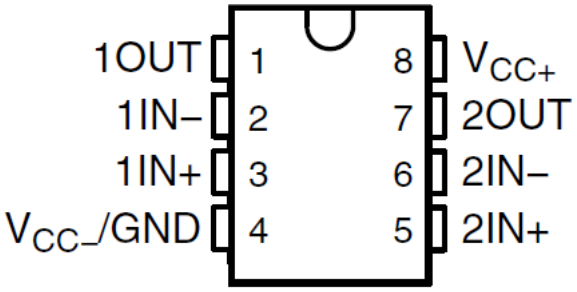

Figure 3-1. D or P Package
Top View

Table 3-1. Pin Functions: TL3472

PIN		TYPE	DESCRIPTION
NAME	NO.		
1OUT	1	O	Output 1
1IN–	2	I	Inverting input
1IN+	3	I	Non inverting input
GND	4	—	Ground
2IN+	5	I	Non inverting input
2IN–	6	I	Inverting input
2OUT	7	O	Output 2
VCC+	8	—	Input voltage

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameters		Test conditions	MIN	MAX	UNIT
	Supply voltage(2)	V_{CC+}		18	V
		V_{CC-}		–18	
V_{ID}	Differential input voltage(3)		–36	36	V
V_I	Input voltage	Any input	V_{CC-}	V_{CC+}	V
I_I	Input current	Each input	–1	1	mA
I_O	Output current		–80	80	mA
	Total current into V_{CC+}			80	mA
	Total current out of V_{CC-}			80	mA
	Duration of short-circuit current at (or below) 25°C(4)			Unlimited	
θ_{JA}	Package thermal impedance(5) (6)	D package		130.7	°C/W
		P package		85	
T_J	Operating virtual junction temperature			150	°C
	Lead temperature 1.6mm (1/16inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* can cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 4.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at the non inverting input with respect to the inverting input. Excessive input current can flow when the input is less than V_{CC-}−0.3V.
(4) The output can be shorted to either supply. Temperature and/or supply voltages must be limited to the maximum dissipation rating is not exceeded.
(5) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

4.2 Recommended Operating Conditions

Parameters			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		4	36	V
V_{IC}	Common-mode input voltage	V_{CC} = 5V	0	2.8	V
		$V_{CC\pm}$ = ±15V	−15	12.8	
T_A	Operating free-air temperature	TL3472C	0	70	°C
		TL3472I	−40	105	

4.3 Electrical Characteristics

at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A	MIN	TYP[1]	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0, R_S = 50Ω	V_{CC} = 5V		25°C		1.5	10	mV
			V_{CC} = ±15 V		25°C		1.0	10	
					Full range[2]			12	
a_{VIO}	Temperature coefficient of input offset voltage		V_{CC} = ±15 V		Full range[2]		10		µV/°C
I_{IO}	Input offset current		V_{CC} = ±15 V		25°C		0.01	75	nA
					Full range[2]			300	
I_{IB}	Input bias current		V_{CC} = ±15 V		25°C		0.01	500	nA
					Full range[2]			700	
V_{ICR}	Common-mode input voltage range	R_S = 50Ω			25°C		−15 to 12.8		V
					Full range[2]		−15 to 12.8		
V_{OH}	High-level output voltage	V_{CC+} = 5V	V_{CC-} = 0,	R_L = 2kΩ	25°C	3.7	4.8		V
		R_L = 10kΩ			25°C	13.6	14.8		
		R_L = 2kΩ			Full range[2]	13.4			
V_{OL}	Low-level output voltage	V_{CC+} = 5V	V_{CC-} = 0,	R_L = 2kΩ	25°C		0.005	0.3	V
		R_L = 10kΩ			25°C		−14.8	−14.3	
		R_L = 2kΩ			Full range[2]			−13.5	
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V,		R_L = 2kΩ	25°C	25	100		V/mV
					Full range[2]	20			
I_{OS}	Short-circuit output current	Source: V_{ID} = 1V,		V_O = 0	25°C	−10	−75		mA
		Sink: V_{ID} =−1V,		V_O = 0		20	75		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}(min),		R_S = 50Ω	25°C	65	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±13.5 V to ±16.5 V,		R_S = 100Ω	25°C	70	97		dB
I_{CC}	Supply current (per channel)	V_O = 0,		No load	25°C		0.56	4.5	mA
					Full range[2]			5.5	
		V_{CC+} = 5V, V_O = 2.5V, V_{CC-} = 0, No load			25°C			4.5	

(1) All typical values are at T_A = 25°C.
(2) Full range is 0°C to 70°C for the TL3472C device and −40°C to 105°C for the TL3472I device.

4.4 Operating Characteristics

Differential input resistance

$V_{CC±}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	V_I =−10V to 10V, R_L = 2kΩ, C_L = 300pF	A_V = 1	8	10		V/μs
SR−	Negative slew rate		A_V = −1		13		V/μs
t_s	Settling time	A_{VD} = −1, 10V step	To 0.1%		2		μs
			To 0.01%		2.5		
V_n	Equivalent input noise voltage	f = 1kHz,	R_S = 100Ω		10.8		nV/√Hz
I_n	Equivalent input noise current	f = 1kHz			2		fA/√Hz
GBW	Gain-bandwidth product	f =100 kHz			4.5		MHz
BW	Power bandwidth	$V_{O(PP)}$ = 20V, R_L= 2kΩ, A_{VD} = 1, THD = 5.0%			85		kHz
φ_m	Phase margin	R_L = 2kΩ	C_L = 0		70		deg
			C_L = 300pF		50		
	Gain margin	R_L = 2kΩ	C_L = 0		12		dB
			C_L = 300pF		4		
r_i	Differential input resistance	V_{IC} = 0			540		GΩ
C_i	Input capacitance	V_{IC} = 0			10		pF
	Channel separation	f = 10kHz			101		dB
z_o	Open-loop output impedance	f = 1MHz,	A_V = 1		525		Ω

5 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.3 Trademarks

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5.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (September 2003) to Revision H (December 2025)	Page
• Deleted High slew-rate	1
• Deleted Low harmonic distortion	1
• Deleted Large capacitance drive capability	1
• Changed Wide bandwidth product from 4MHz to 4.5MHz	1
• Changed Fast setting time from 1.1µs to 2µs	1
• Updated Gain-bandwidth product from 4MHz to 4.5MHz	1
• Deleted Ordering information table	1
• Deleted Schematic Information	1
• Updated Thermal impedance D package value from 97°C/W to 130.7°C/W	4
• Updated Input offset current from 6nA to 0.01nA	5
• Updated Input bias current from 100nA to 0.01nA	5
• Updated Low-level Output voltage at 10kΩ from −14.7V to −14.8V	5
• Updated High-level Output voltage from 4V to 4.8V	5
• Updated High-level Output voltage at 10kΩ from 14V to 14.8V	5
• Updated Low-level Output voltage from 0.1V to 5mV	5
• Updated Short circuit output current for source from −34mA to −75mA	5
• Updated Low-level Input voltage for sink from 27mA to 75mA	5
• Updated Supply current from 3.5mA to 0.56mA	5
• Updated Settling time from 1.1µs to 2µs for 0.1% and 2.2µs to 2.5µs for 0.01%	6

- Updated Equivalent input noise voltage from 49nV/√Hz to 10.8nV/√Hz 6
- Updated Equivalent input noise current from 0.22pA/√Hz to 2fA/√Hz 6
- Updated Gain bandwidth product from 4MHz to 4.5MHz..... 6
- Deleted Gain bandwidth product minimum value..... 6
- Updated Power bandwidth value from 160kHz to 85KHz..... 6
- Updated Differential input resistance from 150MΩ to 540GΩ..... 6
- Updated Input capacitance from 2.5pF to 10pF..... 6
- Updated Open-loop output impedance from 20Ω to 525Ω..... 6

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL3472CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3472C
TL3472CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3472C
TL3472CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3472CP
TL3472CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3472CP
TL3472IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3472
TL3472IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z3472
TL3472IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3472IP
TL3472IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	TL3472IP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL3472 :

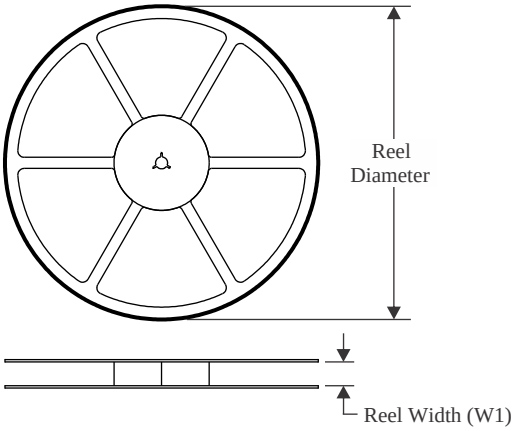
- Automotive : TL3472-Q1

NOTE: Qualified Version Definitions:

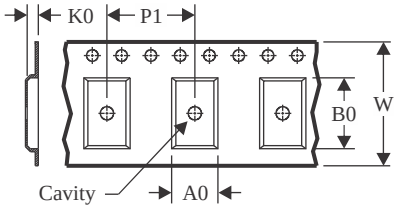
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

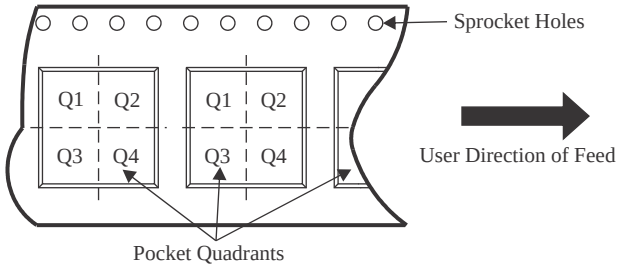


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

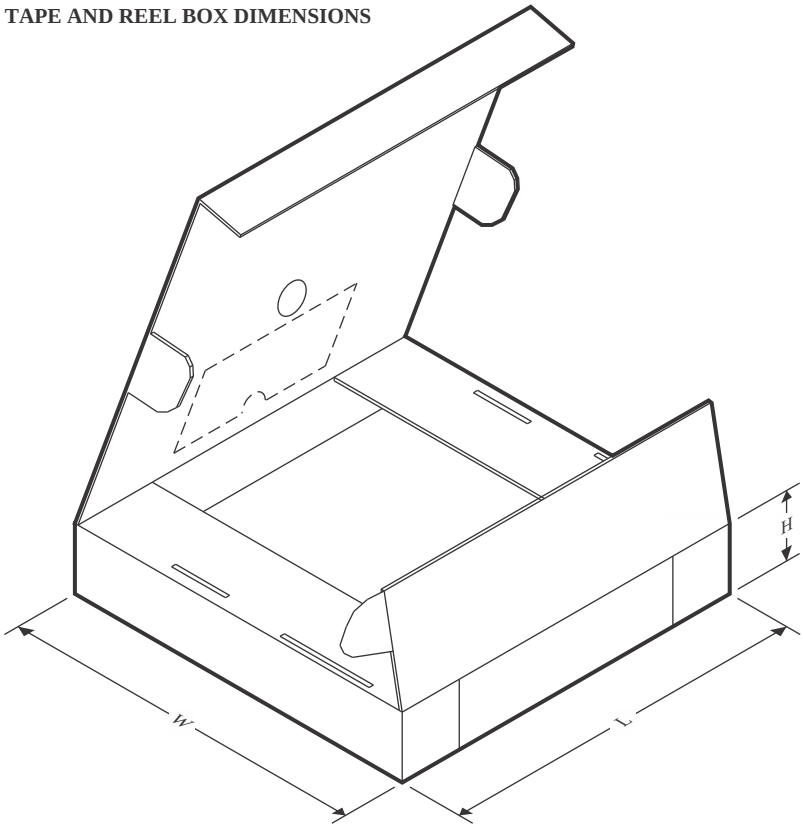
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3472CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3472IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

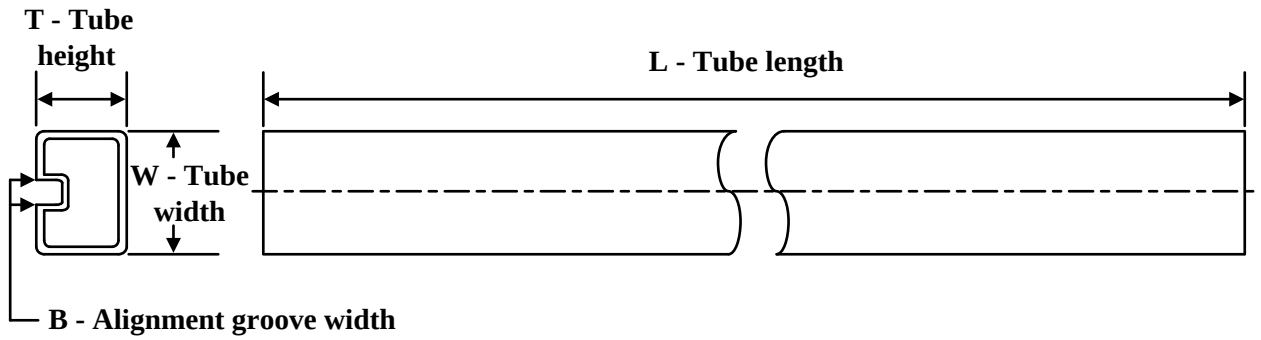
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

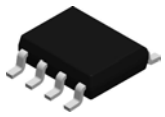
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3472CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL3472IDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL3472CP	P	PDIP	8	50	506	13.97	11230	4.32
TL3472CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL3472IP	P	PDIP	8	50	506	13.97	11230	4.32
TL3472IP.A	P	PDIP	8	50	506	13.97	11230	4.32

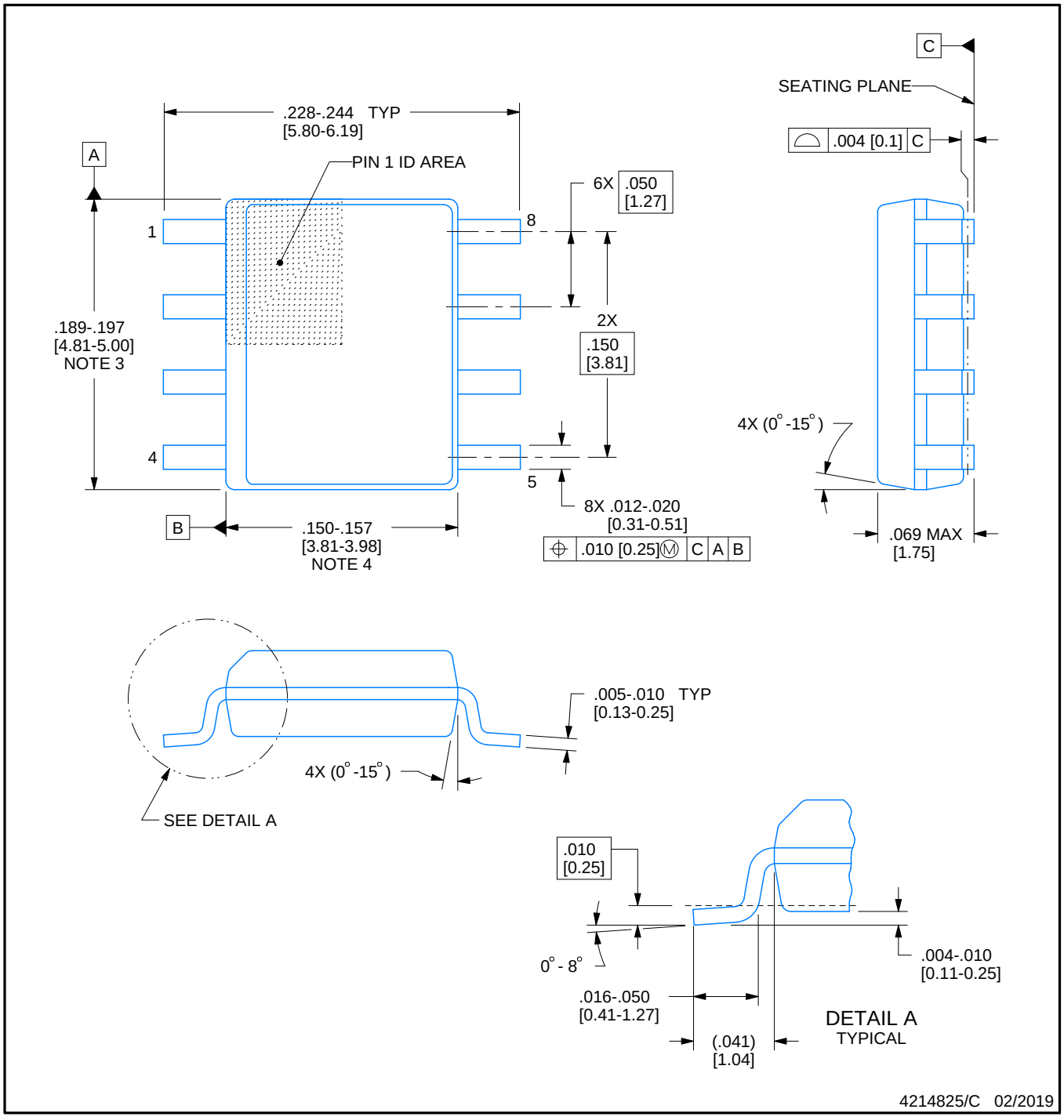


PACKAGE OUTLINE

D0008A

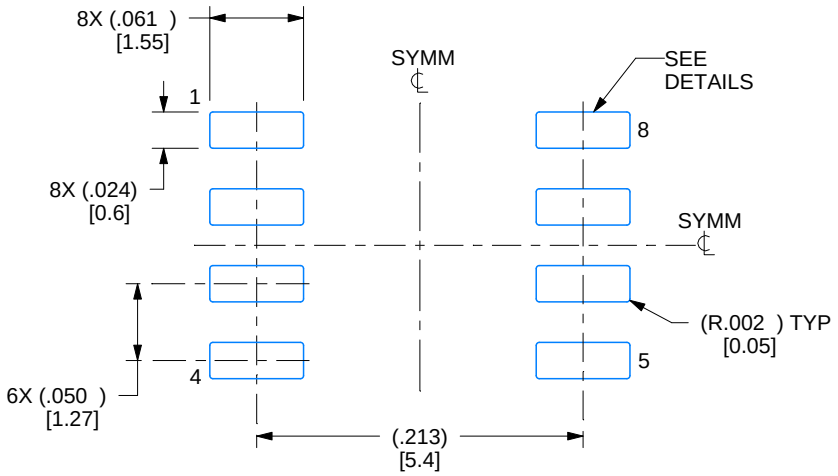
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

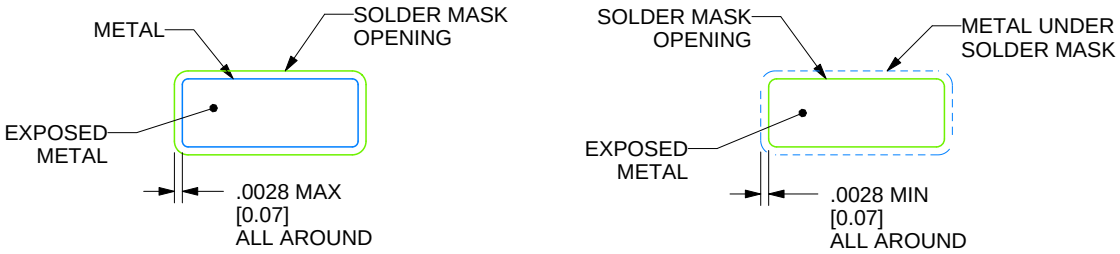


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

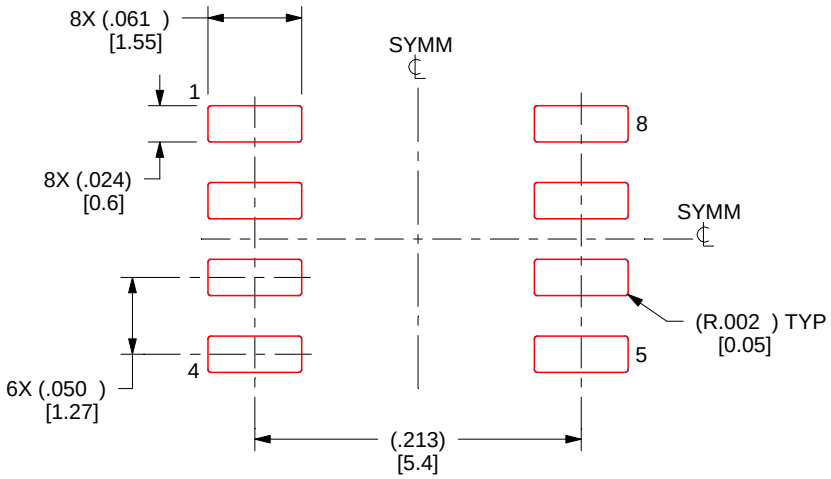
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



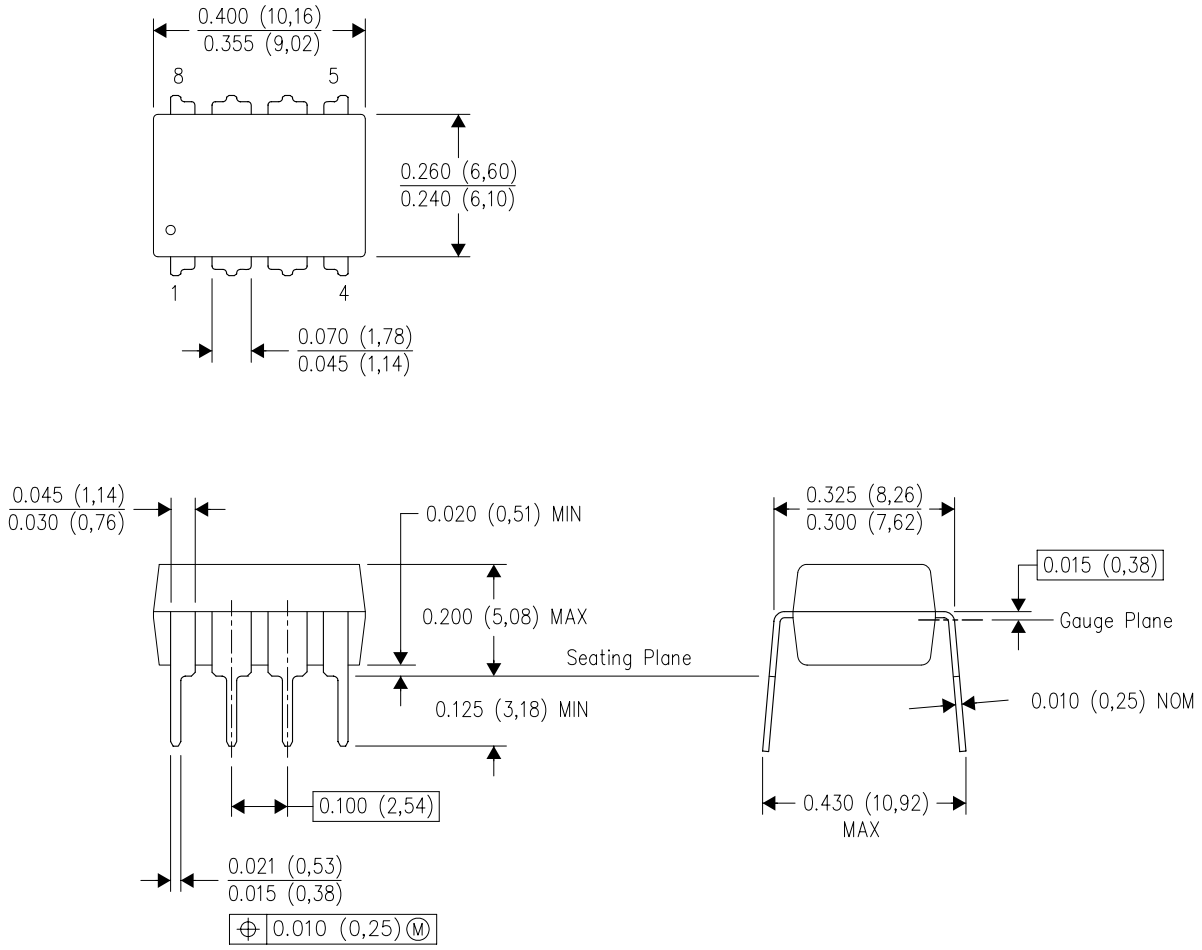
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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Last updated 10/2025