TLC27xx Precision Dual Operational Amplifiers

1 Features

- Wide range of supply voltages over specified temperature range:
  - 0°C to 70°C: 3V to 16V
  - –40°C to 125°C: 4V to 16V
  - –55°C to 125°C: 4V to 16V
- Single-supply operation
- Common-mode input voltage range extends below the negative rail (C-suffix, I-suffix types)
- Low noise: typically 10.8nV/√Hz at f = 1kHz
- Output voltage range includes negative rail
- High input impedance: >10^{12} Ω typical
- ESD-protection circuitry
- Small-outline package option also available in tape and reel
- Designed-in latch-up immunity

2 Description

The TLC272 and TLC277 precision dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching those of general-purpose BiFET devices.

The extremely high input impedance, low bias currents, and boosted slew rates make these cost effective devices an excellent choice for applications previously reserved for BiFET and NFET products.Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC272 (10mV) to the high-precision TLC277 (500µV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

Device Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TLC272	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.9mm × 6mm
	PS (SOP, 8)	6.2mm × 7.8mm
	PW (TSSOP, 8)	3mm × 6.4mm
TLC272A	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.9mm × 6mm
TLC272B	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.9mm × 6mm
	PS (SOP, 8)	6.2mm × 7.8mm
TLC277	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.9mm × 6mm
	PS (SOP, 8)	6.2mm × 7.8mm

(1) For more information, see Section 9
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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3 Pin Configuration and Functions

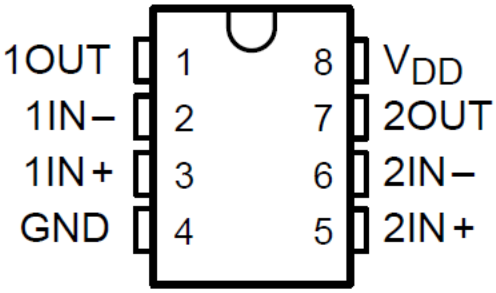


Figure 3-1. D, JG, P, or PW Package (Top View)

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage(2)			18	V
V_{ID}	Differential input voltage(3)		$-V_{DD}$	$+V_{DD}$	
V_I	Input voltage range	Any input	–0.3	V_{DD}	V
I_I	Input current		–5	5	mA
I_O	Output current	Each output	–30	30	mA
	Total current into V_{DD}			45	mA
	Total current out of GND			45	mA
	Duration of short-circuit current at (or below) 25°C(4)			Unlimited	
T_A	Operating free-air temperature	C suffix	0	70	°C
		I suffix	–40	85	
T_{stg}	Storage temperature		–65	150	°C
	Lead temperature 1,6mm (1/16 inch) from case for 10 seconds	D package		260	°C
		P package			
		PW package			
	Lead temperature 1,6mm (1/16 inch) from case for 60 seconds	JG package		300	°C

(1) Stresses beyond those listed under Section 4.1 can cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 4.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at IN+ with respect to IN –.
(4) The output can be shorted to either supply. Temperature and/or supply voltages must be limited to make sure that the maximum dissipation rating is not exceeded (see application section).

4.2 Recommended Operating Conditions

			C SUFFIX		I SUFFIX		UNIT
			MIN	MAX	MIN	MAX	
V_{DD}	Supply voltage		3	16	4	16	V
V_{IC}	Common-mode input voltage	V_{DD} = 5V	–0.2	3.5	–0.2	3.5	V
		V_{DD} = 10V	–0.2	8.5	–0.2	8.5	
T_A	Operating free-air temperature		0	70	–40	85	°C

4.3 Electrical Characteristics

at specified free-air temperature, V_{DD} = 5V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4V R_S = 50Ω	V_{IC} = 0, R_L = 10kΩ	25°C		0.12	10	mV
					Full range			12	
		TLC272AC	V_O = 1.4V, R_S = 50Ω	V_{IC} = 0, R_L = 10kΩ	25°C		0.12	5	
					Full range			6.5	
		TLC272BC	V_O = 1.4V, R_S = 50Ω	V_{IC} = 0, R_L = 10kΩ	25°C		0.12	2000	µV
					Full range			3000	
		TLC277C	V_O = 1.4V R_S = 50Ω	V_{IC} = 0 R_L = 10kΩ	25°C		0.12	500	
					Full range			1500	
a_{VIO}	Temperature coefficient of input offset voltage				25°C to 70°C		0.3		µV/°C
I_{IO}	Input offset current(1)		V_O = 2.5V	V_{IC} =2.5 V	25°C		10	60	pA
					70°C		7	300	
I_{IB}	Input bias current(1)				25°C		10	60	pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range(2)				25°C	–0.1 to 4	–0.3 to 4.2		V
					Full range	–0.1 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100mV	R_L = 10kΩ	25°C	3.2	4.95		V
					0°C	3	4.95		
					70°C	3	4.95		
V_{OL}	Low-level output voltage		V_{ID} = –100 mV	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25V to 2V	R_L = 10kΩ	25°C	5	1000		V/mV
					0°C	4			
					70°C	4			
CMRR	Common-mode rejection ratio		V_{IC} = –0.1V < VIC < 3V		25°C	65	80		dB
					0°C	60			
					70°C	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5V to 10V	V_O =1.4 V	25°C	65	120		dB
					0°C	60			
					70°C	60			
I_{DD}	Supply current (two amplifiers)		V_O = 2.5V, No load	V_{IC} = 2.5V,	25°C		1.12	3.2	mA
					0°C			3.6	
					70°C			2.6	

(1) The typical values of input bias current and input offset current below 5pA were determined mathematically.
(2) This range also applies to each input individually.

4.4 Electrical Characteristics

at specified free-air temperature, V_{DD} = 10V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4V R_S = 50Ω,	V_{IC} = 0, R_L = 10kΩ	25°C		0.12	10	mV
					Full range			12	
		TLC272AC	V_O = 1.4V R_S = 50Ω	V_{IC} = 0, R_L = 10kΩ	25°C		0.12	5	
					Full range			6.5	
		TLC272BC	V_O = 1.4V, R_S = 50Ω	V_{IC} = 0, R_L = 10kΩ	25°C		0.12	2000	µV
					Full range			3000	
		TLC277C	V_O = 1.4V R_S = 50Ω	V_{IC} = 0 R_L = 10kΩ	25°C		0.12	800	
					Full range			1900	
a_{VIO}	Temperature coefficient of input offset voltage				25°C to 70°C		0.3		µV/°C
I_{IO}	Input offset current(1)		V_O = 5V	V_{IC} = 5V	25°C		10	60	pA
					70°C		7	300	
I_{IB}	Input bias current(1)				25°C		10	60	pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range(2)				25°C	–0.1 to 9	–0.3 to 9.2		V
					Full range	–0.1 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100mV	R_L = 10kΩ	25°C	8	9.95		V
					0°C	7.8			
					70°C	7.8			
V_{OL}	Low-level output voltage		V_{ID} = –100 mV	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1V to 6V	R_L = 10kΩ	25°C	10	1000		V/mV
					0°C	7.5			
					70°C	7.5			
CMRR	Common-mode rejection ratio		V_{IC} = -0.1V < V_{IC} < 8V		25°C	65	85		dB
					0°C	60			
					70°C	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5V to 10V	V_O = 1.4V	25°C	65	120		dB
					0°C	60			
					70°C	60			
I_{DD}	Supply current (two amplifiers)		V_O = 5V, No load	V_{IC} = 5V	25°C		1.12	4	mA
					0°C			4.4	
					70°C			3.4	

(1) The typical values of input bias current and input offset current below 5pA were determined mathematically.
(2) This range also applies to each input individually.

4.5 Electrical Characteristics

at specified free-air temperature, V_{DD} = 5V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4V R_S = 50Ω	V_{IC} = 0 R_L = 10kΩ	25°C		0.12	10	mV
					Full range			13	
		TLC272AI	V_O = 1.4V R_S = 50Ω	V_{IC} = 0 R_L = 10kΩ	25°C		0.12	5	
					Full range			7	
		TLC272BI	V_O = 1.4V R_S = 50Ω	V_{IC} = 0 R_L = 10kΩ	25°C		0.12	2000	µV
					Full range			3500	
		TLC277I	V_O = 1.4V R_S = 50Ω	V_{IC} = 0 R_L = 10kΩ	25°C		0.12	500	
					Full range			2000	
a_{VIO}	Temperature coefficient of input offset voltage				25°C to 85°C		0.3		µV/°C
I_{IO}	Input offset current[1]		V_O = 2.5V,	V_{IC} = 2.5V	25°C		10	60	pA
					85°C		24	15	
I_{IB}	Input bias current[1]				25°C		10	60	pA
					85°C		200	35	
V_{ICR}	Common-mode input voltage range[2]				25°C	–0.1 to 4	–0.3 to 4.2		V
					Full range	–0.1 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100mV	R_L = 10kΩ	25°C	3.2	4.95		V
					–40°C	3	4.95		
					85°C	3	4.95		
V_{OL}	Low-level output voltage		V_{ID} = –100 mV	I_{OL} = 0	25°C		0	50	mV
					–40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1V to 6V	R_L = 10kΩ	25°C	5	1000		V/mV
					–40°C	3.5			
					85°C	3.5			
CMRR	Common-mode rejection ratio		V_{IC} = –0.1 V < V_{IC} < 3V		25°C	65	80		dB
					–40°C	60			
					85°C	60			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} /ΔV_{IO})		V_{DD} = 5V to 10V	V_O = 1.4V	25°C	65	120		dB
					–40°C	60			
					85°C	60			
I_{DD}	Supply current (two amplifiers)		V_O = 2.5V, No load	V_{IC} = 2.5V	25°C		1.12	3.2	mA
					–40°C			4.4	
					85°C			2.4	

(1) The typical values of input bias current and input offset current below 5pA were determined mathematically.
(2) This range also applies to each input individually.

4.6 Electrical Characteristics

at specified free-air temperature, V_{DD} =10V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4V R_S = 50Ω	V_{IC} = 0 R_L = 10kΩ	25°C		0.12	10	mV
					Full range			13	
		TLC272AI	V_O = 1.4V R_S = 50Ω	V_{IC} = 0 R_L = 10kΩ	25°C		0.12	5	
					Full range			7	
		TLC272BI	V_O = 1.4V R_S = 50Ω	V_{IC} = 0 R_L = 10kΩ	25°C		0.12	2000	µV
					Full range			3500	
		TLC277I	V_O = 1.4V R_S = 50Ω	V_{IC} = 0 R_L = 10kΩ	25°C		0.12	800	
					Full range			2900	
a_{VIO}	Temperature coefficient of input offset voltage				25°C to 85°C		0.3		µV/°C
I_{IO}	Input offset current[1]		V_O = 5V	V_{IC} = 5V	25°C		10	60	pA
					85°C		26	1000	
I_{IB}	Input bias current[1]				25°C		10	60	pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range[2]				25°C	–0.1 to 9	–0.3 to 9.2		V
					Full range	–0.1 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100mV	R_L = 10kΩ	25°C	8	9.95		V
					–40°C	7.8			
					85°C	7.8			
V_{OL}	Low-level output voltage		V_{ID} = –100 mV,	I_{OL} = 0	25°C		0	50	mV
					–40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1V to 6V	R_L = 10kΩ	25°C	10	1000		V/mV
					–40°C	7			
					85°C	7			
CMRR	Common-mode rejection ratio		V_{IC} = -0.1V < V_{IC} < 8V		25°C	65	85		dB
					–40°C	60			
					85°C	60	88		
kS_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} /ΔV_{IO})		V_{DD} = 5V to 10V	V_O = 1.4V	25°C	65	120		dB
					–40°C	60			
					85°C	60			
I_{DD}	Supply current (two amplifiers)		V_O = 5V, No load	V_{IC} = 5V,	25°C		1.12	4	mA
					–40°C			5	
					85°C			3.2	

(1) The typical values of input bias current and input offset current below 5pA were determined mathematically.
(2) This range also applies to each input individually.

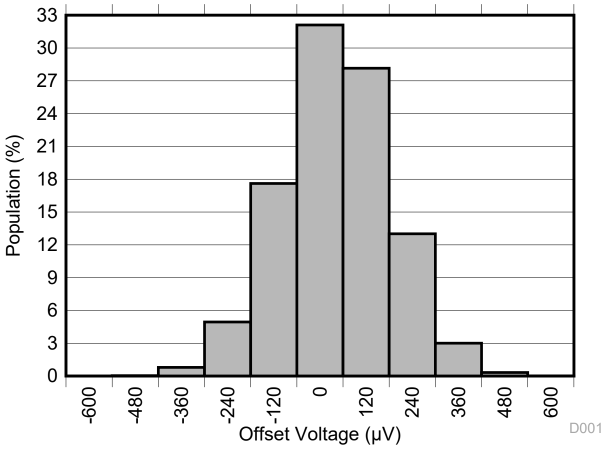
4.7 Operating Characteristics

at specified free-air temperature, V_{DD} = 5V

PARAMETER		TEST CONDITIONS		T_A	TLC272I, TLC272AI,TLC272BI, TLC277I TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 10kΩ C_L = 20pF	V_{IPP} = 100mV	25°C		0.5		V/μs
			V_{IPP} = 1V	25°C		21		
V_n	Equivalent input noise voltage	f = 1kHz	R_S = 20Ω	25°C		10.8		nV/√Hz
B_{OM}	Maximum output-swing bandwidth	V_O = V_{OH} R_L = 10kΩ	C_L = 20pF	25°C		10		kHz
B_1	Unity-gain bandwidth	V_I = 10mV	C_L = 20pF,	25°C		4.5		MHz
φ_m	Phase margin	V_I = 10mV, C_L = 20pF,	f = B_1	25°C		60°		

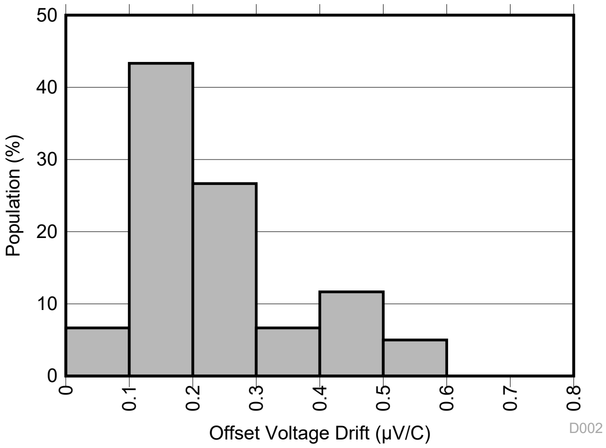
4.8 Typical Characteristics

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)



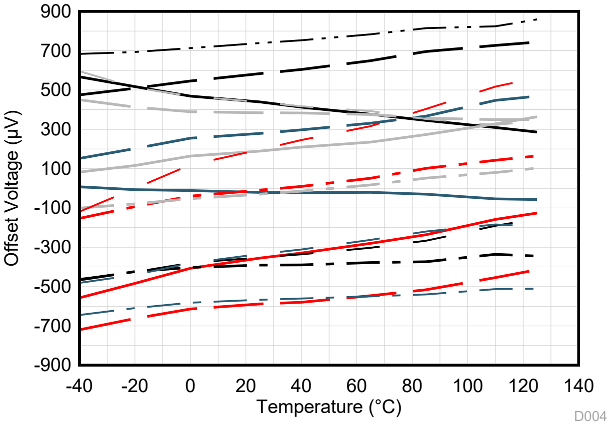
Distribution from 15462 amplifiers, T_A = 25°C

Figure 4-1. Offset Voltage Production Distribution



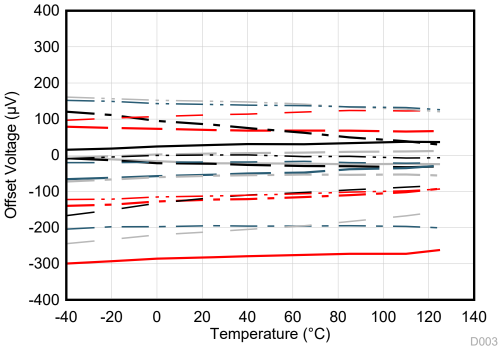
Distribution from 60 amplifiers

Figure 4-2. Offset Voltage Drift Distribution



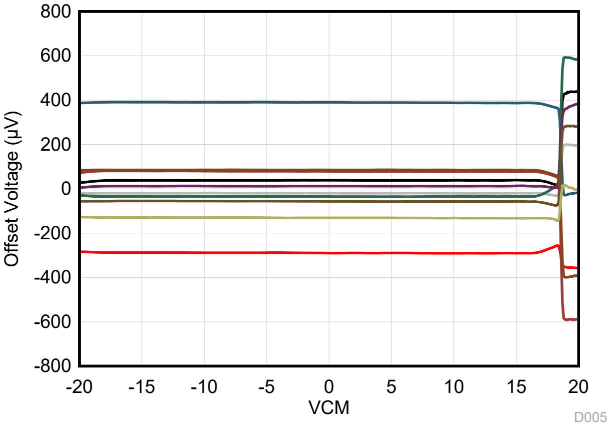
V_{CM} = V+

Figure 4-3. Offset Voltage vs Temperature



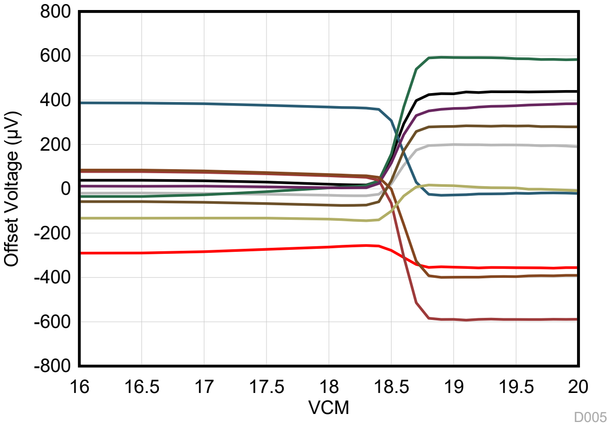
V_{CM} = V–

Figure 4-4. Offset Voltage vs Temperature



T_A = 25°C

Figure 4-5. Offset Voltage vs Common-Mode Voltage

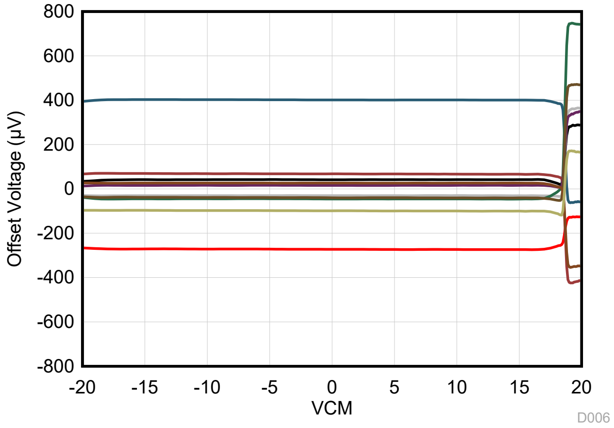


T_A = 25°C

Figure 4-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

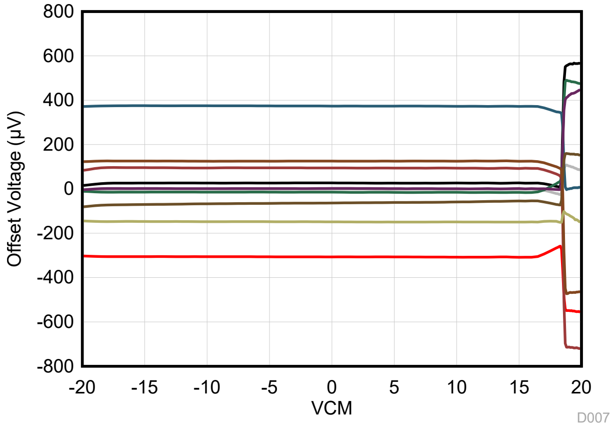
4.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)



T_A = 125°C

Figure 4-7. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

Figure 4-8. Offset Voltage vs Common-Mode Voltage

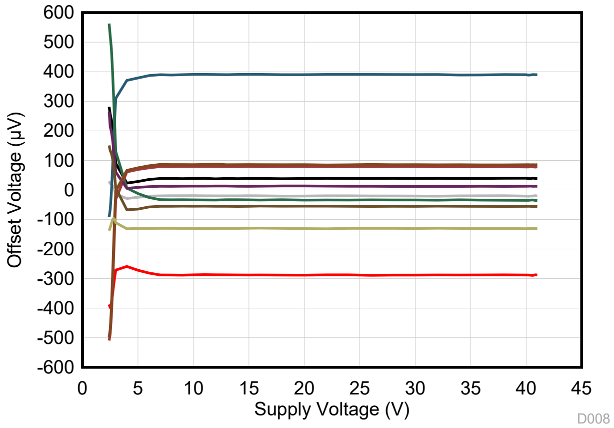
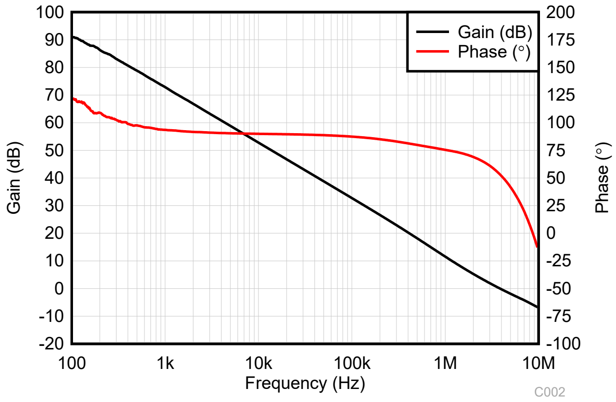


Figure 4-9. Offset Voltage vs Power Supply



C_L = 20pF

Figure 4-10. Open-Loop Gain and Phase vs Frequency

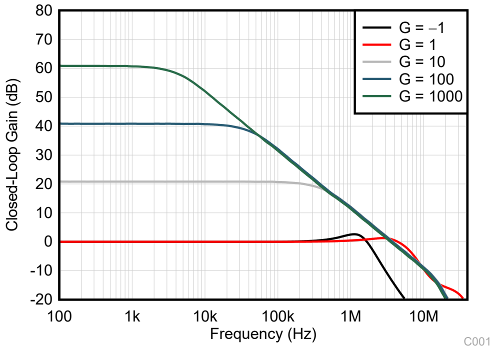


Figure 4-11. Closed-Loop Gain vs Frequency

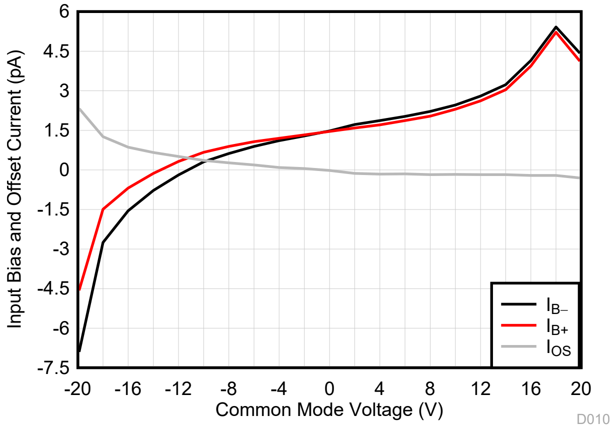


Figure 4-12. Input Bias Current vs Common-Mode Voltage

4.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 10pF (unless otherwise noted)

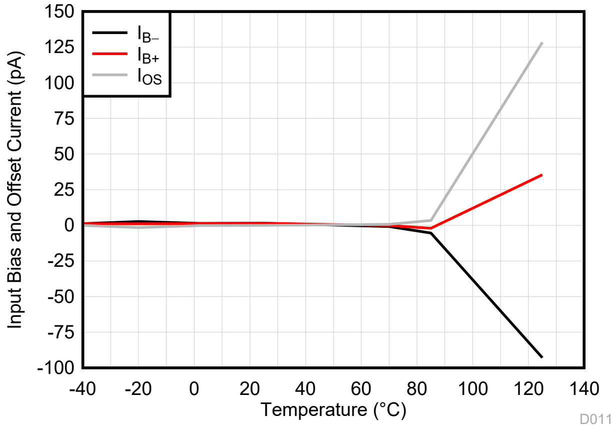


Figure 4-13. Input Bias Current vs Temperature

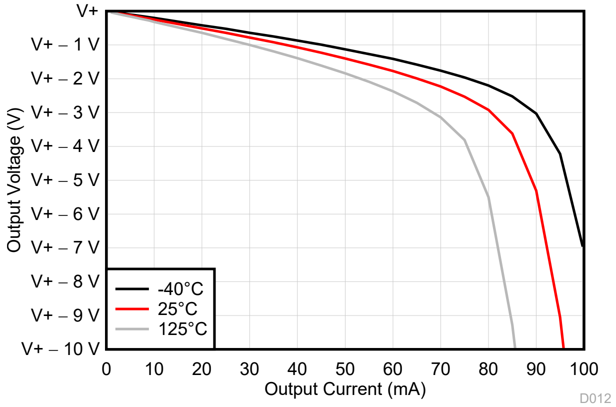


Figure 4-14. Output Voltage Swing vs Output Current (Sourcing)

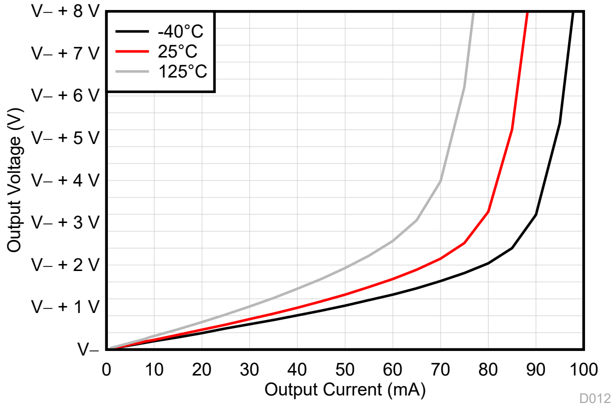


Figure 4-15. Output Voltage Swing vs Output Current (Sinking)

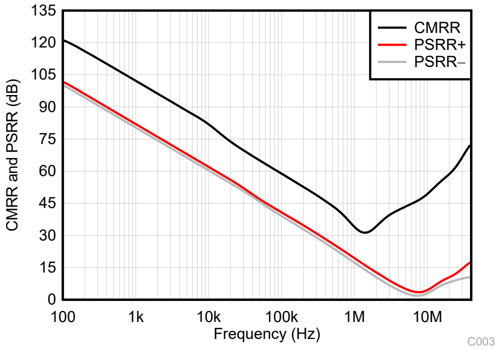
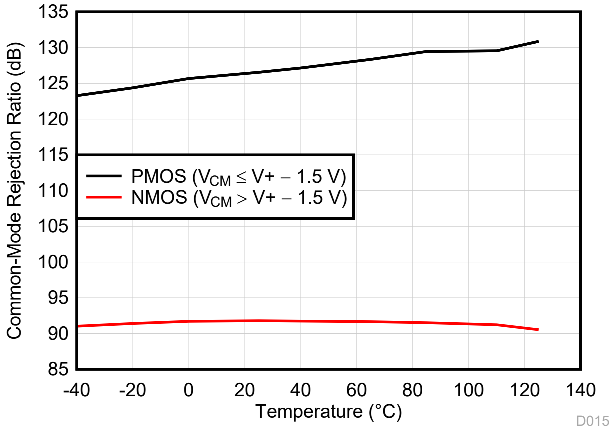
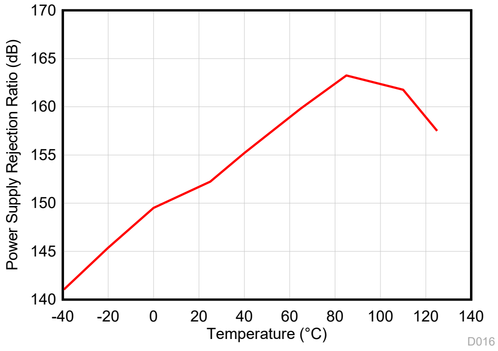


Figure 4-16. CMRR and PSRR vs Frequency



f = 0Hz

Figure 4-17. CMRR vs Temperature (dB)



f = 0Hz

Figure 4-18. PSRR vs Temperature (dB)

5 Parameter Measurement Information

5.1 Single-Supply vs Split-Supply Test Circuits

Because the TLC272 and TLC277 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

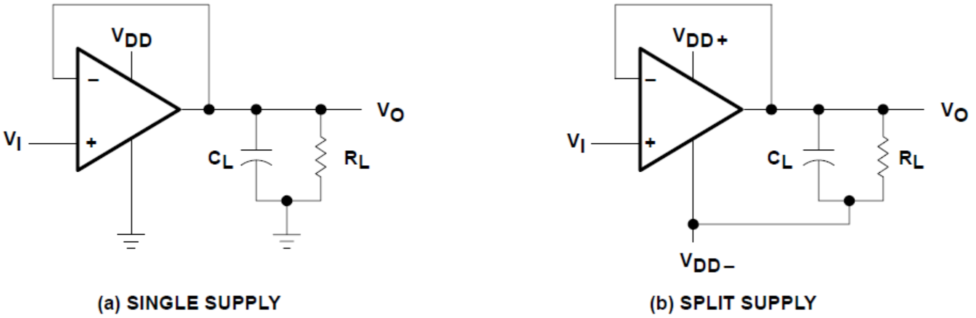


Figure 5-1. Unity-Gain Amplifier

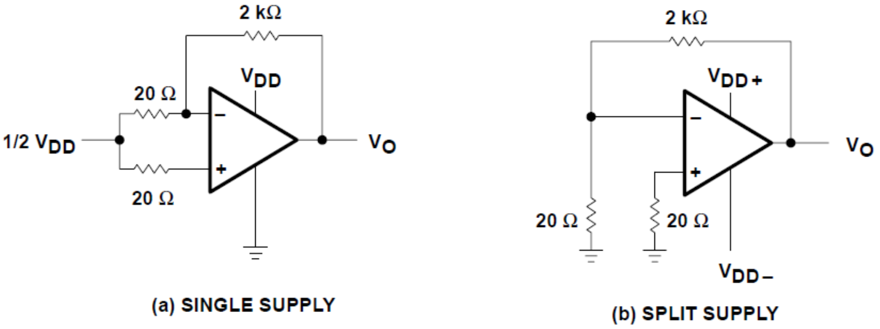


Figure 5-2. Noise-Test Circuit

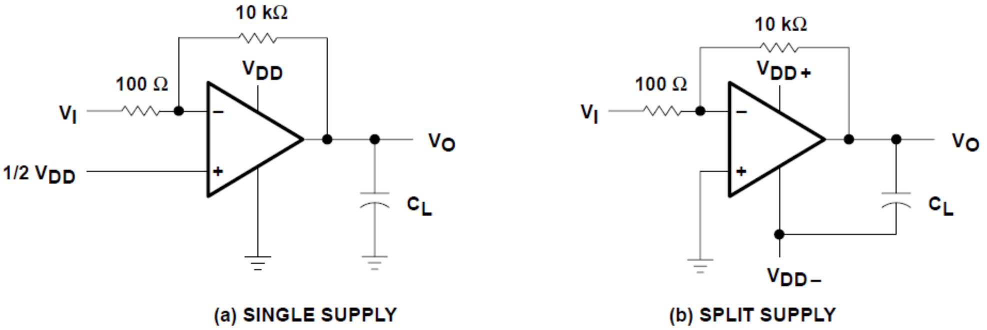


Figure 5-3. Gain-of-100 Inverting Amplifier

5.2 Input Bias Current

Because of the high input impedance of the TLC272 and TLC277 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 5-4). Leakages that otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

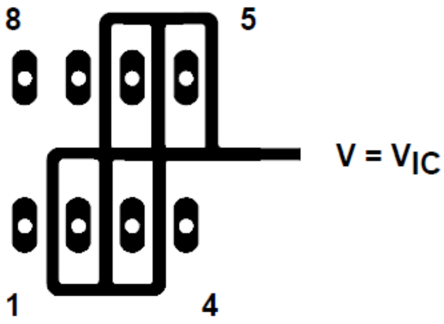


Figure 5-4. Isolation Metal Around Device Inputs (JG and P packages)

5.3 Low-Level Output Voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions must be observed.

5.4 Input Offset Voltage Temperature Coefficient

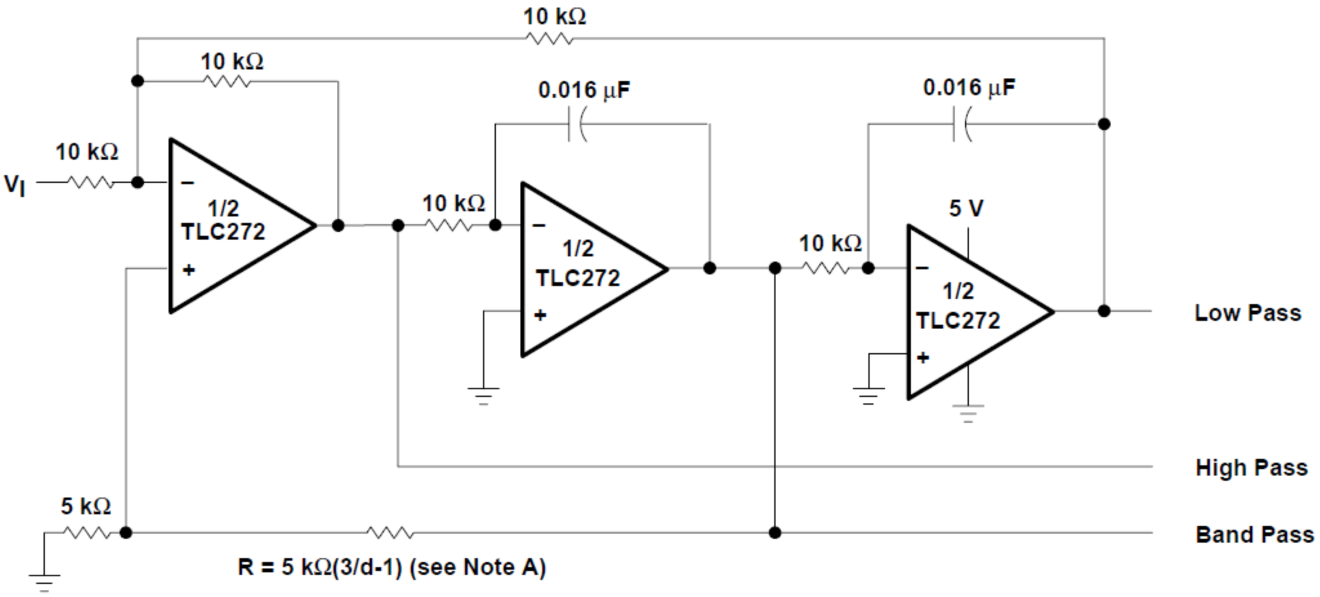
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage because the moisture also covers the isolation metal, thereby rendering the method useless. TI also suggests that these measurements be performed at temperatures above freezing to minimize error.

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information



A. d = damping factor, 1/Q

Figure 6-1. State-Variable Filter

6.1.1 Single-Supply Operation

While the TLC272 and TLC277 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 6-2). The low input bias current of the TLC272 and TLC277 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC272 and TLC277 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 6-3); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications can require RC decoupling.

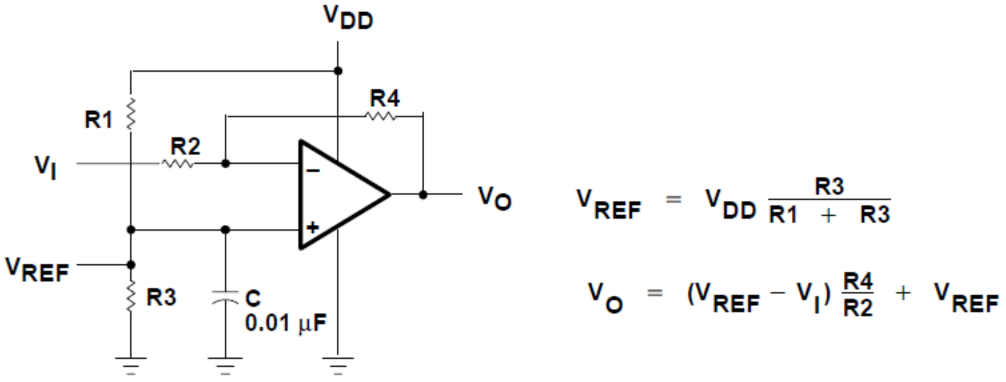
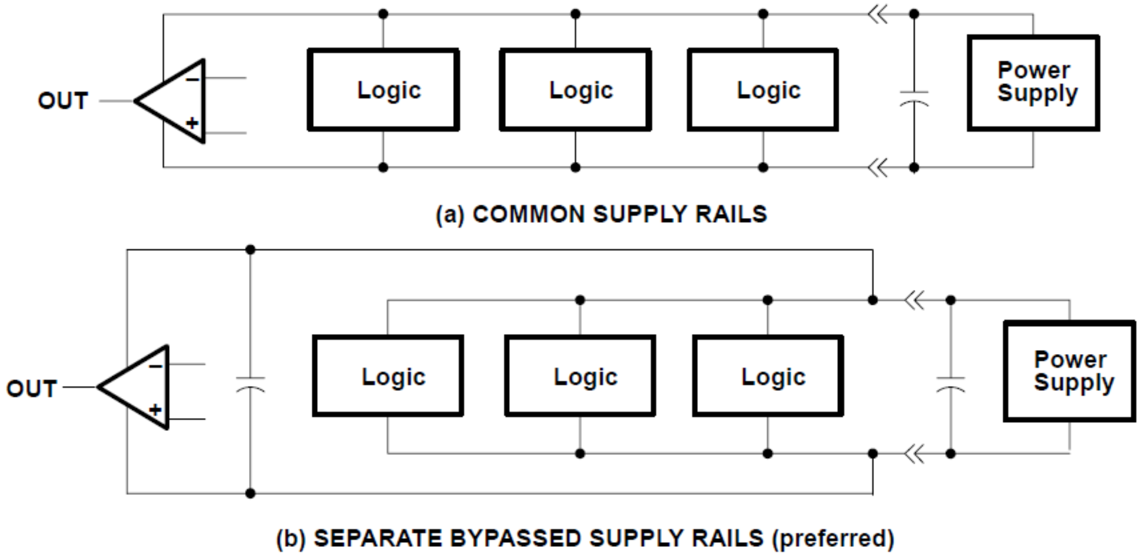


Figure 6-2. Inverting Amplifier With Voltage Reference



(a) COMMON SUPPLY RAILS

(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 6-3. Common vs Separate Supply Rails

6.1.2 Input Characteristics

The TLC272 and TLC277 are specified with a minimum and a maximum input voltage that, if exceeded at either input, can cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1V at T_A = 25°C and at V_{DD} – 1.5V at all other temperatures.

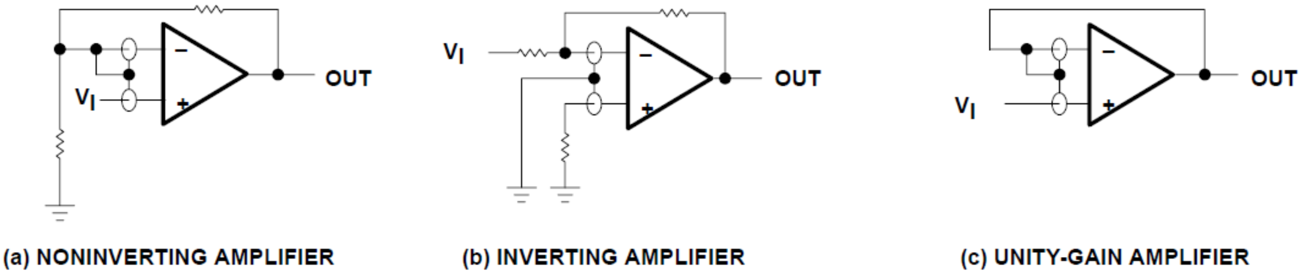
The use of the polysilicon-gate process and the careful input circuit design gives the TLC272 and TLC277 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1µV/month,including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC272 and TLC277 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. Including guard rings around inputs (similar to those of Figure 5-4 in the Section 5 section) is good practice. These guards must be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 6-4).

Connect unused amplifiers as grounded unity-gain followers to avoid possible oscillation.

6.1.3 Noise Performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC272 and TLC277 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 6-4. Guard-Ring Schemes

7 Device and Documentation Support

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (February 2002) to Revision F (January 2026) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Deleted TLC272Y throughout the document.. 1
- Deleted input offset voltage drift bullet from the *Features* 1
- Deleted trimmed offset voltage bullet from the *Features* 1
- Changed low noise typical from 25nV/√Hz to 10.8nV/√Hz in the *Features* 1
- Deleted references to LinCMOS throughout the document...1
- Deleted the *Available Options* table in the *Description* 1
- Deleted Equivalent Schematic figure from the document...1
- Added the *Pin Configuration and Functions* section...3
- Deleted FK package pinout details from the document...3
- Deleted all tables in the *Specifications* related to TLC272M and TLC272Y... 4
- Deleted M-suffix and FK package related information in the *Absolute Maximum Ratings* table............. 4
- Deleted the *Dissipation Ratings* table..4
- Deleted M suffix table column in the *Recommended Operating Conditions* table...................................4
- Changed Input offset Voltage for 272C typical from 1.1mV to 0.12mV in all of the *Electrical Characteristics* tables.. 5
- Changed Input offset Voltage for 272AC typical from 0.9mV to 0.12mV in all of the *Electrical Characteristics* tables.. 5
- Changed Input offset Voltage for 272BC typical from 230µV to 0.12mV in all of the *Electrical Characteristics* tables.. 5
- Changed Input offset Voltage for 277C typical from 200µV to 0.12mV in all of the *Electrical Characteristics* tables.. 5

- Changed Temperature coefficient of input offset voltage from 1.8μV/°C to 0.3μV/°C in all of the *Electrical Characteristics* tables.......... 5
- Changed Input offset current from 0.1pA to 10pA in all of the *Electrical Characteristics* tables.......... 5
- Changed Input bias current from 0.6pA to 10pA in all of the *Electrical Characteristics* tables.......... 5
- Changed Common-mode input voltage range at 25°C and full range from –0.2V to –0.1V in all of the *Electrical Characteristics* tables.......... 5
- Changed High-level output voltage at 5V, 25°C, 0°C and 70°C from 3.8V to 4.95V in all of the *Electrical Characteristics* tables.......... 5
- Changed Large-signal differential voltage amplification at 25°C from 23V/mV to 1000V/mV in all of the *Electrical Characteristics* tables.......... 5
- Deleted large-signal differential voltage amplification at 0°C and 70°C in all of the *Electrical Characteristics* tables.......... 5
- Deleted common-mode rejection ratio at 0°C and 70°C in all of the *Electrical Characteristics* tables.......... 5
- Changed supply-voltage rejection ratio at 25°C from 95dB to 120dB in all of the *Electrical Characteristics* tables.......... 5
- Deleted Supply-voltage rejection ratio at 0°C and 70°C in all of the *Electrical Characteristics* tables.......... 5
- Deleted Supply current (two amplifiers) at 25°C from 1.4mA to 1.12mA in all of the *Electrical Characteristics* tables.......... 5
- Deleted Supply current (two amplifiers) at 0°C and 70°C in all of the *Electrical Characteristics* tables.......... 5
- Changed high-level output voltage at 10V, 25°C from 8.5V to 9.95V in the 10V *Electrical Characteristics* table. 6
- Deleted high-level output voltage at 10V, 0°C and 70°C in the *Electrical Characteristics* table.......... 6
- Changed Equivalent input noise voltage from 25nV/√Hz to 10.8nV/√Hz in the *Operating Characteristics* table. 9
- Changed V_{IPP} from 1V to 100mV and 2.5V to 1V in the *Operating Characteristics* table.......... 9
- Changed Maximum output-swing bandwidth from 320kHz to 10kHz in the *Operating Characteristics* table.......... 9
- Changed Slew Rate at Unity gain typical at V_{IPP} 100mV from 3.6V/μs to 0.5V/μs and at 1V from 2.9V/μs to 21V/μs in the *Operating Characteristics* table.......... 9
- Changed Unity gain bandwidth typical from 1.7MHz to 4.5MHz in the *Operating Characteristics* table.......... 9
- Changed Phase Margin typical from 46° to 60° in the *Operating Characteristics* table.......... 9
- Deleted all values for –40°C and 85°C in the *Operating Characteristics* table.......... 9
- Added TLC272C, TLC272AC TLC272BC, TLC277C in the *Operating Characteristics* table.......... 9
- Updated the *Typical Characteristics* as per latest data.......... 10
- Deleted *Full Power Response* and *Test Time* sections.......... 14
- Deleted *Output Characteristics*, *Feedback*, *Electrostatic Discharge*, and *Latch-up* sections.......... 17

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9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC272ACD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	272AC
TLC272ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	272AC
TLC272ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	272AC
TLC272ACP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC272ACP
TLC272ACP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC272ACP
TLC272ACPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TLC272AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	272AI
TLC272AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272AI
TLC272AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272AI
TLC272AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272AI
TLC272AIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272AI
TLC272AIP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC272AIP
TLC272AIP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC272AIP
TLC272BCD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	272BC
TLC272BCDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	272BC
TLC272BCDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	272BC
TLC272BCP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC272BCP
TLC272BCP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC272BCP
TLC272BCPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TLC272BCPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272B
TLC272BCPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272B
TLC272BID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	272BI
TLC272BIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272BI
TLC272BIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272BI
TLC272BIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272BI
TLC272BIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272BI
TLC272BIP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC272BIP
TLC272BIP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC272BIP
TLC272CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	272C

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC272CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	272C
TLC272CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	272C
TLC272CDR1G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272C
TLC272CDR1G4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272C
TLC272CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	0 to 70	
TLC272CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC272CP
TLC272CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC272CP
TLC272CPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TLC272CPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272
TLC272CPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272
TLC272CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272
TLC272CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272
TLC272CPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272C
TLC272CPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272C
TLC272ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	272I
TLC272IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272I
TLC272IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272I
TLC272IDR1G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272I
TLC272IDR1G4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272I
TLC272IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLC272IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC272IP
TLC272IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC272IP
TLC272IPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	-40 to 85	
TLC277CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	277C
TLC277CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	277C
TLC277CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	277C
TLC277CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC277CP
TLC277CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC277CP
TLC277CPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P277
TLC277CPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P277
TLC277CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P277

PACKAGE OPTION ADDENDUM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC277CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P277
TLC277ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	277I
TLC277IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	277I
TLC277IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	277I
TLC277IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	277I
TLC277IDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	277I
TLC277IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC277IP
TLC277IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC277IP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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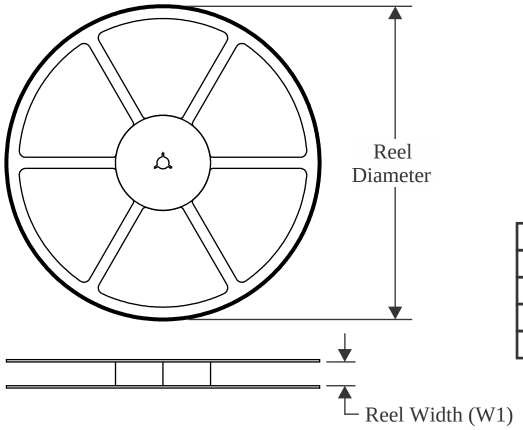
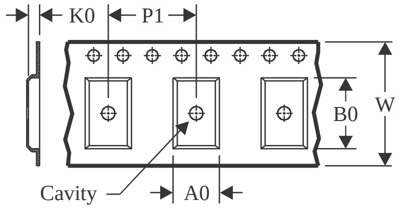
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

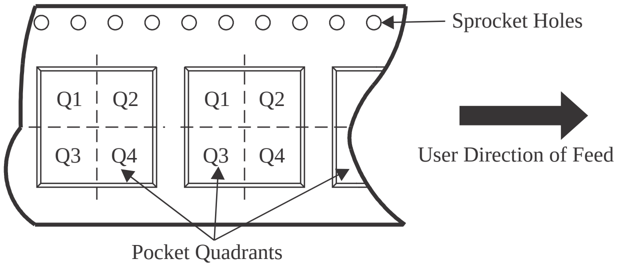


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

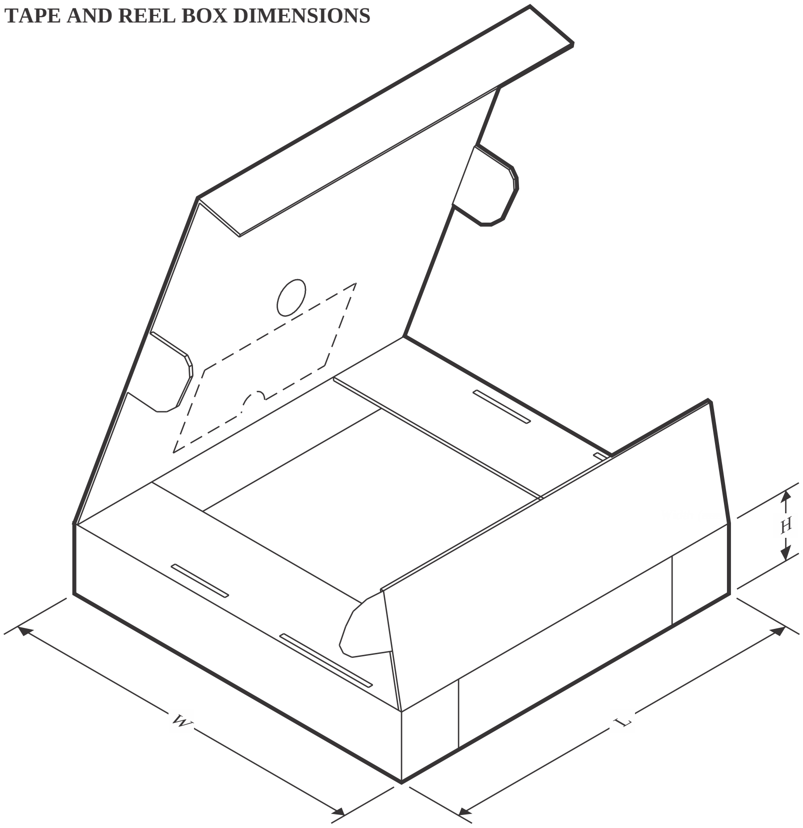
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC272ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272BIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272CDR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TLC272CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC272IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272IDR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC277CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC277CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TLC277IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC277IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

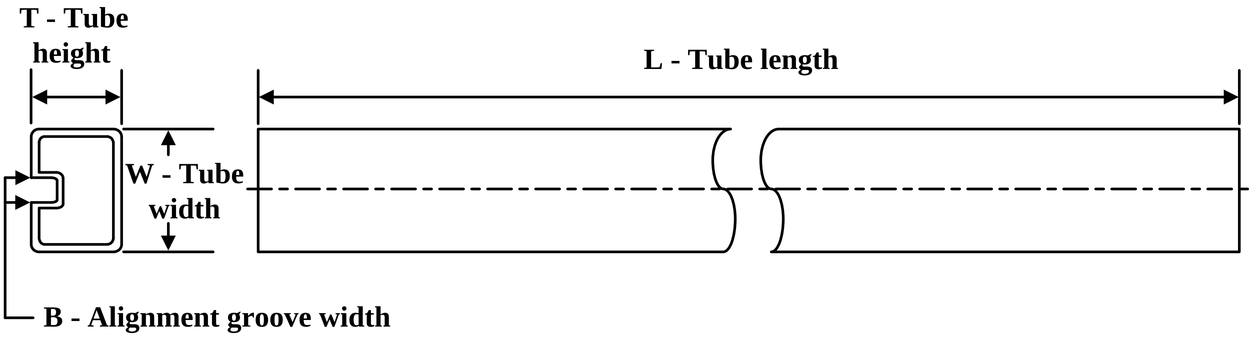
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

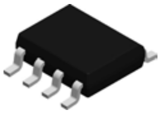
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC272ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLC272BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC272BIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272BIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLC272CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272CDR1G4	SOIC	D	8	2500	353.0	353.0	32.0
TLC272CPSR	SO	PS	8	2000	353.0	353.0	32.0
TLC272CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC272IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272IDR1G4	SOIC	D	8	2500	353.0	353.0	32.0
TLC277CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC277CPSR	SO	PS	8	2000	353.0	353.0	32.0
TLC277IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC277IDRG4	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



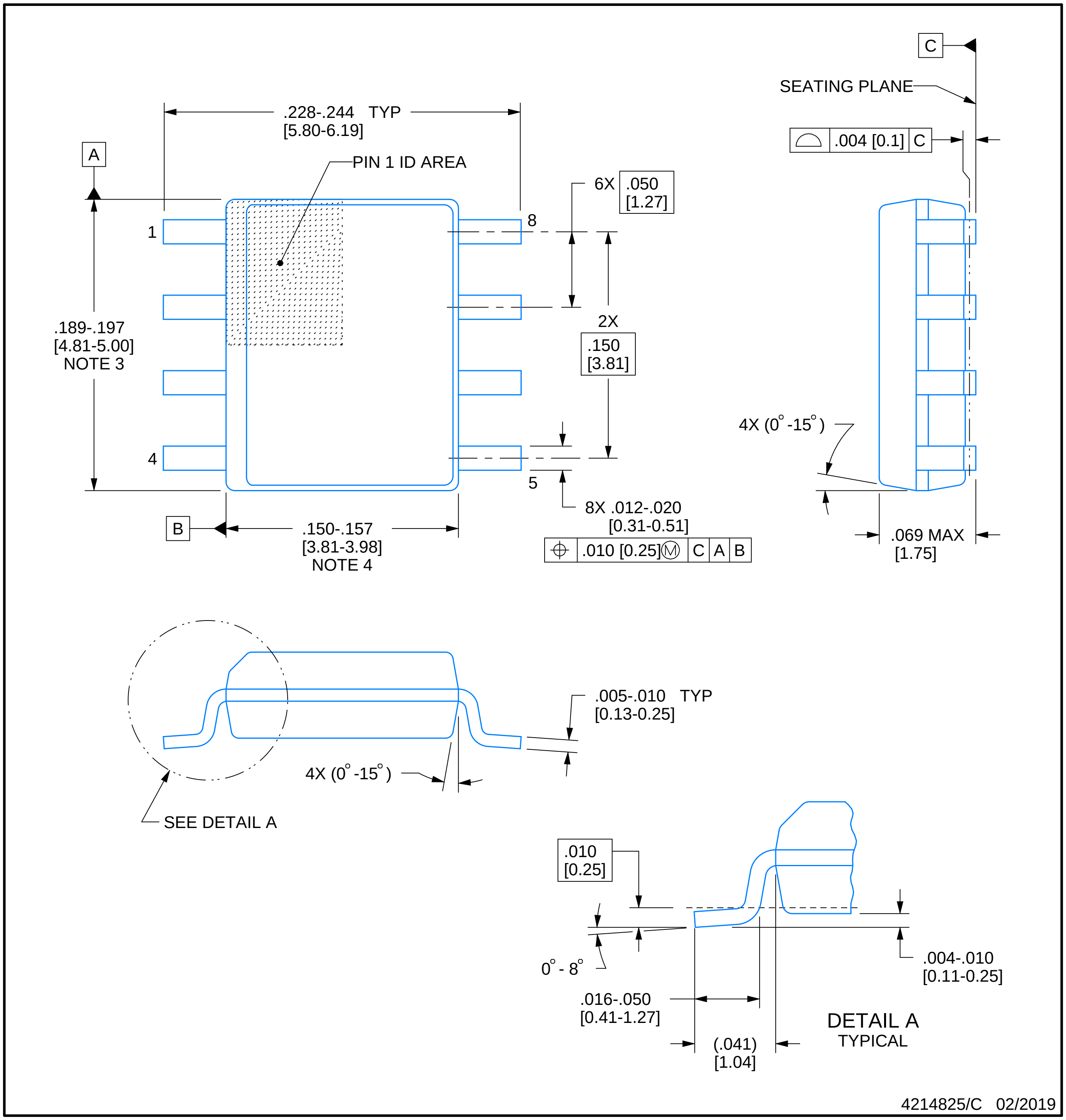
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC272ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLC272ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC272AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC272AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC272BCP	P	PDIP	8	50	506	13.97	11230	4.32
TLC272BCP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC272BCPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC272BCPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC272BIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC272BIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC272CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC272CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC272CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC272CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC272IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC272IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC277CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC277CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC277CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC277CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC277IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC277IP.A	P	PDIP	8	50	506	13.97	11230	4.32



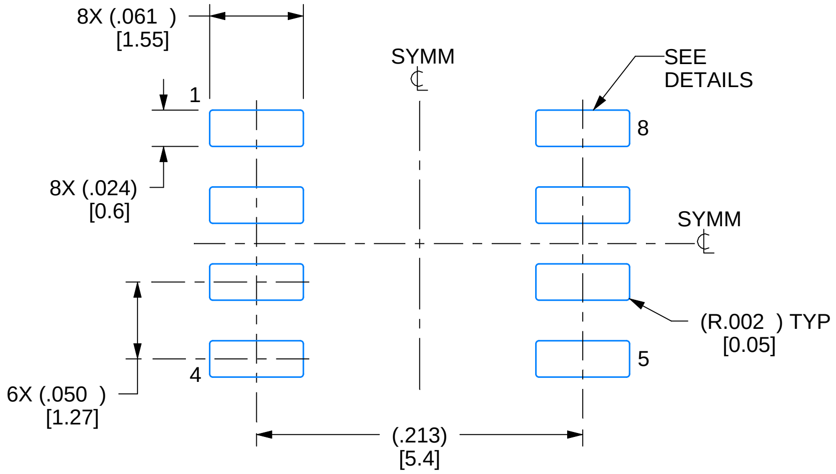
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

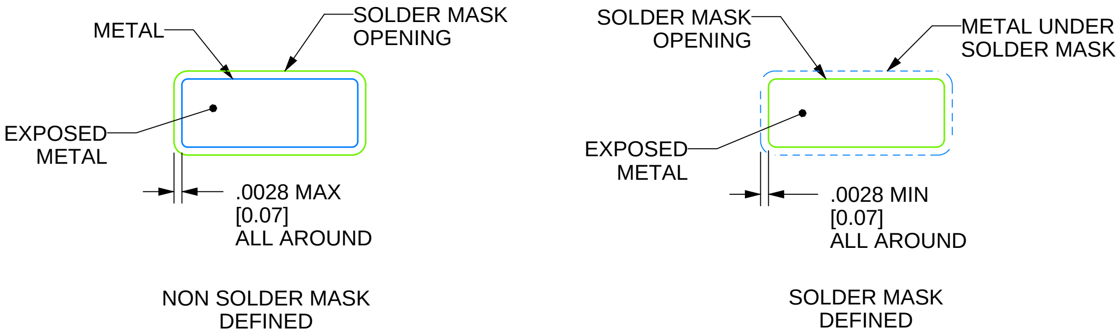


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



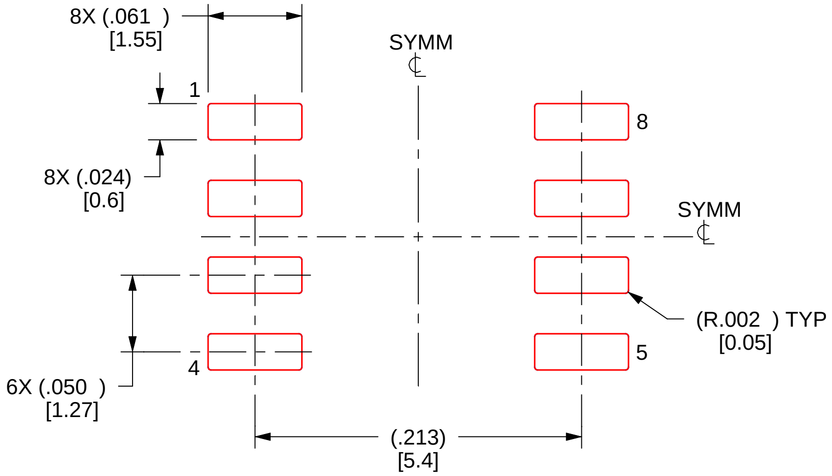
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

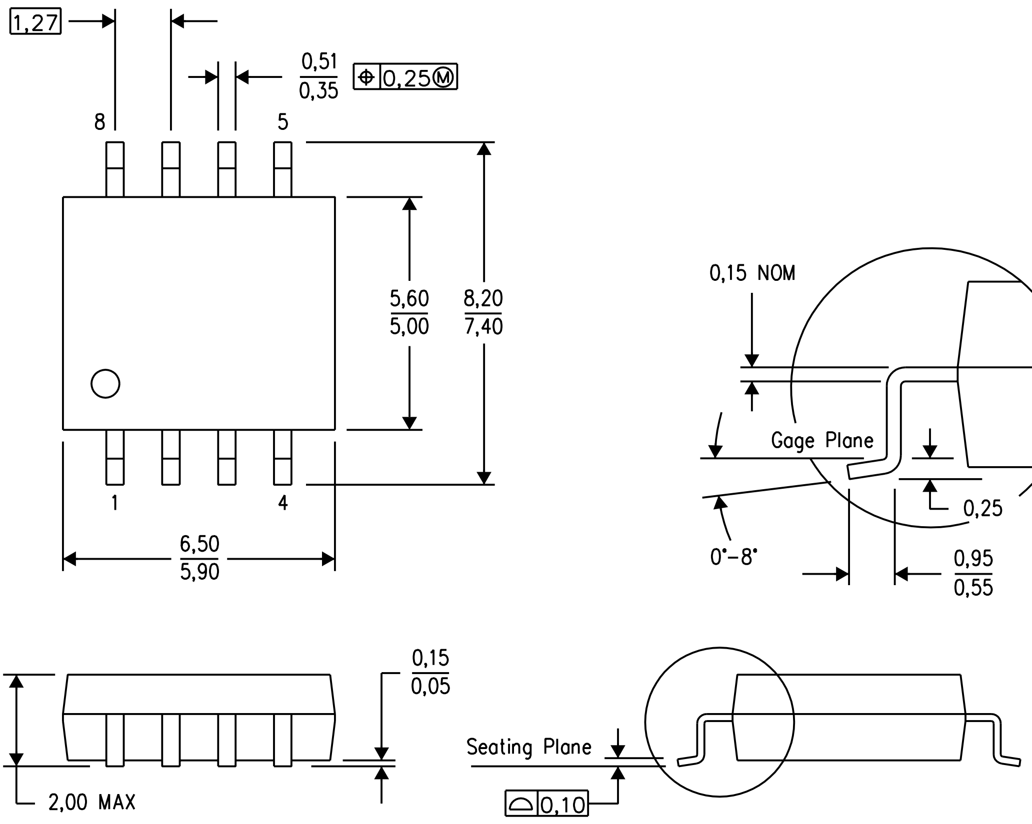


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

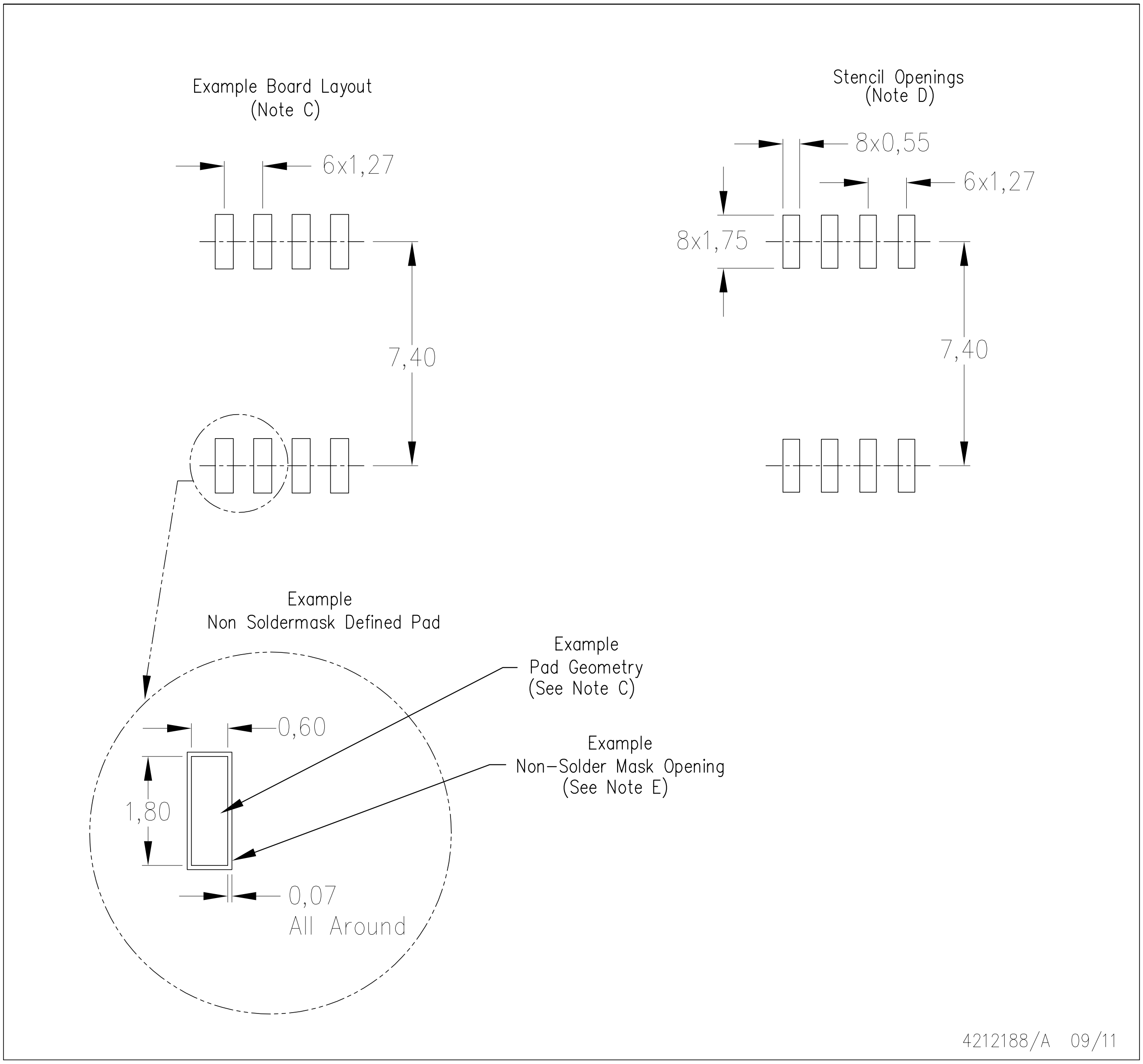
PS (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



4040063/C 03/03

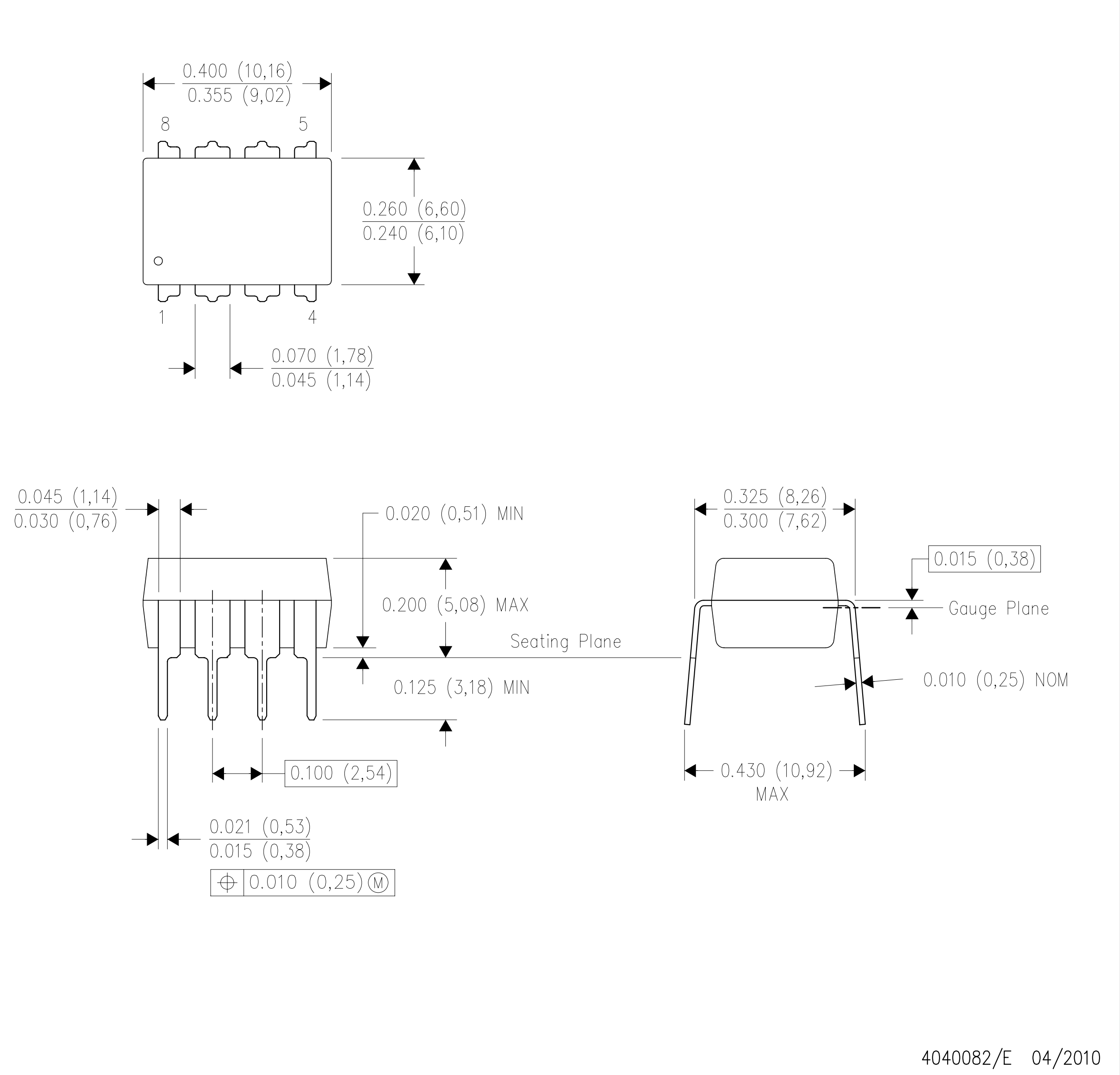
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8) PLASTIC SMALL OUTLINE

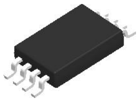


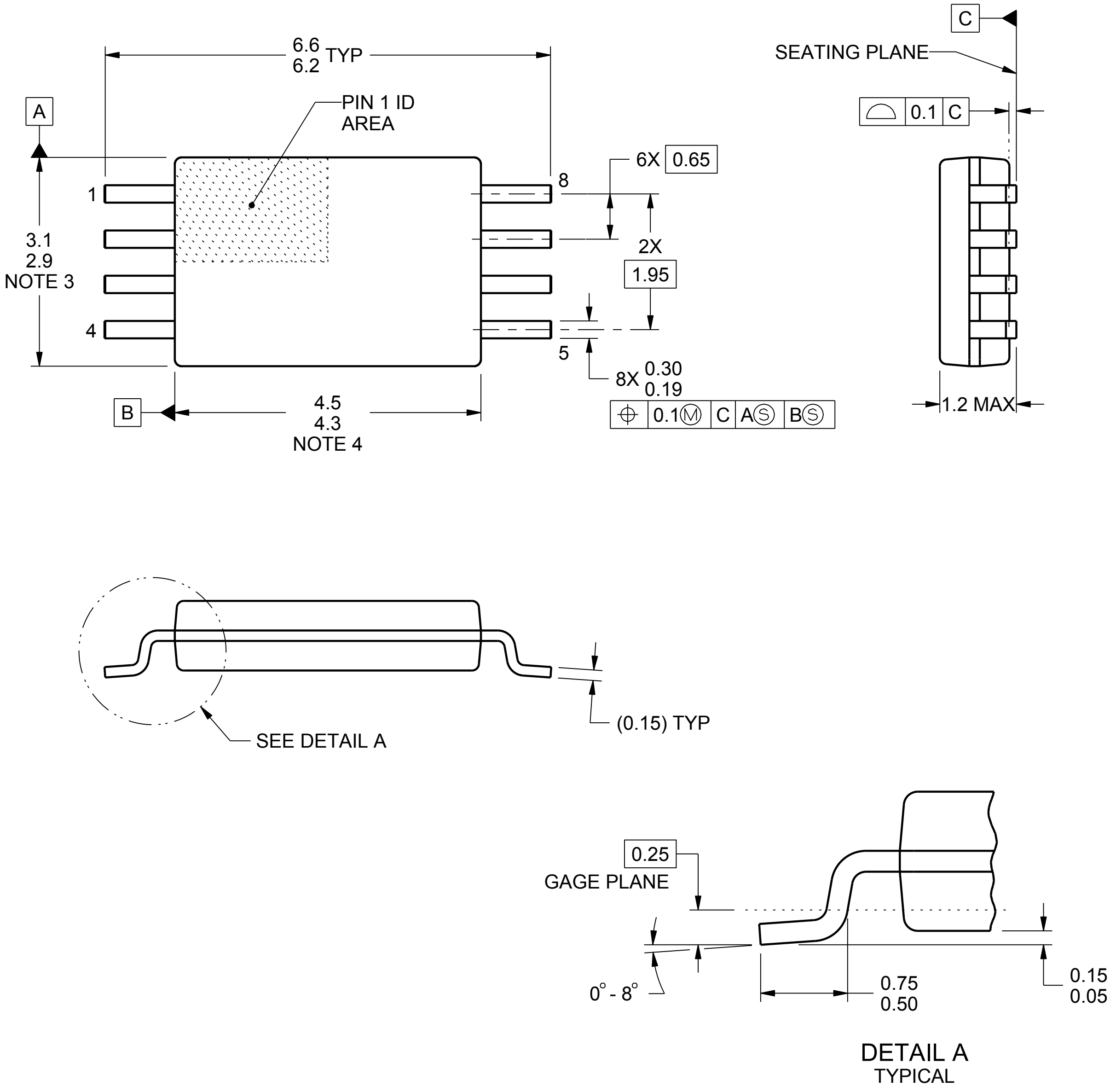
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

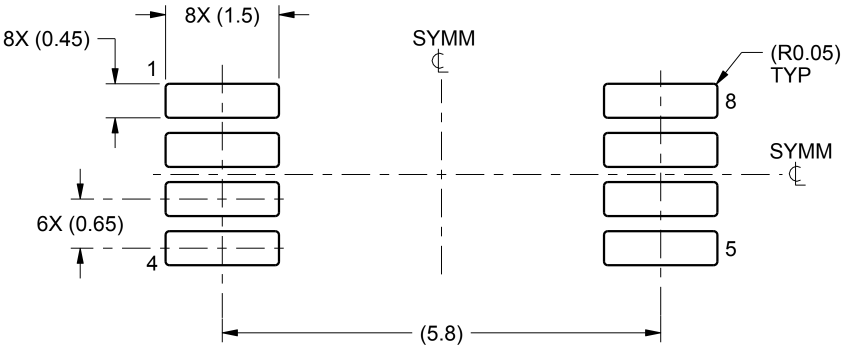




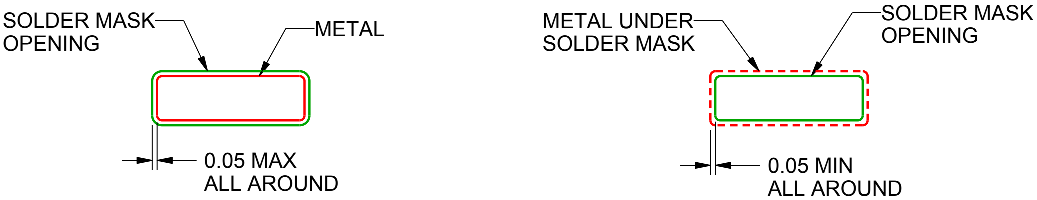
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

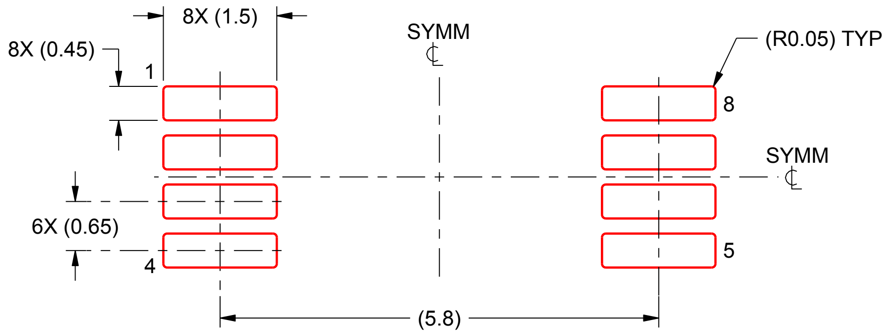
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025