

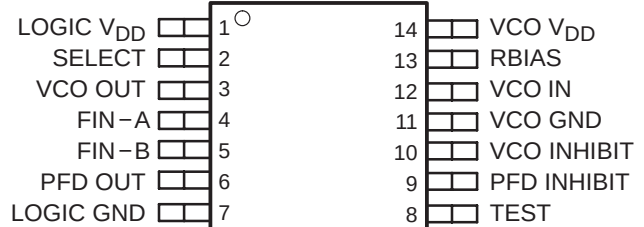
TLC2932A HIGH PERFORMANCE PHASE LOCKED LOOP

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- **VCO (Voltage-Controlled Oscillator):**
 - Complete Oscillator Using Only One External Bias Resistor (RBIAS)
 - Lock Frequency:
 - 13 MHz to 32 MHz (VDD = 3 V $\pm$ 5%,
T_A = –20°C to 75°C, x1 Output)
 - 13 MHz to 35 MHz (VDD = 3.3 V $\pm$ 5%,
T_A = –20°C to 75°C, x1 Output)
 - 15 MHz to 55 MHz (VDD = 5 V $\pm$ 5%,
T_A = –20°C to 75°C, x1 Output)
 - Selectable Output Frequency
- **PFD (Phase Frequency Detector):**
High Speed, Edge-Triggered Detector with Internal Charge Pump

- Independent VCO, PFD Power-Down Mode
- Thin Small-Outline Package (14 Terminal)
- CMOS Technology
- Pin Compatible TLC2932IPW

14-PIN TSOP (PW PACKAGE)
(TOP VIEW)



description

The TLC2932A is designed for phase-locked loop (PLL) systems and is composed of a voltage-controlled oscillator (VCO) and an edge-triggered type phase frequency detector (PFD). The oscillation frequency range of the VCO is set by an external bias resistor (R_{BIA}S). The VCO has a 1/2 frequency divider at the output stage. The high speed PFD with internal charge pump detects the phase difference between the reference frequency input and signal frequency input from the external counter. Both the VCO and the PFD have inhibit functions, which can be used as power-down mode. Due to the TLC2932A high speed and stable oscillation capability, the TLC2932A is suitable for use as a high-performance PLL.

AVAILABLE OPTIONS

T _A	PACKAGE
	SMALL OUTLINE (PW)
–20°C to 75°C	TLC2932AIPW



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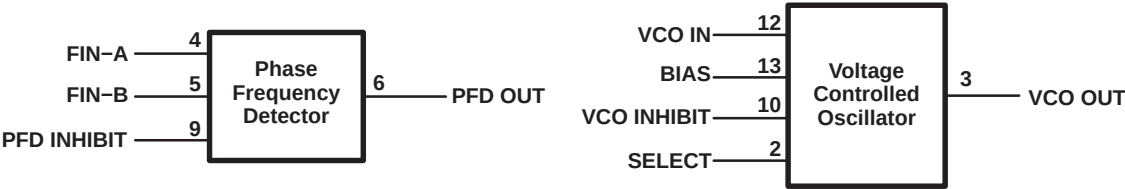
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functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
LOGIC VDD	1		Power supply for the internal logic. This power supply should be separated from VCO V _{DD} to reduce cross-coupling between supplies.
SELECT	2	I	VCO output frequency select. When SELECT is high, the VCO output frequency is $\times 1/2$ and when low. The output frequency is $\times 1$.
VCO OUT	3	O	VCO output. When the VCO INHIBIT is high, VCO output is low.
FIN-A	4	I	Input reference frequency $f_{(REF IN)}$ is applied to FIN-A.
FIN-B	5	I	Input for VCO external counter output frequency $f_{(FIN-B)}$. FIN-B is nominally provided from the external counter.
PFD OUT	6	O	PFD output. When the PFD INHIBIT is high, PFD output is in the high-impedance state.
LOGIC GND	7		GND for the internal logic.
TEST	8		Connect to GND.
PFD INHIBIT	9	I	PFD inhibit control. When PFD INHIBIT is high, PFD output is in the high-impedance state.
VCO INHIBIT	10	I	VCO inhibit control. When VCO INHIBIT is high, VCO output is low.
VCO GND	11		GND for VCO.
VCO IN	12	I	VCO control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.
RBIAS	13	I	Bias supply. An external resistor (R _{BIAS}) between VCO V _{DD} and R _{BIAS} supplies bias for adjusting the oscillation frequency range.
VCO V _{DD}	14		Power supply for VCO. This power supply should be separated from LOGIC V _{DD} to reduce cross-coupling between supplies.

detailed description

VCO oscillation frequency

The VCO oscillation frequency is determined by an external register (R_{BIAS}) connected between the VCO V_{DD} and the BIAS terminals. The oscillation frequency and range depends on this resistor value. For the lock frequency range refer to the recommended operating conditions. Figure 1 shows the typical frequency variation and VCO control voltage.

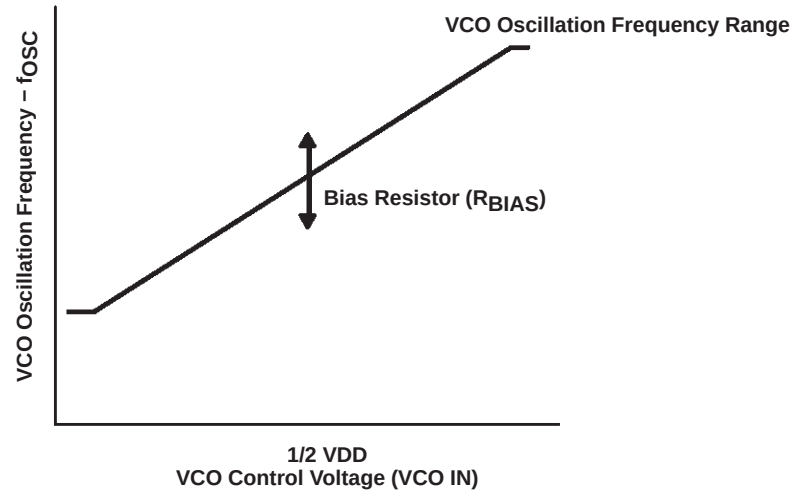


Figure 1. Oscillation Frequency

VCO output frequency 1/2 divider

The TLC2932A SELECT terminal sets the f_{OSC} VCO output frequency as shown in Table 1. The $1/2 f_{OSC}$ output should be used for minimum VCO output jitter.

Table 1. VCO Output 1/2 Divider Function

SELECT	VCO OUTPUT
Low	f_{OSC}
High	$1/2 f_{OSC}$

VCO inhibit function

The VCO has an externally controlled inhibit function which inhibit the VCO output. A high level on the VCO INHIBIT terminal stops the VCO oscillation and powers down the VCO. The output maintains a low level during the power-down mode as shown in Table 2.

Table 2. VCO Inhibit Function

VCO INHIBIT	VCO OSCILLATOR	VCO OUT	$I_{DD}(VCO)$
Low	Active	Active	Normal
High	Stopped	Low level	Power Down

PFD operation

The PFD is a high-speed, edge-triggered detector with an internal charge pump. The PFD detects the phase difference between two frequency inputs supplied to FIN-A and FIN-B as shown in Figure 2. Normally the reference is supplied to FIN-A and the frequency from the external counter output is fed to FIN-B. For clock recovery PLL system, other types of phase detectors should be used.

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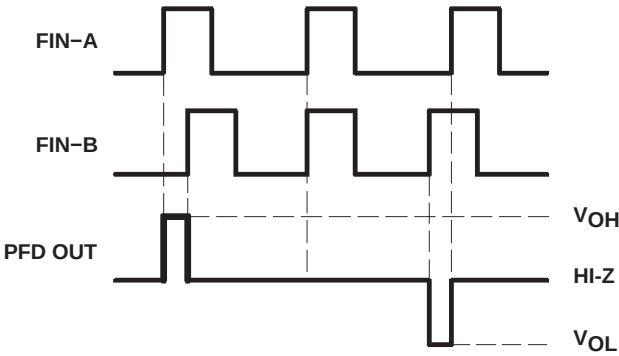


Figure 2. PFD Function Timing Chart

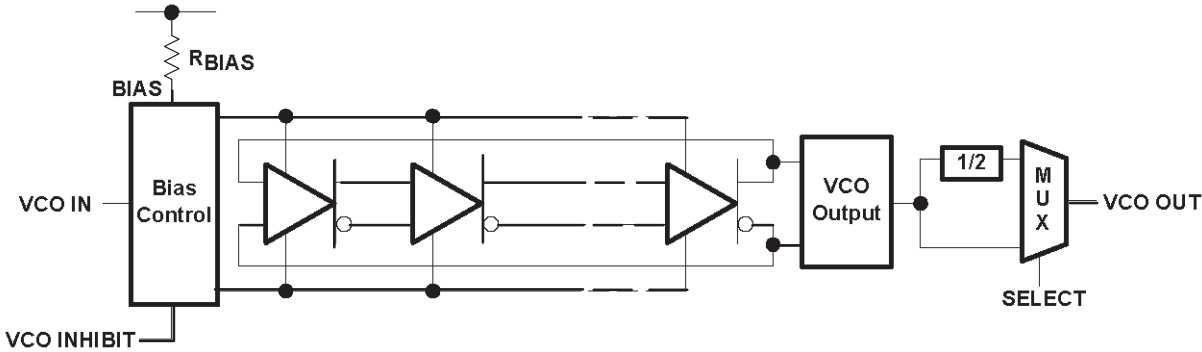
PFD inhibit control

A high level on the PFD INHIBIT terminal places PFD OUT in the high-impedance state and the PFD stops phase detection as shown in Table 3. A high level on the PFD INHIBIT terminal can also be used as the power-down mode for the PFD.

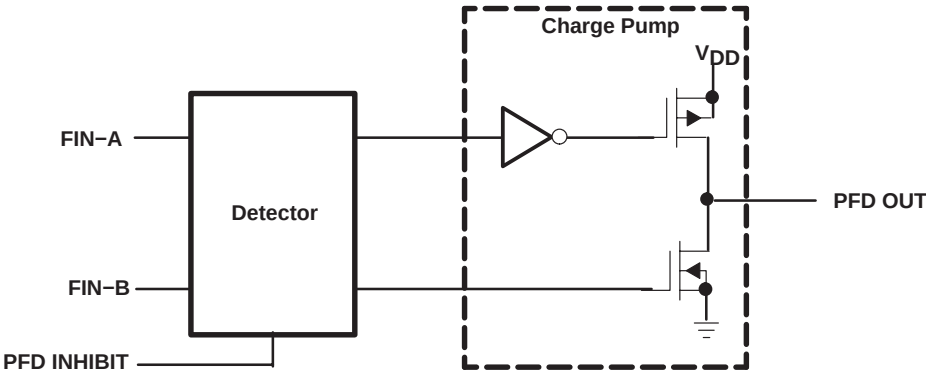
Table 3. VCO Output Control Function

PFD INHIBIT	DETECTION	PFD OUT	I _{DD} (PFD)
Low	Active	Active	Normal
High	Stopped	Hi-Z	Power Down

VCO block schematic



PFD block schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage (each supply), V_{DD} (see Note 1)	7 V
Input voltage range (each input), V_{IN} (see Note 1)	-0.5 V to $V_{DD} + 0.5$ V
Input current (each input), I_{IN}	±20 mA
Output current (each output), I_O	±20 mA
Operating free-air temperature range, T_A	-20°C to 75°C
Storage temperature range, T_{Stg}	-65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 5.6 mW/°C.

recommended operating conditions

PARAMETERS		MIN	TYP	MAX	UNIT
Supply voltage (each supply, see Note 3)	$V_{DD} = 3$ V	2.85	3	3.15	V
	$V_{DD} = 3.3$ V	3.135	3.3	3.465	
	$V_{DD} = 5$ V	4.75	5	5.25	
Input voltage, (inputs except VCO IN)		0		V_{DD}	V
Output current, (each output)		0		±2	mA
VCO control voltage at VCO IN		0.9		V_{DD}	V
Lock frequency	$V_{DD} = 3$ V	13		32	MHz
	$V_{DD} = 3.3$ V	13		35	
	$V_{DD} = 5$ V	15		55	
Bias Resistor	$V_{DD} = 3$ V	2.2		5.1	kΩ
	$V_{DD} = 3.3$ V	2.2		5.1	
	$V_{DD} = 5$ V	2.2		5.1	

NOTE 3: It is recommended that the logic supply terminal (LOGIC V_{DD}) and the VCO supply terminal (VCO V_{DD}) should be at the same voltage and separated from each other.

electrical characteristics, $V_{DD} = 3$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

VCO section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High level output voltage	$I_{OH} = -2$ mA	2.4			V
V_{OL} Low level output voltage	$I_{OL} = 2$ mA			0.3	V
V_{TH} Input threshold voltage at select, VCO inhibit		0.9	1.5	2.1	V
I_I Input current at Select, VCO inhibit	$V_I = V_{DD}$ or GND			±1	μA
$Z_I(V_{CON})$ VCO IN input impedance	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD}(INH)$ VCO supply current (inhibit)	See Note 4		0.35	1	μA
$I_{DD}(VCO)$ VCO supply current	See Note 5		8.4	17	mA

- NOTES: 4. Current into VCO V_{DD} , when VCO INHIBIT = high, PFD is inhibited.
5. Current into VCO V_{DD} , when VCO IN = 1/2 V_{DD} , $R_{BIAS} = 3.3$ kΩ, VCOOUT = 15-pF Load, VCO INHIBIT = GND, and PFD INHIBIT = GND.

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electrical characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted) (continued)

PFD section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	$I_{OH} = -2\text{ mA}$	2.4		V
V_{OL}	Low level output voltage	$I_{OL} = 2\text{ mA}$		0.3	V
I_{OZ}	High impedance state output current	PFD inhibit = high, $V_O = V_{DD}$ or GND		± 1	μA
V_{IH}	High level input voltage at Fin-A, Fin-B		2.1		V
V_{IL}	Low level input voltage at Fin-A, Fin-B			0.5	V
V_{TH}	Input threshold voltage at PFD inhibit		0.9	1.5	2.1
C_{IN}	Input capacitance at Fin-A, Fin-B		5.6		pF
Z_{IN}	Input impedance at Fin-A, Fin-B		10		M Ω
$I_{DD(Z)}$	High impedance state PFD supply current	See Note 6		1	μA
$I_{DD(PFD)}$	PFD supply current	See Note 7		3	mA

NOTES: 6. The current into LOGIC V_{DD} when FIN-A and FIN-B = ground, PFD INHIBIT = V_{DD} , PFD OUT open, and VCO OUT is inhibited.
7. The current into LOGIC V_{DD} when FIN-A = 1 MHz and FIN-B = 1 MHz ($V_{I(PP)} = 3\text{ V}$, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.

operation characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

VCO section

Parameter	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Operation oscillation frequency	$R_{BIAS} = 3.3\text{ k}\Omega$, VCO IN = $1/2 V_{DD}$	17	25	33
t_{STB}	Time to stable oscillation (see Note 8)			10	μs
t_r	Rise time	$C_L = 15\text{ pF}$	9	14	ns
t_f	Fall time	$C_L = 15\text{ pF}$	7.6	12	ns
	Duty cycle at VCO OUT	$R_{BIAS} = 3.3\text{ k}\Omega$, VCO IN = $1/2 V_{DD}$	45%	50%	55%
$\alpha (f_{OSC})$	Temperature coefficient of oscillation frequency	VCO IN = $1/2 V_{DD}$, $T_A = -20^\circ\text{C}$ to 75°C	-0.264		$\%/^\circ\text{C}$
k_{SVS} (f_{osc})	Supply voltage coefficient of oscillation frequency	VCO IN = $1/2 V_{DD}$, $V_{DD} = 4.75\text{ V}$ to 5.25 V	0.004		$\%/mV$
	Jitter absolute (see Note 9)	PLL jitter, N = 128	325		ps

NOTES: 8. The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully deigned PCB with no device socket.

PFD section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operation frequency	17			MH
t_{PLZ}	PFD output disable time from low level		22	50	ns
t_{PHZ}	PFD output disable time from high level		21	50	ns
t_{PZL}	PFD output enable time to low level		6.5	30	ns
t_{PZH}	PFD output enable time to high level		7	30	ns
t_r	Rise time	$C_L = 15\text{ pF}$	3.4	10	ns
t_f	Fall time	$C_L = 15\text{ pF}$	1.9	10	ns



electrical characteristics, $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

VCO section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	$I_{OH} = -2\text{ mA}$			V
V_{OL}	Low level output voltage	$I_{OL} = 2\text{ mA}$			V
V_{TH}	Input threshold voltage at select, VCO inhibit	1.05	1.65	2.25	V
I_I	Input current at Select, VCO inhibit	$V_I = V_{DD}$ or GND			μA
$Z_I(V_{CON})$	VCO IN input impedance	VCO IN = $1/2 V_{DD}$			$\text{M}\Omega$
$I_{DD}(INH)$	VCO supply current (inhibit)	See Note 10			μA
$I_{DD}(VCO)$	VCO supply current	See Note 11			mA

NOTES: 10. Current into VCO V_{DD} , when VCO INHIBIT = high, PFD is inhibited.

11. Current into VCO V_{DD} , when VCO IN = $1/2 V_{DD}$, $R_{BIAS} = 3.3\text{ k}\Omega$, $V_{COOUT} = 15\text{-pF}$ Load, VCO INHIBIT = GND, and PFD INHIBIT = GND.

PFD section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	$I_{OH} = -2\text{ mA}$			V
V_{OL}	Low level output voltage	$I_{OL} = 2\text{ mA}$			V
I_{OZ}	High impedance state output current	PFD inhibit = high, $V_O = V_{DD}$ or GND			μA
V_{IH}	High level input voltage at Fin-A, Fin-B	2.1			V
V_{IL}	Low level input voltage at Fin-A, Fin-B	0.5			V
V_{TH}	Input threshold voltage at PFD inhibit	1.05	1.65	2.25	
C_{IN}	Input capacitance at Fin-A, Fin-B	5.6			pF
Z_{IN}	Input impedance at Fin-A, Fin-B	10			$\text{M}\Omega$
$I_{DD}(Z)$	High impedance state PFD supply current	See Note 12			μA
$I_{DD}(PFD)$	PFD supply current	See Note 13			mA

NOTES: 12. The current into LOGIC V_{DD} when FIN-A and FIN-B = ground, PFD INHIBIT = V_{DD} , PFD OUT open, and VCO OUT is inhibited.

13. The current into LOGIC V_{DD} when FIN-A = 1 MHz and FIN-B = 1 MHz ($V_{I(pp)} = 3.3\text{ V}$, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.

operation characteristics, $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

VCO section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Operation oscillation frequency	$R_{BIAS} = 3.3\text{ k}\Omega$, VCO IN = $1/2 V_{DD}$			MHz
t_{stb}	Time to stable oscillation (see Note 14)	10			μs
t_r	Rise time	$C_L = 15\text{ pF}$			ns
t_f	Fall time	$C_L = 15\text{ pF}$			ns
f_{DUTY}	Duty cycle at VCO OUT	$R_{BIAS} = 3.3\text{ k}\Omega$, VCO IN = $1/2 V_{DD}$			%
$\alpha(f_{OSC})$	Temperature coefficient of oscillation frequency	VCO IN = $1/2 V_{DD}$, $T_A = -20^\circ\text{C}$ to 75°C			$\%/^\circ\text{C}$
$k_{SVS}(f_{OSC})$	Supply voltage coefficient of oscillation frequency	VCO IN = $1/2 V_{DD}$, $V_{DD} = 4.75\text{ V}$ to 5.25 V			$\%/m\text{ V}$
Jitter absolute (see Note 15)		PLL jitter, N = 128			ps

NOTES: 14. The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.

15. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully deigned PCB with no device socket.

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operation characteristics, $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted) (continued)

PFD section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operation frequency	22			MHz
t_{PLZ}	PFD output disable time from low level		21	50	ns
t_{PHZ}	PFD output disable time from high level		21	50	ns
t_{PZL}	PFD output enable time to low level		5.8	30	ns
t_{PZH}	PFD output enable time to high level		6.2	30	ns
t_r	Rise time	$C_L = 15\text{ pF}$	3	10	ns
t_f	Fall time	$C_L = 15\text{ pF}$	1.7	10	ns

electrical characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

VCO section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	$I_{OH} = -2\text{ mA}$	4		V
V_{OL}	Low level output voltage	$I_{OL} = 2\text{ mA}$		0.5	V
V_{TH}	Input threshold voltage at select, VCO inhibit	1.5	2.5	3.5	V
I_I	Input current at Select, VCO inhibit	$V_I = V_{DD}$ or GND		± 1	μA
$Z_I(\text{VCON})$	VCO IN input impedance	$V_{CO\text{ IN}} = 1/2 V_{DD}$	10		M Ω
$I_{DD}(\text{inh})$	VCO supply current (inhibit)	See Note 16	0.56	1	μA
$I_{DD}(\text{vco})$	VCO supply current	See Note 17	28	50	mA

NOTES: 16. Current into VCO V_{DD} , when VCO INHIBIT = high, PFD is inhibited.

17. Current into VCO V_{DD} , when VCO IN = $1/2 V_{DD}$, $R_{BIAS} = 3.3\text{ k}\Omega$, $V_{COOUT} = 15\text{-pF Load}$, VCO INHIBIT = GND, and PFD INHIBIT = GND.

PFD section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	$I_{OH} = -2\text{ mA}$	4.5		V
V_{OL}	Low level output voltage	$I_{OL} = 2\text{ mA}$		0.2	V
I_{OZ}	High impedance state output current	PFD inhibit = high, $V_O = V_{DD}$ or GND		± 1	μA
V_{IH}	High level input voltage at Fin-A, Fin-B	4.5			V
V_{IL}	Low level input voltage at Fin-A, Fin-B			1	V
V_{TH}	Input threshold voltage at PFD inhibit	1.5	2.5	3.5	
C_{IN}	Input capacitance at Fin-A, Fin-B		5.6		pF
Z_{IN}	Input impedance at Fin-A, Fin-B		10		M Ω
$I_{DD}(Z)$	High impedance state PFD supply current	See Note 18		1	μA
$I_{DD}(\text{PFD})$	PFD supply current	See Note 19	0.5	3	mA

NOTES: 18. The current into LOGIC V_{DD} when FIN-A and FIN-B = ground, PFD INHIBIT = V_{DD} , PFD OUT open, and VCO OUT is inhibited.

19. The current into LOGIC V_{DD} when FIN-A = 1 MHz and FIN-B = 1 MHz ($V_{I(\text{PP})} = 5\text{ V}$, rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited



operation characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OSC}	Operation oscillation frequency	R _{BIAS} = 3.3 kΩ, VCO IN = 1/2 V _{DD}	37	57	75	MHz
f _{STB}	Time to stable oscillation (see Note 20)				10	us
t _r	Rise time	C _L = 15 pF		7.5	10	ns
t _f	Fall time	C _L = 15 pF		6.4	10	ns
f _{DUTY}	Duty cycle at VCO OUT	R _{BIAS} = 3.3 kΩ, VCO IN = 1/2 V _{DD}	45%	50%	55%	
α (f _{OSC})	Temperature coefficient of oscillation frequency	VCO IN = 1/2 V _{DD} , T _A = −20°C to 75°C		−0.346		%/°C
k _{SVS} (f _{OSC})	Supply voltage coefficient of oscillation frequency	VCO IN = 1/2 V _{DD} , V _{DD} = 4.75 V to 5.25 V		0.002		%/mV
	Jitter absolute (see Note 21)	PLL jitter, N = 128		145		ps

NOTES: 20. The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.

21. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully deigned PCB with no device socket.

PFD section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operation frequency	38			MHz
t_{PLZ}	PFD output disable time from low level		20	40	ns
t_{PHZ}	PFD output disable time from high level		20	40	ns
t_{PZL}	PFD output enable time to low level		4	20	ns
t_{PZH}	PFD output enable time to high level		4.3	20	ns
t_r	Rise time	$C_L = 15\text{ pF}$	2.1	10	ns
t_f	Fall time	$C_L = 15\text{ pF}$	1.3	10	ns

PARAMETER MEASUREMENT INFORMATION

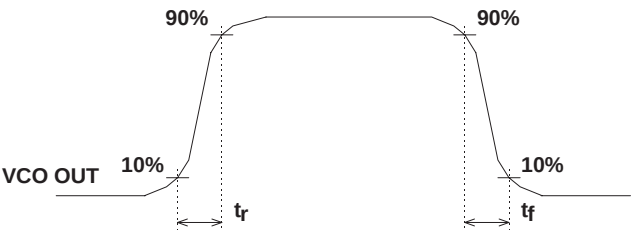


Figure 3. VCO Output Voltage Waveform

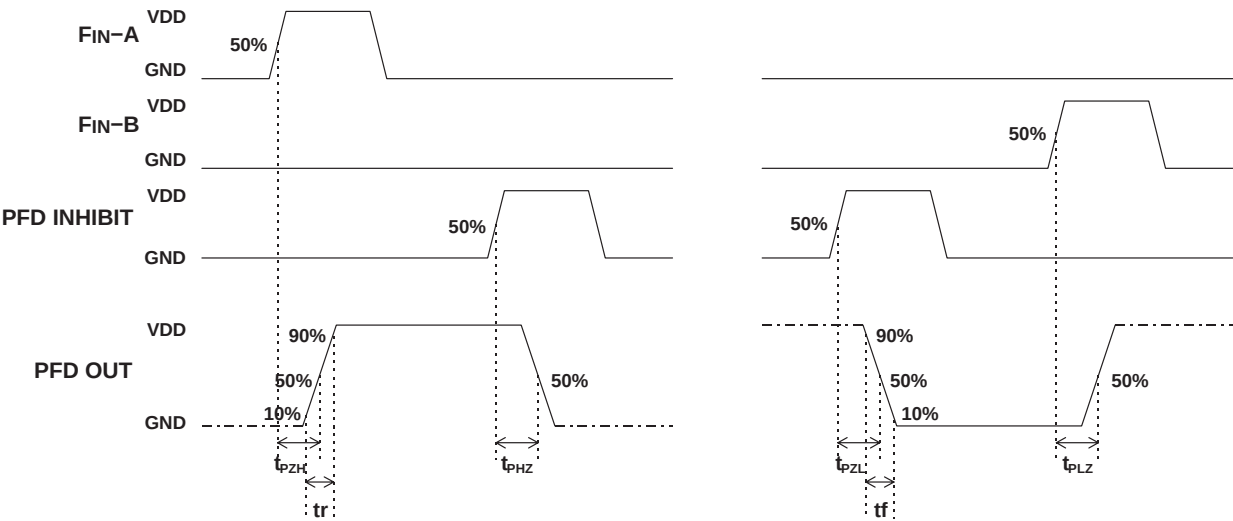


Figure 4. PFD Output Voltage Waveform

Table 4. PFD Output Test Conditions

PARAMETER	R_L	C_L	S1	S2
t_{pZH}	1 k Ω	15 pF	OPEN	CLOSE
t_{pHZ}				
t_r				
t_{pZL}			CLOSE	OPEN
t_{pLZ}				
t_f				

PARAMETER MEASUREMENT INFORMATION

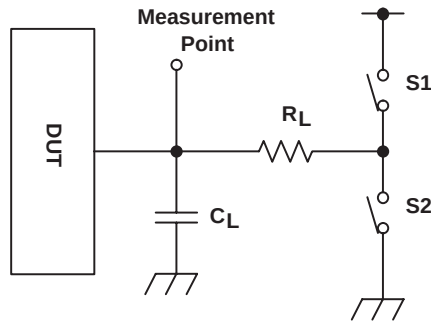


Figure 5. PFD Output Test Conditions

TYPICAL CHARACTERISTICS

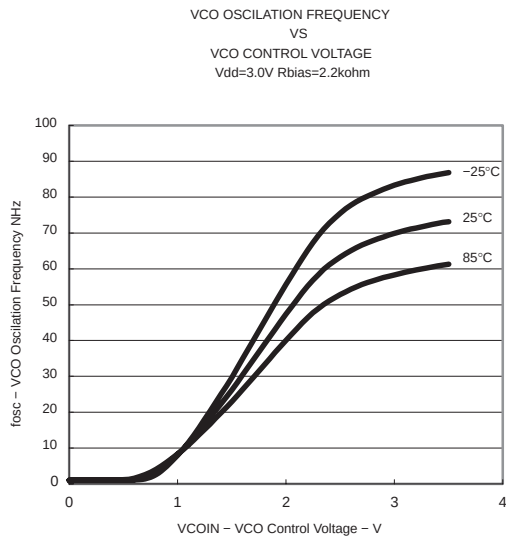


Figure 6.

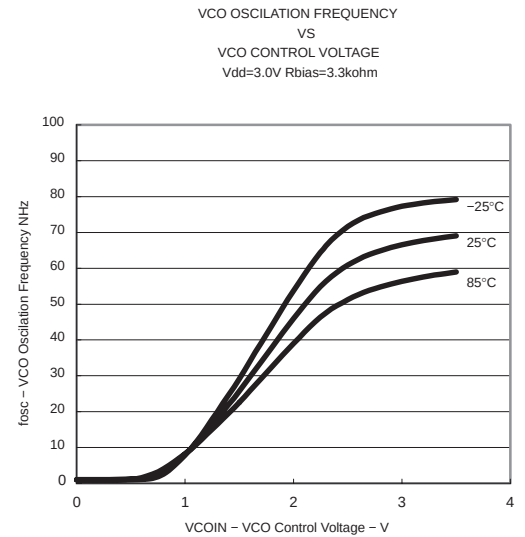


Figure 7.

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TYPICAL CHARACTERISTICS

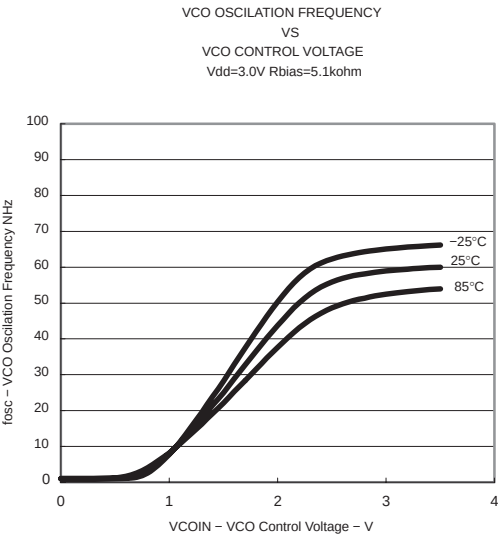


Figure 8.

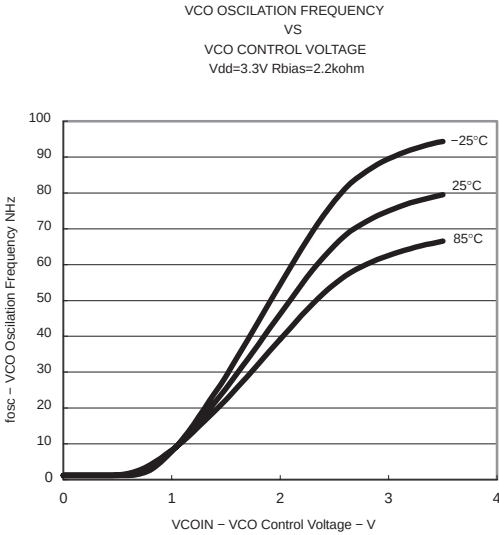


Figure 9.

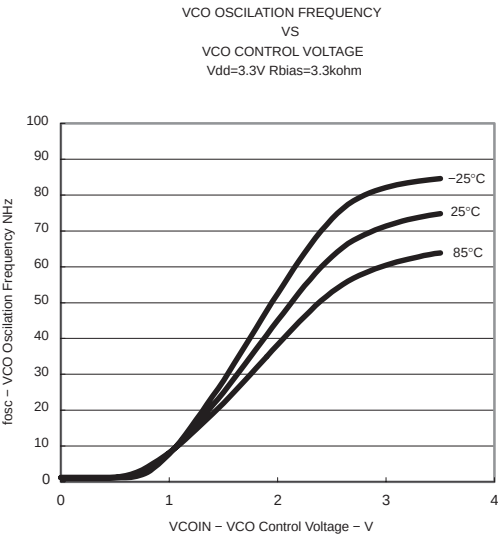


Figure 10.

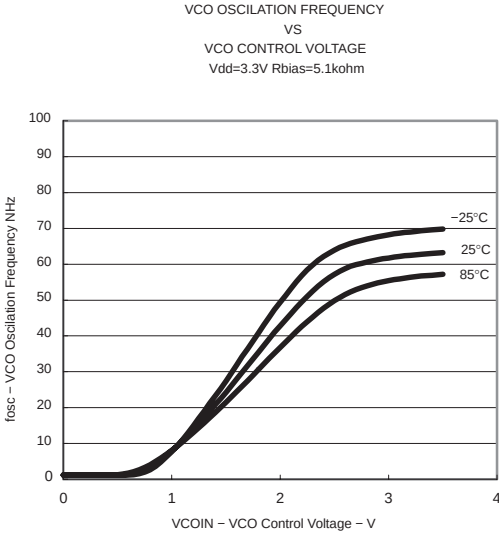


Figure 11.

TYPICAL CHARACTERISTICS

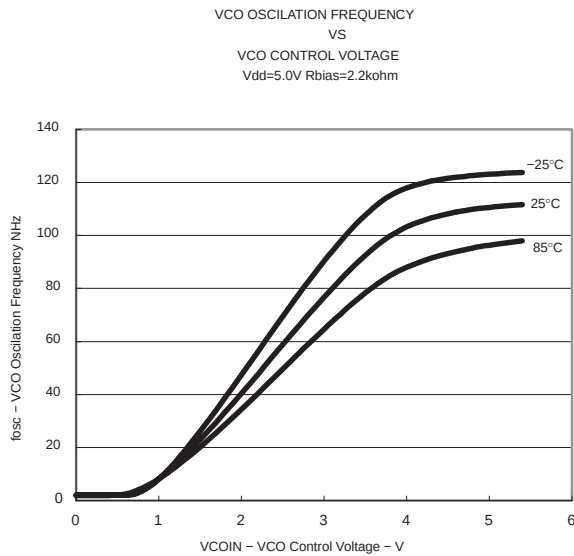


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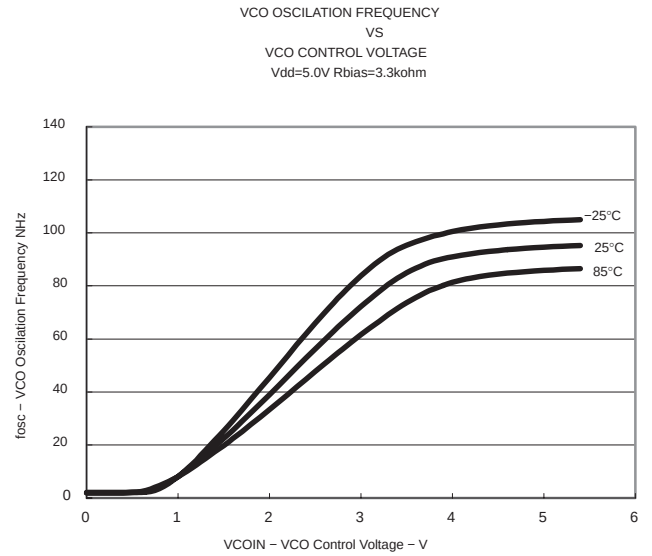


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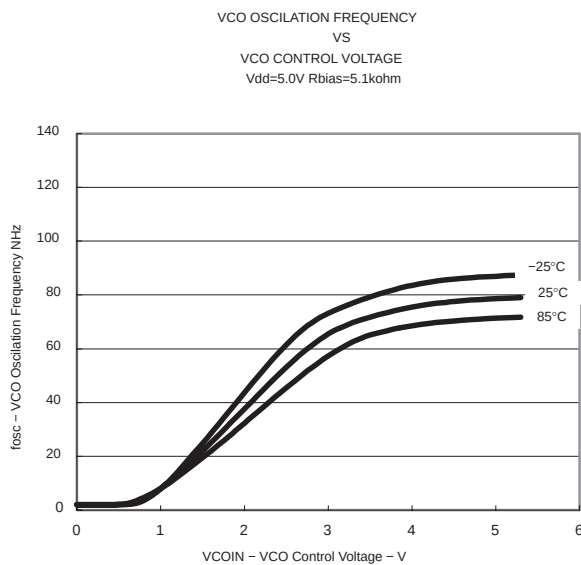


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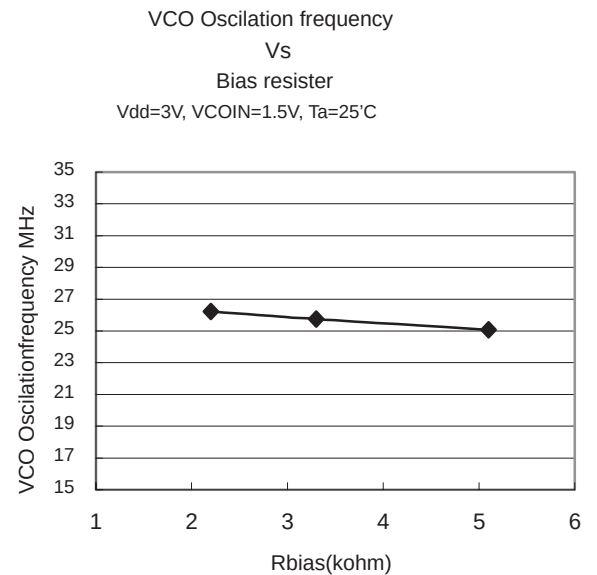


Figure 15.

TLC2932A
HIGH PERFORMANCE PHASE LOCKED LOOP

SLES150 – OCTOBER 2005

TYPICAL CHARACTERISTICS

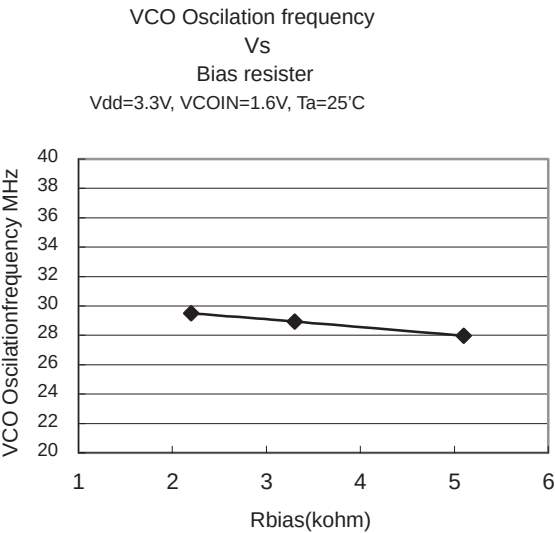


Figure 16.

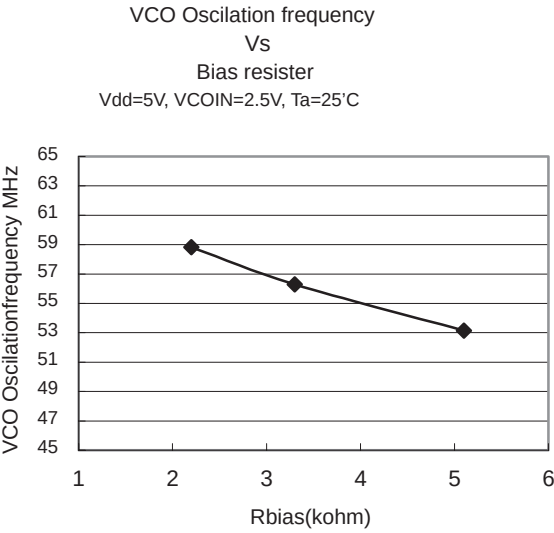


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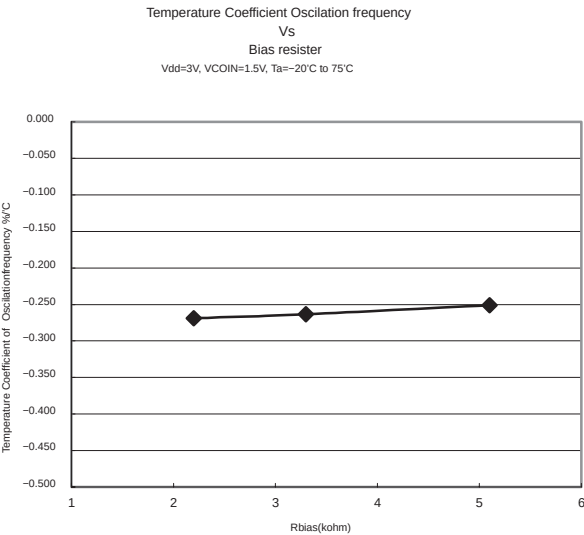


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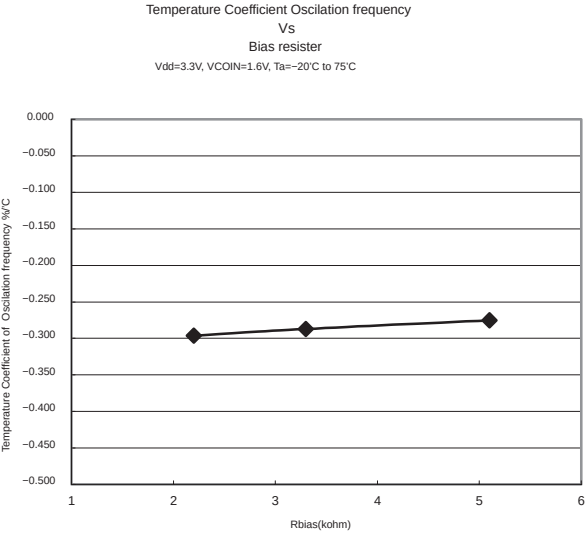


Figure 19.

TYPICAL CHARACTERISTICS

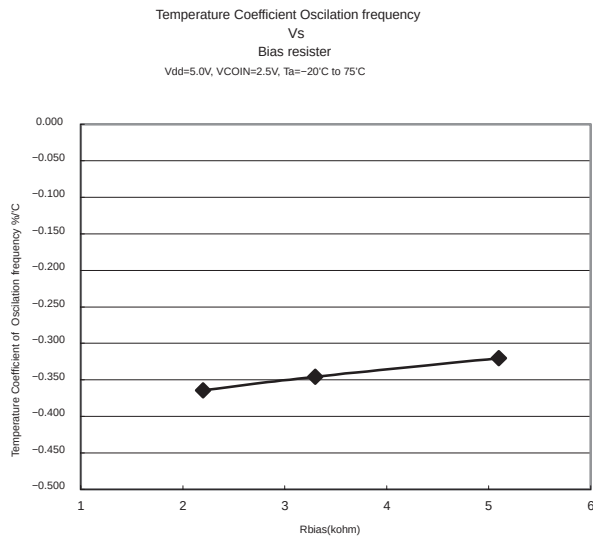


Figure 20.

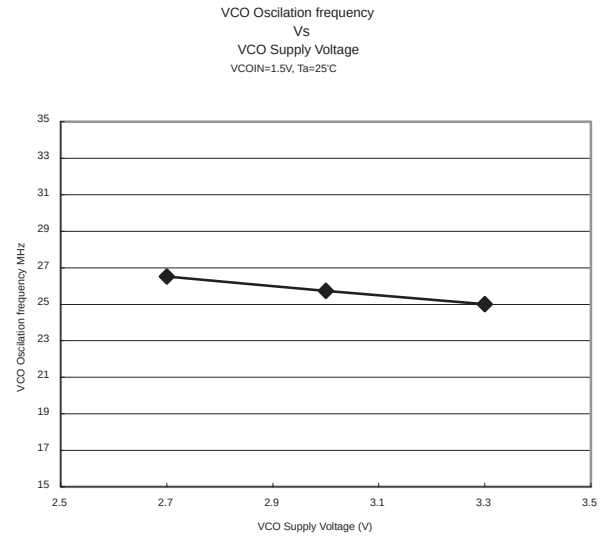


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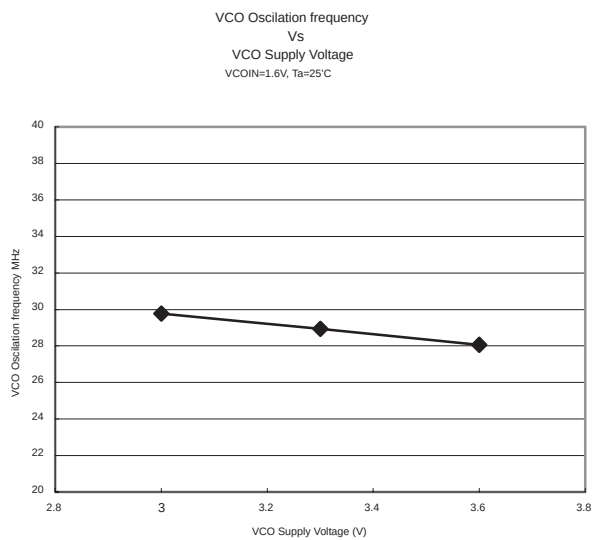


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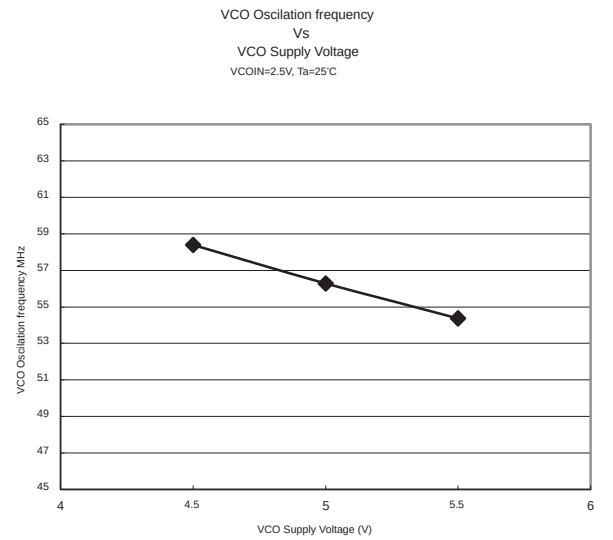


Figure 23.

TLC2932A

HIGH PERFORMANCE PHASE LOCKED LOOP

SLES150 – OCTOBER 2005

TYPICAL CHARACTERISTICS

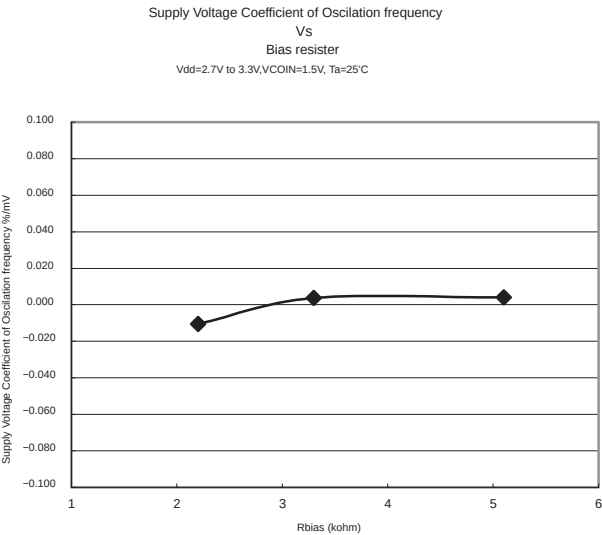


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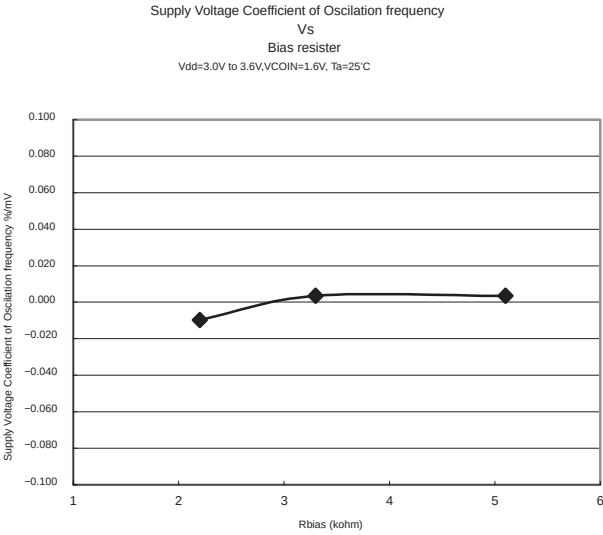


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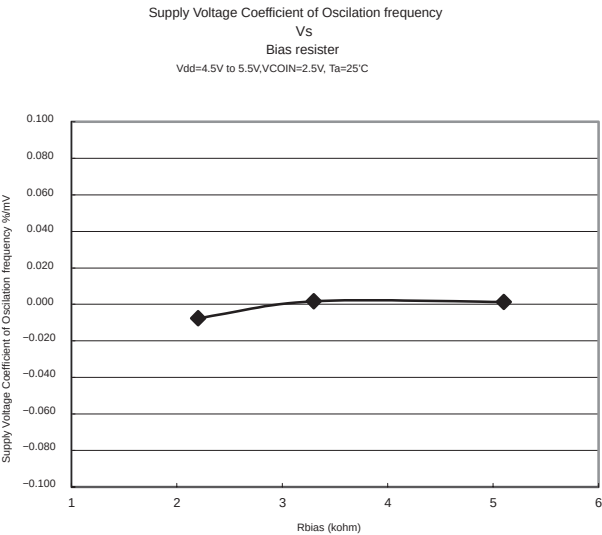


Figure 26.

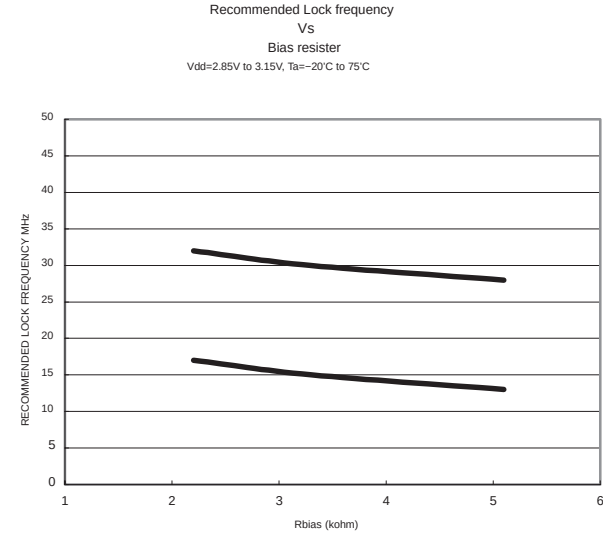


Figure 27.

TYPICAL CHARACTERISTICS

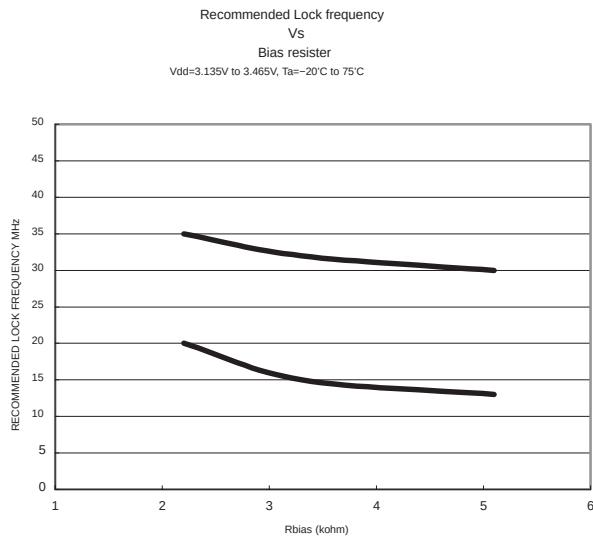


Figure 28.

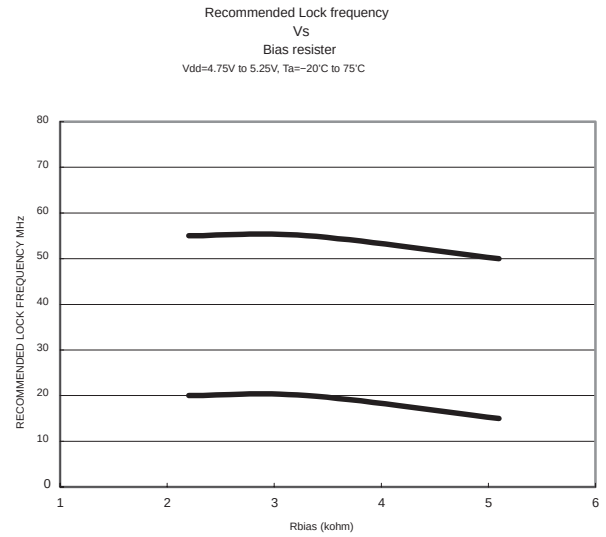


Figure 29.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2932AIPW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2932A
TLC2932AIPW.B	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2932A
TLC2932AIPWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2932A
TLC2932AIPWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2932A
TLC2932AIPWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2932A
TLC2932AIPWRG4.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 75	Y2932A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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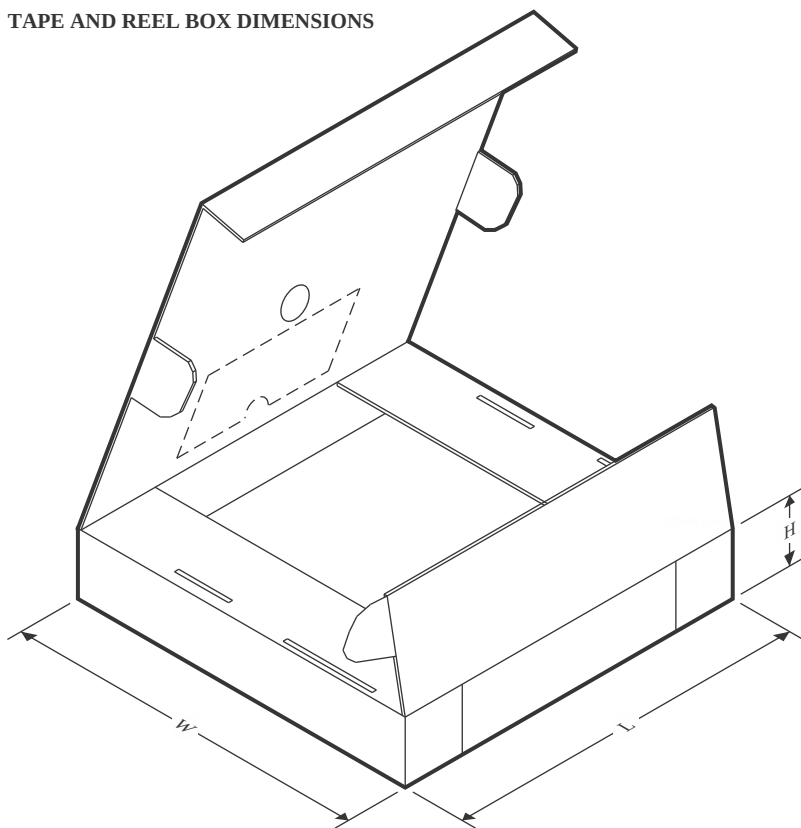
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2932AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2932AIPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

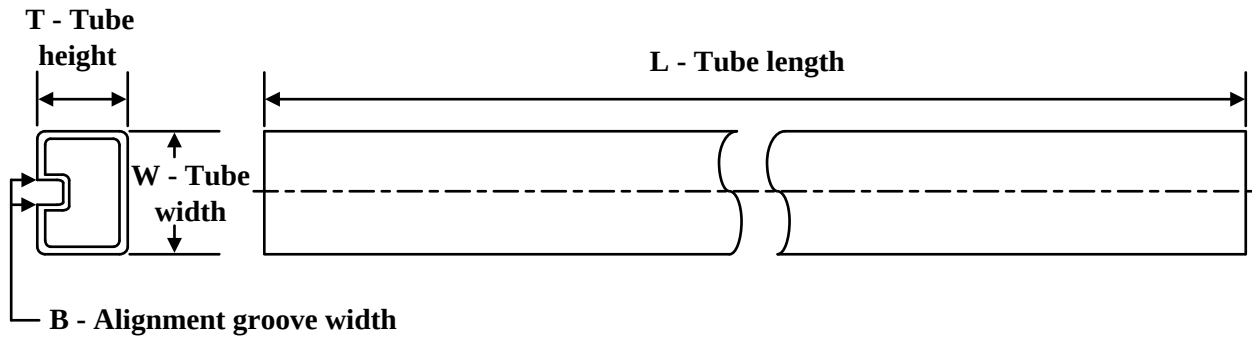
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2932AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLC2932AIPWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

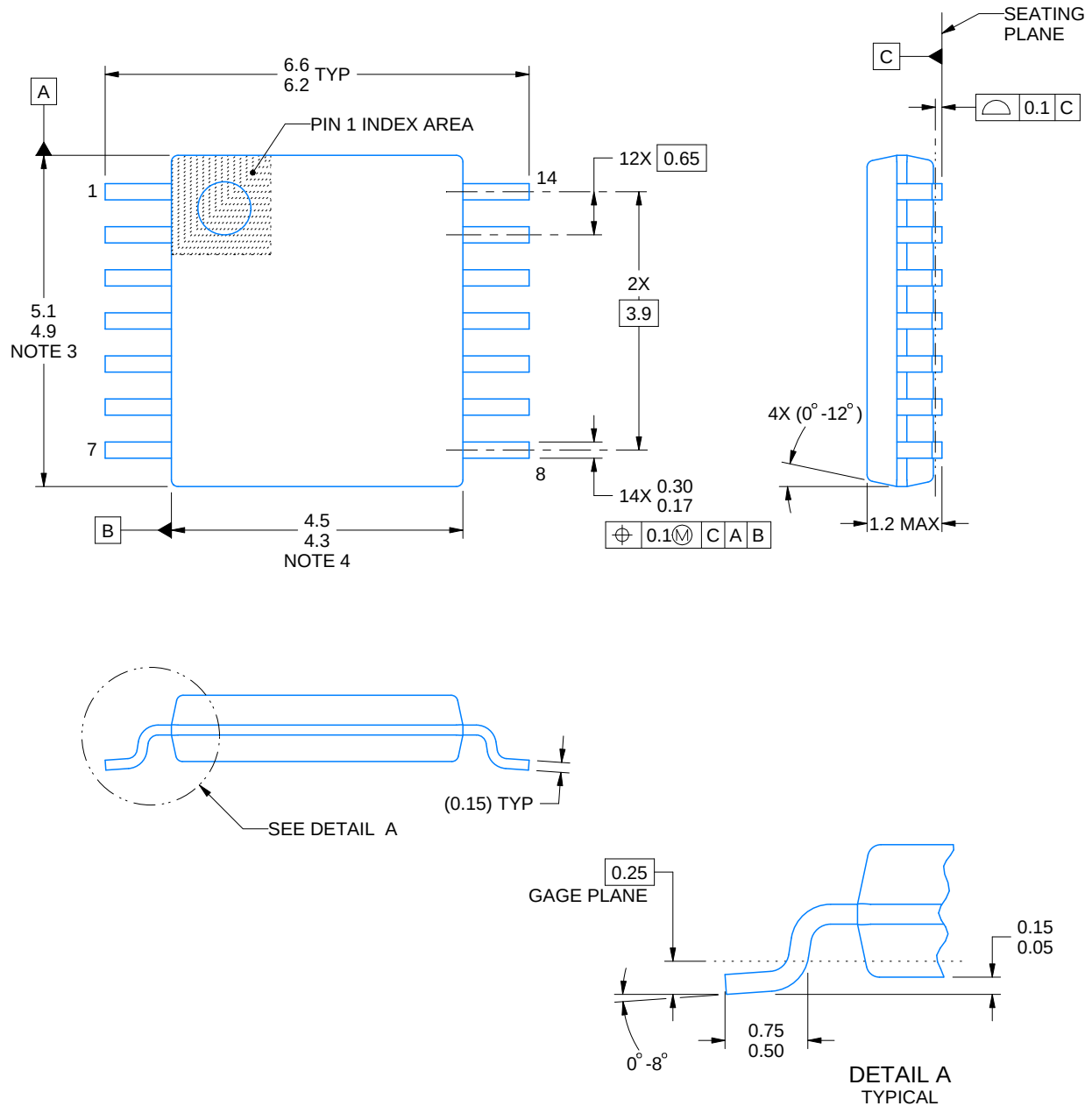
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC2932AIPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLC2932AIPW.B	PW	TSSOP	14	90	530	10.2	3600	3.5

PW0014A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

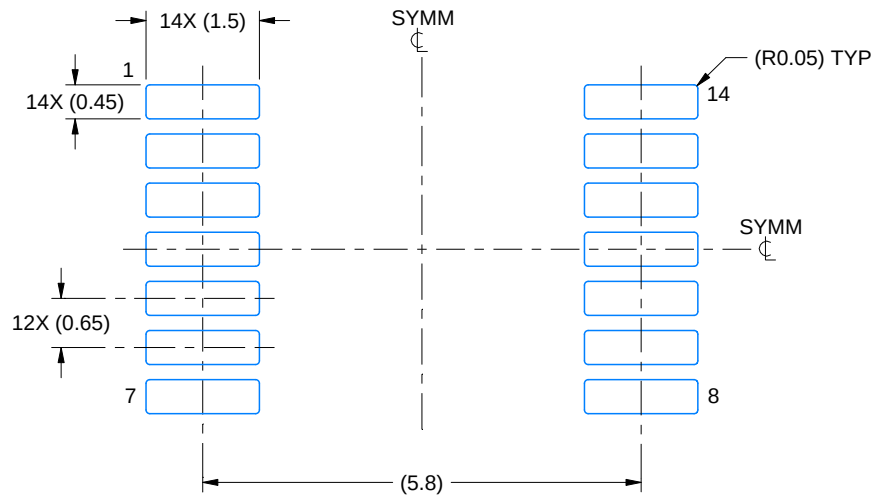
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

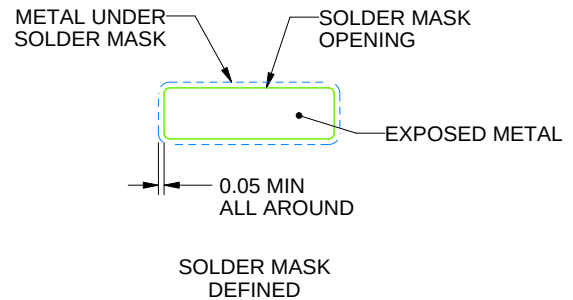
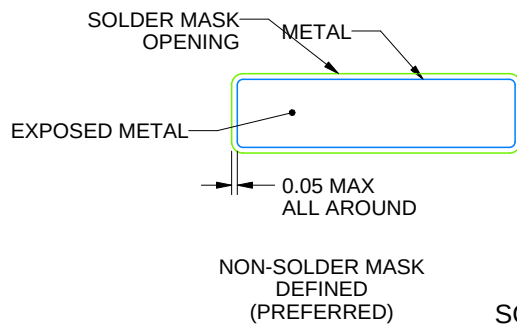
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

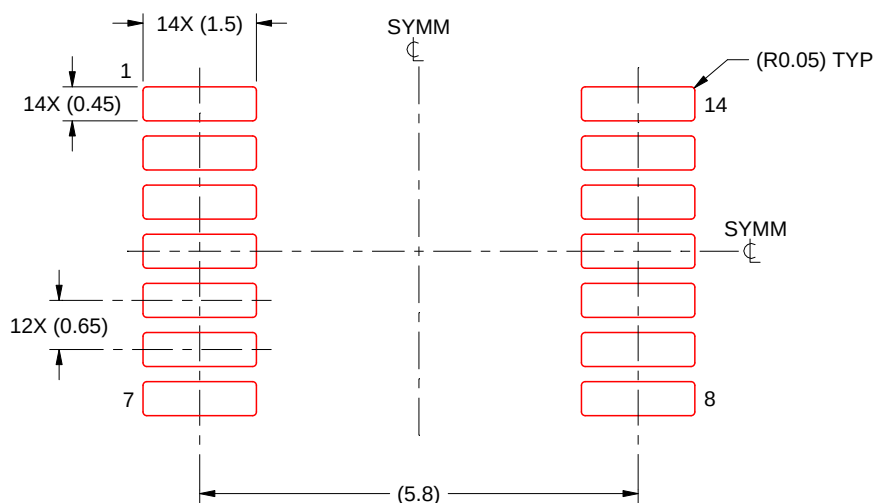
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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