TEXAS INSTRUMENTS

TLC59213, **TLC59213A**

SLVS867B – MAY 2009 – REVISED AUGUST 2015

TLC59213x 8-Bit Parallel In and Out Darlington Source Driver With Latch

1 Features

- Output Current on Each Channel
  (I_{OUT} Max = –500 mA)
- $V_{CE(sus)}$ = 13.2 V
- Input Compatible With TTL/5-V CMOS
- Clear ($\overline{CLR}$) and Clock (CLK) TTL/CMOS Control Inputs
- CLR Control Input to Off the Output
- Darlington Source Driver
- Clock Input Up to 1 MHz
- Enhanced Hold Time (t_h) on TLC59213A
- Temperature Range: –40°C to 85°C

2 Applications

- Lamp and Display (LED)
- Hammer
- Relay

3 Description

The TLC59213 and TLC59213A are 8-bit source drivers with input latch with CLK input and $\overline{CLR}$ to set the output OFF. The TLC59213 and TLC59213A have large output source currents up to 500 mA with Darlington transistor and collectors tied to V_{CC}. These feature make the device optimum level of driving the matrix of ink jet printer head, LEDs, and the scan-side of resistor's matrix. The TLC59213 and TLC59213A differ only in the Data Hold Time Specification (t_h).

The clamp diode is between output and ground for switching inductive load.

All inputs are TTL/CMOS, which enable to any logic-level inputs such as MCU, CPU or SN74LV594 (serial to parallel) and the output enable LED matrix display. It can also be used with another device sink driver such as TLC59210, TLC59211 and TLC59212.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC59213 TLC59213A	PDIP (20)	24.33 mm × 6.35 mm
	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Application Diagram÷**

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2010) to Revision B   **Page**

5 Pin Configuration and Functions

N or PW Package
20-Pin PDIP or TSSOP
Top View

```
         ┌────∪────┐
 CLR □ 1          20 □ VCC
  D1 □ 2          19 □ Y1
  D2 □ 3          18 □ Y2
  D3 □ 4          17 □ Y3
  D4 □ 5          16 □ Y4
  D5 □ 6          15 □ Y5
  D6 □ 7          14 □ Y6
  D7 □ 8          13 □ Y7
  D8 □ 9          12 □ Y8
 CLK □ 10         11 □ GND
         └─────────┘
```
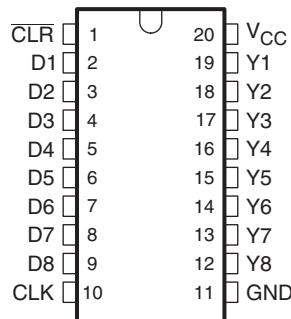
Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{CLR}}$	1	I	Direct clear of output
D1	2	I	Input control to the current source driver
D2	3	I	Input control to the current source driver
D3	4	I	Input control to the current source driver
D4	5	I	Input control to the current source driver
D5	6	I	Input control to the current source driver
D6	7	I	Input control to the current source driver
D7	8	I	Input control to the current source driver
D8	9	I	Input control to the current source driver
CLK	10	I	Clock to positive edge triggered D flipflops
GND	11	—	Ground
Y8	12	O	Output to load
Y7	13	O	Output to load
Y6	14	O	Output to load
Y5	15	O	Output to load
Y4	16	O	Output to load
Y3	17	O	Output to load
Y2	18	O	Output to load
Y1	19	O	Output to load
V_{cc}	20	I	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		−0.5	15	V
V_I	Input voltage		−0.5	V_{CC} + 0.5	V
	Collector-emitter voltage		−0.5	15	V
I_O	Peak output current			−500	mA
I_{IK}	Input clamp current	$V_I < 0$ V		−20	mA
I_{OK}	Output clamp current	$V_O < 0$ V		−500	mA
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage			4.5	13.2	V
V_{IH}	High-level input voltage			2		V
V_{IL}	Low-level input voltage				0.8	V
I_O	Output current (8 channel)	N package	Duty cycle < 10%		400	mA
			Duty cycle < 50%		200	
		PW package	Duty cycle < 10%		350	
			Duty cycle < 50%		170	
T_A	Operating free-air temperature			−40	85	°C

6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CEX}	Output leakage current	$V_{CC} = 13.2$ V, Outputs off				2	µA
$V_{CE(sus)}$	Output saturation voltage	$I_{OUT} = −350$ mA				2.35	V
		$I_{OUT} = −225$ mA				2.15	
		$I_{OUT} = −100$ mA				1.96	
I_I	Input current	$V_{CC} = 13.2$ V, $V_I = 0$ or 13.2 V				1	µA
V_f	Clamp forward voltage	$I_f = −350$ mA		−2			V
I_{CC}	Supply current	$V_{CC} = 13.2$ V, $V_I = 0$ or 13.2 V	All outputs OFF		4.6	13	mA
			All outputs ON		4.8	13	
C_I	Input capacitance					10	pF

Product Folder Links: *TLC59213 TLC59213A*

6.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted), see Figure 3

					MIN	MAX	UNIT
t_{su}	Setup time	D before CLK ↑			50		ns
		$\overline{CLR}$ high before CLK ↑			50		ns
t_h	Hold time	D after CLK ↑	TLC59213, TLC59213A	T_A = -40°C to 85°C	50		ns
			TLC59213	T_A = 0°C to 70°C	25		
			TLC59213A	T_A = 0°C to 70°C, V_{CC} = 4.5 V to 5.5 V	15		
				T_A = 0°C to 70°C, V_{CC} = 10.8 V to 13.2 V	19		
t_w	Pulse width	CLK, $\overline{CLR}$			100		ns

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted), see Figure 3

| PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A = 25°C			T_A = –40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	CLK	Y	RL = 25 Ω, C_L = 15 pF		107	200		250	ns
t_{PHL}	Propagation delay time, high-to-low level output	CLK	Y	RL = 25 Ω, C_L = 15 pF		111	200		250	ns
t_{PHLR}	Propagation delay time, high-to-low level output	$\overline{CLR}$	Y	RL = 25 Ω, C_L = 15 pF		104	200		250	ns

6.7 Typical Characteristics
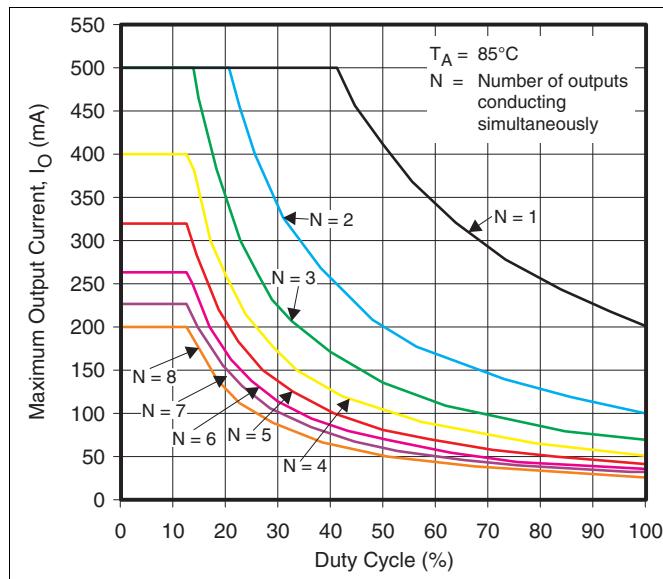
Figure 1. Maximum Output Current vs Duty Cycle (TSSOP (PW) Package)
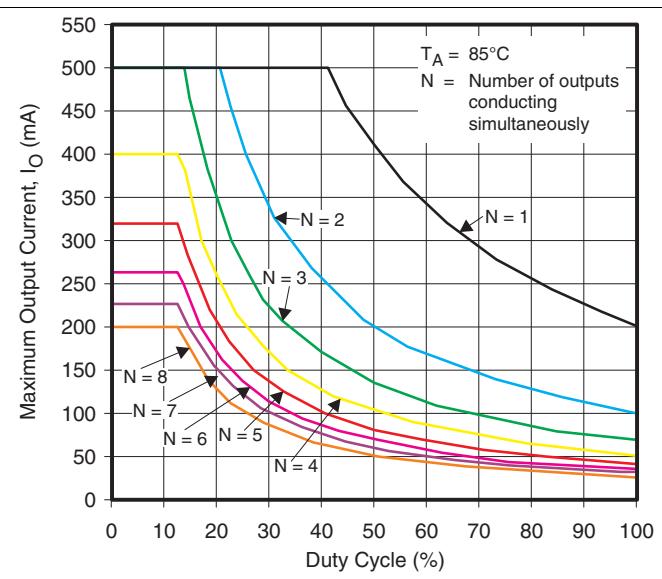

Figure 2. Maximum Output Current vs Duty Cycle (DIP (N) Package)

7 Parameter Measurement Information

TEST CIRCUIT

VOLTAGE WAVEFORMS
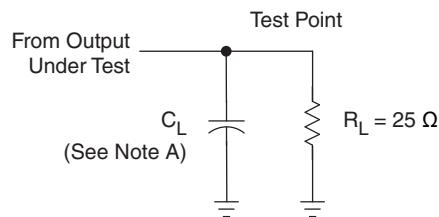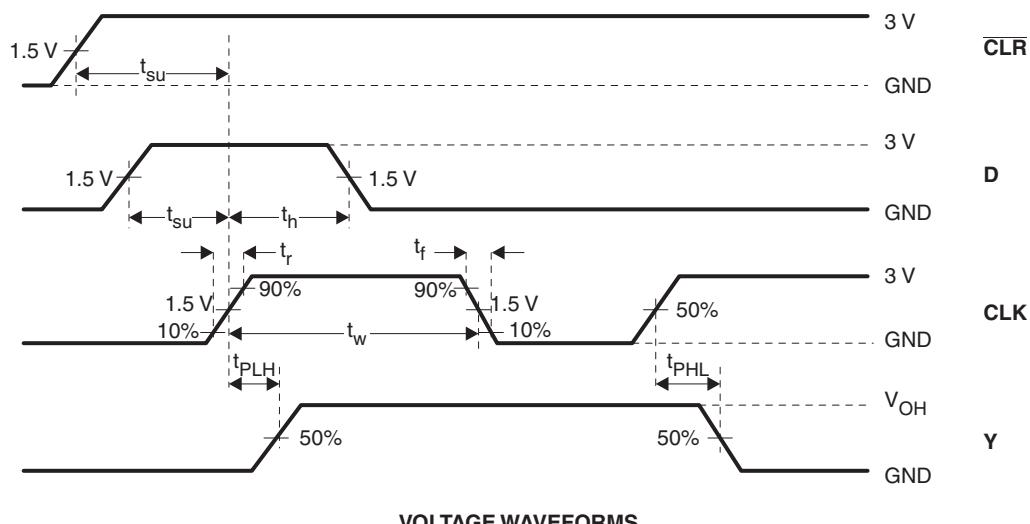
A. C_L includes probe and jig capacitance.

B.   All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, and t_f ≤ 3 ns.

C.   The outputs are measured one at a time with one transition per measurement.

Figure 3. Test Circuit and Voltage Waveforms

Product Folder Links: *TLC59213 TLC59213A*

8 Detailed Description

8.1 Overview

The TLC59213 device is an 8-bit Darlington source driver with latch for large-output source currents up to 500 mA.

## 8.2 Functional Block Diagram
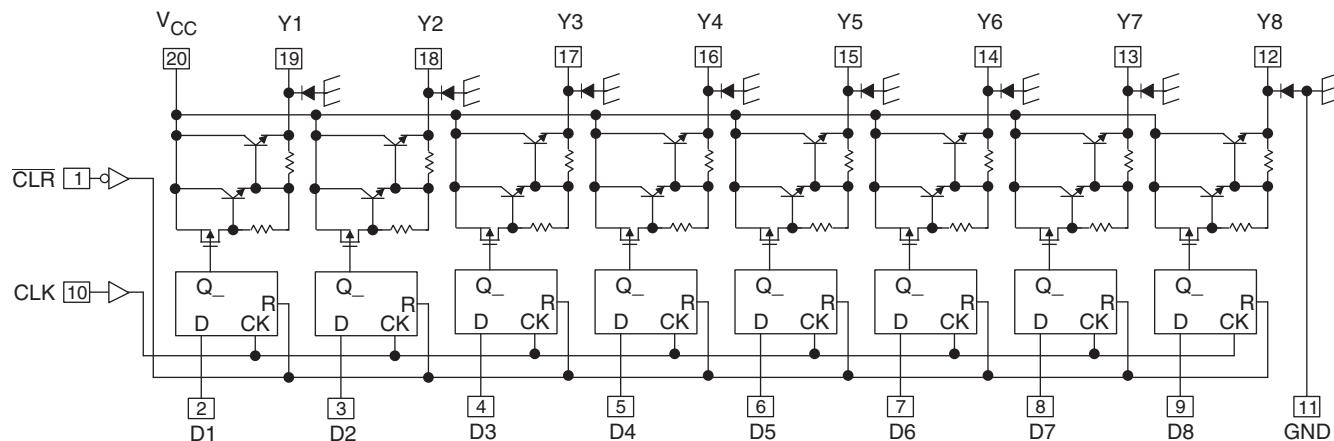
(1)   This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

8.3 Feature Description

Each of the 8 channels is controlled by its input (Dn), a direct clear ($\overline{\text{CLR}}$), and clock (CLK) through a positive-edge-triggered D-type flip-flops. Information at the data (D) input meeting the setup time requirements is transferred to the output (Y) on the positive-going edge of the clock (CLK) pulse. When CLK is at either the high or low level, the D-input has no effect at the output. When $\overline{\text{CLR}}$ is at low level, the D-input has no effect at the output.

8.4 Device Functional Modes

Table 1 lists the functional modes of the TLC59213.

Table 1. Function Table (Each Latch)[1]

INPUTS			OUTPUT Y
$\overline{\text{CLR}}$	CLK	D	
L	X	X	Z (OFF)
H	↑	L	Z (OFF)
H	↑	H	H (ON)
H	L	X	Y_0
H	↓	X	Y_0

(1)   L: Low-level
      H: High-level
      X: Irrelevant
      ↑: Rising edge
      ↓: Falling edge
      Z : High-impedance (OFF)

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In LED display application, TLC59213 is used to drive the current source for 8 LEDs in parallel. LED display pattern can be created by providing different bit pattern. At every positive clock edge, new bit pattern will be transferred to LED display.

9.2 Typical Application
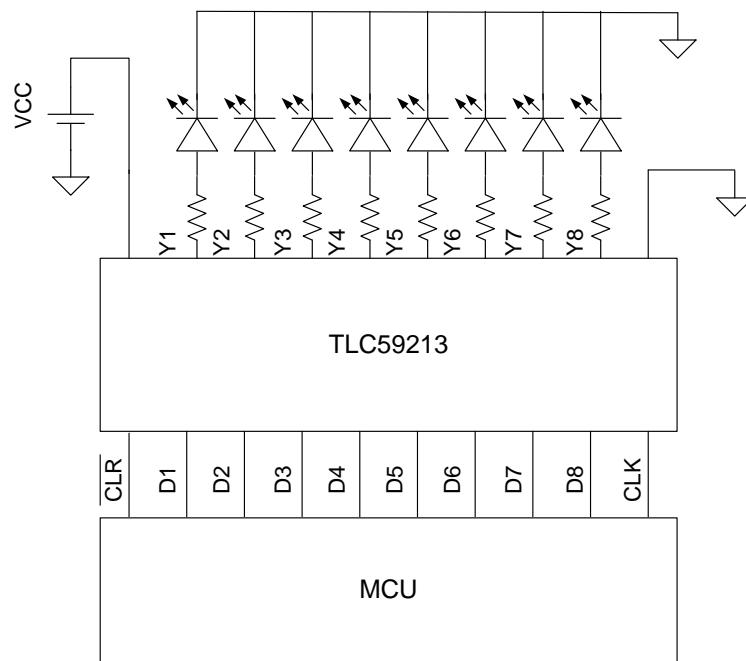
Figure 4. Typical Application Diagram

9.2.1 Design Requirements

For LED display application, LED is selected based on the application. The current level is determined by the required brightness. Given the available supply, the resistor value could be determined. The maximum output current is constrained by the duty cycle. See Figure 1 and Figure 2.

9.2.2 Detailed Design Procedure

The selection of supply voltage (VCC), LED, and resistor sets the current of the LED.

$$VR + VL + VCE = VCC \tag{1}$$
$$I = (VCC - VL - VCE) / R \tag{2}$$

VR is the voltage drop across the resistor, VL is the voltage drop across the LED when LED is on, VCE is the collector-to-emitter voltage of the Darlington current source driver, when the driver is enabled. For example, when VCC = 12 V, VL = 2.9 V, and VCE = 1.6 V, a 75-Ω resistor is used to obtain output current 100 mA.

Product Folder Links: *TLC59213 TLC59213A*

Typical Application (continued)

9.2.3 Application Curve
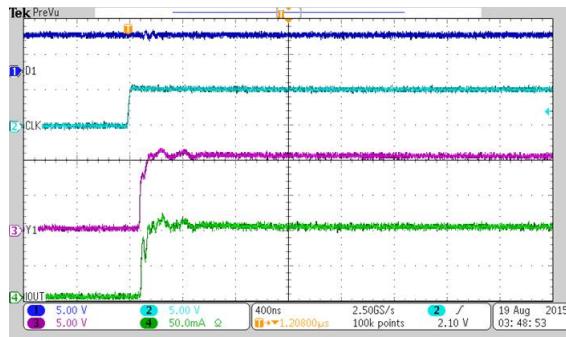
Figure 5. Output Voltage and Current Response

10 Power Supply Recommendations

The supply voltage to TLC59213 is from 4.5 V to 13.2 V.

11 Layout

11.1 Layout Guidelines

The traces that carry current from the output pins must be wide enough to support the current.

### 11.2 Layout Example
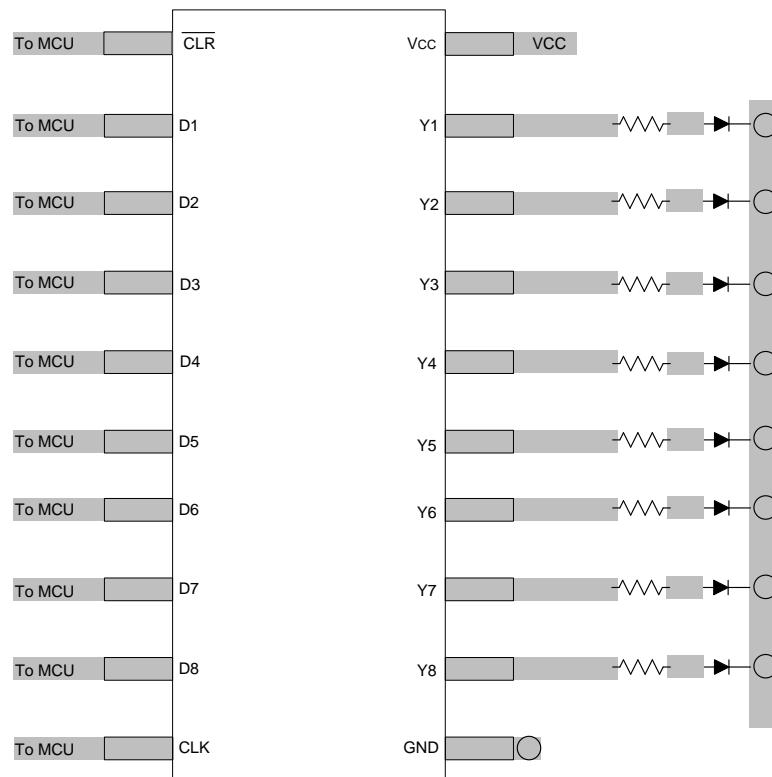
◯ VIA to GND

Figure 6. Layout Recommendation

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC59213AIN	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC59213AIN
TLC59213AIN.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC59213AIN
TLC59213AIPW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-	Y59213A
TLC59213AIPWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59213A
TLC59213AIPWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59213A
TLC59213AIPWT	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	Y59213A
TLC59213IN	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC59213IN
TLC59213IN.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC59213IN
TLC59213IPWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59213
TLC59213IPWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59213

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS
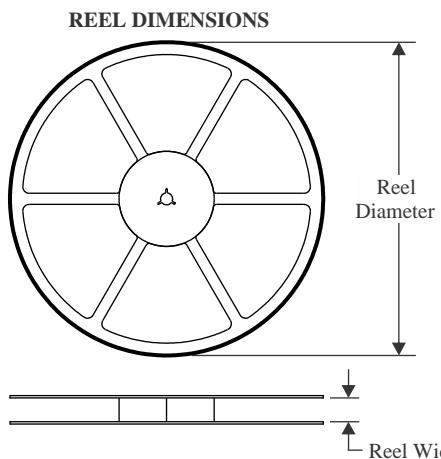
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59213AIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TLC59213IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59213AIPWR	TSSOP	PW	20	2000	353.0	353.0	32.0
TLC59213IPWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width
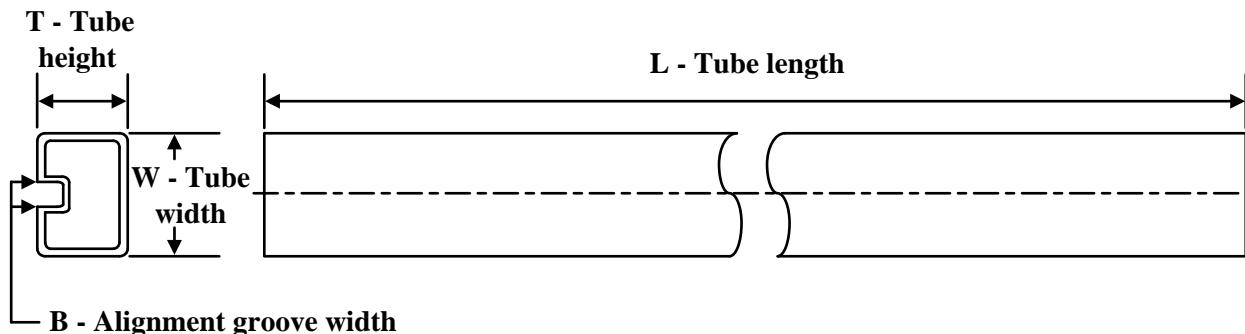
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC59213AIN	N	PDIP	20	20	506	13.97	11230	4.32
TLC59213AIN.A	N	PDIP	20	20	506	13.97	11230	4.32
TLC59213IN	N	PDIP	20	20	506	13.97	11230	4.32
TLC59213IN.A	N	PDIP	20	20	506	13.97	11230	4.32

SEATING PLANE

PIN 1 INDEX AREA

6.6
6.2 TYP

18X 0.65

2X
5.85

6.6
6.4
NOTE 3

20X 0.30
0.19

4.5
4.3
NOTE 4

1.2 MAX

0.1 C

0.1 Ⓜ C A B

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0.15
0.05

0.75
0.50

0° -8°

DETAIL A
TYPICAL

4220206/A   02/2017
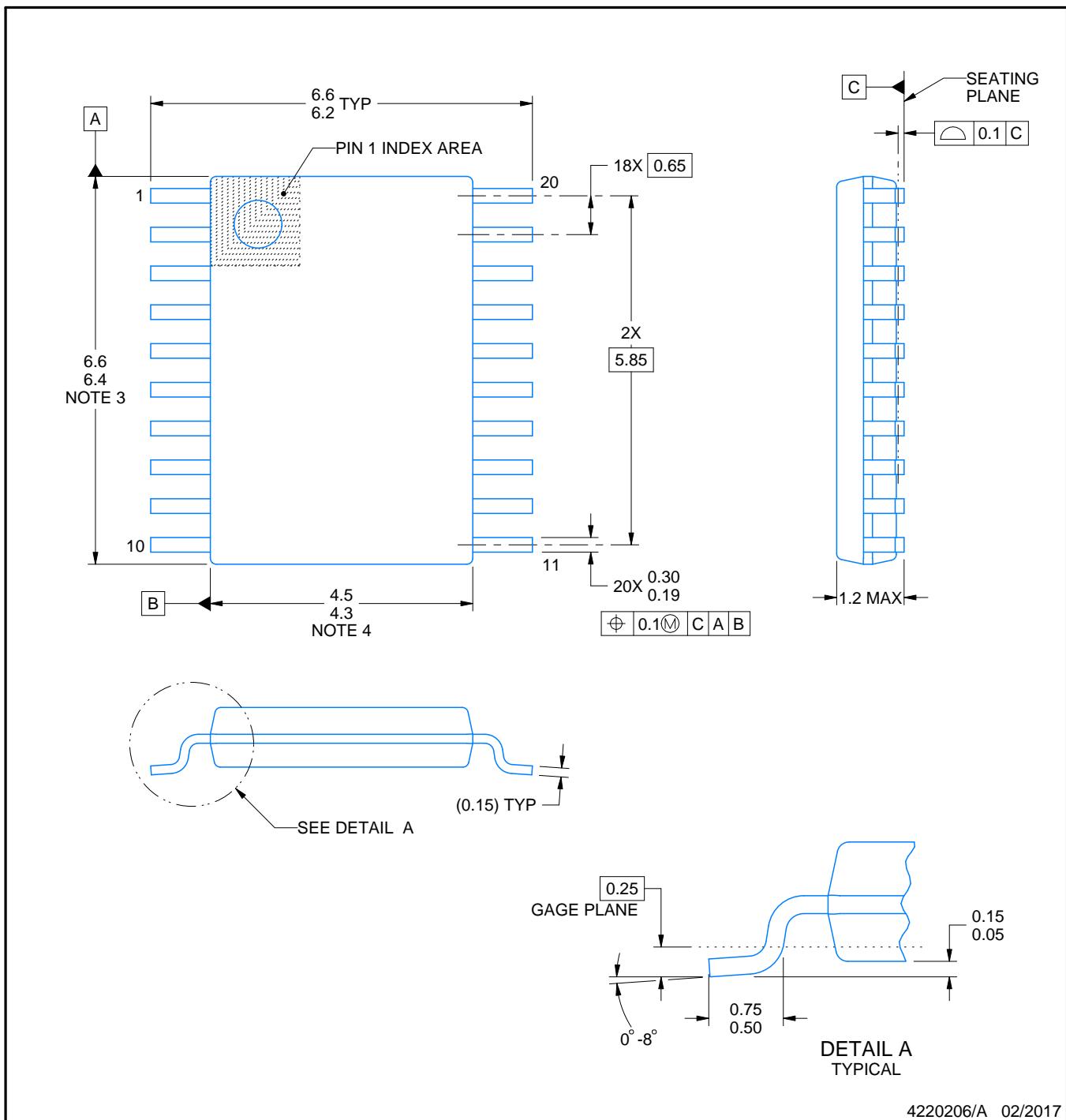
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

TEXAS INSTRUMENTS
www.ti.com

20X (1.5)

SYMM

(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)
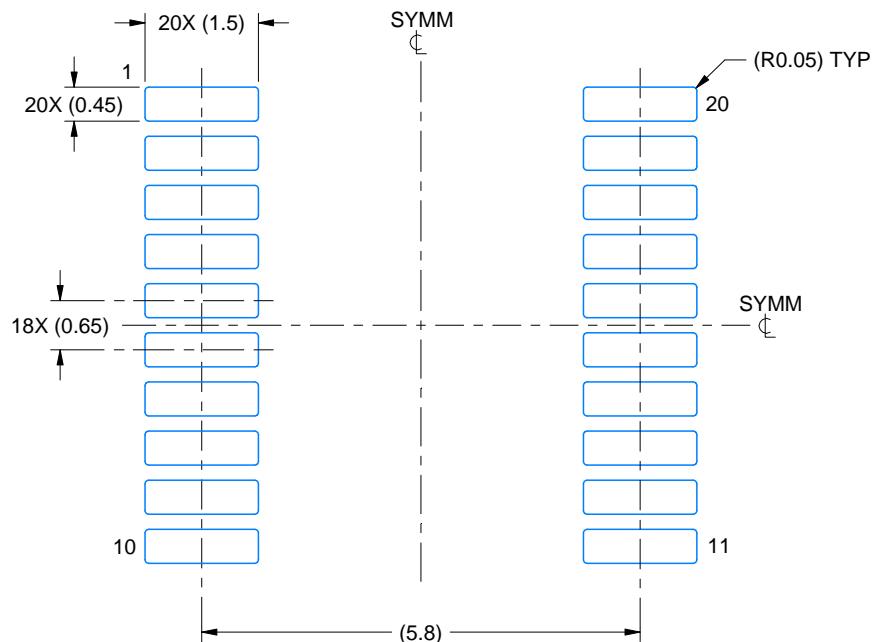
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
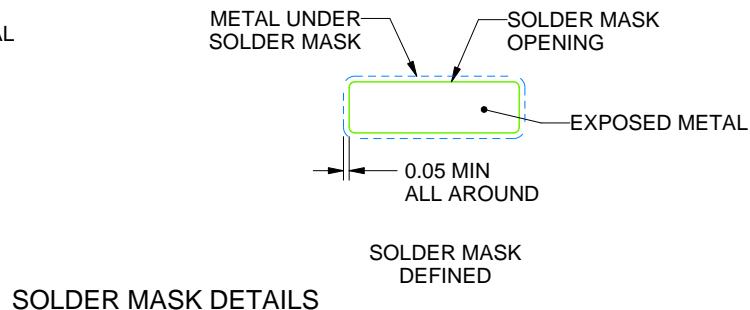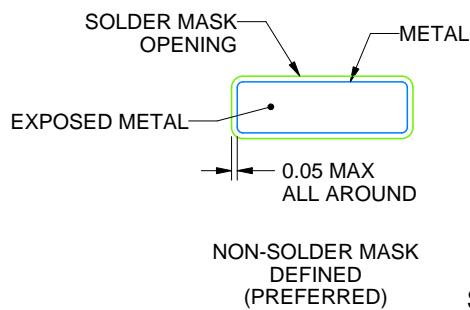
4220206/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (1.5)

SYMM

(R0.05) TYP

1

20X (0.45)

20

18X (0.65)

SYMM

10

11

(5.8)
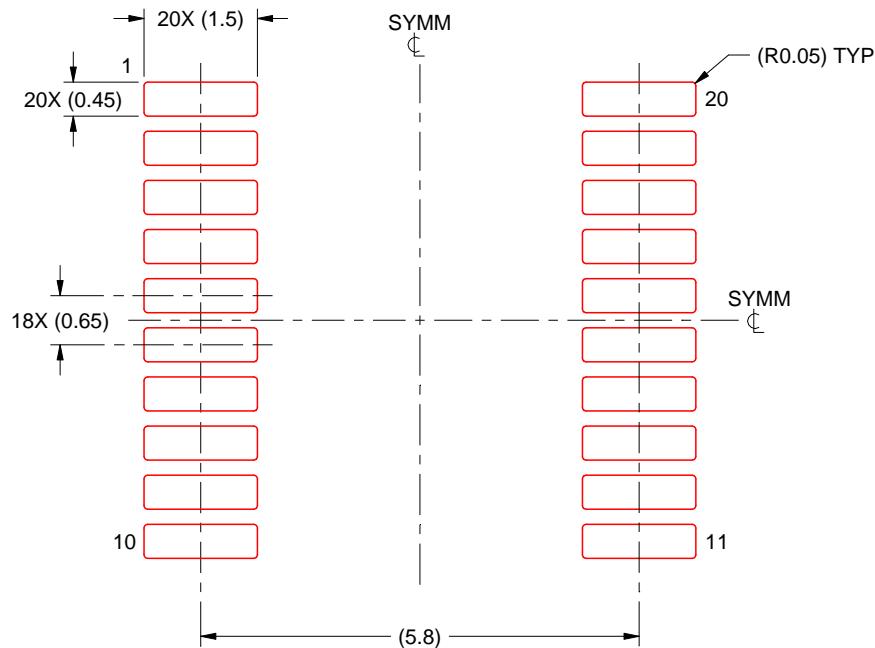
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R−PDIP−T**) PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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