TLIN1021A-Q1 故障保护 LIN 收发器，配备抑制和唤醒功能

1 特性

- 符合面向汽车应用的 AEC-Q100（1 级）标准
- 符合 LIN 2.0、LIN 2.1、LIN 2.2、LIN 2.2A 和 ISO 17987 – 4 电气物理层 (EPL) 规格标准
- 符合 SAE J2602-1 面向汽车应用的 LIN 网络标准
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 宽工作输入电压范围：
  - V_{SUP} 范围为 4.5V 至 36V
- LIN 传输数据速率高达 20kbps
- LIN 接收数据速率高达 100kbps
- 工作模式：正常、待机和睡眠
- 通过源识别提供低功耗模式唤醒支持：
  - 通过 LIN 总线实现远程唤醒
  - 通过 WAKE 引脚实现本地唤醒
  - 通过 EN 引脚实现本地唤醒
- 集成 45kΩ LIN 上拉电阻器
- 使用 INH 引脚控制系统级功耗
- 在 LIN 总线和 RXD 输出上实现上电/断电无干扰运行
- 保护特性：±45V LIN 总线容错、42V 负载突降支持、V_{SUP} 上的欠压保护、TXD 显性状态超时、热关断、系统级未供电节点或接地断开失效防护
- 结温范围为 -40°C 至 150°C
- 可采用 8 引脚 SOIC、具有可湿性侧面的 VSON 和 SOT23 封装

2 应用

- 车身电子装置和照明
- 汽车信息娱乐系统与仪表组
- 混合动力电动汽车和动力总成系统
- 工业运输

3 说明

TLIN1021A-Q1 是一款本地互连网络 (LIN) 物理层收发器。LIN 是支持汽车车载网络的低速通用异步接收器发送器 (UART) 通信协议。

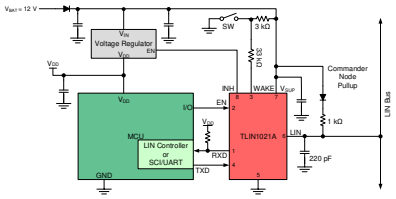
TLIN1021A-Q1 变送器支持高达 20 kbps 的数据速率。收发器通过 TXD 引脚控制 LIN 总线的状态，并通过其开漏 RXD 输出引脚报告总线的状态。该器件具有限流波形整形驱动器，用于降低电磁辐射 (EME)。

TLIN1021A-Q1 旨在为 12V 应用提供支持，具有宽输入工作电压范围。该器件支持低功耗睡眠模式，并可通过从 LIN、WAKE 引脚或 EN 引脚唤醒的功能从低功耗模式唤醒。该器件可以通过 TLIN1021A-Q1 INH 输出引脚选择性地启用节点上会存在的各种电源，从而在整个系统级别减少电池电流消耗。

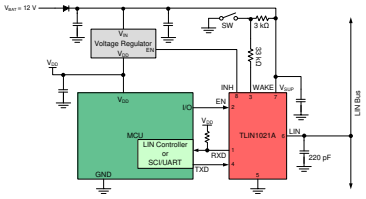
器件信息

器件型号	封装(1)	封装尺寸（标称值）
TLIN1021A-Q1	SOIC (D) (8)	4.90mm x 3.91mm
	VSON (DRB) (8)	3.00mm x 3.00mm
	SOT (DDF) (8)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版指挥官节点原理图



简化版响应者节点原理图

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (January 2022) to Revision B (April 2022)	Page
• 删除了原理图后面的注释	1
• Corrected WAKE I_{IL} parameter description	7

Changes from Revision * (December 2020) to Revision A (January 2022)	Page
• 删除了*器件信息*表 SOIC (D) 和 SOT (DDF) 封装的“产品预发布”说明	1

5 说明（续）

TLIN1021A-Q1 集成了一个用于 LIN 响应器节点应用并能实现 ESD 保护和故障保护的电阻器，可减少应用中的外部组件数量。一旦发生接地漂移或电源电压断开，该器件可防止反馈电流经 LIN 流向电源输入。

TLIN1021A-Q1 还包含欠压检测、过热关断保护和接地失效保护功能。一旦发生故障情况，此发送器便会立即关闭并在故障被排除之前一直保持关闭状态。

6 Pin Configuration and Functions

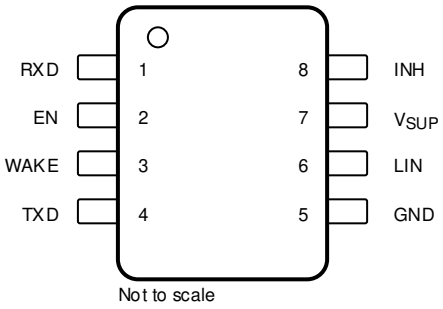


图 6-1. D Package, 8-Pin (SOIC), and DDF Package, 8-Pin (SOT23) Top View

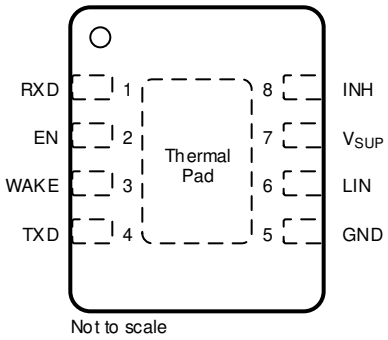


图 6-2. DRB Package, 8-Pin (VSON), Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
RXD	1	Digital	LIN receive data output, open-drain
EN	2	Digital	Sleep mode control input, integrated pull-down
WAKE	3	High Voltage	Local wake-up input, high voltage
TXD	4	Digital	LIN transmit data input, integrated pulled down - active low after a local wake-up event
GND	5	GND	Ground connection
LIN	6	Bus IO	LIN bus input/output line
V_{SUP}	7	Supply	High-voltage supply from the battery
INH	8	High Voltage	Inhibit output to control system voltage regulators and supplies, high voltage
Thermal Pad	—		Electrically connected to GND, connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

7 Specification

7.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range (ISO 17987)	–0.3	45	V
V_{LIN}	LIN Bus input voltage (ISO 17987)	–45	45	V
V_{WAKE}	WAKE pin input voltage	–0.3	45	V
V_{INH}	INH pin output voltage	–0.3	45 and $V_O \leq V_{SUP}$+0.3	V
V_{LOGIC_INPUT}	Logic input voltage	–0.3	6	V
V_{LOGIC_OUTPUT}	Logic output voltage	–0.3	6	V
I_O	Digital pin output current		8	mA
$I_{O(INH)}$	Inhibit output current		4	mA
$I_{O(WAKE)}$	WAKE output current due to ground shift ($V_{WAKE} \leq V_{GND}$) – 0.3 V thus current out of the WAKE pin must be limited		3	mA
T_J	Junction Temp	–55	165	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM) classification level 3B: V_{SUP}, INH, and WAKE with respect to ground		±8000	V
		Human body model (HBM) classification level 3B: LIN with respect to ground		±10000	
		Human body model (HBM) classification level 3A: all other pins, per AEC Q100-002(1)		±4000	
		Charged device model (CDM) classification level C5, per AEC Q100-011	All pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 ESD Ratings - IEC Specification

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	LIN, V_{SUP}, WAKE terminal to GND(1)	IEC 62228-2 per ISO 10605 Contact discharge R = 330 Ω, C = 150 pF (IEC 61000-4-2)	±8000	V
		LIN terminal to GND(1)	IEC 62228-2 per ISO 10605 Indirect contact discharge R = 330 Ω, C = 150 pF (IEC 61000-4-2)	±8000	

7.3 ESD Ratings - IEC Specification (continued)

				VALUE	UNIT
V_{TRAN}	Non-synchronous transient injection	LIN, V_{SUP}, WAKE terminal to GND(1)	IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 1	-100	V
			IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 2	75	
			IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 3a	-150	
			IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 3b	150	
	Direct capacitor coupling	LIN terminal to GND(2)	SAE J2962-1 per ISO 7637-3 DCC - Slow transient pulse	±30	

(1) Results given here are specific to the IEC 62228-2 Integrated circuits – EMC evaluation of transceivers – Part 2: LIN transceivers. Testing performed by OEM approved independent 3rd party, EMC report available upon request.
(2) Results given here are specific to the SAE J2962-1 Communication Transceivers Qualification Requirements - LIN. Testing performed by OEM approved independent 3rd party, EMC report available upon request.

7.4 Thermal Information

THERMAL METRIC(1)		TLIN1021AD-Q1 SOIC 8 PINS	TLIN1021ADRB-Q1 VSON 8 PINS	TLIN1021ADDF-Q1 SOT 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.2	54.4	120.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.4	61.1	60.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.6	26.8	42.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.7	2.3	2.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	68.9	26.7	41.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	10.8	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Recommended Operating Conditions

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply Voltage	4.5		36	V
V_{LIN}	LIN Bus input voltage	0		36	V
V_{LOGIC}	Logic Pin Voltage	0		5.25	V
T_J	Operating virtual junction temperature range	-40		150	°C
T_{SDR}	Thermal shutdown rising	160			°C
T_{SDF}	Thermal shutdown falling			150	°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis		10		°C

7.6 Power Supply Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage and Current					

7.6 Power Supply Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SUP}	Operational supply voltage	Device is operational beyond the LIN defined nominal supply voltage range See 图 8-1 See 图 8-2	4.5		36	V
	Nominal supply voltage	Normal and standby modes(1) See 图 8-1 See 图 8-2	4.5		36	V
		Sleep mode	4.5		36	V
I_{SUP}	Supply current Bus dominant	Normal mode EN = V_{CC}, R_{LIN} ≥ 500 Ω, C_{LIN} ≤ 10 nF, INH = WAKE = V_{SUP}		1.2	6.5	mA
		Standby mode EN = 0 V, R_{LIN} ≥ 500 Ω, C_{LIN} ≤ 10 nF, INH =WAKE = V_{SUP}		1	1.7	mA
	Supply current Bus recessive	Normal mode EN = V_{CC}, INH = WAKE = V_{SUP}		300	700	µA
		Standby mode EN = 0 V, INH = WAKE = V_{SUP}		20	55	µA
	Supply current Sleep mode	4.5 V < V_{SUP} ≤ 14 V, T_J = 125℃ EN = 0 V, LIN = WAKE = V_{SUP}, TXD and RXD floating		9	16	µA
		14 V < V_{SUP} ≤ 36 V, T_J = 125℃ EN = 0 V, LIN = WAKE = V_{SUP}, TXD and RXD floating			22	µA
UV_{SUPR}	Under voltage V_{SUP} threshold	Ramp up		4.15	4.45	V
UV_{SUPF}	Under voltage V_{SUP} threshold	Ramp down	3.5	4		V
U_{VHYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			0.13		V

(1) Normal mode ramp V_{SUP} while LIN signal is a 10 kHz square wave with 50% duty cycle and 36 V swing.

7.7 Electrical Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXD Output Terminal						
V_{OL}	Low-level voltage	Based upon external pull-up to V_{CC} (4)			0.6	V
I_{OL}	Low-level output current, open drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, RXD = V_{CC}	-5		5	µA
TXD Input Terminal						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2			V
I_{LKG}	Low-level input leakage current	TXD = 0 V	-5		5	µA
$I_{TXD(WAKE)}$	Local wake-up source recognition TXD	Standby mode after a local wake-up event V_{LIN} = V_{SUP}, WAKE = 0 V or V_{SUP}, TXD = 1 V	1.3		8	mA
R_{TXD}	Internal pull-down resistor value		125	350	800	kΩ
EN Input Terminal						
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{IH}	High-level input voltage		2		5.25	V
V_{HYS}	Hysteresis voltage	By design and characterization	30		500	mV
I_{IL}	Low-level input current	EN = 0 V	-5		5	µA
R_{EN}	Internal pull-down resistor		125	350	800	kΩ
LIN Terminal (Referenced to V_{SUP})						
V_{OH}	LIN recessive high-level output voltage(3)	TXD = V_{CC}, I_O = 0 mA 7 V ≤ V_{SUP} ≤ 36 V	0.85			V_{SUP}

7.7 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	LIN recessive high-level output voltage(1) (2)	TXD = V_{CC}, I_O = 0 mA 7 V ≤ V_{SUP} ≤ 18 V	0.8			V_{SUP}
V_{OH}	LIN recessive high-level output voltage(3)	TXD = V_{CC}, I_O = 0 mA 4.5 V ≤ V_{SUP} ≤ 7 V	3			V
V_{OL}	LIN dominant low-level output voltage(3)	TXD = 0 V 7 V ≤ V_{SUP} ≤ 36 V			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage(1) (2)	TXD = 0 V 7 V ≤ V_{SUP} ≤ 18 V			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage(3)	TXD = 0 V 4.5 V ≤ V_{SUP} ≤ 7 V			1.2	V
V_{BUSdom}	Low-level input voltage(3)	LIN dominant (including LIN dominant for wake up) See 图 8-3 See 图 8-4			0.4	V_{SUP}
V_{BUSrec}	High-level input voltage(3)	Lin recessive See 图 8-3 See 图 8-4	0.6			V_{SUP}
V_{IH}	LIN recessive high-level input voltage(1) (2)	7 V ≤ V_{SUP} ≤ 18 V	0.47		0.6	V_{SUP}
V_{IL}	LIN dominant low-level input voltge(1) (2)	7 V ≤ V_{SUP} ≤ 18 V	0.4		0.53	V_{SUP}
$V_{SUP\_NON\_OP}$	V_{SUP} where impact of recessive LIN bus < 5%(3)	TXD & RXD open 4.5 V ≤ V_{LIN} ≤ 45 V	-0.3		42	V
V_{BUS_CNT}	Receiver center threshold(3)	V_{BUS_CNT} = (V_{BUSrec} + V_{BUSdom})/2 See 图 8-3 See 图 8-4	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO 17987)	V_{HYS} = V_{BUSrec} - V_{BUSdom} See 图 8-3 See 图 8-4			0.175	V_{SUP}
V_{HYS}	Hysteresis voltage (SAE J2602)	V_{HYS} = V_{IH} - V_{IL} See 图 8-3 See 图 8-4	0.07		0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN termination pull-up path	I_{SERIAL_DIODE} = 10 µA	0.4	0.7	1.0	V
$I_{BUS(LIM)}$	Limiting current ISO 17987 Param 12	TXD = 0 V, V_{LIN} = 18 V, V_{SUP} = 18 V	40	90	200	mA
$I_{BUS\_PAS\_dom}$	Receiver leakage current, dominant	Driver off/recessive, LIN = 0 V V_{SUP} = 12 V See 图 8-6	-1			mA
$I_{BUS\_PAS\_rec1}$	Receiver leakage current, recessive	Driver off/recessive, LIN ≥ V_{SUP} 4.5 V ≤ V_{SUP} ≤ 36 V See 图 8-7			20	µA
$I_{BUS\_PAS\_rec2}$	Receiver leakage current, recessive	Driver off/recessive, LIN = V_{SUP} See 图 8-7	-5		5	µA
$I_{BUS\_NO\_GND}$	Leakage current, loss of ground	GND_{Device} = V_{SUP} = 18 V R_{Meas} = 1 kΩ 0 V < V_{LIN} < 18 V	-1		1	mA
$I_{leak\ gnd(dom)}$	Leakage current, loss of ground(5)	V_{SUP} = 8 V, GND = open, V_{SUP} = 18 V, GND = open $R_{Commander}$ = 1 kΩ, C_L = 1 nF $R_{Responder}$ = 20 kΩ, C_L = 1 nF LIN = dominant	-1		1	mA
$I_{leak\ gnd(rec)}$	Leakage current, loss of ground(5)	V_{SUP} = 8 V, GND = open, V_{SUP} = 18 V, GND = open $R_{Commander}$ = 1 kΩ, C_L = 1 nF $R_{Responder}$ = 20 kΩ, C_L = 1 nF LIN = recessive	-100		100	µA
$I_{BUS\_NO\_BAT}$	Leakage current, loss of supply	V_{SUP} = GND 0 V ≤ V_{LIN} ≤ 18 V			5	µA
I_{RSLEEP}	Pull-up current source to V_{SUP} sleep mode	V_{SUP} = 14 V, LIN = GND	-20		-1.5	µA
R_{PU}	Internal pull-up resistor to V_{SUP}	Normal and standby modes	20	45	60	kΩ

7.7 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{LIN}	Capacitance of the LIN pin	V_{SUP} = 14 V			25	pF
INH Output Terminal						
ΔV_H	High level voltage drop INH with respect to V_{SUP}	I_{INH} = - 0.5 mA		0.5	1	V
$I_{LKG(INH)}$	Leakage current sleep mode	INH = 0 V	– 0.5		0.5	µA
WAKE Input Terminal						
V_{IH}	High-level input voltage	Standby and sleep mode	V_{SUP} – 1.8			V
V_{IL}	Low-level input voltage	Standby and sleep mode			V_{SUP} – 3.85	V
I_{IH}	High-level input leakage current	WAKE = V_{SUP} - 1 V	– 25	– 12.5		µA
I_{IL}	Low-level input leakage current	WAKE = 1 V		15	25	µA
t_{WAKE}	WAKE hold time	Wake up time from sleep mode	5		50	µs
Duty Cycle Characteristics						
D1	Duty cycle 1(3) ISO 17987 Param 27	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50 µs D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See 图 8-8 and 图 8-9	0.396			
D1	Duty cycle 1(3) (6)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} V_{SUP} = 4.5 V to 7 V, t_{BIT} = 50 µs D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See 图 8-8 and 图 8-9	0.396			
D1	Duty cycle 1(1) (2) (6)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 52 µs D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See 图 8-8 and 图 8-9	0.396			
D2	Duty cycle 2(3) ISO 17987 Param 28	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50 µs D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See 图 8-8 and 图 8-9			0.581	
D2	Duty cycle 2(3) (6)	$TH_{REC(MIN)}$ = 0.496 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.361 x V_{SUP}, V_{SUP} = 4.5 V to 7 V, t_{BIT} = 50 µs D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See 图 8-8 and 图 8-9			0.581	
D2	Duty cycle 2(1) (2) (6)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 52 µs D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See 图 8-8 and 图 8-9			0.581	
D3	Duty cycle 3(3) ISO 17987 Param 29	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See 图 8-8 and 图 8-9	0.417			
D3	Duty cycle 3(3) (6)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP} $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} V_{SUP} = 4.5 V to 7 V, t_{BIT} = 96 µs D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See 图 8-8 and 图 8-9	0.417			
D3	Duty cycle 3(1) (2) (6)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) See 图 8-8 and 图 8-9	0.417			

7.7 Electrical Characteristics (continued)

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D4	Duty cycle 4[3] ISO 17987 Param 30	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See 图 8-8 and 图 8-9			0.59	
D4	Duty cycle 4[3] [6]	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 4.5 V to 7 V, t_{BIT} = 96 µs D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See 图 8-8 and 图 8-9			0.59	
D4	Duty cycle 4[1] [2] [6]	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) See 图 8-8 and 图 8-9			0.59	
$D1_{LB}$	Duty cycle 1 at low battery[1] [2] [6]	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 52 µs	0.396			
$D2_{LB}$	Duty cycle 2 at low battery[1] [2] [6]	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 6.1 V to 7 V, t_{BIT} = 52 µs			0.581	
$D3_{LB}$	Duty cycle 3 at low battery[1] [2] [6]	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 96 µs	0.396			
D_{4LB}	Duty cycle 4 at low battery[1] [2] [6]	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 6.1 V to 7 V, t_{BIT} = 96 µs			0.581	
$T_{r\text{-}d\ max}$	Transmitter propagation delay timings for the duty cycle[1] [2] [6] Recessive to dominant	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 52 µs $t_{REC(MAX)\_D1}$ - $t_{DOM(MIN)\_D1}$			10.8	µs
$T_{d\text{-}r\ max}$	Transmitter propagation delay timings for the duty cycle[1] [2] [6] Dominant to recessive	$TH_{REC(MAX)}$ = 0.422 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.284 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 52 µs $t_{DOM(MAX)\_D2}$ - $t_{REC(MIN)\_D2}$			8.4	µs
$T_{r\text{-}d\ max}$	Transmitter propagation delay timings for the duty cycle[1] [2] [6] Recessive to dominant	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 96 µs $t_{REC(MAX)\_D3}$ - $t_{DOM(MIN)\_D3}$			15.9	µs
$T_{d\text{-}r\ max}$	Transmitter propagation delay timings for the duty cycle[1] [2] [6] Dominant to recessive	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 96 µs $t_{DOM(MAX)\_D4}$ - $t_{REC(MIN)\_D4}$			17.28	µs
$T_{r\text{-}d\ max\_low}$	Low battery transmitter propagation delay timings for the duty cycle[1] [2] [6] Recessive to dominant	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} 5.5 V ≤ V_{SUP} ≤ 7 V, t_{BIT} = 52 µs $t_{REC(MAX)\_low}$ - $t_{DOM(MIN)\_low}$			10.8	µs
$T_{d\text{-}r\ max\_low}$	Low battery transmitter propagation delay timings for the duty cycle[1] [2] [6] Dominant to recessive	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} 6.1 V ≤ V_{SUP} ≤ 7 V, t_{BIT} = 52 µs $t_{DOM(MAX)\_low}$ - $t_{REC(MIN)\_low}$			8.4	µs

(1) SAE 2602 commander node load conditions: 5.5 nF/4 kΩ and 899 pF/20 kΩ
(2) SAE 2602 responder node load conditions: 5.5 nF/875 Ω and 899 pF/900 Ω
(3) ISO 17987 bus load conditions (C_{LINBUS}, R_{LINBUS}) include 1 nF/1 kΩ; 6.8 nF/660 Ω; 10 nF/500 Ω.
(4) RXD uses open drain output structure therefore V_{OL} level is based upon microcontroller supply voltage.
(5) $I_{leak\ gnd}$ = (V_{BAT} - V_{LIN})/R_{Load}
(6) Specified by design

7.8 AC Switching Characteristics

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
t_{rx_pdr}	Receiver rising propagation delay time ISO 17987 Param 31	4.5 V ≤ VSUP < 5.5 V, R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF See 图 8-10 and 图 8-11			6	µs
t_{rx_pdf}	Receiver falling propagation delay time ISO 17987 Param 31				6	µs
t_{rx_pdf}	Receiver falling propagation delay time ISO 17987 Param 31	5.5 V ≤ VSUP, R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF See 图 8-10 and 图 8-11			5	µs
t_{rx_pdf}	Receiver falling propagation delay time ISO 17987 Param 31				5	µs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time ISO 17987 Param 32	Rising edge with respect to falling edge $t_{rx\_sym} = t_{rx\_pdf} - t_{rx\_pdr}$), R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF See 图 8-10 and 图 8-11	–2		2	µs
t_{LINBUS}	Minimum dominant time on LIN bus for wake-up	See 图 8-14, 图 9-2 and 图 9-3	25	65	150	µs
t_{CLEAR}	Time to clear false wake-up prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See 图 9-3	8	25	50	µs
t_{MODE_CHANGE}	Mode change delay time	Time to change from normal mode to sleep mode through EN pin See 图 8-12	2		15	µs
t_{NOMINT}	Normal mode initialization time(1)	Time for normal mode to initialize and data on RXD pin to be valid, includes t_{MODE_CHANGE} for standby to normal mode. See 图 8-12			45	µs
t_{PWR}	Power-up time	Time it takes for valid data on RXD upon power-up			1.5	ms
t_{TXD_DTO}	Dominant state time out		20	50	80	ms

(1) The transition time from sleep mode to normal mode includes both t_{MODE_CHANGE} and t_{NOMINT}.

7.9 Typical Curves

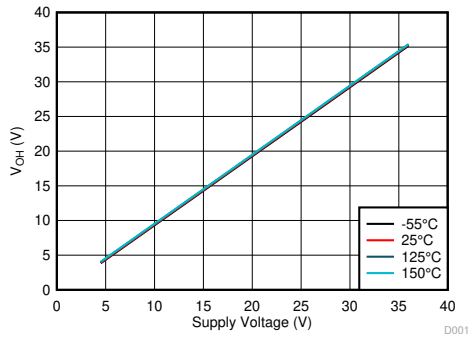


图 7-1. V_{OH} vs V_{SUP} and Temperature

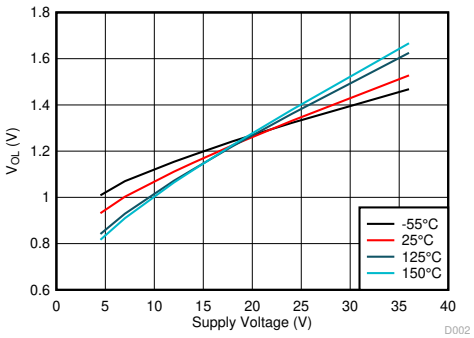


图 7-2. V_{OL} vs V_{SUP} and Temperature

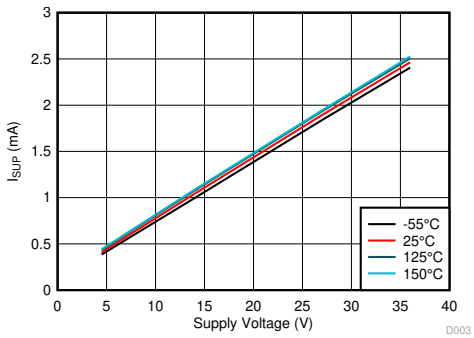


图 7-3. Normal mode I_{SUP} dominant vs V_{SUP} and Temperature

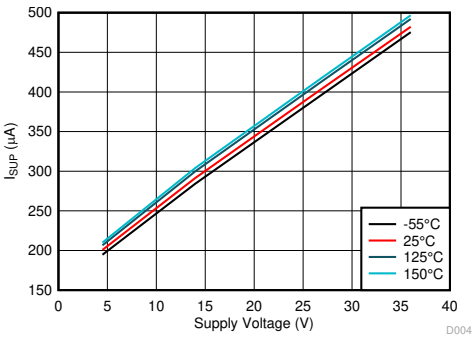


图 7-4. Normal mode I_{SUP} recessive vs V_{SUP} and Temperature

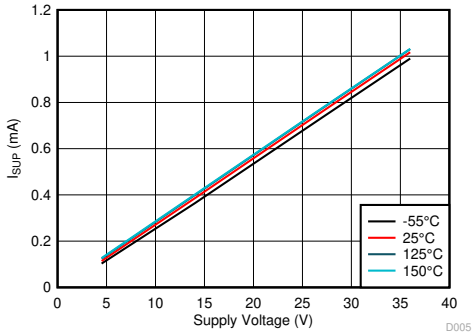


图 7-5. Standby mode I_{SUP} dominant vs V_{SUP} and Temperature

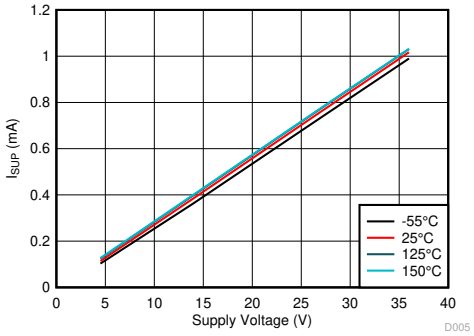


图 7-6. Standby mode I_{SUP} recessive vs V_{SUP} and Temperature

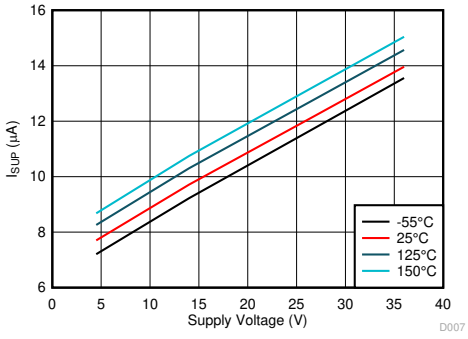


图 7-7. Sleep mode I_{SUP} vs V_{SUP} and Temperature

8 Parameter Measurement Information

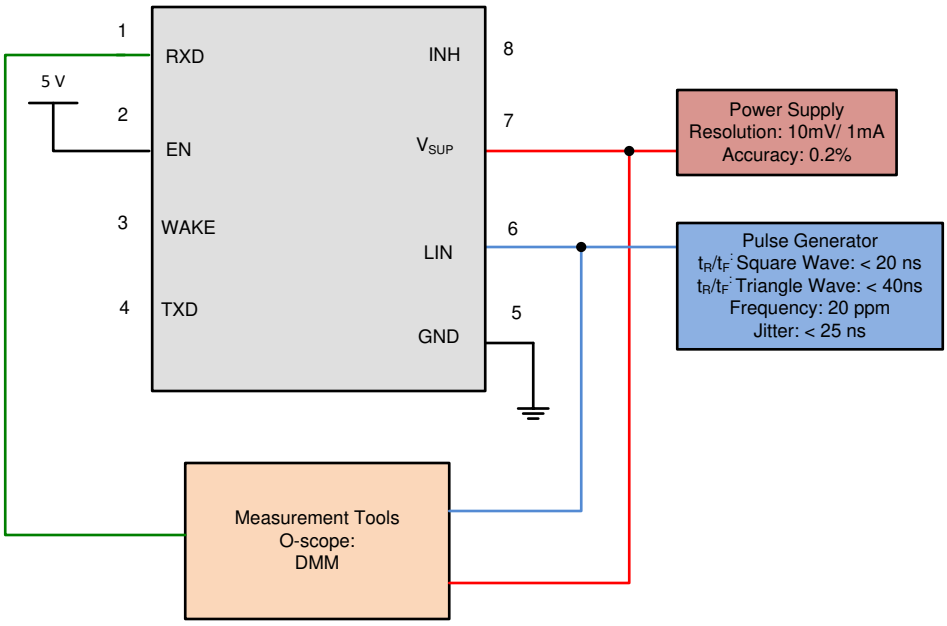


图 8-1. Test System: Operating Voltage Range with RX and TX Access: Parameters 9, 10

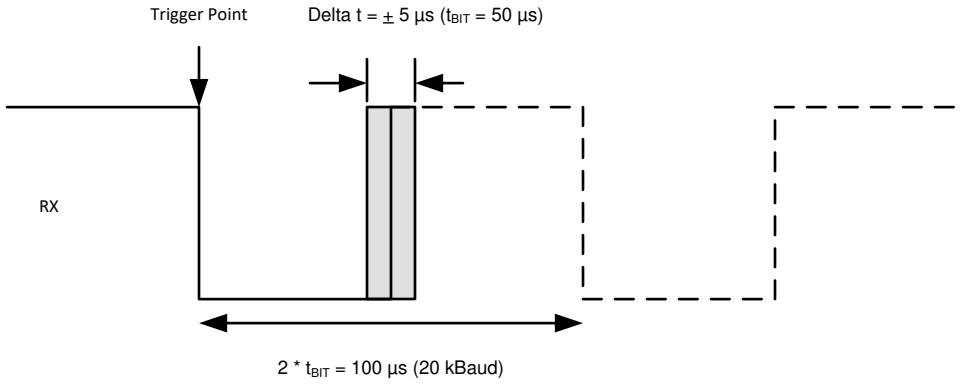


图 8-2. RX Response: Operating Voltage Range

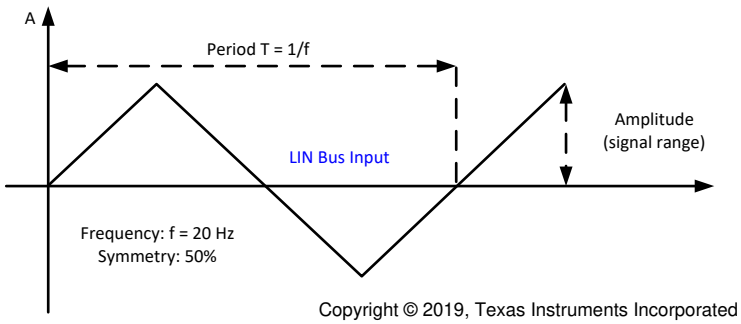


图 8-3. LIN Bus Input Signal

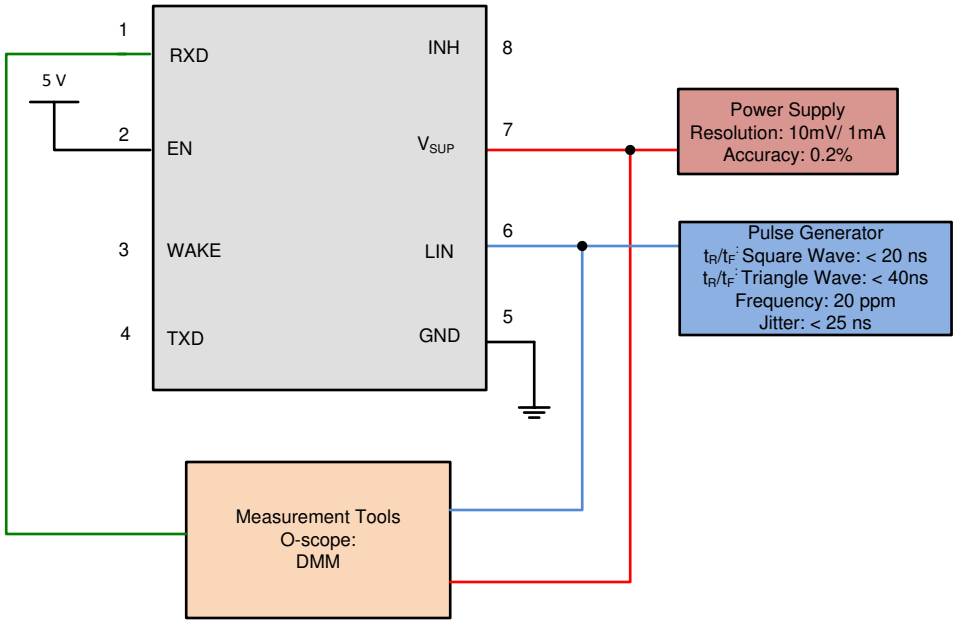


图 8-4. LIN Receiver Test with RX access Param 17, 18, 19, 20

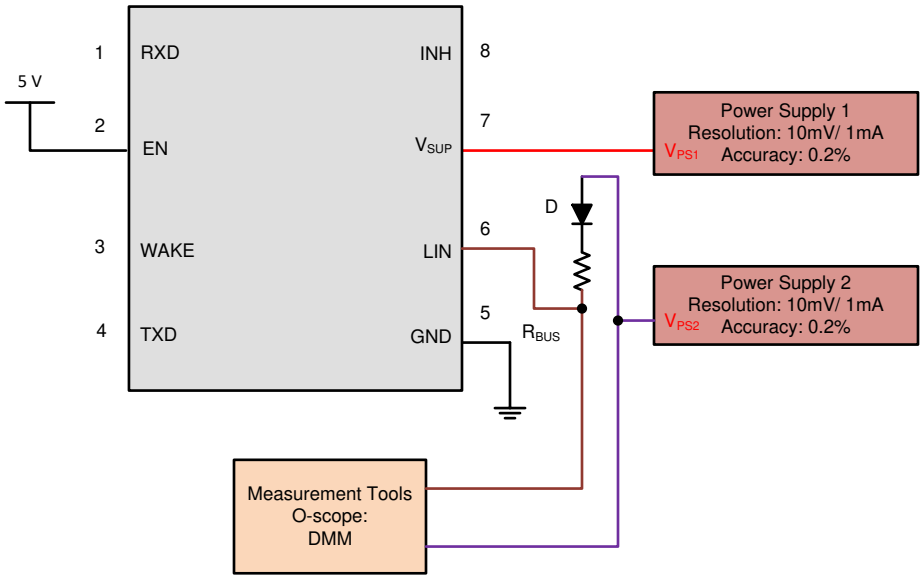


图 8-5. $V_{SUP\_NON\_OP}$ Param 11

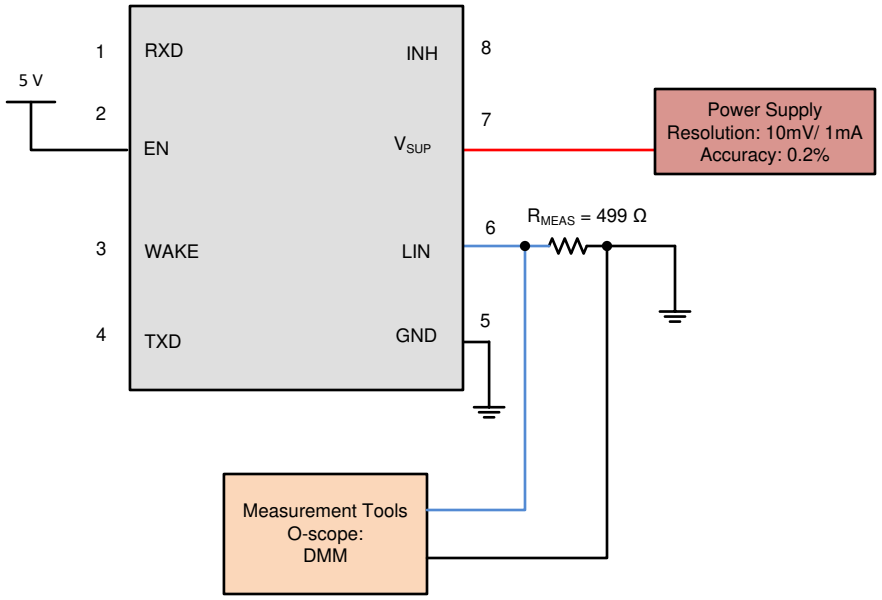


图 8-6. Test Circuit for $I_{BUS\_PAS\_dom}$; TXD = Recessive State V_{BUS} = 0 V, Param 13

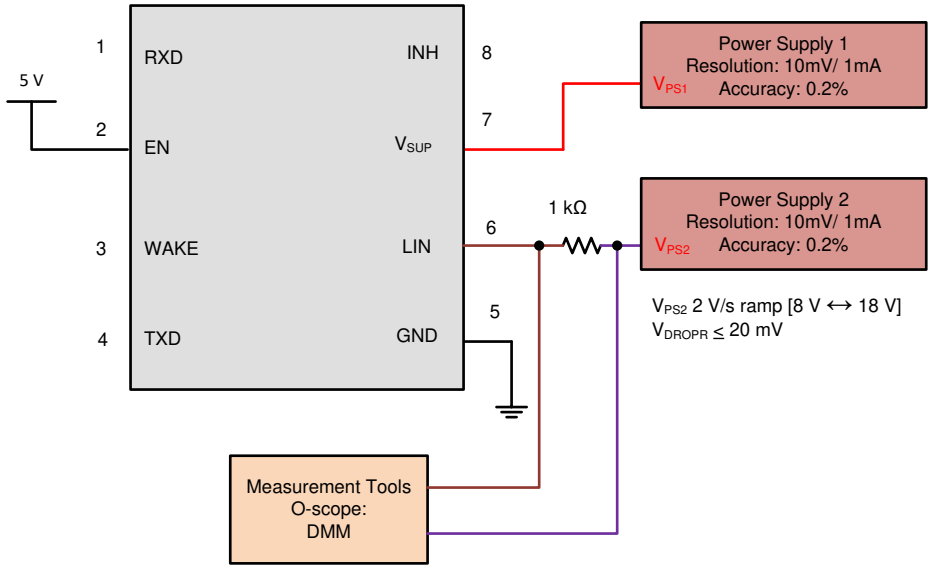


图 8-7. Test Circuit for $I_{BUS\_PAS\_rec}$ Param 14

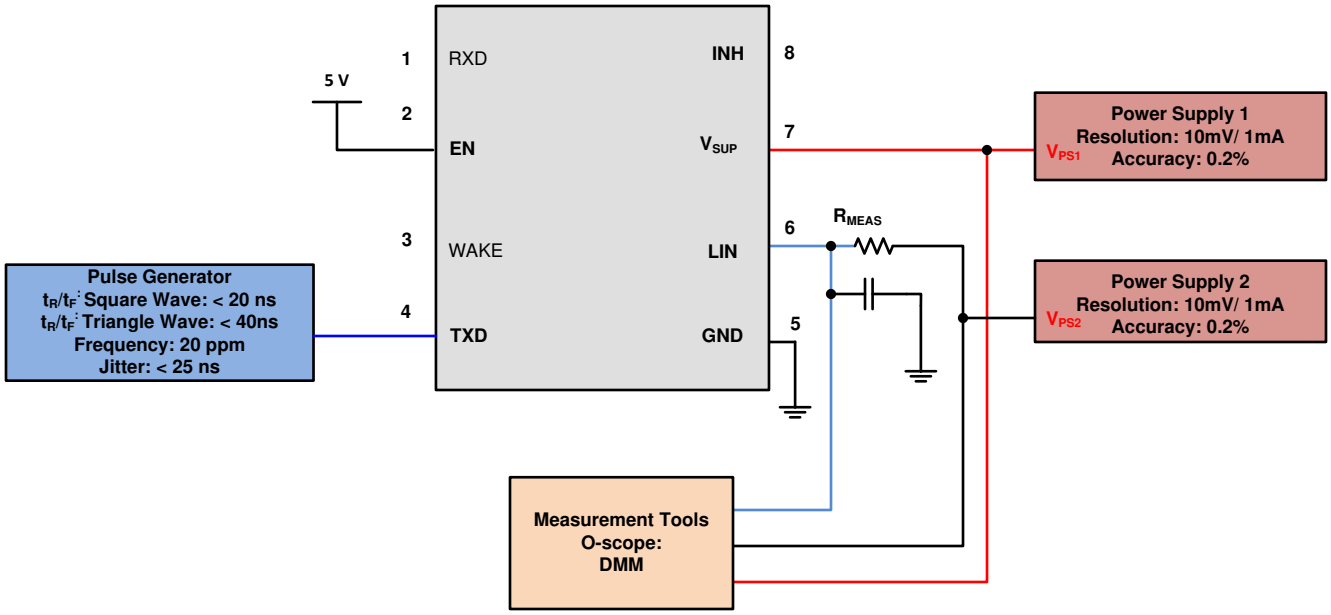


图 8-8. Test Circuit Slope Control and Duty Cycle Param 27, 28, 29, 30

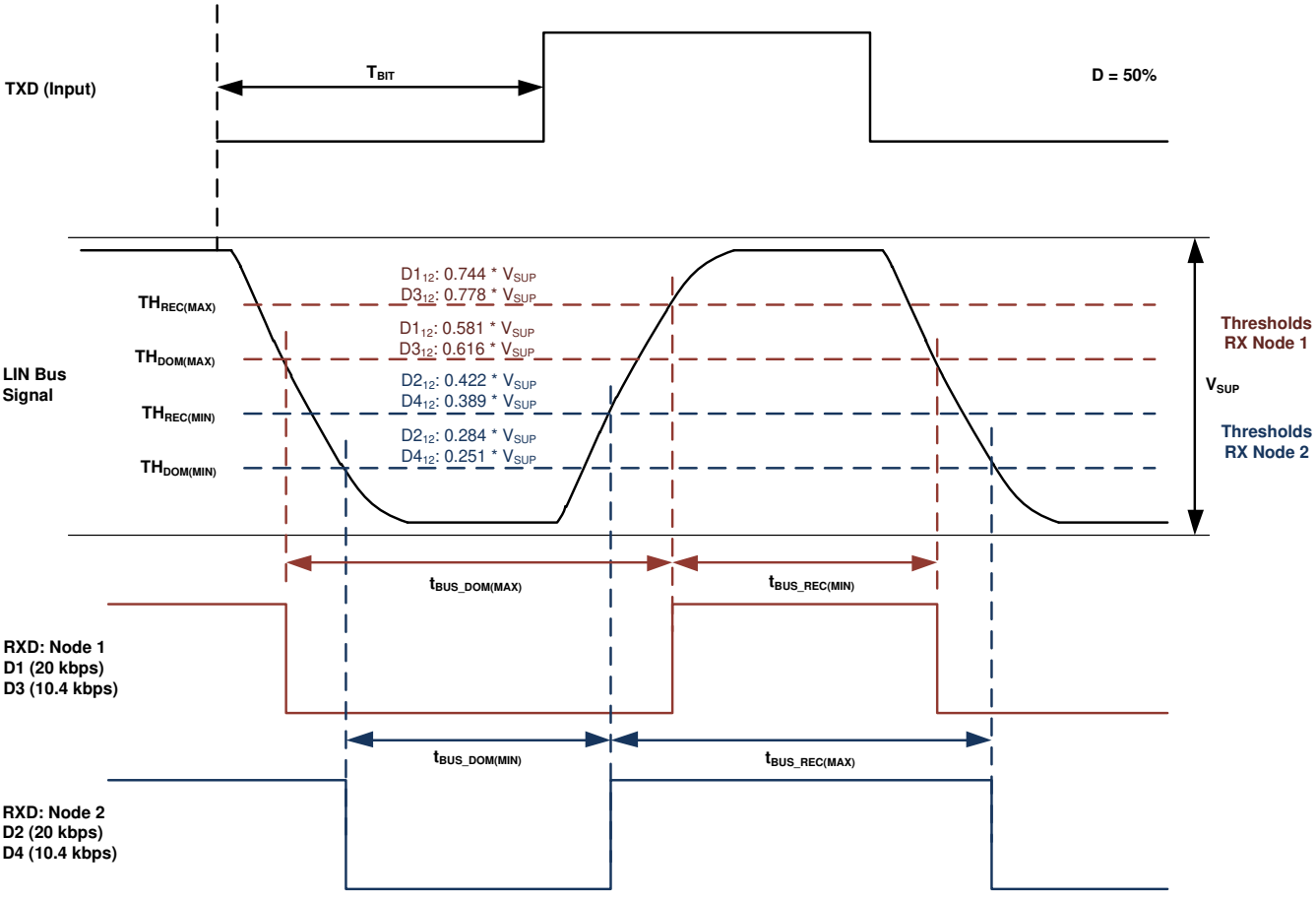


图 8-9. Definition of Bus Timing Parameters

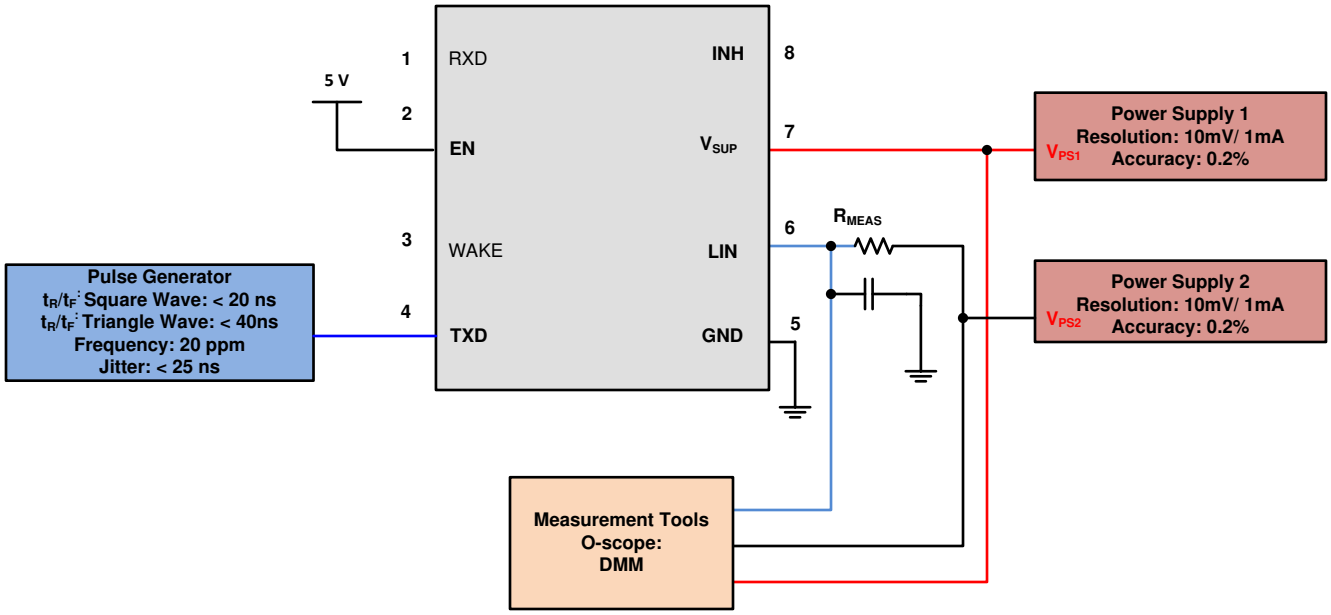


图 8-10. Propagation Delay Test Circuit; Param 31, 32

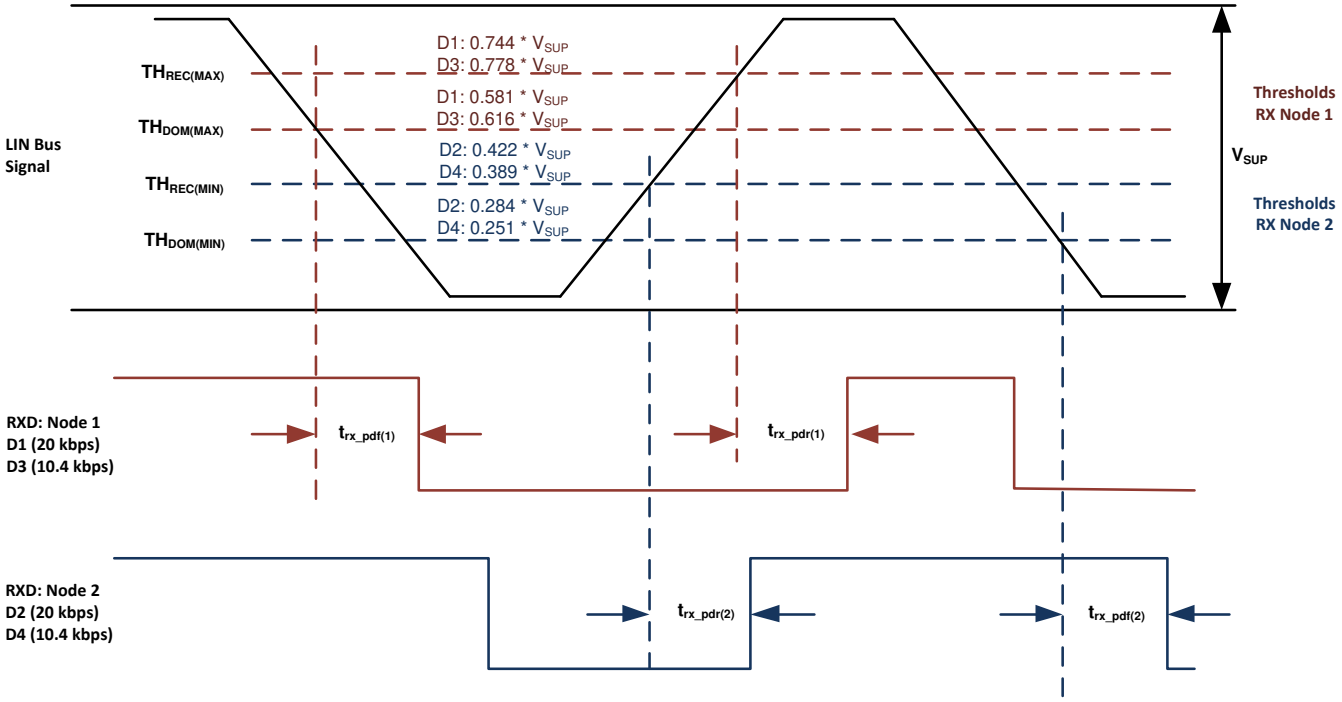


图 8-11. Propagation Delay

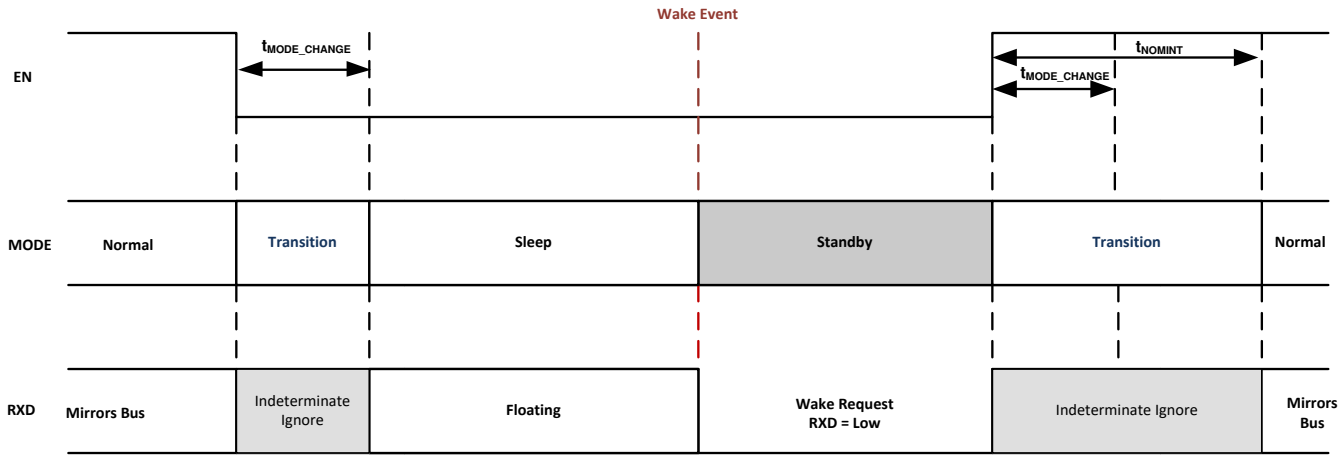


图 8-12. Mode Transitions

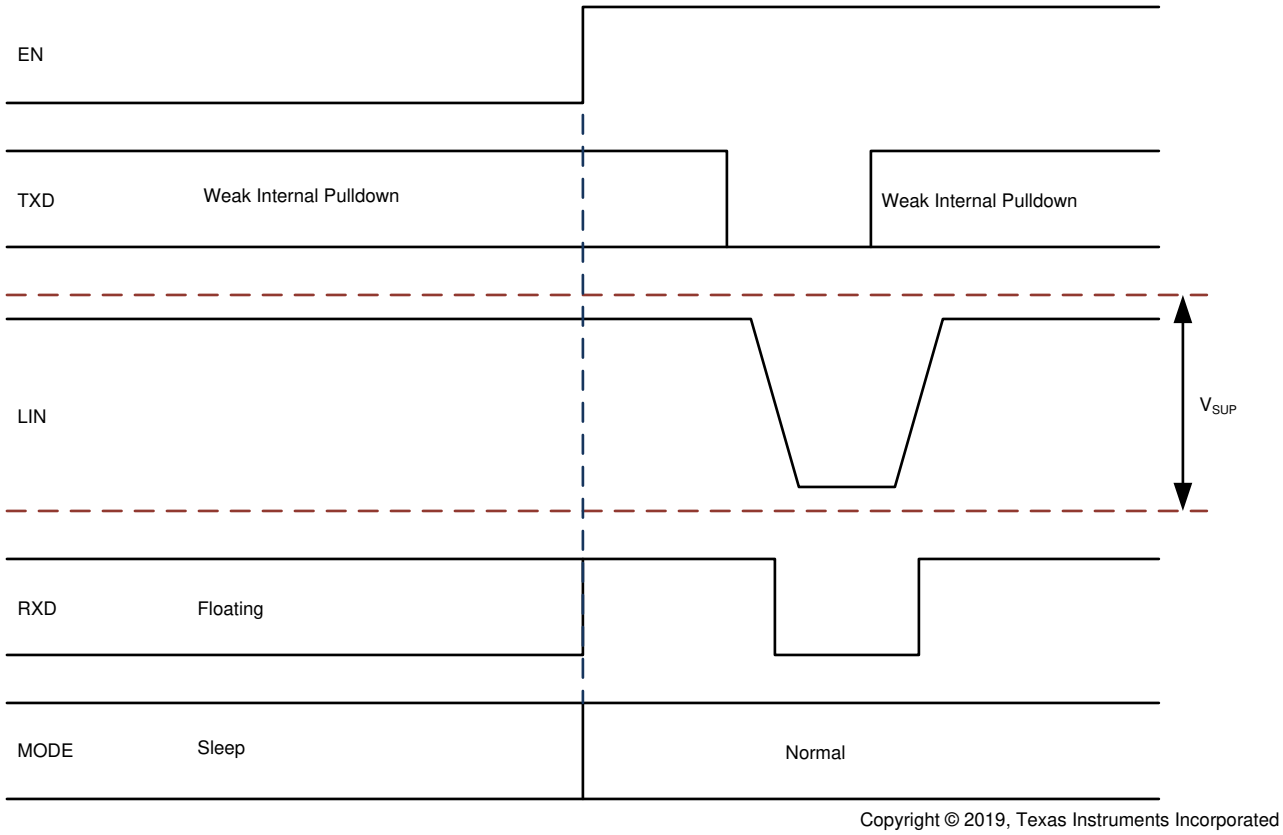


图 8-13. Wake-up Through EN

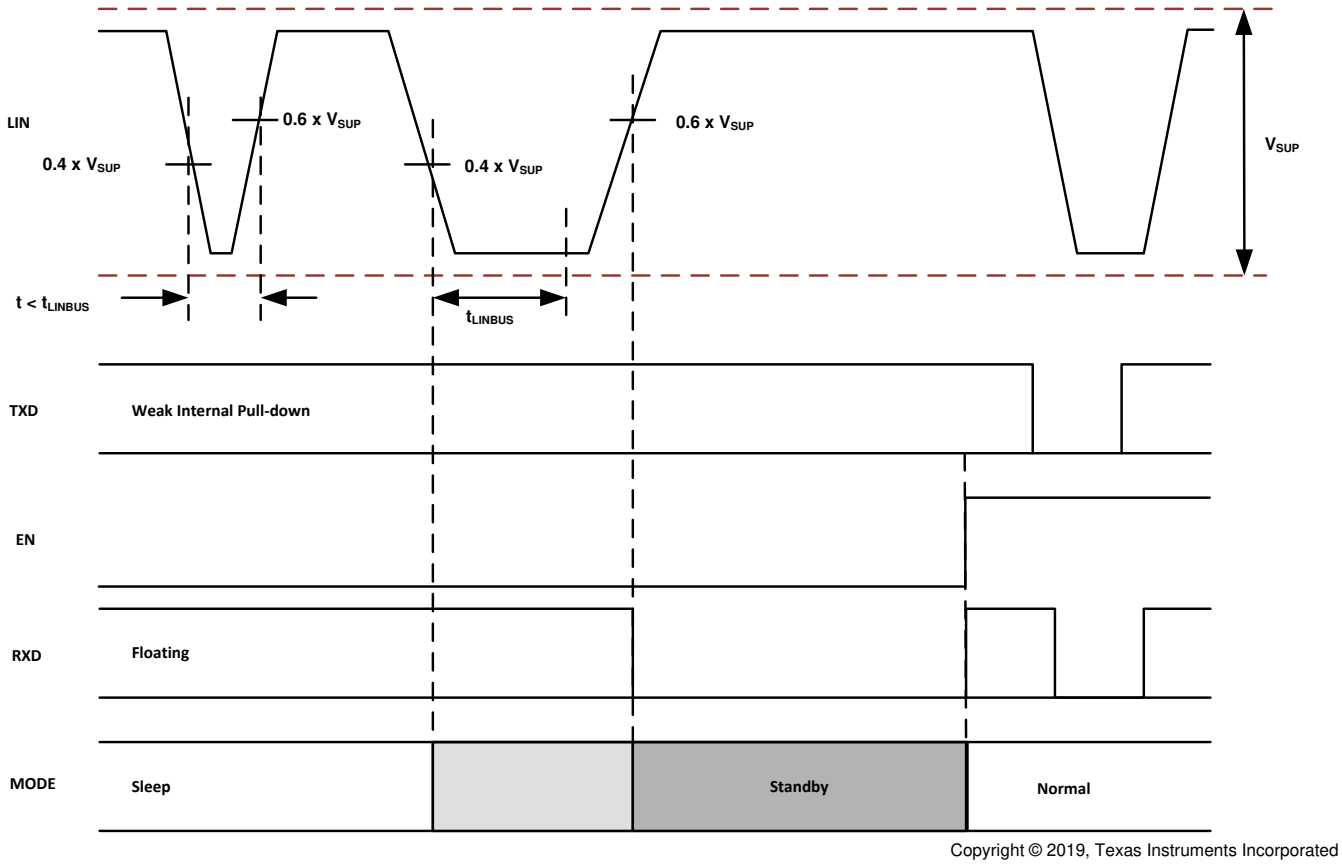


图 8-14. Wake-up through LIN

9 Detailed Description

9.1 Overview

The TLIN1021A-Q1 is a local interconnect network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, SAE J2602-1, SAE J2602-2, ISO 17987 – 4, and ISO 17987 – 7 standards. LIN is a low-speed universal asynchronous receiver transmitter (UART) communication protocol focused on automotive in-vehicle networking.

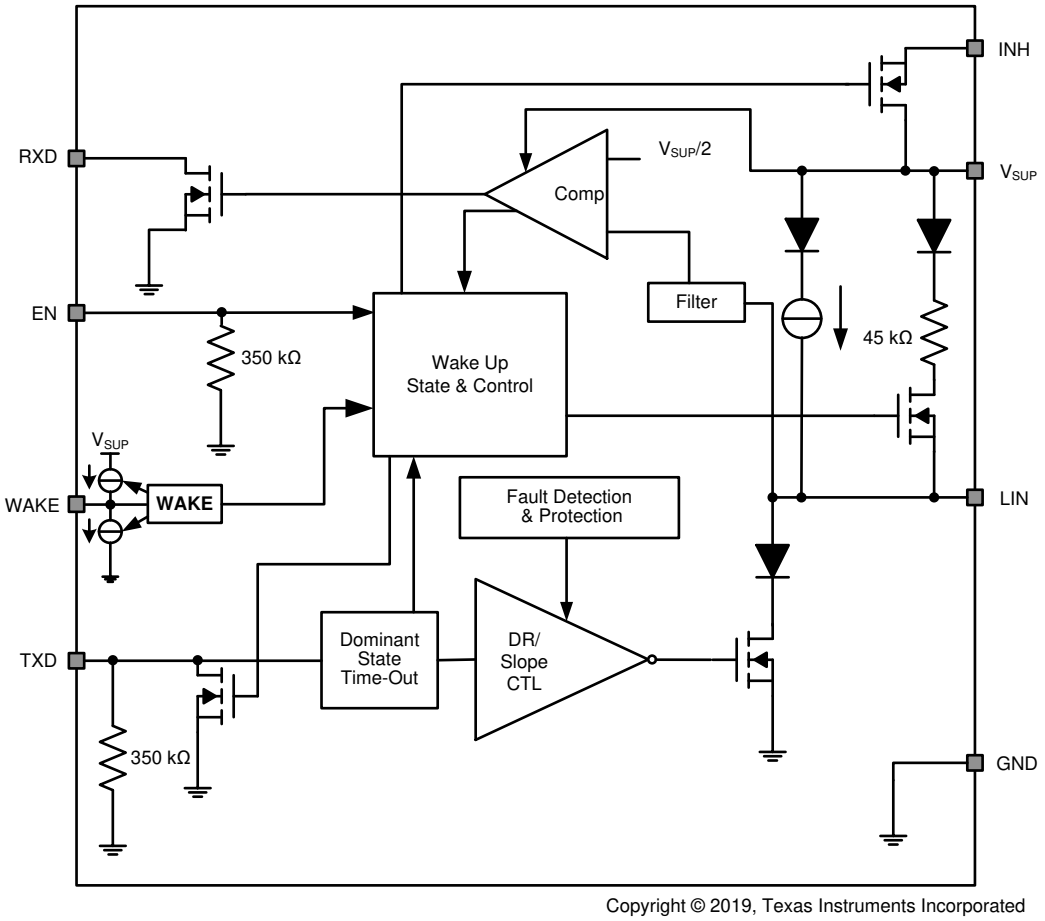
The device transmitter supports data rates from 2.4-kbps to 20-kbps and the receiver supports data rates up to 100-kbps for end-of-line programming. The device controls the state of the LIN bus through the TXD pin and reports the state of the bus through its open-drain RXD output pin. The LIN protocol data stream on the TXD input is converted by the device into a LIN bus signal using an optimized electromagnetic emissions current-limited wave-shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic-level signals that are sent to the microcontroller through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the transceivers internal pull-up resistor (45-kΩ) and a series diode. No external pull-up components are required for responder node applications. Commander node applications require an external pull-up resistor (1-kΩ) as well as a series diode per the LIN specification.

The device is designed to support 12-V applications with a wide input voltage operating range and also supports low-power sleep mode. The device supports wake-up from low-power mode via wake over LIN, the WAKE pin, or the EN pin. The device allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that may be present on a node through the INH output pin.

The TLIN1021A-Q1 integrates ESD protection and fault protection which allow for a reduction in the required external components in the applications. In the event of a ground shift or supply voltage disconnection, the device prevents back-feed current through LIN to the supply input.

The TLIN1021A-Q1 also include undervoltage detection, temperature shutdown protection, and loss-of-ground protection. In the event of a fault condition, the transmitter is immediately switched off and remains off until the fault condition is removed.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 LIN

This high voltage input/output pin is the single-wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 45-V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

9.3.1.1 LIN Transmitter Characteristics

The LIN transmitter has thresholds and AC switching parameters according to the LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for LIN responder node applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used for in a commander node application per the LIN specification.

9.3.1.2 LIN Receiver Characteristics

The receiver characteristic thresholds are proportional to the device supply pin in accordance to the LIN specification.

The receiver is capable of receiving higher data rates, > 100 kbps, than supported by LIN or SAEJ2602 specifications. This allows the TLIN1021A-Q1 to be used for high-speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

9.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor (1-kΩ) and a series diode to V_{SUP} must be added when the device is used for commander node applications as per the LIN specification.

图 9-1 shows a commander node configuration and how the voltage levels are defined

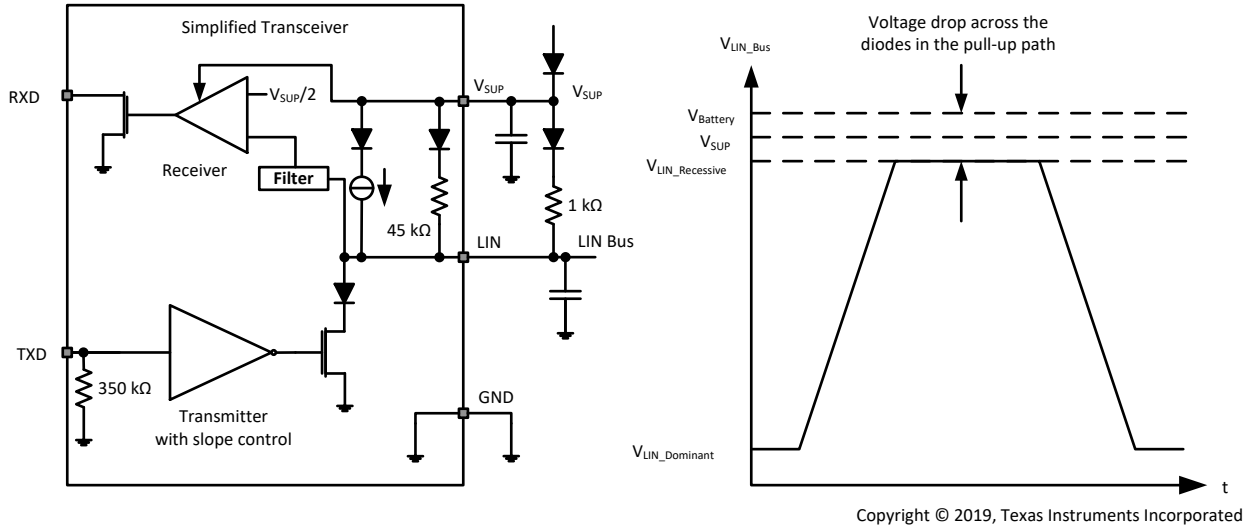


图 9-1. Commander Node Configuration with Voltage Levels

9.3.2 TXD

TXD is the interface to the MCU LIN protocol controller or SCI and UART that is used to control the state of the LIN output. When TXD is low the LIN output is dominant (near ground) and when TXD is high the LIN output is recessive (near V_{SUP}), see 图 9-1.

The TXD input structure is compatible with 3.3-V and 5-V microcontrollers and integrates a weak pull-down resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state timer-out timer. When a change of state on the WAKE pin initiates a local wake-up event, the TXD pin is pulled hard to ground indicating a local wake-up event. The hard pull to ground is released upon the rising edge on the EN pin. If an external pull-up resistor is added to the TXD pin to the microcontollers IO voltage then TXD is pulled high to indicate a remote wake-up event.

9.3.3 RXD

RXD is the interface to the MCU’s LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near V_{SUP}) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3-V and 5-V microcontrollers. If the microcontrollers RXD pin does not have an integrated pull-up, an external pull-up resistor to the microcontrolers IO supply voltage is required. In standby mode, the RXD pin is driven low to indicate a wake-up request.

9.3.4 V_{SUP}

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse-blocking diode, see 图 9-1. If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.5 GND

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the

device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.6 EN

EN controls the operational modes of the device. When EN is high the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low, the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake-up. EN has an internal pull-down resistor to ensure the device remains in low power mode even if EN floats.

9.3.7 WAKE

The WAKE pin is a high-voltage input used for the local wake-up (LWU) function. This function is explained further in 节 9.4.4.1 section. The pin is defaulted to bidirectional edge trigger, meaning it recognizes a local wake-up (LWU) on a rising or falling edge of WAKE pin transition.

9.3.8 INH

The TLIN1021A-Q1 inhibit, INH, output pin can be used to control the enable of system power-management devices allowing for a significant reduction in battery quiescent current consumption while the application is in sleep mode. The INH pin has two states: driven high and high impedance. When the INH pin is driven high, the terminal shows V_{SUP} minus a diode voltage drop. In the high impedance state the output is left floating. The INH pin is high in the normal and standby modes and is low when in sleep mode. A 100 kΩ load can be added to the INH output to ensure a fast transition time from the driven high state to the low state and to also force the pin low when left floating.

The INH terminal should be considered a high-voltage logic terminal and not a power output. Thus should be used to drive the EN terminal of the systems power-management device and not used as a switch for the power-management supply itself. This terminal is not reverse battery protected and thus should not be connected outside the system module.

9.3.9 Local Faults

The TLIN1021A-Q1 has several protection features that are described as follows.

9.3.10 TXD Dominant Time-Out (DTO)

While the LIN driver is in active mode a TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time-out period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time-out constant of the circuit, t_{TXD_DTO}, expires the LIN driver is disabled releasing the bus line to the recessive level. This keeps the bus free for communication between other nodes on the network. The LIN driver is re-activated on the next dominant to recessive transition on the TXD terminal, thus clearing the dominant time-out. During this fault, the transceiver remains in normal mode, the integrated LIN bus pull-up termination remains on, and the LIN receiver and RXD terminal remain active reflecting the LIN bus data.

The TXD pin has an internal pull-down to ensure the device fails to a known state if TXD is disconnected. If EN pin is high at power-up, the TLIN1021A-Q1 enters normal mode. With the internal TXD connected low, the DTO timer starts. To avoid a t_{TXD_DTO} fault, a recessive signal should be put onto the TXD pin before the t_{TXD_DTO} timer expires, or the device should be into sleep mode by connecting EN pin low.

9.3.11 Bus Stuck Dominant System Fault: False Wake-Up Lockout

The TLIN1021A-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus clears the bus stuck dominant fault, preventing excessive current use, see 图 9-2 and 图 9-3.

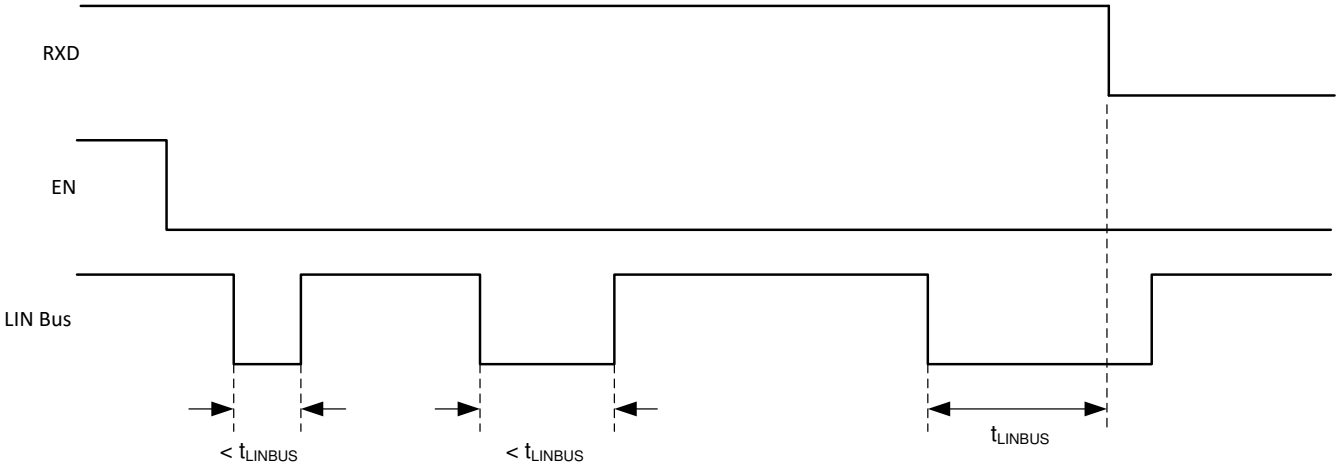


图 9-2. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wake-up

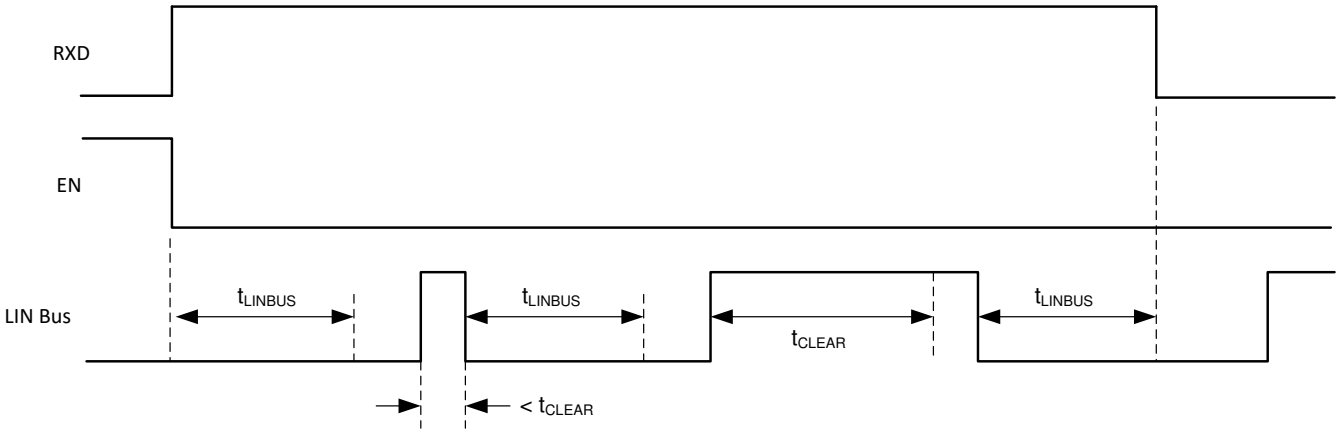


图 9-3. Bus Fault: Entering Sleep Mode With Bus Stuck Dominant Fault, Clearing, and Wake-up

9.3.12 Thermal Shutdown

The TLIN1021A-Q1 transmitter is protected by limiting the current. If the junction temperature, T_J, of the device exceeds the thermal shutdown threshold, $T_J > T_{SDR}$, the device puts the LIN transmitter into the recessive state. Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled. During this fault, the transceiver remains in normal mode, the integrated LIN bus pull-up termination remains on, the LIN receiver and RXD terminal remain active reflecting the LIN bus data.

9.3.13 Under Voltage on V_{SUP}

The device contains a power on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP}.

9.3.14 Unpowered Device

In automotive applications, some LIN nodes in a system can be unpowered, ignition supplied, while others in the network remains powered by the battery. The device has extremely low unpowered leakage current from the bus so an unpowered node does not affect the network or load it down.

9.4 Device Functional Modes

The TLIN1021A-Q1 has three functional modes of operation: normal, sleep, and standby. The next sections describe these modes and how the device transitions between the different modes. 图 9-4 graphically shows the relationship while 表 9-1 shows the state of pins.

表 9-1. Operating Modes

MODE	EN	TXD	RXD	INH	LIN BUS TERMINATION	TRANSMITTER	COMMENT
Sleep	Low	Weak pull-down	Floating	Floating	Weak current pull-up	Off	
Standby	Low	weak pull-down if LIN bus wake-up; Strong pull-down if a local wake-up event (WAKE pin)	Low	High	45-kΩ	Off	Wake-up event detected, waiting on MCU to set EN
Normal	High	High: recessive state Low: dominant state	LIN Bus Data	High	45-kΩ	On	LIN transmission up to 20 kbps

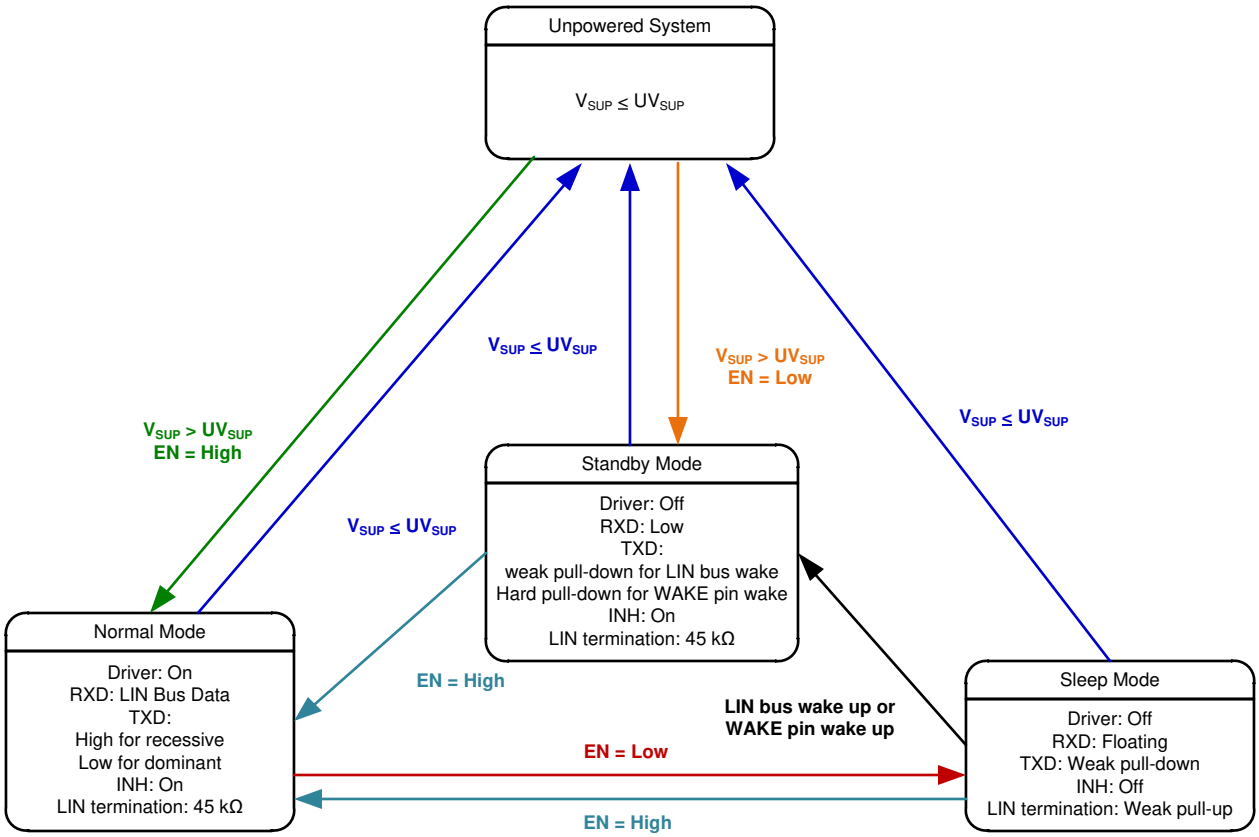


图 9-4. Operating State Diagram

9.4.1 Normal Mode

The EN pin controls the mode of the device. If the EN pin is high at power-up the device powers-up in normal mode, if the EN is low at power-up the device powers-up in standby mode. In normal mode the receiver and transmitter fully operational. The LIN transmitter transmits data from the LIN controller to the LIN bus up to the LIN specified maximum data rate of 20-kbps. The LIN receiver detects the data stream on the LIN bus up to data rates of 100-kbps and outputs the data on RXD output for the LIN controller. Upon an EN pin transition from from low to high the TLIN1021A-Q1 transitions from sleep mode to normal mode in $t \geqslant t_{NOMINT}$.

9.4.2 Sleep Mode

Sleep mode is the lowest power mode of the TLIN1021A-Q1 and is only entered from normal mode when the EN pin transitions from high to low for $t > t_{MODE\_CHANGE}$. In sleep mode, the LIN driver and receiver are switched off, the LIN bus is weakly pulled up, an the transceiver cannot send or receive data. The INH pin is switched to a floating output in sleep mode causing any system power elements controlled by the INH pin to be switched off thus reducing the system power consumption. While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off to minimize power loss if LIN is short circuited to ground.
- A weak current pull-up is active to prevent false wake-up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input, WAKE pin and LIN wake-up receiver are active.

The TLIN1021A-Q1 supports three methods for wake-up from sleep mode:

- Wake-up over the LIN bus via the LIN wake-up receiver.
- Local wake-up via the WAKE pin.
- Local wake-up via the EN pin. The EN pin must be set high for t > t_{NOMINT} in order for the device to wake-up.

9.4.3 Standby Mode

Standby mode is entered whenever a wake-up event occurs through LIN bus or the WAKE pin while the device is in sleep mode. In standby mode, the LIN bus responder termination circuit, 45-kΩ, is on. When a wake-up event occurs and the TLIN1021A-Q1 enters standby mode the RXD pin is driven low signaling the wake-up event to the LIN controller.

The TLIN1021A-Q1 exits standby mode and transitions to normal mode when the EN pin is set high for longer than t_{MODE_CHANGE} where the normal LIN transmitter and receiver are fully operational and bi-directional communication is possible.

9.4.4 Wake-Up Events

There are three ways to wake-up the TLIN1021A-Q1 from sleep mode:

- Remote wake-up initiated by the falling edge of a recessive-to-dominant state transition on the LIN bus where the dominant state is be held than t_{LINBUS} filter time. After the t_{LINBUS} filter time has been met a rising edge on the LIN bus going from dominant-to-recessive initiates a remote wake-up event. The pattern and t_{LINBUS} filter time used for the LIN wake-up prevents noise and bus stuck dominant faults from causing false wake requests.
- A local wake-up event due to the EN pin being set high for t > t_{MODE_CHANGE}.
- A local wake-up event due to a change in voltage level on the WAKE pin for t > t_{WAKE}

9.4.4.1 Local Wake-Up (LWU) via WAKE Input Terminal

The WAKE terminal is a bi-directional high-voltage input which can be used for local wake-up (LWU) requests through a voltage transition. An LWU event is triggered on either a low-to-high or high-to-low transition since it has bi-directional input thresholds. The WAKE pin can be used with a switch to V_{SUP} or to ground. If the terminal is unused, pull it to V_{SUP} or ground to avoid unwanted parasitic wake-up events. When an LWU event takes place, the TXD pin is pulled hard to GND letting the LIN controller know that the wake-up event was due to the WAKE pin and not a wake over LIN event.

The LWU circuitry is active in standby mode and sleep mode. If a valid LWU event occurs in standby mode, the device remains in standby mode and drive the RXD output low. If a valid LWU event occurs in sleep mode, the device transitions to standby mode and drive the RXD output low. The LWU circuitry is not active in normal mode. To minimize system level current consumption, the internal bias voltages of the terminal follows the state on the terminal with a delay of $t_{WAKE(MIN)}$. A constant high level on WAKE has an internal pull-up to V_{SUP}, and a constant low level on WAKE has an internal pull-down to GND.

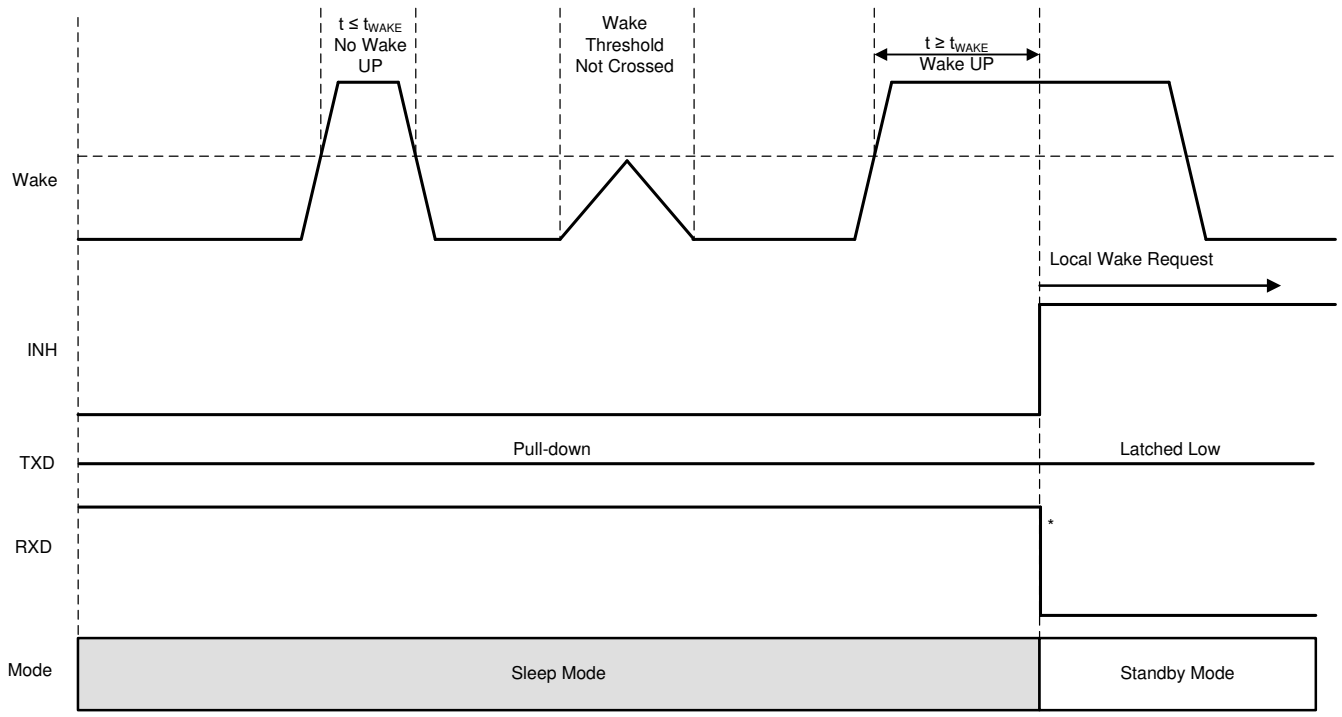


图 9-5. Local Wake-Up – Rising Edge

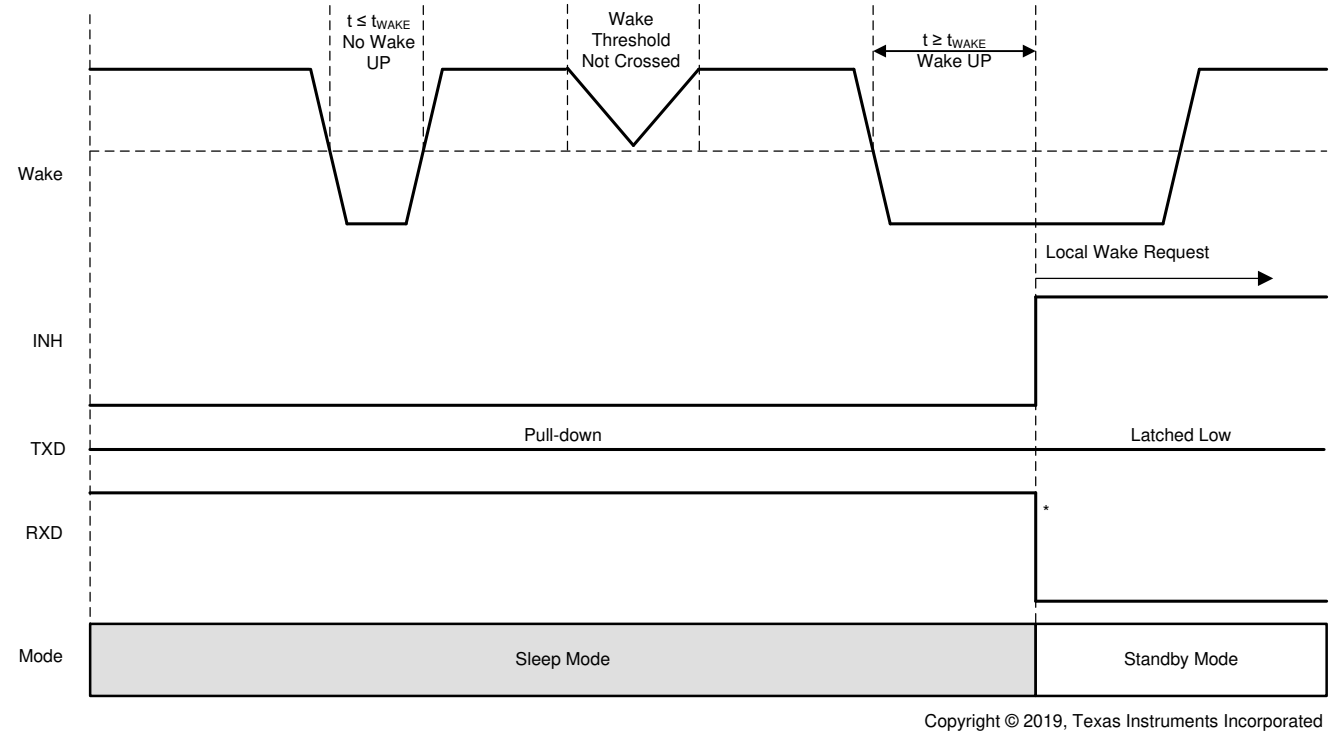


图 9-6. Local Wake-Up – Falling Edge

9.4.4.2 Wake-Up Request (RXD)

When the TLIN1021A-Q1 encounters a wake-up event from the WAKE pin, or the LIN bus the RXD output is driven low until EN is asserted high, the device enters normal mode. Once the device enters normal mode, the

wake-up event is cleared, and the RXD output is released. The RXD output is fully operation and reflects the receiver output from the LIN bus.

10 Application Information Disclaimer

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

The TLIN1021A-Q1 can be used in both a responder node application and a commander node application in a LIN network.

10.2 Typical Application

The device integrates a 45-kΩ pull-up resistor and series diode for responder node applications. For commander node applications, an external 1-kΩ pull-up resistor with series blocking diode can be used. 图 10-1 shows the device being used in both commander node and responder node applications.

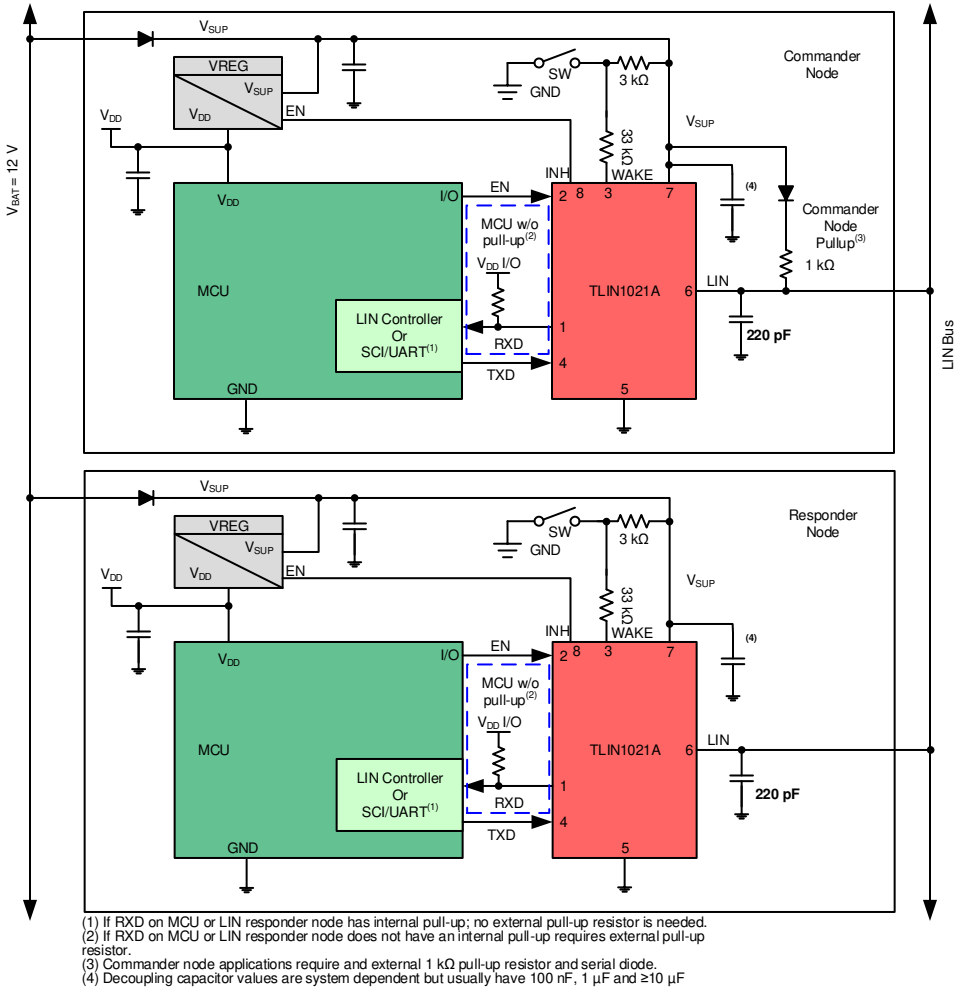


图 10-1. Typical LIN Bus

10.2.1 Design Requirements

The RXD output structure is an open-drain output stage which allows the TLIN1021A-Q1 to be used with 3.3-V and 5-V controllers. If the RXD pin of the controller does not have an integrated pull-up, an external pull-up resistor to the controllers IO voltage is required. The external pull-up resistor value should be between 1-kΩ to 10-kΩ. The V_{SUP} pin of the device should be decoupled with a 100-nF capacitor by placing it close to the V_{SUP} supply pin. The system should include additional decoupling on the V_{SUP} line as needed per the application requirements.

10.2.2 Detailed Design Procedures

10.2.2.1 Normal Mode Application Note

When using the TLIN1021A-Q1 in systems which are monitoring the RXD pin for a wake-up request, be very cautious during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake-up request until t_{MODE_CHANGE} has been met. This is shown in 图 8-12

10.2.2.2 TXD Dominant State Time-Out Application Note

The maximum dominant TXD time allowed by the TXD dominant state time-out limits the minimum possible data rate of the device. The LIN protocol has different constraints for commander node and responder node applications thus there are different maximum consecutive dominant bits for each application case thus different minimum data rates.

10.2.2.3 Standby Mode Application Note

If the TLIN1021A-Q1 detects an under voltage on V_{SUP} the RXD pin transitions low signaling to the controller that the TLIN1021A-Q1 is in standby mode. Return the transceiver to sleep mode for the lowest power state.

10.2.3 Application Curves

图 10-2 and 图 10-3 show the propagation delay from the TXD pin to the LIN pin for the dominant to recessive and recessive to dominant edges. Device was configured in commander mode with external pull-up resistor (1 kΩ) and 680 pF bus capacitance.

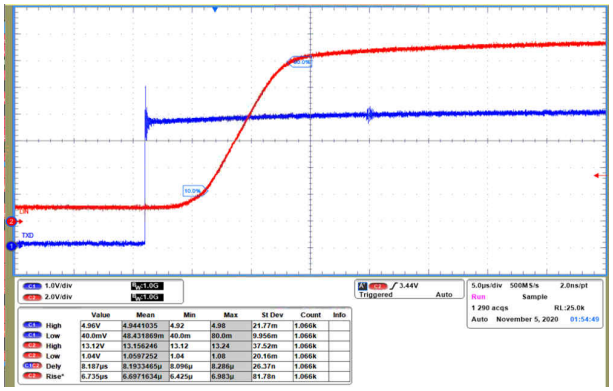


图 10-2. Dominant To Recessive Propagation Delay

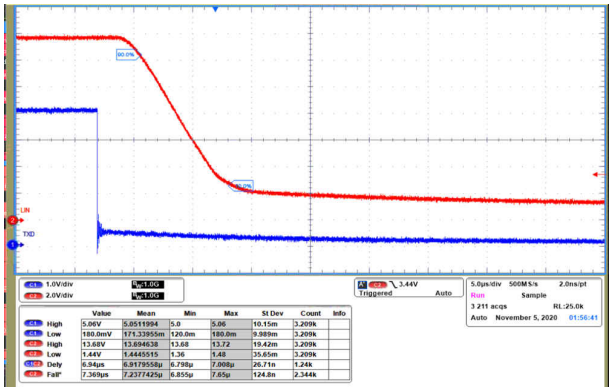


图 10-3. Recessive to Dominant Propagation Delay

11 Power Supply Recommendations

The TLIN1021A-Q1 was designed to operate directly from a car battery, or any other DC supply ranging from 4.5-V to 36-V. The V_{SUP} pin of the device should be decoupled with a 100-nF capacitor by placing it close to the V_{SUP} supply pin. The system should include additional decoupling on the V_{SUP} line as needed per the application requirements.

12 Layout

For the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

12.1 Layout Guidelines

- **Pin 1(RXD):** The RXD pin is an open-drain output and requires and external pull-up resistor in the range of 1-kΩ and 10-kΩ to function properly. If the controller paired with the transceiver does not have an integrated pull-up, place an external resistor between RXD and the supply voltage for the controller.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in low-power sleep mode. If this feature is not used, connect the pin to the supply voltage for the controller through a series resistor using a pull-up value between 1-kΩ and 10-kΩ. Additionally, a series resistor may be placed on the pin to limit current on the digital lines in the case of an over voltage fault.
- **Pin 3 (WAKE):** SW1 is oriented in a low-side configuration which is used to implement a local WAKE event. The series resistor R5 is needed for protection against over current conditions as it limits the current into the WAKE pin when the ECU has lost its ground connection. The pull-up resistor R4 is required to provide sufficient current during stimulation of a WAKE event. In this layout example R4 is set to 3-kΩ and R5 is set to 33-kΩ.
- **Pin 4 (TXD):** The TXD pin is the transmit input signal to the device from the controller. A series resistor can be placed to limit the input current to the device in the case of an over-voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to help filter noise.
- **Pin 5 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 6 (LIN):** The LIN pin connects to the TLIN1021A-Q1 to the LIN bus. For responder node applications a 220 pF capacitor to ground is implemented. For commander node applications an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin, see Typical LIN Bus.
- **Pin 7 (V_{SUP}):** This is the supply pin for the device. A 100-nF capacitor should be placed close to the V_{SUP} supply pin for local power supply decoupling.
- **Pin 8 (INH):**The INH pin is used for system power-management. A 100-kΩ load can be added to the INH output to ensure a fast transition time from the driven high state to the low state and to also force the pin low when left floating.

备注

Make all ground and power connections as short as possible and use at least two vias to minimize the total loop inductance.

12.2 Layout Example

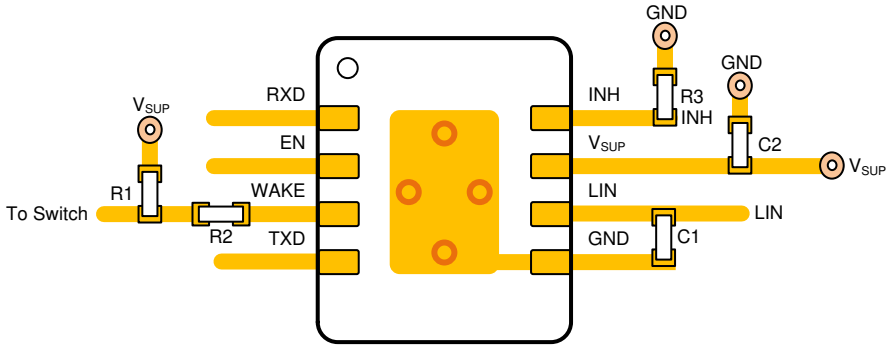


图 12-1. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLIN1021ADDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2JHF
TLIN1021ADDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JHF
TLIN1021ADRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL021A
TLIN1021ADRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL021A
TLIN1021ADRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL021A
TLIN1021ADRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL021A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

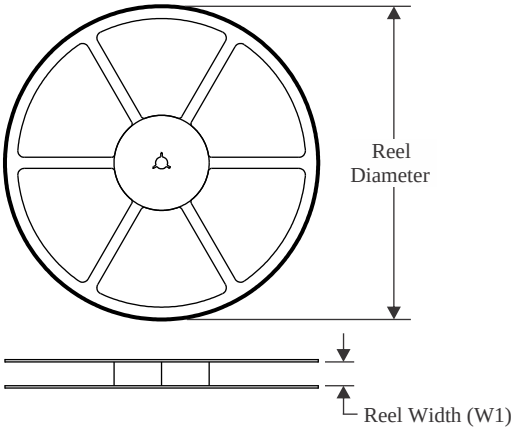
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

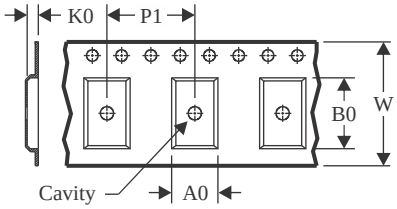
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

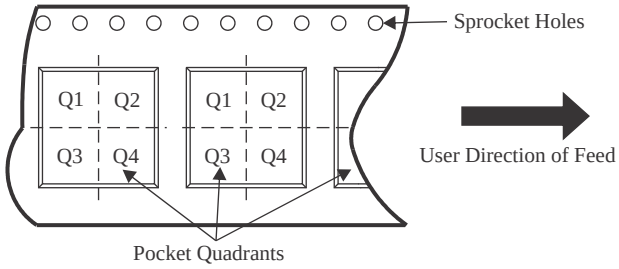


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

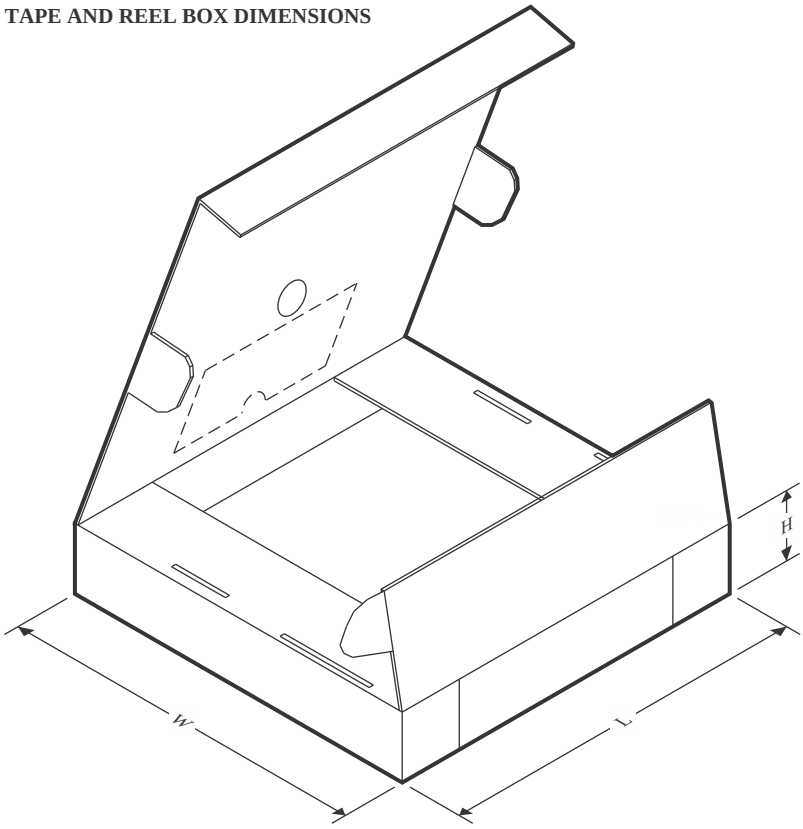
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLIN1021ADDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLIN1021ADRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TLIN1021ADRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLIN1021ADDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLIN1021ADRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLIN1021ADRQ1	SOIC	D	8	2500	353.0	353.0	32.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

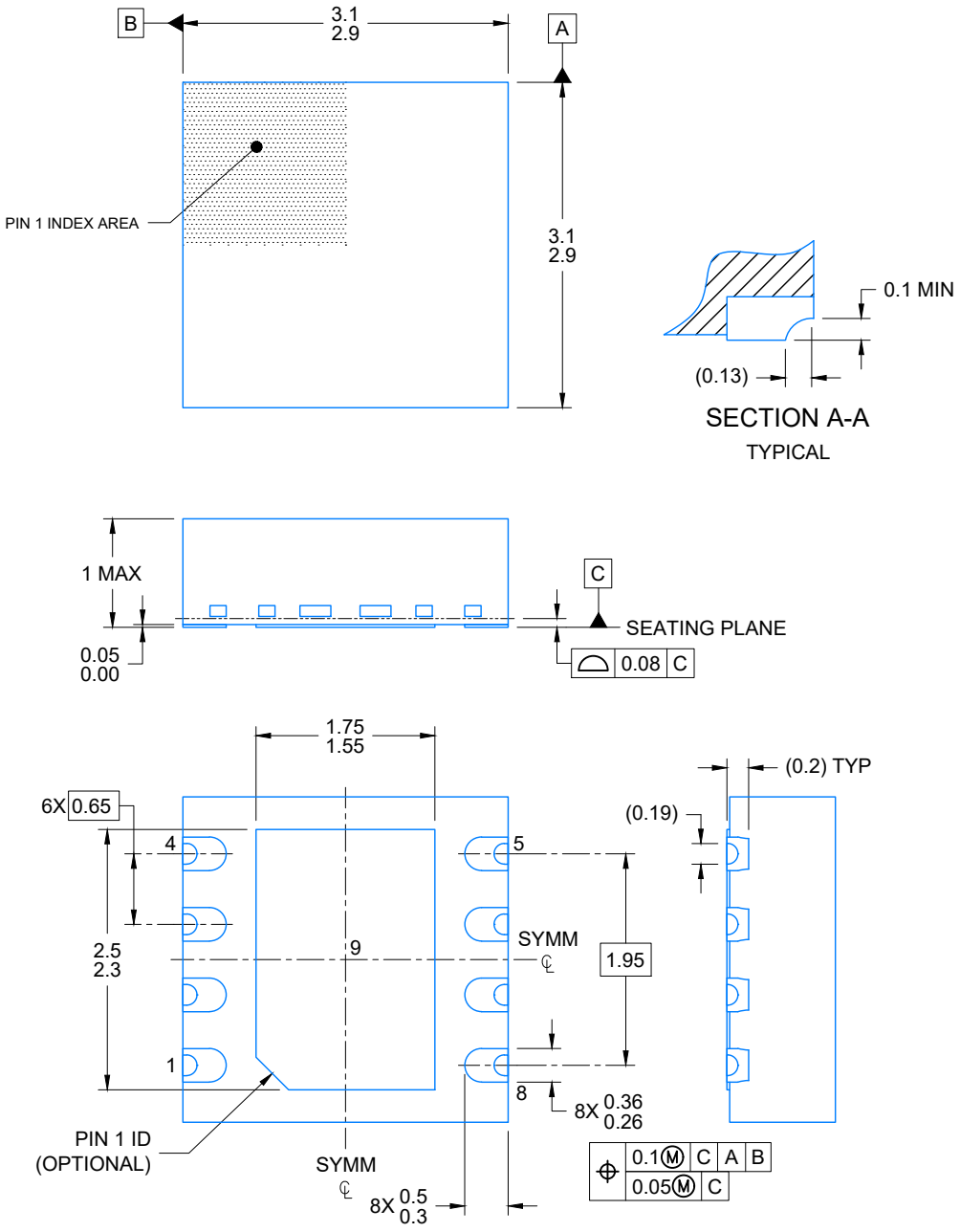
4203482/L

PACKAGE OUTLINE

DRB0008J

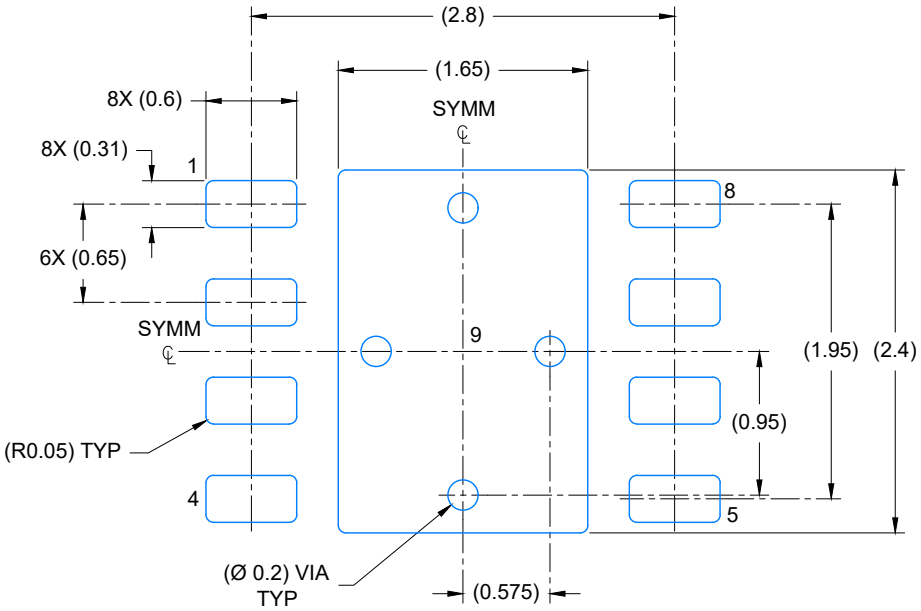
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

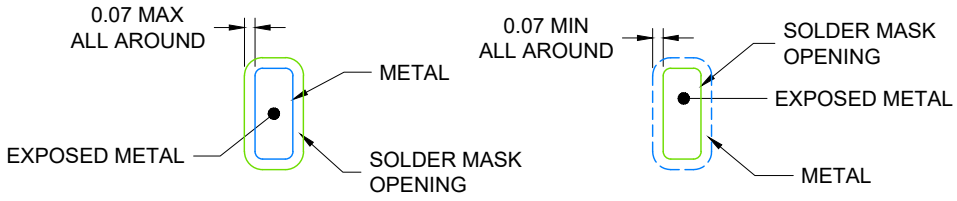


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

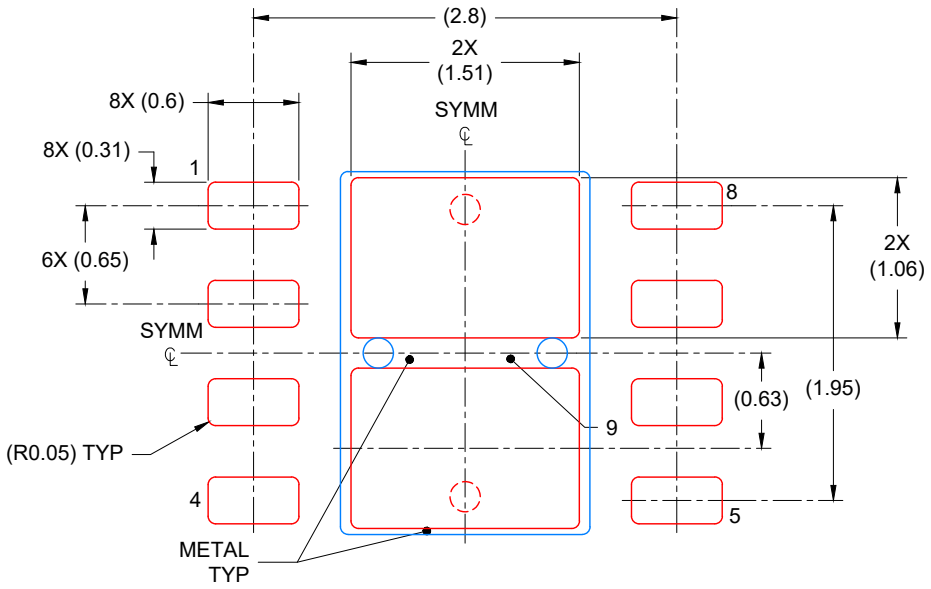
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

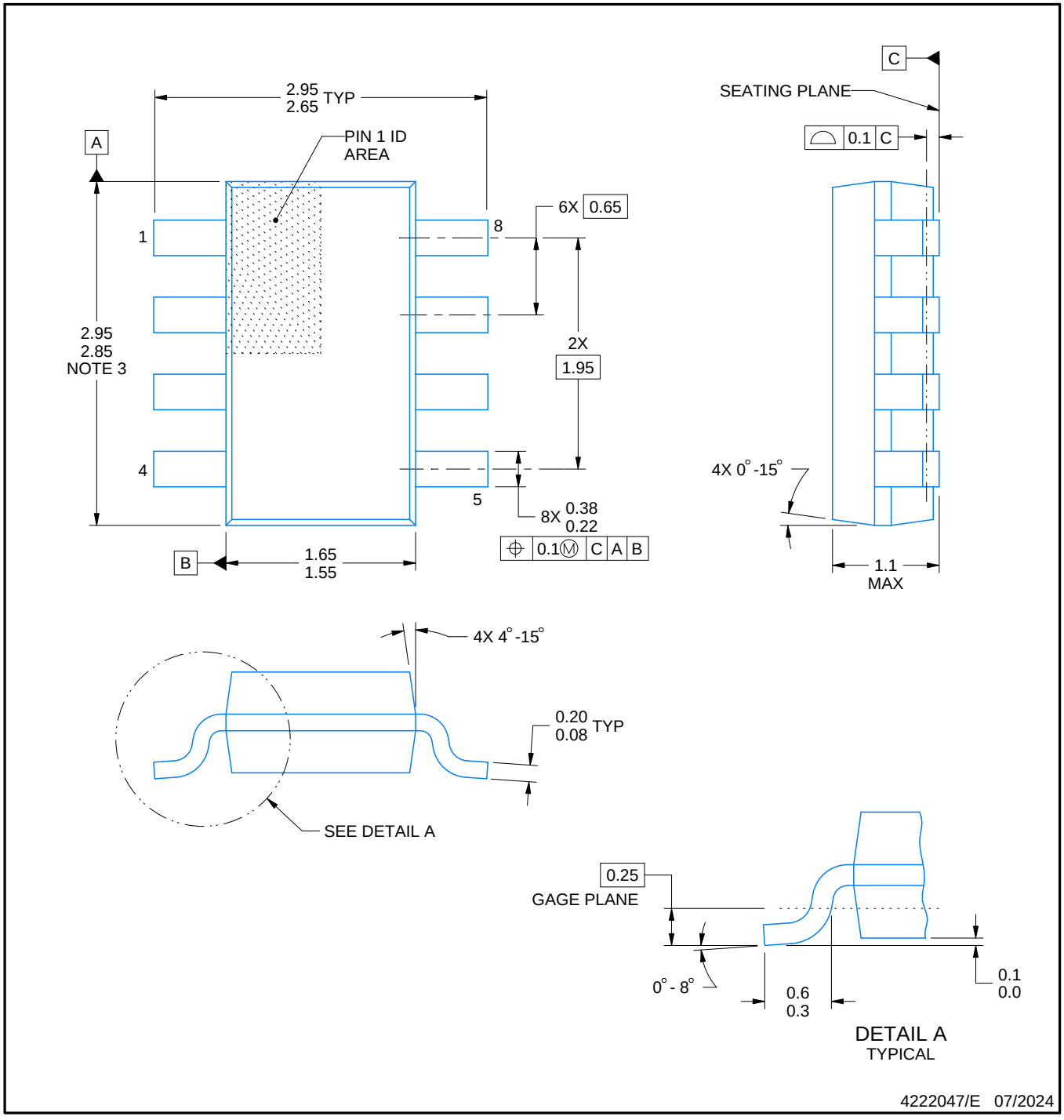
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DDF0008A

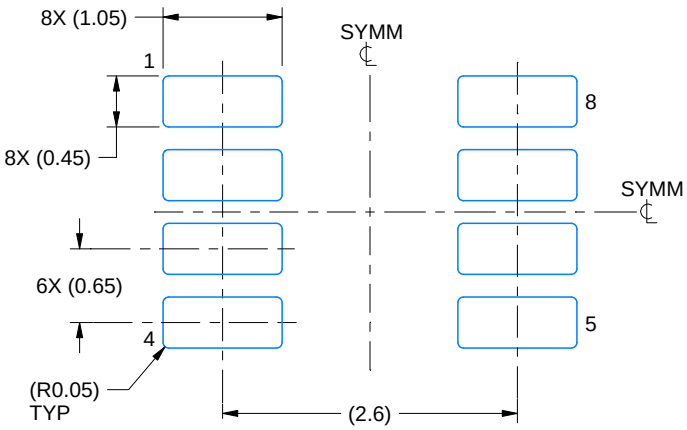
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

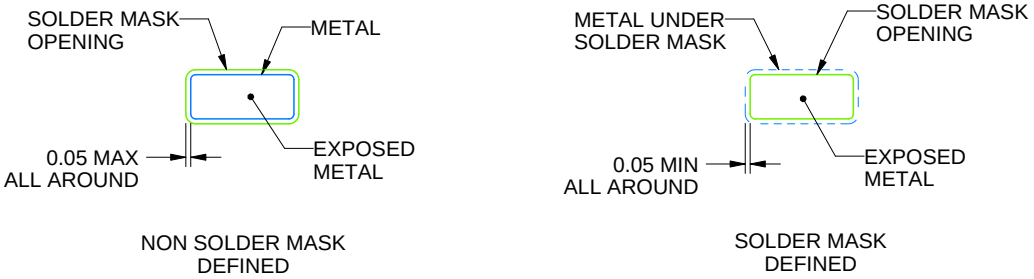


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

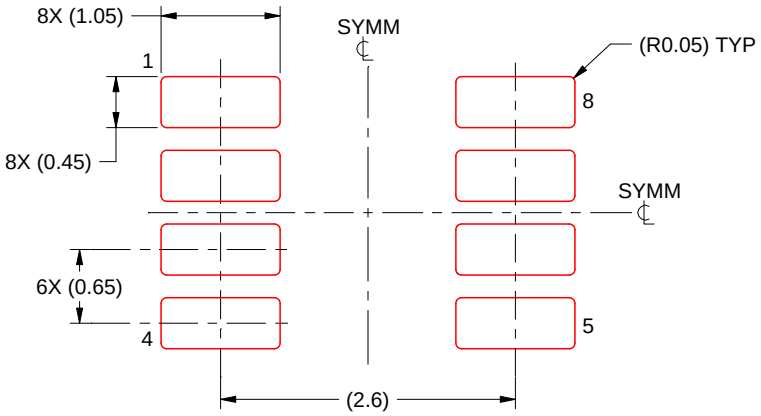
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

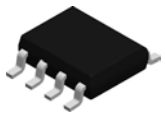


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

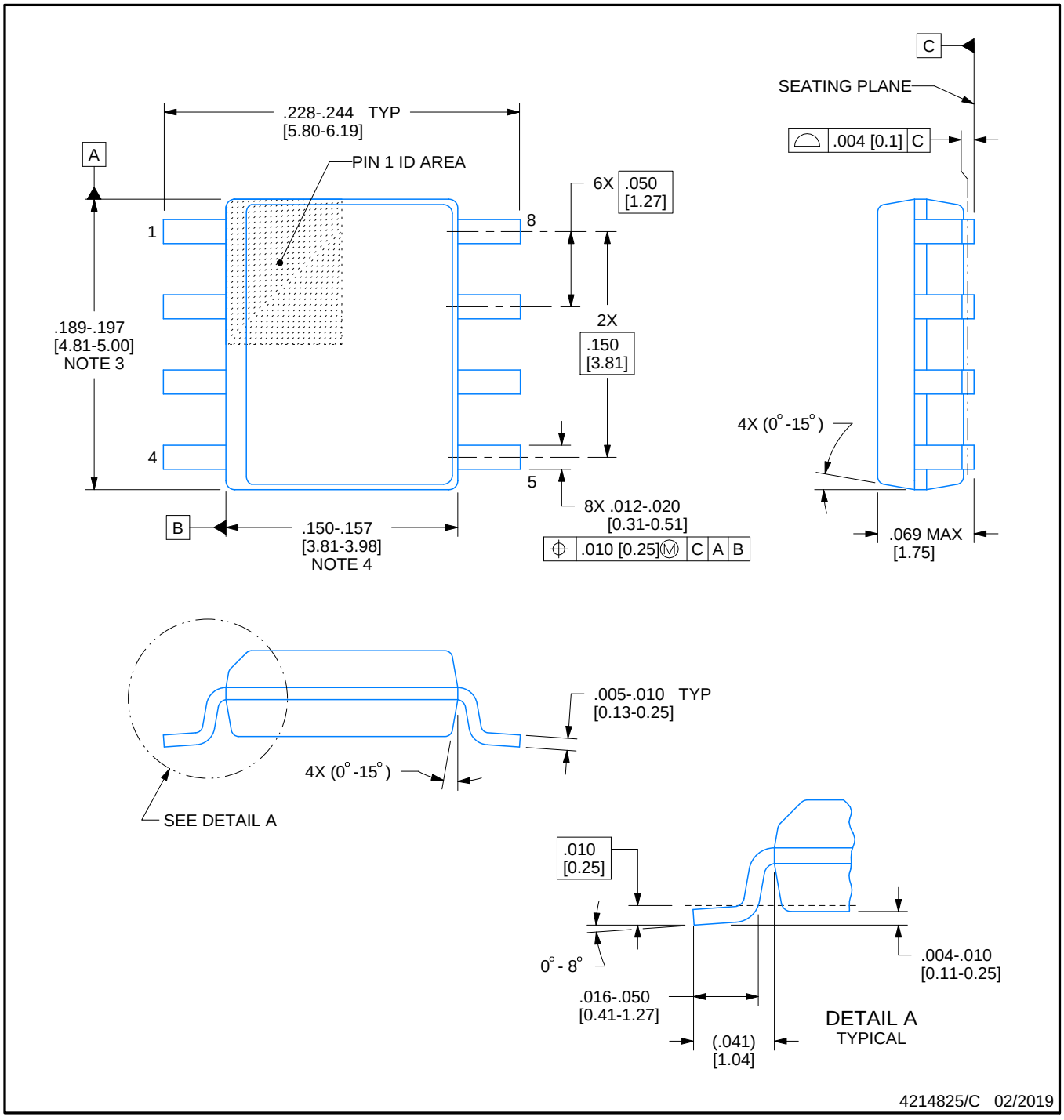


PACKAGE OUTLINE

D0008A

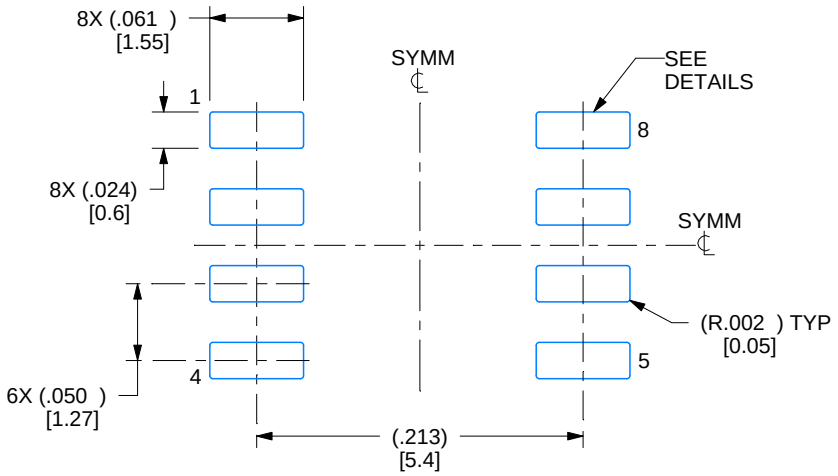
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

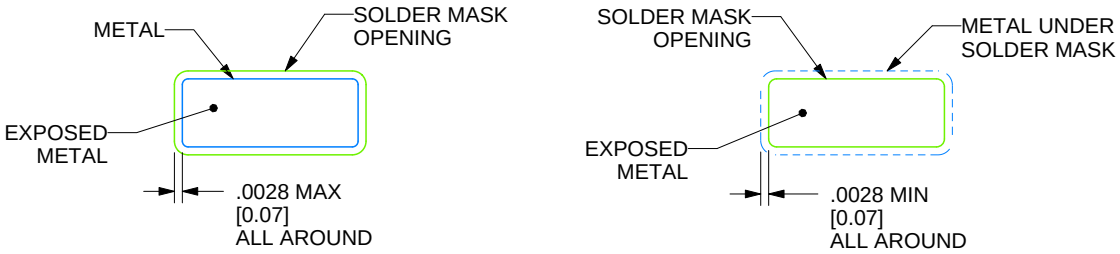


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

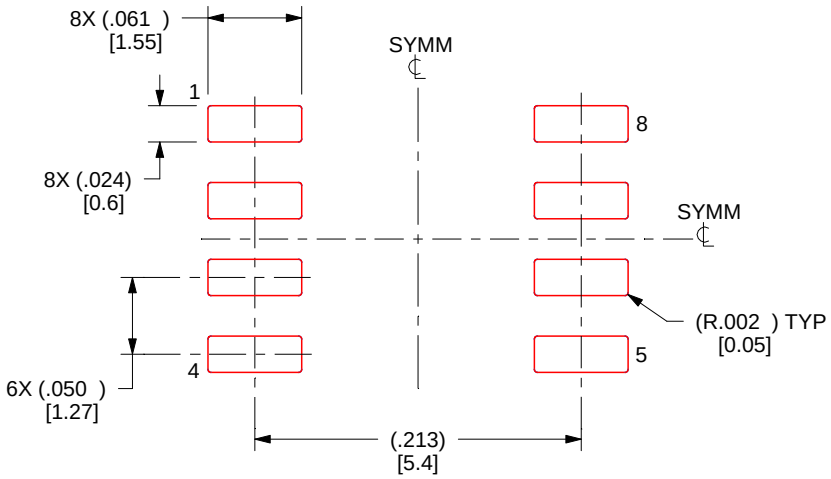
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

最后更新日期：2025 年 10 月