TLIN2029A-Q1 具有显性状态超时的故障保护 LIN 收发器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
- 符合 LIN 2.0、LIN 2.1、LIN 2.2、LIN 2.2 A 和 ISO/DIS 17987 – 4 电气物理层 (EPL) 规格标准
- 符合面向汽车应用的 SAE J2602-1 LIN 网络标准
- 功能安全型
  - 可提供用于功能安全系统设计的文档
- 支持 12V 和 24V 应用
- LIN 传输数据速率高达 20kbps
- LIN 接收数据速率高达 100kbps
- 宽工作电源电压范围：4V 至 48V
- 休眠模式：超低电流消耗支持以下类型的唤醒事件：
  - LIN 总线
  - 通过 EN 引脚实施的本地唤醒
- 在 LIN 总线和 RXD 输出上实现上电和断电无干扰运行
- 保护特性：
  - ±60V LIN 总线容错
  - V_{SUP} 欠压保护
  - TXD 显性超时 (DTO) 保护
  - 热关断保护
  - 系统级未供电节点或接地断开失效防护。
- 可提供具有可润湿侧翼的 SOIC (8) 和无引线 VSON (8)

2 应用

- 车身电子装置和照明
- 信息娱乐系统与仪表组
- 混合动力电动汽车和动力总成系统
- 被动安全
- 电器

3 说明

TLIN2029A-Q1 是一款本地互连网络 (LIN) 物理层收发器，集成了唤醒和保护功能，符合 LIN 2.0、LIN 2.1、LIN 2.2、LIN 2.2 A 和 ISO/DIS 17987 – 4 标准。LIN 是一种单线双向总线，通常用于数据传输速率高达 20kbps 的车载网络。TLIN2029A-Q1 旨在为 12V 和 24V 应用提供支持，具有更宽的工作电压范围和额外的总线故障保护。

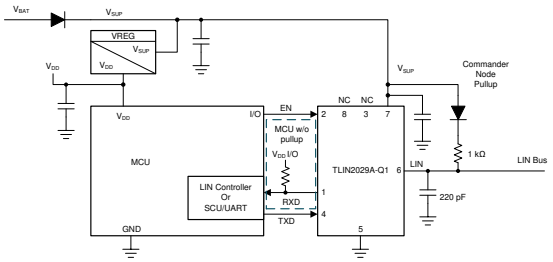
LIN 接收器支持高达 100kbps 的数据传输速率，从而更快速地执行内联编程。TLIN2029A-Q1 使用一个可降低电磁辐射 (EME) 的限流波形整形驱动器将 TXD 输入上的数据流转化为 LIN 总线信号。接收器将数据流转化为逻辑电平信号，此信号通过开漏 RXD 引脚发送到微处理器。睡眠模式可实现超低电流消耗，该模式允许通过 LIN 总线或 EN 引脚实现唤醒。

TLIN2029A-Q1 集成了一个用于 LIN 响应器节点应用、ESD 保护和故障保护的电阻器，可减少应用中的外部元件数量。一旦发生接地漂移或电源电压断开的情况，该器件可防止反馈电流经 LIN 流向电源输入。TLIN2029A-Q1 还包含欠压保护、过热关断保护和接地失效保护功能。

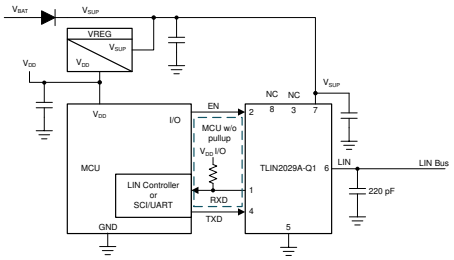
封装信息

器件型号	封装(1)	封装尺寸(2)
TLIN2029A-Q1	SOIC (D) (8)	4.9mm x 6mm
	VSON (DRB) (8)	3mm x 3mm

(1) 如需更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化版原理图，指挥官模式



简化版原理图，响应者模式

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

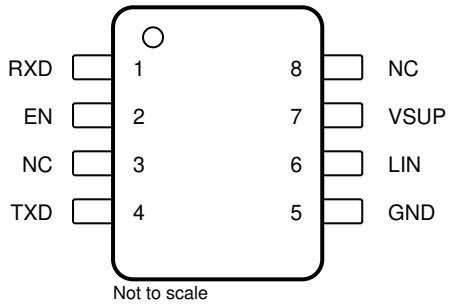


图 4-1. D Package, 8-Pin (SOIC)
(Top View)

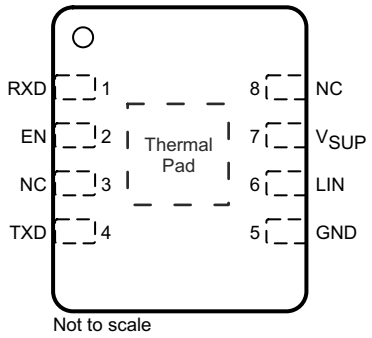


图 4-2. DRB Package, 8-Pin (VSON)
(Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
RXD	1	DO	RXD output (open-drain) interface reporting state of LIN bus voltage
EN	2	DI	Enable input - High puts the device in normal operation mode and low puts the device in sleep mode
NC	3	–	Not connected
TXD	4	DI	TXD input interface to control state of LIN output - Internally pulled to ground
GND	5	GND	Ground
LIN	6	HV I/O	LIN bus single-wire transmitter and receiver
V_{SUP}	7	HV Supply	Device supply voltage (connected to battery in series with external reverse blocking diode)
NC	8	–	Not connected
Thermal Pad		-	Can be connected to the PCB ground plane to improve thermal coupling (DRB package only)

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5 Specifications

5.1 Absolute Maximum Ratings

(1) (2)

Symbol	Parameter	MIN	MAX	UNIT
V_{SUP}	Supply voltage range (ISO/DIS 17987)	–0.3	60	V
V_{LIN}	LIN bus input voltage (ISO/DIS 17987)	–60	60	V
V_{LOGIC}	Logic pin voltage (RXD, TXD, EN)	–0.3	6	V
I_O	Digital pin output current		8	mA
T_J	Junction temperature range	–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground terminal.

5.2 ESD Ratings

ESD Ratings				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) classification level 3A: TXD, RXD, EN Pins, per AEC Q100-002(1)		±4000	V
		Human body model (HBM) classification level 3B: LIN and V_{SUP} Pin with respect to ground		±8000	
		Charged device model (CDM) classification level C5, per AEC Q100-011	All terminals	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings - IEC

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	LIN, V_{SUP} to GND(1)	IEC 62228-2 per ISO 10605 Contact discharge R = 330 Ω, C = 150 pF	±8000	V

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5.3 ESD Ratings - IEC（续）

				VALUE	UNIT
V_{TRAN}	Non-synchronous transient injection	LIN , V_{SUP} to GND	IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 1	– 100	V
			IEC 62215-3 24 V electrical systems (2) Pulse 1	– 450	
			IEC 62228-2 per IEC 62215-3 12 V electrical systems 24 V electrical systems (2) Pulse 2	75	
			IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 3a	– 150	
			IEC 62215-3 24 V electrical systems (2) Pulse 3a	-225	
			IEC 62228-2 per IEC 62215-3 12 V electrical systems Pulse 3b	100	
			IEC 62215-3 24 V electrical systems (2) Pulse 3b	225	

(1) Results given here are specific to the IEC 62228-2 Integrated circuits – EMC evaluation of transceivers – Part 2: LIN transceivers. Testing performed by OEM approved independent 3rd party, EMC report available upon request.
(2) Verified during characterization

5.4 Thermal Information

THERMAL METRIC(1)		TLIN2029AD-Q1	TLIN2029ADRB-Q1	UNIT
		D (SOIC)	DRB (VSON)	
		8-PINS	8-PINS	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	115.5	48.5	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	58.7	55.5	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	58.9	22.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.1	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.2	22.2	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	--	4.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

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5.5 Recommended Operating Conditions

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER - DEFINITION		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage	4		48	V
V_{LIN}	LIN Bus input voltage	0		48	V
V_{LOGIC}	Logic Pin Voltage (RXD, TXD, EN)	0		5.25	V
T_A	Ambient temperature range	-40		125	℃

5.6 Electrical Characteristics

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
V_{SUP}	Operational supply voltage (ISO/DIS 17987 Param 10)	Device is operational beyond the LIN defined nominal supply voltage range See Figure 8-1 and Figure 8-2	4		48	V
V_{SUP}	Nominal supply voltage (ISO/DIS 17987 Param 10)	Normal and Standby Modes: ramp V_{SUP} while LIN signal is a 10 kHz square wave with 50 % duty cycle and 36V swing. See Figure 8-1 and Figure 8-2	4		48	V
		Sleep Mode	4		48	V
UV_{SUP}	Under voltage V_{SUP} threshold	Min is falling edge and Max is rising edge	2.9		3.85	V
UV_{HYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			0.2		V
I_{SUP}	Supply current	Normal Mode: EN = high, bus dominant: total bus load where R_{LIN} > 500 Ω and C_{LIN} < 10 nF		1.2	5	mA
		Standby Mode: EN = low, bus dominant: total bus load where R_{LIN} > 500 Ω and C_{LIN} < 10 nF		1	2.1	mA
I_{SUP}	Supply current	Normal Mode: EN = high, bus recessive: LIN = V_{SUP},		400	700	µA
		Standby Mode: EN = low, bus recessive: LIN = V_{SUP},		20	35	µA
		Sleep Mode: 4.0 V < V_{SUP} ≤ 27 V, LIN = V_{SUP}, EN = 0 V, TXD and RXD floating		9	15	µA
		Sleep Mode: 27 V < V_{SUP} ≤ 48 V, LIN = V_{SUP}, EN = 0 V, TXD and RXD floating			30	µA
TSD	Thermal shutdown		165			℃
$TSD_{(HYS)}$	Thermal shutdown hysteresis			15		℃
RXD Output Pin (Open Drain)						
V_{OL}	Output low voltage	Based upon external pull-up to V_{CC} (4)			0.6	V
I_{OL}	Low level output current, open drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{ILG}	Leakage current, high-level	LIN = V_{SUP}, RXD = 5 V	-5	0	5	µA
TXD Input Pin						
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{IH}	High level input voltage		2		5.25	V
I_{ILG}	Low level input leakage current	TXD = low	-5	0	5	µA
R_{TXD}	Internal pull-down resistor value		125	350	800	kΩ

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5.6 Electrical Characteristics（续）

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LIN PIN						
V_{OH}	HIGH level output voltage (3)	LIN recessive, TXD = high, I_O = 0 mA, 7 V ≤ V_{SUP} ≤ 48 V	0.85			V_{SUP}
V_{OH}	LIN recessive high-level output voltage (1) (2)	TXD = high, I_O = 0 mA, 7 V ≤ V_{SUP} ≤ 18 V	0.8			V_{SUP}
V_{OH}	HIGH level output voltage(3)	LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 4 V ≤ V_{SUP} < 7 V	3			V
V_{OL}	LOW level output voltage(3)	LIN dominant, TXD = low, V_{SUP} = 7 V to 48 V			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage (1) (2)	TXD = low, 7 V ≤ V_{SUP} ≤ 18 V			0.2	V_{SUP}
V_{OL}	LOW level output voltage(3)	LIN dominant, TXD = low, V_{SUP} = 4 V ≤ V_{SUP} < 7 V			1.2	V
$V_{SUP_NON_OP}$	VSUP where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	TXD & RXD open LIN = 4 V to 58 V	-0.3		58	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 57)	TXD = 0 V, V_{LIN} = 36 V, R_{MEAS} = 440 Ω, V_{SUP} = 36 V, V_{BUSdom} < 4.518 V	75	120	300	mA
$I_{BUS_PAS_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13, 58)	LIN = 0 V, V_{SUP} = 24 V Driver off/ recessive, Figure 8-6	-1			mA
$I_{BUS_PAS_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14, 59)	LIN > V_{SUP}, 4 V ≤ V_{SUP} ≤ 45 V Driver off; Figure 8-7			20	µA
$I_{BUS_PAS_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14, 59)	LIN = V_{SUP}, Driver off; Figure 8-7	-5		5	µA
$I_{BUS_NO_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15, 60)	GND = V_{SUP}, V_{SUP} = 27 V, LIN = 0 V; Figure 8-8	-1		1	mA
$I_{BUS_NO_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15, 60)	GND = V_{SUP}, V_{SUP} ≥ 36 V, LIN = 0 V; Figure 8-8	-1.5		1.5	mA
$I_{leak\ gnd(dom)}$	Leakage current, loss of ground (5)	V_{SUP} = 8 V, GND = open, V_{SUP} = 18 V, GND = open $R_{Commander}$ = 1 kΩ, C_L = 1 nF $R_{Responder}$ = 20 kΩ, C_L = 1 nF LIN = dominant	-1		1	mA
$I_{leak\ gnd(rec)}$	Leakage current, loss of ground (5)	V_{SUP} = 8 V, GND = open, V_{SUP} = 18 V, GND = open $R_{Commander}$ = 1 kΩ, C_L = 1 nF $R_{Responder}$ = 20 kΩ, C_L = 1 nF LIN = recessive	-100		100	µA
$I_{BUS_NO_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16, 61)	LIN = 48 V, V_{SUP} = GND; Figure 8-9			5	µA
V_{BUSdom}	Low level input voltage (ISO/DIS 17987 Param 17, 62)	LIN dominant (including LIN dominant for wake up) See Figure 8-4, Figure 8-3			0.4	V_{SUP}
V_{BUSrec}	High level input voltage (ISO/DIS 17987 Param 18, 63)	LIN recessive See Figure 8-4, Figure 8-3	0.6			V_{SUP}
V_{IH}	LIN recessive high-level input voltage (1) (2)	7 V ≤ V_{SUP} ≤ 18 V	0.47		0.6	V_{SUP}
V_{IL}	LIN dominant low-level input voltage (1) (2)	7 V ≤ V_{SUP} ≤ 18 V	0.4		0.53	V_{SUP}
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19, 64)	V_{BUS_CNT} = (V_{BUSrec} + V_{BUSdom})/2 See Figure 8-4, Figure 8-3	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20, 65)	V_{HYS} = (V_{BUSrec} - V_{BUSdom}) See Figure 8-4, Figure 8-3			0.175	V_{SUP}

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5.6 Electrical Characteristics（续）

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS}	Hysteresis voltage (SAE J2602)	V_{HYS} = V_{IH} - V_{IL} See Figure 8-4, Figure 8-3	0.07		0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN termination pull-up path	I_{SERIAL_DIODE} = 10 μA	0.4	0.7	1	V
R_{PU}	Internal pull-up resistor to V_{SUP}	Normal and standby modes	20	45	60	kΩ
I_{RSLEEP}	Pull-up current source to V_{SUP}	Sleep mode, V_{SUP} = 27 V, LIN = GND	-20		-2	μA
C_{LINPIN}	Capacitance of the LIN pin	V_{SUP} = 14 V			25	pF
EN Input Pin						
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{IH}	High level input voltage		2		5.25	V
V_{IT}	Hysteresis voltage	By design and characterization		50	500	mV
I_{ILG}	Low level input current	EN = low	-5	0	5	μA
R_{EN}	Internal pull-down resistor		125	350	800	kΩ

(1) SAE 2602 commander node load conditions: 5.5 nF/4 kΩ and 899 pF/20 kΩ
(2) SAE 2602 responder node load conditions: 5.5 nF/875 Ω and 899 pF/900 Ω
(3) ISO 17987 bus load conditions (C_{LINBUS}, R_{LINBUS}) include 1 nF/1 kΩ; 6.8 nF/660 Ω; 10 nF/500 Ω.
(4) RXD uses open drain output structure therefore V_{OL} level is based upon microcontroller supply voltage V_{CC}.
(5) $I_{leak\ gnd}$ = (V_{BAT} - V_{LIN})/R_{Load}

5.7 Duty Cycle Characteristics

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$D1_{12V}$	Duty Cycle 1 (ISO/DIS 17987 Param 27) (3)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP} $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50 μs (20 kbps), D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.396			
$D1_{12V}$	Duty Cycle 1 (ISO/DIS 17987 Param 27)(3) (4)	$TH_{REC(MAX)}$ = 0.625 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 50 μs (20 kbps), D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.396			
D1	Duty cycle 1 (1) (2) (4)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 52 μs D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.396			
$D2_{12V}$	Duty Cycle 2 (ISO/DIS 17987 Param 28)(3)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50 μs (20 kbps), D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.581	
$D2_{12V}$	Duty Cycle 2(3) (4)	$TH_{REC(MIN)}$ = 0.546 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.4 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 50 μs (20 kbps), D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.581	
D2	Duty Cycle 2 (1) (2) (4)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 52 μs D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.581	

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5.7 Duty Cycle Characteristics（续）

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$D3_{12V}$	Duty Cycle 3 (ISO/DIS 17987 Param 29)(3)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.417			
$D3_{12V}$	Duty Cycle 3(3) (4)	$TH_{REC(MAX)}$ = 0.645 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.417			
D3	Duty Cycle 3 (1) (2) (4)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.417			
$D4_{12V}$	Duty Cycle 4 (ISO/DIS 17987 Param 30)(3)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.59	
$D4_{12V}$	Duty Cycle 4(3) (4)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.59	
D4	Duty Cycle 4 (1) (2) (4)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.59	
$D1_{24V}$	Duty Cycle 1 (ISO/DIS 17987 Param 72)	$TH_{REC(MAX)}$ = 0.710 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.544 x V_{SUP}, V_{SUP} = 15 V to 36 V, t_{BIT} = 50 µs (20 kbps), D1 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.33			
$D2_{24V}$	Duty Cycle 2 (ISO/DIS 17987 Param 73)	$TH_{REC(MIN)}$ = 0.446 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.302 x V_{SUP}, V_{SUP} = 15.6 V to 36 V, t_{BIT} = 50 µs (20 kbps), D2 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.642	
$D3_{24V}$	Duty Cycle 3 (ISO/DIS 17987 Param 74)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 36 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.386			
$D3_{24V}$	Duty Cycle (4)	$TH_{REC(MAX)}$ = 0.645 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 4 V to 7 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS_rec(min)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)	0.386			
$D4_{24V}$	Duty Cycle 4 (ISO/DIS 17987 Param 75) (4)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 4.6 V to 36 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-10, Figure 8-11)			0.591	
$D1_{LB}$	Duty cycle 1 at low battery (1) (2) (4)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 52 µs	0.396			
$D2_{LB}$	Duty cycle 2 at low battery (1) (2) (4)	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 6.1 V to 7 V, t_{BIT} = 52 µs			0.581	

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5.7 Duty Cycle Characteristics（续）

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$D3_{LB}$	Duty cycle 3 at low battery (1) (2) (4)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 96 µs	0.396			
$D4_{LB}$	Duty cycle 4 at low battery (1) (2) (4)	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 6.1 V to 7 V, t_{BIT} = 96 µs			0.581	
Tr-d max	Transmitter propagation delay timings for the duty cycle(1) (2) (4) Recessive to dominant	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 52 µs $t_{REC(MAX)_D1}$ - $t_{DOM(MIN)_D1}$			10.8	µs
Td-r max	Transmitter propagation delay timings for the duty cycle(1) (2) (4) Dominant to recessive	$TH_{REC(MAX)}$ = 0.422 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.284 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 52 µs $t_{DOM(MAX)_D2}$ - $t_{REC(MIN)_D2}$			8.4	µs
Tr-d max	Transmitter propagation delay timings for the duty cycle(1) (2) (4) Recessive to dominant	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 96 µs $t_{REC(MAX)_D3}$ - $t_{DOM(MIN)_D3}$			15.9	µs
Td-r max	Transmitter propagation delay timings for the duty cycle(1) (2) (4) Dominant to recessive	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} 7 V ≤ V_{SUP} ≤ 18 V, t_{BIT} = 96 µs $t_{DOM(MAX)_D4}$ - $t_{REC(MIN)_D4}$			17.28	µs
Tr-d max_low	Low battery transmitter propagation delay timings for the duty cycle(1) (2) (4) Recessive to dominant	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} 5.5 V ≤ V_{SUP} ≤ 7 V, t_{BIT} = 52 µs $t_{REC(MAX)_low}$ - $t_{DOM(MIN)_low}$			10.8	µs
Td-r max_low	Low battery transmitter propagation delay timings for the duty cycle(1) (2) (4) Dominant to recessive	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} 6.1 V ≤ V_{SUP} ≤ 7 V, t_{BIT} = 52 µs $t_{DOM(MAX)_low}$ - $t_{REC(MIN)_low}$			8.4	µs

(1) SAE 2602 commander node load conditions: 5.5 nF/4 kΩ and 899 pF/20 kΩ
(2) SAE 2602 responder node load conditions: 5.5 nF/875 Ω and 899 pF/900 Ω
(3) ISO 17987 bus load conditions (C_{LINBUS}, R_{LINBUS}) include 1 nF/1 kΩ; 6.8 nF/660 Ω; 10 nF/500 Ω.
(4) Specified by design

5.8 Timing Requirements

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{rx_pdr}, t_{rx_pdf}	Receiver rising propagation delay time (ISO/DIS 17987 Param 31, 76)	R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See Figure 8-12 and Figure 8-13)			6	µs
t_{rx_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time	Rising edge with respect to falling edge, (t_{rx_sym} = t_{rx_pdf} – t_{rx_pdr}), R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See Figure 8-12 and Figure 8-13)	–2		2	µs
t_{LINBUS}	LIN wakeup time (Minimum dominant time on LIN bus for wakeup)	See Figure 8-16, Figure 9-2, and Figure 9-3	25	65	150	µs
t_{CLEAR}	Time to clear false wakeup prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See Figure 9-3	8	25	50	µs
t_{DST}	Dominant state time out		20	45	80	ms

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5.8 Timing Requirements（续）

parameters valid across -40℃ ≤ T_A ≤ 125℃ (unless otherwise noted)

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{MODE_CHANGE}	Mode change delay time	Time to change from standby mode to normal mode or normal mode to sleep mode through EN pin (See Figure 8-14 and Figure 9-4)	2		15	µs
t_{NOMINT}	Normal mode initialization time	Time for normal mode to initialize and data on RXD pin to be valid See Figure 8-14			35	µs
t_{PWR}	Power up time	Upon power up time it takes for valid data on RXD			1.5	ms

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5.9 Typical Characteristics

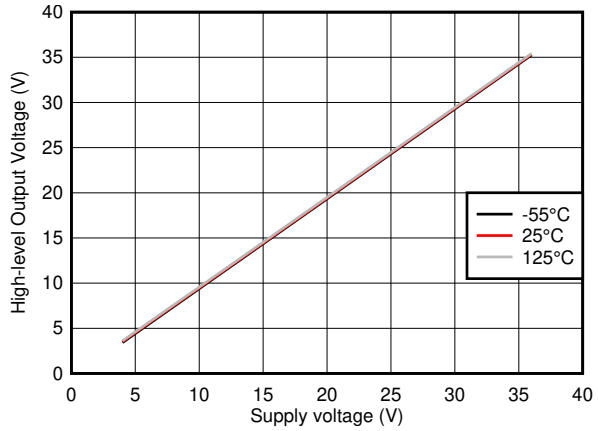


图 5-1. V_{OH} vs V_{SUP} and Temperature

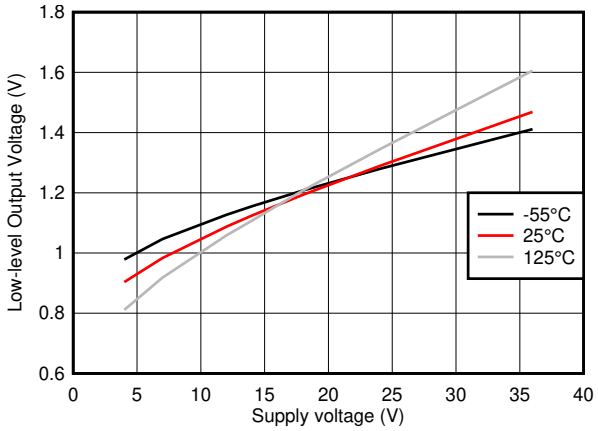


图 5-2. V_{OL} vs V_{SUP} and Temperature

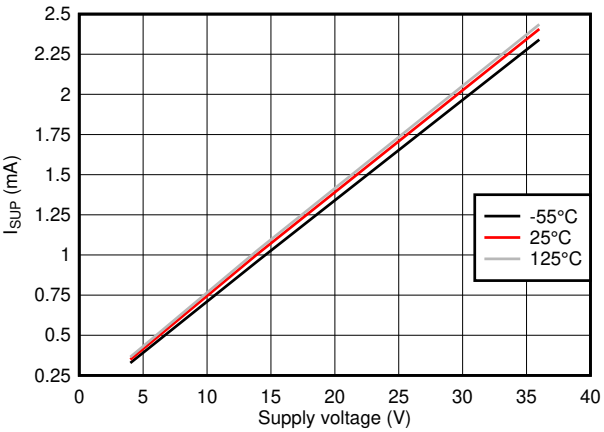


图 5-3. Dominant I_{SUP} vs V_{SUP} and Temperature

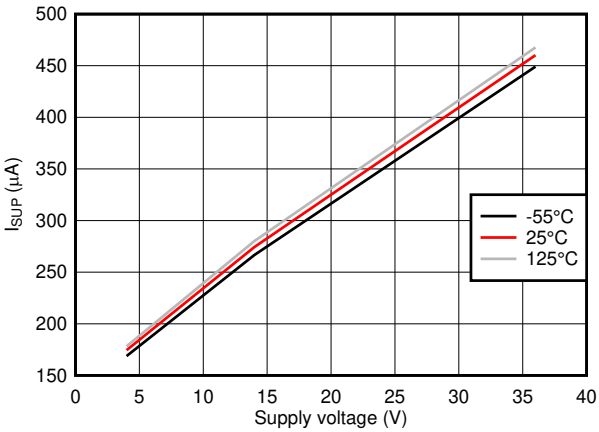


图 5-4. Recessive I_{SUP} vs V_{SUP} and Temperature

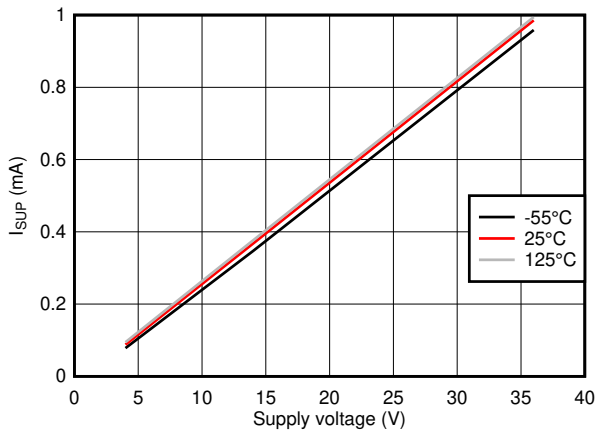


图 5-5. Standby Dominant I_{SUP} vs V_{SUP} and Temperature

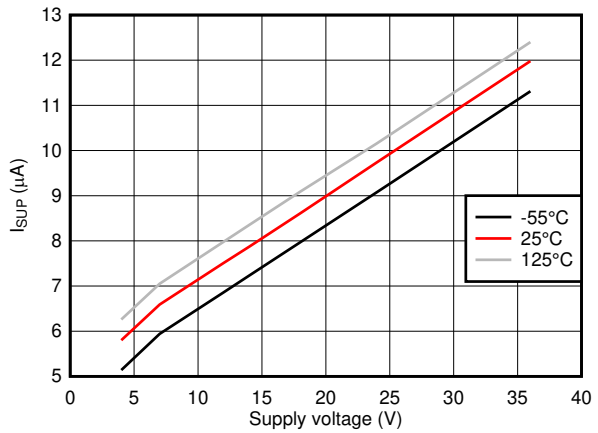


图 5-6. Standby Recessive I_{SUP} vs V_{SUP} and Temperature

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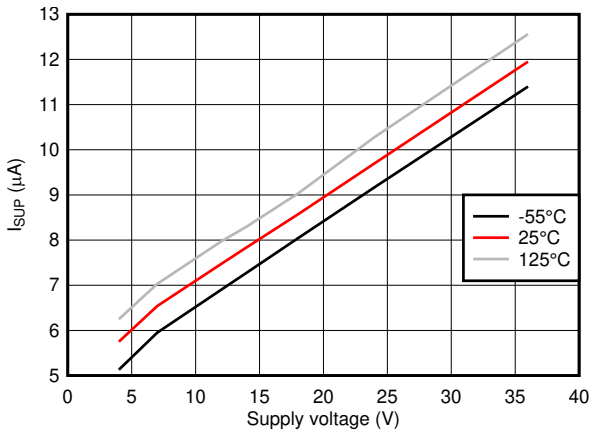


图 5-7. Sleep Current vs V_{SUP} and Temperature

6 Parameter Measurement Information

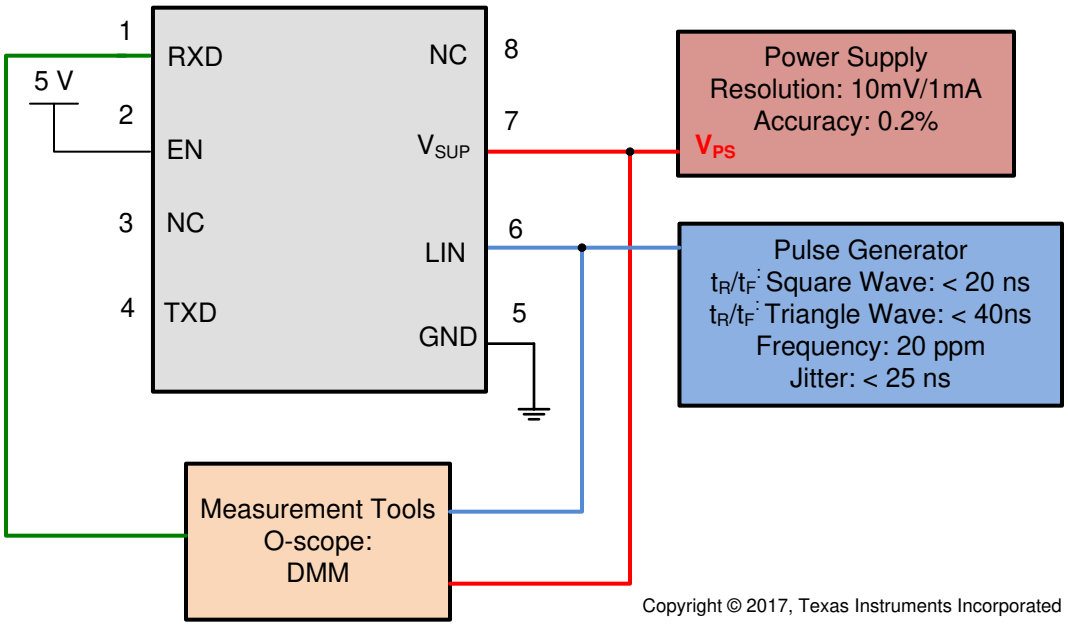


图 6-1. Test System: Operating Voltage Range with RX and TX Access: Parameters 9, 10

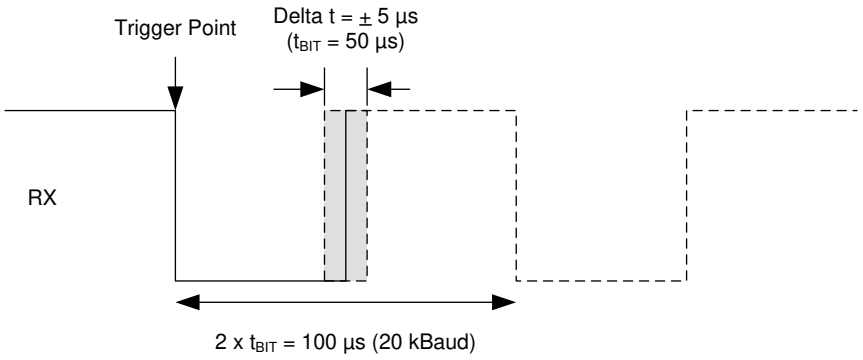


图 6-2. RX Response: Operating Voltage Range

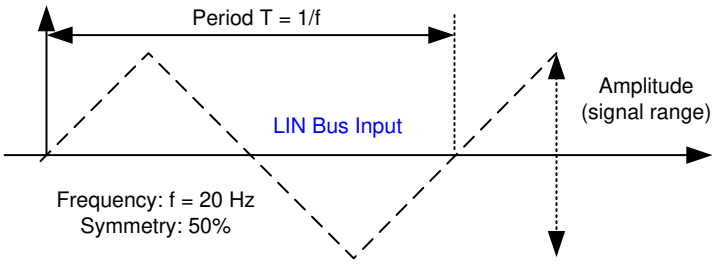


图 6-3. LIN Bus Input Signal

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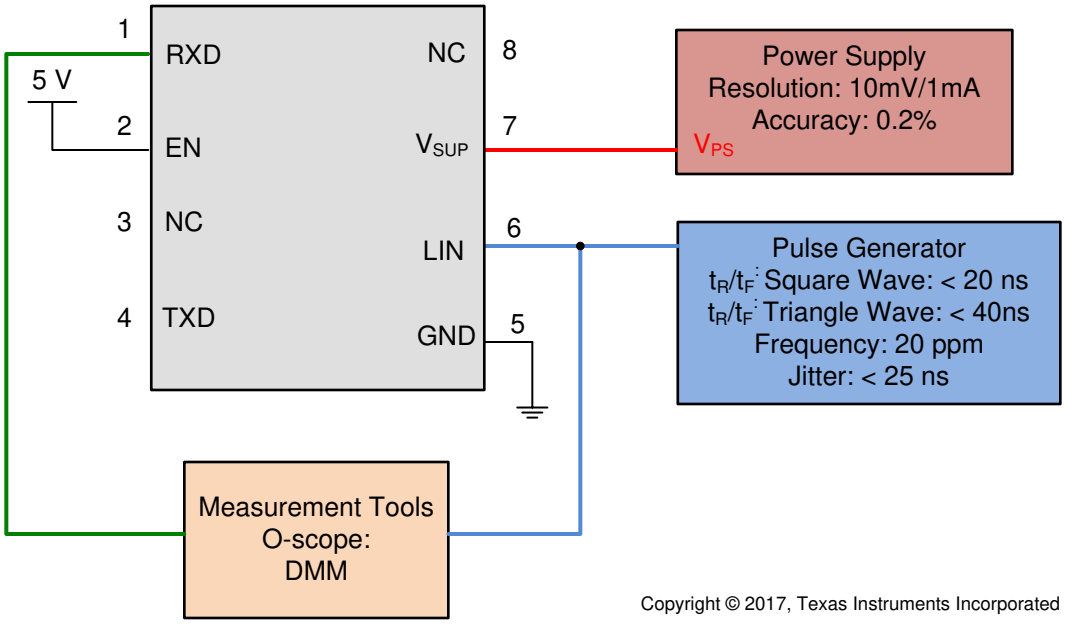


图 6-4. LIN Receiver Test with RX access Param 17, 18, 19, 20

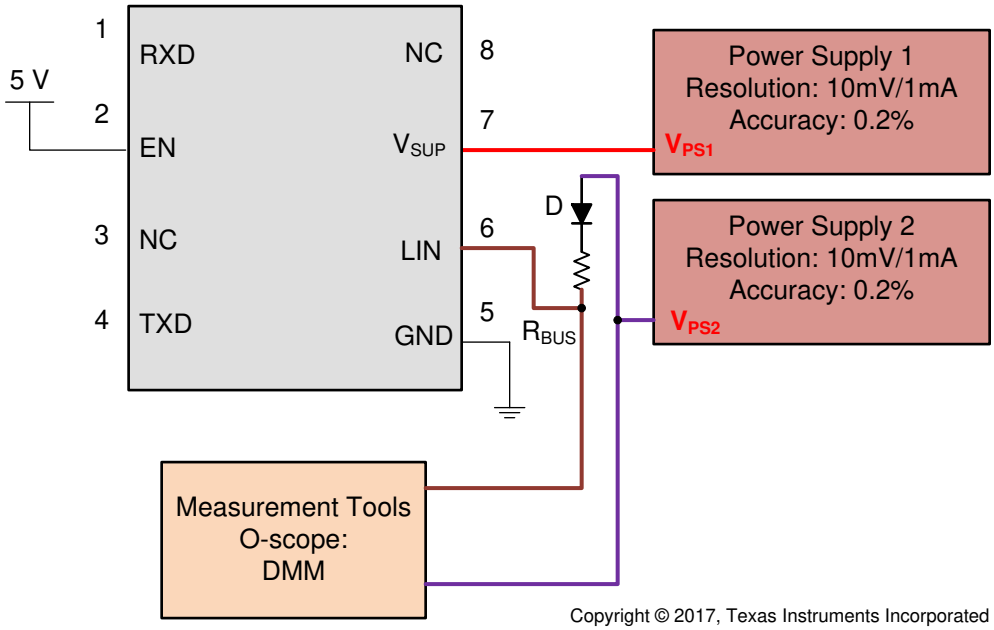


图 6-5. $V_{SUP_NON_OP}$ Param 11

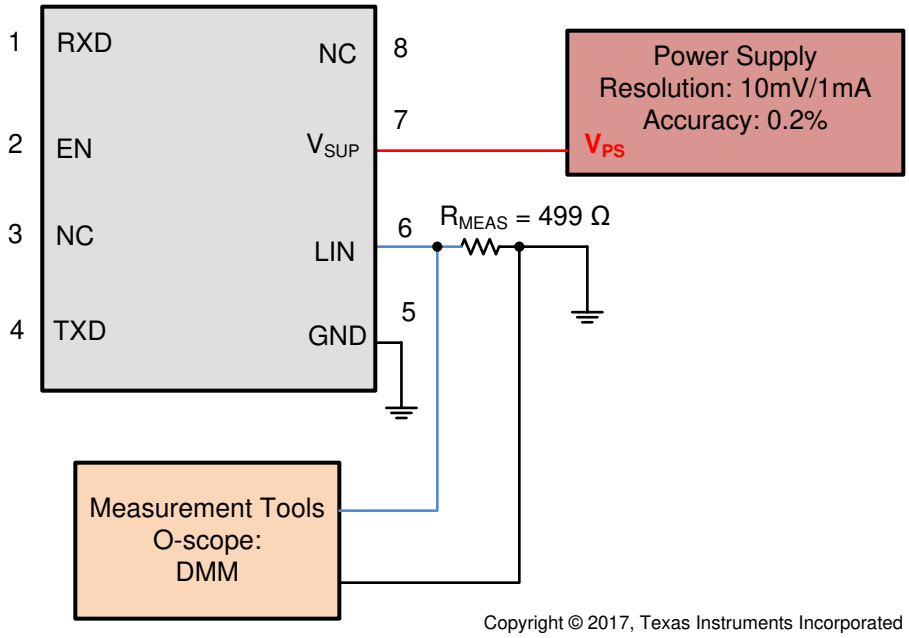


图 6-6. Test Circuit for $I_{BUS_PAS_dom}$; TXD = Recessive State V_{BUS} = 0 V, Param 13

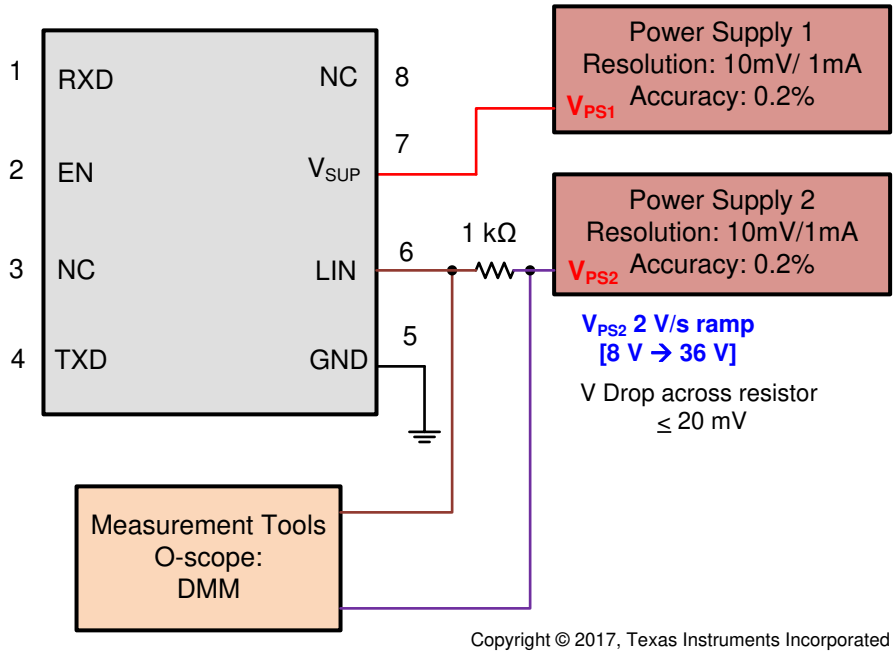


图 6-7. Test Circuit for $I_{BUS_PAS_rec}$ Param 14

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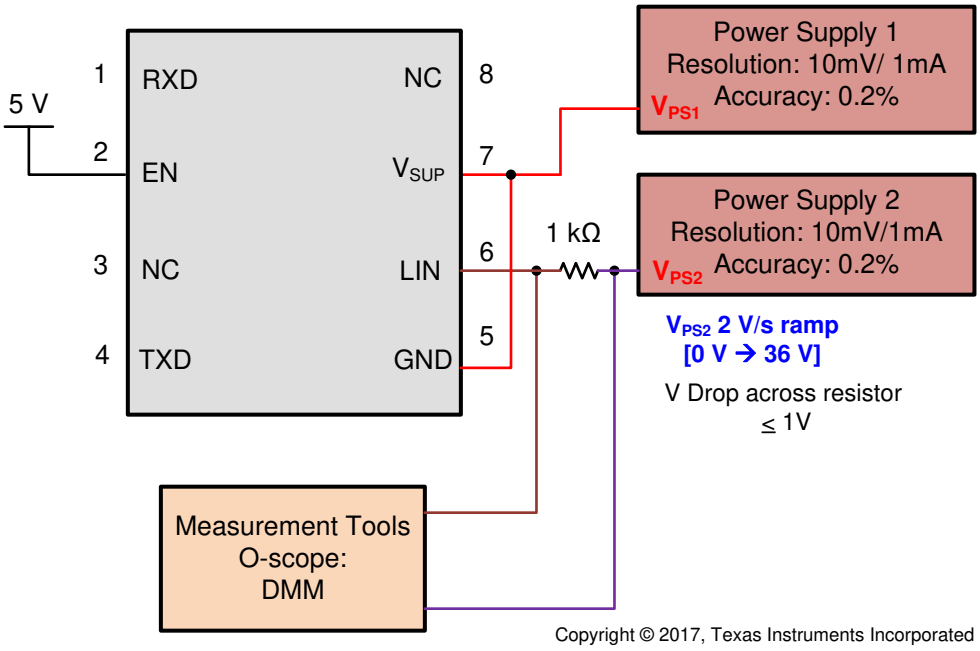


图 6-8. Test Circuit for $I_{BUS_NO_GND}$ Loss of GND

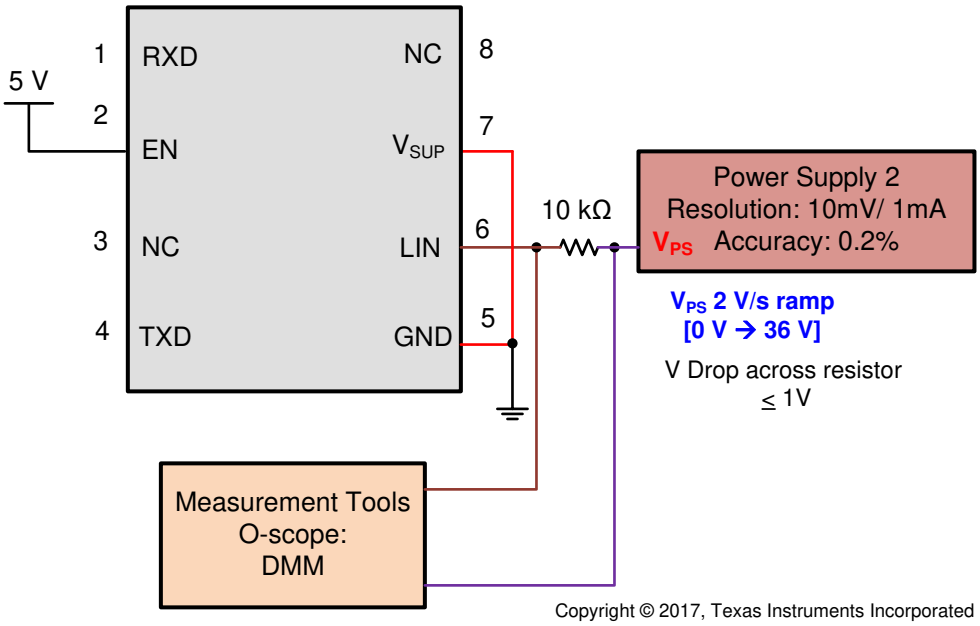


图 6-9. Test Circuit for $I_{BUS_NO_BAT}$ Loss of Battery

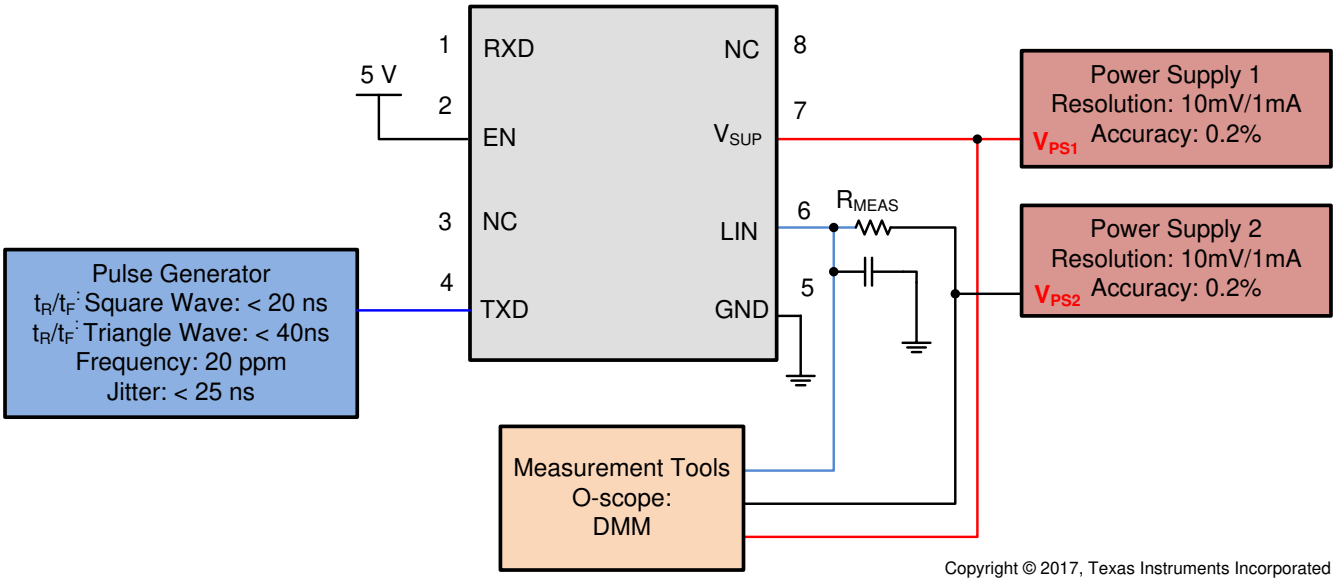


图 6-10. Test Circuit Slope Control and Duty Cycle Param 27, 28, 29, 30

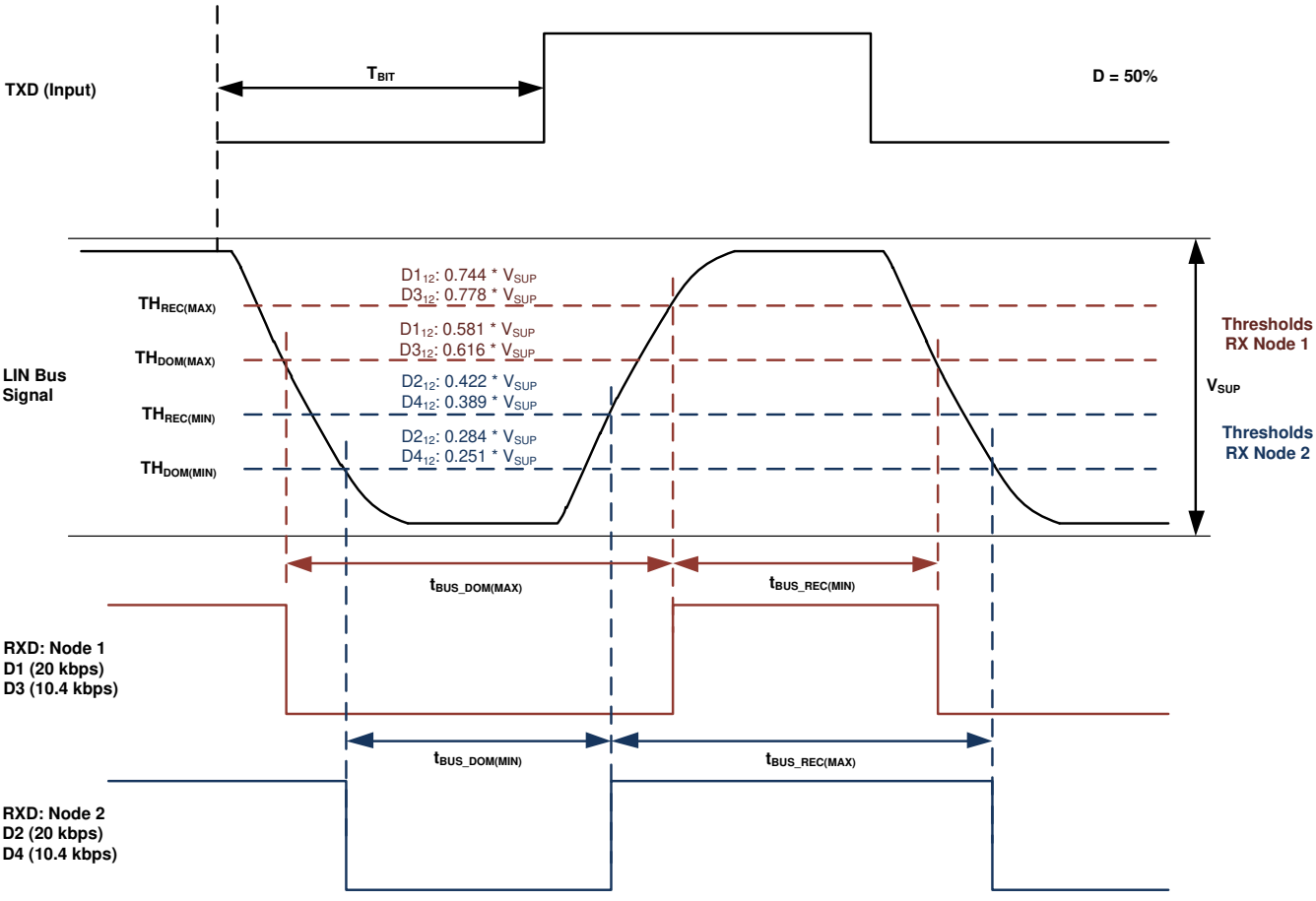


图 6-11. Definition of Bus Timing Parameters

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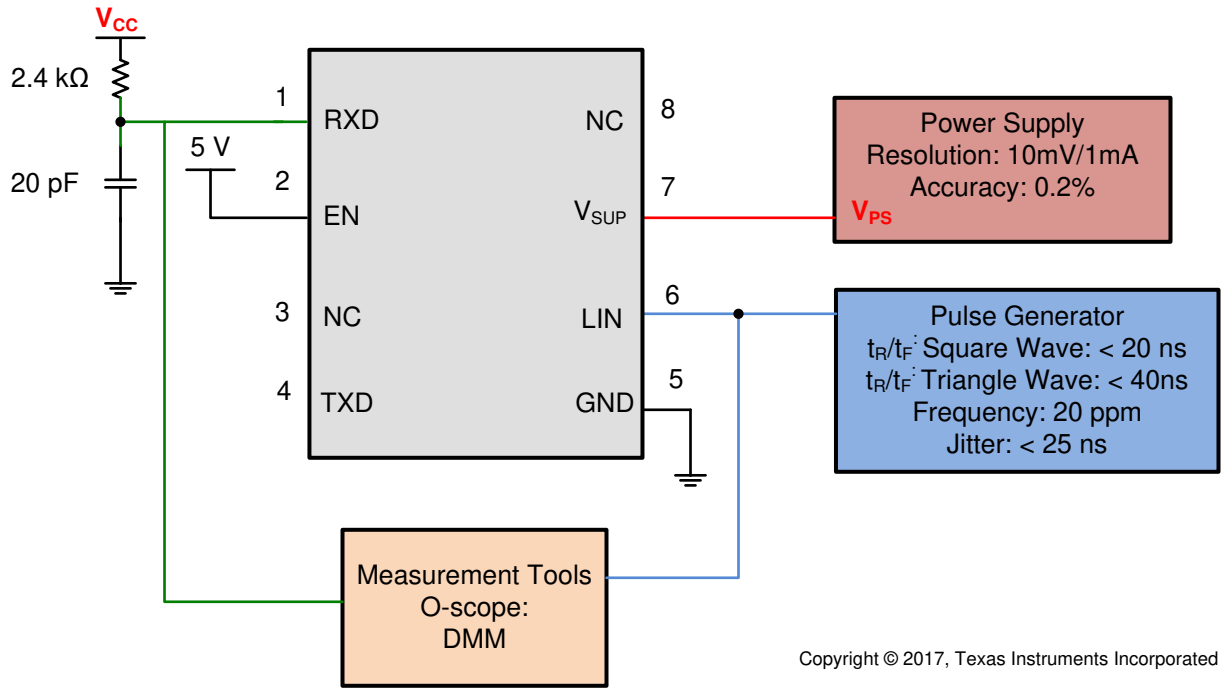


图 6-12. Propagation Delay Test Circuit; Param 31, 32

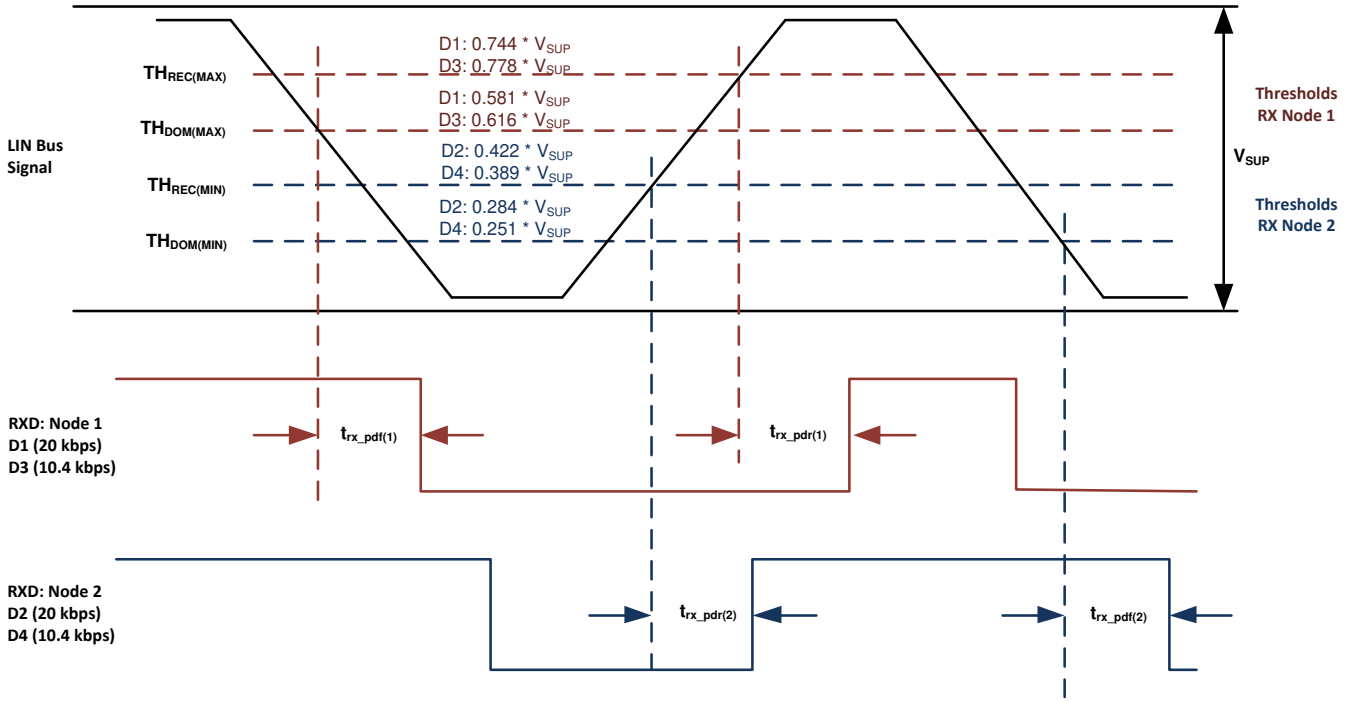


图 6-13. Propagation Delay

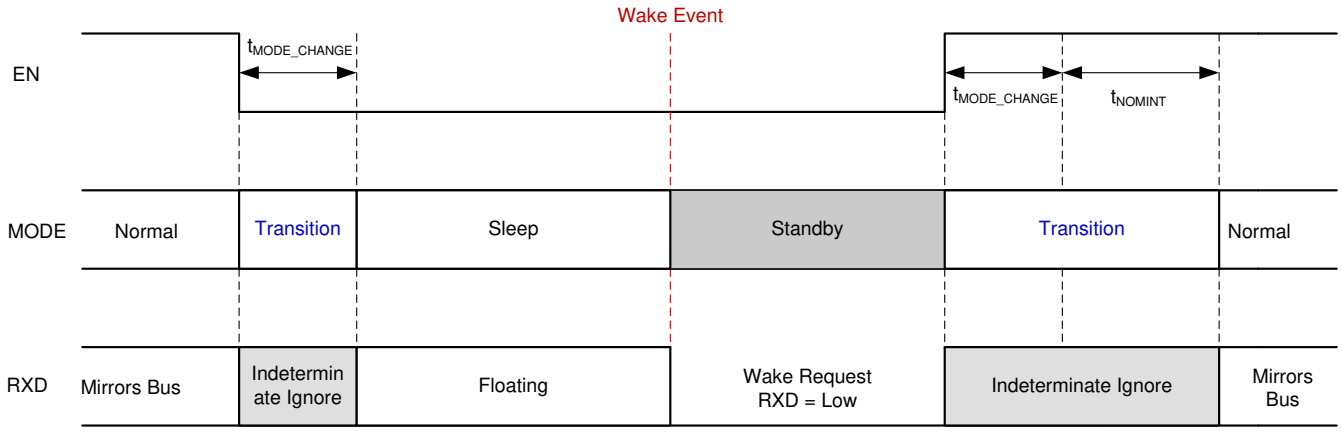


图 6-14. Mode Transitions

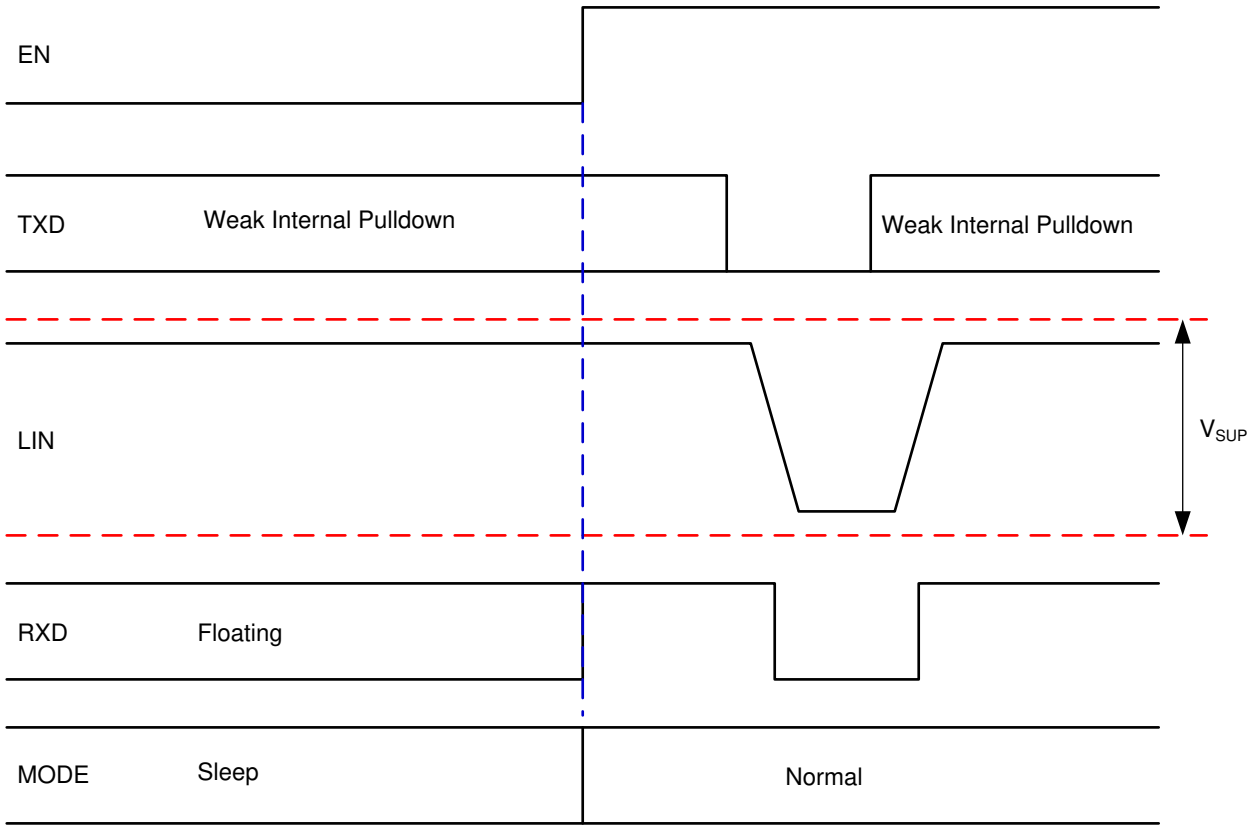


图 6-15. Wakeup Through EN

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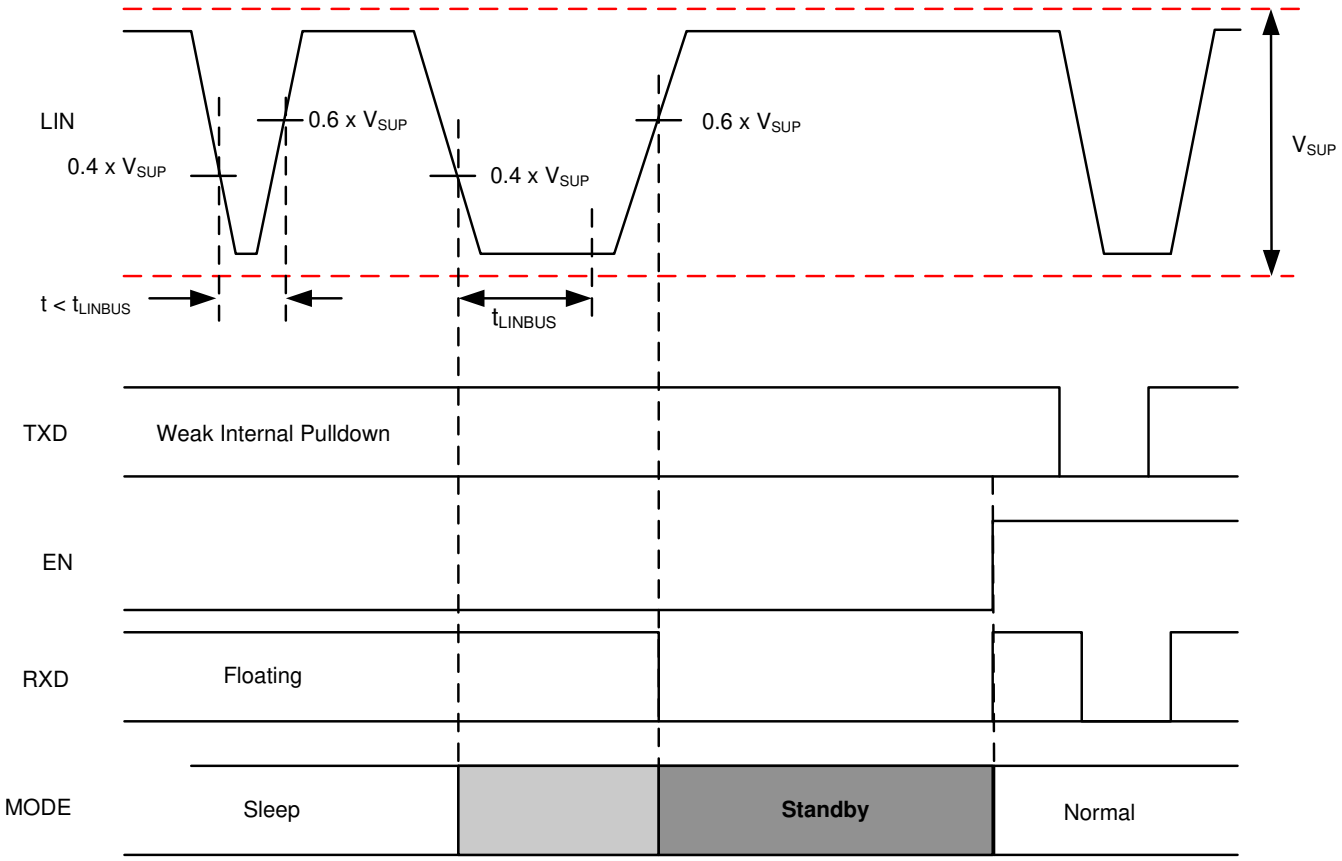


图 6-16. Wakeup through LIN

7 Detailed Description

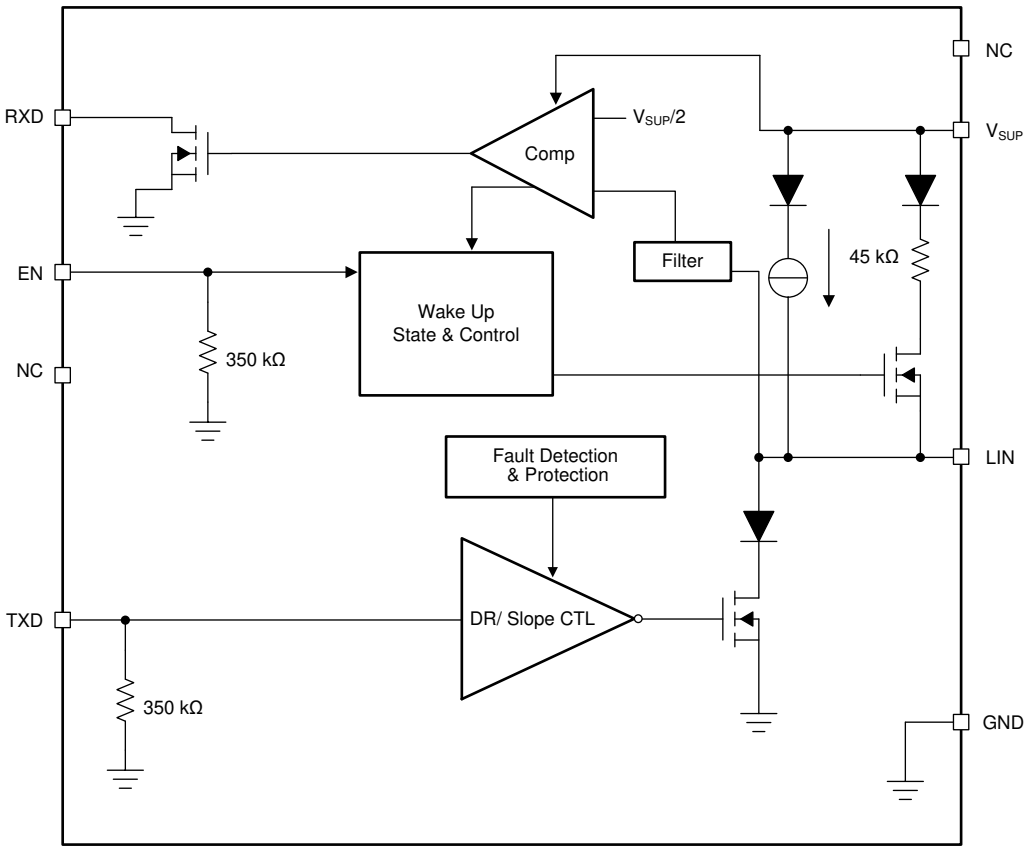
7.1 Overview

The TLIN2029A-Q1 is a Local Interconnect Network (LIN) physical layer transceiver, compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987 – 4 standards, with integrated wake-up and protection features. The LIN bus is a single-wire bidirectional bus typically used for low speed in-vehicle networks. The device transmitter supports data rates from 2.4kbps to 20kbps and the receiver works up to 100kbps supporting in-line programming. The LIN protocol data stream on the TXD input is converted by the TLIN2029A-Q1 into a LIN bus signal using a current-limited wave-shaping driver as outlined by the LIN physical layer specification. The receiver converts the data stream to logic-level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45kΩ) and a series diode. No external pull-up components are required for responder node applications. commander node applications require an external pull-up resistor (1kΩ) plus a series diode per the LIN specification.

The device is designed to support 12V and 24V applications with a wide input voltage operating range and also supports low-power sleep mode. The device also provides two methods to wake up: EN pin and from the LIN bus.

The TLIN2029A-Q1 integrates ESD protection and fault protection which allow for a reduction in the required external components in the applications. In the event of a ground shift or supply voltage disconnection, the device prevents back-feed current through LIN to the supply input. The device also includes undervoltage detection, temperature shutdown protection, and loss-of-ground protection.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 LIN (Local Interconnect Network) Bus

This high voltage input/output pin is a single-wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 60V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

7.3.1.1 LIN Transmitter Characteristics

The transmitter has thresholds and AC parameters according to the LIN specification. The transmitter is a low-side transistor with internal current limitation and thermal shutdown. During a thermal shut-down condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used for a commander node application.

7.3.1.2 LIN Receiver Characteristics

The receiver characteristic thresholds are proportional to the device supply pin in accordance to the LIN specification.

The receiver is capable of receiving higher data rates (> 100kbps) than supported by LIN or SAEJ2602 specifications. This allows the TLIN2029A-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

7.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor (1kΩ) and a series diode to V_{SUP} must be added when the device is used for commander node applications as per the LIN specification.

图 7-1 shows a commander node configuration and how the voltage levels are defined

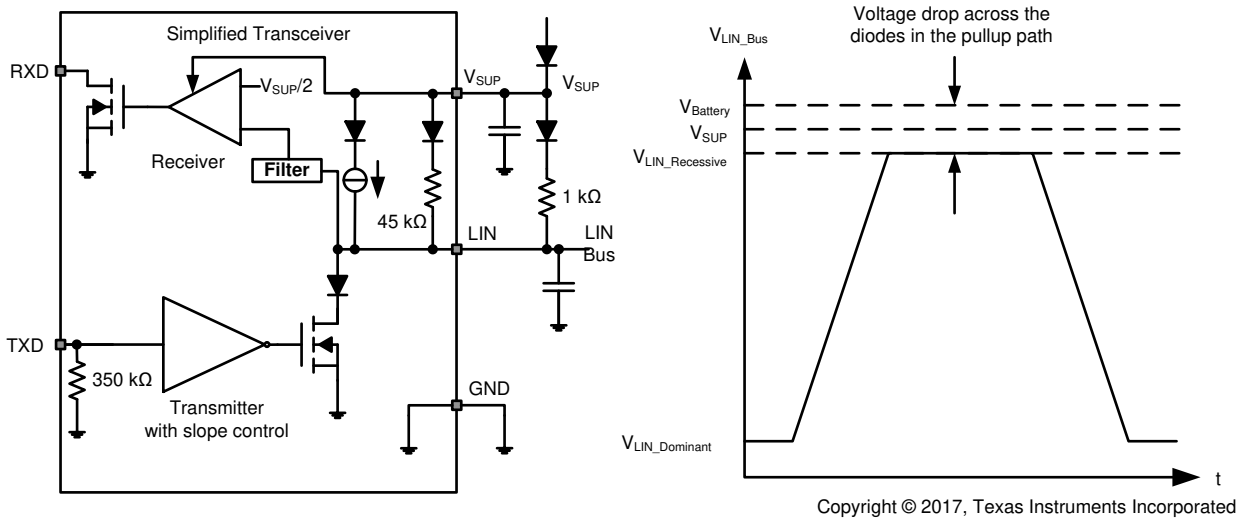


图 7-1. Commander Node Configuration with Voltage Levels

7.3.2 TXD (Transmit Input and Output)

TXD is the interface to the MCUs LIN protocol controller or SCI and UART that is used to control the state of the LIN output. When TXD is low the LIN output is dominant (near ground). When TXD is high the LIN output is recessive (near $V_{Battery}$). See 图 7-1. The TXD input structure is compatible with micrcontrollers with 3.3V and 5V I/O.

7.3.3 RXD (Receive Output)

RXD is the interface to the MCUs LIN protocol controller or SCI and UART, which reports the state of the LIN bus voltage. LIN recessive (near $V_{Battery}$) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3V and 5V I/O micrcontrollers. If the micrcontroller RXD pin does not have an integrated pull-up, an external pull-up resistor to the micrcontroller I/O supply voltage is required. In standby mode, the RXD pin is driven low to indicate a wake up request from the LIN bus.

7.3.4 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse-blocking diode (图 7-1). If there is a loss of power at the ECU level, the device has extremely low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

7.3.5 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage. Making sure the input and output voltages are within their appropriate thresholds. If there is a loss of ground at the ECU level, the device has low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

7.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after wake up. EN has an internal pull-down resistor to make sure the device remains in low-power mode even if EN floats.

7.3.7 Protection Features

The TLIN2029A-Q1 has several protection features that will now be described.

7.3.8 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure. The LIN bus is protected by the dominant state timeout timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{DST}, the transmitter is disabled, thus, allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{DST} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-down to make sure the device fails to a known state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of stated request on EN), the transmitter is disabled, the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on.

7.3.9 Bus Stuck Dominant System Fault: False Wake Up Lockout

The TLIN2029A-Q1 contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current consumption. 图 7-2 and 图 7-3 show the behavior of this protection.

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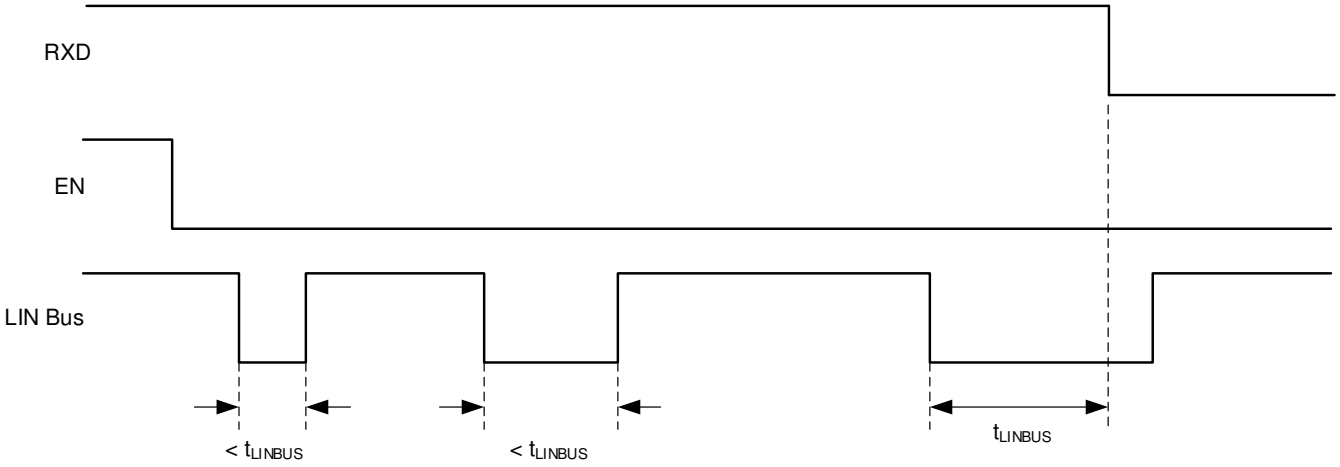


图 7-2. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wakeup

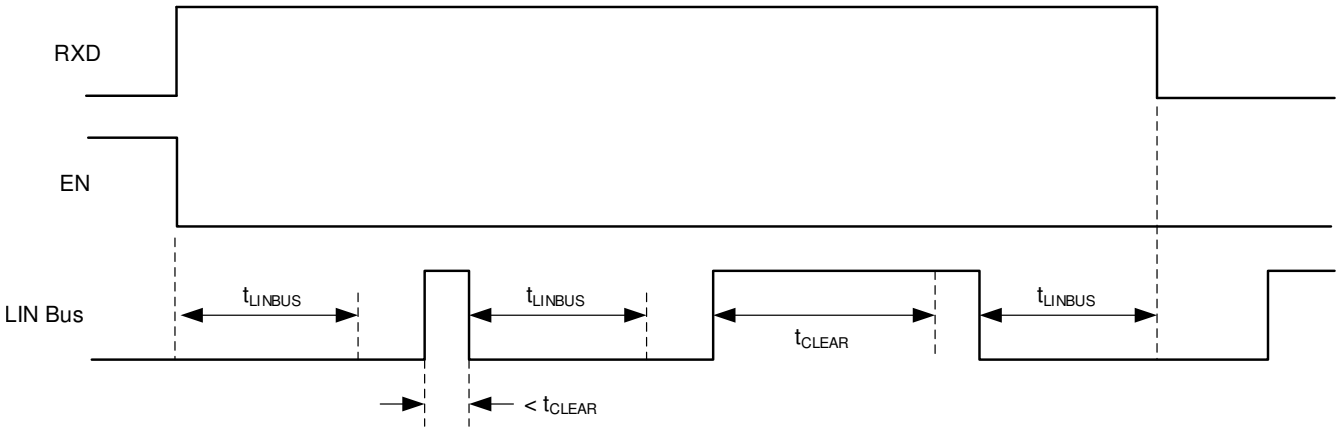


图 7-3. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wakeup

7.3.10 Thermal Shutdown

The LIN transmitter is protected by current limiting circuitry; however, if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state. Once the over-temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled, assuming the device remained in the normal operation mode. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the transmitter is in recessive state, the RXD pin reflects the LIN bus and LIN bus pull-up termination remains on.

7.3.11 Under Voltage on V_{SUP}

The TLIN2029A-Q1 contains a power-on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP}.

7.3.12 Unpowered Device and LIN Bus

In automotive applications, some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remain powered by the battery. The TLIN2029A-Q1 has a low unpowered leakage current from the bus, so an unpowered node does not affect the network or load it down.

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7.4 Device Functional Modes

The TLIN2029A-Q1 has three functional modes of operation: normal, sleep, and standby. The next sections will describe these modes as well as how the device moves between the different modes. 图 7-4 graphically shows the relationship while 表 7-1 shows the state of pins.

表 7-1. Operating Modes

MODE	EN	RXD	LIN BUS TERMINATION	TRANSMITTER	COMMENT
Sleep	Low	Floating	Weak current pull-up	Off	
Standby	Low	Low	45 kΩ (typical)	Off	Wake-up event detected, waiting on MCU to set EN
Normal	High	LIN bus data	45 kΩ (typical)	On	LIN transmission up to 20 kbps

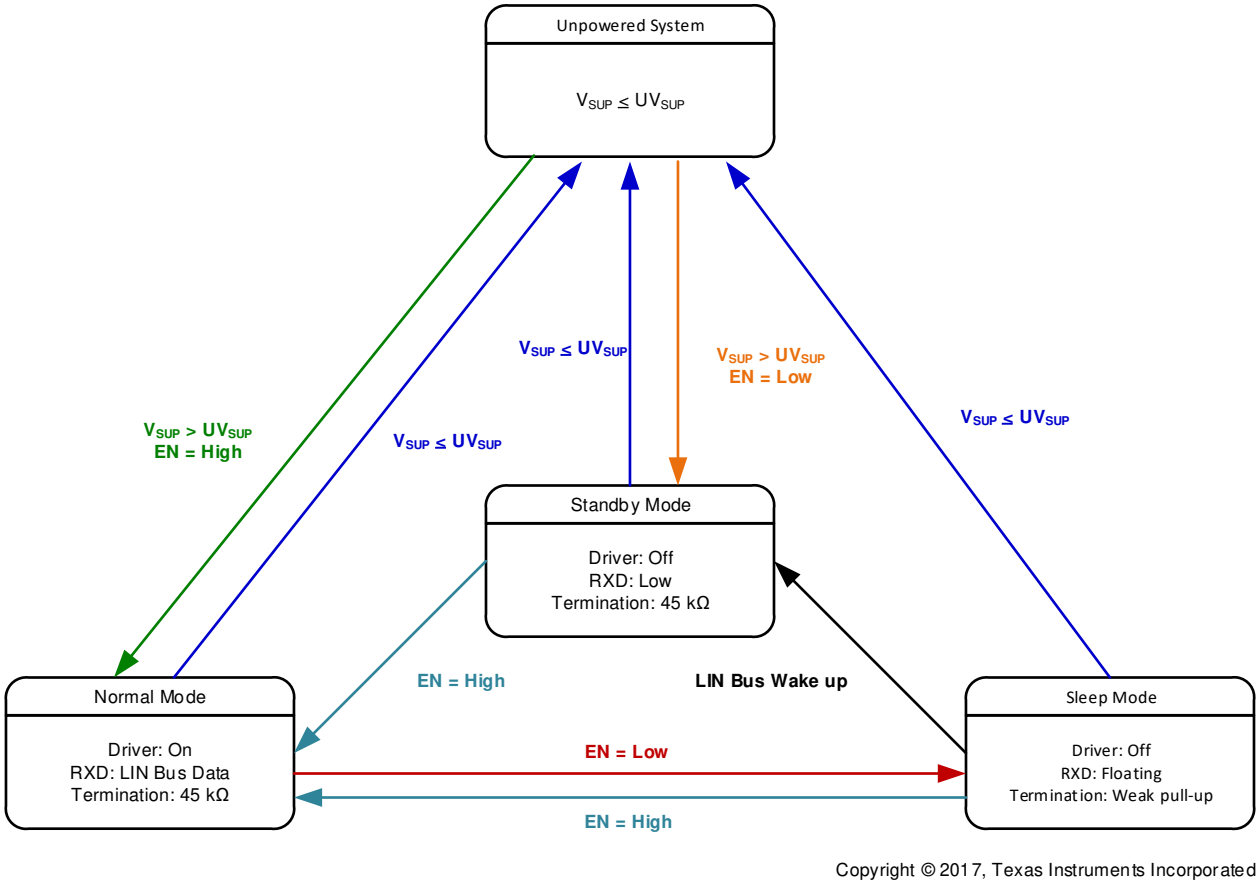


图 7-4. Operating State Diagram

7.4.1 Normal Mode

If the EN pin is high at power up, the device powers up in normal mode. If the EN pin is low, it powers up in standby mode. The EN pin controls the mode of the device. In normal operational mode, the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a logic high and a dominant signal on the LIN bus is a logic low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while the TLIN2029A-Q1 is in sleep or standby mode for > t_{MODE_CHANGE} plus t_{NOMINT}.

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7.4.2 Sleep Mode

Sleep mode is the power saving mode for the TLIN2029A-Q1. Sleep mode is only entered when the EN pin is low and from normal mode. Even with a low current consumption in this mode, the TLIN2029A-Q1 can still wake up from LIN bus through a wake-up signal or if EN is set high for ≥ t_{MODE_CHANGE}. The LIN bus is filtered to prevent false wake up events. The wake-up events must be active for the respective time periods (t_{LINBUS}).

The sleep mode is entered by setting EN low for longer than t_{MODE_CHANGE}.

While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short circuited to ground). However, the weak current pull-up is active to prevent false wake up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input and LIN wake up receiver are active.

7.4.3 Standby Mode

This mode is entered whenever a wake up event occurs through LIN bus while the device is in sleep mode. The LIN bus responder mode termination circuit is turned on when standby mode is entered. Standby mode is signaled through a low level on RXD. See 节 *8.2.2.2* for more application information.

When EN is set high for longer than t_{MODE_CHANGE} while the device is in standby mode, the device returns to normal mode. The normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

7.4.4 Wake Up Events

There are two ways to wake up from sleep mode:

- Remote wake up initiated by the falling edge of a recessive (high) to dominant (low) state transition on LIN bus where the dominant state is be held for t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake up event, eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake up through EN being set high for longer than t_{MODE_CHANGE}.

7.4.4.1 Wake Up Request (RXD)

When the TLIN2029A-Q1 encounters a wake up event from the LIN bus, RXD goes low, and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode, the RXD pin releases the wake up request signal and the RXD pin then reflects the receiver output from the LIN bus.

7.4.4.2 Mode Transitions

When the TLIN2029A-Q1 is transitioning from normal to sleep or standby modes the device needs the time t_{MODE_CHANGE} to allow the change to fully propagate from the EN pin through the device into the new state. When transitioning from sleep or standby to normal mode the device needs t_{MODE_CHANGE} plus t_{NOMINT}.

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8 Application Information Disclaimer

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

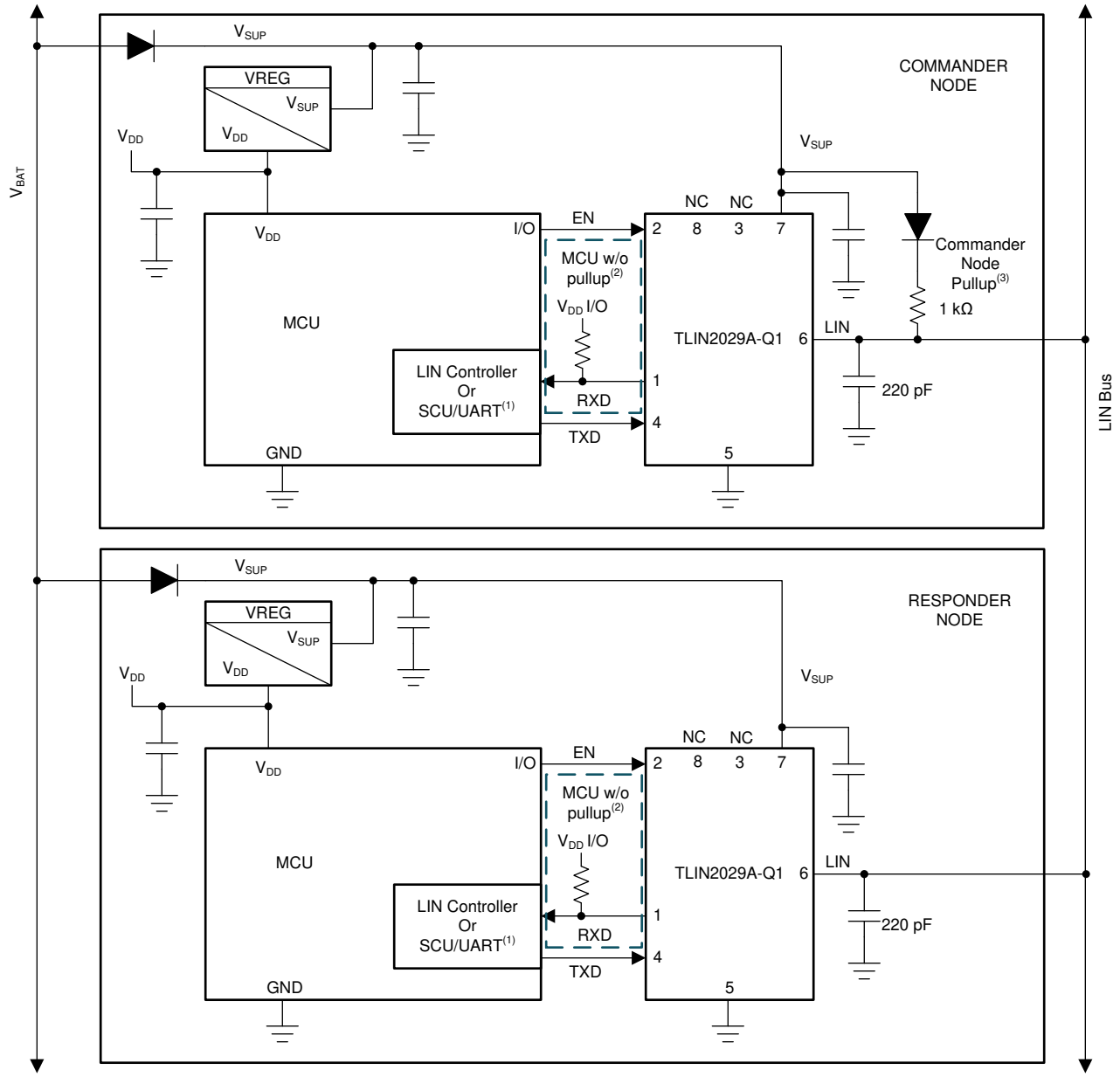
8.1 Application Information

The TLIN2029A-Q1 can be used as both a responder node device and a commander node device in a LIN network. The device comes with the ability to support both remote wake up request and local wake up request.

8.2 Typical Application

The device integrates a 45kΩ pull-up resistor and series diode for responder node applications. For commander applications, an external 1kΩ pull-up resistor with series blocking diode can be used. 图 8-1 shows the device being used in both commander mode and responder mode applications.

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A. If RXD on MCU on LIN responder node has internal pullup; no external pullup resistor is needed.
B. If RXD on MCU or LIN responder node does not have an internal pullup requires external pullup resistor.
C. Commander node applications require and external 1 kΩ pullup resistor and serial diode.
D. Decoupling capacitor values on V_{SUP} are system dependent but usually have 100nF, 1µF and ⩾ 10µF.

图 8-1. Typical LIN Bus

8.2.1 Design Requirements

The RXD output structure is an open-drain output stage. This allows the TLIN2029A-Q1 to be used with 3.3V and 5V I/O processor. If the RXD pin of the processor does not have an integrated pull-up, an external pull-up resistor to the processor I/O supply voltage is required. The select external pull-up resistor value should be between 1kΩ to 10kΩ, depending on supply used (See I_{OL} in *Electrical Characteristics*). The V_{SUP} pin of the device should be decoupled with a 100nF capacitor by placing it close to the V_{SUP} supply pin. The system should include additional decoupling on the V_{SUP} line as needed per the application requirements.

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8.2.2 Detailed Design Procedures

8.2.2.1 Normal Mode Application Note

When using the TLIN2029A-Q1 in systems which are monitoring the RXD pin for a wake up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake up request until t_{MODE_CHANGE}. This is shown in 图 6-14

8.2.2.2 Standby Mode Application Note

If the TLIN2029A-Q1 detects an under voltage on V_{SUP}, the RXD pin transitions low and would signal to the software that the TLIN2029A-Q1 is in standby mode and should be returned to sleep mode for the lowest power state.

8.2.3 Application Curves

The following figures show the propagation delay from the TXD pin to the LIN pin for both dominant to recessive and recessive to dominant edges. The device was configured in commander mode with external pull-up resistor (1kΩ) and 680pF bus capacitance.

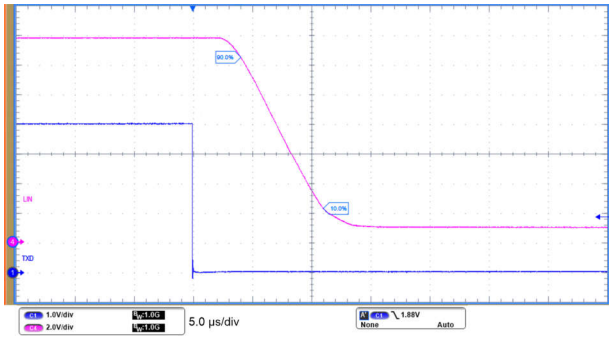


图 8-2. Recessive to Dominant Propagation

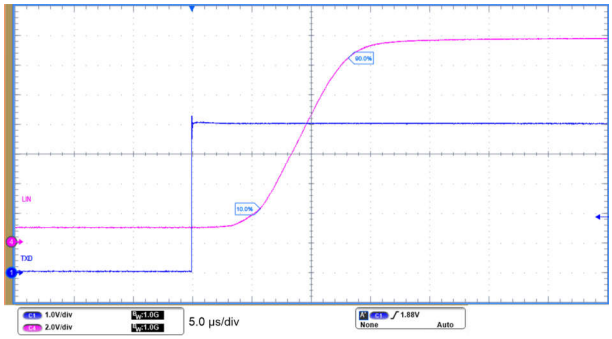


图 8-3. Dominant to Recessive Propagation

8.3 Power Supply Recommendations

The TLIN2029A-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 4V to 36V. A 100nF decoupling capacitor should be placed as close to the V_{SUP} pin of the device as possible. It is good practice for some applications with noisier supplies to include 1µF and 10µF decoupling capacitor, as well.

8.4 Layout

For the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

8.4.1 Layout Guidelines

- **Pin 1 (RXD):** The pin is an open-drain output and requires an external pull-up resistor in the range of 1kΩ to 10kΩ to function properly. Note that the minimum value depends on the V_{IO} supply used. See I_{OL} in electrical specifications. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external resistor should be placed between RXD and the regulated voltage supply for the microprocessor.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in a low-power sleep mode. If this feature is not used, the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor between 1 kΩ and 10 kΩ. Additionally, a series resistor may be placed on the pin to limit current on the digital lines in the case of an over voltage fault.
- **Pin 3 (NC):** Not Connected.

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- **Pin 4 (TXD):** The TXD pin is used to transmit the input signal from the microcontroller. A series resistor can be placed to limit the input current to the device if there is an over-voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 5 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 6 (LIN):** This pin connects to the LIN bus. For responder mode applications, a 220pF capacitor to ground is implemented. For commander mode applications, an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin. See 图 8-1.
- **Pin 7 (VSUP):** This is the supply pin for the device. A 100nF decoupling capacitor should be placed as close to the device as possible.
- **Pin 8 (NC):** Not Connected.

备注

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

8.4.2 Layout Example

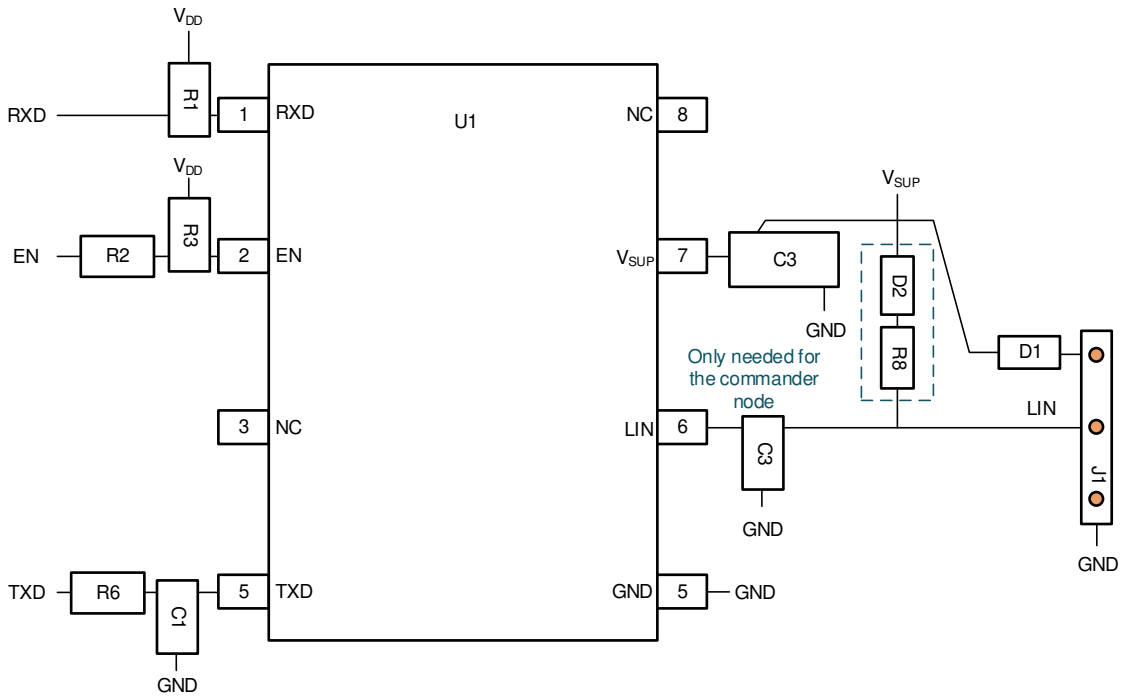


图 8-4. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- LIN Standards:
  - ISO/DIS 17987-1.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
  - ISO/DIS 17987-4.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V/24V
  - SAEJ2602-1: LIN Network for Vehicle Applications
  - LIN Specifications LIN 2.0, LIN 2.1, LIN 2.2 and LIN 2.2A
- EMC requirements:
  - SAEJ2962-1: Communication Transceivers Qualification Requirements - LIN
  - ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
  - ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
  - ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
  - ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
  - IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
  - IEC 61000-4-2
  - IEC 61967-4
  - CISPR25
- Conformance Test requirements:
  - ISO/DIS 17987-7.2: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
  - SAEJ2602-2: LIN Network for Vehicle Applications Conformance Test
-

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 支持资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (April 2022) to Revision B (February 2024)	Page
• 将“器件信息”表更改为*封装信息*表	1
• Updated the I_{BUS_LIM} values in the *Electrical Characteristics* table	6

Changes from Revision * (March 2021) to Revision A (April 2022)	Page
• 删除了原理图后面的注释	1
• 通篇将术语从“领导者和跟随者”更改为“指挥官和响应者”	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLIN2029ADRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL029A
TLIN2029ADRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL029A
TLIN2029ADRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TL029A
TLIN2029ADRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL029A
TLIN2029AMDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL029A
TLIN2029AMDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL029A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

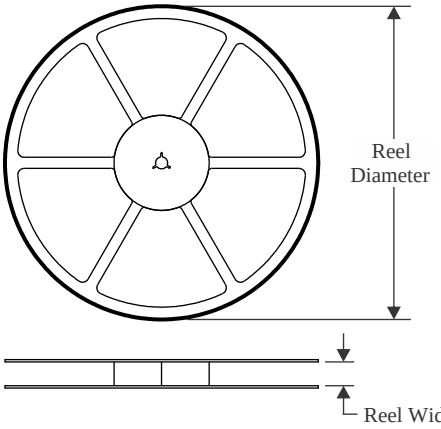
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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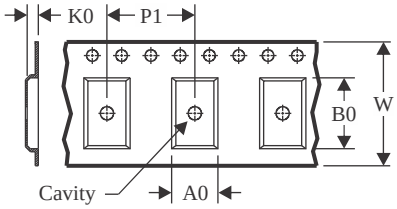
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

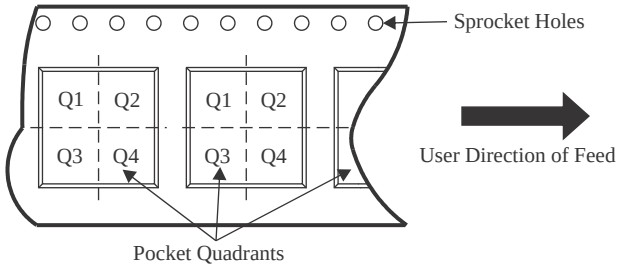


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

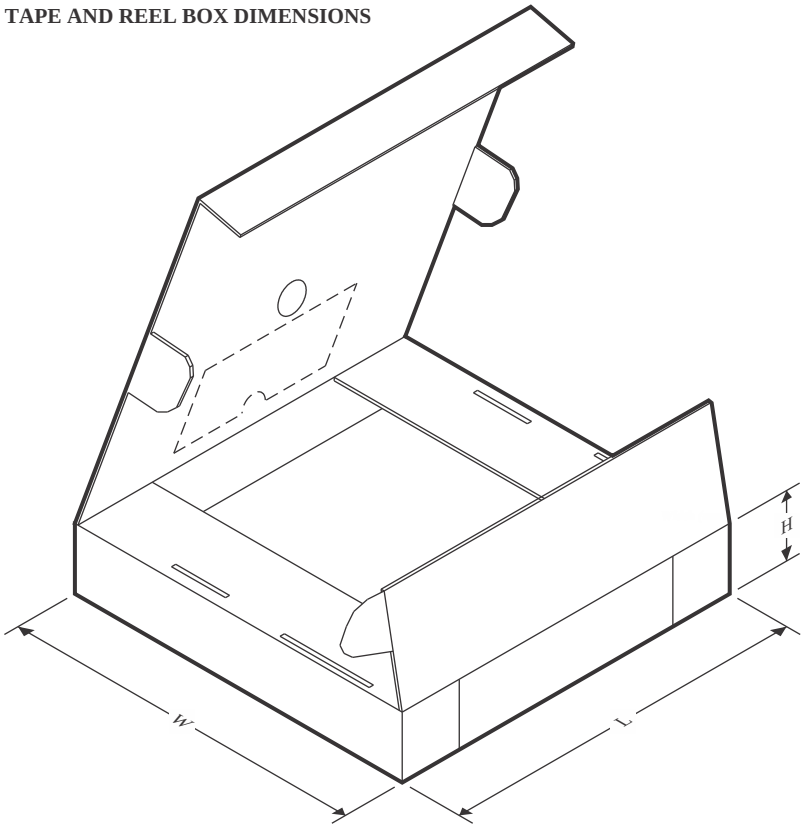
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLIN2029ADRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLIN2029ADRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLIN2029ADRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLIN2029AMDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLIN2029ADRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLIN2029ADRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLIN2029ADRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TLIN2029AMDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

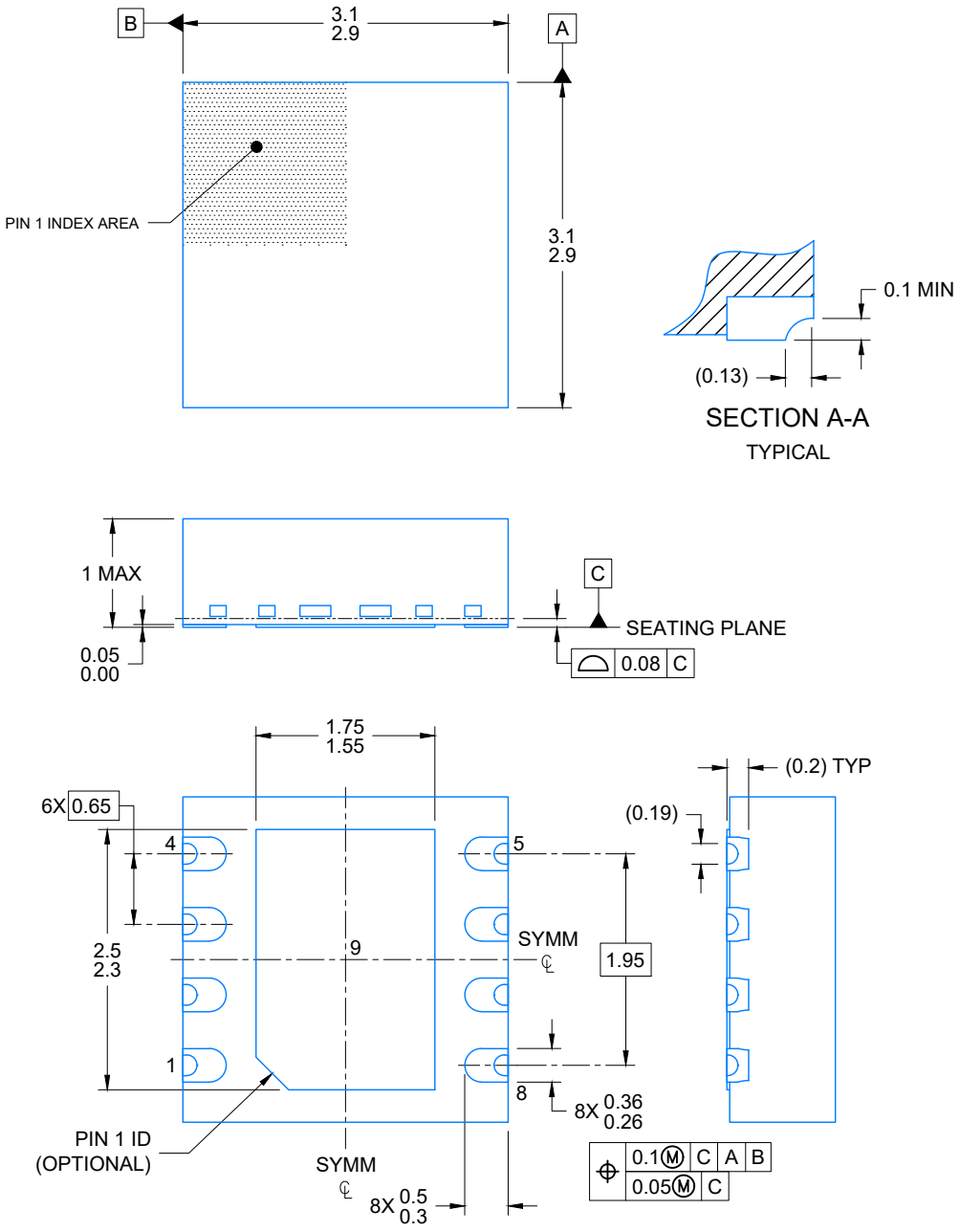
4203482/L

PACKAGE OUTLINE

DRB0008J

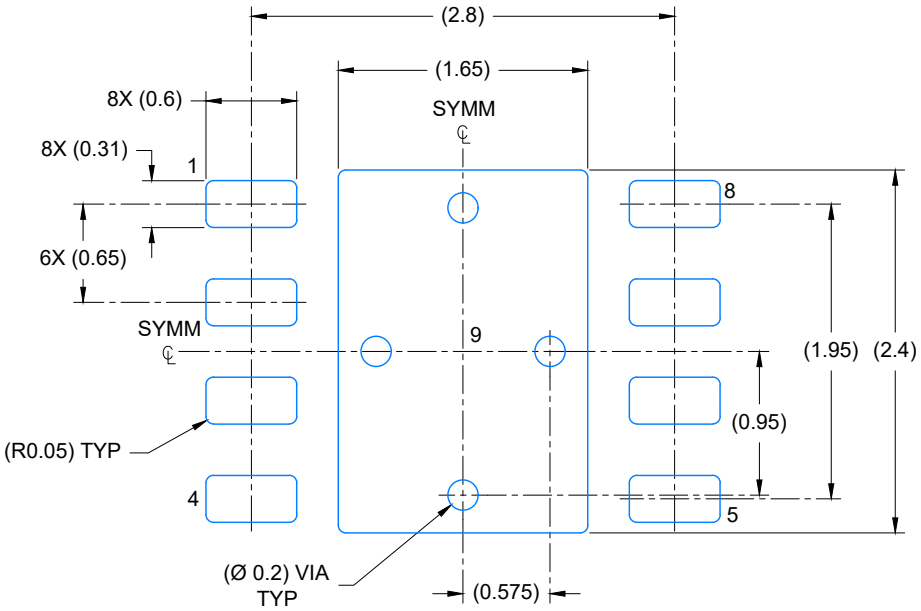
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

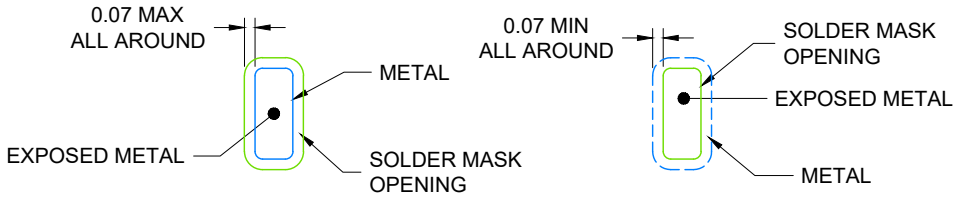


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

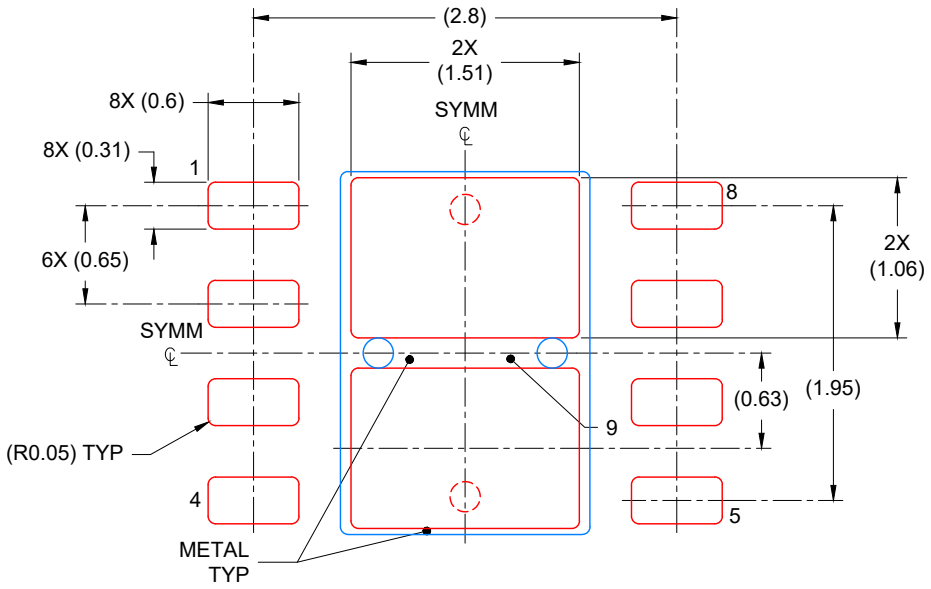
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



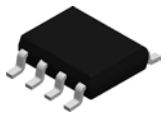
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

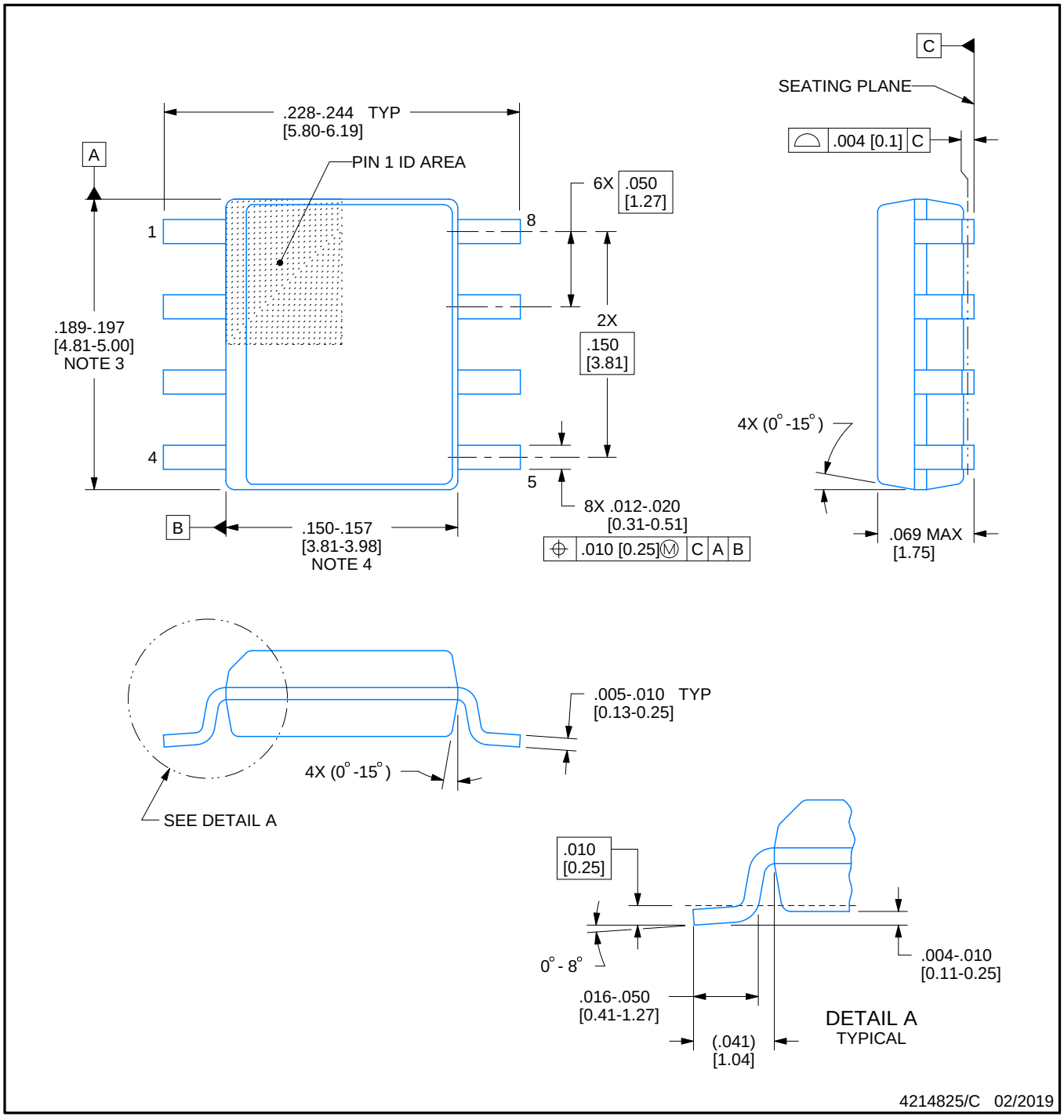


PACKAGE OUTLINE

D0008A

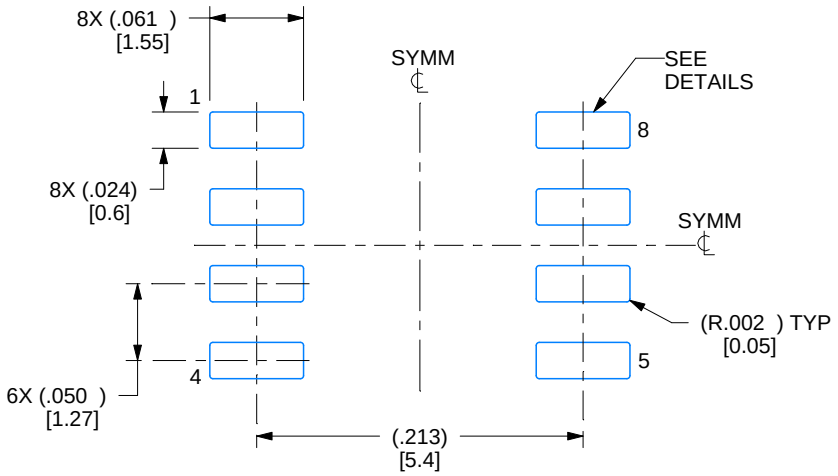
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

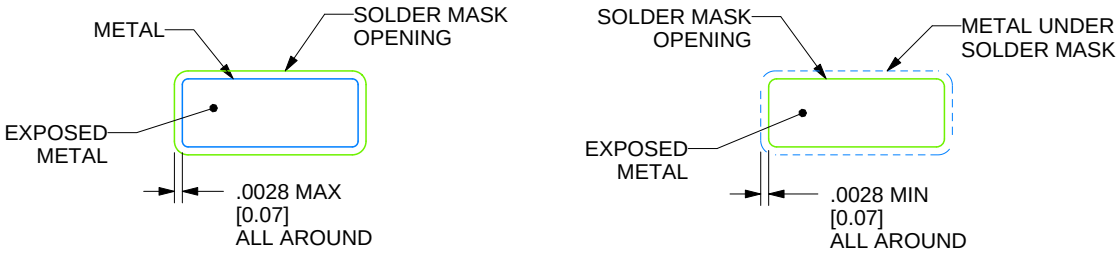


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

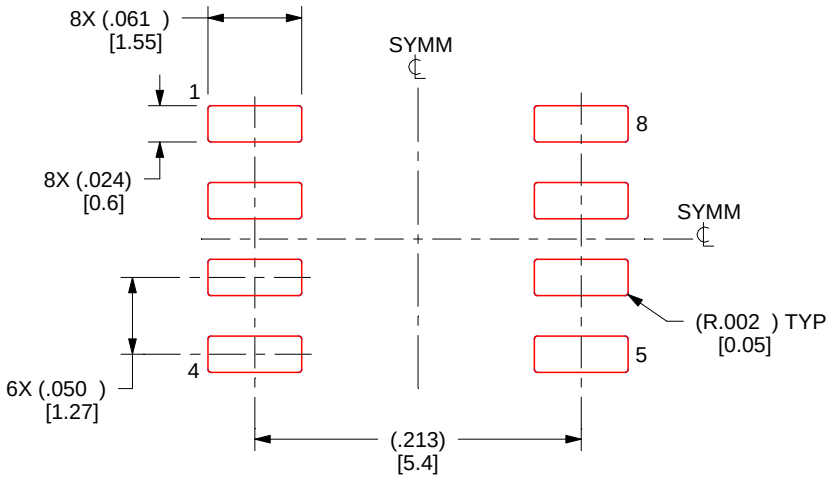
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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