TLV2221, TLV2221Y Advanced LinCMOS™ Rail-to-Rail Very Low-power Single Operational Amplifiers

1 Features

- Output Swing Includes Both Supply Rails
- Low Noise: $19nV/\sqrt{Hz}$ Typical at f = 1kHz
- Low Input Bias Current: ±10pA Typical
- Fully Specified for Single-Supply 3V and 5V Operation
- Very Low Power: 130μA Typical
- Common-Mode Input Voltage Range Includes Negative Rail
- Wide Supply Voltage Range: 2.7V to 10V

2 Description

The TLV2221 is a single low-voltage operational amplifier available in the SOT-23 package. TLV2221 offers a compromise between the ac performance and output drive of the TLV2231 and the micro-power TLV2211.

TLV2221 consumes only 150μA (max) of supply current and is designed for battery-powered applications. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications.

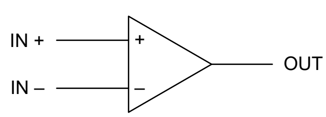
The TLV2221, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels combined with 3V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs).

With a total area of $5.6mm^2$, the SOT-23 package only requires one-third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long printed circuit board (PCB) traces. TI has also taken special care to provide a pinout that is optimized for board layout (see Typical Surface-Mount Layout for a Fixed-Gain Non-inverting Amplifier). Both inputs are separated by GND to prevent coupling or leakage paths. The OUT and IN− terminals are on the same end of the board to provide negative feedback. Finally, gain setting resistors and decoupling capacitor are easily placed around the package.

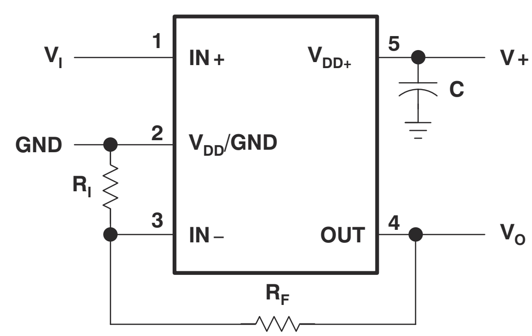
Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TLV2221	DBV (SOT-23, 5)	2.90mm × 1.60mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol (Each Amplifier)



Typical Surface-Mount Layout for a Fixed-Gain Non-inverting Amplifier

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3 Available Options

T_A	V_{IO}max AT +25°C	PACKAGED DEVICES SOT23 (DBV)(1)	SYMBOL
–40°C to +85°C	3mV	TLV2221IDBV	VADI

(1) The DBV package is available in tape and reel only.

4 Pin Configuration and Functions

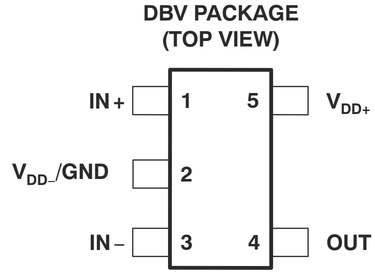


Figure 4-1. TLV2221, TLV2221Y DBV Package, 5-pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN-	3	I	Inverted input
IN+	1	I	Non inverted input
OUT	4	O	Output
V_{DD-}/GND	2	P/G	Ground or negative power supply
V_{DD+}	5	P	Positive power supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P= Power, G = Ground.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.

[1]	TLV2221	UNIT
Supply voltage, V_{DD} [2]	12	V
Differential input voltage, V_{ID} [3]	$\pm V_{DD}$	V
Input voltage range, V_I (any input[2])	–0.3 to V_{DD}	V
Input current, I_I (each input)	±5	mA
Output current, I_O	±50	mA
Duration of short-circuit current (at or below) +25°C[4]	Unlimited	
Continuous total power dissipation	See Dissipation Ratings Table	
Operating free-air temperature range, T_A: TLV2221I	–40 to +85	°C
Storage temperature range, T_{stg}	–65 to +150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential voltages, are with respect to V_{DD-}.
(3) Differential voltages are at the non-inverting input with respect to the inverting input. Excessive current flows when input is brought below (V_{DD-}) – (0.3V).
(4) The output can be shorted to either supply. Temperature and/or supply voltages must be limited to make sure that the maximum dissipation rating is not exceeded.

5.2 Dissipation Ratings Table for Old Device

PACKAGE	$T_A \le$ +25°C POWER RATING	DERATING FACTOR ABOVE T_A = +25°C	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
DBV	150mW	1.2mW/°C	96mW	78mW

5.3 Thermal Information for New device

THERMAL METRIC [1]		DBV (SOT-23)	UNIT
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	113.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	37.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	60.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.4 Recommended Operating Conditions

	TLV2221I		UNIT
	MIN	MAX	
Supply voltage, V_{DD} [1]	2.7	10	V
Input voltage range, V_I	V_{DD-}	$(V_{DD+}) - (1.3)$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$(V_{DD+}) - (1.3)$	V

5.4 Recommended Operating Conditions (continued)

	TLV2221I		UNIT
	MIN	MAX	
Operating free-air temperature, T_A	–40	+85	°C

(1) All voltage values, except differential voltages, are with respect to V_{DD-}.

5.5 Electrical Characteristics: V_{DD} = 3V

At specified free-air temperature, unless otherwise noted.

PARAMETER		TEST CONDITIONS		T_A (1)	TLV2221I			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5V, V_{IC} = 0, V_O = 0, R_S = 50Ω		Full range		±0.3	3	mV
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD\pm}$ = ±1.5V, V_{IC} = 0, V_O = 0, R_S = 50Ω		Full range		±0.6		μV/°C
I_{IO}	Input offset current	$V_{DD\pm}$ = ±1.5V, V_{IC} = 0, V_O = 0, R_S = 50Ω		+25°C		±5		pA
I_{IB}	Input bias current	$V_{DD\pm}$ = ±1.5V, V_{IC} = 0, V_O = 0, R_S = 50Ω		+25°C		±10		pA
V_{ICR}	Common-mode input voltage range	R_S = 50Ω, $\|V_{IO}\|$ ≤ 5mV		+25°C	0 to 2	–0.3 to 2.2		V
				Full range	0 to 1.7			V
V_{OH}	High-level output voltage	I_{OH} = –100μA		+25°C		2.97		V
		I_{OH} = –400μA		+25°C		2.88		V
V_{OL}	Low-level output voltage	V_{IC} = 1.5V, I_{OL} = 50μA		+25°C		15		mV
		V_{IC} = 1.5V, I_{OL} = 500μA		+25°C		150		mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5V, V_O = 1V to 2V	R_L = 2kΩ(2)	+25°C	66	118		dB
				Full range	60			dB
			R_L = 1MΩ(2)	+25°C		108		dB
r_{id}	Differential input resistance			+25°C		540		GΩ
r_{ic}	Common-mode input resistance			+25°C		6		TΩ
c_{ic}	Common-mode input capacitance	f = 10kHz		+25°C		6		pF
z_o	Closed-loop output impedance	f = 10kHz, A_V = 10		+25°C		575		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0V to 1.7V, V_O = 1.5V, R_S = 50Ω		+25°C	70	90		dB
				Full range	65			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7V to 8V, V_{IC} = V_{DD}/2, no load		+25°C	80	95		dB
				Full range	80			dB
I_{DD}	Supply current	V_O = 1.5V, no load		+25°C		130	150	μA
				Full range			200	μA

(1) Full range for the TLV2221C is 0°C to +70°C. Full range for the TLV2221I is –40°C to +85°C.
(2) Referenced to 1.5V.

5.6 Operating Characteristics: V_{DD} = 3V

At specified free-air temperature, unless otherwise noted.

PARAMETER		TEST CONDITIONS		T_A [1]	TLV2221I MIN	TLV2221I TYP	TLV2221I MAX	UNIT
SR	Slew rate at unity gain	C_L = 20pF[2]		+25°C		4.5		V/μs
V_n	Equivalent input noise voltage	f = 10kHz		+25°C		28		$nV/\sqrt{Hz}$
		f = 1kHz		+25°C		30		$nV/\sqrt{Hz}$
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1Hz to 10Hz		+25°C		6		μV_{pp}
I_n	Equivalent input noise current	f = 1kHz		+25°C		2		$fA/\sqrt{Hz}$
THD+N	Total harmonic distortion plus noise	V_O = 1V to 2V, f = 20kHz, R_L = 2kΩ[2]	A_V = 1	+25°C		2.52		%
			A_V = 10	+25°C		7.01		%
		V_O = 1V to 2V, f = 20kHz, R_L = 2kΩ[3]	A_V = 1	+25°C		0.076		%
			A_V = 10	+25°C		0.147		%
	Gain-bandwidth product			+25°C		1.1		MHz
t_s	Settling time	A_V = –1, Step = 1V to 2V, R_L = 2kΩ[2], C_L = 100pF[2]	To 0.1%	+25°C		4.5		μs
			To 0.01%	+25°C		6.8		μs

(1) Full range is –40°C to 85°C.
(2) Referenced to 1.5V.
(3) Referenced to 0V.

5.7 Electrical Characteristics: V_{DD} = 5V

At specified free-air temperature, unless otherwise noted.

PARAMETER		TEST CONDITIONS		T_A [(1)]	TLV2221I MIN	TLV2221I TYP	TLV2221I MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5V, V_{IC} = 0, V_O = 0, R_S = 50Ω		Full range		±0.3	3	mV
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD\pm}$ = ±2.5V, V_{IC} = 0, V_O = 0, R_S = 50Ω		Full range		±0.6		μV/°C
I_{IO}	Input offset current	$V_{DD\pm}$ = ±2.5V, V_{IC} = 0, V_O = 0, R_S = 50Ω		+25°C		±5		pA
I_{IB}	Input bias current	$V_{DD\pm}$ = ±2.5V, V_{IC} = 0, V_O = 0, R_S = 50Ω		+25°C		±10		pA
V_{ICR}	Common-mode input voltage range	R_S = 50Ω, $\lvert V_{IO}\rvert$ ≤ 5mV		+25°C	0 to 4	–0.3 to 4.2		V
				Full range	0 to 3.5			V
V_{OH}	High-level output voltage	I_{OH} = –500 μA		+25°C	4.75	4.88		V
		I_{OH} = –1mA		+25°C	4.5	4.76		V
V_{OL}	Low-level output voltage	V_{IC} = 2.5V, I_{OL} = 50μA		+25°C		12		mV
		V_{IC} = 2.5V, I_{OL} = 500μA		+25°C		120		mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5V, V_O = 1V to 4V	R_L = 2kΩ[(2)]	+25°C	69.5	130		dB
				Full range	60			
			R_L = 10kΩ[(2)]	+25°C		130		
r_{id}	Differential input resistance			+25°C		540		GΩ
r_{ic}	Common-mode input resistance			+25°C		6		TΩ
c_{ic}	Common-mode input capacitance	f = 10kHz		+25°C		6		pF
z_o	Closed-loop output impedance	f = 10kHz, A_V = 10		+25°C		575		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0V to 2.7V, V_O = 1.5V, R_S = 50Ω		+25°C	70	90		dB
				Full range	65			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4V to 8V, V_{IC} = V_{DD}/2, no load		+25°C	80	95		dB
				Full range	80			dB
I_{DD}	Supply current	V_O = 2.5V, no load		+25°C		130	150	μA
				Full range			200	μA

(1) Full range for the TLV2221C is 0°C to +70°C. Full range for the TLV2221I is –40°C to +85°C.
(2) Referenced to 2.5V.

5.8 Operating Characteristics: V_{DD} = 5V

At specified free-air temperature, unless otherwise noted.

PARAMETER		TEST CONDITIONS		T_A [1]	TLV2221I MIN	TLV2221I TYP	TLV2221I MAX	UNIT
SR	Slew rate at unity gain	C_L = 20pF[2]		+25°C		4.5		V/μs
V_n	Equivalent input noise voltage	f = 10kHz		+25°C		28		$nV/\sqrt{Hz}$
		f = 1kHz		+25°C		30		$nV/\sqrt{Hz}$
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1Hz to 10Hz		+25°C		6		μV_{pp}
I_n	Equivalent input noise current	f = 1kHz		+25°C		2		$fA/\sqrt{Hz}$
THD+N	Total harmonic distortion plus noise	V_O = 1.5V to 3.5V, f = 20kHz, R_L = 2kΩ[2]	A_V = 1	+25°C		2.45		%
			A_V = 10	+25°C		5.54		%
		V_O = 1.5V to 3.5V, f = 20kHz, R_L = 2kΩ[3]	A_V = 1	+25°C		0.142		%
			A_V = 10	+25°C		0.257		%
	Gain-bandwidth product			+25°C		1.1		MHz
t_s	Settling time	A_V = –1, Step = 1.5V to 3.5V, R_L = 2kΩ[2], C_L = 100pF[2]	To 0.1%	+25°C		6.8		μs
			To 0.01%	+25°C		9.2		μs

(1) Full range is –40°C to +85°C.
(2) Referenced to 2.5V.
(3) Referenced to 0V.

5.9 Typical Characteristics

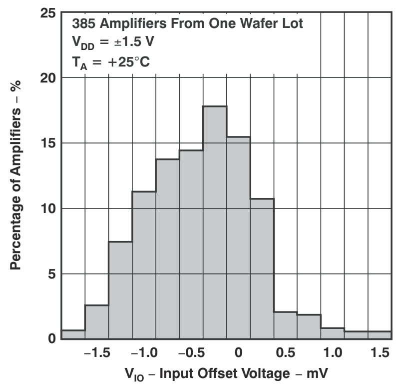


Figure 5-1. Distribution of TLV2221 Input Offset Voltage (Old Die)

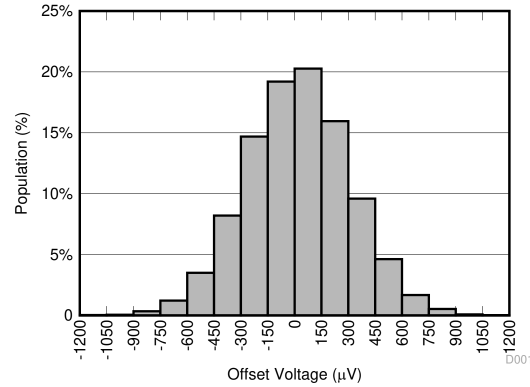
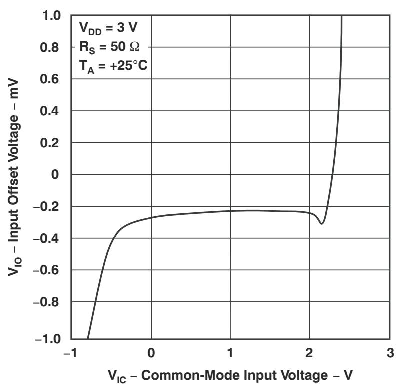


Figure 5-2. Distribution of TLV2221 Input Offset Voltage (New Die)



Note

1

Figure 5-3. Input Offset Voltage vs Common-mode Input Voltage (Old Die)

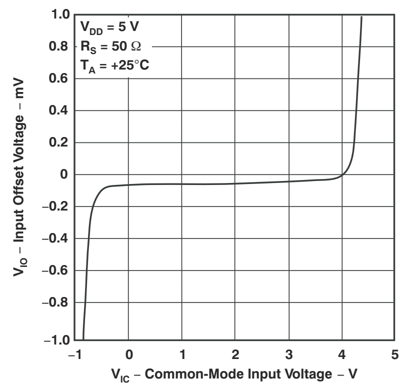
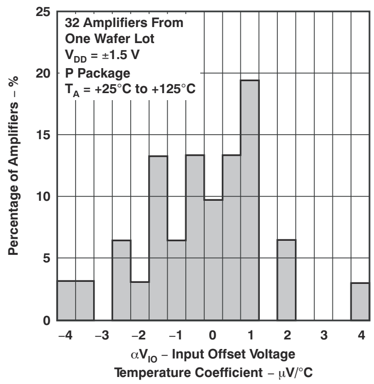


Figure 5-4. Input Offset Voltage vs Common-mode Input VOLTAGE (Old Die)(1)

[1] For all curves where V_{DD} = 5V, all loads are referenced to 2.5V. For all curves where V_{DD} = 3V, all loads are referenced to 1.5V.



Note

[2]

Figure 5-5. Distribution of TLV2221 Input Offset Voltage Temperature Coefficient (Old Die)

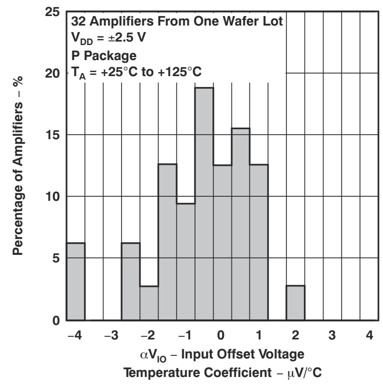
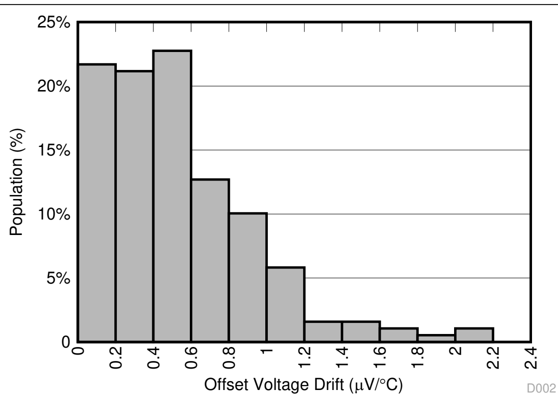


Figure 5-6. Distribution of TLV2221 Input Offset Voltage Temperature Coefficient (Old Die)[2]



Distribution from 175 amplifiers

Figure 5-7. Offset Voltage Drift Distribution (New Die)

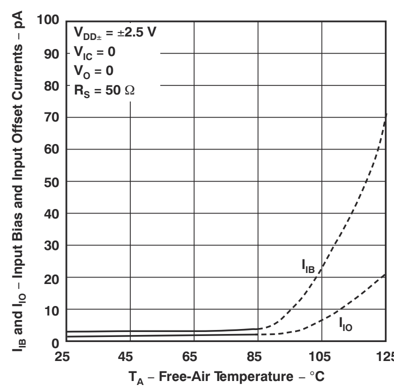


Figure 5-8. Input Bias and Input Offset Currents vs Free-air Temperature (Old Die)

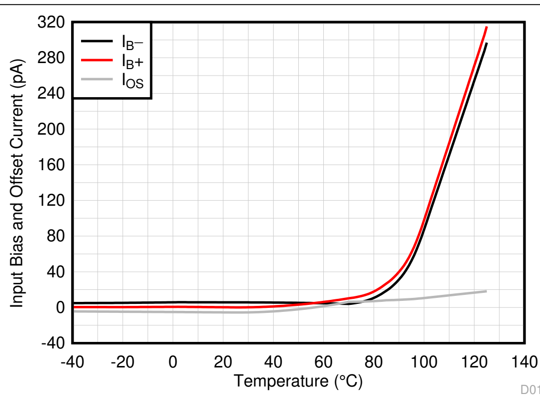


Figure 5-9. Input Bias Current vs Temperature (New Die)

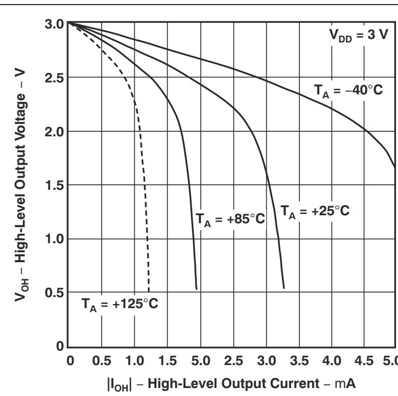


Figure 5-10. High-level Output Voltage vs High-level Output Current (Old Die)[3] [4]

[2] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

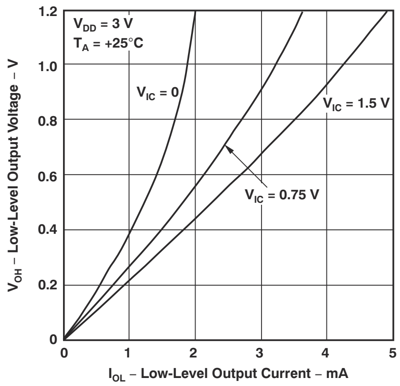


Figure 5-11. Low-level Output Voltage vs Low-level Output Current (Old Die)[4]

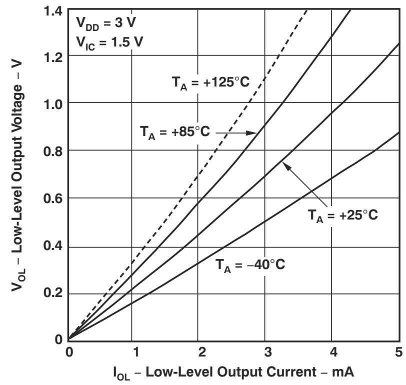
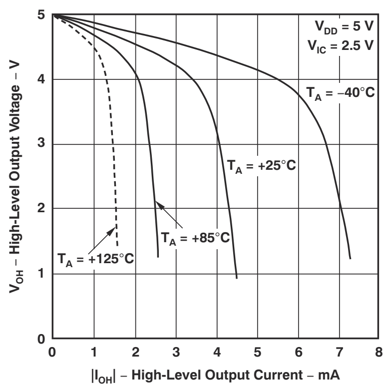


Figure 5-12. Low-level Output Voltage vs Low-level Output Current (Old Die)[3] [4]



3 4

Figure 5-13. High-level Output Voltage vs High-level Output Current (Old Die)

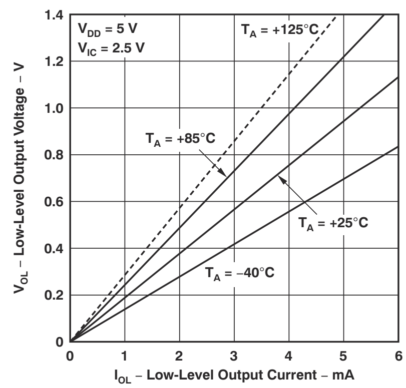


Figure 5-14. Low-level Output Voltage vs Low-level Output Current (Old Die)[5] [6]

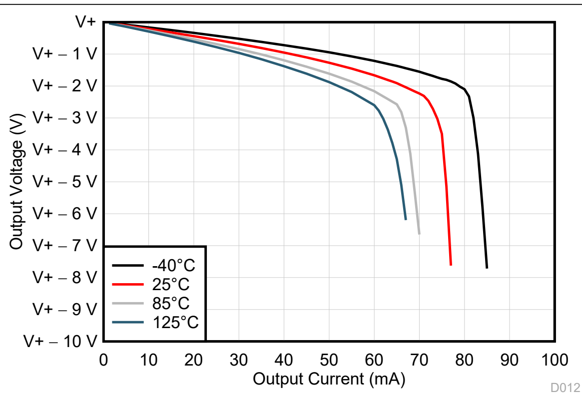


Figure 5-15. Output Voltage Swing vs Output Current (Sourcing) (New Die)

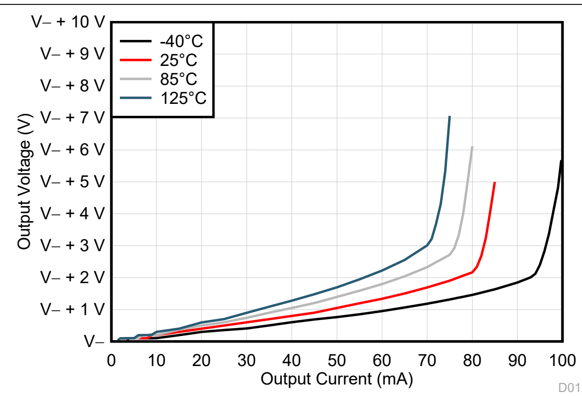


Figure 5-16. Output Voltage Swing vs Output Current (Sinking) (New Die)

3 Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

4 For all curves where V_{DD} = 5V, all loads are referenced to 2.5V. For all curves where V_{DD} = 3V, all loads are referenced to 1.5V.

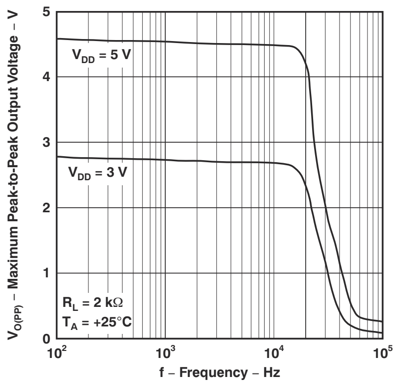
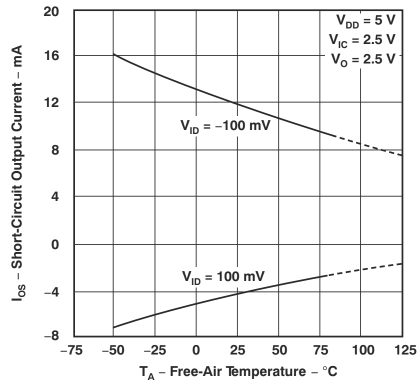
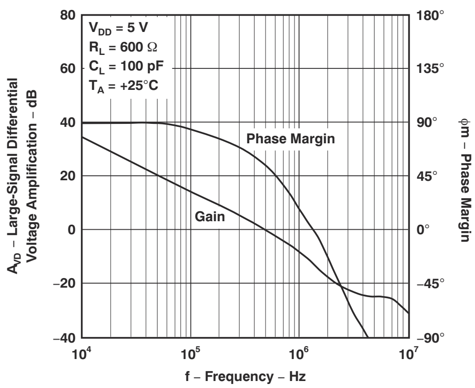


Figure 5-17. Maximum Peak-to-peak Output Voltage vs Frequency (Old Die)[6]



[5] [6]

Figure 5-18. Short-circuit Output Current vs Free-air Temperature (Old Die)



[7]

Figure 5-19. Large-signal Differential Voltage Amplification and Phase Margin vs Frequency (Old Die)

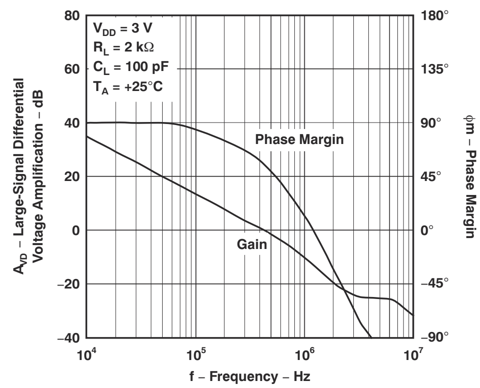
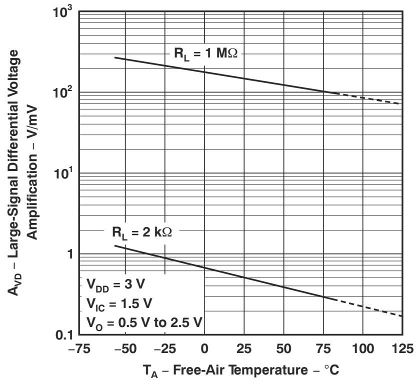


Figure 5-20. Large-signal Differential Voltage Amplification and Phase Margin vs Frequency (Old Die)[9]

[5] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
[6] For all curves where V_{DD} = 5V, all loads are referenced to 2.5V. For all curves where V_{DD} = 3V, all loads are referenced to 1.5V.
[7] For all curves where V_{DD} = 5V, all loads are referenced to 2.5V. For all curves where V_{DD} = 3V, all loads are referenced to 1.5V.



[8] [9]

Figure 5-21. Large-signal Differential Voltage Amplification vs Free-air Temperature (Old Die)

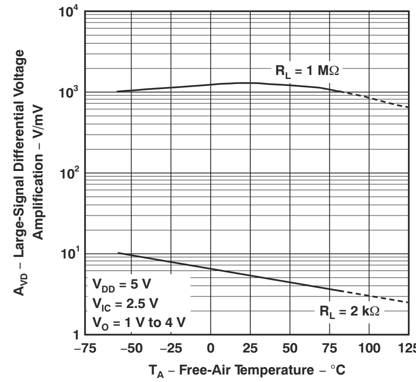


Figure 5-22. Large-signal Differential Voltage Amplification vs Free-air Temperature (Old Die)[10] [11]

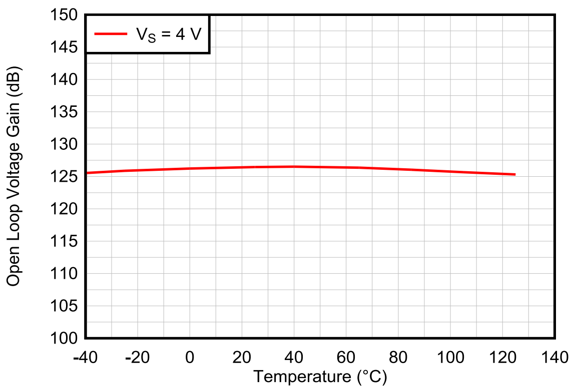


Figure 5-23. Open-Loop Voltage Gain vs Temperature (dB) (New Die)

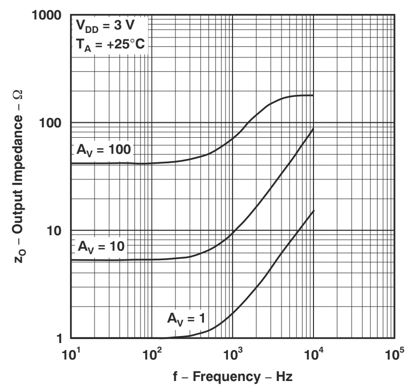


Figure 5-24. Output Impedance vs Frequency (Old Die)[11]

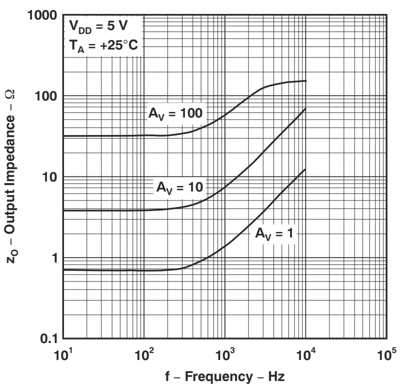


Figure 5-25. Output Impedance vs Frequency (Old Die)[11]

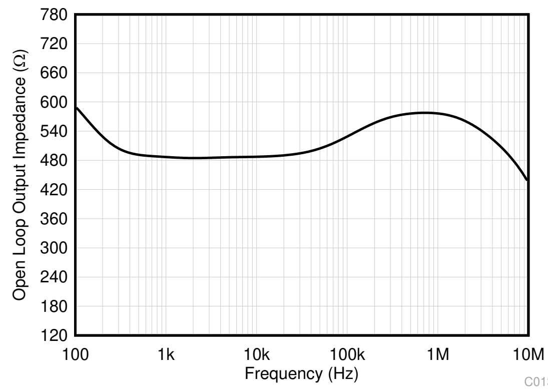
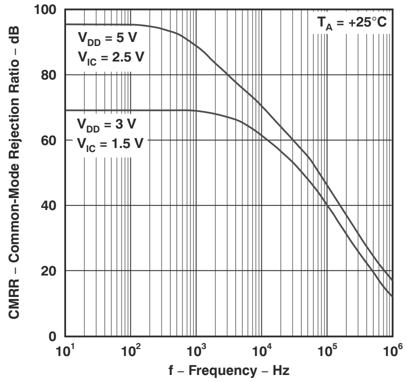


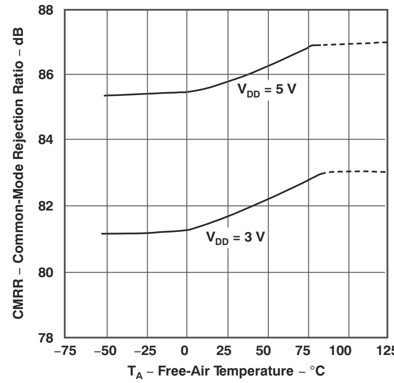
Figure 5-26. Open-Loop Output Impedance vs Frequency (New Die)

8 Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
9 For all curves where V_{DD} = 5V, all loads are referenced to 2.5V. For all curves where V_{DD} = 3V, all loads are referenced to 1.5V.



[10]

Figure 5-27. Common-mode Rejection Ratio vs Frequency (Old Die)



[11]

Figure 5-28. Common-mode Rejection Ratio vs Free-air Temperature (Old Die)[12]

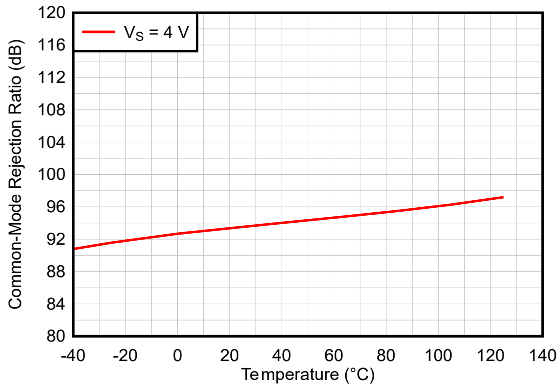


Figure 5-29. CMRR vs Temperature (dB) (New Die)

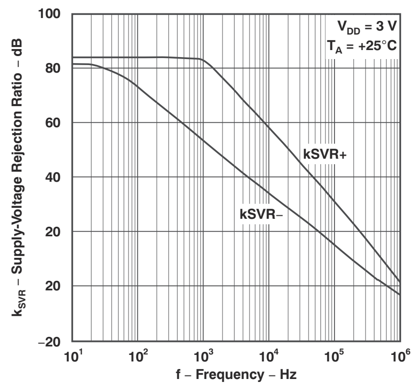


Figure 5-30. Supply Voltage Rejection Ratio vs Frequency (Old Die)[12]

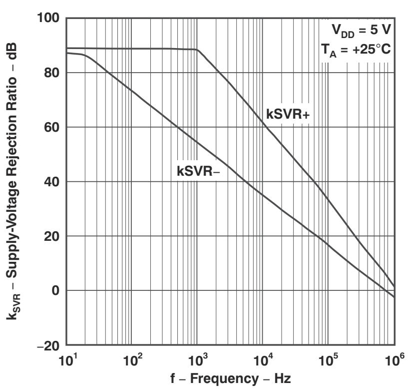


Figure 5-31. Supply-voltage Rejection Ratio vs Frequency (Old Die)[12]

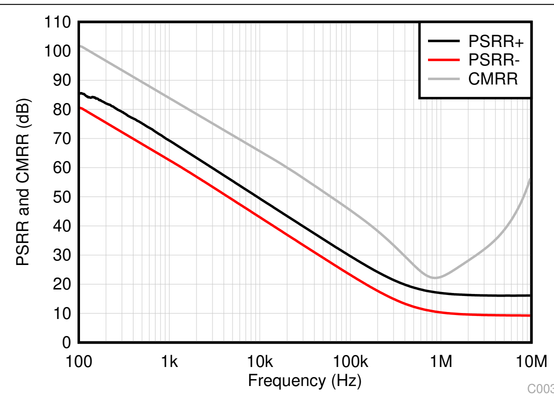
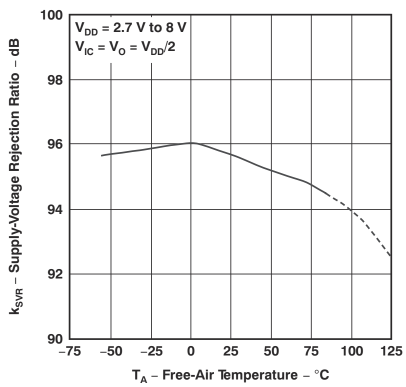


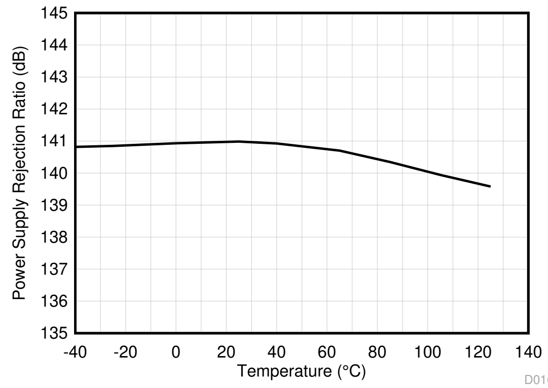
Figure 5-32. CMRR and PSRR vs Frequency (New Die)

10 For all curves where V_{DD} = 5V, all loads are referenced to 2.5V. For all curves where V_{DD} = 3V, all loads are referenced to 1.5V.
11 Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



12

Figure 5-33. Supply-voltage Rejection Ratio vs Free-air Temperature (Old Die)



f = 0Hz

Figure 5-34. PSRR vs Temperature (dB) (New Die)

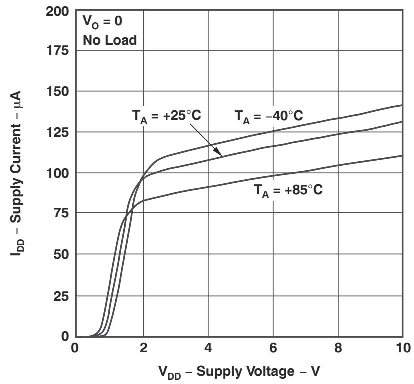


Figure 5-35. Supply Current vs Supply Voltage (Old Die)[14]

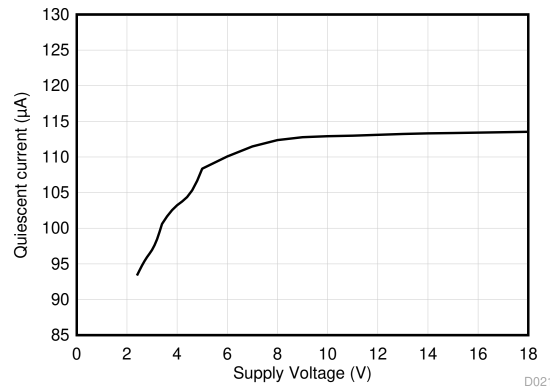


Figure 5-36. Quiescent Current vs Supply Voltage (New Die)

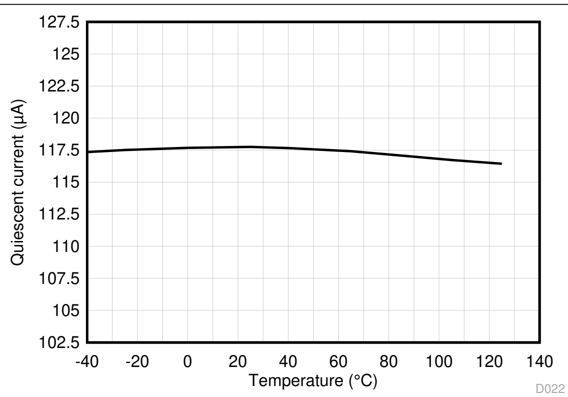
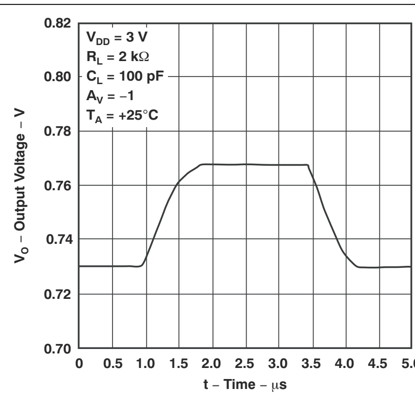


Figure 5-37. Quiescent Current vs Temperature (New Die)



13

Figure 5-38. Inverting Small-signal Pulse Response (Old Die)

12 Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
13 For all curves where V_{DD} = 5V, all loads are referenced to 2.5V. For all curves where V_{DD} = 3V, all loads are referenced to 1.5V.

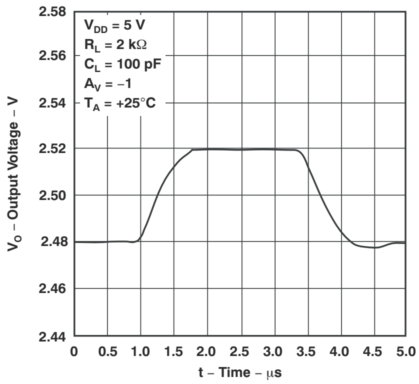


Figure 5-39. Inverting Small-signal Pulse Response (Old Die)(17)

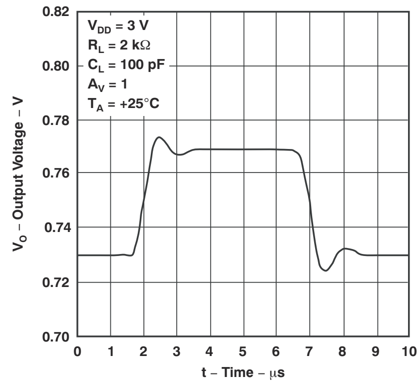


Figure 5-40. Voltage-follower Small-signal Pulse Response (Old Die)(17)

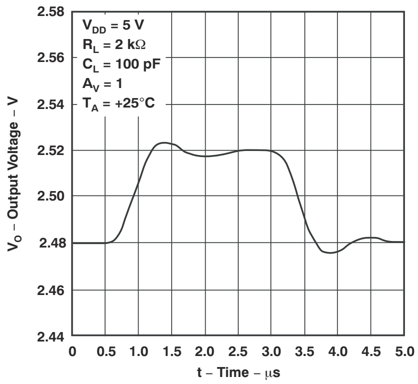
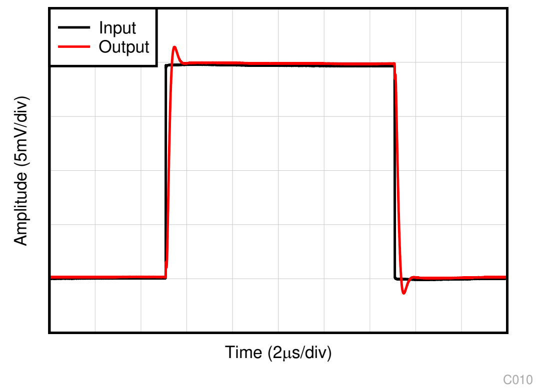
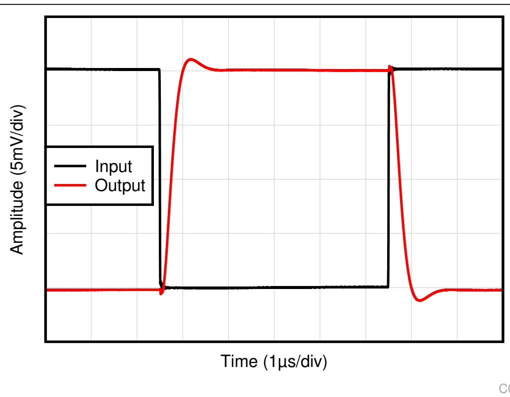


Figure 5-41. Voltage-follower Small-signal Pulse Response (Old Die)(17)



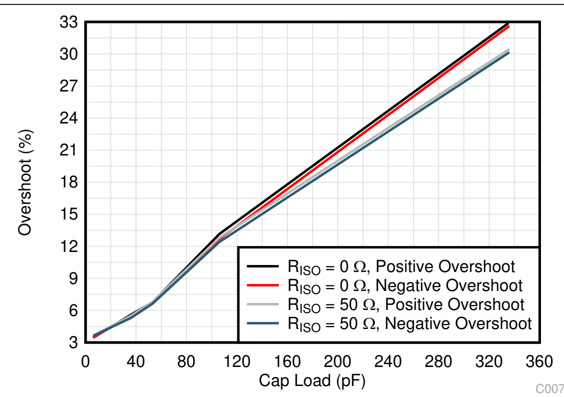
C_L = 20pF, G = 1, 20mV step response

Figure 5-42. Small-Signal Step Response (New Die)



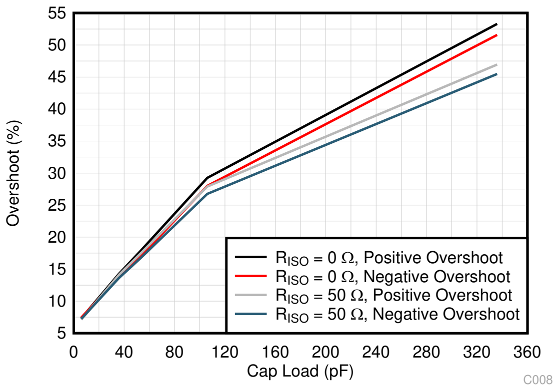
R_L = 1kΩ, C_L = 20pF, G = –1, 10mV step response

Figure 5-43. Small-Signal Step Response (New Die)



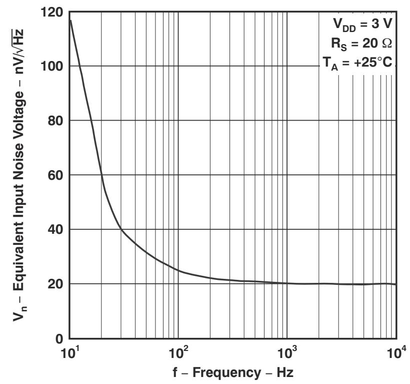
G = –1, 100mV output step

Figure 5-44. Small-Signal Overshoot vs Capacitive Load (New Die)



G = 1, 100mV output step

Figure 5-45. Small-Signal Overshoot vs Capacitive Load (New Die)



14

Figure 5-46. Equivalent Input Noise Voltage vs Frequency (Old Die)

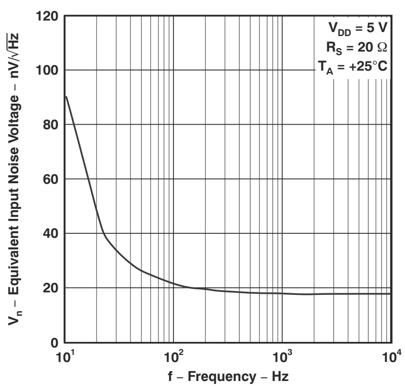


Figure 5-47. Equivalent Input Noise Voltage vs Frequency (Old Die)[18]

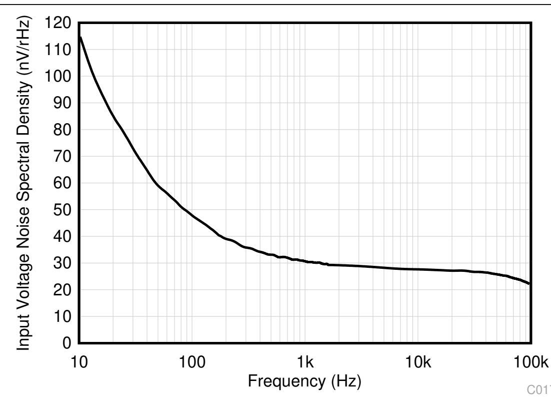


Figure 5-48. Input Voltage Noise Spectral Density vs Frequency (New Die)

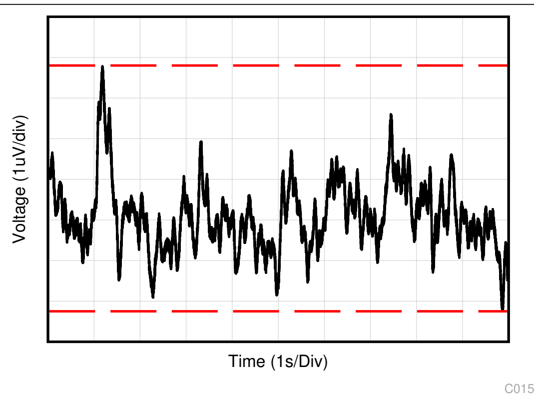


Figure 5-49. 0.1Hz to 10Hz Noise (New Die)

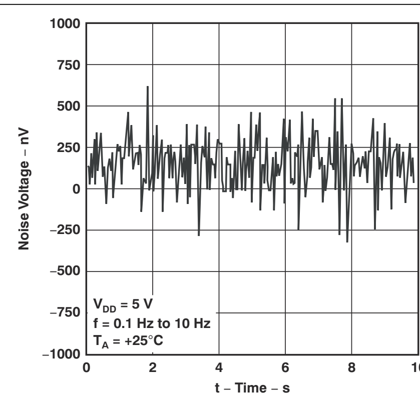


Figure 5-50. Input Noise Voltage Over a 10-second Period (Old Die)[18]

14 For all curves where V_{DD} = 5V, all loads are referenced to 2.5V. For all curves where V_{DD} = 3V, all loads are referenced to 1.5V.

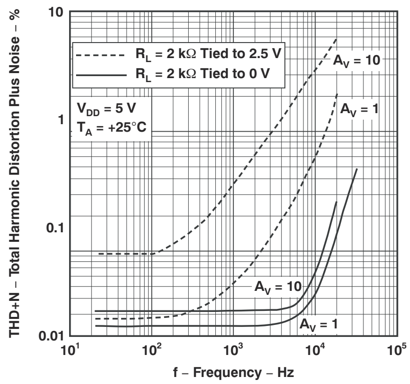


Figure 5-51. Total Harmonic Distortion Plus Noise vs Frequency (Old Die)(18)

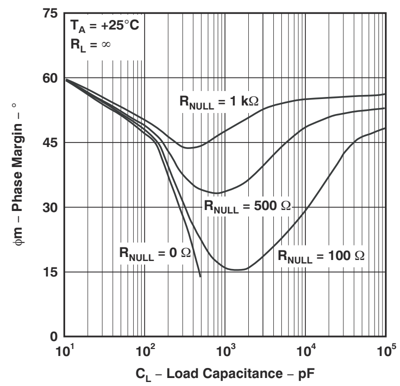


Figure 5-52. Phase Margin vs Load Capacitance (Old Die)

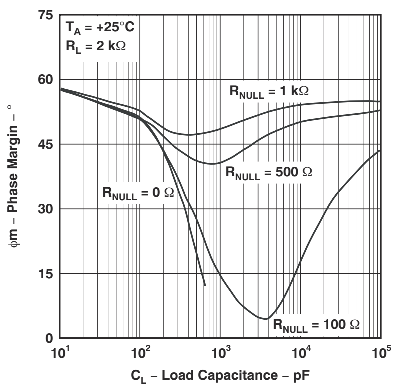
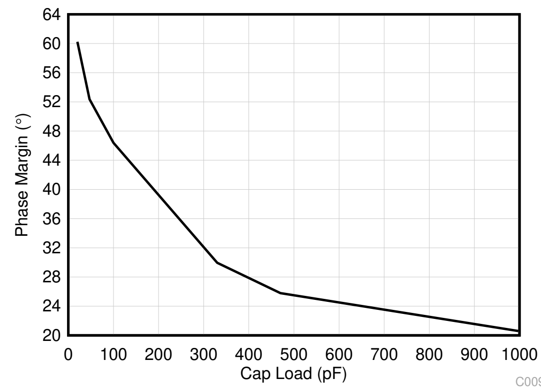


Figure 5-53. Phase Margin vs Load Capacitance (Old Die)



G = –1, 100mV output step

Figure 5-54. Small-Signal Overshoot vs Capacitive Load (New Die)

6 Detailed Description

6.1 Common-Mode Voltage Range

The TLV2221x is a true rail-to-rail input operational amplifier with an input common-mode range that extends 100mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 6-1. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1V to 100mV above the positive supply. The P-channel pair is active for inputs from 100mV below the negative supply to approximately (V+) – 2V. There is a small transition region, typically (V+) –2V to (V+) – 1V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance can be degraded compared to operation outside this region. To achieve best performance with the TLV2221x family, avoid this transition region when possible.

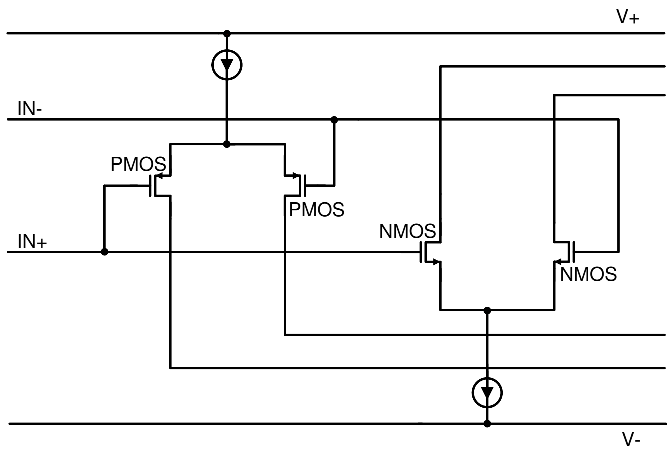


Figure 6-1. Rail-to-Rail Input Stage

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Documentation Support

7.2.1 Related Documentation

- Texas Instruments, *Use of Rail-to-Rail Operational Amplifiers*, Application Note

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

LinCMOS™ is a trademark of Marconi Electronic Devices Limited.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2005) to Revision C (May 2026) **Page**

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2221CDBVR	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	0 to 70	VADC
TLV2221CDBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	0 to 70	VADC
TLV2221IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	VADI
TLV2221IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	VADI
TLV2221IDBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLV2221IDBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-	VADI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

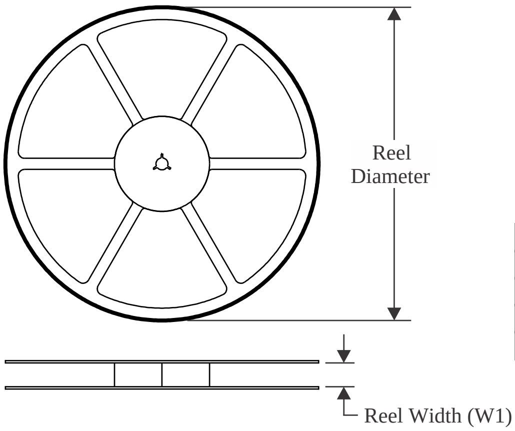
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

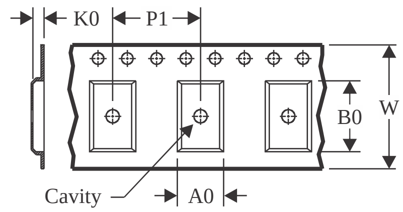
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

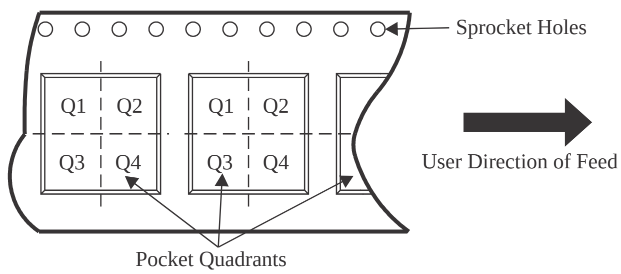


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

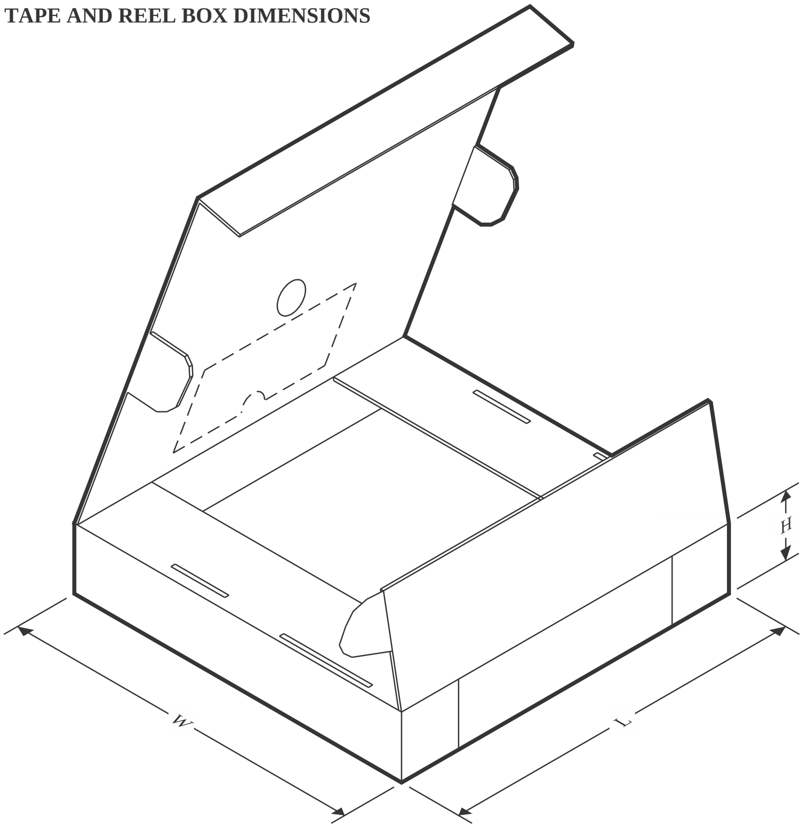
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

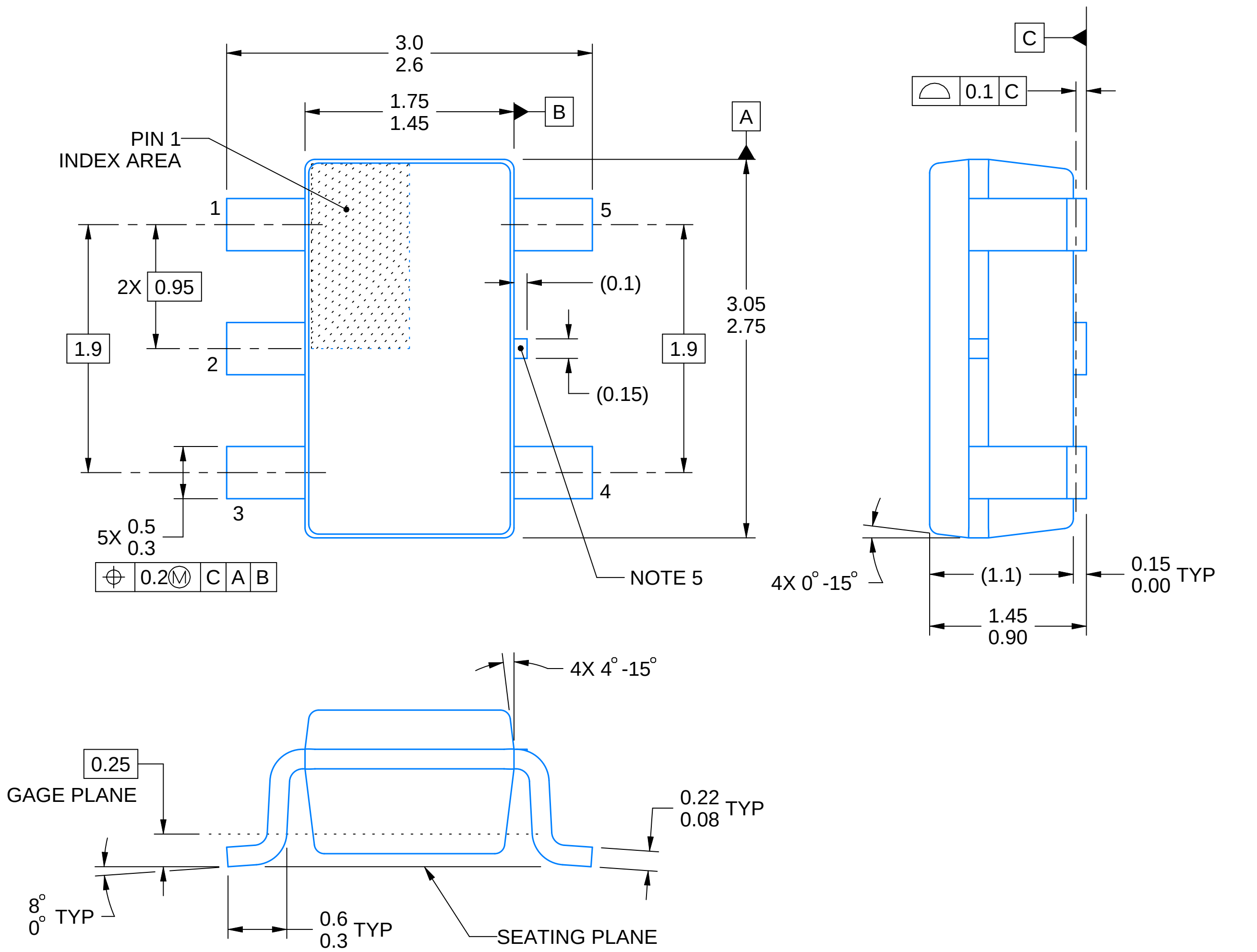
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2221IDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2221IDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0



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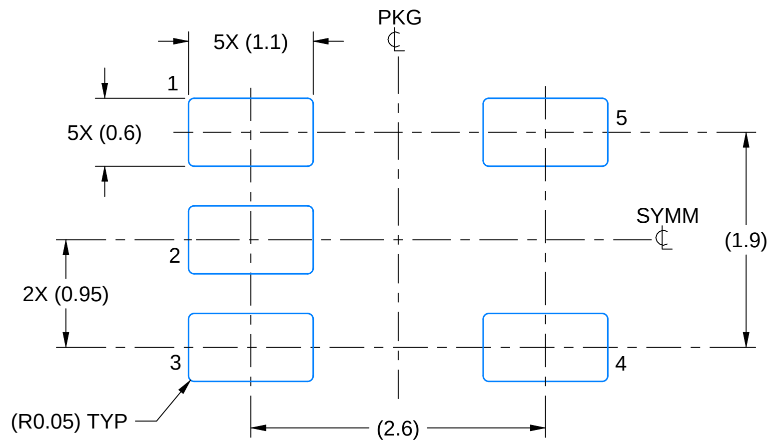
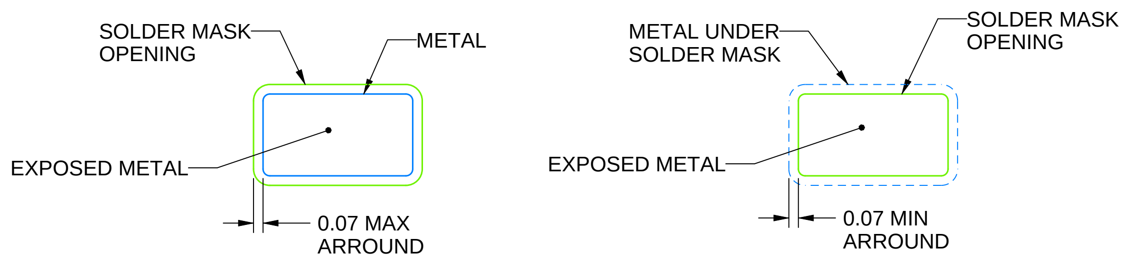
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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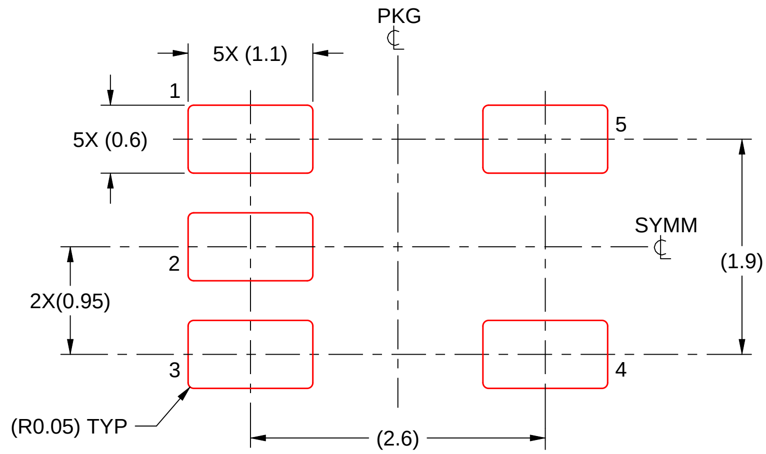
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.