TLV62130x 采用 3x3 QFN 封装的 3V 至 17V 3A 降压转换器

1 特性

- DCS-Control™拓扑
- 输入电压范围：3V 至 17V
- 输出电流高达 3A
- 可调节输出电压为 0.9V 至 5.5V
- 可通过引脚选择输出电压（标称值，+5%）
- 可编程软启动和跟踪
- 无缝省电模式转换
- 19μA 的静态电流（典型值）
- 可选运行频率
- 电源正常输出
- 100% 占空比模式
- 短路保护功能
- 过热保护
- 要获得改进的特性集，请见 TPS62130
- 与 TLV62150 引脚兼容 中）
- 采用 3mm × 3mm VQFN-16 封装
- 使用 TLV62130 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 标准 12V 导轨式电源
- 由单节或多节锂离子电池组成的负载点 (POL) 电源
- 电机驱动器、电子销售终端
- 移动 PC、平板、调制解调器、摄像头
- TV、机顶盒、音频

3 说明

TLV62130 器件是易于使用的同步降压 DC-DC 转换器，针对 高功率密度的应用 进行了优化。该器件的开关频率典型值高达 2.5MHz，允许使用小型电感器，通过利用 DCS-Control™拓扑技术提供快速的瞬态响应并实现高输出电压精度。

此器件具有 3V 至 17V 宽运行输入电压范围，非常适用于由锂离子或其它电池以及 12V 中间电源轨供电的系统。其支持高达 3A 的持续输出电流，输出电压范围为 0.9V 至 5.5V（100% 占空比模式下）。

输出电压启动斜坡由软启动引脚控制，可由独立电源供电运行，也可在跟踪配置下运行。此外，还可以通过配置使能引脚和开漏电源正常状态引脚实现电源排序。

在节能模式下，器件可根据 V_{IN} 生成约 19μA 的静态电流。负载较小时可自动且无缝进入节能模式，同时该模式可保持整个负载范围内的高效率。在关断模式下，此器件会关闭且关断期间的流耗少于 2μA。

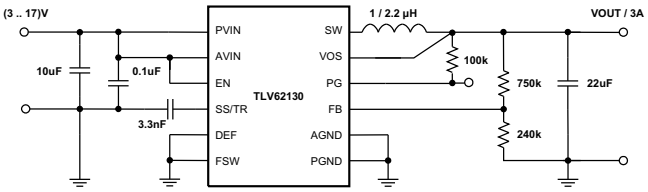
该器件采用 3mm × 3mm (RGT) 16 引脚超薄型四方扁平无引线 (VQFN) 封装。

器件信息(1)

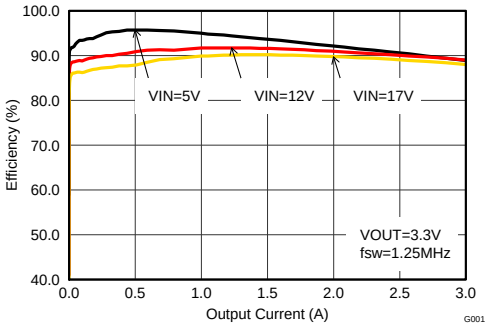
器件型号	封装	封装尺寸（标称值）
TLV62130	VQFN (16)	3.00mm × 3.00mm
TLV62130A		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型应用原理图



效率与输出电流间的关系



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision G (January 2017) to Revision H — **Page**

- 将可调节输出电压从“0.9V 至 5V”更改成了“0.9V 至 5.5V”- 通改。 ... 1
- Changed the VOUT MAX value From: 5 V To: 5.5 V in the *Electrical Characteristics* table ... 6

Changes from Revision F (January 2017) to Revision G — **Page**

- 已添加 WEBENCH® 信息至 *特性*，*详细设计流程和开发支持*部分。 ... 1

Changes from Revision E (July 2016) to Revision F — **Page**

- Added ac voltage specification for SW pin in Absolute Maximum Ratings ... 5

Changes from Revision D (August 2015) to Revision E — **Page**

- 已添加 “与 TLV62150 引脚兼容”（*特性* ... 1
- Changed temperature data in the *Thermal Information* table ... 5
- Changed V_{OUT} Intitial Output Voltage Accuracy from "–2.5% MIN and +2.5% MAX" to "780 mV MIN, 800 mV TYP, 820 mV MAX" in the *Electrical Characteristics* table ... 6
- Added information to the *Power Good (PG)* section. ... 9
- Changed *Layout Example* image ... 28
- 已添加 *接收文档更新通知* 部分 ... 30

Changes from Revision C (June 2015) to Revision D — **Page**

- 已更改 输入电压范围，从“4V 至 17V”改为“3V 至 17V”（通改）。 ... 1

Changes from Revision B (June 2013) to Revision C **Page**

- 已添加 *ESD 额定值表，特性 描述 部分，器件功能模式，应用和实现部分，电源相关建议部分，布局部分，器件*和*文档支持部分*以及*机械、封装*和*可订购信息部分* 1

Changes from Revision A (February 2013) to Revision B **Page**

- 已添加 器件 TLV62130A 至数据表 1
- Added text to Power Good (PG) section regarding TLV62130A function 9
- Added additional option to Pin-Selectable Output Voltage (DEF) section footnote. 10
- Added text to Frequency Selection (FSW) section regarding pin control..... 10

Changes from Original (February 2012) to Revision A **Page**

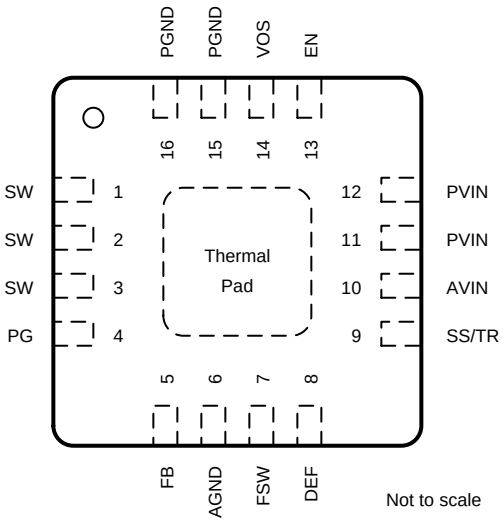
- Added text to Power Save Mode Operation section for clarification. 11
- Changed Layout Considerations description for clarification. 28

5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	Power Good Logic Level (EN=Low)
TLV62130	Adjustable	High Impedance
TLV62130A	Adjustable	Low

6 Pin Configuration and Functions

RGT Package
16-Pin VQFN
Top View



Pin Functions

PIN(1)		I/O	DESCRIPTION
NAME	NO.		
AGND	6	—	Analog Ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.
AVIN	10	I	Supply voltage for control circuitry. Connect to same source as PVIN.
DEF	8	I	Output Voltage Scaling (Low = nominal, High = nominal + 5%)(2)
EN	13	I	Enable input (High = enabled, Low = disabled)(2)
FB	5	I	Voltage feedback. Connect resistive voltage divider to this pin.
FSW	7	I	Switching Frequency Select (Low ≈ 2.5 MHz, High ≈ 1.25 MHz(3) for typical operation)(2)
PG	4	O	Output power good (High = V_{OUT} ready, Low = V_{OUT} below nominal regulation) ; open drain (requires pull-up resistor)
PGND	15, 16	—	Power ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.
PVIN	11, 12	I	Supply voltage for power stage. Connect to same source as AVIN.
SS/TR	9	I	Soft-Start / Tracking Pin. An external capacitor connected to this pin sets the internal voltage reference rise time. It can be used for tracking and sequencing.
SW	1, 2, 3	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
VOS	14	I	Output voltage sense pin and connection for the control loop circuitry.
Exposed Thermal Pad	—	—	Must be connected to AGND (pin 6), PGND (pin 15,16) and common ground plane. See *Layout Example*. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see *Detailed Description* and *Application and Implementation* sections.
(2) An internal pull-down resistor keeps logic level low, if pin is floating.
(3) Connect FSW to V_{OUT} or PG in this case.

7 Specifications

7.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Pin voltage (1)	AVIN, PVIN	–0.3	20	V
	EN, SS/TR	–0.3	V_{IN}+0.3	
	SW (DC)	–0.3	V_{IN}+0.3	V
	SW (AC), less than 10ns (2)	–2	24.5	
	DEF, FSW, FB, PG, VOS	–0.3	7	V
Power Good sink current	PG		10	mA
Operating junction temperature	T_J	–40	125	°C
Storage temperature	T_{stg}	–65	150	

(1) All voltages are with respect to network ground terminal.
(2) While switching.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge (1)	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (3)	±500	

(1) ESD testing is performed according to the respective JESD22 JEDEC standard.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

	MIX	MAX	UNIT
Supply Voltage	3	17	V
Operating free air temperature, T_A	–40	85	°C
Operating junction temperature, T_J	–40	125	

7.4 Thermal Information

THERMAL METRIC (1)		TLV62130 RGT [VQFN] 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (T_A = -40°C to +85°C), typical values at V_{IN} = 12 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input Voltage Range (1)		3		17	V
I_Q	Operating Quiescent Current	EN=High, I_{OUT} = 0 mA, device not switching		19	27	µA
I_{SD}	Shutdown Current (2)	EN=Low		1.5	4	µA
V_{UVLO}	Undervoltage Lockout Threshold	Falling Input Voltage (PWM mode operation)	2.6	2.7	2.8	V
		Hysteresis		200		mV
T_{SD}	Thermal Shutdown Temperature			160		°C
	Thermal Shutdown Hysteresis			20		
CONTROL (EN, DEF, FSW, SS/TR, PG)						
V_H	High Level Input Threshold Voltage (EN, DEF, FSW)		0.9			V
V_L	Low Level Input Threshold Voltage (EN, DEF, FSW)				0.3	V
I_{LKG}	Input Leakage Current (EN, DEF, FSW)	EN = V_{IN} or GND; DEF, FSW = V_{OUT} or GND		0.01	1	µA
V_{TH_PG}	Power Good Threshold Voltage	Rising (%V_{OUT})	92%	95%	98%	
		Falling (%V_{OUT})	87%	90%	94%	
V_{OL_PG}	Power Good Output Low	I_{PG} = -2 mA		0.07	0.3	V
I_{LKG_PG}	Input Leakage Current (PG)	V_{PG} = 1.8 V		1	400	nA
$I_{SS/TR}$	SS/TR Pin Source Current		2.3	2.5	2.7	µA
POWER SWITCH						
$R_{DS(ON)}$	High-Side MOSFET ON-Resistance	V_{IN} ≥ 6 V		90		mΩ
	Low-Side MOSFET ON-Resistance	V_{IN} ≥ 6 V		40		mΩ
I_{LIMF}	High-Side MOSFET Forward Current Limit (3)	V_{IN} = 12 V, T_A = 25°C	3.6	4.2		A
OUTPUT						
I_{LKG_FB}	Input Leakage Current (FB)	V_{FB} = 0.8 V		1	100	nA
V_{OUT}	Output Voltage Range	V_{IN} ≥ V_{OUT}	0.9		5.5	V
	DEF (Output Voltage Programming)	DEF=0 (GND)		V_{OUT}		
		DEF=1 (V_{OUT})		V_{OUT}+5%		
	Initial Output Voltage Accuracy (4)	PWM mode operation, V_{IN} ≥ V_{OUT} +1 V	780	800	820	mV
	Load Regulation (5)	V_{IN} = 12 V, V_{OUT} = 3.3 V, PWM mode operation		0.05		%/A
	Line Regulation (5)	4 V ≤ V_{IN} ≤ 17 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, PWM mode operation		0.02		%/V

(1) The device is still functional down to Undervoltage Lockout (see parameter V_{UVLO}).
(2) Current into AVIN + PVIN pin.
(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see *Current Limit and Short Circuit Protection*).
(4) This is the accuracy provided at the FB pin (line and load regulation effects are not included).
(5) Line and load regulation depend on external component selection and layout (see Figure 20 and Figure 21).

7.6 Typical Characteristics

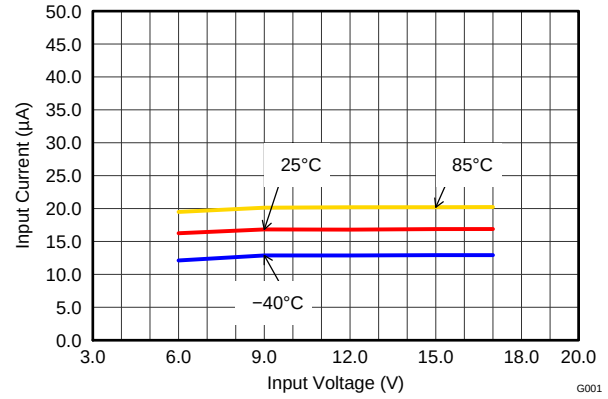


Figure 1. Quiescent Current

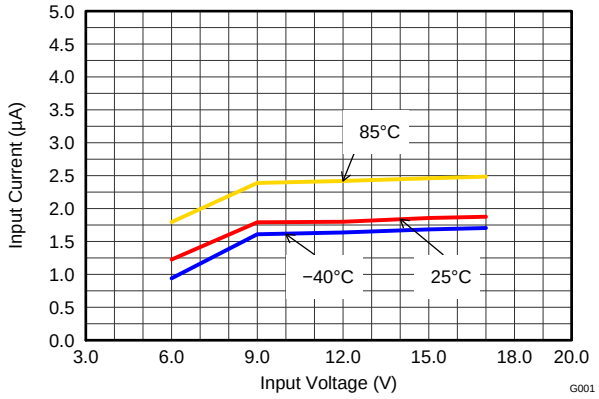


Figure 2. Shutdown Current

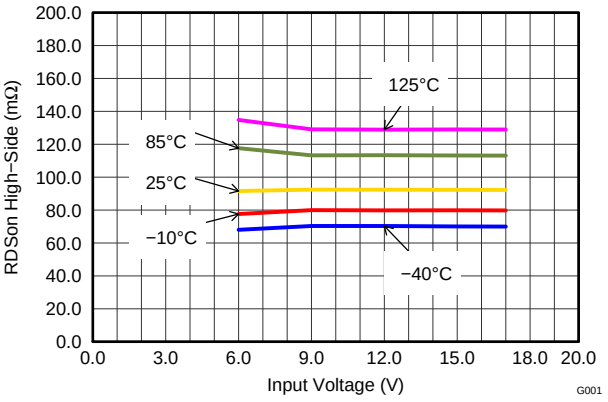


Figure 3. High-Side Switch Resistance

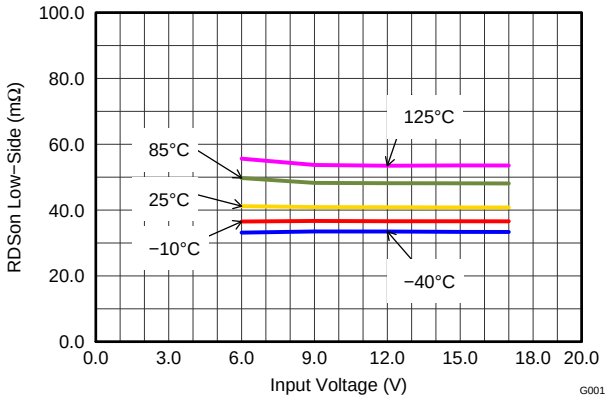


Figure 4. Low-Side Switch Resistance

8 Detailed Description

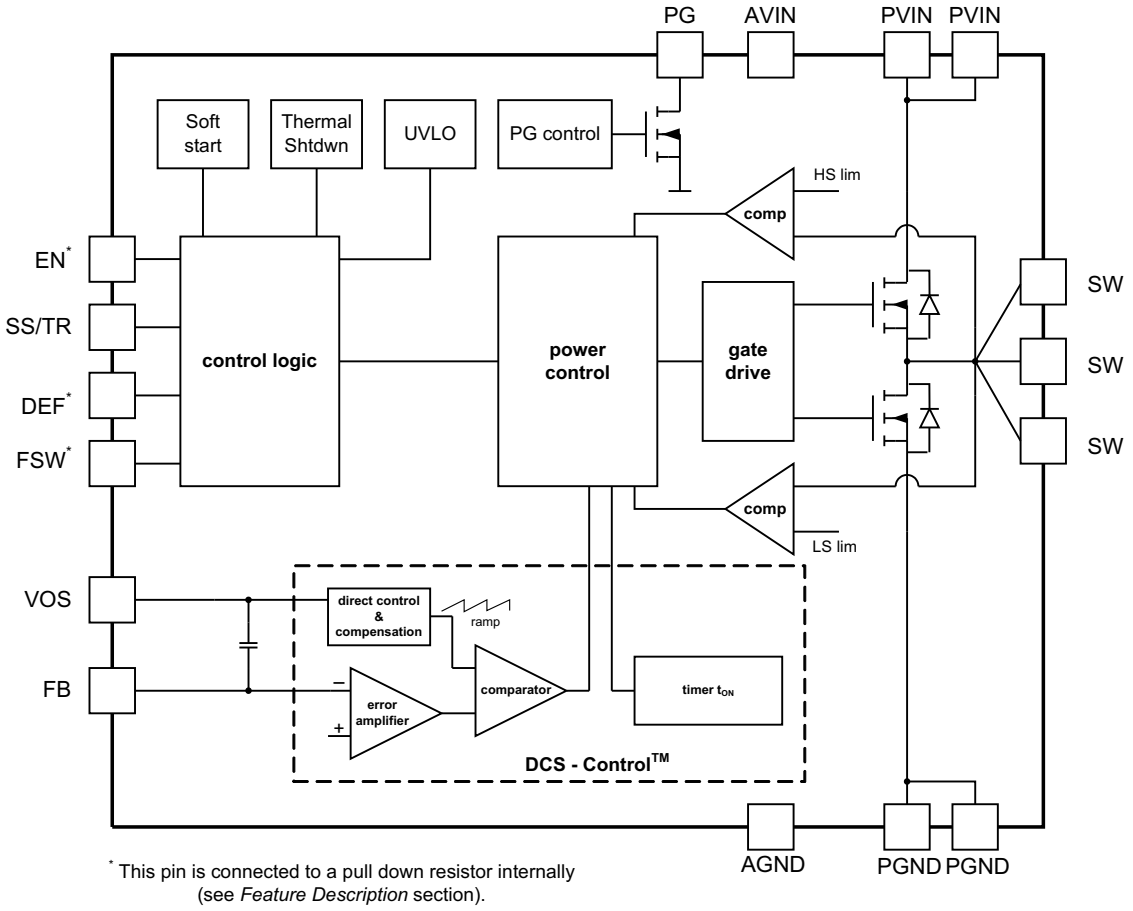
8.1 Overview

The TLV62130 synchronous switched-mode power converters are based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless Transition into Power Save Mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports Pulse Width Modulation (PWM) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.5 MHz or 1.25 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage. An internal current limit supports nominal output currents of up to 3 A.

The TLV62130 offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

8.2 Functional Block Diagram



* This pin is connected to a pull down resistor internally (see *Feature Description* section).

8.3 Feature Description

8.3.1 Enable / Shutdown (EN)

When Enable (EN) is set High, the device starts operation. Shutdown is forced if EN is pulled Low with a shutdown current of typically 1.5 µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The EN signal must be set externally to High or Low. An internal pull-down resistor of about 400 kΩ is connected and keeps EN logic low, if the pin is floating. It is disconnected if the pin is High.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

8.3.2 Soft Start / Tracking (SS/TR)

The internal soft start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50 µs and VOUT rises with a slope controlled by an external capacitor connected to the SS/TR pin. See Figure 32 and Figure 33 for typical startup operation.

Using a very small capacitor (or leaving SS/TR pin un-connected) provides fastest startup behavior. There is no theoretical limit for the longest startup time. The TLV62130 can start into a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to turn on until the device's internal ramp sets an output voltage above the pre-bias voltage. As long as the output is below about 0.5 V, a reduced current limit of typically 1.6 A is set internally. If the device is set to shutdown (EN=GND), undervoltage lockout or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new startup sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used for tracking a master voltage. The output voltage will follow this voltage in both directions up and down (see *Application and Implementation*).

8.3.3 Power Good (PG)

The TLV62130 has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic low level. With TLV62130 it is high impedance when the device is turned off due to EN, UVLO or thermal shutdown. TLV62130A features PG=Low in this case and can be used to actively discharge Vout (see Figure 39). VIN must remain present for the PG pin to stay Low. See SLVA644 for application details. If not used, the PG pin should be connected to GND but may be left floating.

Table 1. Power Good Pin Logic Table (TLV62130)

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown (EN=Low)		√	
UVLO	$0.7V < V_{IN} < V_{UVLO}$	√	
Thermal Shutdown	$T_J > T_{SD}$	√	
Power Supply Removal	$V_{IN} < 0.7V$	√	

Table 2. Power Good Pin Logic Table (TLV62130A)

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown (EN=Low)			√
UVLO	$0.7V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7V$	√	

8.3.4 Pin-Selectable Output Voltage (DEF)

The output voltage of the TLV62130 devices can be increased by 5% above the nominal voltage by setting the DEF pin to High (1). When DEF is Low, the device regulates to the nominal output voltage. Increasing the nominal voltage allows adapting the power supply voltage to the variations of the application hardware. More detailed information on voltage margining using TLV62130 can be found in SLVA489. A pull down resistor of about 400 kΩ is internally connected to the pin, to ensure a proper logic level if the pin is high impedance or floating after initially set to Low. The resistor is disconnected if the pin is set High.

8.3.5 Frequency Selection (FSW)

To get high power density with very small solution size, a high switching frequency allows the use of small external components for the output filter. However switching losses increase with the switching frequency. If efficiency is the key parameter, more than solution size, the switching frequency can be set to half (1.25 MHz typical) by pulling FSW to High. It is mandatory to start with FSW=Low to limit inrush current, which can be done by connecting to V_{OUT} or PG. Running with lower frequency a higher efficiency, but also a higher output voltage ripple, is achieved. Pull FSW to Low for high frequency operation (2.5 MHz typical). To get low ripple and full output current at the lower switching frequency, it's recommended to use an inductor of at least 2.2 µH. The switching frequency can be changed during operation, if needed. A pull down resistor of about 400kOhm is internally connected to the pin, acting the same way as at the DEF Pin (see above).

8.3.6 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents misoperation of the device by switching off both the power FETs. The undervoltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200 mV.

8.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typical), the device goes into thermal shut down. Both the high-side and low-side power FETs are turned off and PG goes high impedance. When T_J decreases below the hysteresis amount, the converter resumes normal operation, beginning with Soft Start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shut down temperature.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

The TLV62130 operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of 2.5 MHz or 1.25 MHz, selectable with the FSW pin. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

(1) Maximum allowed voltage is 7 V. Therefore, TI recommends connecting it to VOUT or PG, not VIN.

Device Functional Modes (continued)

8.4.2 Power Save Mode Operation

The TLV62130X enters its built in Power Save Mode seamlessly if the load current decreases. This secures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

TLV62130 includes a fixed on-time circuitry. This on-time, in steady-state operation, can be estimated (for FSW=Low) as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400\ ns \tag{1}$$

For very small output voltages, an absolute minimum on-time of about 80ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Also the off-time can reach its minimum value at high duty cycles. The output voltage remains regulated in such cases. Using t_{ON}, the typical peak inductor current in Power Save Mode can be approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \times t_{ON} \tag{2}$$

When V_{IN} decreases to typically 15% above VOUT, the TLV62130 won't enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

8.4.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by D=Vout/Vin and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input to output voltage differences, for example, for longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right) \tag{3}$$

where

- I_{OUT} is the output current.
- $R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET.
- R_L is the DC resistance of the inductor used.

8.4.4 Current Limit and Short Circuit Protection

The TLV62130 device is protected against heavy load and short circuit events. If a short circuit is detected (V_{OUT} drops below 0.5 V), the current limit is reduced to 1.6 A typically. If the output voltage rises above 0.5 V, the device runs in normal operation again. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET is turned off. Avoiding shoot through current, then the low-side FET switches on to allow the inductor current to decrease. The low-side current limit is typically 3.5 A. The high-side FET turns on again only if the current in the low-side FET has decreased below the low side current limit threshold.

Device Functional Modes (continued)

The output current of the device is limited by the current limit (see *Electrical Characteristics*). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \times t_{PD}$$

where

- I_{LIMF} is the static current limit, specified in the *Electrical Characteristics*.
- L is the inductor value.
- V_L is the voltage across the inductor (V_{IN} - V_{OUT}).
- t_{PD} is the internal propagation delay. (4)

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{(V_{IN} - V_{OUT})}{L} \times 30ns \quad (5)$$

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV62130 is a switched-mode step-down converter, able to convert a 3-V to 17-V input voltage into a 0.9-V to 5.5-V output voltage, providing up to 3 A. It needs a minimum amount of external components. Apart from the LC output filter and the input capacitors, the TLV62130 (TLV62130A) needs an additional resistive divider to set the output voltage level.

9.2 Typical Application

Figure 5 shows an application for Point-Of-Load Power Supply Using TLV62130.

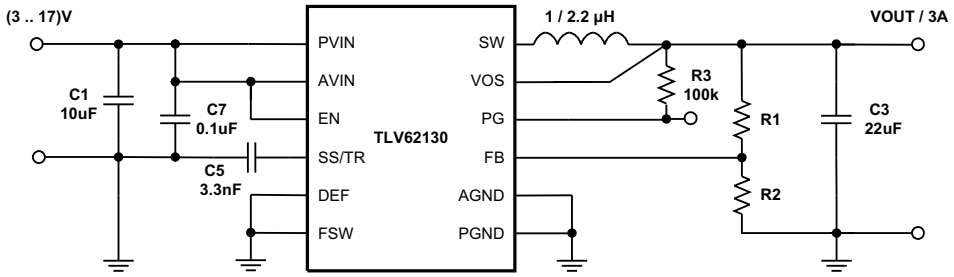


Figure 5. 3-A Step-Down Converter

9.2.1 Design Requirements

The following design guideline provides a component selection to operate the device within the recommended operating conditions. Using the FSW pin, the design can be optimized for highest efficiency or smallest solution size and lowest output voltage ripple. For highest efficiency set FSW=High and the device operates at the lower switching frequency. For smallest solution size and lowest output voltage ripple set FSW=Low and the device operates with higher switching frequency. The typical values for all measurements are V_{IN} = 12 V, V_{OUT} = 3.3 V and T = 25°C, using the external components of Table 3.

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TLV62130 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

Typical Application (continued)

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

The component selection used for measurements is given as follows:

Table 3. List of Components(1)

REFERENCE	DESCRIPTION	MANUFACTURER
IC	17-V, 3-A Step-Down Converter, VQFN	TLV62130RGT, Texas Instruments
L1	2.2 µH, 0.165 × 0.165 in	XFL4020-222MEB, Coilcraft
C1	10 µF, 25 V, Ceramic, 1210	Standard
C3	22 µF, 6.3 V, Ceramic, 0805	Standard
C5	3300 pF, 25 V, Ceramic, 0603	
C7	0.1 µF, 25V, Ceramic, 0603	
R1	depending on Vout	
R2	depending on Vout	
R3	100 kΩ, Chip, 0603, 1/16W, 1%	Standard

(1) See *Third-Party Products* Disclaimer

9.2.2.2 Programming the Output Voltage

The TLV62130 (TLV62130A) can be programmed for output voltages from 0.9 V to 5.5 V by using a resistive divider from V_{OUT} to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6. It is recommended to choose resistor values which allow a current of at least 2 uA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design.

$$R_1 = R_2 \left(\frac{V_{OUT}}{0.8V} - 1 \right) \quad (6)$$

In case the FB pin gets opened, the device clamps the output voltage at the VOS pin internally to about 7.4 V.

9.2.2.3 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TLV62130 is optimized to work within a range of external components. The LC output filter's inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter (see *Output Filter and Loop Stability*). Table 4 can be used to simplify the output filter component selection. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application. See SLVA463 for details.

Table 4. Recommended LC Output Filter Combinations(1)

	4.7 µF	10 µF	22 µF	47 µF	100 µF	200 µF	400 µF
0.47 µH							
1 µH			√	√	√	√	
2.2 µH		√	√(2)	√	√	√	
3.3 µH		√	√	√	√		
4.7 µH							

(1) The values in the table are nominal values. The effective capacitance was considered to vary by +20% and -50%.
(2) This LC combination is the standard value and recommended for most applications.

The TLV62130 can be run with an inductor as low as 1 µH. FSW should be set Low in this case. However, for applications running with the low frequency setting (FSW=High) or with low input voltages, 2.2 µH is recommended.

9.2.2.3.1 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \quad (7)$$

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L_{(min)} \times f_{SW}} \right) \quad (8)$$

where

- I_L(max) is the maximum inductor current.
- ΔI_L is the Peak to Peak Inductor Ripple Current.
- L(min) is the minimum effective inductor value.
- f_{SW} is the actual PWM Switching Frequency.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TLV62130 and are recommended for use:

Table 5. List of Inductors

Type	Inductance [µH]	Current [A](1)	Dimensions [LxBxH] mm	MANUFACTURER(2)
XFL4020-102ME_	1.0 µH, ±20%	4.7	4 × 4 × 2.1	Coilcraft
XFL4020-152ME_	1.5 µH, ±20%	4.2	4 × 4 × 2.1	Coilcraft
XFL4020-222ME_	2.2 µH, ±20%	3.8	4 × 4 × 2.1	Coilcraft
IHLP1212BZ-11	1.0 µH, ±20%	4.5	3 × 3.6 × 2	Vishay
IHLP1212BZ-11	2.2 µH, ±20%	3.0	3 × 3.6 × 2	Vishay
SRP4020-3R3M	3.3µH, ±20%	3.3	4.8 × 4 × 2	Bourns
VLC5045T-3R3N	3.3µH, ±30%	4.0	5 × 5 × 4.5	TDK

(1) Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop.
(2) See *Third-Party Products* Disclaimer

The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L \quad (9)$$

Using Equation 8, this current level can be adjusted by changing the inductor value.

9.2.2.3.2 Capacitor Selection

9.2.2.3.2.1 Output Capacitor

The recommended value for the output capacitor is 22 µF. The architecture of the TLV62130 allows the use of tiny ceramic output capacitors which have low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in Power Save Mode (see SLVA463).

Note: In power save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

9.2.2.3.2.2 Input Capacitor

For most applications, 10 µF will be sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between PVIN and PGND as close as possible to those pins. Even though AVIN and PVIN must be supplied from the same input source, it's required to place a capacitance of 0.1 µF from AVIN to AGND, to avoid potential noise coupling. An RC, low-pass filter from PVIN to AVIN may be used but is not required.

9.2.2.3.2.3 Soft Start Capacitor

A capacitance connected between SS/TR pin and AGND allows a user programmable start-up slope of the output voltage. A constant current source supports 2.5 µA to charge the external capacitance. The capacitor required for a given soft-start ramp time for the output voltage is given by:

$$C_{SS} = t_{SS} \times \frac{2.5\mu A}{1.25V} \left[F\right] \quad (10)$$

where

- C_{SS} is the capacitance (F) required at the SS/TR pin.
- t_{SS} is the desired soft-start ramp time (s).

NOTE

DC Bias effect: High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

9.2.2.4 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage. If the tracking voltage is between 50 mV and 1.2 V, the FB pin will track the SS/TR pin voltage as described in Equation 11 and shown in Figure 6.

$$V_{FB} = 0.64 \cdot V_{SS/TR} \quad \text{with} \quad \pm 2\% \quad (\text{typ.}) \quad (11)$$

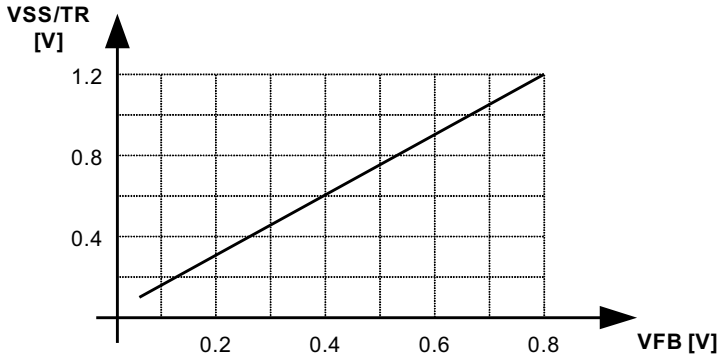


Figure 6. Voltage Tracking Relationship

Once the SS/TR pin voltage reaches about 1.2 V, the internal voltage is clamped to the internal feedback voltage and device goes to normal regulation. This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing SS/TR pin voltage, the device doesn't sink current from the output. So, the resulting decrease of the output voltage may be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is V_{IN} + 0.3 V.

If the input voltage drops into undervoltage lockout or even down to zero, the output voltage will go to zero, independent of the tracking voltage. Figure 7 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.

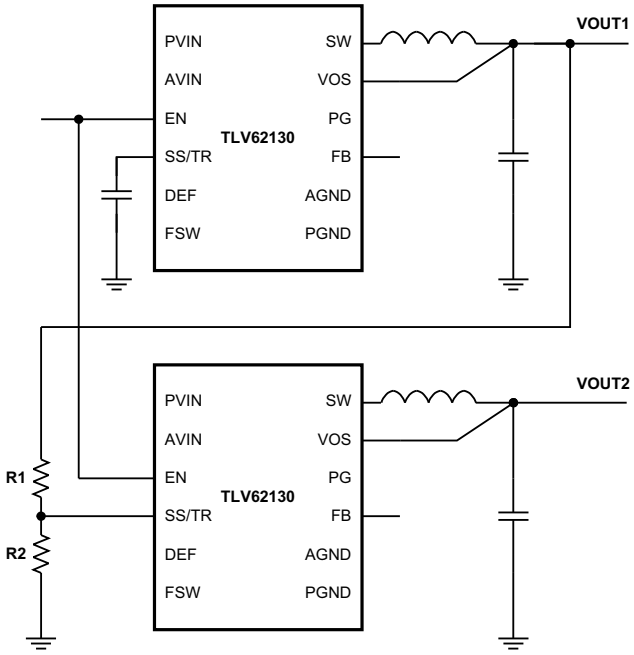


Figure 7. Sequence for Ratiometric and Simultaneous Startup

The resistive divider of R1 and R2 can be used to change the ramp rate of VOUT2 faster, slower or the same as VOUT1.

A sequential startup is achieved by connecting the PG pin of VOUT1 to the EN pin of VOUT2. Ratiometric start-up sequence happens if both supplies are sharing the same soft start capacitor. Equation 10 calculates the soft start time, though the SS/TR current has to be doubled. Details about these and other tracking and sequencing circuits are found in SLVA470.

Note: If the voltage at the FB pin is below its typical value of 0.8 V, the output voltage accuracy may have a wider tolerance than specified.

9.2.2.5 Output Filter and Loop Stability

The TLV62130 is internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 12:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C}} \tag{12}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 4 and are recommended for use. Different values may work, but care has to be taken on the loop stability which will be affected. More information including a detailed LC stability matrix can be found in SLVA463.

The TLV62130 device includes an internal 25-pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per equation Equation 13 and Equation 14:

$$f_{zero} = \frac{1}{2\pi \times R_1 \times 25pF} \tag{13}$$

$$f_{pole} = \frac{1}{2\pi \times 25pF} \times \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \tag{14}$$

Though the TLV62130 is stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in Power Save mode and/or improved transient response. An external feedforward capacitor can also be added. A more detailed discussion on the optimization for stability vs. transient response can be found in SLVA289 and SLVA466.

9.2.3 Application Curves

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)

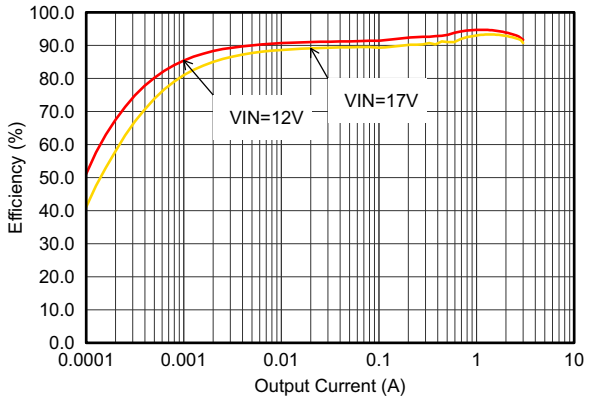


Figure 8. Efficiency With 1.25 MHz, Vout = 5 V

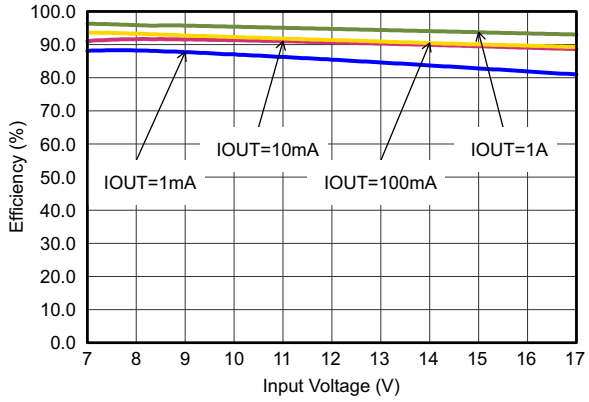


Figure 9. Efficiency With 1.25 MHz, Vout = 5 V

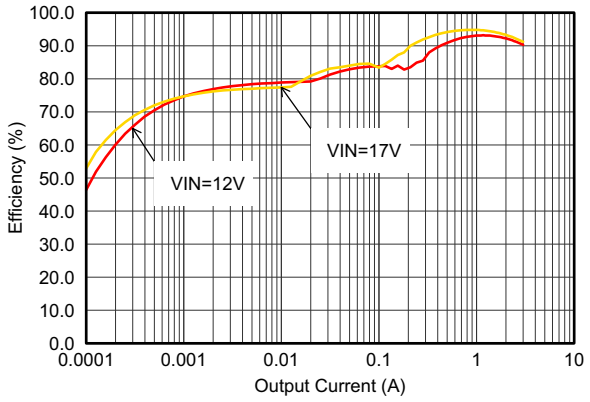


Figure 10. Efficiency With 2.5 MHz, Vout = 5 V

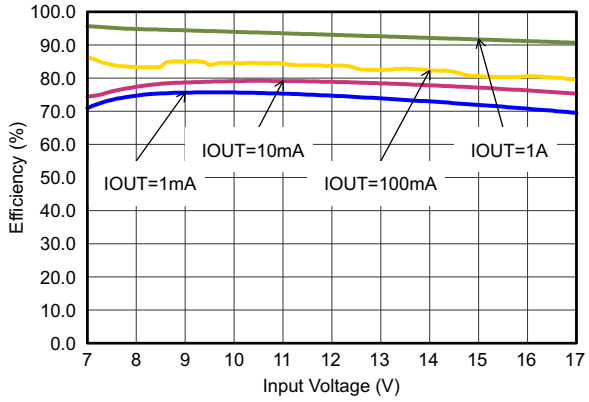


Figure 11. Efficiency With 2.5 MHz, Vout = 5 V

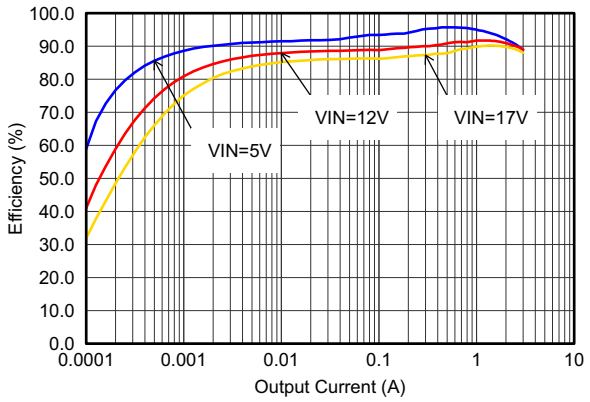


Figure 12. Efficiency With 1.25 MHz, Vout = 3.3 V

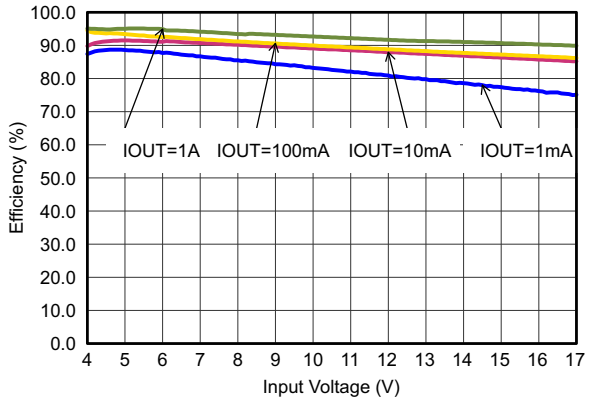


Figure 13. Efficiency With 1.25 MHz, Vout = 3.3 V

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)

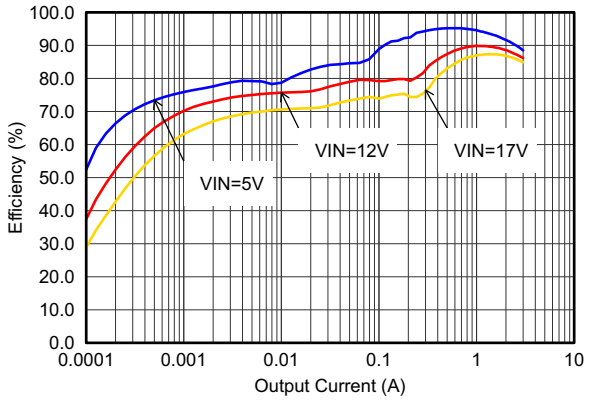


Figure 14. Efficiency With 2.5 MHz, Vout = 3.3 V

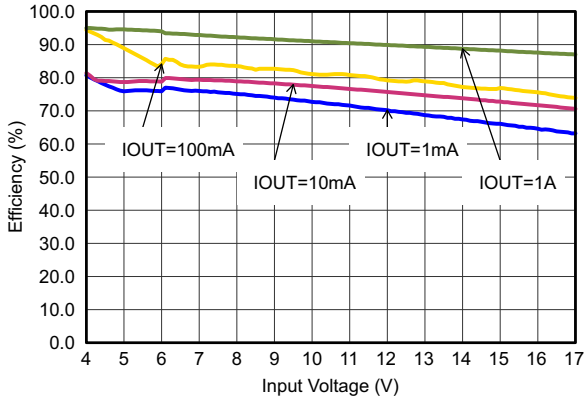


Figure 15. Efficiency With 2.5 MHz, Vout = 3.3 V

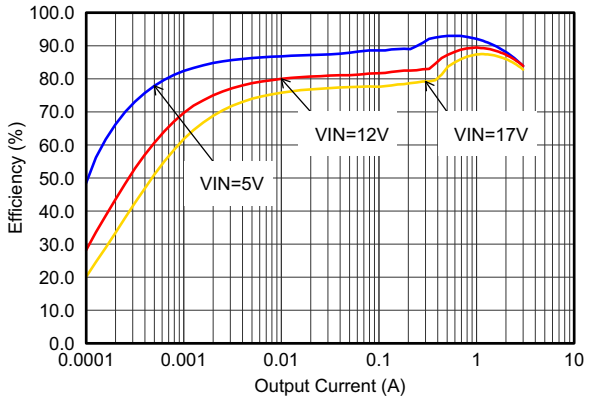


Figure 16. Efficiency With 1.25 MHz, Vout = 1.8 V

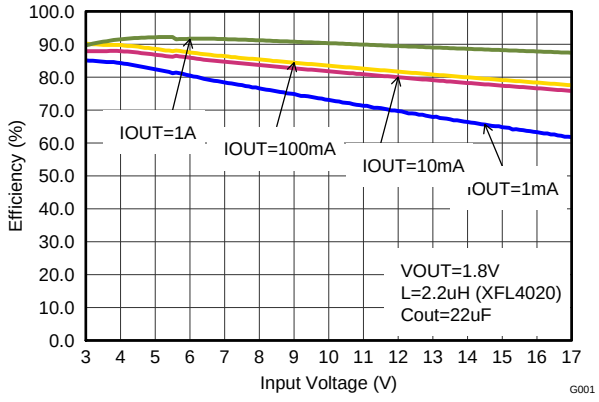


Figure 17. Efficiency With 1.25 MHz, Vout = 1.8 V

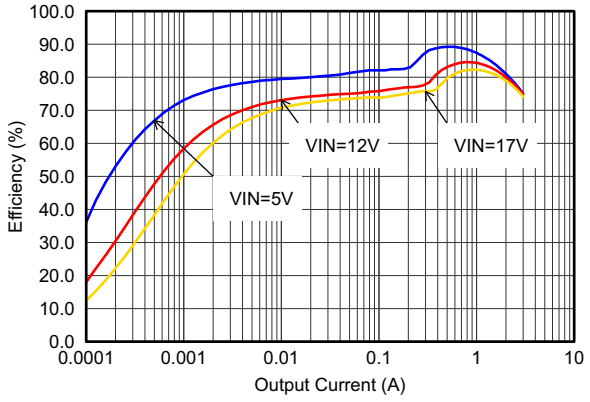


Figure 18. Efficiency With 1.25 MHz, Vout = 0.9 V

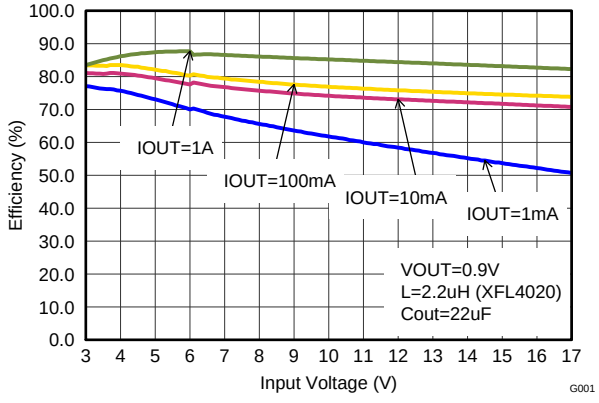


Figure 19. Efficiency With 1.25 MHz, Vout = 0.9 V

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)

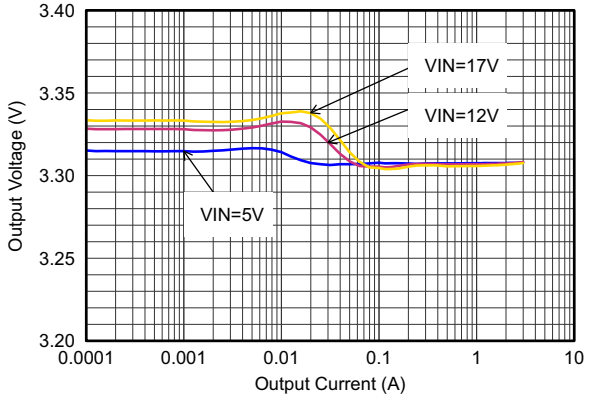


Figure 20. Output Voltage Accuracy (Load Regulation)

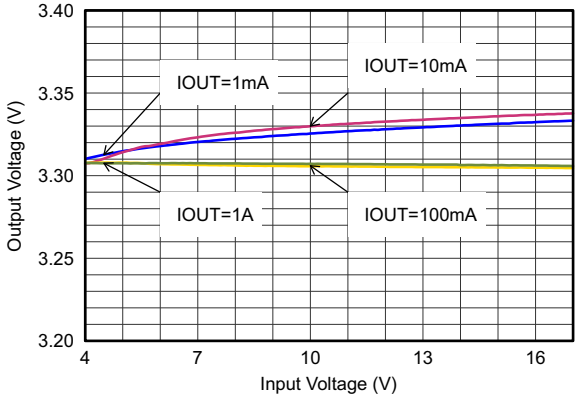


Figure 21. Output Voltage Accuracy (Line Regulation)

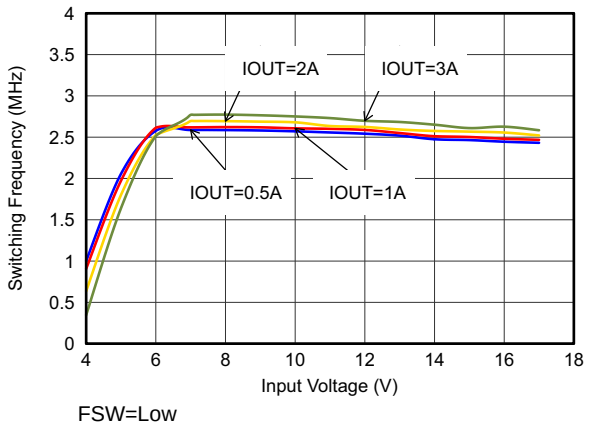


Figure 22. Switching Frequency

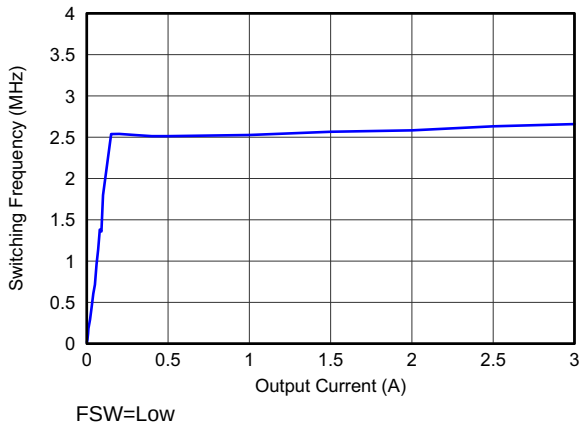


Figure 23. Switching Frequency

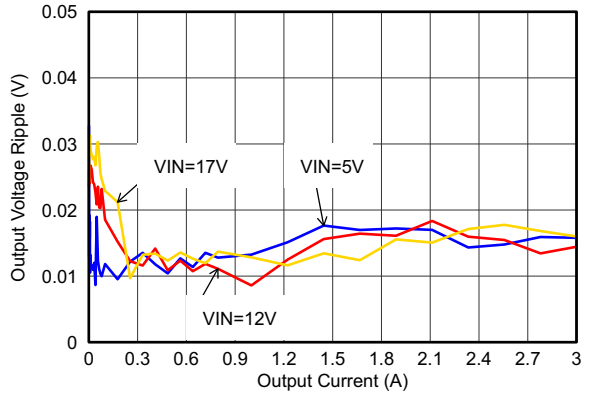


Figure 24. Output Voltage Ripple

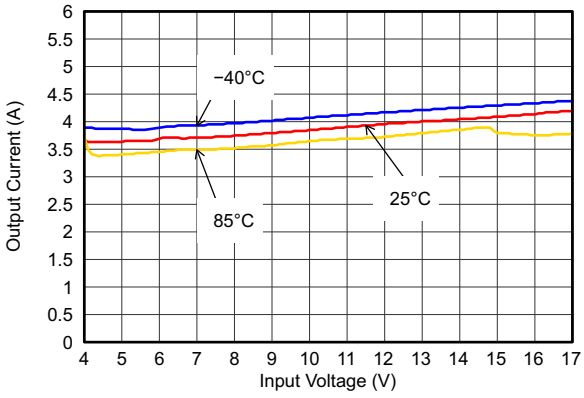
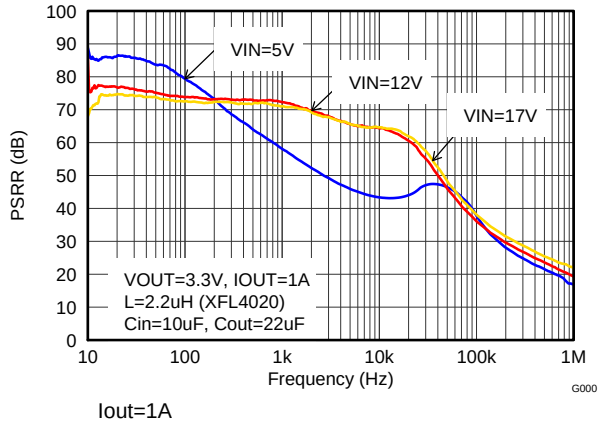


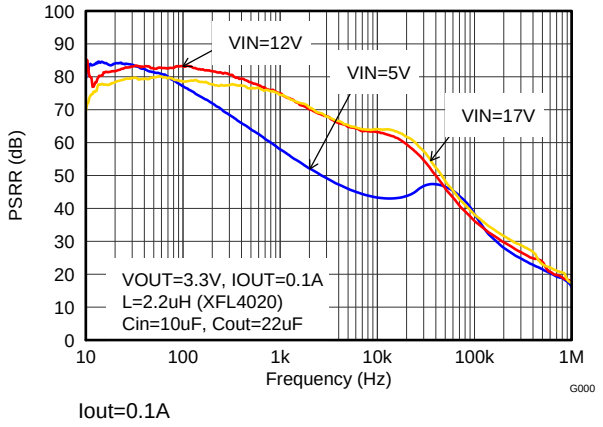
Figure 25. Maximum Output Current

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)



Iout=1A

Figure 26. Power Supply Rejection Ratio, F_{SW} = 2.5 MHz



Iout=0.1A

Figure 27. Power Supply Rejection Ratio, F_{SW} = 2.5 MHz

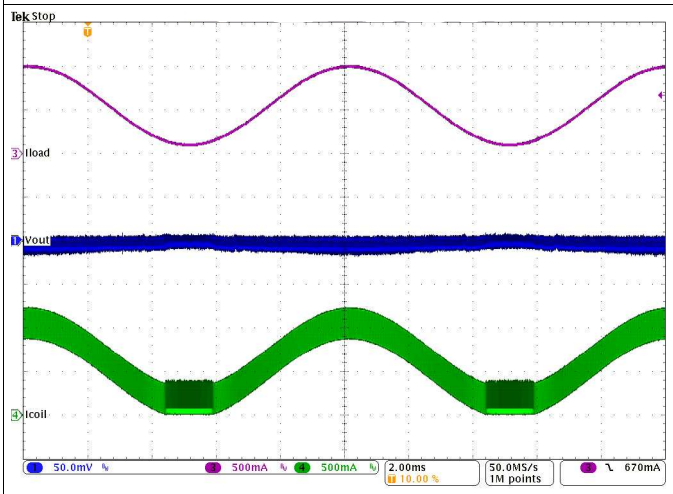


Figure 28. PWM-PSM-Transition (V_{IN} = 12 V, V_{OUT}=3.3 V with 50 mV/Div)

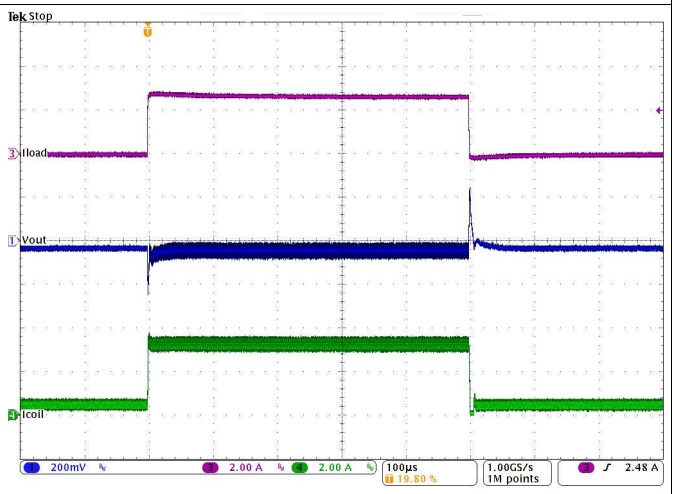


Figure 29. Load Transient Response (I_{OUT} = 0.5 to 3 to 0.5 A)

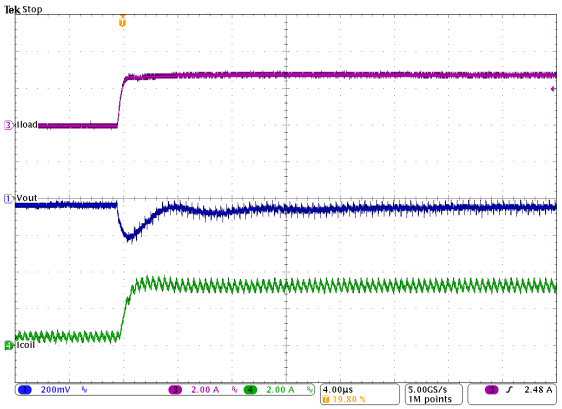


Figure 30. Load Transient Response of Figure 29, Rising Edge

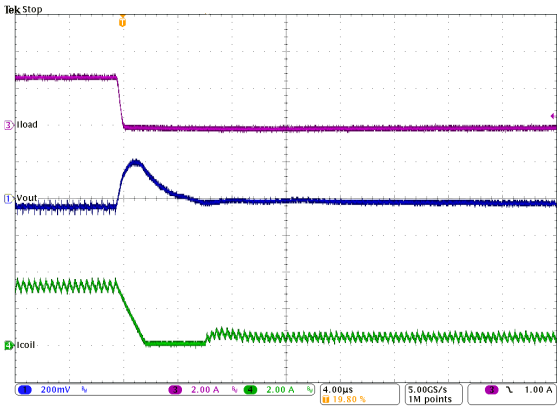


Figure 31. Load Transient Response of Figure 29, Falling Edge

V_{IN} = 12 V, V_{OUT} = 3.3 V, T_A = 25°C, (unless otherwise noted)

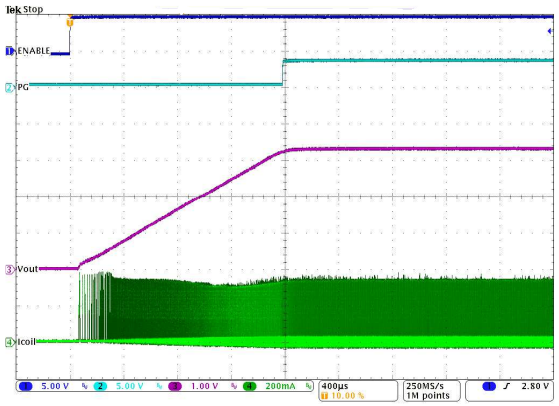


Figure 32. Startup into 100 mA

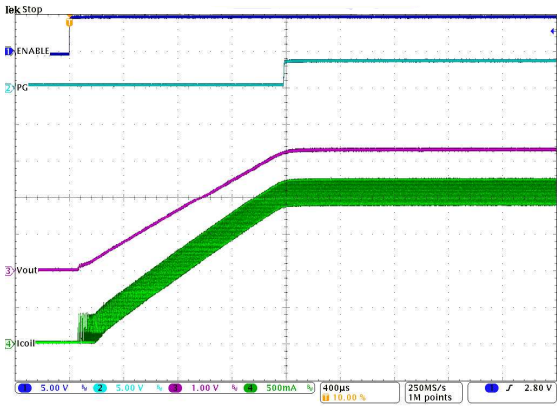


Figure 33. Startup into 3 A

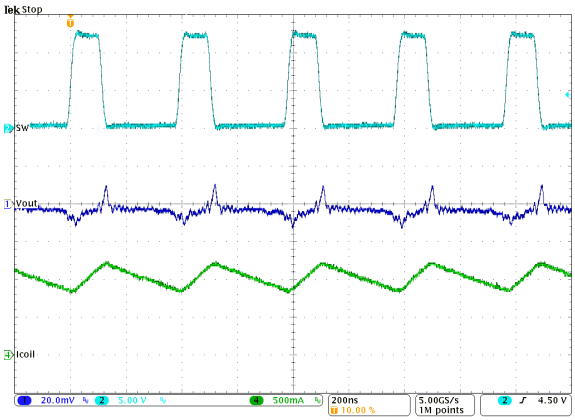


Figure 34. Typical Operation in PWM Mode (I_{OUT} = 1 A)

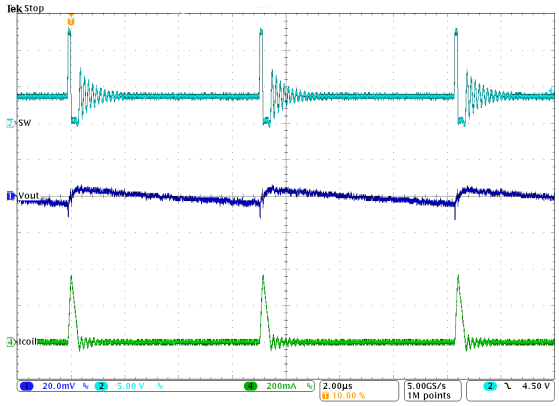


Figure 35. Typical Operation in Power Save Mode (I_{OUT} = 10 mA)

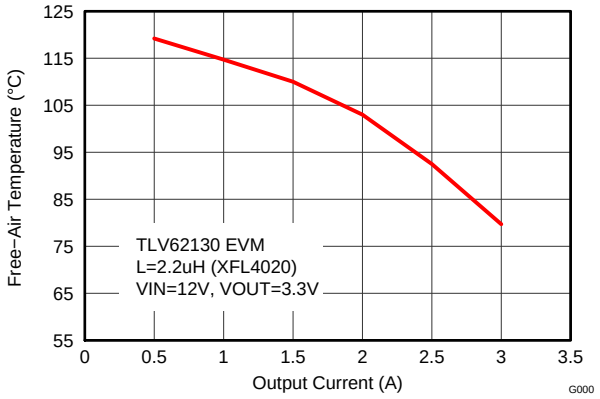


Figure 36. Maximum Ambient Temperature (F_{SW} = 2.5 MHz)

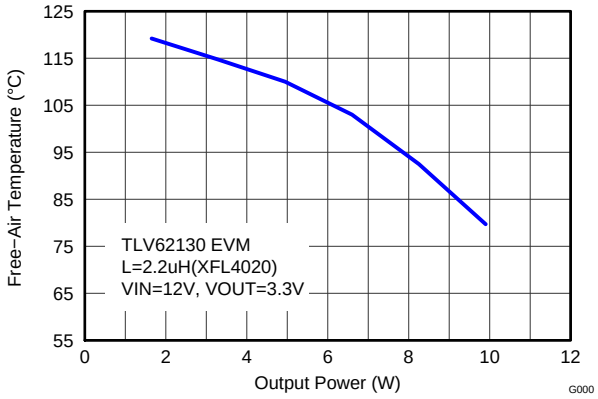


Figure 37. Maximum Ambient Temperature (F_{SW} = 2.5 MHz)

9.3 System Examples

9.3.1 LED Power Supply

The TLV62130 can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low to avoid excessive power loss. Since this pin provides 2.5 µA, the feedback pin voltage can be adjusted by an external resistor per Equation 15. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TLV62130. Figure 38 shows an application circuit, tested with analog dimming:

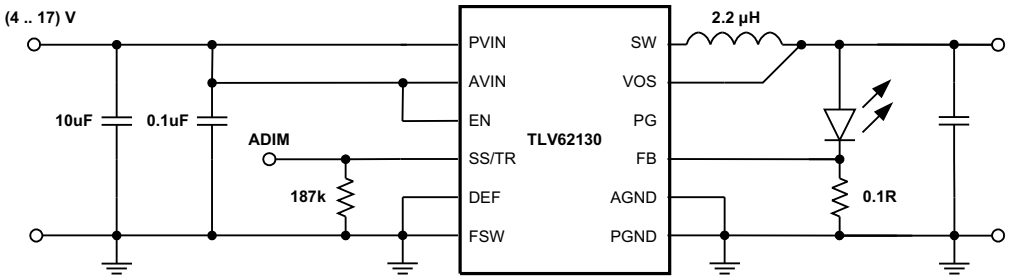


Figure 38. 3 A Single LED Power Supply

The resistor at SS/TR sets the FB voltage to a level of about 300 mV and is calculated from Equation 15.

$$V_{FB} = 0.64 \times 2.5\mu A \times R_{SS/TR} \quad (15)$$

The device now supplies a constant current, set by the resistor at the FB pin, by regulating the output voltage accordingly. The minimum input voltage has to be rated according the forward voltage needed by the LED used. More information is available in the Application Note SLVA451.

9.3.2 Active Output Discharge

The TLV62130A pulls the PG pin Low, when the device is shut down by EN, UVLO or thermal shutdown. Connecting PG to Vout through a resistor can be used to discharge Vout in those cases (see Figure 39). The discharge rate can be adjusted by R3, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10 mA.

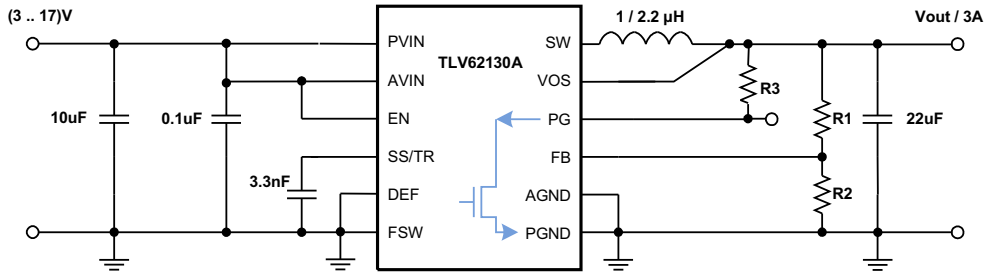


Figure 39. Discharge Vout Through PG Pin With TLV62130A

System Examples (continued)

9.3.3 Inverting Power Supply

The TLV62130 can be used as inverting power supply by rearranging external circuitry as shown in Figure 40. As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} has to be limited for operation to the maximum supply voltage of 17 V (see Equation 16).

$$V_{IN} + |V_{OUT}| \le V_{IN\,max} \tag{16}$$

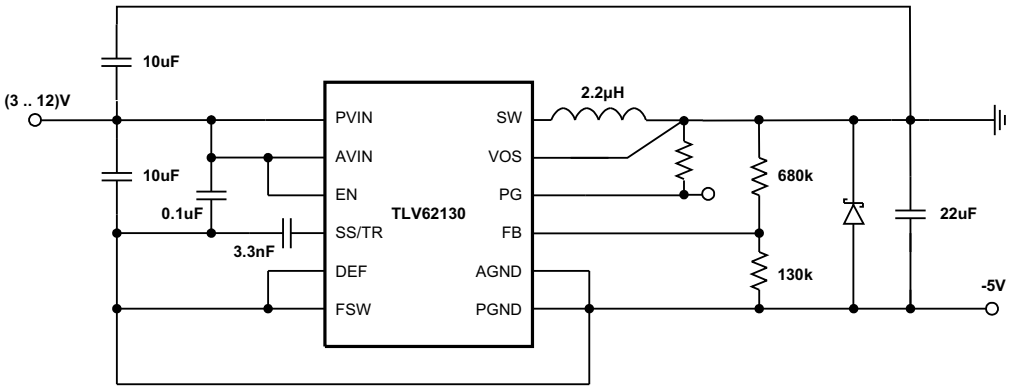


Figure 40. –5 V Inverting Power Supply

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted and an output capacitance of at least 22 µF is recommended. A detailed design example is given in SLVA469.

9.3.4 Various Output Voltages

The following example circuits show how to configure the external circuitry to furnish different output voltages at 3 A.

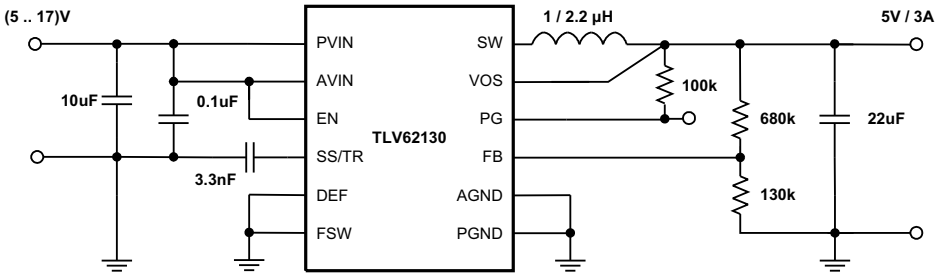


Figure 41. 5-V / 3-A Power Supply

System Examples (continued)

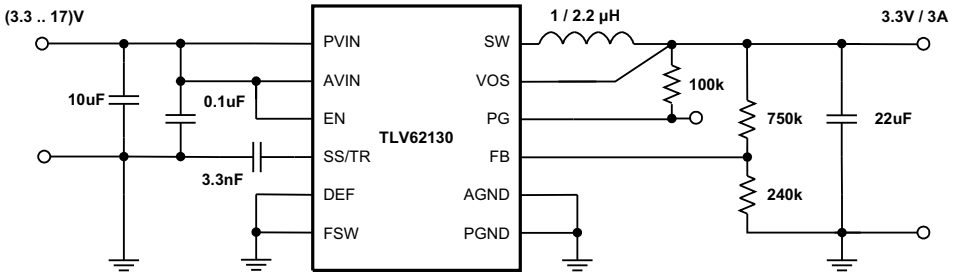


Figure 42. 3.3-V / 3-A Power Supply

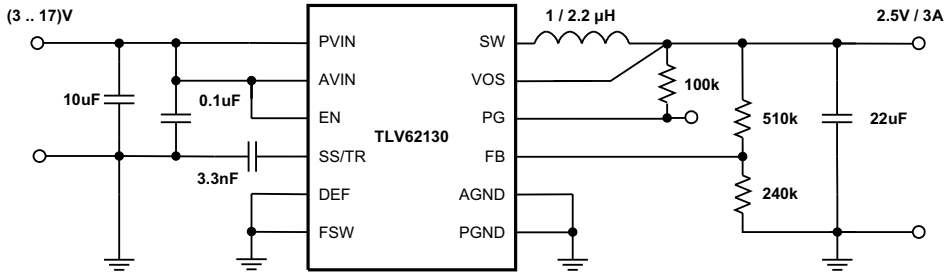


Figure 43. 2.5-V / 3-A Power Supply

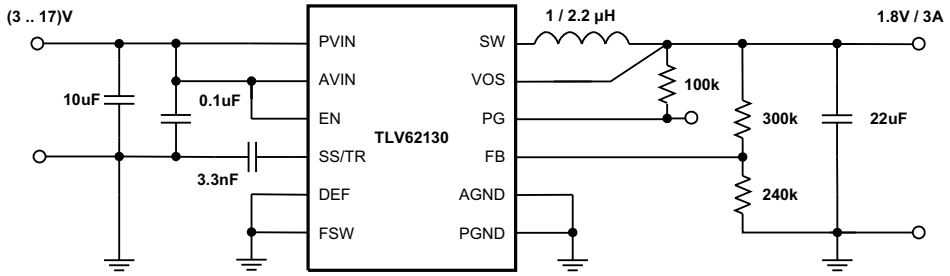


Figure 44. 1.8-V / 3-A Power Supply

System Examples (continued)

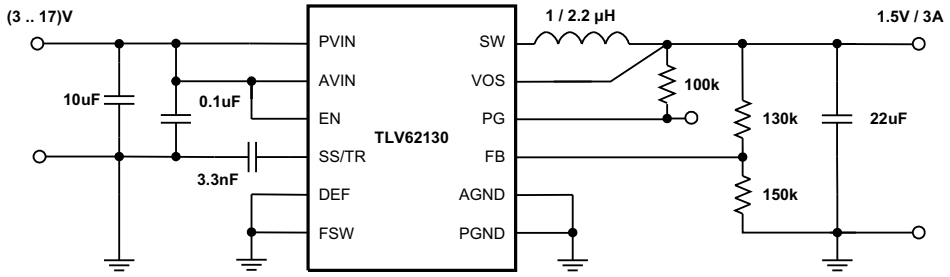


Figure 45. 1.5-V / 3-A Power Supply

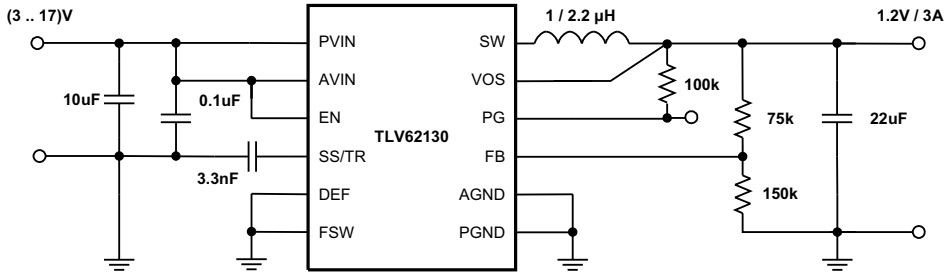


Figure 46. 1.2-V / 3-A Power Supply

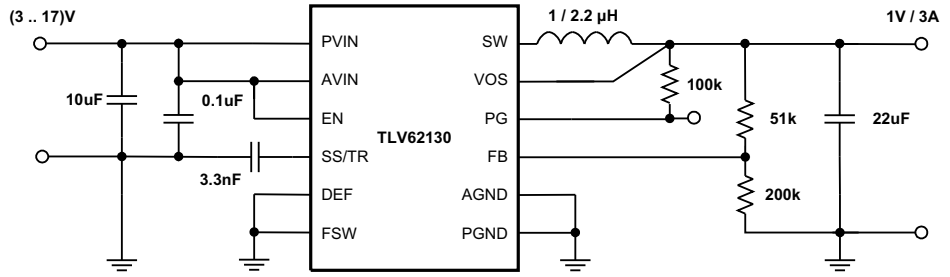


Figure 47. 1-V / 3-A Power Supply

10 Power Supply Recommendations

The TLV62130 are designed to operate from a 3-V to 17-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

11 Layout

11.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TLV62130 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity.

See Figure 48 for the recommended layout of the TLV62130, which is designed for common external ground connections. Therefore both AGND and PGND pins are directly connected to the Exposed Thermal Pad. On the PCB, the direct common ground connection of AGND and PGND to the Exposed Thermal Pad and the system ground (ground plane) is mandatory. Also connect the VOS pin in the shortest way to V_{OUT} at the output capacitor. To avoid noise coupling into the VOS line, this connection should be separated from the V_{OUT} power line/plane as shown in Figure 48.

Provide low inductive and resistive paths for loops with high di/dt. Therefore paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals (for example, SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin and on AVIN as well as the FB resistors, R1 and R2, should be kept close to the IC and connect directly to those pins and the system ground plane.

The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

The recommended layout is implemented on the EVM and shown in its Users Guide, SLAU416. Additionally, the EVM Gerber data are available for download here, SLVC394.

11.2 Layout Example

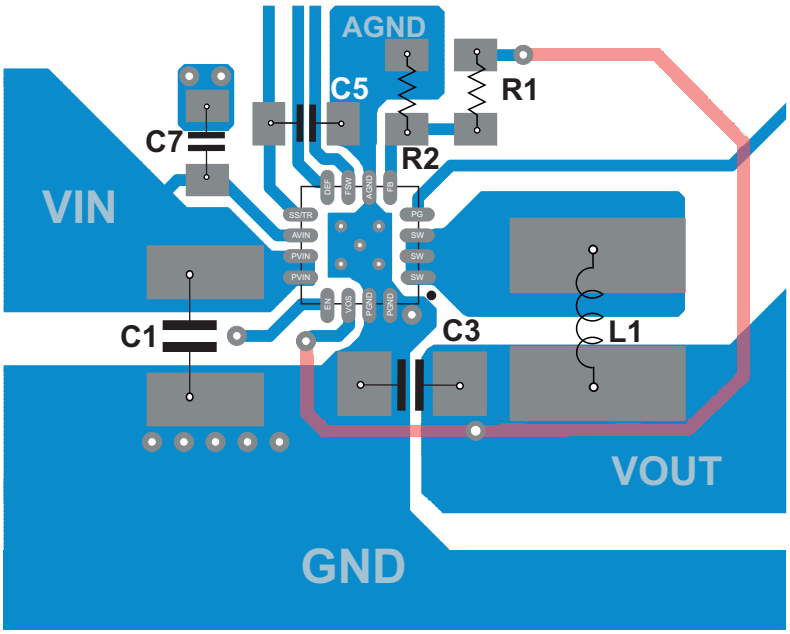


Figure 48. Layout Example Recommendation

11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the Exposed Thermal Pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: thermal characteristics application note (SZZA017), and (SPRA953).

The TLV62130 is designed for a maximum operating junction temperature (T_j) of 125°C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. Since the thermal resistance of the package is fixed, increasing the size of the surrounding copper area and improving the thermal connection to the IC can reduce the thermal resistance. To get an improved thermal behavior, it's recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation. Experimental data, taken from the TLV62130 EVM, shows the maximum ambient temperature (without additional cooling like airflow or heat sink), that can be allowed to limit the junction temperature to at most 125°C (see Figure 36).

12 器件和文档支持

12.1 器件支持

12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

12.1.2 开发支持

12.1.2.1 使用 WEBENCH® 工具创建定制设计

请单击此处，借助 WEBENCH® Power Designer 并使用 TLV62130 器件定制设计方案

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 文档支持

12.3.1 相关文档

请参阅如下相关文档：

- *《TLV62130EVM-505 和 TLV62150EVM-505 评估模块》*，SLAU416
- 《EVM 光绘数据》，SLVC394
- *《采用 JEDEC PCB 设计的线性和逻辑封装散热特性》*，SZZA017
- *《半导体和 IC 封装热指标》*，SPRA953

12.4 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **6.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TLV62130	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV62130A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 *TI 的工程师对工程师 (E2E) 社区*。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

社区资源 (接下页)

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.6 商标

DCS-Control, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.8 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV62130ARGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VUNI	Samples
TLV62130ARGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VUNI	Samples
TLV62130RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VUBI	Samples
TLV62130RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VUBI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

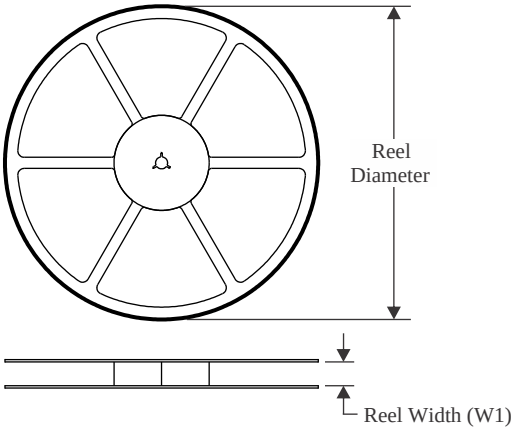
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

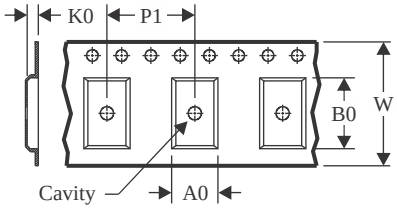
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

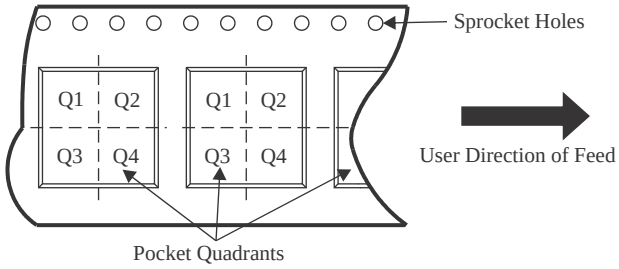


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

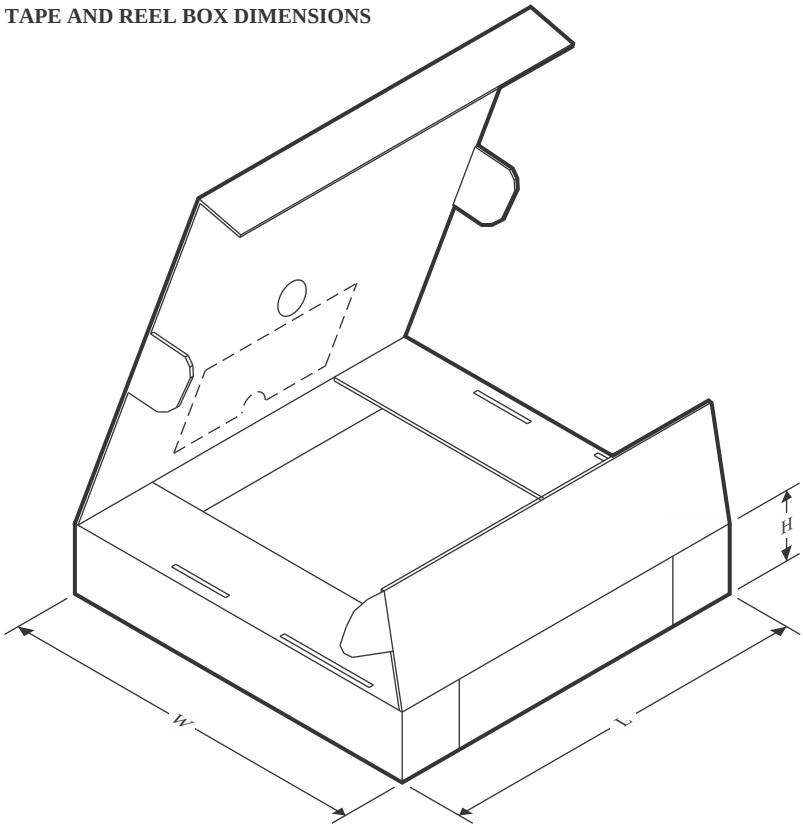
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62130ARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62130ARGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62130ARGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62130RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62130RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62130RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV62130RGTT	VQFN	RGT	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2

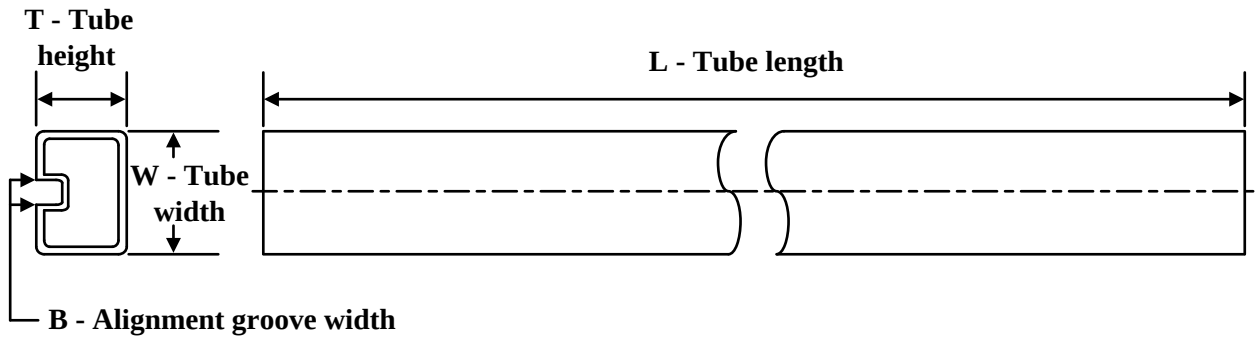
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62130ARGTR	VQFN	RGT	16	3000	552.0	346.0	36.0
TLV62130ARGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TLV62130ARGTT	VQFN	RGT	16	250	552.0	185.0	36.0
TLV62130RGTR	VQFN	RGT	16	3000	552.0	346.0	36.0
TLV62130RGTT	VQFN	RGT	16	250	552.0	185.0	36.0
TLV62130RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TLV62130RGTT	VQFN	RGT	16	250	338.0	355.0	50.0

TUBE

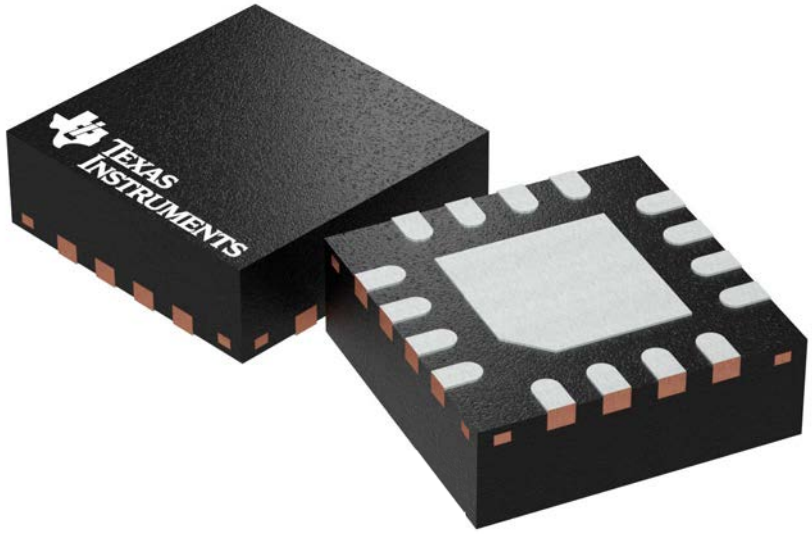


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV62130ARGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TLV62130ARGTT	RGT	VQFN	16	250	381	4.83	2286	0
TLV62130RGTR	RGT	VQFN	16	3000	381	4.83	2286	0
TLV62130RGTT	RGT	VQFN	16	250	381	4.83	2286	0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



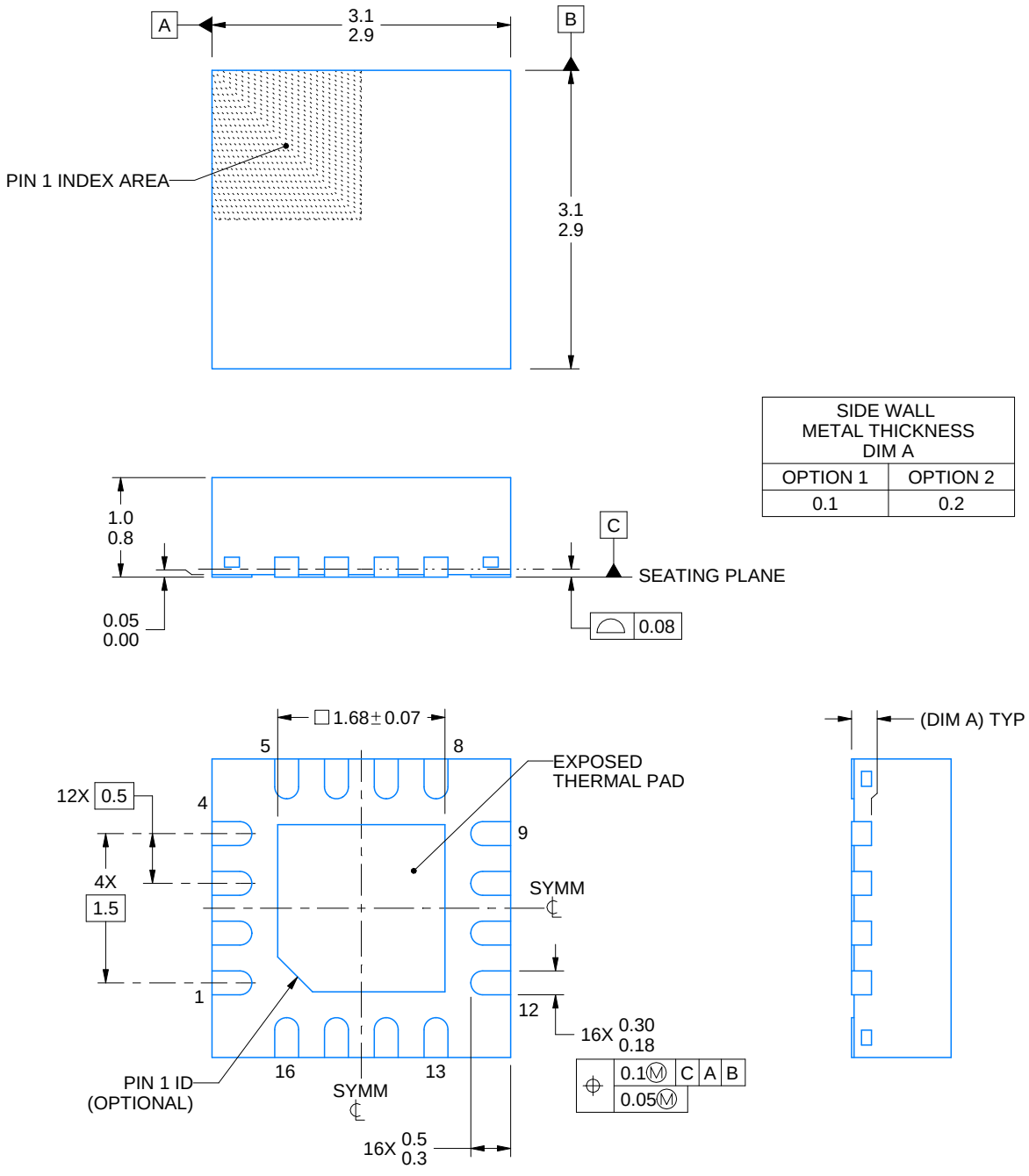
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

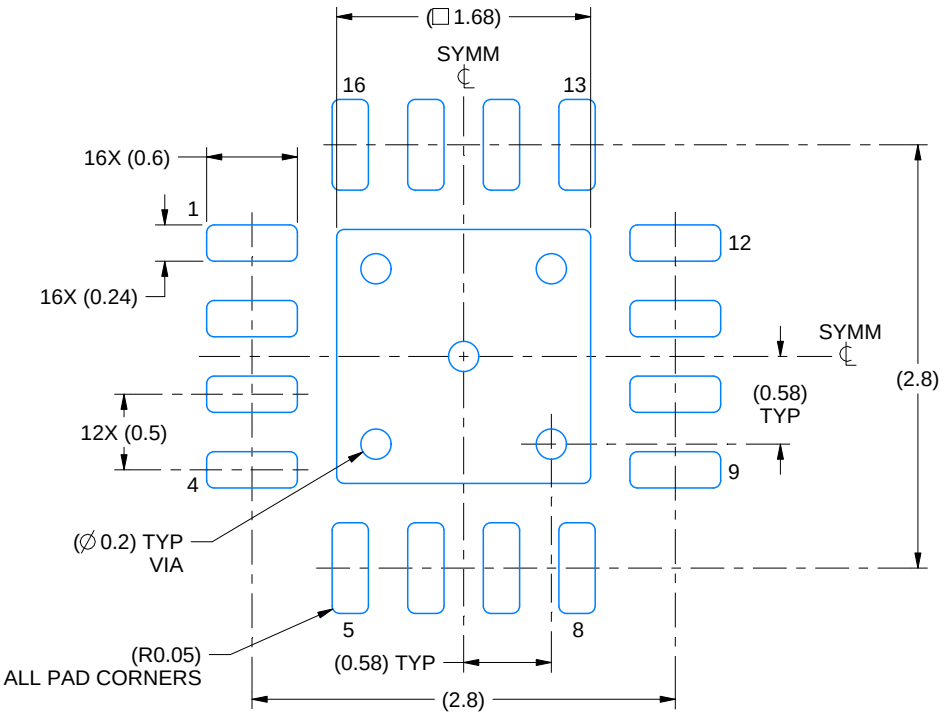
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

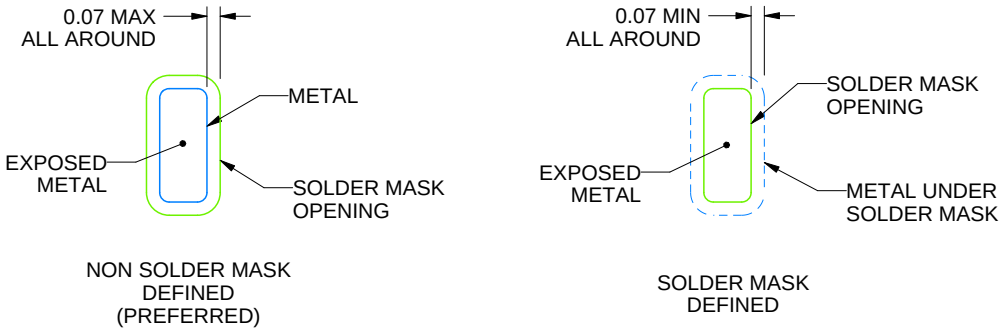


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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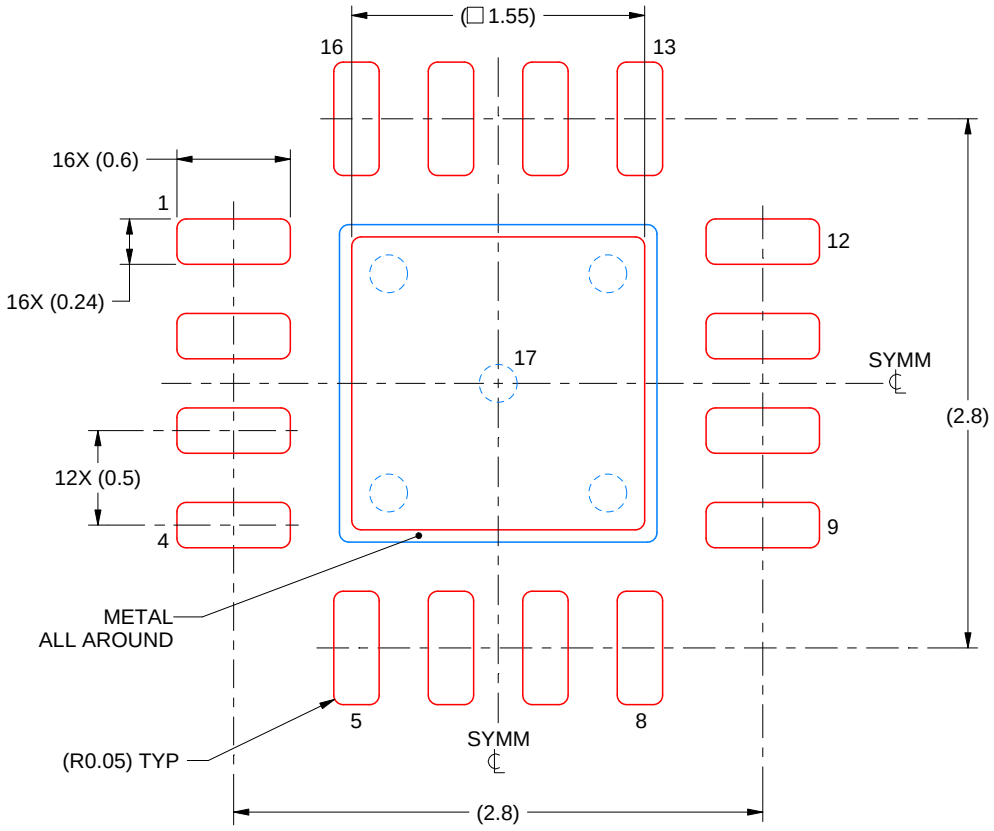
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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