TLV701x 和 TLV702x 小尺寸、低功耗、低电压比较器

1 特性

- 超小型封装：X2SON (0.8 x 0.8mm^2)
- 标准封装：SOT23、SC70、VSSOP
- 1.6V 至 6.5V 的宽电源电压范围
- 5µA 静态电源电流
- 260ns 低传播延迟
- 轨至轨共模输入电压
- 内部迟滞
- 推挽和开漏输出选项
- 过驱动输入无相位反转
- –40°C 至 +125°C 的工作环境温度范围

2 应用

- 手机和平板电脑
- 便携式电池供电器件
- 红外接收器
- 电平转换器
- 阈值检测器与鉴别器
- 窗口比较器
- 过零检测器

3 说明

TLV7011/7021（单通道）和 TLV7012/7022（双通道）是微功耗比较器，采用低工作电压，具有轨至轨输入功能。这些比较器采用 0.8mm × 0.8mm 超小型无引线封装和标准引线式封装，适用于空间紧凑型设计，例如智能手机和其他便携式或电池供电 应用。

TLV701x 和 TLV702x 提供出色的速度功率综合性能，其传播延迟为 260ns，静态电源电流为 5µA。得益于这种微功率下快速响应时间的综合性能，功率敏感型系统能够监测故障状况并快速做出响应。这些比较器的工作电压范围为 1.6V 至 6.5V，因此可与 3V 和 5V 系统兼容。

此外，这些比较器在发生过驱动输入和内部迟滞时，不会产生输出相位反转。这些 特性 该系列的比较器非常适合在恶劣嘈杂环境中进行精密电压监测，其中缓慢输入信号必须转换为无噪声数字输出。

TLV701x 具有推挽式输出级，能够灌/拉毫安级电流，同时可对 LED 进行控制或驱动容性负载。TLV702x 具有可上拉到 V_{CC} 之上的漏极开路输出级，因此适用于电平转换器和双极至单端转换器。

器件信息[(1)]

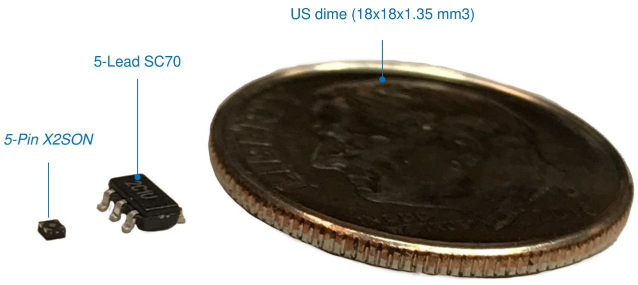
器件型号	封装（引脚）	封装尺寸（标称值）
TLV7011、TLV7021	X2SON (5)	0.80mm × 0.80mm
	SC70 (5)	2.00mm × 1.25mm
	SOT-23 (5)	2.90mm × 1.60mm
TLV7012、TLV7022	VSSOP (8)	3mm x 3mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

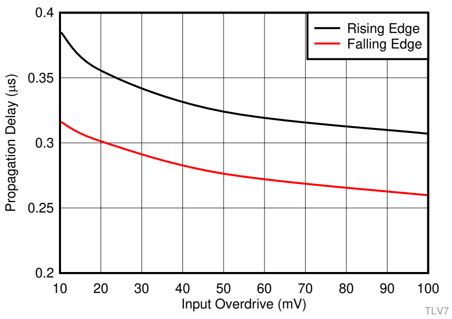
TLV70x1 系列低功耗比较器

部件号	输出	I_Q（典型值）	t_{PD}（典型值）
TLV701x	推挽	5µA	260ns
TLV702x	漏极开路	5µA	260ns
TLV703x	推挽	335nA	3µs
TLV704x	漏极开路	335nA	3µs

X2SON 封装与 SC70 和美元硬币对比



传播延迟与过驱动



T_A = 25°C，V_{CC} = 5V，C_L = 15pF

English Data Sheet: SLVSDM5

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4 修订历史记录

Changes from Revision D (February 2019) to Revision E	Page
• 已添加 添加了双通道选项	1

Changes from Revision C (March 2018) to Revision D	Page
• 已添加 添加了引线式封装选项，目标位置： 特性	1
• 已删除 SOT23 封装的预览状态	1
• Deleted preview status of SOT23 package	3

Changes from Revision B (November 2017) to Revision C	Page
• 将预览 SC70 封装更改为生产数据	1

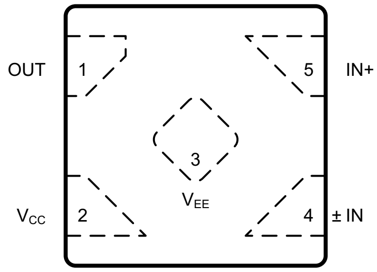
Changes from Revision A (July 2017) to Revision B	Page
• 已将传播延迟从 200ns 更改为 260ns	1
• 向数据表添加了预览 SC70 和 SOT-23 封装	1
• 应营销部门请求添加了 *TLV70x1 系列微功耗比较器*	1
• 已将重要图形标题从*传播延迟与过驱电压 (TLV7011)* *间的关系*更改为*传播延迟与过驱电压间的关系*	1
• Removed (TLV7011 only) text from several *Typical Characteristics* graphs	10
• Removed some *Typical Characteristics* graphs	10
• Added 图 14	10
• Added 图 21	12
• Added content to the *Inputs* section	16
• Added the *IR Receiver Analog Front End* section	21

Changes from Original (May 2017) to Revision A **Page**

- 将器件状态从“高级信息”更改为“生产数据” 1

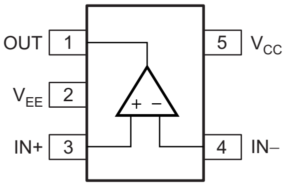
5 Pin Configuration and Functions

DPW Package
5-Pin X2SON
Top View



Not to scale

DBV and DCK Package
5-Pin SOT-23 and SC70
Top View

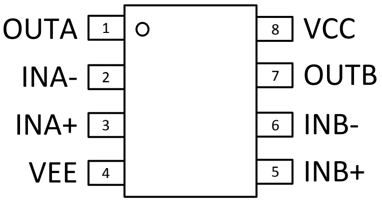


Pin Functions

PIN			I/O/P(1)	DESCRIPTION
NAME	X2SON	SOT-23, SC70		
OUT	1	1	O	Output
V_{CC}	2	5	P	Positive (highest) power supply
V_{EE}	3	2	P	Negative (lowest) power supply
IN–	4	4	I	Inverting input
IN+	5	3	I	Noninverting input

(1) I = Input, O = Output, P = Power

TLV7012/22 DGK Packages
8-Pin VSSOP
Top View



Pin Functions: TLV7012/22

PIN		I/O	DESCRIPTION
NAME	NO.		
INA–	2	I	Inverting input, channel A
INA+	3	I	Noninverting input, channel A
INB–	6	I	Inverting input, channel B
INB+	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
VEE	4	—	Negative (lowest) supply or ground (for single-supply operation)
VCC	8	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings (Single)

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage ($V_S = V_{CC} – V_{EE}$)			6	V
Input pins (IN+, IN–)(2)		V_{EE} – 0.3	6	V
Current into Input pins (IN+, IN–)(2)			±10	mA
Output (OUT)	TLV7011/7012(3)	V_{EE} – 0.3	V_{CC} + 0.3	V
	TLV7021/7022	V_{EE} – 0.3	6	
Output short-circuit duration(4)			10	s
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to V_{EE}. Input signals that can swing 0.3V below V_{EE} must be current-limited to 10mA or less.
(3) Output maximum is (V_{CC} + 0.3V) or 6V, whichever is less.
(4) Short-circuit to ground, one comparator per package.

6.2 Absolute Maximum Ratings (Dual)

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} - V_{EE}$	–0.3	7	V
Input pins (IN+, IN-)(2)	V_{EE} – 0.3	7	V
Current into Input pins (IN+, IN-)		±10	mA
Output (OUT) (TLV7012)(3)	V_{EE} – 0.3	V_{CC} + 0.3	V
Output (OUT) (TLV7022)	V_{EE} – 0.3	7	V
Output short-circuit duration(4)		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to V_{EE}. Input signals that can swing 0.3V below V_{EE} must be current-limited to 10mA or less
(3) Output maximum is (V_{CC} + 0.3 V) or 7 V, whichever is less.
(4) Short-circuit to ground, one comparator per package.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions (Single)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage ($V_S = V_{CC} – V_{EE}$)		1.6		5.5	V
Input Voltage Range		V_{EE} – 0.1		V_{CC} + 0.2	V
Ambient temperature, T_A		–40		125	°C

6.5 Recommended Operating Conditions (Dual)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} – V_{EE}$	1.6	6.5	V
Input voltage range	V_{CC} – 0.1	V_{EE} + 0.2	V
Ambient temperature, T_A	–40	125	°C

6.6 Thermal Information (Single)

THERMAL METRIC[1]		TLV7011/TLV7021			UNIT
		DPW (X2SON)	DBV (SOT23)	DCK (SC70)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	497.5	306.3	278.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	275.5	228.4	188.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	372.2	166.5	113.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	55.5	138.5	82.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	370.3	165.3	112.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	165.1	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Thermal Information (Dual)

THERMAL METRIC[1]		TLV7012/TLV7022	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	211.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	133.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	28.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	131.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.8 Electrical Characteristics (Single)

V_S = 1.8 V to 5 V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_S = 1.8 V and 5 V, V_{CM} = V_S / 2		±0.5	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8 V and 5 V, V_{CM} = V_S / 2	1.2	4.2	14	mV
V_{CM}	Common-mode voltage range	V_S = 2.5 V to 5 V	V_{EE}		V_{CC} + 0.1	V
		V_S = 1.8 V to 2.5 V	V_{EE} + 0.1		V_{CC} + 0.1	
I_B	Input bias current			5		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (for TLV7011 only)	V_S = 5 V, I_O = 3 mA	4.7	4.8		V
V_{OL}	Output voltage low	V_S = 5 V, I_O = 3 mA		120	220	mV
I_{LKG}	Open-drain output leakage current (TLV7021 only)	V_S = 5 V, V_{ID} = +0.1 V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	$V_{EE} < V_{CM} < V_{CC}$, V_S = 5 V		78		dB
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5 V, V_{CM} = V_S / 2		78		dB
I_{SC}	Short-circuit current	V_S = 5 V, sourcing		65		mA
		V_S = 5 V, sinking		44		
I_{CC}	Supply current	V_S = 1.8 V, no load, V_{ID} = –0.1 V (Output Low)		5	10	µA

6.9 Switching Characteristics (Single)

Typical values are at T_A = 25°C, V_{CC} = 5 V, V_{CM} = 2.5 V; C_L = 15 pF, input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low (R_P = 2.5 kΩ TLV7021 only)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		260		ns
t_{PLH}	Propagation delay time, low-to-high (R_P = 2.5 kΩ TLV7021 only)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		310		ns
t_R	Rise time (for TLV7011 only)	20% to 80%		5		ns
t_F	Fall time	80% to 20%		5		ns
t_{ON}	Power-up time (1)			20		µs

(1) During power on, V_S must exceed 1.6 V for t_{ON} before the output tracks the input.

6.10 Electrical Characteristics (Dual)

V_S = 1.8 V to 5 V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8 V and 5 V, V_{CM} = VS / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8 V and 5 V, V_{CM} = VS / 2	2	9	15	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (for TLV7012 only)	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA		250	350	mV
I_{LKG}	Open-drain output leakage current (TLV7022 only)	V_S = 5 V, V_{ID} = +0.1 V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5 V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5 V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	VS = 5 V, sourcing (for TLV7012 only)		29		mA
		VS = 5 V, sinking		33		
I_{CC}	Supply current / Channel	V_S = 1.8 V, no load, V_{ID} = –0.1 V (Output Low)		4.7	9	µA

6.11 Switching Characteristics (Dual)

Typical values are at T_A = 25°C, V_S = 5 V, V_{CM} = V_S / 2; CL = 15 pF, input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99 kΩ TLV7022 only) (1)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		310		ns
t_{PLH}	Propagation delay time, low-to high (RP = 4.99 kΩ TLV7022 only) (1)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		260		ns
t_R	Rise time (TLV7012 only)	Measured from 20% to 80%		5		ns
t_F	Fall time	Measured from 20% to 80%		5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for 200 µs before the output is in correct state.		20		µs

(1) The lower limit for RP is 650 Ω

6.12 Timing Diagrams

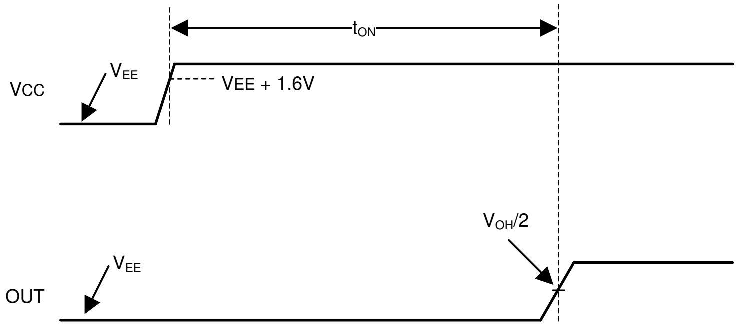


图 1. Start-Up Time Timing Diagram (IN+ > IN–)

Timing Diagrams (接下页)

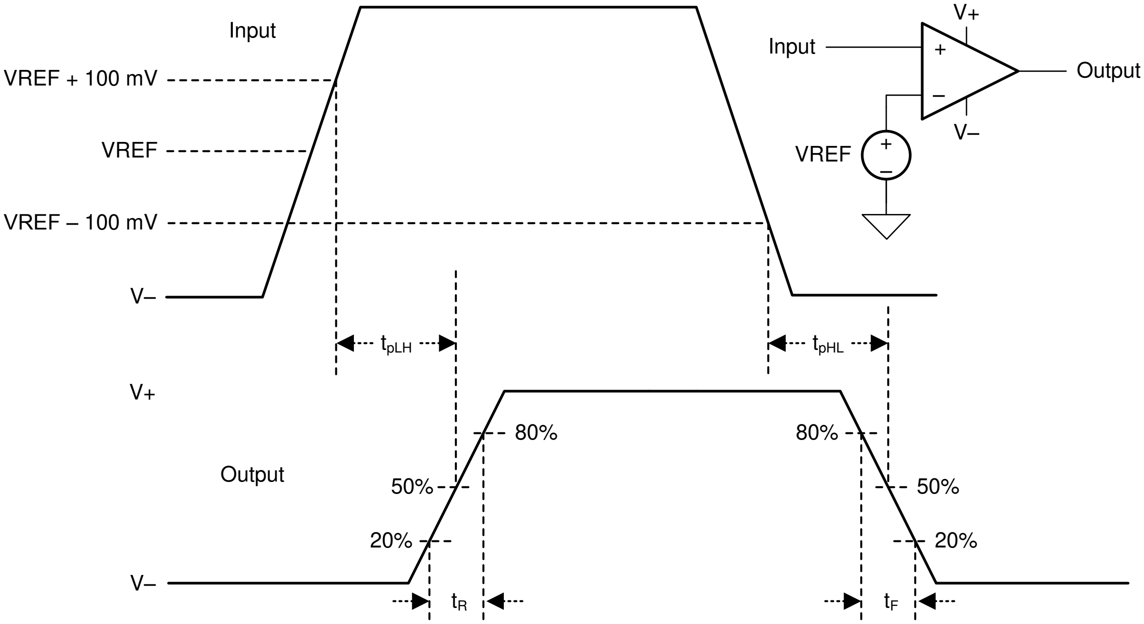
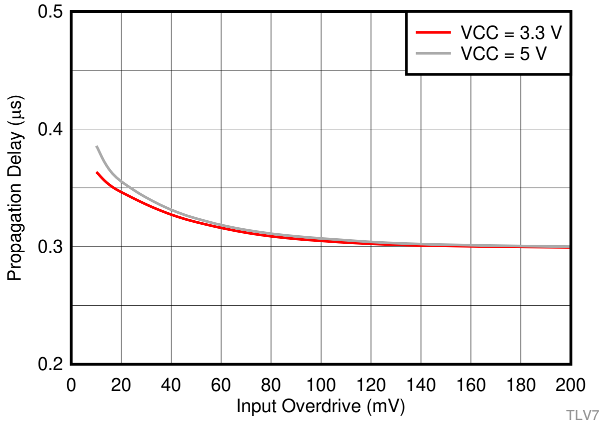


图 2. Propagation Delay Timing Diagram

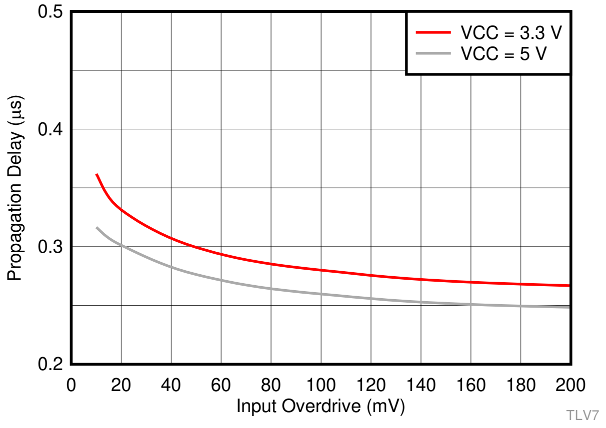
6.13 Typical Characteristics

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



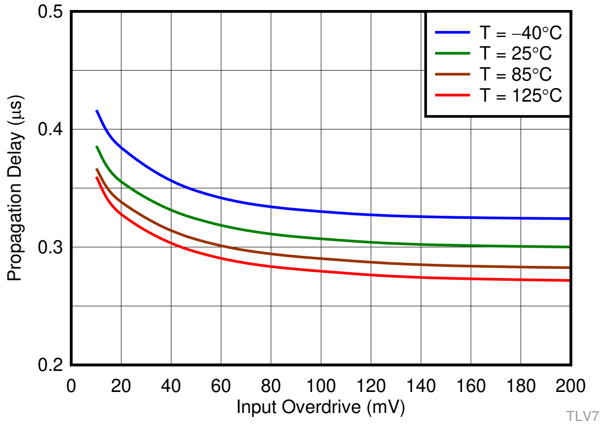
T_A = 25°C,

图 3. TLV7011 Propagation Delay (L-H) vs. Input Overdrive



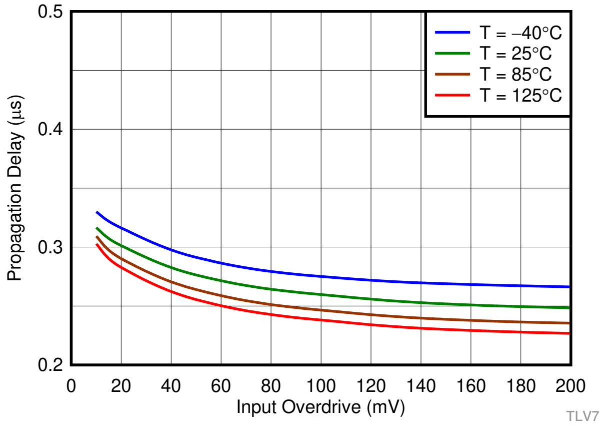
T_A = 25°C

图 4. Propagation Delay (H-L) vs. Input Overdrive



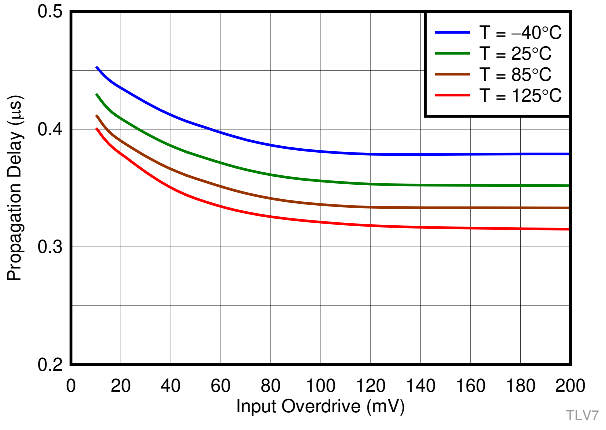
V_{CC} = 5 V

图 5. TLV7011 Propagation Delay (L-H) vs. Input Overdrive



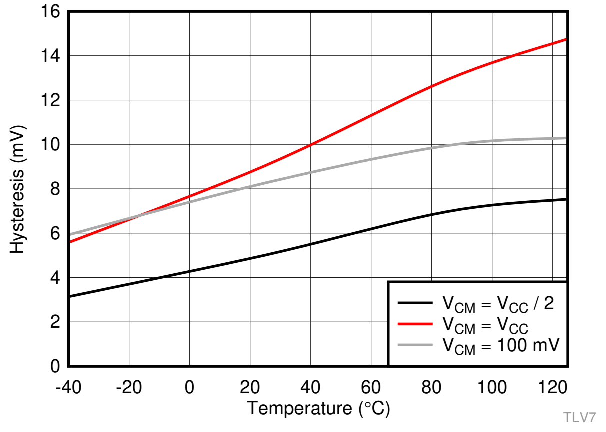
V_{CC} = 5 V

图 6. Propagation Delay (H-L) vs. Input Overdrive



$R_{pull-up}$ = 2.5k

图 7. TLV7021 Propagation Delay (L-H) vs. Input Overdrive



V_{CC} = 1.8 V

图 8. Hysteresis vs. Temperature

Typical Characteristics (接下页)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF

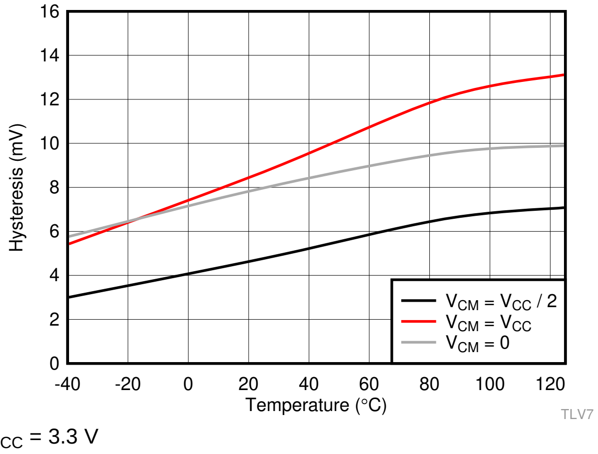


图 9. Hysteresis vs. Temperature

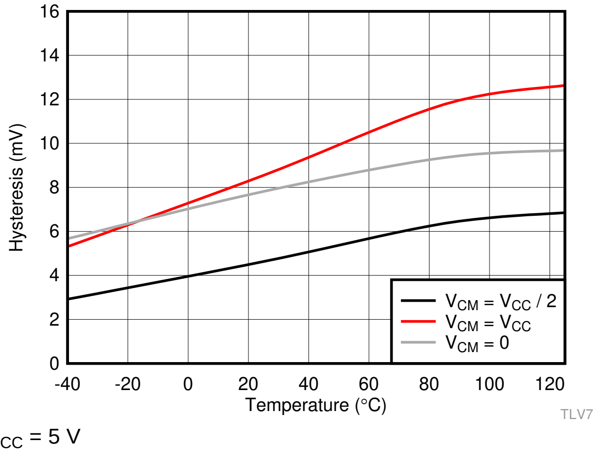


图 10. Hysteresis vs. Temperature

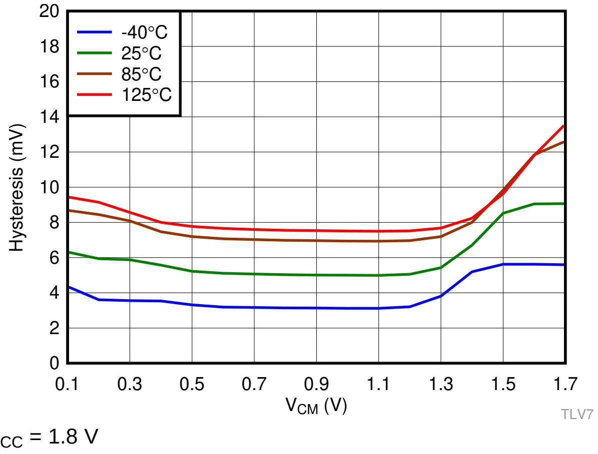


图 11. Hysteresis vs. V_{CM}

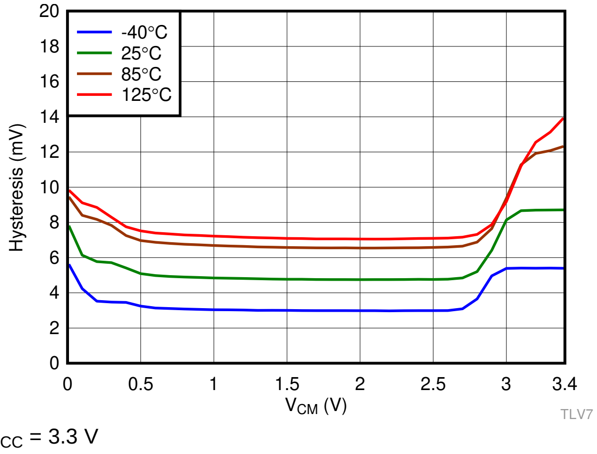


图 12. Hysteresis vs. V_{CM}

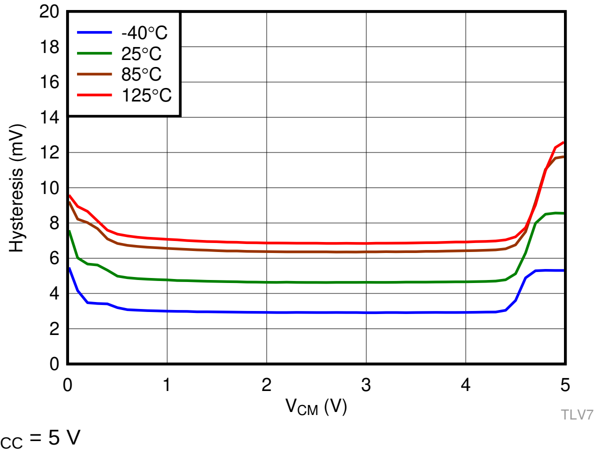


图 13. Hysteresis vs. V_{CM}

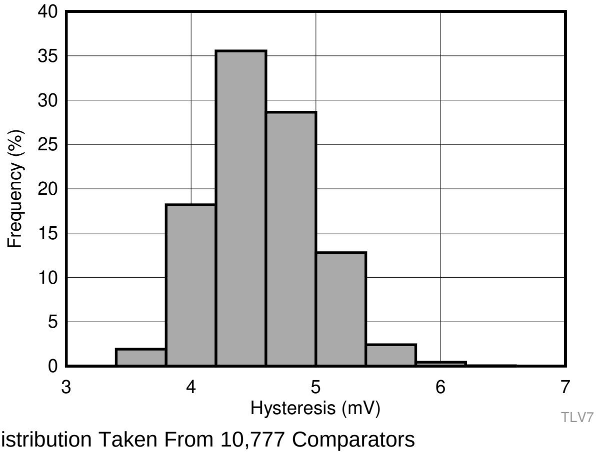
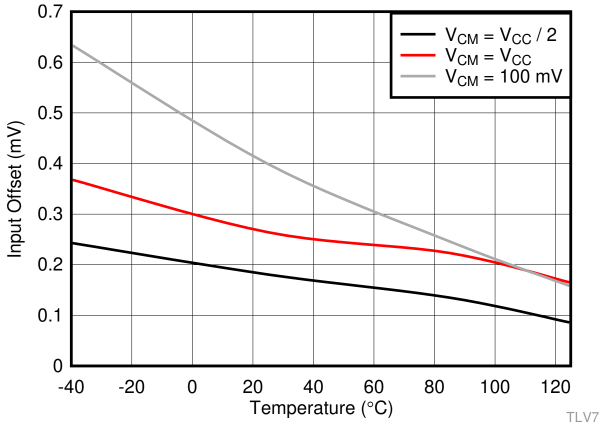


图 14. Hysteresis Histogram

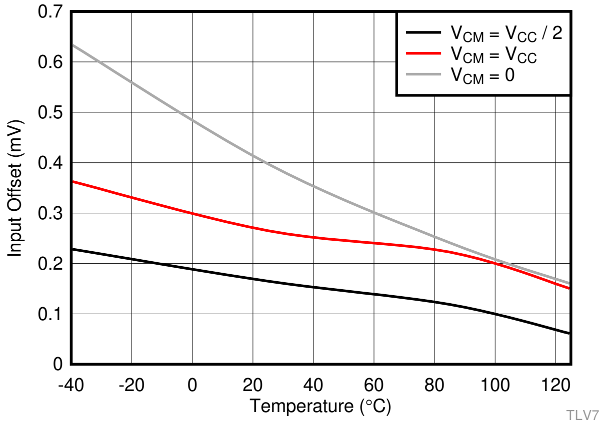
Typical Characteristics (接下页)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



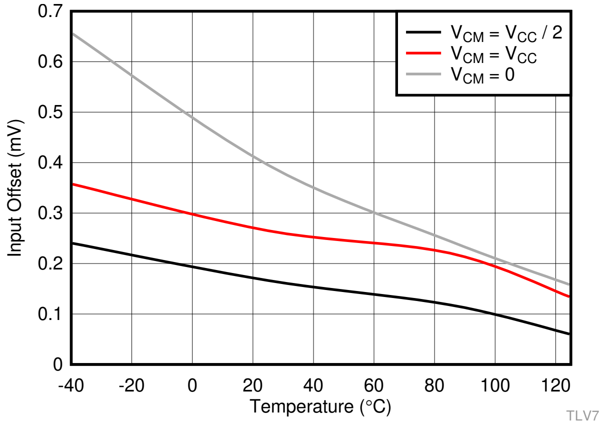
V_{CC} = 1.8 V

图 15. Input Offset vs. Temperature



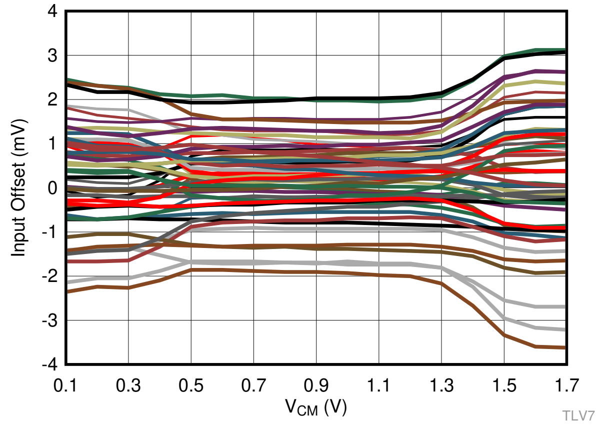
V_{CC} = 3.3 V

图 16. Input Offset vs. Temperature



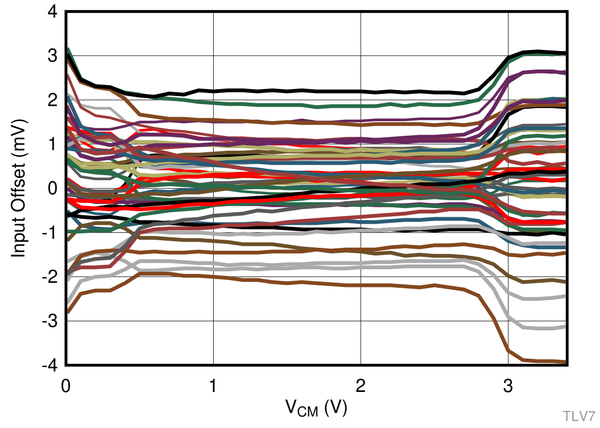
V_{CC} = 5 V

图 17. Input Offset vs. Temperature



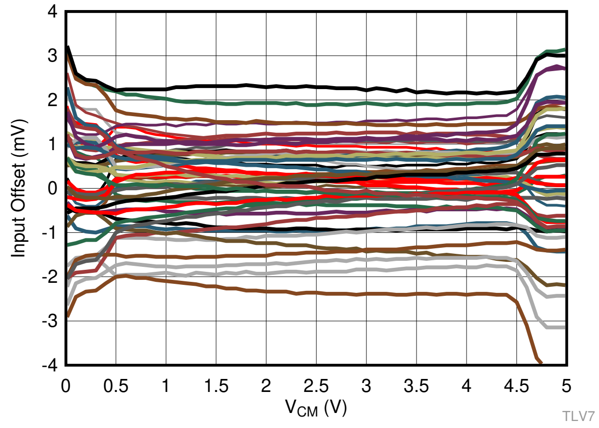
V_{CC} = 1.8 V, 50 devices

图 18. Input Offset Voltage vs. V_{CM}



V_{CC} = 3.3 V, 50 devices

图 19. Input Offset Voltage vs. V_{CM}

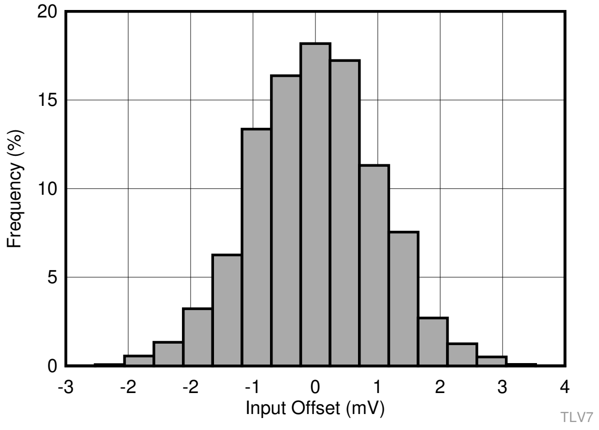


V_{CC} = 5 V, 50 devices

图 20. Input Offset Voltage vs. V_{CM}

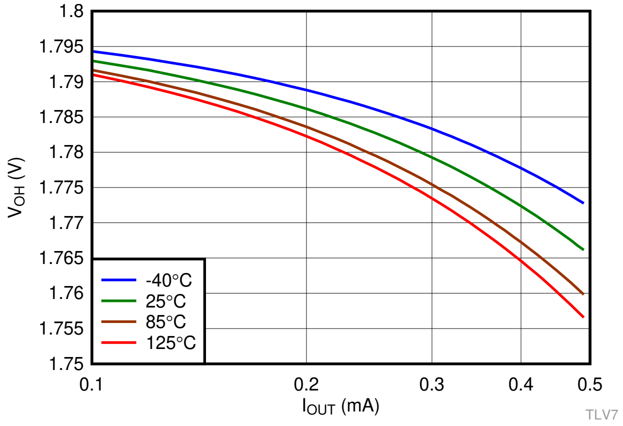
Typical Characteristics (接下页)

$T_A = 25°C$, $V_{CC} = 5$ V, $V_{EE} = 0$ V, $V_{CM} = V_{CC}/2$, $C_L = 15$ pF



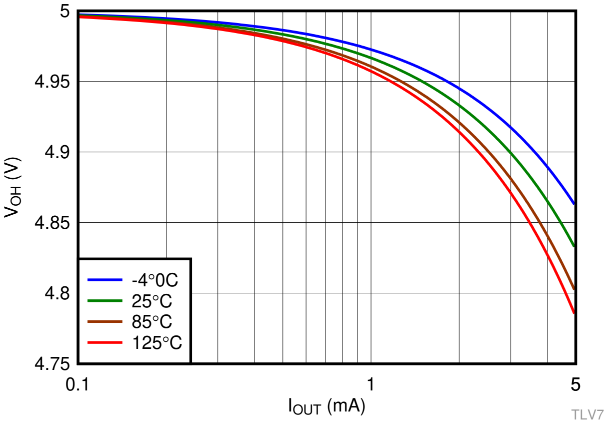
Distribution Taken From 10,777 Comparators

图 21. Input Offset Voltage Histogram



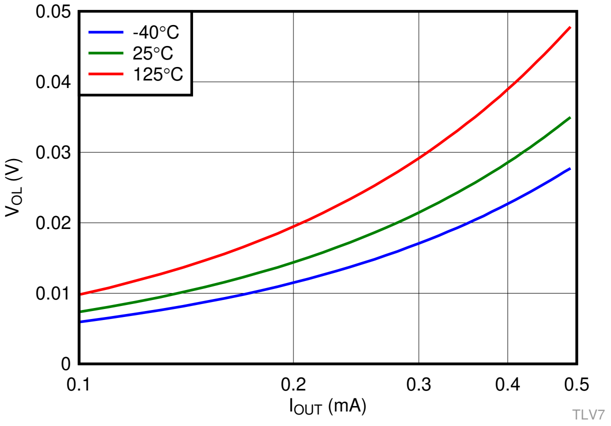
$V_{CC} = 1.8$ V

图 22. TLV7011 Output Voltage High vs. Output Source Current



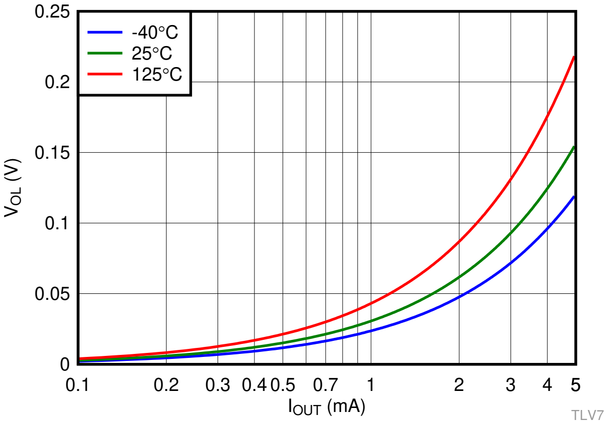
$V_{CC} = 5$ V

图 23. TLV7011 Output Voltage High vs. Output Source Current



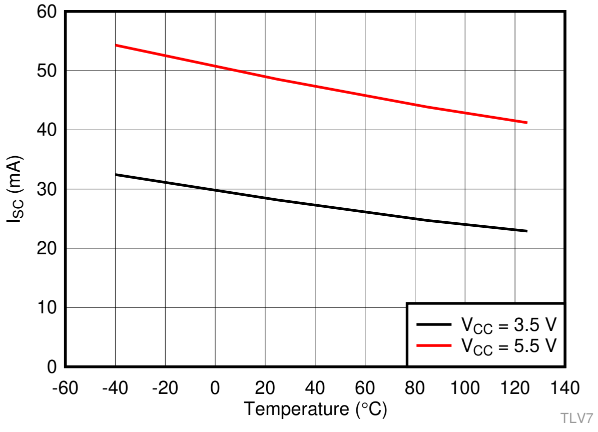
$V_{CC} = 1.8$ V

图 24. Output Voltage Low vs. Output Sink Current



$V_{CC} = 5$ V

图 25. Output Voltage Low vs. Output Sink Current

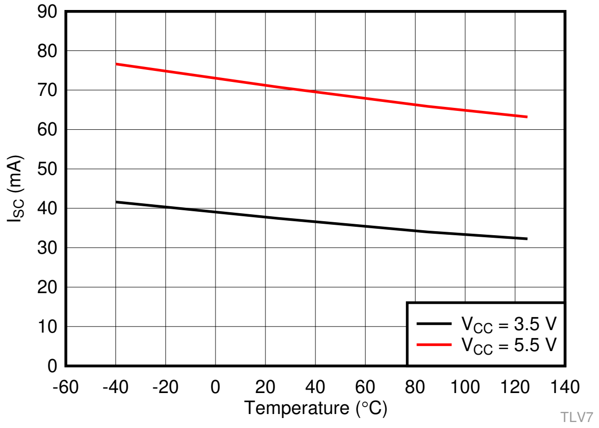


$V_{CM} = V_{CC}/2$

图 26. Output Short-Circuit (Sink) Current vs. Temperature

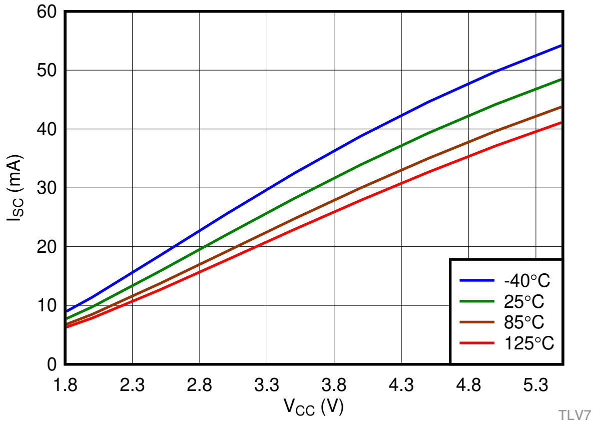
Typical Characteristics (接下页)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



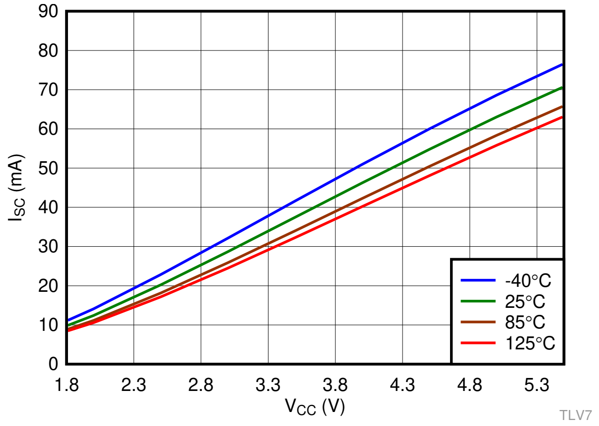
V_{CM} = V_{CC}/2

图 27. TLV7011 Output Short-Circuit (Source) Current vs. Temperature



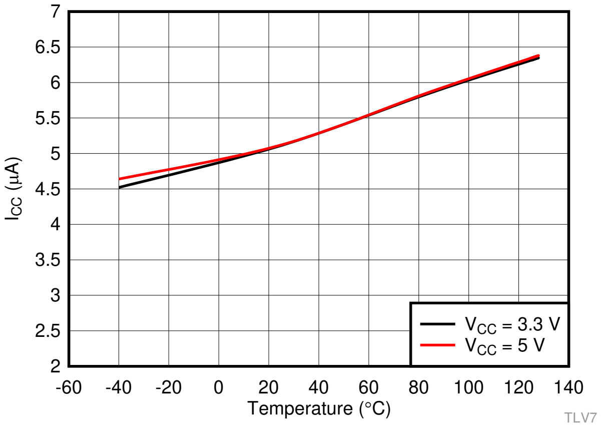
V_{CM} = V_{CC}/2

图 28. Output Short Circuit (Sink) vs. V_{CC}



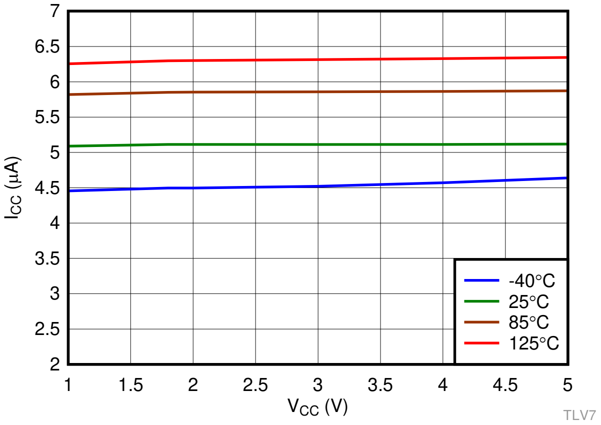
V_{CM} = V_{CC}/2

图 29. TLV7011 Output Short Circuit (Source) vs. V_{CC}



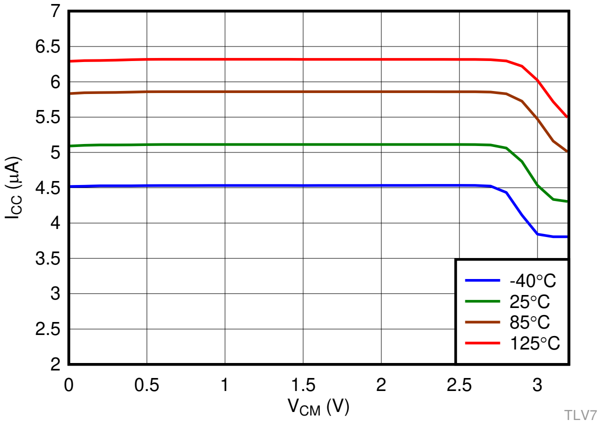
V_{CM} = V_{CC}/2

图 30. I_{CC} vs. Temperature



V_{CM} = V_{CC}/2

图 31. I_{CC} vs. V_{CC}

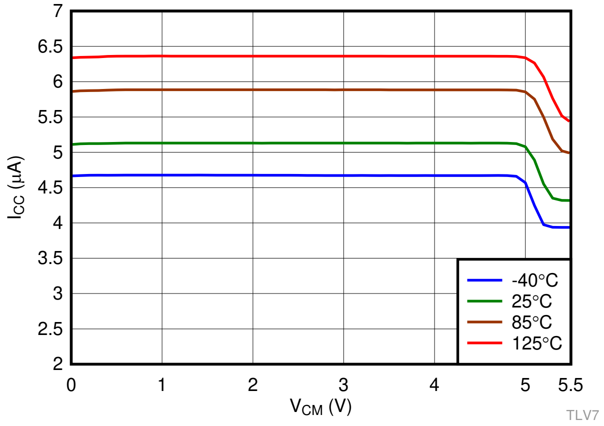


V_{CC} = 3.3 V

图 32. I_{CC} vs. V_{CM}

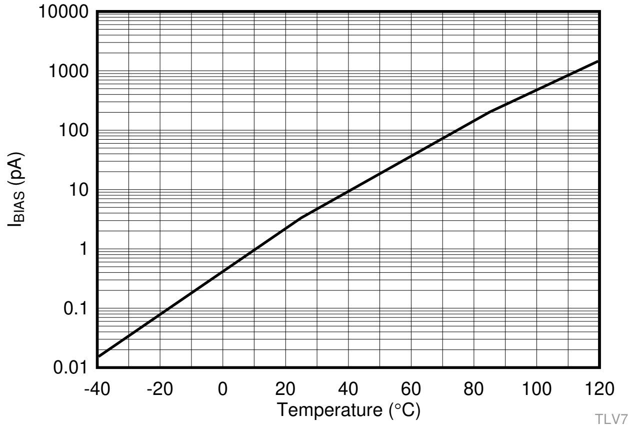
Typical Characteristics (接下页)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



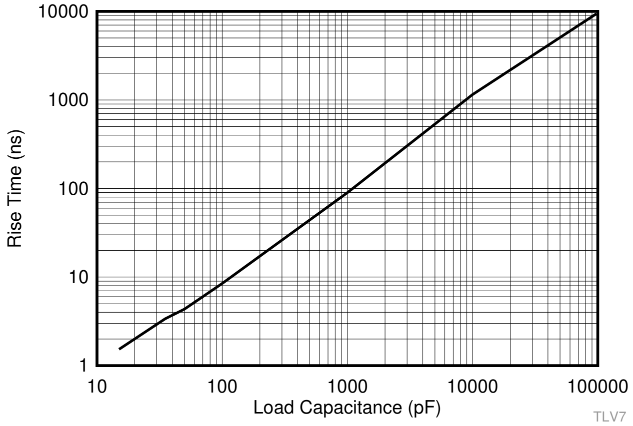
V_{CC} = 5 V

图 33. I_{CC} vs. V_{CM}



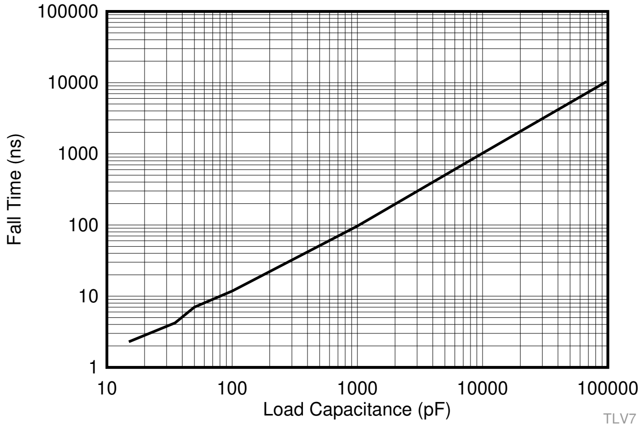
V_{CC} = 3.3V

图 34. Input Bias Current vs. Temperature



V_{OD} = 100mV

图 35. TLV7011 Output Rise Time vs. Load Capacitance



V_{OD} = 100mV

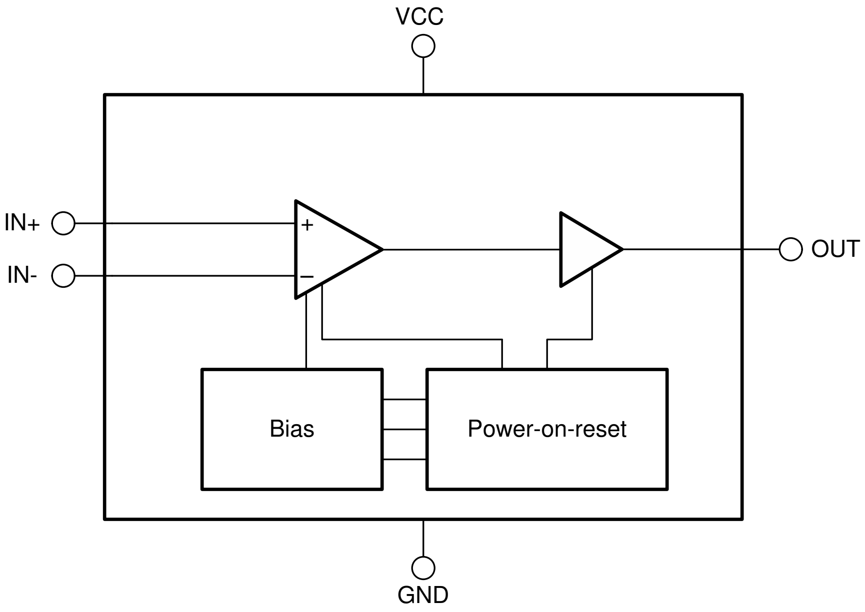
图 36. Output Fall Time vs. Load Capacitance

7 Detailed Description

7.1 Overview

The TLV701x and TLV702x devices are single-channel, micro-power comparators with push-pull and open-drain outputs. Operating down to 1.6 V and consuming only 5 µA, the TLV701x and TLV702x are ideally suited for portable and industrial applications. The comparators are available in leadless and leaded packages to offer significant board space saving in space-challenged designs.

7.2 Functional Block Diagram



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7.3 Feature Description

The TLV701x (push-pull) and TLV702x (open-drain) devices are micro-power comparators that are capable of operating at low voltages. The TLV701x and TLV702x feature a rail-to-rail input stage capable of operating up to 100 mV beyond the VCC power supply rail. The comparators also feature a push-pull and open-drain output stage with internal hysteresis.

7.4 Device Functional Modes

The TLV701x and TLV702x have a Power-on-Reset (POR) circuit. While the power supply (V_S) is ramping up or ramping down, the POR circuitry will be activated.

For the TLV701x, the POR circuit will hold the output low (at V_{EE}) while activated.

For the TLV702x, the POR circuit will keep the output high impedance (logical high) while activated.

When the supply voltage is greater than, or equal to, the minimum supply voltage, the comparator output reflects the state of the differential input (V_{ID}).

7.4.1 Inputs

The TLV701x and TLV702x input common-mode extends from V_{EE} to 100 mV above V_{CC}. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output will occur when the input pins exceed V_{CC} and V_{EE}.

Device Functional Modes (接下页)

While TI recommends operating the TLV701x and TLV702x within the specified common-mode range, the inputs are fault tolerant to voltages up to 5.5 V independent of the applied V_{CC} value. Fault tolerant is defined as maintaining the same high input impedance when V_{CC} is unpowered or within the recommended operating range. Because the inputs of the TLV701x and TLV702x are fault tolerant, the inputs to the comparator can be any value between 0 V and 5.5 V while V_{CC} is ramping up. This feature allows any supply and input driven sequence as long as the input value and supply are within the specified ranges. In this case, no current limiting resistor is required. This is possible since the V_{CC} is isolated from the inputs such that it maintains its value even when a higher voltage is applied to the input.

The input bias current is typically 1 pA for input voltages between V_{CC} and V_{EE}. The comparator inputs are protected from undervoltage by internal diodes connected to V_{EE}. As the input voltage goes under V_{EE}, the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles for 10°C temperature increases.

7.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in 图 37. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (4.2 mV for the TLV7011).

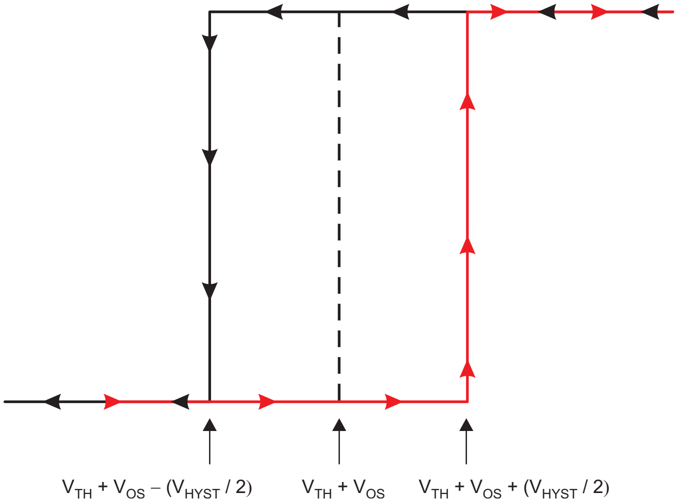

图 37. Hysteresis Transfer Curve

7.4.3 Output

The TLV701x feature a push-pull output stage eliminating the need for an external pull-up resistor. On the other hand, the TLV702x feature an open-drain output stage enabling the output logic levels to be pulled up to an external source independent of the supply voltage.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV701x and TLV702x are micro-power comparators with reasonable response time. The comparators have a rail-to-rail input stage that can monitor signals beyond the positive supply rail with integrated hysteresis. When higher levels of hysteresis are required, positive feedback can be externally added. The push-pull output stage of the TLV701x is optimal for reduced power budget applications and features no shoot-through current. When level shifting or wire-ORing of the comparator outputs is needed, the TLV702x with its open-drain output stage is well suited to meet the system needs. In either case, the wide operating voltage range, low quiescent current, and micro-package of the TLV701x and TLV702x make these comparators excellent candidates for battery-operated and portable, handheld designs.

8.1.1 Inverting Comparator With Hysteresis for TLV701x

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in 图 38. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. 公式 1 defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. Use 公式 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

公式 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

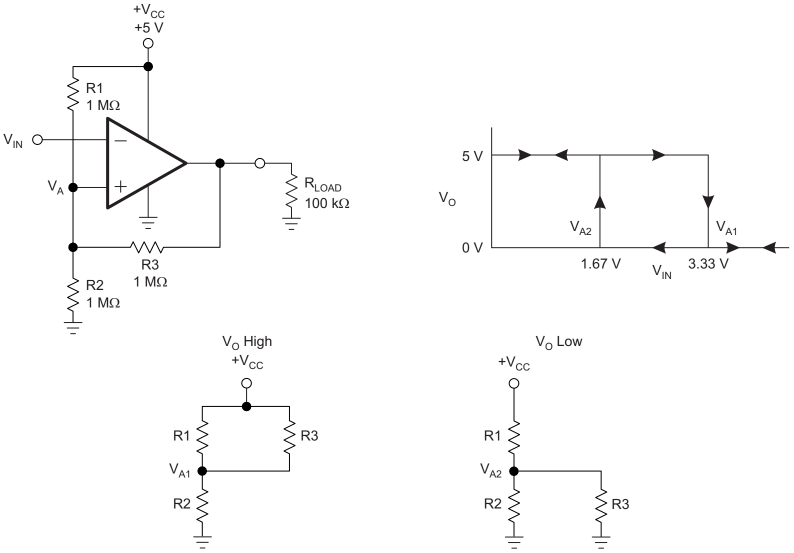

图 38. TLV701x in an Inverting Configuration With Hysteresis

Application Information (接下页)

8.1.2 Noninverting Comparator With Hysteresis for TLV701x

A noninverting comparator with hysteresis requires a two-resistor network, as shown in 图 39, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise to V_{IN1}. Use 公式 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is high, the output is also high. For the comparator to switch back to a low state, V_{IN} must drop to V_{IN2} such that V_A is equal to V_{REF}. Use 公式 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in 公式 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

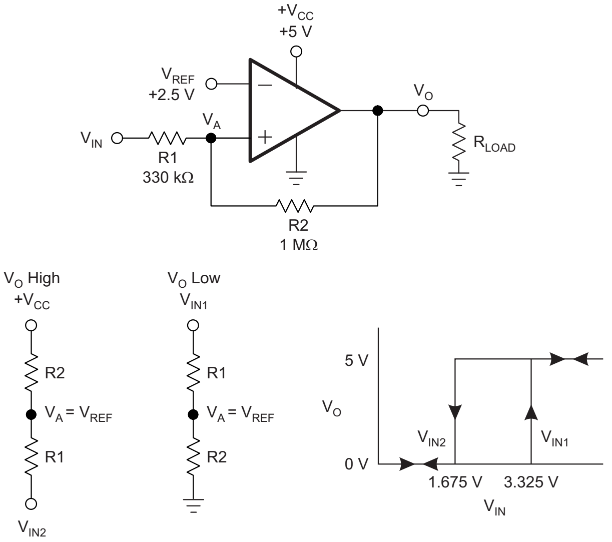

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图 39. TLV701x in a Noninverting Configuration With Hysteresis

8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. 图 40 shows a simple window comparator circuit.

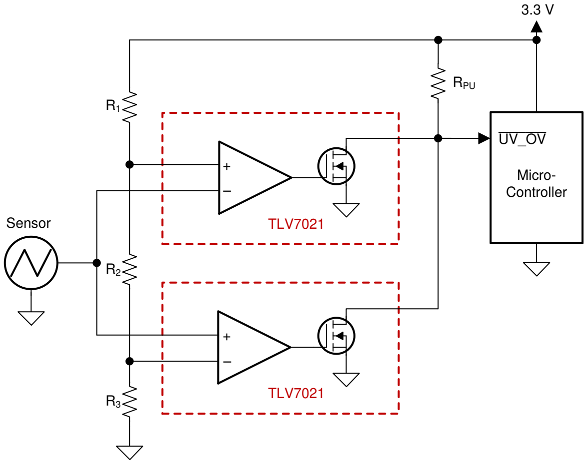


图 40. Window Comparator

8.2.1.1 *Design Requirements*

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

8.2.1.2 *Detailed Design Procedure*

Configure the circuit as shown in 图 40. Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R1, R2 and R3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$). With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10-MΩ are used to minimize power consumption. The sensor output voltage is applied to the inverting and noninverting inputs of the two TLV702x's. The TLV7021 is used for its open-drain output configuration. Using the TLV702x allows the two comparator outputs to be Wire-Ored together. The respective comparator outputs will be low when the sensor is less than 1.1 V or greater than 2.2 V. V_{OUT} will be high when the sensor is in the range of 1.1 V to 2.2 V.

Typical Applications (接下页)

8.2.1.3 Application Curve

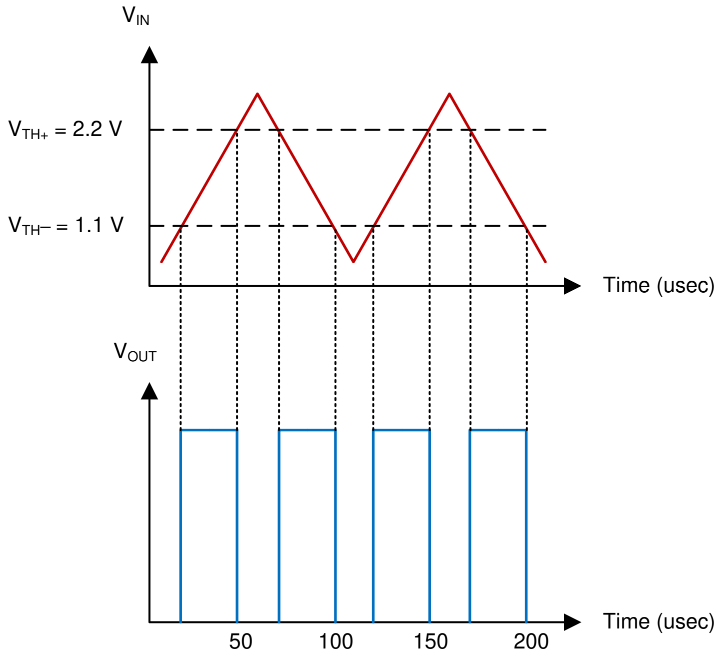


图 41. **Window Comparator Results**

8.2.2 IR Receiver Analog Front End

A single TLV7011 device can be used to build a complete IR receiver analog front end (AFE). The nanoamp quiescent current and low input bias current make it possible to be powered with a coin cell battery, which could last for years.

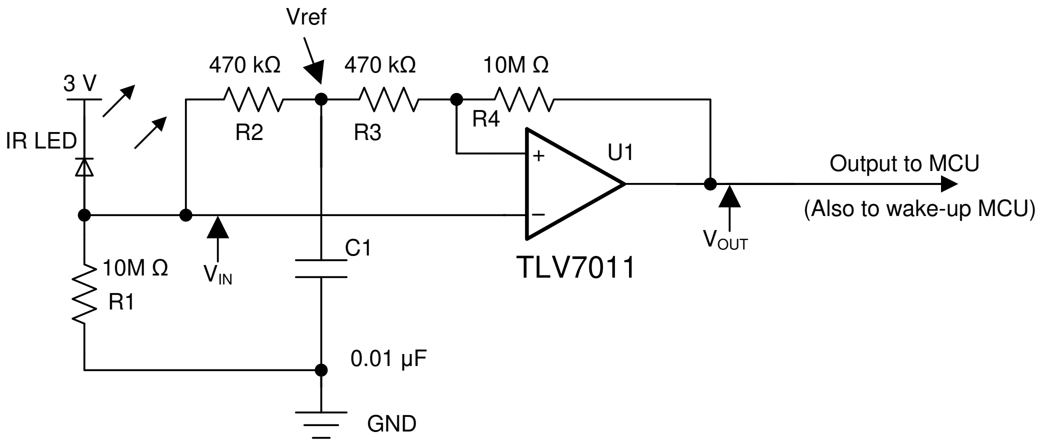


图 42. **IR Receiver Analog Front End Using TLV7011**

8.2.2.1 Design Requirements

For this design, follow these design requirements:

- Use a proper resistor (R_1) value to generate an adequate signal amplitude applied to the inverting input of the comparator.
- The low input bias current I_B (2 pA typical) ensures that a greater value of R1 to be used.

Typical Applications (接下页)

- The RC constant value (R_2 and C_1) must support the targeted data rate (that is, 9,600 bauds) to maintain a valid tripping threshold.
- The hysteresis introduced with R_3 and R_4 helps to avoid spurious output toggles.

8.2.2.2 Detailed Design Procedure

The IR receiver AFE design is highly streamlined and optimized. R_1 converts the IR light energy induced current into voltage and applies to the inverting input of the comparator. Because a reverse biased IR LED is used as the IR receiver, a higher I/V transimpedance gain is required to boost the amplitude of reduced current. A 10M resistor is used as R_1 to support a 1-V, 100-nA transimpedance gain. This is made possible with the picoamps Input bias current I_B (5pA typical). The RC network of R_2 and C_1 establishes a reference voltage V_{ref} which tracks the mean amplitude of the IR signal. The RC constant of R_2 and C_1 (about 4.7 ms) is chosen for V_{ref} to track the received IR current fluctuation but not the actual data bit stream. The noninverting input is connected to V_{ref} and the output over the R_3 and R_4 resistor network which provides additional hysteresis for improved guard against spurious toggles.

To reduce the current drain from the coin cell battery, data transmission must be short and infrequent.

8.2.2.3 Application Curve

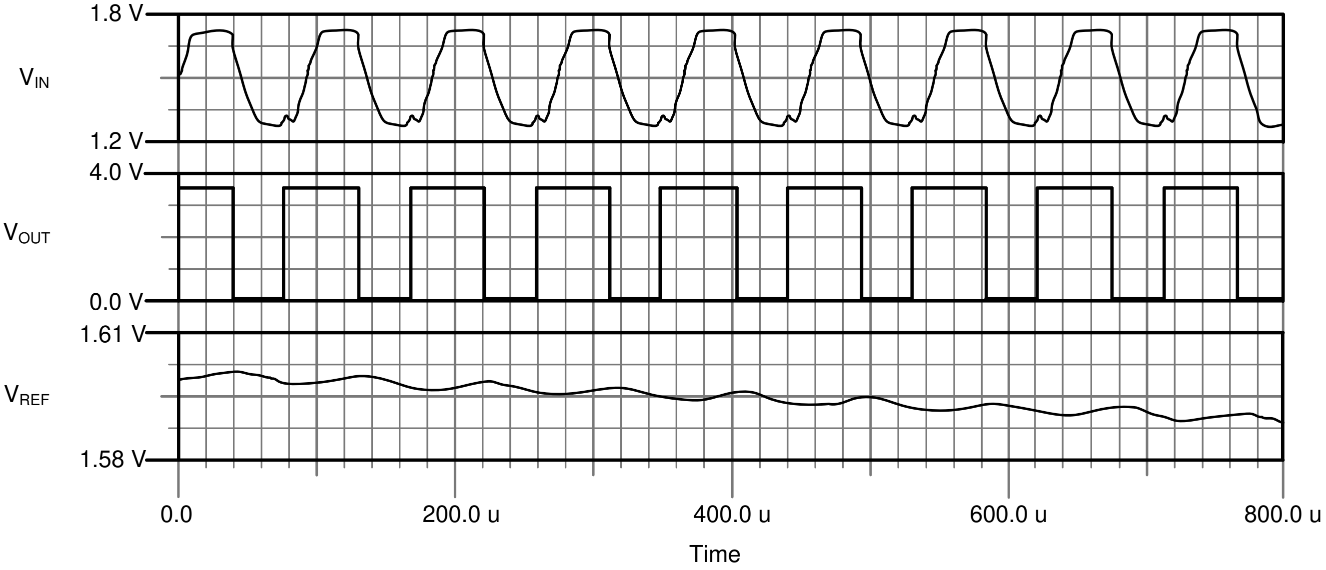


图 43. IR Receiver AFE Waveforms

Typical Applications (接下页)

8.2.3 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source.

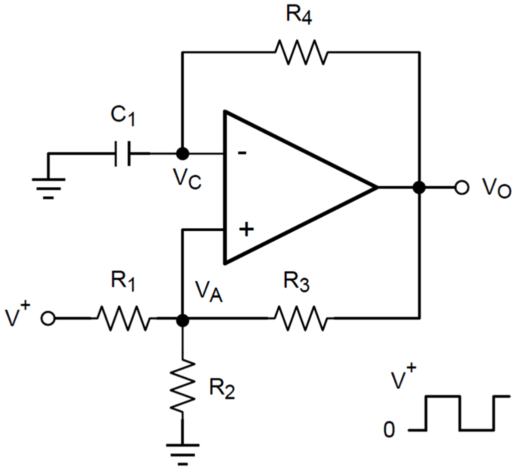


图 44. Square-Wave Oscillator

8.2.3.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor and resistor. The maximum frequency is limited by propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help to reduce BOM cost and board space.

8.2.3.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.

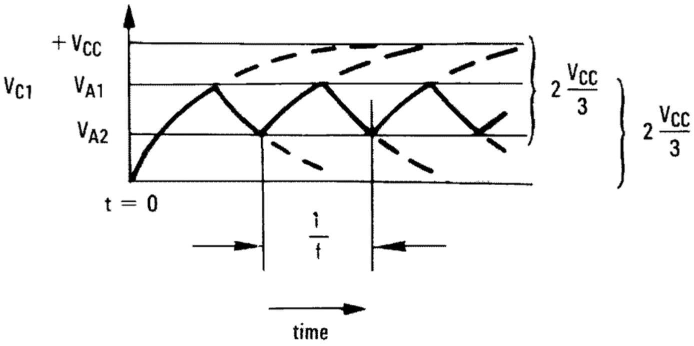


图 45. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure 图 44 is high which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated by 公式 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \parallel R_3} \quad (7)$$

if $R_1 = R_2 = R_3$, then $V_{A1} = 2\ V_{CC} / 3$

Typical Applications (接下页)

At this time the comparator output trips pulling down the output to the negative rail. The value of $V_A$at this point is calculated by 公式 8.

$$V_{A2} = \frac{V_{CC}(R_2 II R_3)}{R_1 + R_2 II R_3} \tag{8}$$

if $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until it reaches V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for C_1 from $2V_{CC}/3$ to V_{CC} / 3 then back to $2V_{CC}/3$, which is given by R_4C_1 × ln 2 fro each trip. Therefore, the total time duration is calculated as 2 R_4C_1 × ln 2. The oscillation frequency can be obtained by 公式 9:

$$f = 1/\left(2\ R4 \times C1 \times \ln 2\right) \tag{9}$$

8.2.3.3 *Application Curve*

图 46 shows the simulated results of tan oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
- $C_1 = 100$ pF, $C_L = 20$ pF
- V+ = 5 V, V– = GND
- C_{stray} (not shown) from V_A TO GND = 10 pF

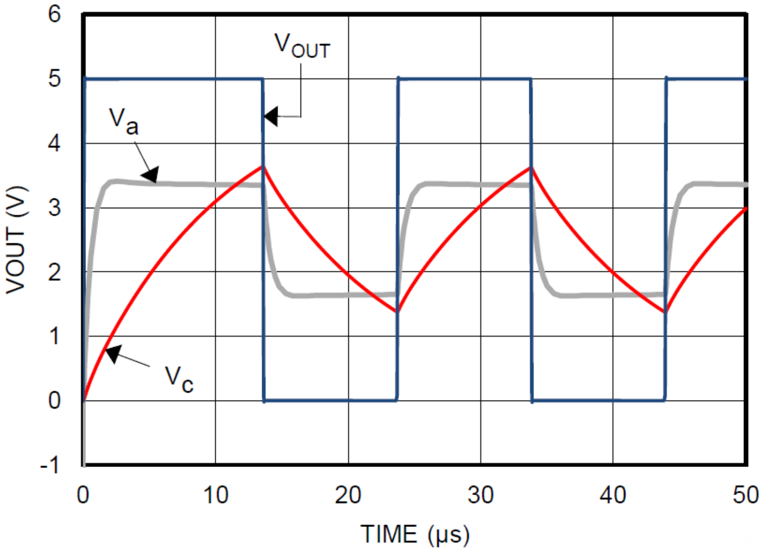


图 46. Square-Wave Oscillator Output Waveform

9 Power Supply Recommendations

The TLV701x and TLV702x have a recommended operating voltage range (V_S) of 1.6 V to 5.5 / 6.5 V. V_S is defined as $V_{CC} – V_{EE}$. Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5 V and 0 V and bipolar supply voltages of +2.5 V and –2.5 V create comparable operating voltages for V_S. However, when bipolar supply voltages are used, it is important to realize that the logic low level of the comparator output is referenced to V_{EE}.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

10 Layout

10.1 Layout Guidelines

To reduce PCB fabrication cost and improve reliability, TI recommends using a 4-mil via at the center pad connected to the ground trace or plane on the bottom layer.

A power-supply bypass capacitor of 100 nF is recommended when supply output impedance is high, supply traces are long, or when excessive noise is expected on the supply lines. Bypass capacitors are also recommended when the comparator output drives a long trace or is required to drive a capacitive load. Due to the fast rising and falling edge rates and high-output sink and source capability of the TLV7011 and TLV7021 output stages, higher than normal quiescent current can be drawn from the power supply. Under this circumstance, the system would benefit from a bypass capacitor across the supply pins.

10.2 Layout Example

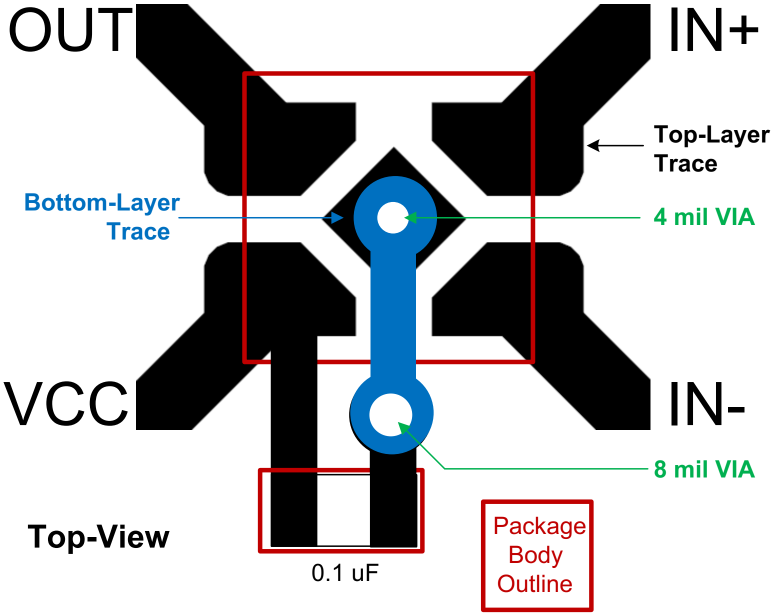


图 47. Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

我们为您提供了评估模块 (EVM)，可以借此来对使用 TLV70x1 器件系列的电路性能进行初始评估。TLV7011 微功耗比较器 DIP 适配器评估模块 可在德州仪器 (TI) 网站上的产品文件夹下申请，也可以直接从 TI 网上商店购买。

11.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **1.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
TLV7011	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV7021	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7011DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1IC2
TLV7011DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IC2
TLV7011DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IC2
TLV7011DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKT.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKTG4	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKTG4.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DCKTG4.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19N
TLV7011DPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7N
TLV7011DPWR.A	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7N
TLV7011DPWR.B	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7N
TLV7012DDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7012DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7012
TLV7021DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1ID2
TLV7021DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ID2
TLV7021DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ID2
TLV7021DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	19O

PACKAGE OPTION ADDENDUM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7021DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19O
TLV7021DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19O
TLV7021DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	19O
TLV7021DCKT.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19O
TLV7021DCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19O
TLV7021DPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7P
TLV7021DPWR.A	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7P
TLV7021DPWR.B	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7P
TLV7022DDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7022
TLV7022DDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7022
TLV7022DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Sn | Nipdau	Level-1-260C-UNLIM	-40 to 125	7022
TLV7022DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7022
TLV7022DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7022
TLV7022DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7022

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

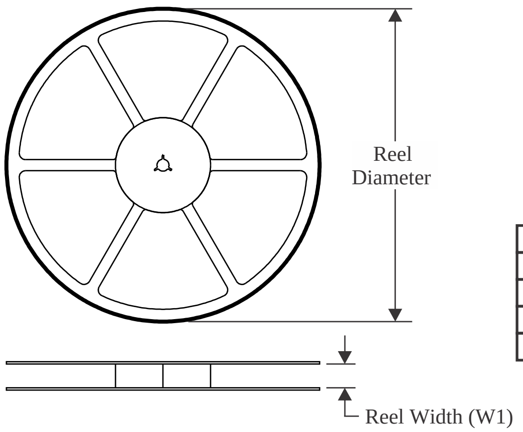
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

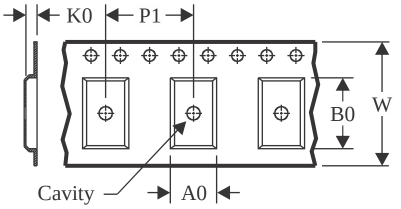
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

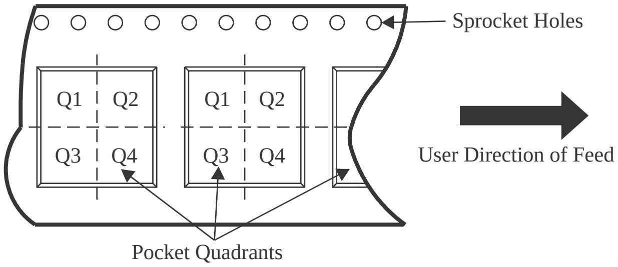


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

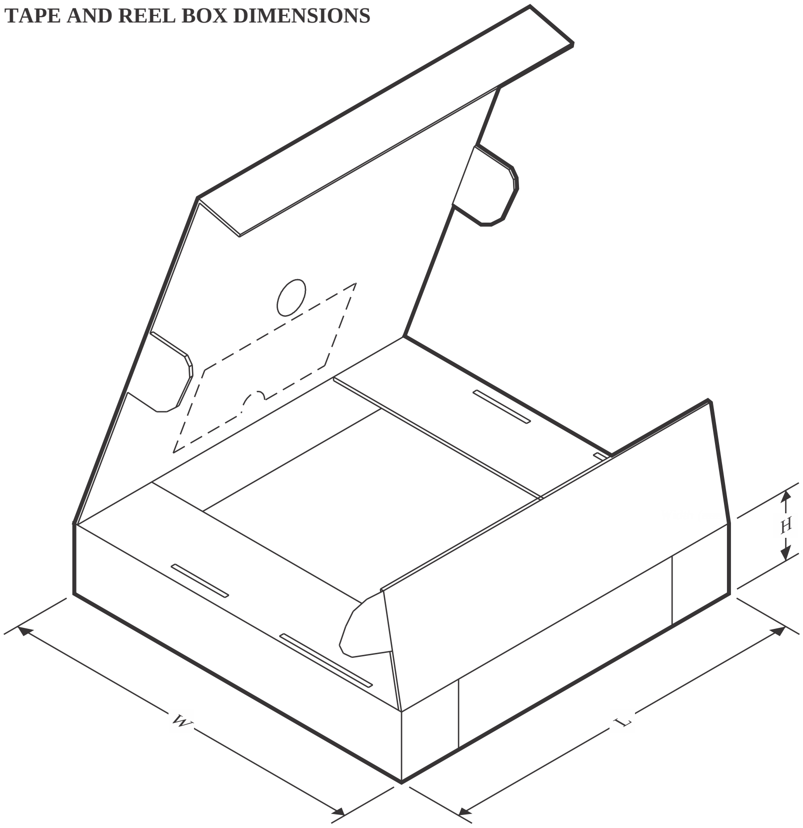


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7011DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7011DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7011DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7011DCKTG4	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7011DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV7012DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7012DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7012DGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7012DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV7021DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7021DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
TLV7021DCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV7021DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV7022DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7022DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7022DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

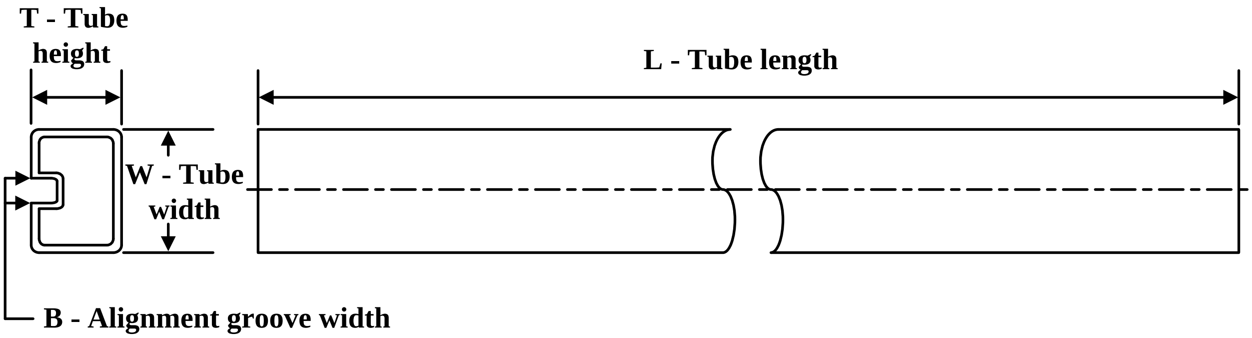
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7011DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV7011DCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV7011DCKT	SC70	DCK	5	250	190.0	190.0	30.0
TLV7011DCKTG4	SC70	DCK	5	250	190.0	190.0	30.0
TLV7011DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV7012DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7012DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7012DGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7012DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV7021DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV7021DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
TLV7021DCKT	SC70	DCK	5	250	210.0	185.0	35.0
TLV7021DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV7022DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7022DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7022DSGR	WSON	DSG	8	3000	210.0	185.0	35.0

TUBE



*All dimensions are nominal

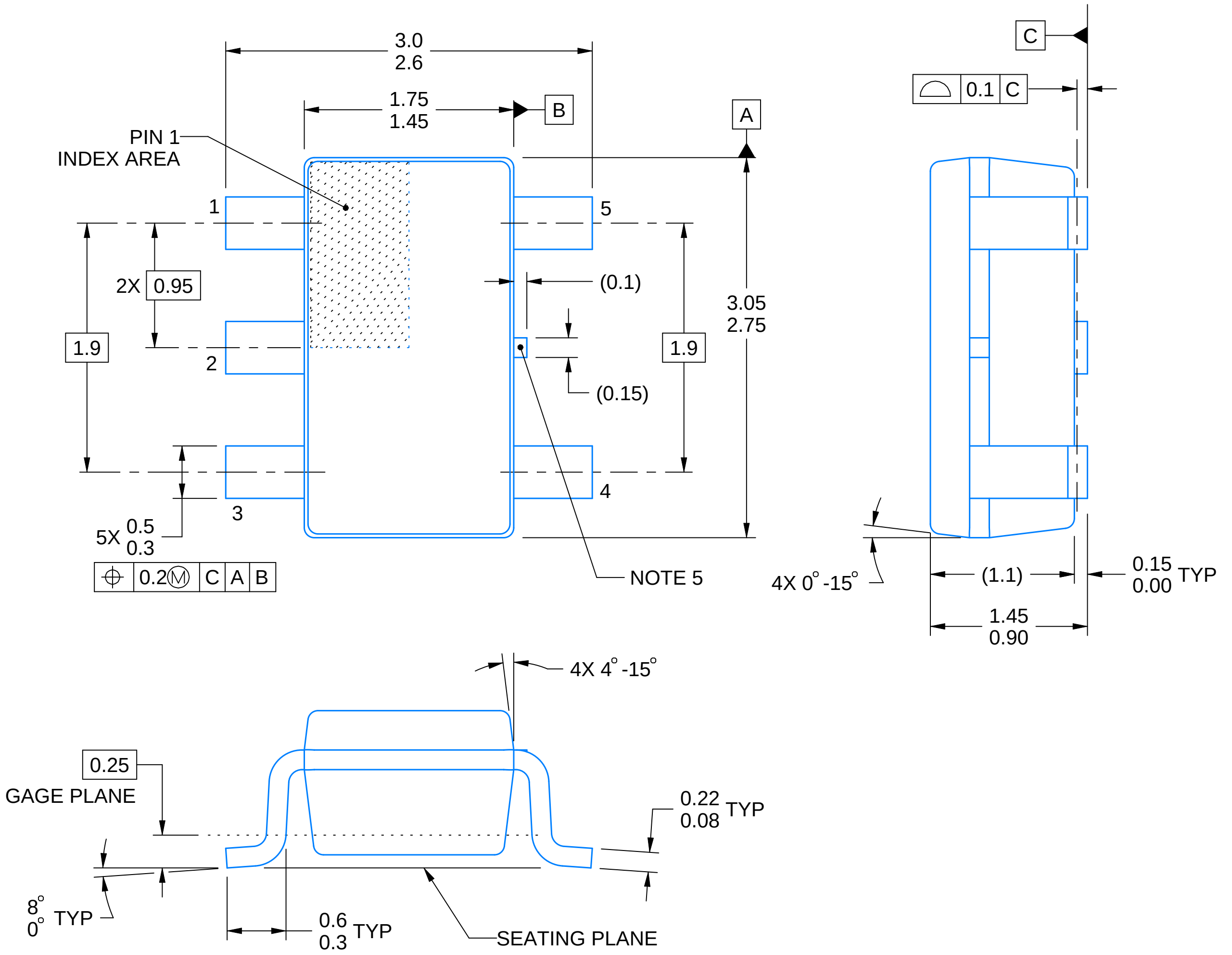
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV7022DGKR	DGK	VSSOP	8	2500	328	7.98	550	NA
TLV7022DGKR.A	DGK	VSSOP	8	2500	328	7.98	550	NA

DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

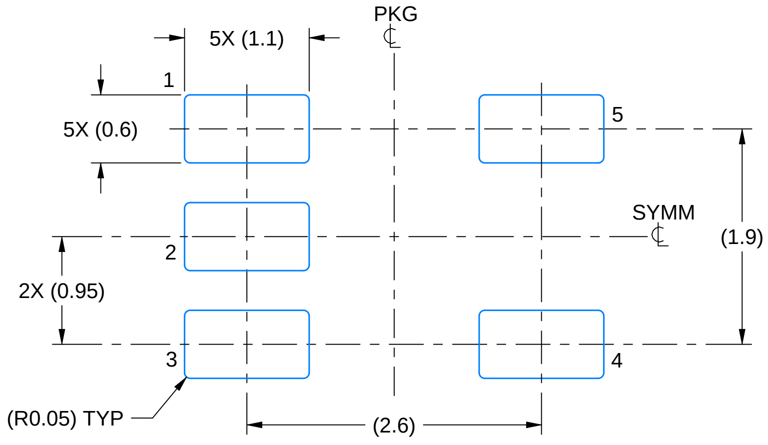
SMALL OUTLINE TRANSISTOR



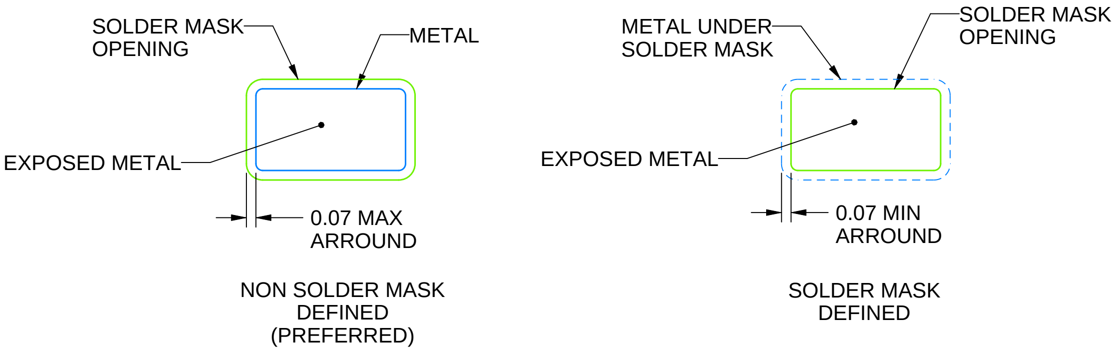
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

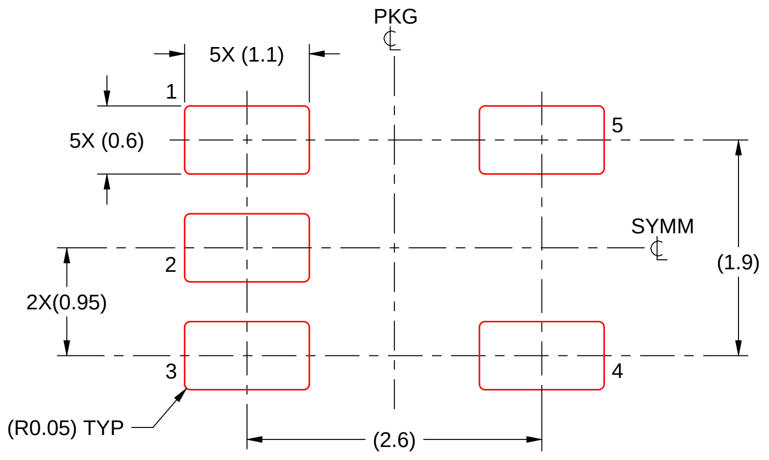


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

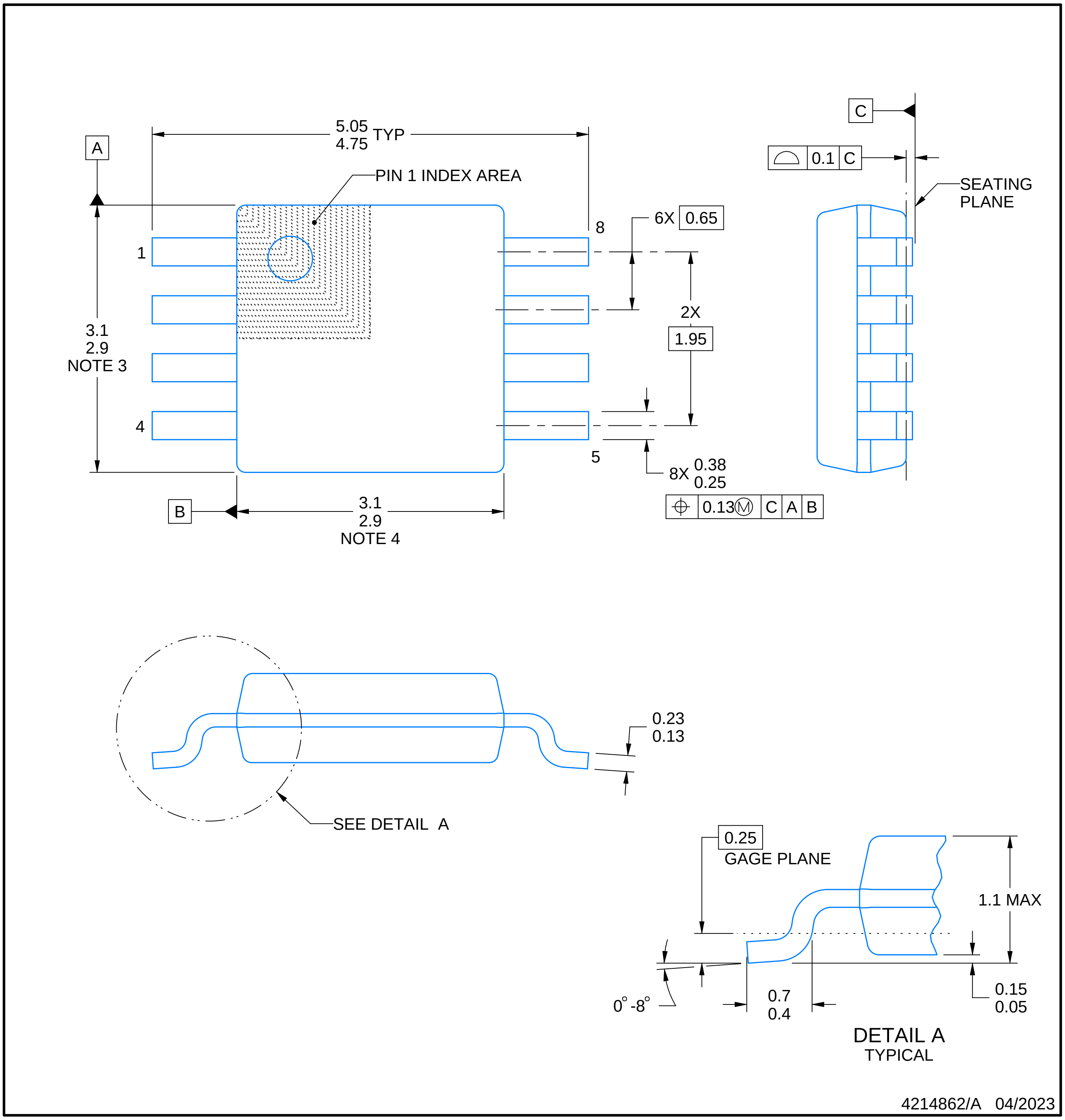
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

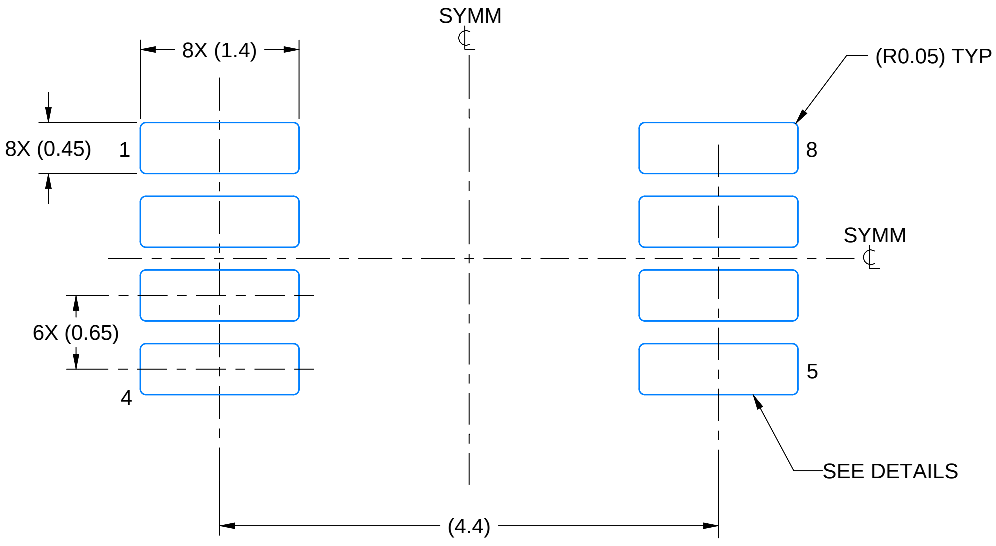


4214862/A 04/2023

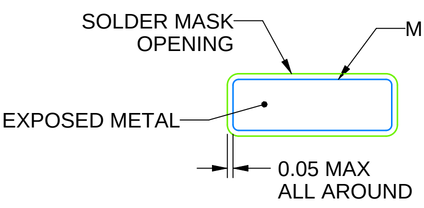
PowerPAD is a trademark of Texas Instruments.

NOTES:

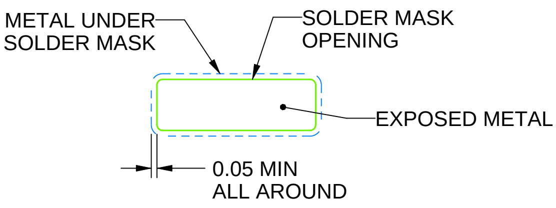
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)



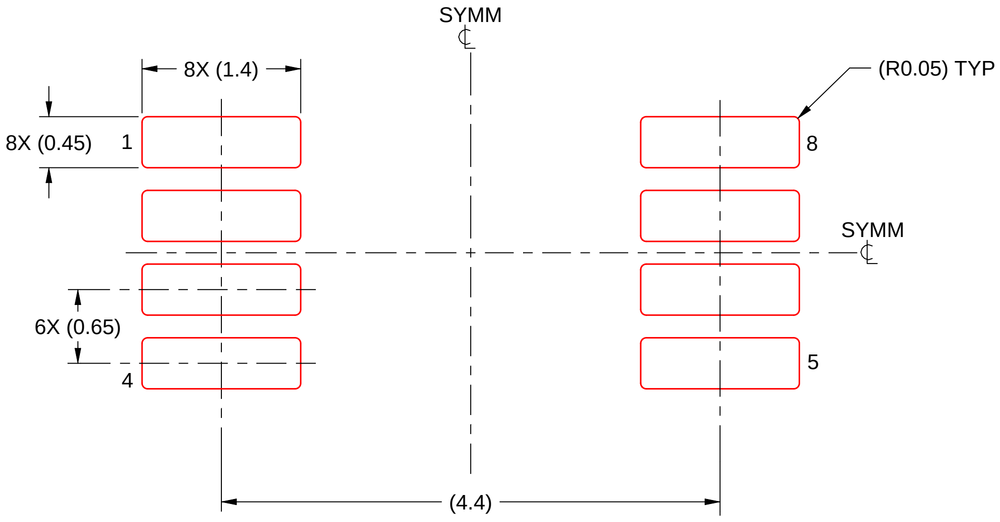
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

NOTES: (continued)

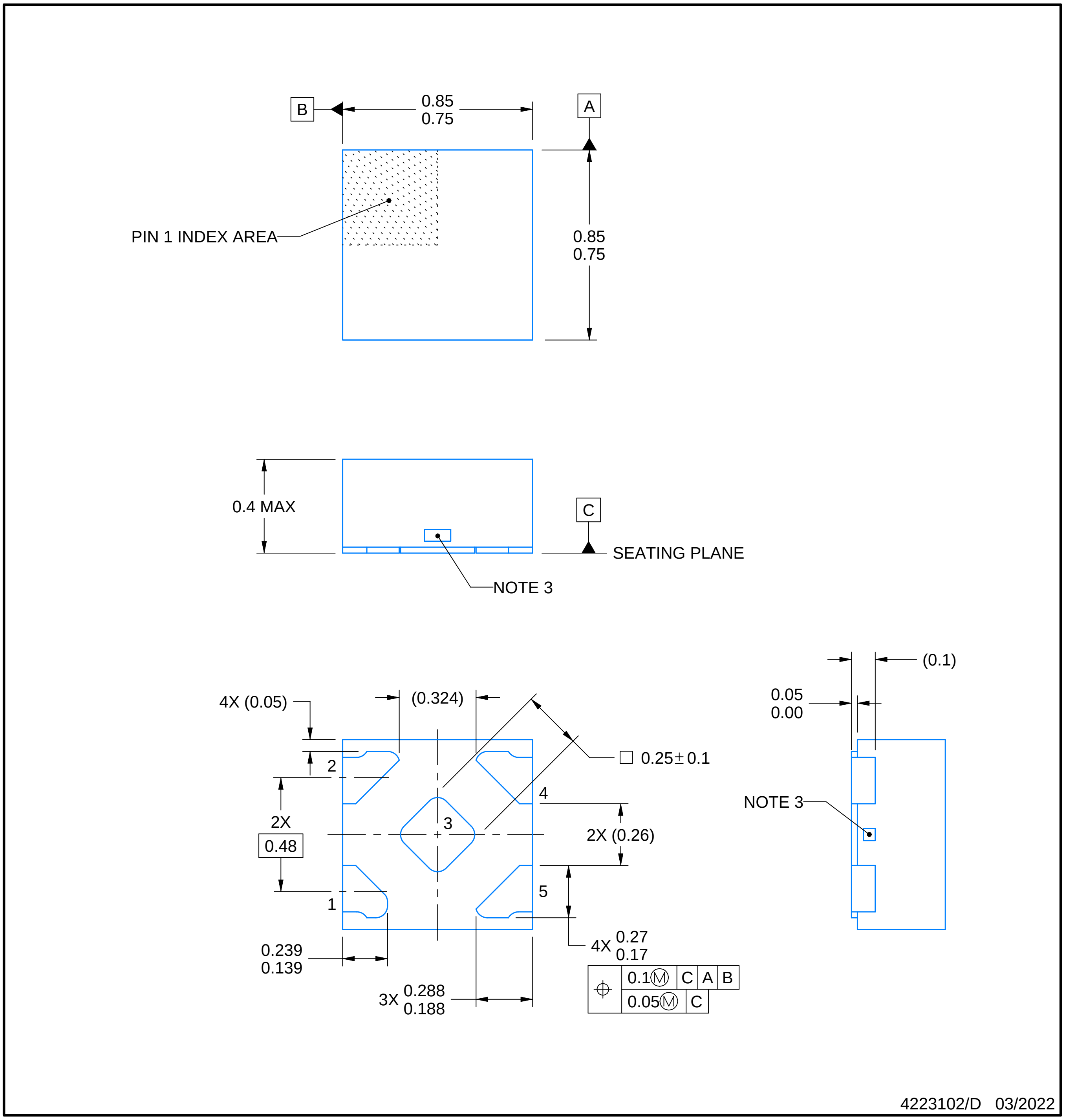
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DPW 5

X2SON - 0.4 mm max height

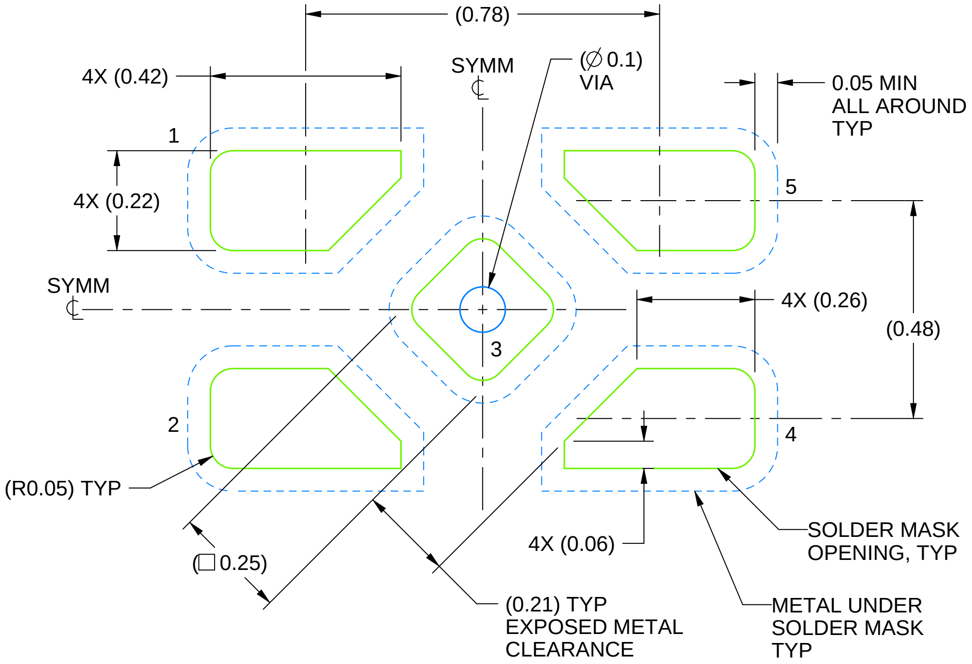
PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



NOTES:

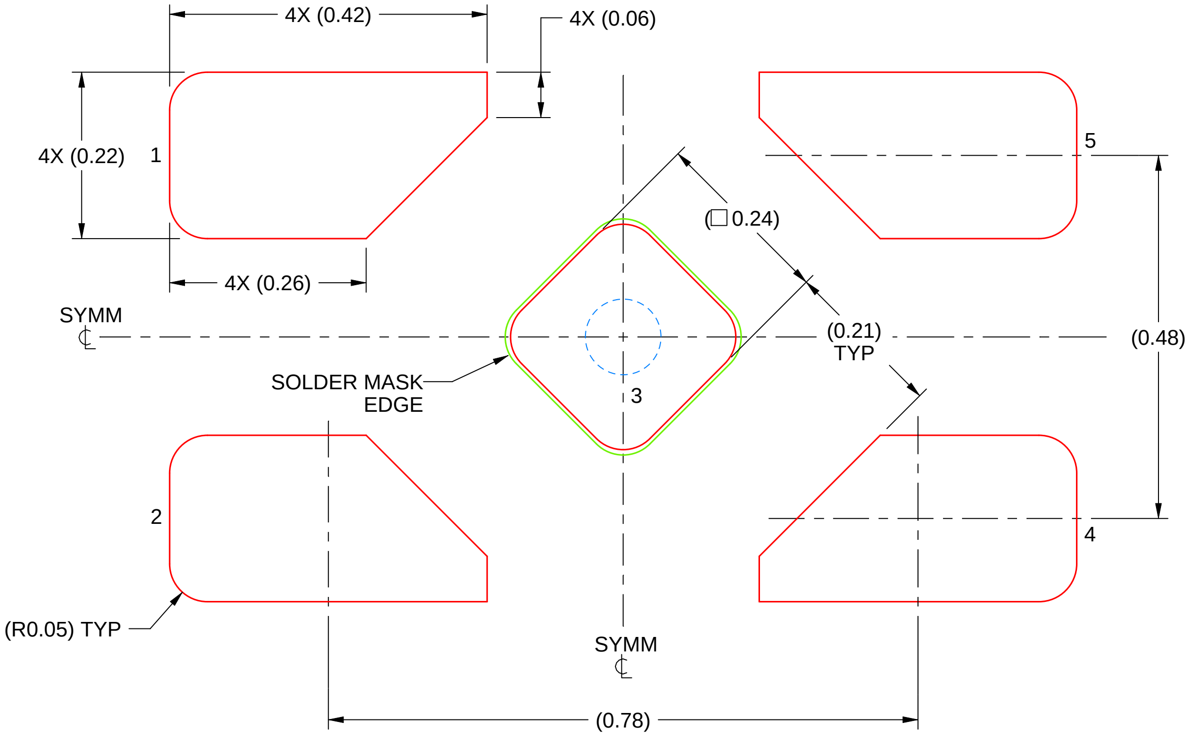
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

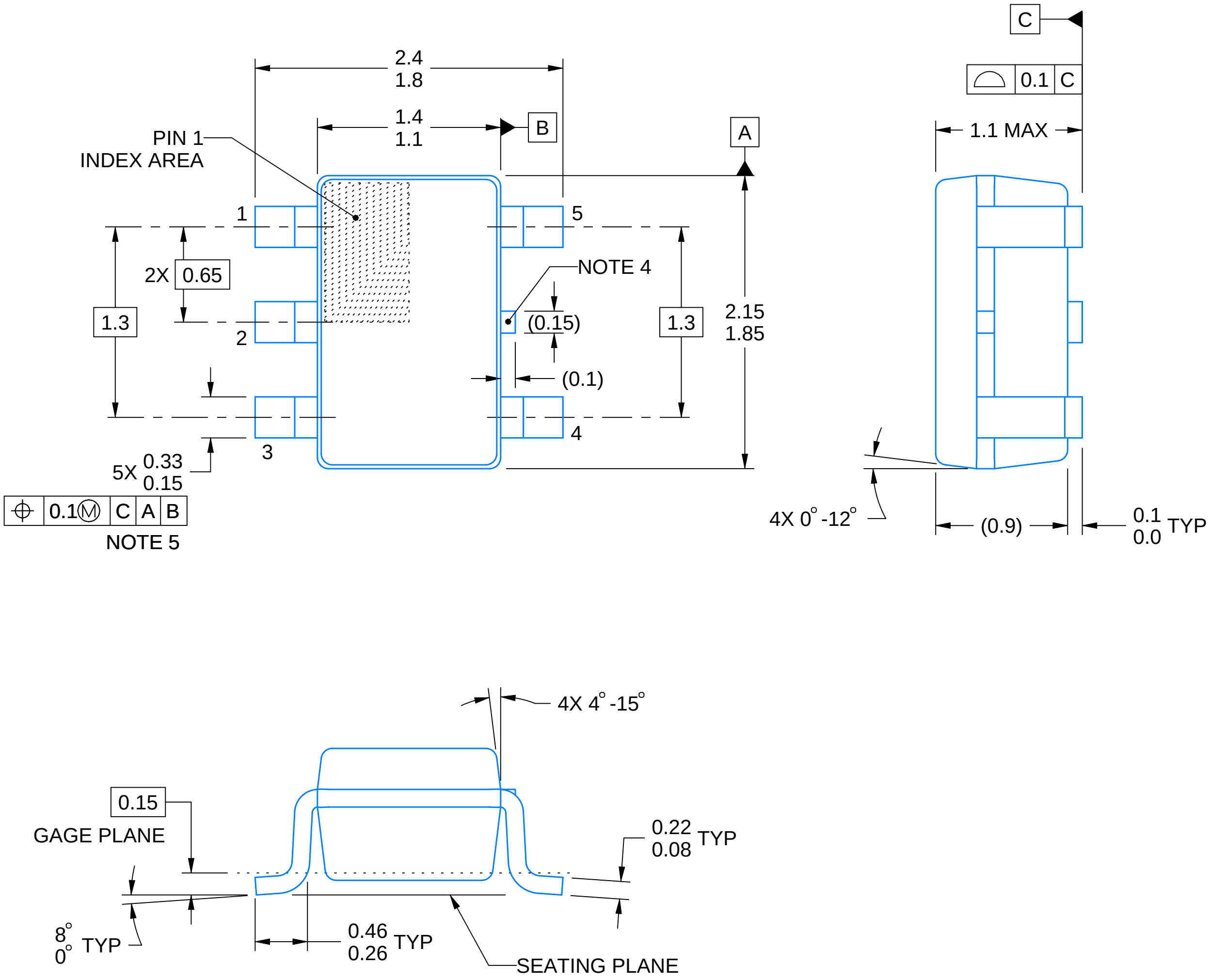


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

NOTES: (continued)

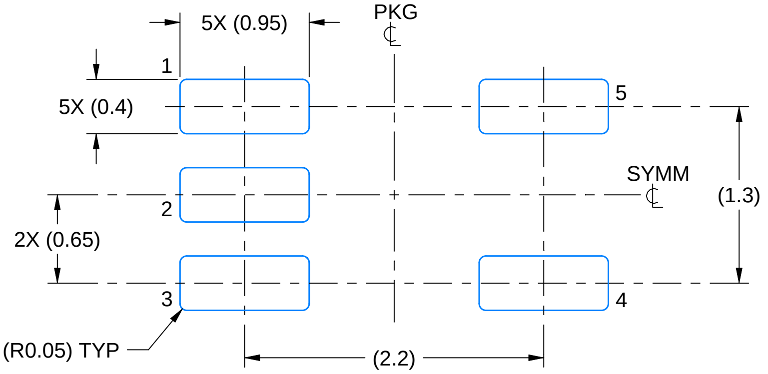
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



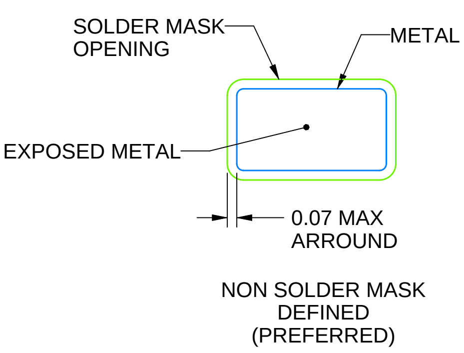
4214834/G 11/2024

NOTES:

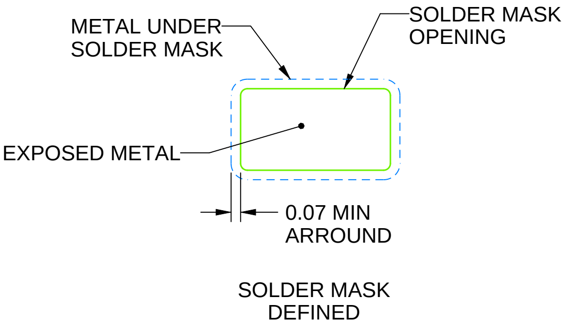
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

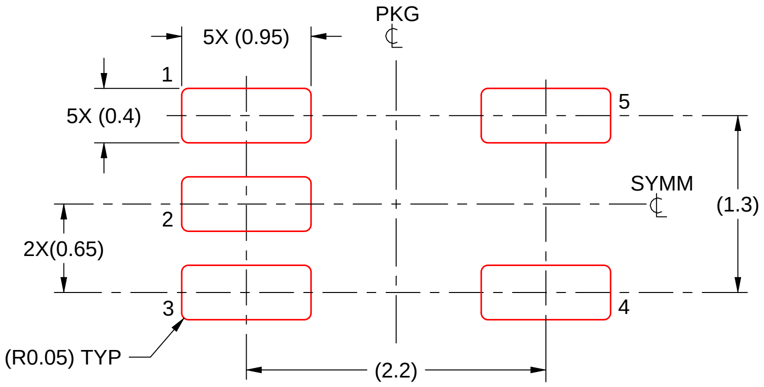


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

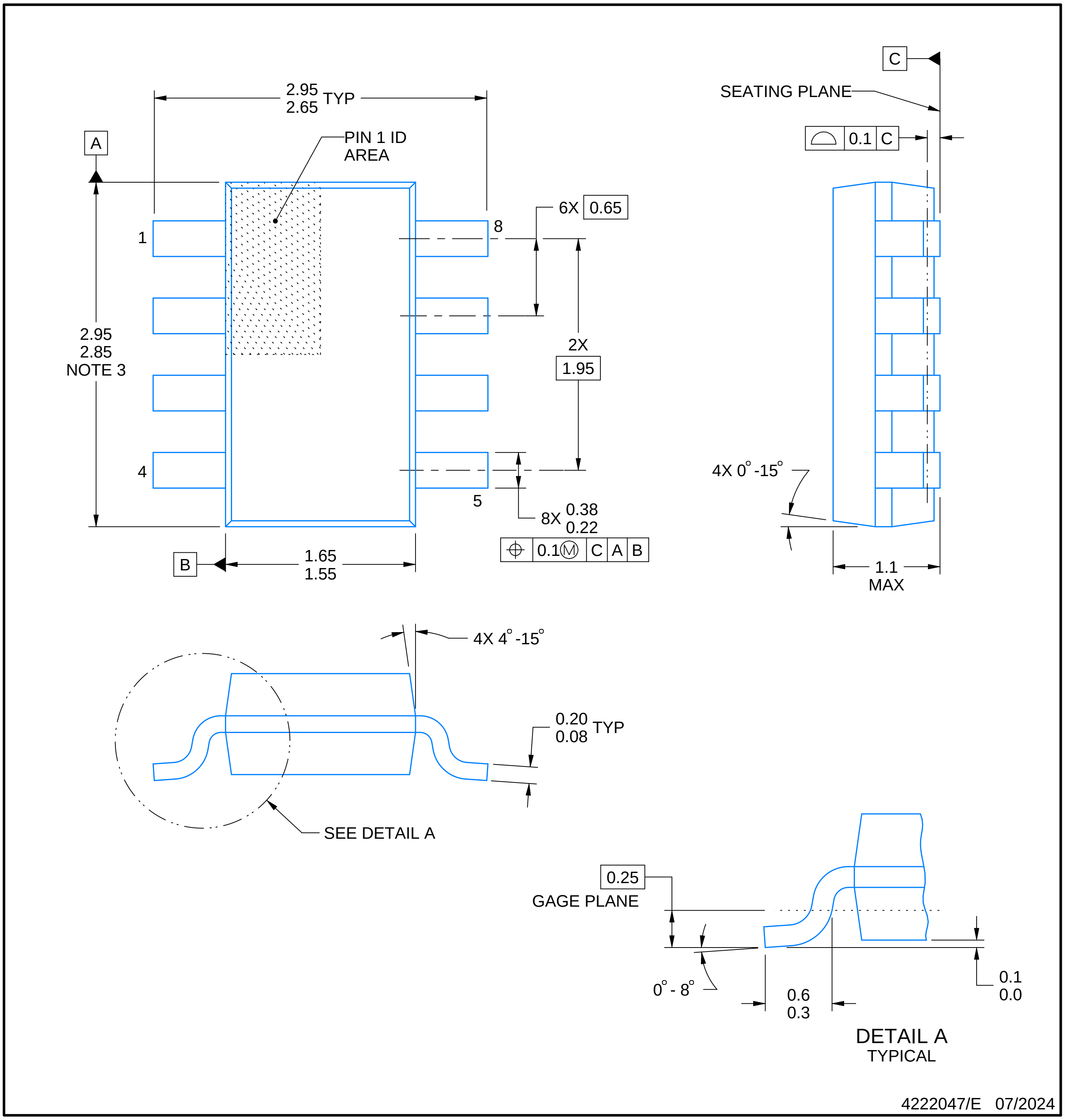
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

SOT-23-THIN - 1.1 mm max height

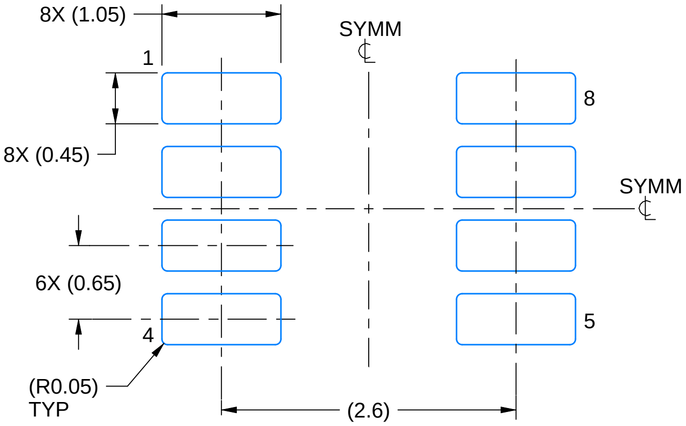
PLASTIC SMALL OUTLINE



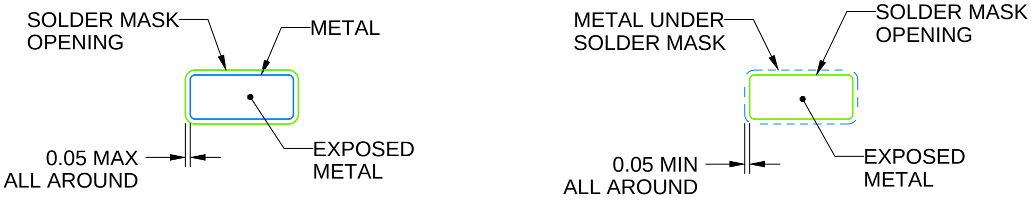
4222047/E 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



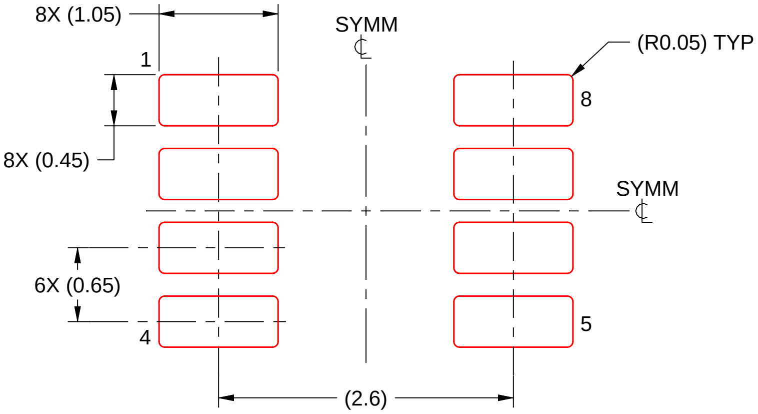
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

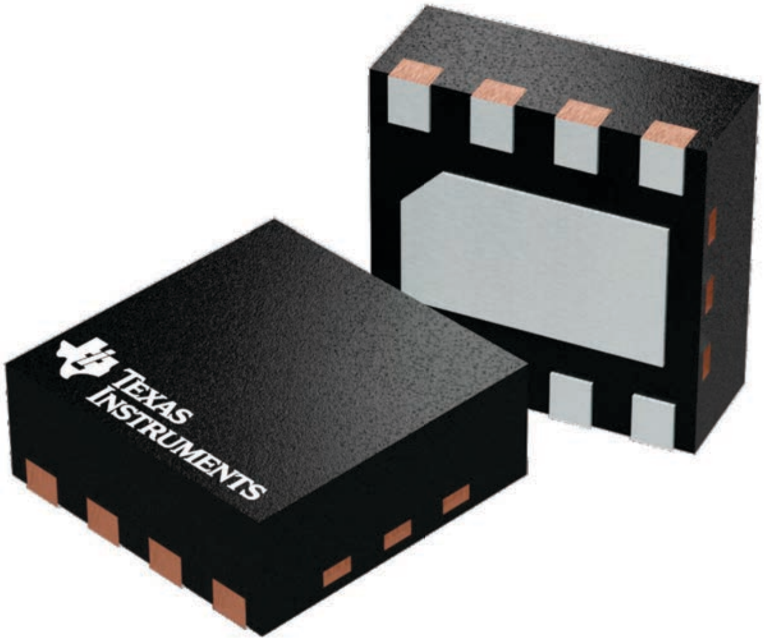
DSG 8

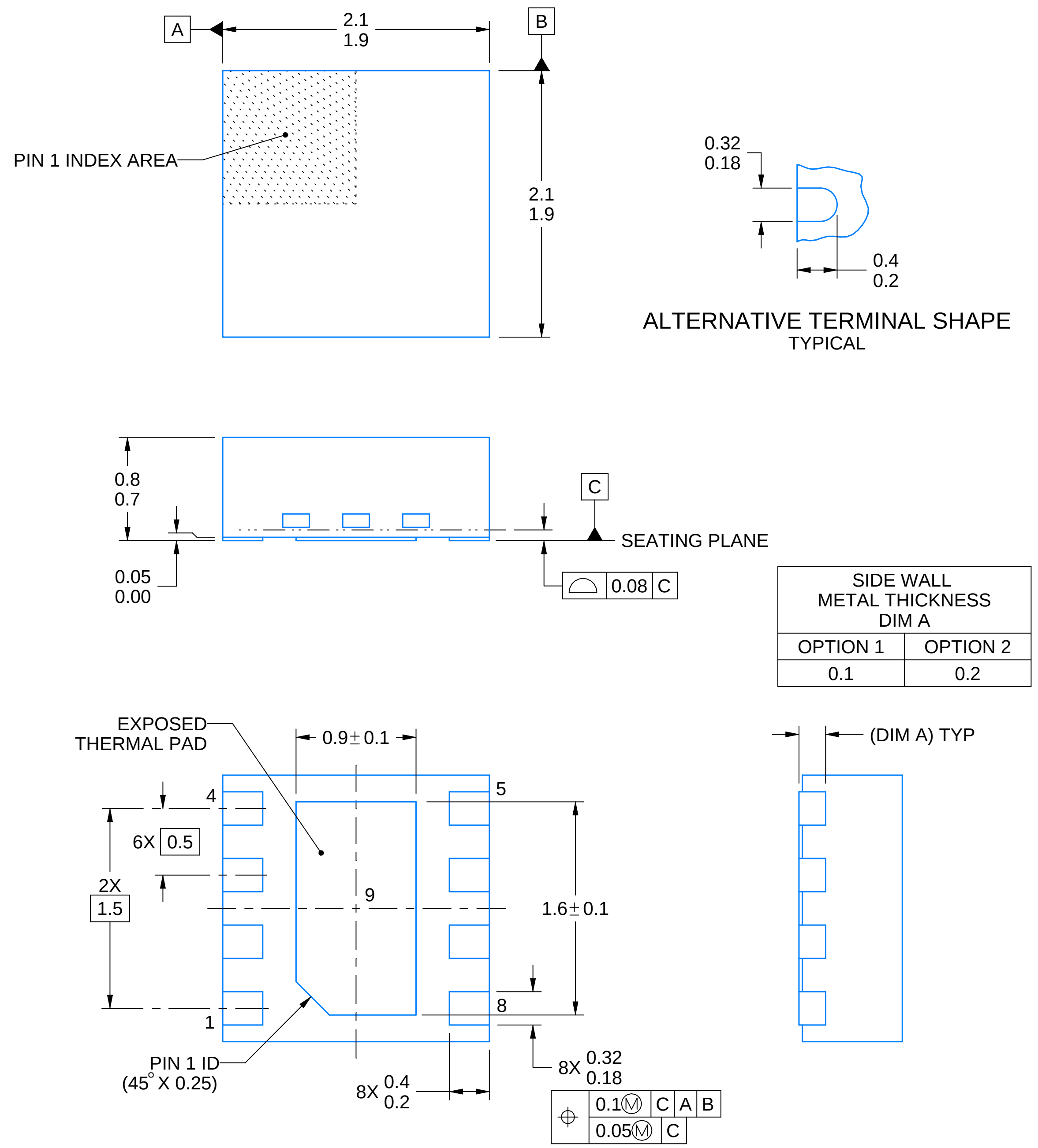
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



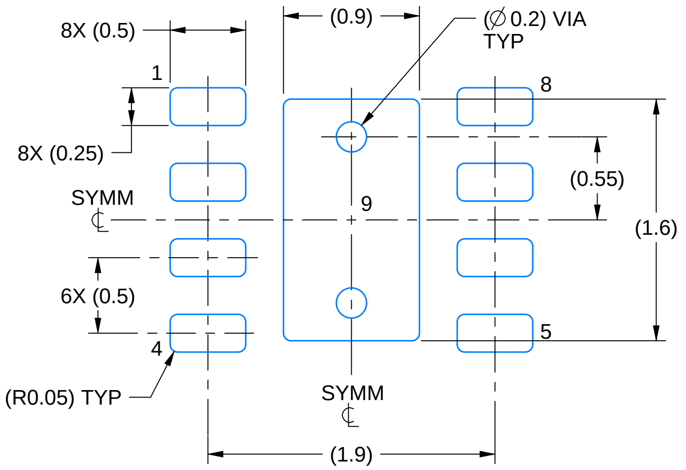


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

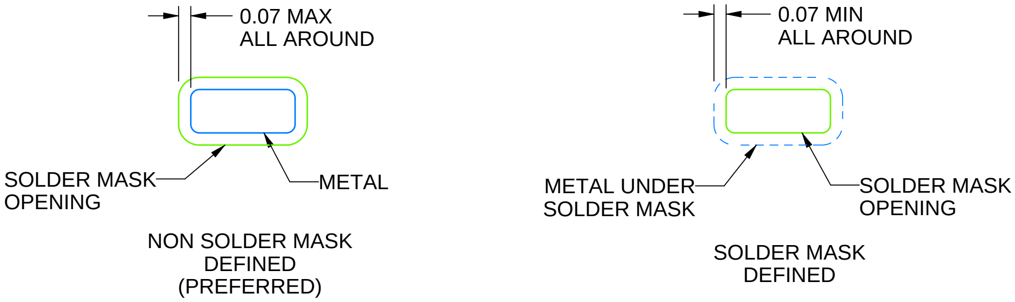
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



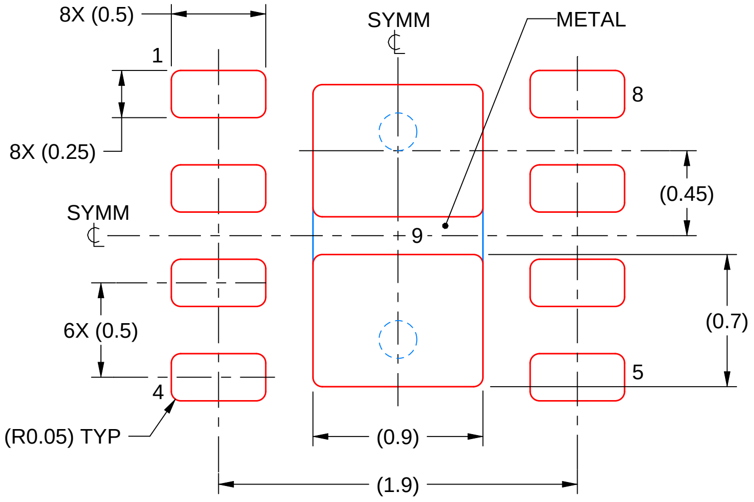
LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明