TLV703x 和 TLV704x 小尺寸、毫微功耗、低电压比较器

1 特性

- 超小型 X2SON、WSON、WQFN 封装
- 1.6V 至 6.5V 的宽电源电压范围
- 315nA 的静态电源电流
- 3µs 低传播延迟
- 轨到轨共模输入电压
- 内部迟滞
- 推挽式输出 (TLV703x)
- 开漏输出 (TLV704x)
- 过驱动输入无相位反转
- “S”和“L”备选引脚排列，具有 1.2V 最小电源电压
- –40°C 至 125°C 工作温度

2 应用

- 手机和平板电脑
- 耳麦/耳机和耳塞
- PC 和笔记本电脑
- 气体检测仪
- 烟雾和热量探测器
- 运动检测器
- 燃气表
- 伺服驱动器位置传感器

3 说明

TLV7031/41（单通道）、TLV7032/42（双通道）和 TLV7034/44（四通道）是低电压、毫微功耗的比较器。这些器件采用超小型无引线封装以及标准的 5 引脚 SC70、SOT-23、VSSOP 和 TSSOP 封装，因此适用于空间受限型设计，例如智能手机、智能仪表和其他便携式或电池供电类应用。

TLV703x 和 TLV704x 提供出色的速度与功耗综合性能，其传播延迟为 3 µ s，静态电源电流为 315nA。得益于毫微功耗下的快速响应优势，功耗敏感型系统能够监测故障状况并快速做出响应。这两款比较器的工作电压范围为 1.6V 至 6.5V，因此可与 3V 和 5V 系统兼容。

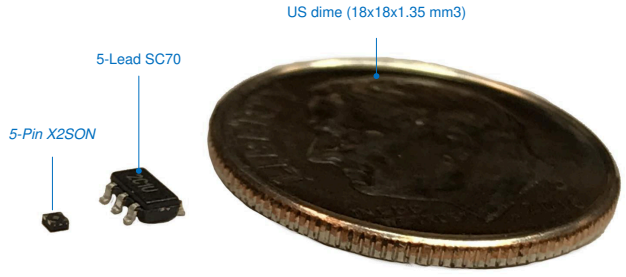
TLV703x 和 TLV704x 凭借过驱输入和内部迟滞特性来确保不会出现输出相位反转，因此工程师可以将此系列的比较器用在必须将慢速输入信号转换为纯净数字输出的严苛、嘈杂环境中进行精密电压监测。

TLV703x 具有推挽式输出级，能够灌/拉毫安级电流，同时可对 LED 进行控制或驱动容性负载。TLV704x 具有可上拉到 V_{CC} 之上的开漏输出级，使此器件适用于电平转换器和双极至单端转换器。“S”和“L”选项是具有 1.2V 最低电源电压的备选单通道引脚排列。

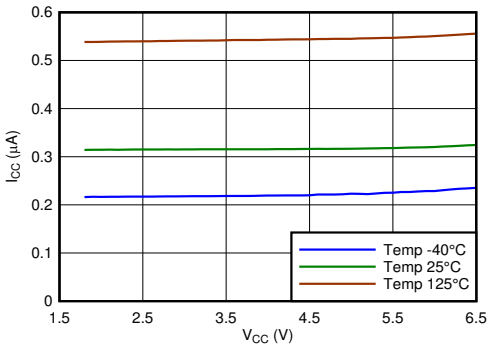
器件信息

器件型号	封装（引脚）(1)	本体尺寸（标称值）(2)
TLV7031、TLV7041	SOT-23 (5)	2.90mm × 1.60mm
	SC70 (5)	2.00mm × 1.25mm
	X2SON (5)	0.80mm × 0.80mm
TLV7031L、TLV7041L	SOT-23 (5)	2.90mm × 1.60mm
TLV7031S、TLV7041S	SC70 (5)	2.00mm × 1.25mm
	SOT-23 (5)	2.90mm × 1.60mm
TLV7032、TLV7042	VSSOP (8)	3.00mm x 3.00mm
	SOT-23 (8)	2.90mm x 1.60mm
	WSON (8)	2.00mm x 2.00mm
TLV7034、TLV7044	WQFN (16)	3.00mm x 3.00mm
	TSSOP (14)	4.40mm x 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



X2SON 封装与 SC70 和美元硬币对比



I_{CC} 与电源电压间的关系（双通道）

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

4.1 Pin Functions: TLV7031/41 Singles including "S" and "L" options

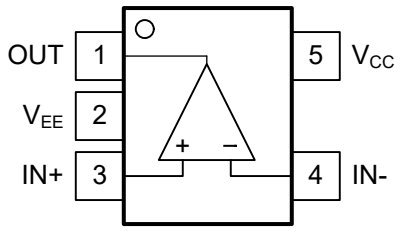


图 4-1.
TLV70x1
"North West" Pinout
DBV, DCK, Packages,
SOT-23-5, SC-70-5
Top View

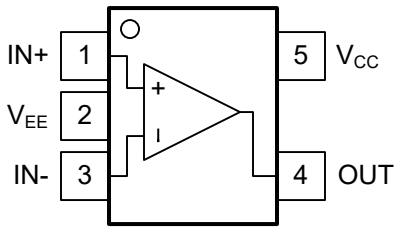


图 4-2.
TLV70x1S
"South East" Pinout
DBV, DCK Packages,
SOT-23-5, SC-70-5
Top View

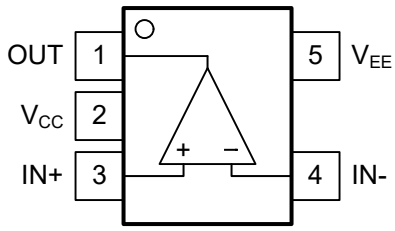


图 4-3.
TLV70x1L(2)
"TLV/LMC72xx type" Pinout
with reversed supplies
DBV Package,
SOT-23-5
Top View

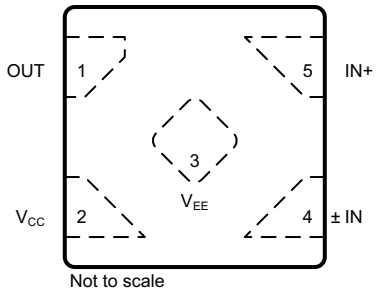


图 4-4.
TLV70x1
5-Pin X2SON
Top View

表 4-1. Pin Functions

NAME	TLV7031, TLV7041		TLV7031S, TLV7041S	TLV7031L, TLV7041L(2)	I/O(1)	DESCRIPTION
	PINS		PINS	PINS		
	SOT-23, SC-70	X2SON(3)	SOT-23, SC-70	SOT-23		
OUT	1	1	4	1	O	Output
V-	2	3	2	5	-	Negative Supply Voltage
IN+	3	5	1	3	I	Non-Inverting (+) Input
IN-	4	4	3	4	I	Inverting (-) Input
V+	5	2	5	2	-	Positive Supply Voltage

(1) I = Input, O = Output
(2) The "L" pinout option is provided to replace the LMC72xx and TLV7211 in legacy designs and is not inteded for new designs. The TLV70x1 or TLV70x1S is recommeded for new designs.
(3) The application report *Designing and Manufacturing With TI's X2SON Packages* (SCEA055) provides more details to optimize PCB designs.

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4.2 Pin Functions: TLV7032/42 Dual

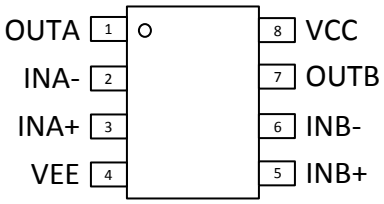
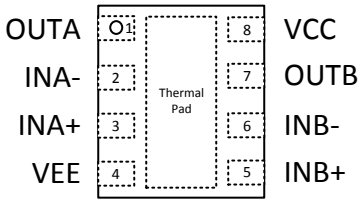


图 4-5.
TLV7032/42
DGK, DDF Packages
8-Pin VSSOP, SOT-23
Top View



A. Connect thermal pad directly to V – pad.

图 4-6.
TLV7032/42
DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View

表 4-2. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
INA –	2	I	Inverting input, channel A
INA+	3	I	Noninverting input, channel A
INB –	6	I	Inverting input, channel B
INB+	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
VEE	4	—	Negative (lowest) supply or ground (for single-supply operation)
VCC	8	—	Positive (highest) supply

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4.3 Pin Functions: TLV7034/44 Quad

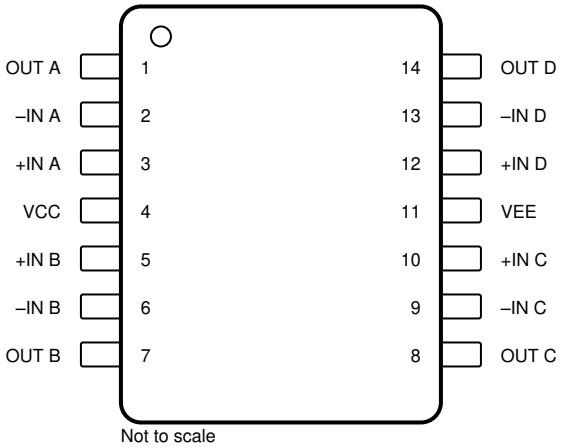
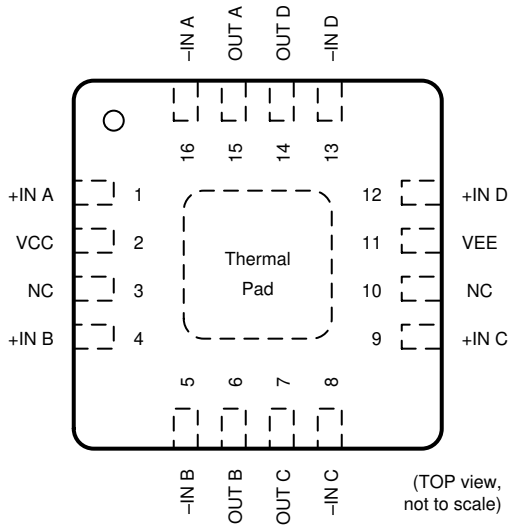


图 4-7.
TLV7034/44
PW Packages
14-Pin TSSOP
Top View



A. Connect thermal pad to V – .

图 4-8.
TLV7034/44
RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View

表 4-3. Pin Functions

PIN			I/O	DESCRIPTION
NAME	TSSOP	WQFN		
– IN1 A	2	16	I	Inverting input, channel A
+IN A	3	1	I	Noninverting input, channel A
– IN B	6	5	I	Inverting input, channel B
+IN B	5	4	I	Noninverting input, channel B
– IN C	9	8	I	Inverting input, channel C
+IN C	10	9	I	Noninverting input, channel C
– IN D	13	13	I	Inverting input, channel D
+IN D	12	12	I	Noninverting input, channel D
NC	—	3, 10	—	No internal connection
OUT A	1	15	O	Output, channel A
OUT B	7	6	O	Output, channel B
OUT C	8	7	O	Output, channel C
OUT D	14	14	O	Output, channel D
VEE	11	11	—	Negative (lowest) supply or ground (for single-supply operation)
VCC	4	2	—	Positive (highest) supply

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} - V_{EE}$	–0.3	7	V
Input pins (IN+, IN-)(2)	V_{EE} – 0.3	7	V
Current into Input pins (IN+, IN-)		±10	mA
Output (OUT) (TLV703x)(3)	V_{EE} – 0.3	V_{CC} + 0.3	V
Output (OUT) (TLV704x)	V_{EE} – 0.3	7	V
Output short-circuit duration(4)		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Input terminals are diode-clamped to V_{EE}. Input signals that can swing 0.3V below V_{EE} must be current-limited to 10mA or less
(3) Output maximum is (V_{CC} + 0.3V) or 7V, whichever is less.
(4) Short-circuit to ground, one comparator per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} - V_{EE}$	1.6	6.5	V
Supply voltage $V_S = V_{CC} - V_{EE}$, TLV70x1L and TLV70x1S only	1.2	6.5	V
Input voltage range	V_{EE} – 0.1	V_{CC} + 0.1	V
Ambient temperature, T_A	–40	125	°C

5.4 Thermal Information (Single)

THERMAL METRIC(1)		TLV7031/TLV7041 (Including L and S)			UNIT
		DPW (X2SON)	DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	533.2	297.2	278.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	302.7	224.7	186.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	408.3	200.1	113.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	71.5	141.2	82.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	405.9	198.9	112.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	188.3	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.5 Thermal Information (Dual)

THERMAL METRIC[1]		TLV7032/TLV7042			UNIT
		DGK (VSSOP)	DDF (SOT-23)	DSG (WSON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	211.7	212.5	106.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	127.3	127.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	133.5	129.2	72.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	28.3	25.8	16.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	131.7	129.0	72.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	47.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Thermal Information (Quad)

THERMAL METRIC[1]		TLV7034/44		UNIT
		RTE (QFN)	PW (TSSOP)	
		16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.4	131.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.2	60.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.5	74.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.6	12.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.5	73.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	24.1	n/a	°C/W

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5.7 Electrical Characteristics (Single)

V_S = 1.8V to 5V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8V and 5V, V_{CM} = VS / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8V and 5V, V_{CM} = VS / 2, T_A = 25°C	2	7	17	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (for TLV7031 only)	V_S = 5V, V_{EE} = 0V, I_O = 3mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5V, V_{EE} = 0V, I_O = 3mA		250	350	mV
I_{LKG}	Open-drain output leakage current (TLV7041 only)	V_S = 5V, V_{ID} = +0.1V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8V to 5V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	VS = 5V, sourcing		29		mA
		VS = 5V, sinking		33		
I_{CC}	Supply current	V_S = 1.8V, no load, V_{ID} = –0.1V (Output Low)		335	900	nA

5.8 Switching Characteristics (Single)

Typical values are at T_A = 25°C, V_S = 5V, V_{CM} = V_S / 2; CL = 15pF, input overdrive = 100mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 2.5kΩ TLV7041 only)	Midpoint of input to midpoint of output, V_{OD} = 100mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 2.5kΩ TLV7041 only)	Midpoint of input to midpoint of output, V_{OD} = 100mV		3		µs
t_R	Rise time (TLV7031 only)	Measured from 10% to 90%		4.5		ns
t_F	Fall time	Measured from 10% to 90%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for 200 µs before the output reflects the input.		200		µs

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5.9 Electrical Characteristics (Dual)

V_S = 1.8V to 5V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8V and 5V, V_{CM} = VS / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8V and 5V, V_{CM} = VS / 2	3	10	25	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (for TLV7032 only)	V_S = 5V, V_{EE} = 0V, I_O = 3mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5V, V_{EE} = 0V, I_O = 3mA		250	350	mV
I_{LKG}	Open-drain output leakage current (TLV7042 only)	V_S = 5V, V_{ID} = +0.1V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8V to 5V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	VS = 5V, sourcing (for TLV7032 only)		29		mA
		VS = 5V, sinking		33		
I_{CC}	Supply current / Channel	V_S = 1.8V, no load, V_{ID} = –0.1V (Output Low)		315	750	nA

5.10 Switching Characteristics (Dual)

Typical values are at T_A = 25°C, V_S = 5V, V_{CM} = V_S / 2; CL = 15pF, input overdrive = 100mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99kΩ TLV7042 only) (1)	Midpoint of input to midpoint of output, V_{OD} = 100mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 4.99kΩ TLV7042 only) (1)	Midpoint of input to midpoint of output, V_{OD} = 100mV		3		µs
t_R	Rise time (TLV7032 only)	Measured from 20% to 80%		4.5		ns
t_F	Fall time	Measured from 20% to 80%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for t_{ON} before the output reflects the input.		200		µs

(1) The lower limit for RP is 650Ω

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5.11 Electrical Characteristics (Quad)

V_S = 1.8V to 5V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8V and 5V, V_{CM} = VS / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8V and 5V, V_{CM} = VS / 2	3	10	25	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (for TLV7034 only)	V_S = 5V, V_{EE} = 0V, I_O = 3mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5V, V_{EE} = 0V, I_O = 3mA		250	350	mV
I_{LKG}	Open-drain output leakage current (TLV7044 only)	V_S = 5V, V_{ID} = +0.1V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8V to 5V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	VS = 5V, sourcing (for TLV7034 only)		29		mA
		VS = 5V, sinking		33		
I_{CC}	Supply current / Channel	V_S = 1.8V, no load, V_{ID} = –0.1V (Output Low)		315	750	nA

5.12 Switching Characteristics (Quad)

Typical values are at T_A = 25°C, V_S = 5V, V_{CM} = V_S / 2; CL = 15pF, input overdrive = 100mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99kΩ TLV7044 only) (1)	Midpoint of input to midpoint of output, V_{OD} = 100mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 4.99kΩ TLV7044 only) (1)	Midpoint of input to midpoint of output, V_{OD} = 100mV		3		µs
t_R	Rise time (TLV7034 only)	Measured from 20% to 80%		4.5		ns
t_F	Fall time	Measured from 20% to 80%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for t_{ON} before the output reflects the input..		400		µs

(1) The lower limit for RP is 650Ω

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5.13 Timing Diagrams

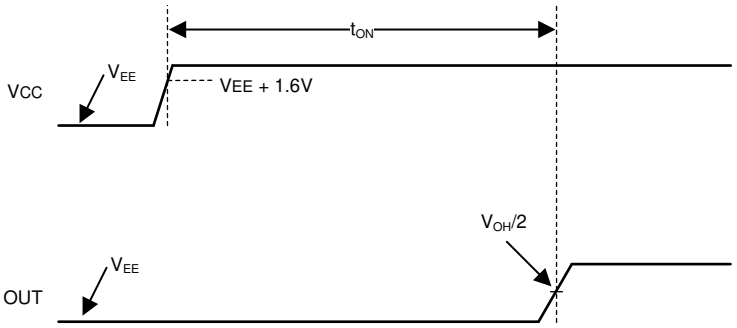


图 5-1. Start-Up Time Timing Diagram (IN+ > IN –)

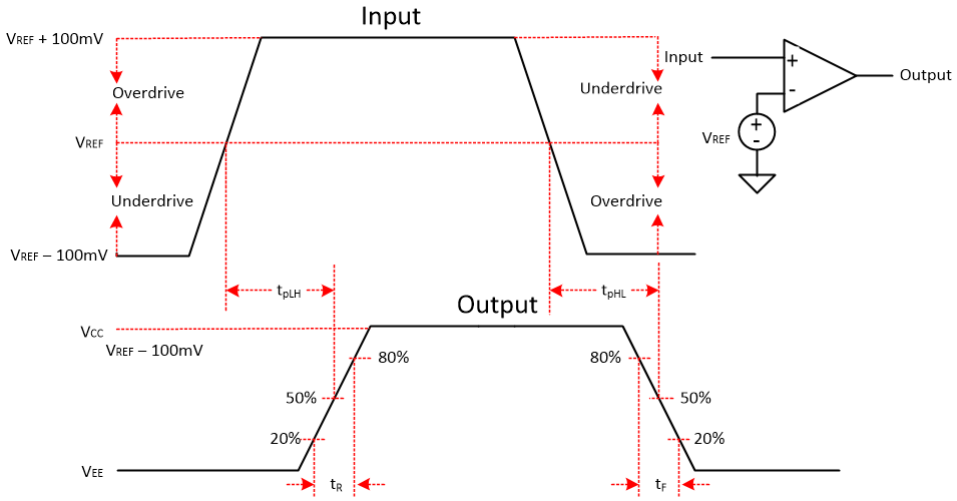


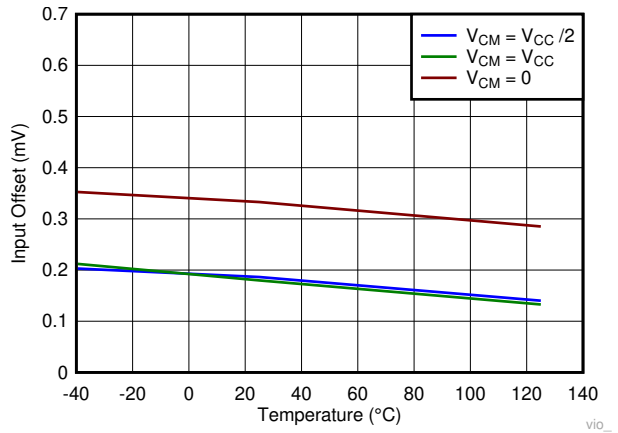
图 5-2. Propagation Delay Timing Diagram

备注

The propagation delays t_{pLH} and t_{pHL} include the contribution of input offset and hysteresis.

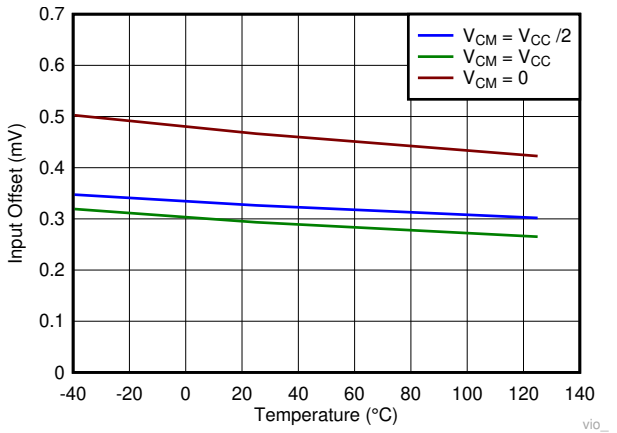
5.14 Typical Characteristics

T_A = 25°C, V_{CC} = 5V, V_{EE} = 0V, V_{CM} = V_{CC}/2, C_L = 15pF



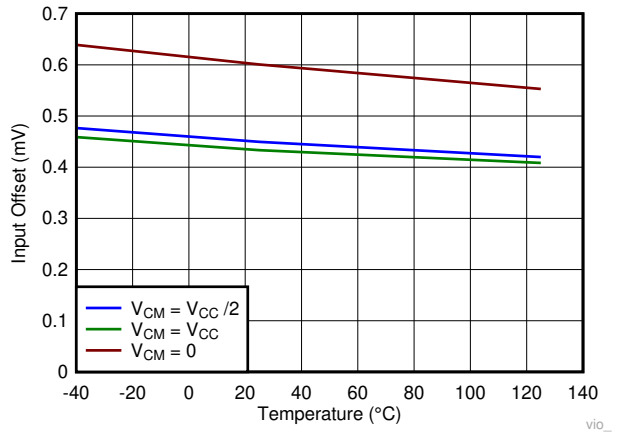
V_{CC} = 1.8V

图 5-3. Input Offset vs Temperature



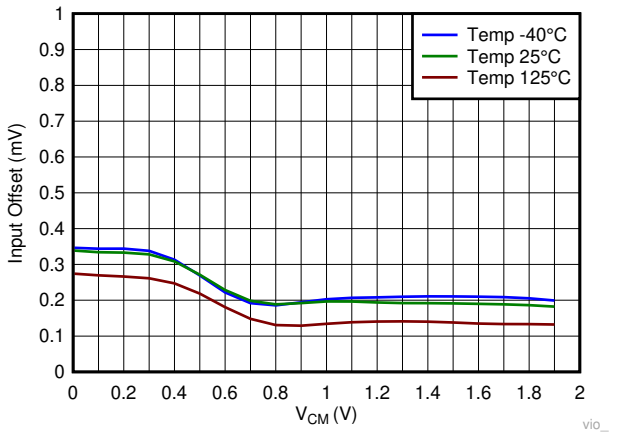
V_{CC} = 3.3V

图 5-4. Input Offset vs Temperature



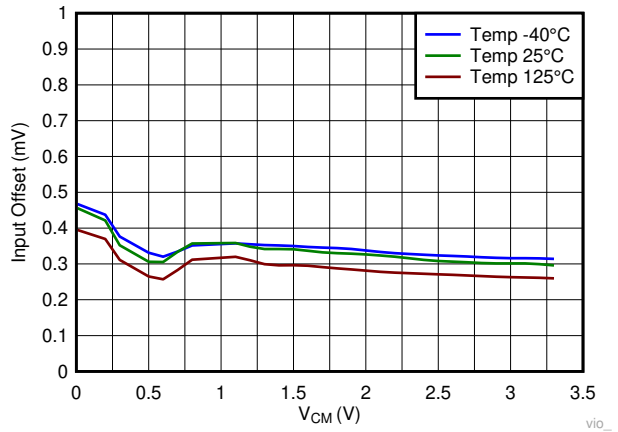
V_{CC} = 5V

图 5-5. Input Offset vs Temperature



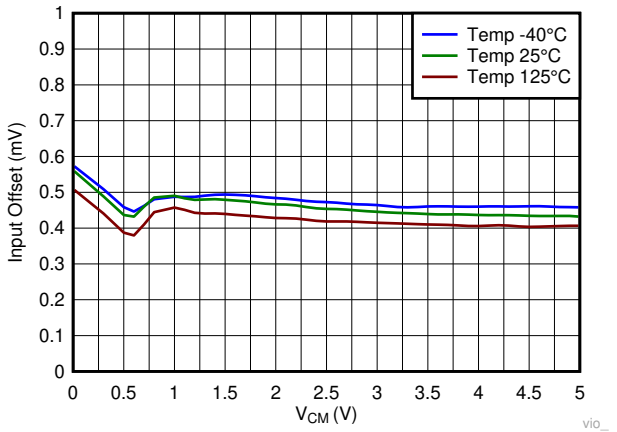
V_{CC} = 1.8V

图 5-6. Input Offset Voltage vs V_{CM}



V_{CC} = 3.3V

图 5-7. Input Offset Voltage vs V_{CM}



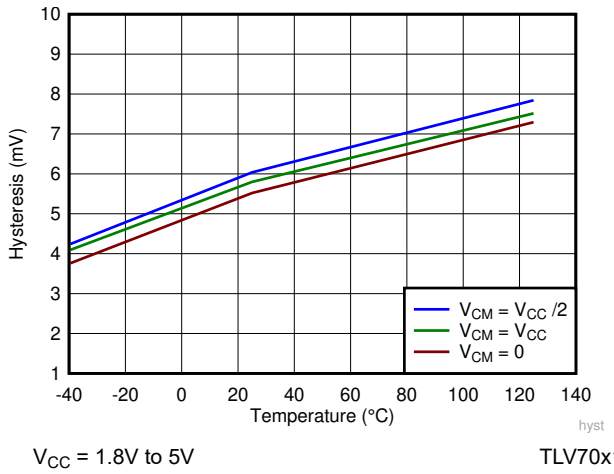
V_{CC} = 5V

图 5-8. Input Offset Voltage vs V_{CM}

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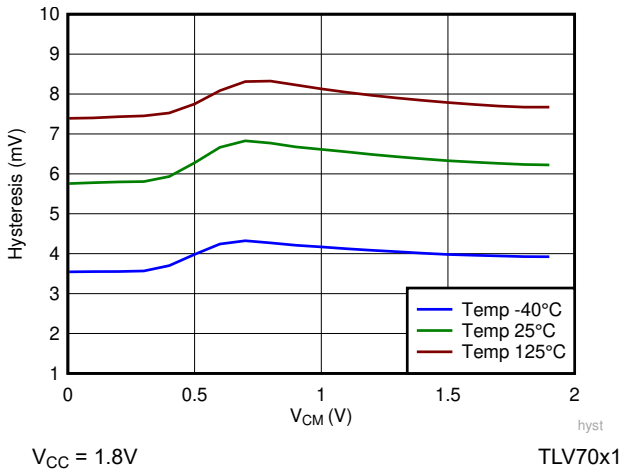
5.14 Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5V, V_{EE} = 0V, V_{CM} = V_{CC}/2, C_L = 15pF



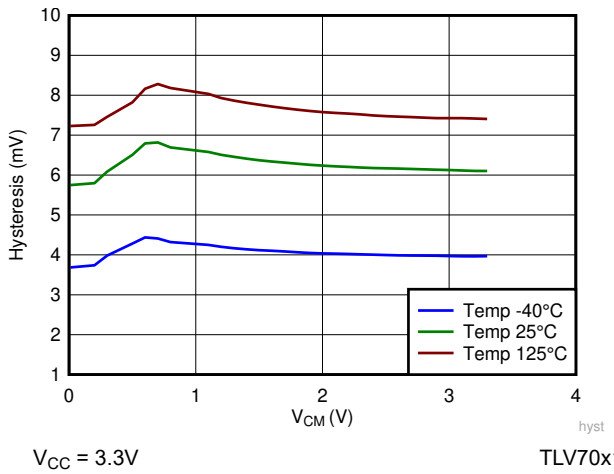
V_{CC} = 1.8V to 5V TLV70x1

图 5-9. Hysteresis vs Temperature



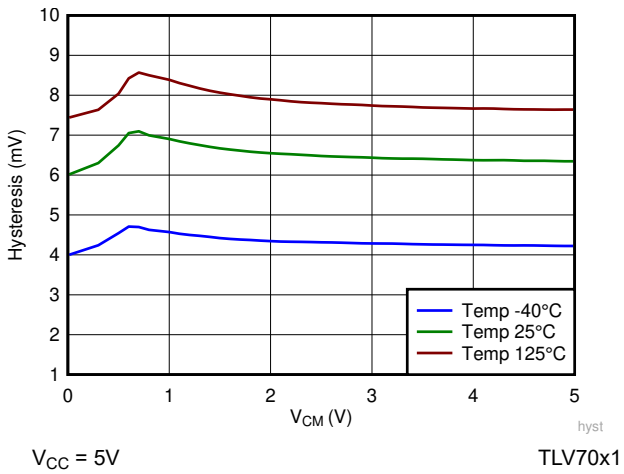
V_{CC} = 1.8V TLV70x1

图 5-10. Hysteresis vs V_{CM}



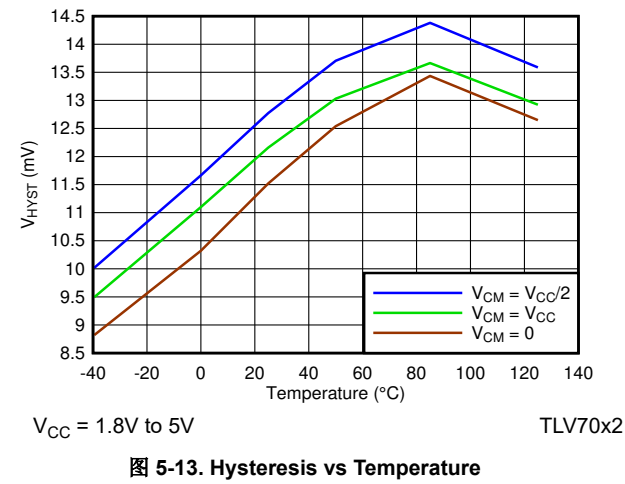
V_{CC} = 3.3V TLV70x1

图 5-11. Hysteresis vs V_{CM}



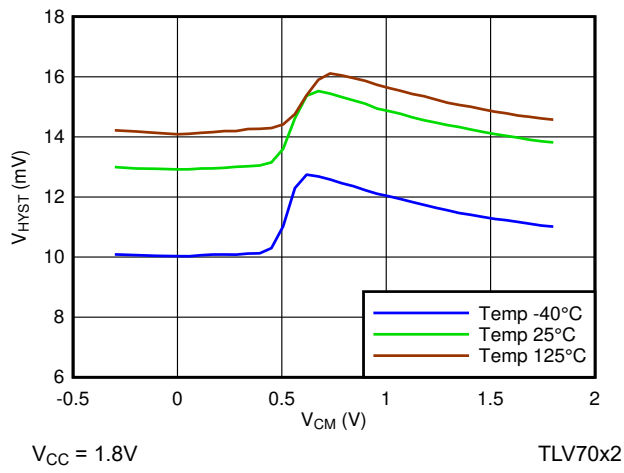
V_{CC} = 5V TLV70x1

图 5-12. Hysteresis vs V_{CM}



V_{CC} = 1.8V to 5V TLV70x2

图 5-13. Hysteresis vs Temperature



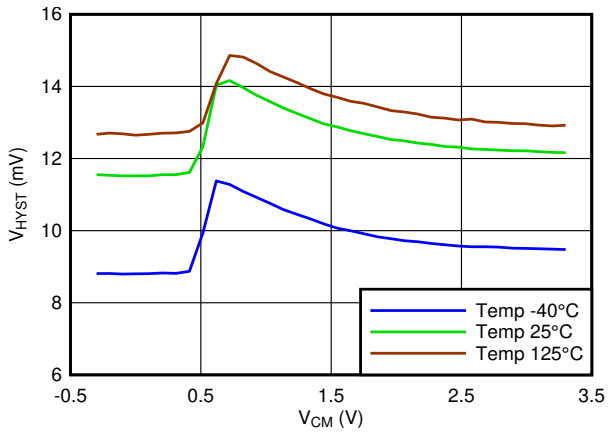
V_{CC} = 1.8V TLV70x2

图 5-14. Hysteresis vs V_{CM}

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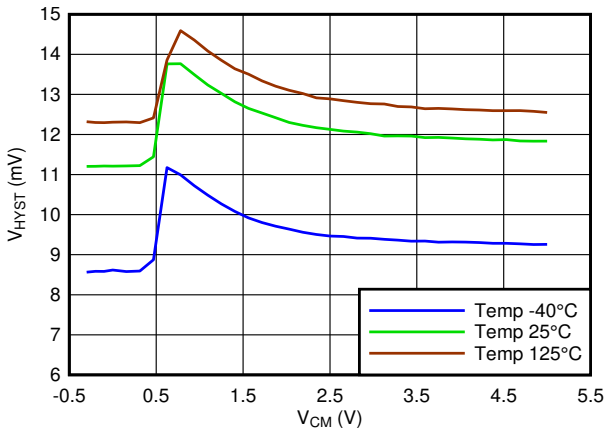
5.14 Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5V, V_{EE} = 0V, V_{CM} = V_{CC}/2, C_L = 15pF



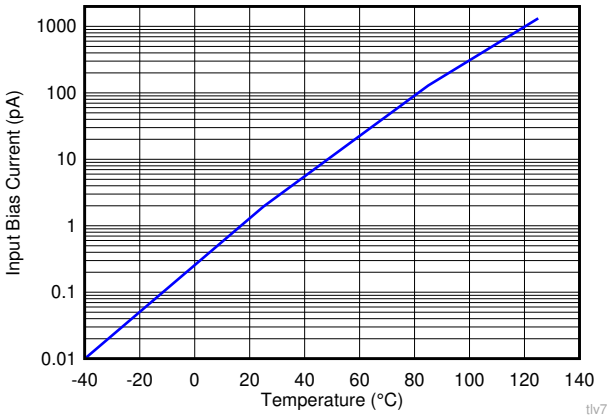
V_{CC} = 3.3V TLV70x2

图 5-15. Hysteresis vs V_{CM}



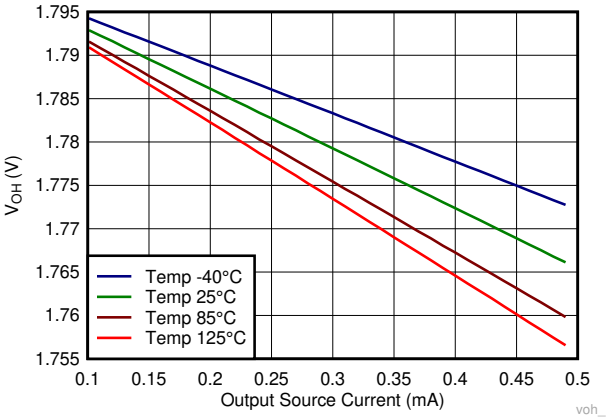
V_{CC} = 5V TLV70x2

图 5-16. Hysteresis vs V_{CM}



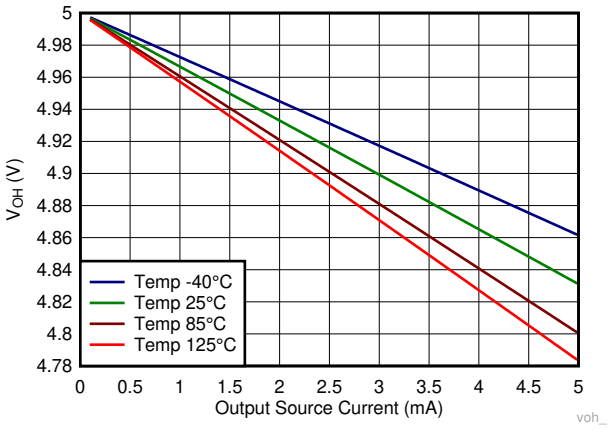
A. V_{CC} = 5V

图 5-17. Input Bias Current vs Temperature



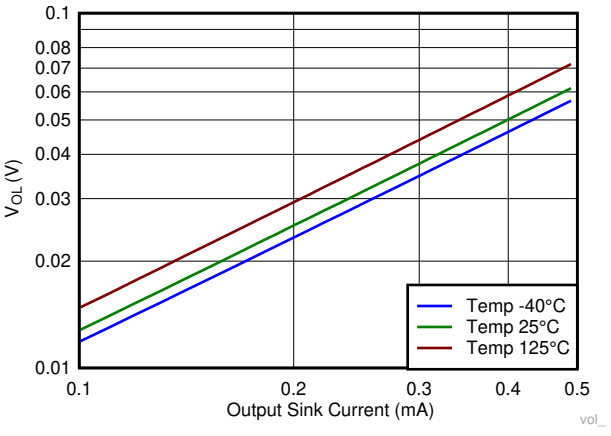
V_{CC} = 1.8V TLV703x

图 5-18. Output Voltage High vs Output Source Current



V_{CC} = 5V TLV703x

图 5-19. Output Voltage High vs Output Source Current



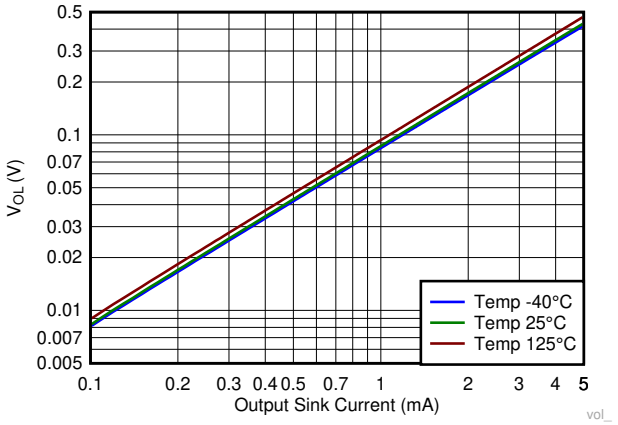
V_{CC} = 1.8V

图 5-20. Output Voltage Low vs Output Sink Current

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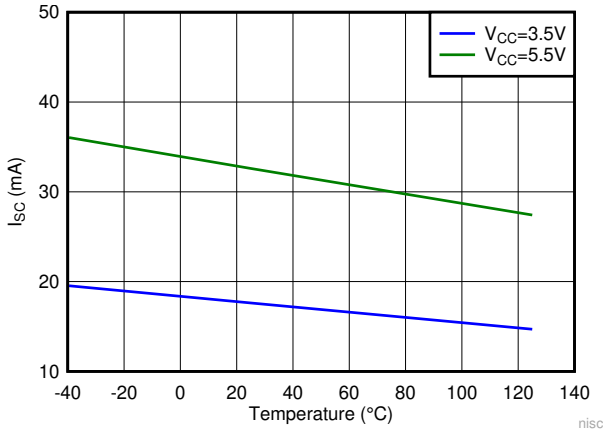
5.14 Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5V, V_{EE} = 0V, V_{CM} = V_{CC}/2, C_L = 15pF



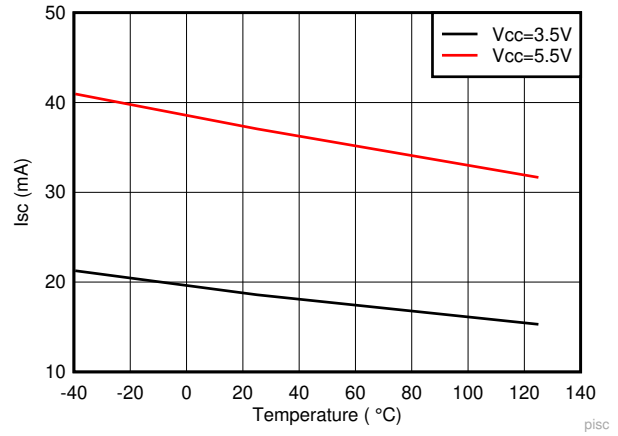
V_{CC} = 5V

图 5-21. Output Voltage Low vs Output Sink Current



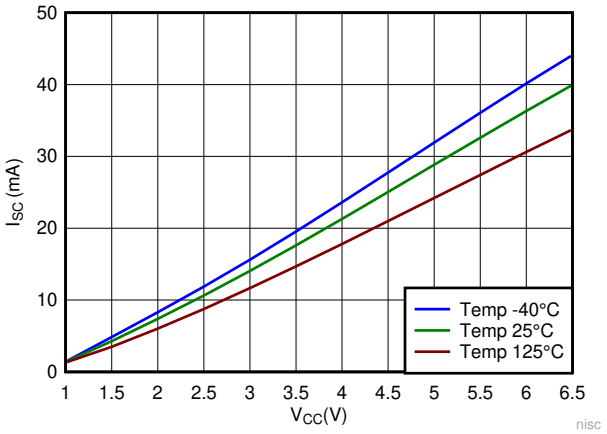
V_{CM} = V_{CC} / 2

图 5-22. Output Short-Circuit (Sink) Current vs Temperature



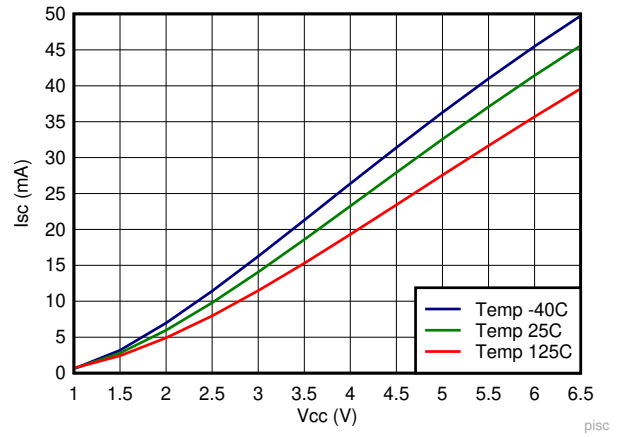
V_{CM} = V_{CC} / 2 TLV703x

图 5-23. Output Short-Circuit (Source) Current vs Temperature



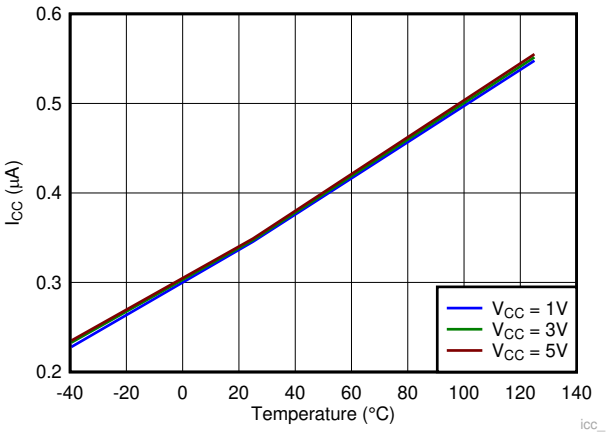
V_{CM} = V_{CC} / 2

图 5-24. Output Short Circuit (Sink) vs V_{CC}



V_{CM} = V_{CC} / 2 TLV703x

图 5-25. Output Short Circuit (Source) vs V_{CC}



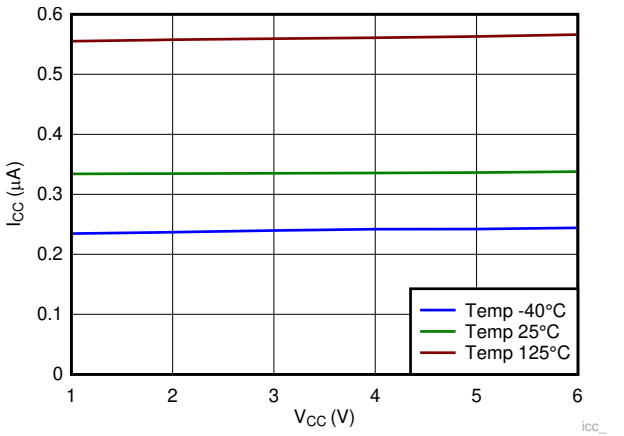
V_{CM} = V_{CC} / 2 TLV70x1

图 5-26. I_{CC} vs Temperature

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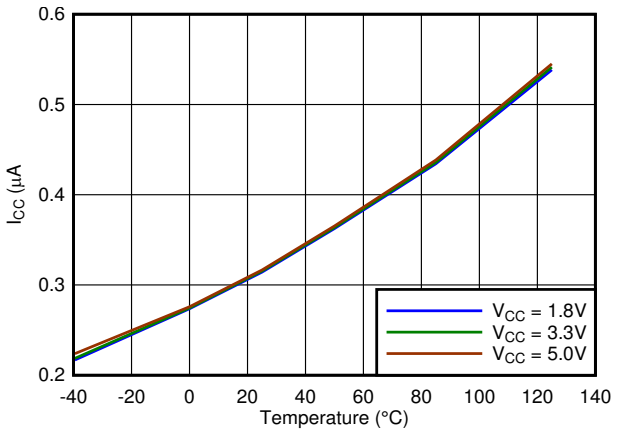
5.14 Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5V, V_{EE} = 0V, V_{CM} = V_{CC}/2, C_L = 15pF



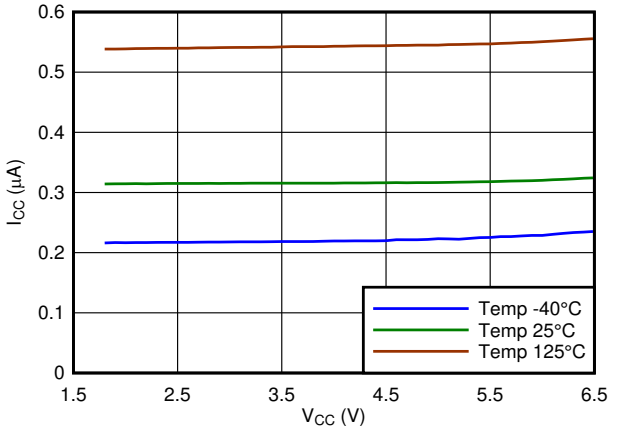
V_{CM} = V_{CC} / 2 TLV70x1

图 5-27. I_{CC} vs V_{CC}



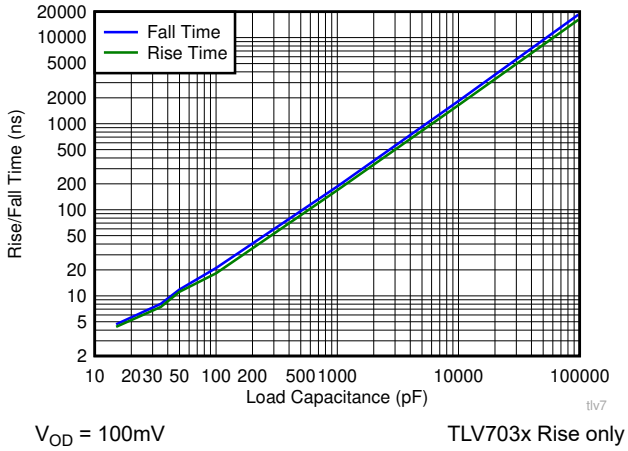
V_{CM} = V_{CC} / 2 TLV70x2

图 5-28. I_{CC} vs Temperature



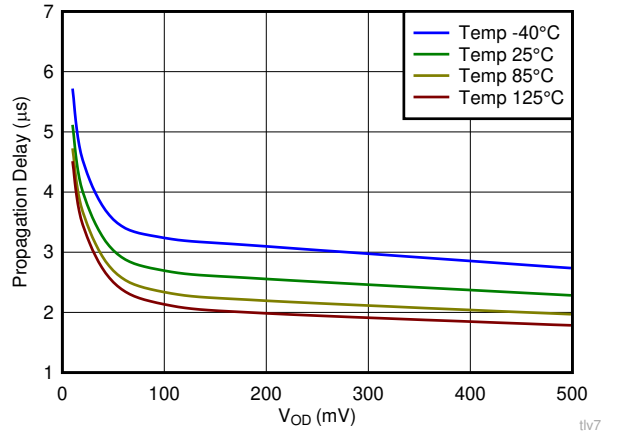
V_{CM} = V_{CC} / 2 TLV70x2

图 5-29. I_{CC} vs V_{CC}



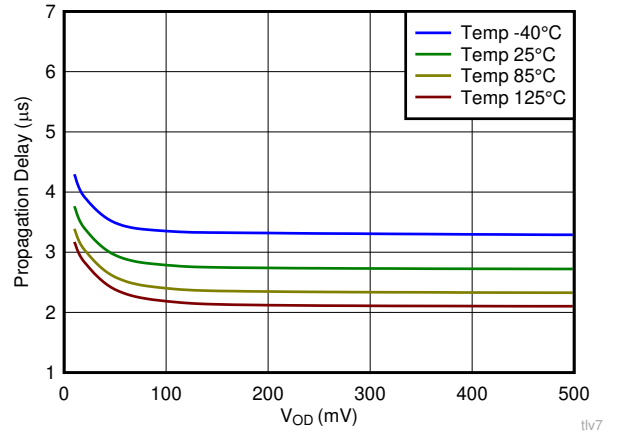
V_{OD} = 100mV TLV703x Rise only

图 5-30. Rise/Fall Time vs Load Capacitance



V_{CC} = 3.3V to 5V TLV703x

图 5-31. Propagation Delay (L-H) vs Input Overdrive



V_{CC} = 3.3V to 5V

图 5-32. Propagation Delay (H-L) vs Input Overdrive

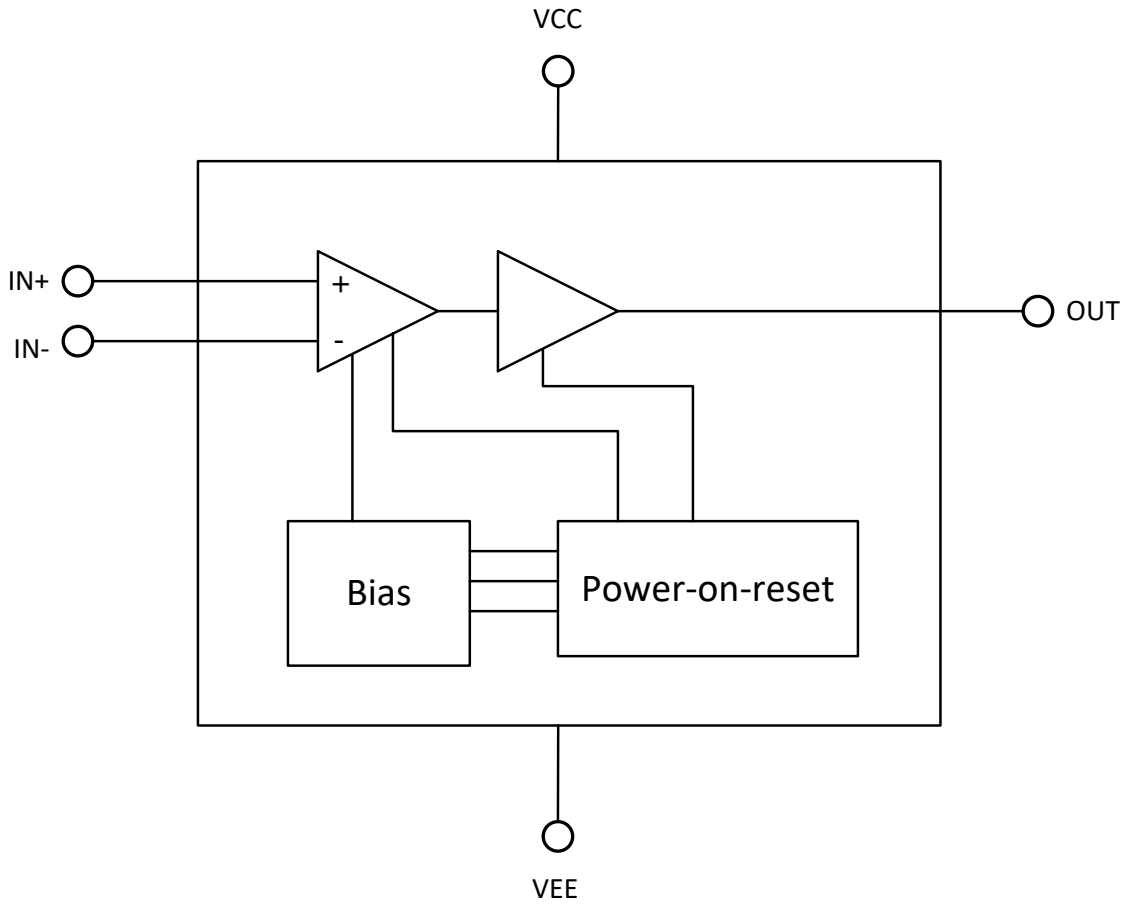
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6 Detailed Description

6.1 Overview

The TLV703x and TLV704x are nano-power comparators with push-pull and open-drain outputs. Operating from 1.6V to 6.5V and consuming only 315nA, the TLV703x and TLV704x are designed for portable and industrial applications. The TLV703x and TLV704x are available in a variety of leadless and leaded packages to offer significant board space saving in space-challenged designs. The TLV70x1S and TLV70x1L offer alternate pinouts with an exteded 1.2V minimum supply.

6.2 Functional Block Diagram



6.3 Feature Description

The TLV703x and TLV704x devices are nanoPower comparators that are capable of operating at low voltages. The TLV703x and TLV704x feature a rail-to-rail input stage capable of operating up to 100mV beyond the VCC power supply rail. The TLV703x (push-pull) and TLV704x (open-drain) also feature internal hysteresis.

6.4 Device Functional Modes

The TLV703x and TLV704x have a power-on-reset (POR) circuit. While the power supply (V_S) is less than the minimum supply voltage, either upon ramp-up or ramp-down, the POR circuitry is activated.

For the TLV703x, the POR circuit holds the output low (at V_{EE}) while activated.

For the TLV704x, the POR circuit keeps the output high impedance (logical high) while activated.

When the supply voltage is greater than, or equal to, the minimum supply voltage, the comparator output reflects the state of the differential input (V_{ID}).

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6.4.1 Inputs

The TLV703x and TLV704x input common-mode extends from V_{EE} to 100mV above V_{CC}. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase inversion of the comparator output occurs when the input pins exceed V_{CC} and V_{EE}.

The input of TLV703x and TLV704x is fault tolerant and maintains the same high input impedance when V_{CC} is unpowered or ramping up. The input can be safely driven up to the specified maximum voltage (7V) with V_{CC} = 0V. The V_{CC} is isolated from the input and maintains the high impedance even when a higher voltage is applied to the input.

The input bias current is typically 1pA for input voltages between V_{CC} and V_{EE}. The comparator inputs are protected from voltages below V_{EE} by internal diodes connected to V_{EE}. As the input voltage goes under V_{EE}, the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles every 10°C temperature increases.

6.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in 图 6-1. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (7mV for both TLV703x and TLV704x).

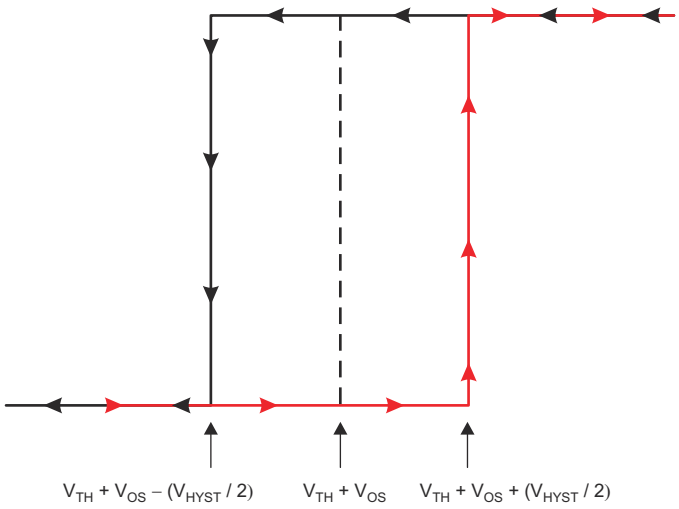


图 6-1. Hysteresis Transfer Curve

6.4.3 Output

The TLV703x features a push-pull output stage eliminating the need for an external pullup resistor.

The TLV704x features an open-drain output stage enabling the output logic levels to be pulled up to an external source up to 6.5V independent of the supply voltage.

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7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The TLV703x and TLV704x are nano-power comparators with reasonable response time. The comparators have a rail-to-rail input stage with integrated hysteresis that can monitor signals beyond the positive supply rail. When higher levels of hysteresis are required, positive feedback can be externally added. The push-pull output stage of the TLV703x is an excellent choice for reduced power budget applications and features no shoot-through current. When level shifting or wire-ORing of the comparator outputs is needed, the TLV704x with open-drain output stage is well suited to meet the system needs. In either case, the wide operating voltage range, low quiescent current, and small size of the TLV703x and TLV704x make these comparators excellent candidates for battery-operated and portable, handheld designs.

7.1.1 Inverting Comparator With Hysteresis for TLV703x

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in 图 7-1. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. 方程式 1 defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. Use 方程式 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

方程式 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

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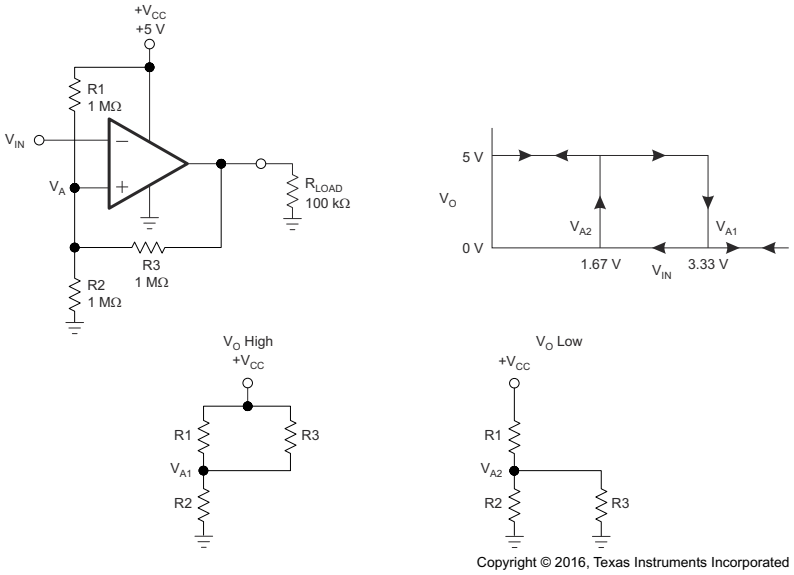


图 7-1. TLV703x in an Inverting Configuration With Hysteresis

7.1.2 Non-Inverting Comparator With Hysteresis for TLV703x

A noninverting comparator with hysteresis requires a two-resistor network, as shown in 图 7-2, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise to V_{IN1}. Use 方程式 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

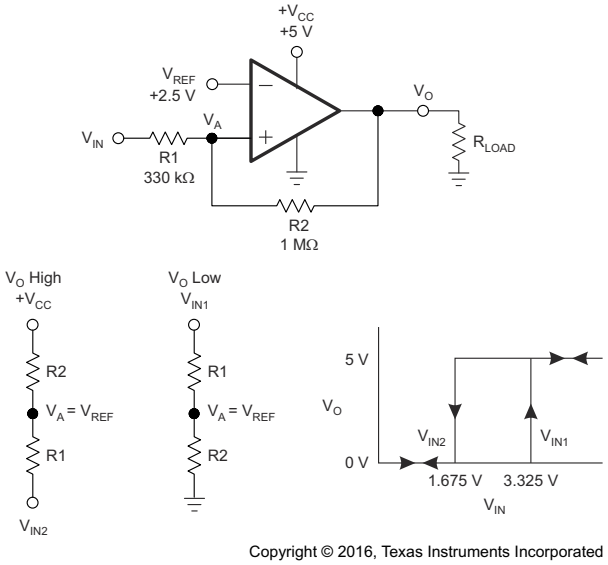
When V_{IN} is high, the output is also high. For the comparator to switch back to a low state, V_{IN} must drop to V_{IN2} such that V_A is equal to V_{REF}. Use 方程式 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in 方程式 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

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图 7-2. TLV703x in a Noninverting Configuration With Hysteresis

7.2 Typical Applications

7.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. 图 7-3 shows a simple window comparator circuit.

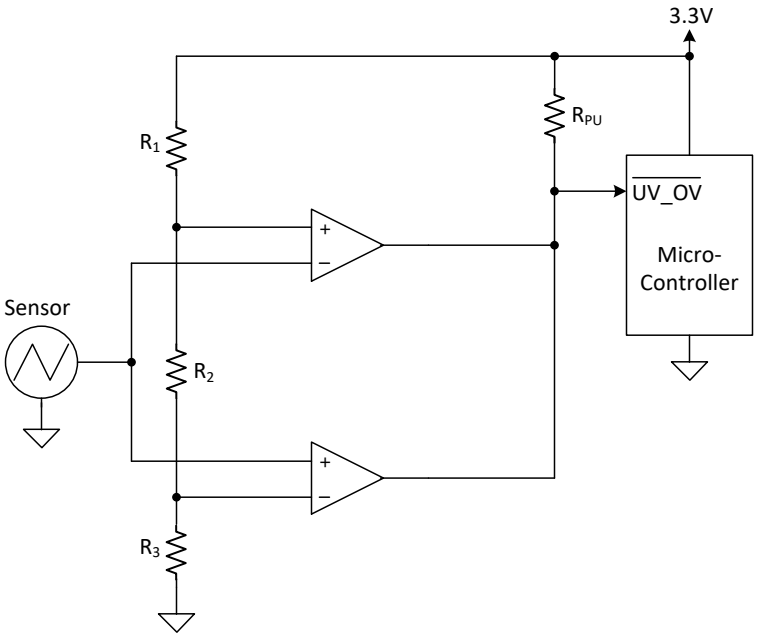


图 7-3. TLV704x-Based Window Comparator

7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1V
- Alert (logic low output) when an input signal is greater than 2.2V
- Alert signal is active low
- Operate from a 3.3V power supply

7.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 图 7-3. Connect V_{CC} to a 3.3V power supply and V_{EE} to ground. Make R1, R2, and R3 each 10MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and V_{TH-}). With each resistor being equal, V_{TH+} is 2.2V and V_{TH-} is 1.1V. Large resistor values such as 10MΩ are used to minimize power consumption. The sensor output voltage is applied to the inverting and noninverting inputs of the two TLV704x devices. The TLV704x is used for the open-drain output configuration. Using the TLV704x allows the two comparator outputs to be wire-ored together. The respective comparator outputs are low when the sensor is less than 1.1V or greater than 2.2V. V_{OUT} is high when the sensor is in the range of 1.1V to 2.2V.

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7.2.1.3 Application Curve

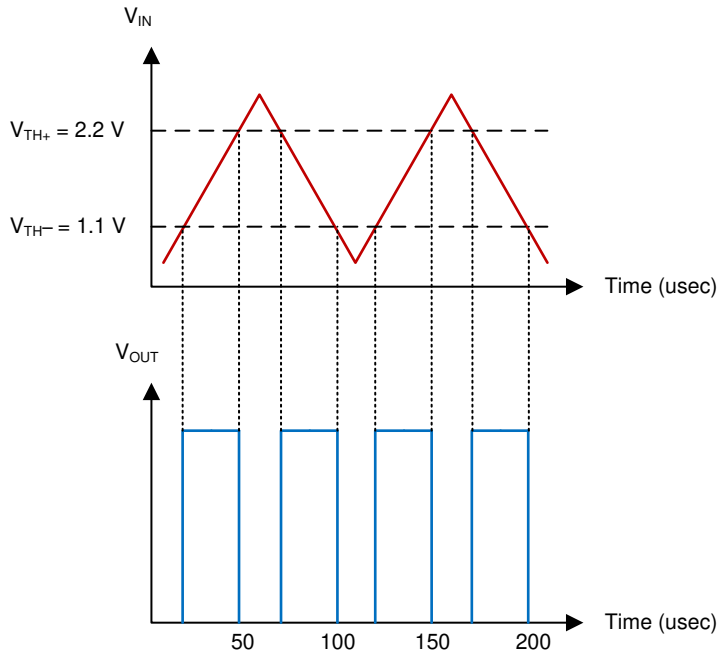
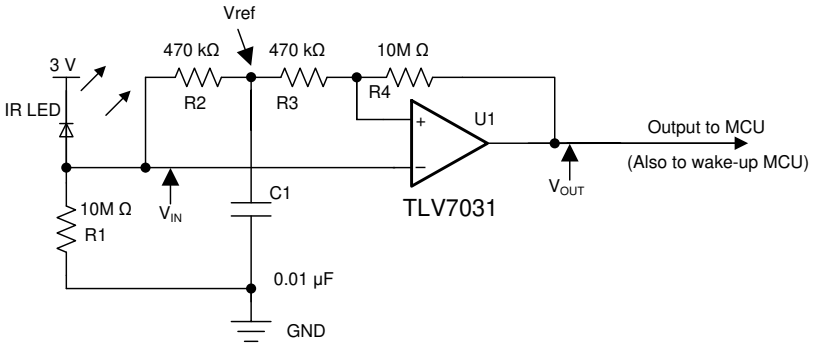


图 7-4. Window Comparator Results

7.2.2 IR Receiver Analog Front End

A single TLV703x device can be used to build a complete IR receiver analog front end (AFE). The nanoamp quiescent current and low input bias current make possible powereing the circuit with a coin cell battery, which can last for years.



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图 7-5. IR Receiver Analog Front End Using TLV703x

7.2.2.1 Design Requirements

For this design, follow these design requirements:

- Use a proper resistor (R_1) value to generate an adequate signal amplitude applied to the inverting input of the comparator.
- The low input bias current I_B (2pA typical) allows a greater value of R1 to be used.
- The RC constant value (R_2 and C_1) must support the targeted data rate (that is, 9,600 bauds) to maintain a valid tripping threshold.
- The hysteresis introduced with R_3 and R_4 helps to avoid spurious output toggles.

7.2.2.2 Detailed Design Procedure

The IR receiver AFE design is highly streamlined and optimized. R_1 converts the IR light energy induced current into voltage and applies to the inverting input of the comparator. The RC network of R_2 and C_1 establishes a reference voltage V_{ref}, which tracks the mean amplitude of the IR signal. The noninverting input is directly connected to V_{ref} through R3. R3 and R4 are used to produce a hysteresis to keep transitions free of spurious toggles. To reduce the current drain from the coin cell battery, data transmission must be short and infrequent.

More technical details are provided in the TI TechNote *Low Power Comparator for Signal Processing and Wake-Up Circuit in Smart Meters* (SNVA808).

7.2.2.3 Application Curve

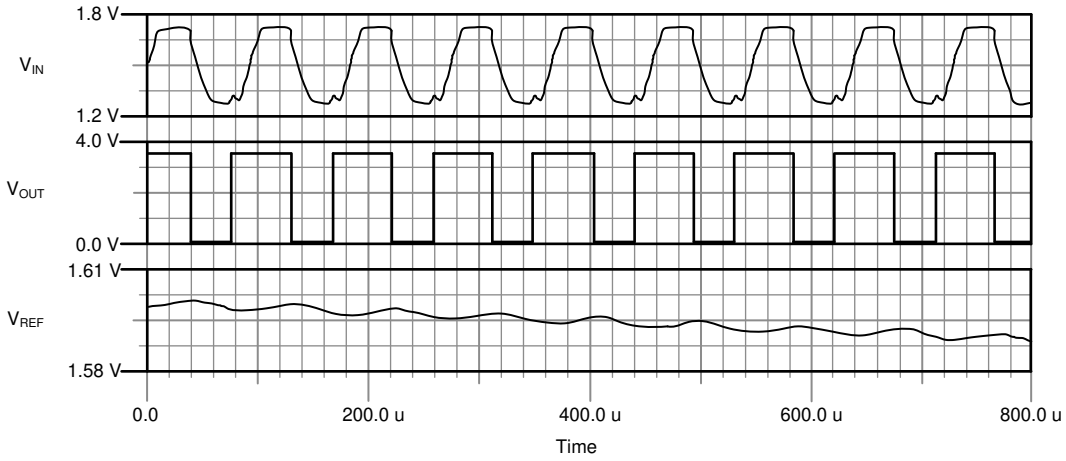


图 7-6. IR Receiver AFE Waveforms

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7.2.3 Square-Wave Oscillator

A square-wave oscillator can be used as low-cost timing reference or system supervisory clock source.

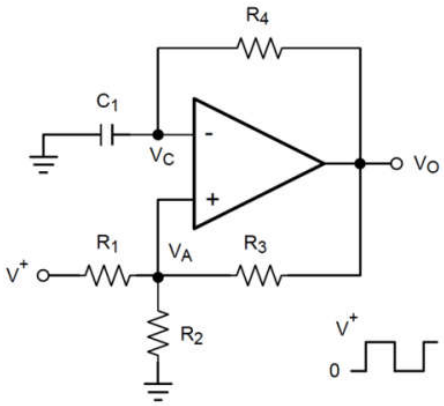


图 7-7. Square-Wave Oscillator

7.2.3.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor and resistor. The maximum frequency is limited by the propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which can help reduce BOM cost and board space.

7.2.3.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following section provides details to calculate these component values.

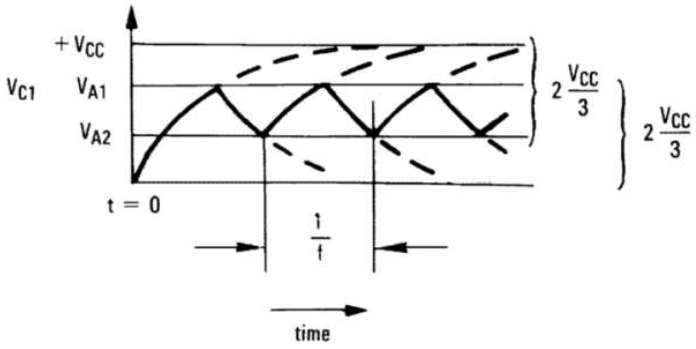


图 7-8. Square-Wave Oscillator Timing Thresholds

First consider the output of figure 图 7-7 is high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until equal to the noninverting input. The value of V_A at the point is calculated by 方程式 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \| R_3} \tag{7}$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2V_{CC}/3$

At this time the comparator output trips pulling down the output to the negative rail. The value of V_A at this point is calculated by 方程式 8.

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3} \tag{8}$$

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until reaching V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals the time duration from $2V_{CC}$ / 3 to V_{CC} / 3 then back to $2V_{CC}$ / 3, which is given by R_4C_1 × ln2 for each trip. Therefore, the total time duration is calculated as $2R_4C_1$ × ln2. The oscillation frequency can be obtained by 方程式 9:

$$f = 1/(2\ R4 \times C1 \times In2) \tag{9}$$

7.2.3.3 Application Curve

图 7-9 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100k\Omega$
- $C_1 = 100pF$, $C_L = 20pF$
- V+ = 5V, V– = GND
- C_{stray} (not shown) from V_A to GND = 10pF

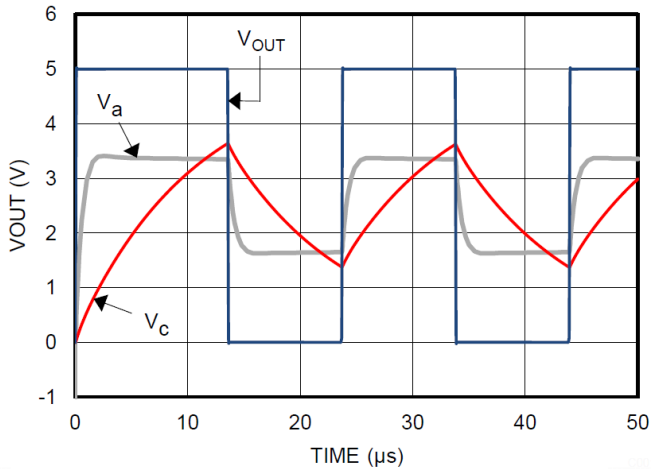


图 7-9. Square-Wave Oscillator Output Waveform

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7.2.4 Quadrature Rotary Encoder

A quadrature encoder for rotary motors/shafts utilizing a Tunneling Magnetoresitance (TMR) Rotation Sensor can track the position of the motor shaft even when power is turned off, while the TLV7032 provides additional hysteresis to prevent unwanted output toggling between quadrants. The TLV7032 can be used with other sensing techniques as well, such as optical, capacitive, or inductive.

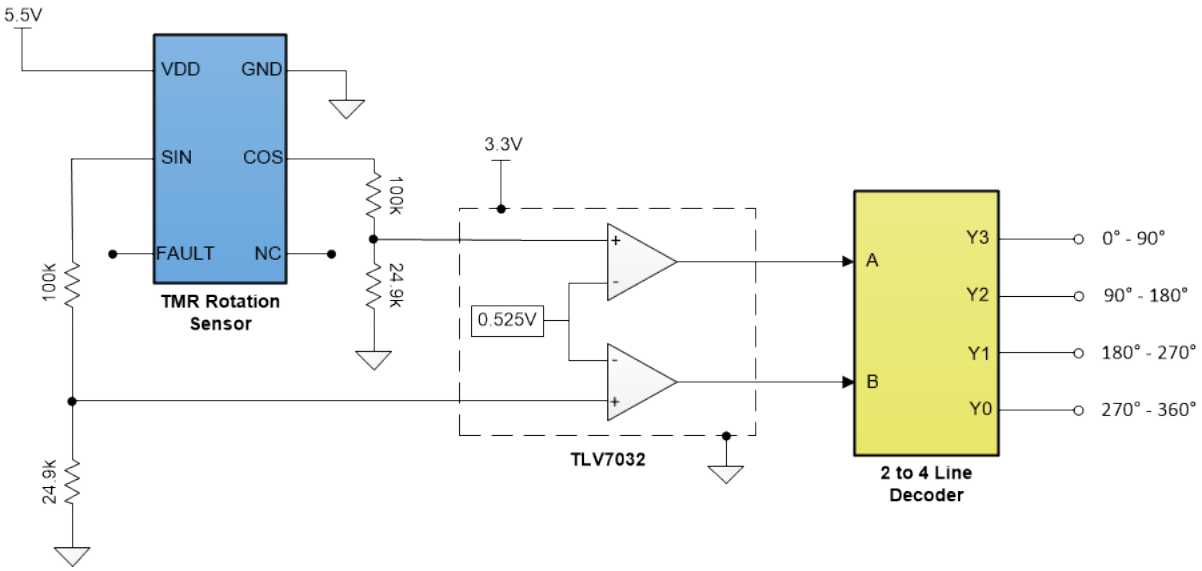
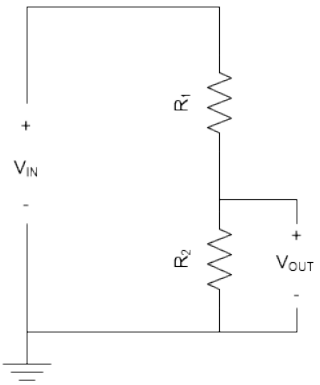


图 7-10. Quadrant Encoder Detector

7.2.4.1 Design Requirements

TMR Rotation Sensors general have two digital, binary outputs that are 90 degrees out of phase. The TLV7032 can be used to provide additional hysteresis maintains there is not any unwanted toggling of the output when the sensors are between the transition points of two quadrants. The TLV7032 already provides 10mV of typical internal hysteresis. By dividing down the output voltage from the rotation sensor using a voltage divider, the internal hysteresis scales up by the same voltage divider ratio.



$$V_{OUT} = V_{IN} \times \frac{R2}{R1+R2}$$

图 7-11. Voltage Divider Equation

7.2.4.2 Detailed Design Procedure

First, choose a target range of hysteresis vlaue to achieve. For this design example, 50mV of hysteresis is chosen as the target. Since the TLV7032 already has 10mV (typ) of internal hysteresis, the voltage output from the TMR Rotation Sensor must be scaled down by a factor of 5. This way, the 10mV of internal hysteresis gets scaled up by a factor of 5, resulting in 50mV of hysteresis. The minimum output HIGH level for the TMR Rotation Sensor used in Figure 47 is 5.25V. Since 5.25V is the minimum output high value, this can be used to substitute V_{IN} from the Voltage Divider Equation in Figure 48. Since the voltage from the TMR rotation sensor needs to be scaled down by a factor of 5, the equation in Figure 48 can be rewritten as:

$$\frac{1}{5} = \frac{R_2}{R_1 + R_2}$$

The above equation can be solved for using standard resistor values, where R_1 = 100kΩ, and R_2 = 24.9kΩ. The minimum voltage seen at the noninverting pins of the comparator when the output is HIGH is 1.05V. To make the device transition at 50% output high level, the inverting pins of the TLV7032 must be tied to a 0.525V reference.

7.2.4.3 Application Curve

Figure 49 shows the TLV7032 achieving approximately 50mV of hysteresis using the following component values:

- R_1 = 100kΩ
- R_2 = 24.9kΩ
- V_{REF} (IN-) = 0.525V

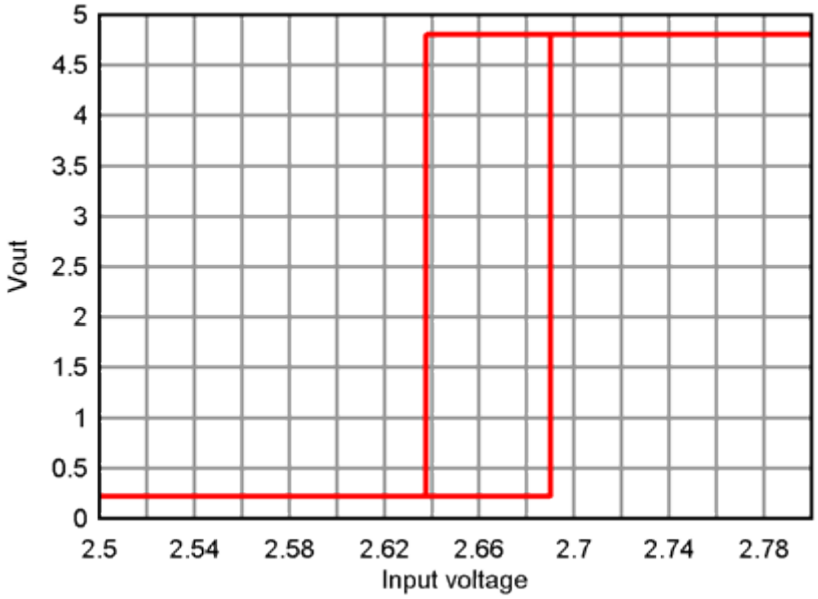


图 7-12. DC Input Voltage Sweep

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7.3 Power Supply Recommendations

The TLV703x and TLV704x have a recommended operating voltage range (V_S) of 1.6V to 6.5V. V_S is defined as V_{CC} – V_{EE}. Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5V and 0V and bipolar supply voltages of +2.5V and –2.5V create comparable operating voltages for V_S. However, when bipolar supply voltages are used, be aware that the logic low level of the comparator output is referenced to V_{EE}.

Output capacitive loading and output toggle rate causes the average supply current to rise over the quiescent current.

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7.4 Layout

7.4.1 Layout Guidelines

To reduce PCB fabrication cost and improve reliability, TI recommends using a 4-mil via at the center pad connected to the ground trace or plane on the bottom layer.

TI recommends a power-supply bypass capacitor of 100nF when supply output impedance is high, supply traces are long, or when excessive noise is expected on the supply lines. Bypass capacitors are also recommended when the comparator output drives a long trace or is required to drive a capacitive load. Due to the fast rising and falling edge rates and high-output sink and source capability of the TLV703x and TLV704x output stages, higher than normal quiescent current can be drawn from the power supply. Under this circumstance, the system will benefit from a bypass capacitor directly from the supply pin to ground.

7.4.2 Layout Example

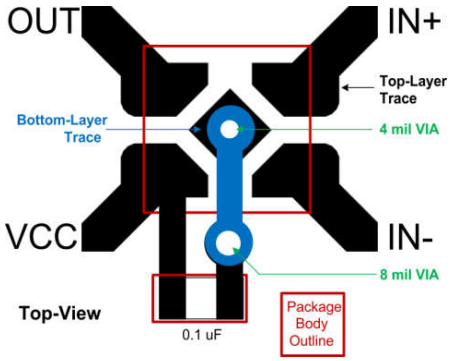


图 7-13. Layout Example

The application report *Designing and Manufacturing With TI's X2SON Packages* (SCEA055) helps PCB designers to achieve optimal designs.

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV70x1 device family. The TLV7011 Micro-Power Comparator Dip Adaptor Evaluation Module can be requested at the Texas Instruments website through the product folder or purchased directly from the TI eStore.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- *Designing and Manufacturing With TI's X2SON Packages* (SCEA055)
- *Low Power Comparator for Signal Processing and Wake-Up Circuit in Smart Meters* (SNVA808)

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision I (June 2024) to Revision J (November 2024)	Page
• 更新了“S”和“L”文本以及电源电压	1
• Added 1.2V Recommended Min Supply for "S" and "L" devices	6

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Changes from Revision H (July 2021) to Revision I (June 2024) **Page**

- 添加了封装型号 TLV70x1L 和 TLV70xS 1

Changes from Revision G (Nov 2020) to Revision H (July 2021) **Page**

- 发布了 TSSOP 封装选项 1

Changes from Revision F (November 2019) to Revision G (December 2020) **Page**

- 更新了整个文档中的表格、图和交叉参考的编号格式 1
- 为双通道选项添加了 SOT-23 (8) 和 WSON (8) 1

Changes from Revision E (June 2019) to Revision F (November 2019) **Page**

- 添加了四通道版本 1
- 为双通道选项添加了 SOT-23 (8) 和 WSON (8) 1
- 添加了 QUAD 封装选项 1
- Added TSSOP and RTE pinout information to *Pin Configuration and Functions* section 4

Changes from Revision D (April 2019) to Revision E (June 2019) **Page**

- Changed VOH min from 4.7V to 4.65V for all package options in EC Table (Single) 8
- Changed VOL max from 300mV to 350mV for all package options in EC Table (Single) 8
- Deleted separate rows for VOH & VOL for DBV package options only in EC Table (Single) 8

Changes from Revision C (March 2019) to Revision D (April 2019) **Page**

- Added separate rows for VOH & VOL for DBV package options in EC Table (Single) 8

Changes from Revision B (May 2018) to Revision C (March 2019) **Page**

- 在 VSSOP 封装中添加了双通道版本 1
- 通篇将 TLV7031 更改为 TLV703x 并将 TLV7041 更改为 TLV704x 1
- 添加了双通道版本 1
- 在 VSSOP 封装中添加了器件信息双通道版本 1
- 删除了“SOT-23 封装仅处于预发布状态” 1

Changes from Revision A (January 2018) to Revision B (May 2018) **Page**

- 将预发布 SC70 封装更改为量产数据 1

Changes from Revision * (September 2017) to Revision A (January 2018) **Page**

- 将数据表标题从“TLV7031/TLV7041 小尺寸、毫微功耗、低电压比较器”更改为“TLV7031 和 TLV7041 小尺寸、毫微功耗、低电压比较器” 1
- 向 *特性* 中添加了“内部磁滞”项目符号 1

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- 在*特性* 中注明了哪个器件具有推挽输出和开漏输出选项 1
- 从重要图形标题中删除了 (TLV7031) , 因为该图形涵盖了 TLV7031 和 TLV7041 器件 1
- Added X2SON tablenote to *Pin Functions* table 3
- Changed 图 5-2 11
- Added note to the *Timing Diagrams* section 11
- Smoothed Propagation Delay plots in 图 5-31 through 12
- Changed vertical labels on 图 5-20, 图 5-21, 图 5-17, and 图 5-30 12
- Changed *Functional Block Diagram* 17
- Changed text '...external source up to 7V to 6.5V' 18
- Changed 图 7-3 22
- Added note to the *Layout Example* section 30
- Added *Documentation Support* section 31

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7031DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1IE2
TLV7031DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IE2
TLV7031DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IE2
TLV7031DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TLV7031DBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TLV7031DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN | POST-PLAT AG SPOT	Level-2-260C-1 YEAR	-40 to 125	19P
TLV7031DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19P
TLV7031DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19P
TLV7031DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | POST-PLAT AG SPOT	Level-2-260C-1 YEAR	-40 to 125	19P
TLV7031DCKT.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19P
TLV7031DCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19P
TLV7031DPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7K
TLV7031DPWR.A	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7K
TLV7031DPWR.B	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7K
TLV7031LDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3JVH
TLV7031SDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3K2H
TLV7031SDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3K2H
TLV7031SDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	POST-PLAT AG SPOT	Level-1-260C-UNLIM	-40 to 125	3JXH
TLV7031SDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	POST-PLAT AG SPOT	Level-1-260C-UNLIM	-40 to 125	3JXH
TLV7032DDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	22KF
TLV7032DDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	22KF
TLV7032DDFRG4	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	22KF
TLV7032DDFRG4.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	22KF
TLV7032DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	7032
TLV7032DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7032
TLV7032DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1ZXH
TLV7032DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1ZXH

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7034PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TLV7034
TLV7034PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV7034
TLV7034RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TL7034
TLV7034RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TL7034
TLV7041DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1IF2
TLV7041DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IF2
TLV7041DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1IF2
TLV7041DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	1IF2
TLV7041DBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	1IF2
TLV7041DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN | POST-PLAT AG SPOT	Level-2-260C-1 YEAR	-40 to 125	19Q
TLV7041DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19Q
TLV7041DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19Q
TLV7041DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | POST-PLAT AG SPOT	Level-2-260C-1 YEAR	-40 to 125	19Q
TLV7041DCKT.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19Q
TLV7041DCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19Q
TLV7041DPWR	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7L
TLV7041DPWR.A	Active	Production	X2SON (DPW) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7L
TLV7041LDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3JWH
TLV7041SDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3K3H
TLV7041SDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3K3H
TLV7041SDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	POST-PLAT AG SPOT	Level-1-260C-UNLIM	-40 to 125	3JZH
TLV7041SDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	POST-PLAT AG SPOT	Level-1-260C-UNLIM	-40 to 125	3JZH
TLV7042DDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	22LF
TLV7042DDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	22LF
TLV7042DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7042
TLV7042DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7042
TLV7042DGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7042
TLV7042DGKRG4.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7042

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7042DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1ZZH
TLV7042DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZZH
TLV7042DSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZZH
TLV7042DSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ZZH
TLV7044PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	TLV7044
TLV7044PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV7044
TLV7044RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TL7044
TLV7044RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	TL7044
TLV7044RTERG4	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL7044
TLV7044RTERG4.A	Active	Production	WQFN (RTE) | 16	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL7044

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV7031, TLV7032, TLV7034, TLV7041, TLV7042, TLV7044 :

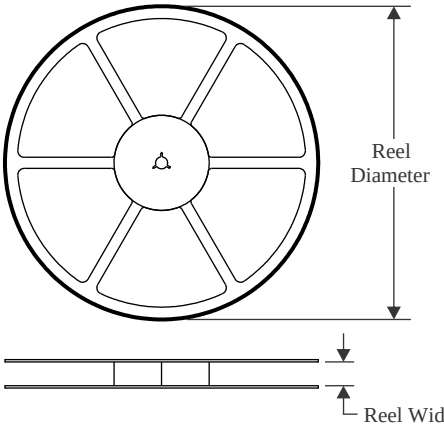
- Automotive : TLV7031-Q1, TLV7032-Q1, TLV7034-Q1, TLV7041-Q1, TLV7042-Q1, TLV7044-Q1

NOTE: Qualified Version Definitions:

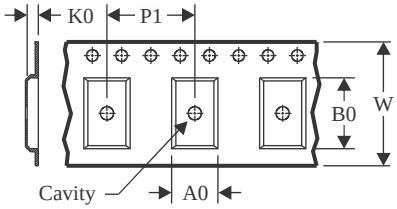
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

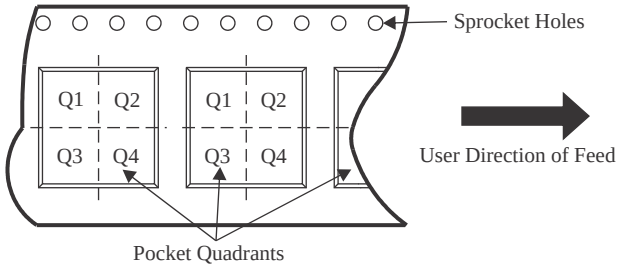


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

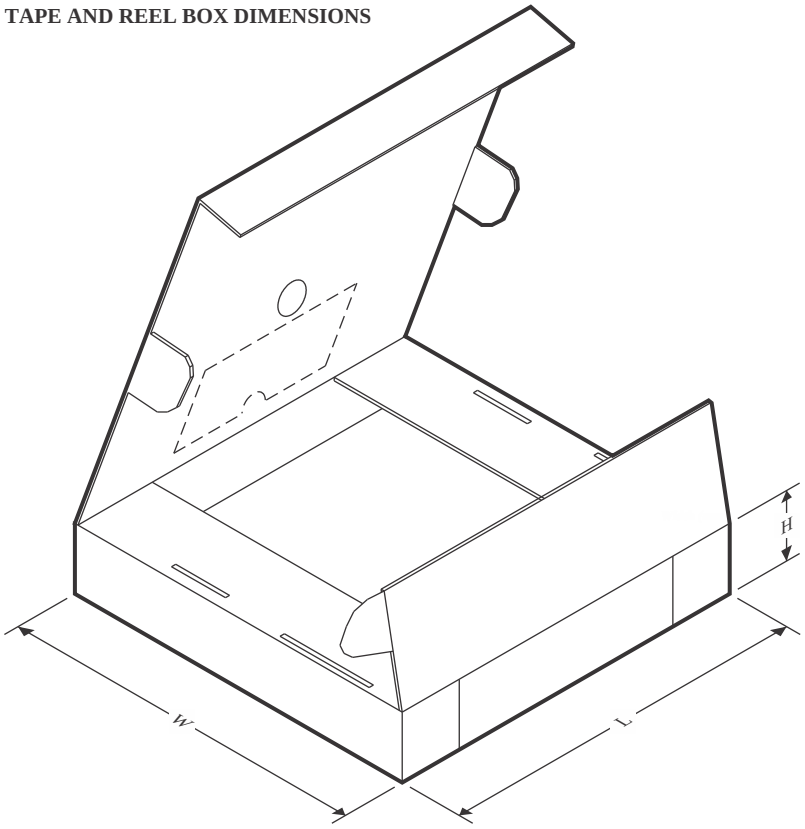


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7031DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7031DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
TLV7031DCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV7031DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV7031LDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7031SDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7031SDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV7032DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7032DDFRG4	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7032DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7032DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV7034PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV7034PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV7034RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV7041DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7041DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
TLV7041DCKT	SC70	DCK	5	250	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV7041DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV7041LDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7041SDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7041SDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV7042DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV7042DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7042DGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7042DSGR	WSON	DSG	8	3000	178.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV7042DSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV7044PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV7044RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV7044RTERG4	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7031DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV7031DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
TLV7031DCKT	SC70	DCK	5	250	210.0	185.0	35.0
TLV7031DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV7031LDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV7031SDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV7031SDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV7032DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7032DDFRG4	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7032DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7032DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV7034PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV7034PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV7034RTER	WQFN	RTE	16	3000	360.0	360.0	36.0
TLV7041DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV7041DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
TLV7041DCKT	SC70	DCK	5	250	210.0	185.0	35.0
TLV7041DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0

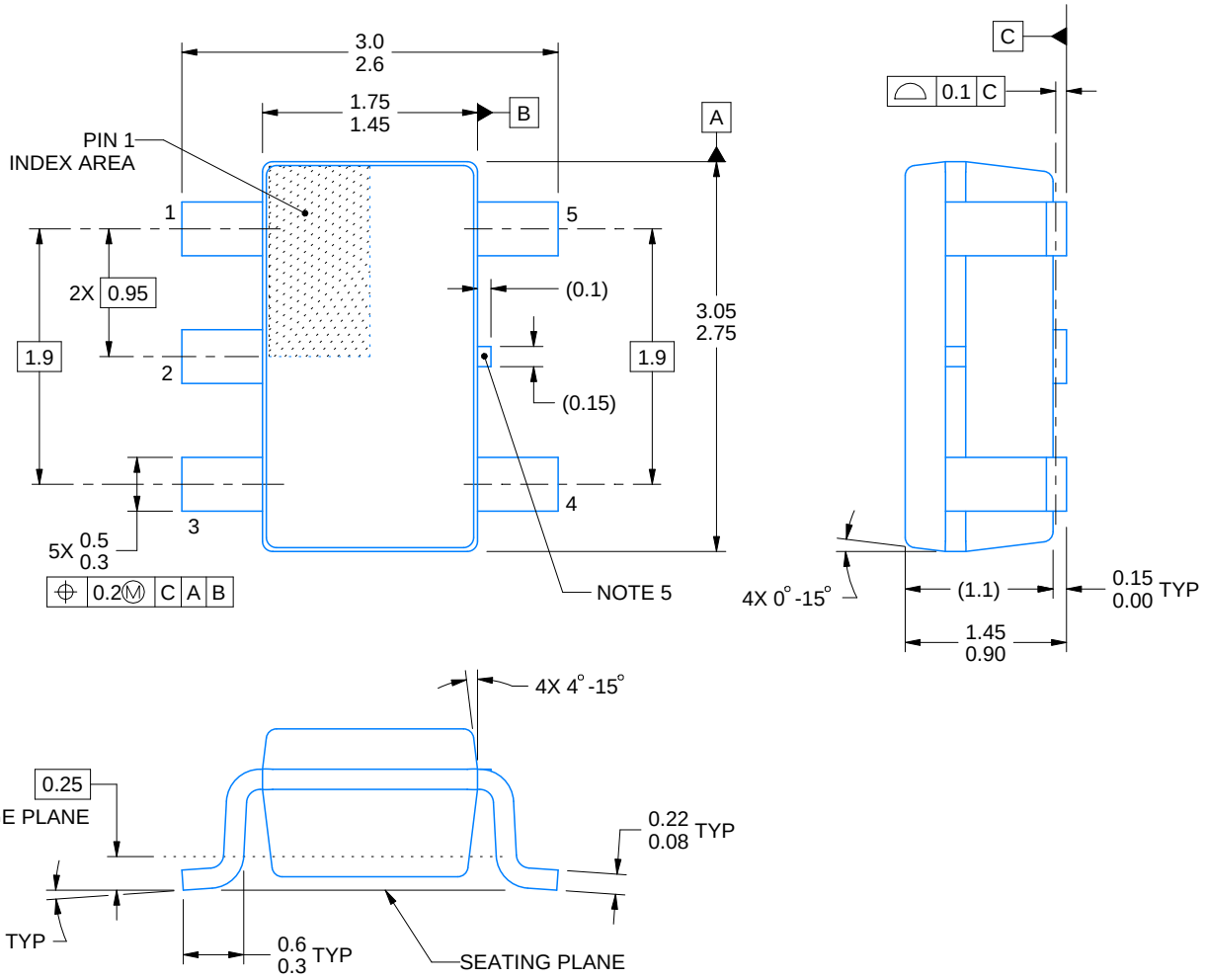
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7041LDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV7041SDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV7041SDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV7042DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV7042DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7042DGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV7042DSGR	WSON	DSG	8	3000	208.0	191.0	35.0
TLV7042DSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TLV7044PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV7044RTER	WQFN	RTE	16	3000	360.0	360.0	36.0
TLV7044RTERG4	WQFN	RTE	16	5000	367.0	367.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

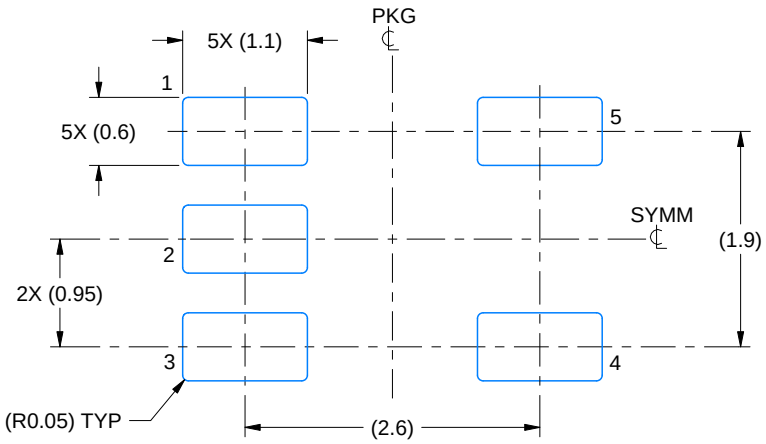
SMALL OUTLINE TRANSISTOR



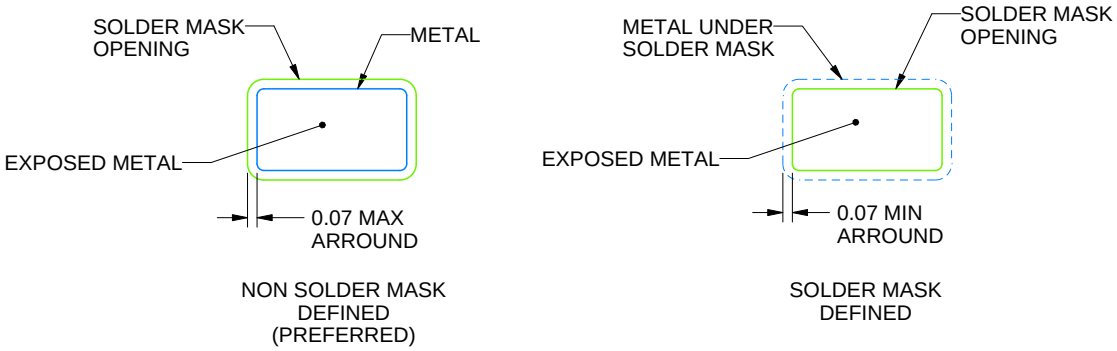
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

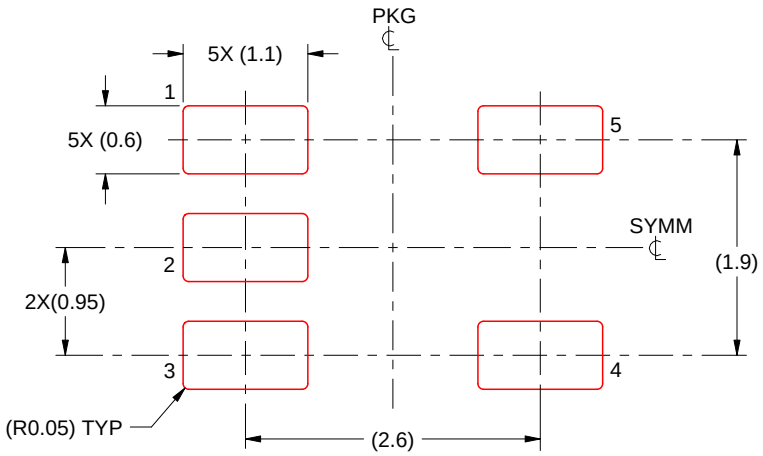


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

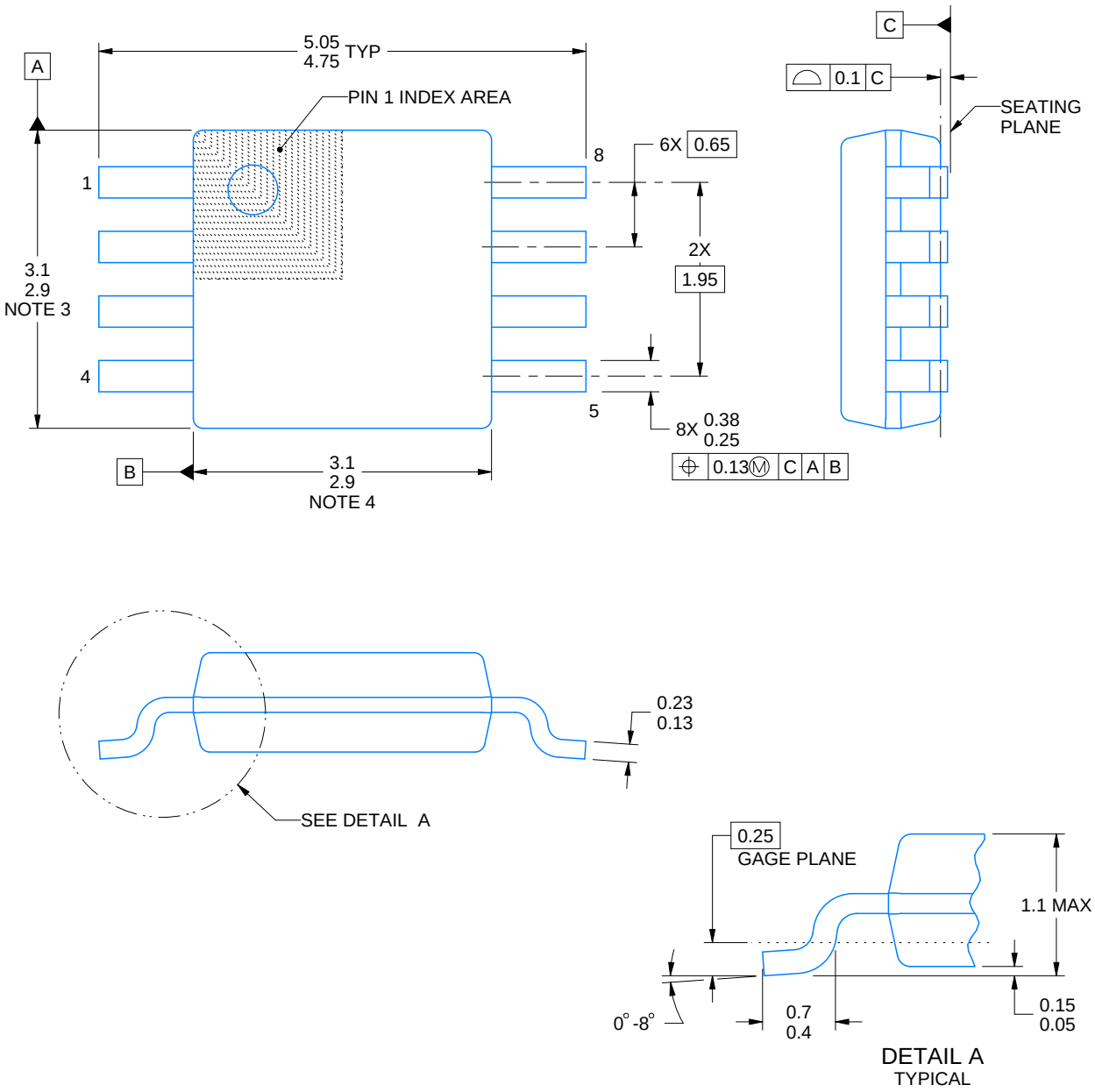
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

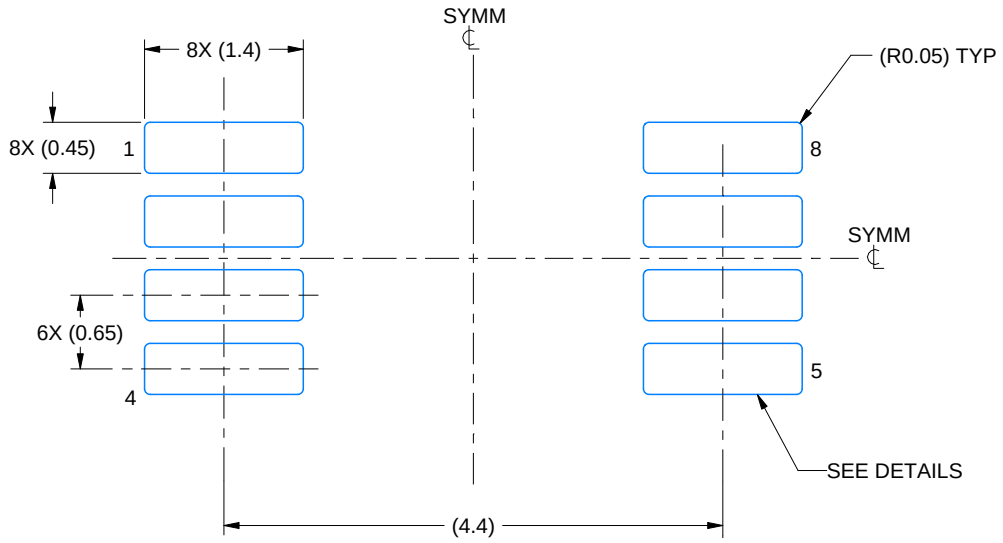
SMALL OUTLINE PACKAGE



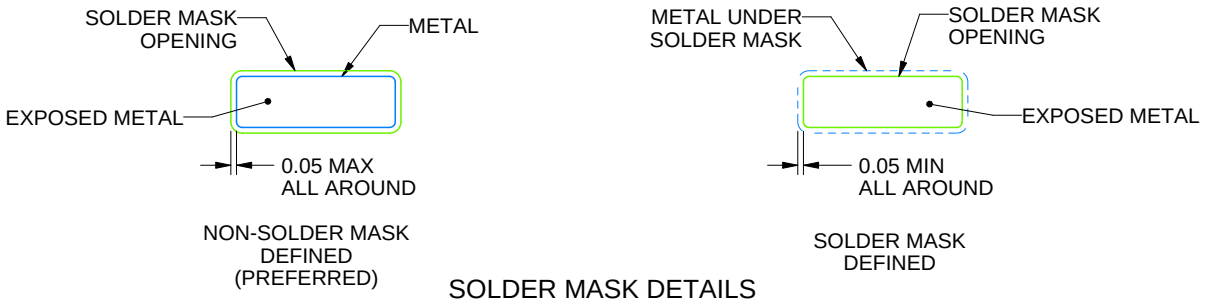
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

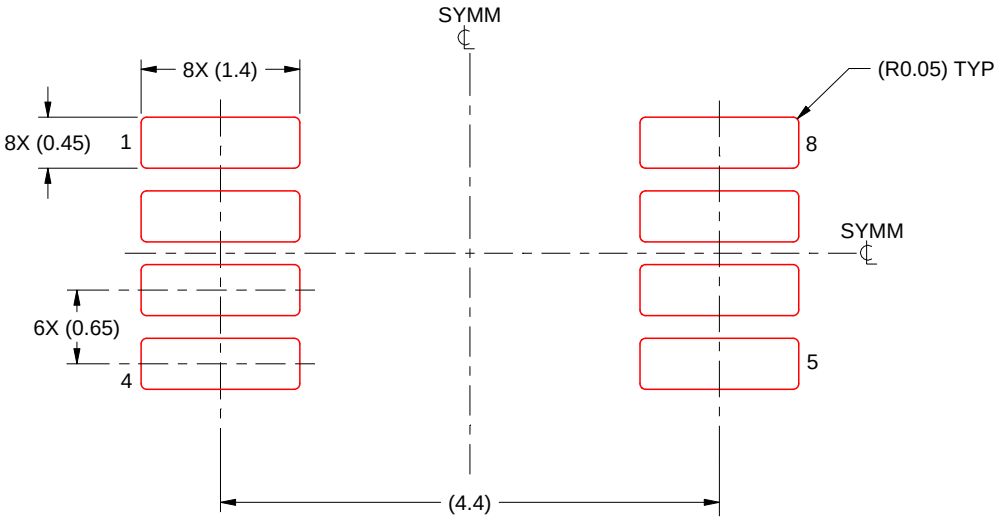


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

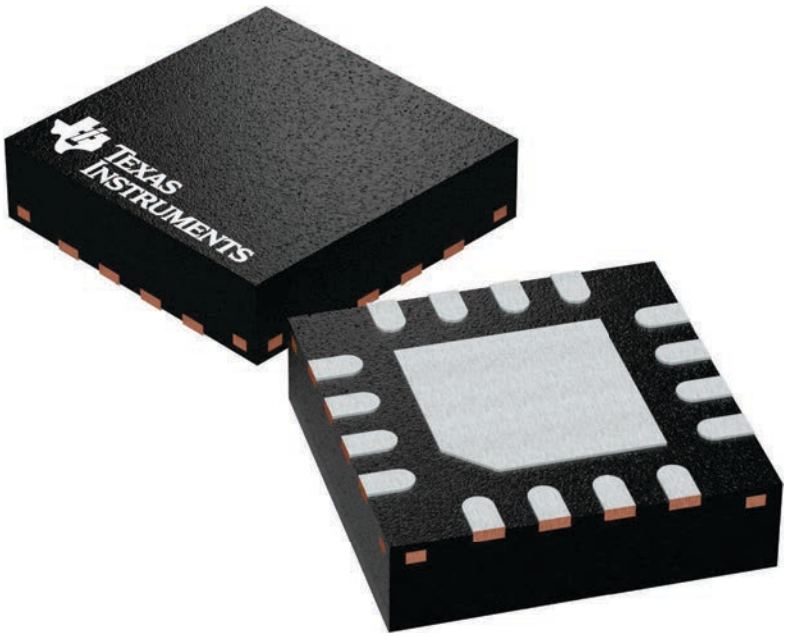
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

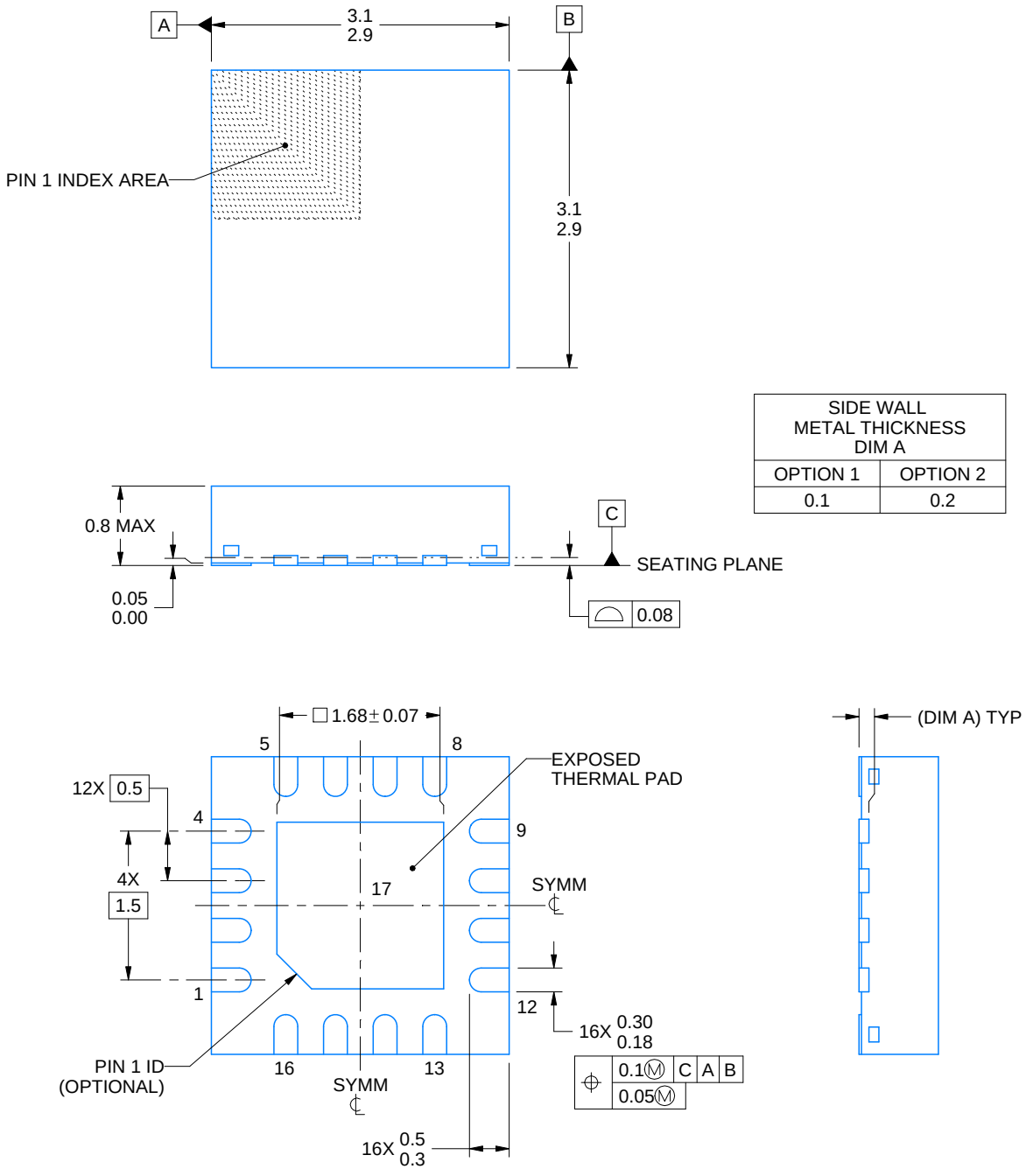


RTE0016C

PACKAGE OUTLINE

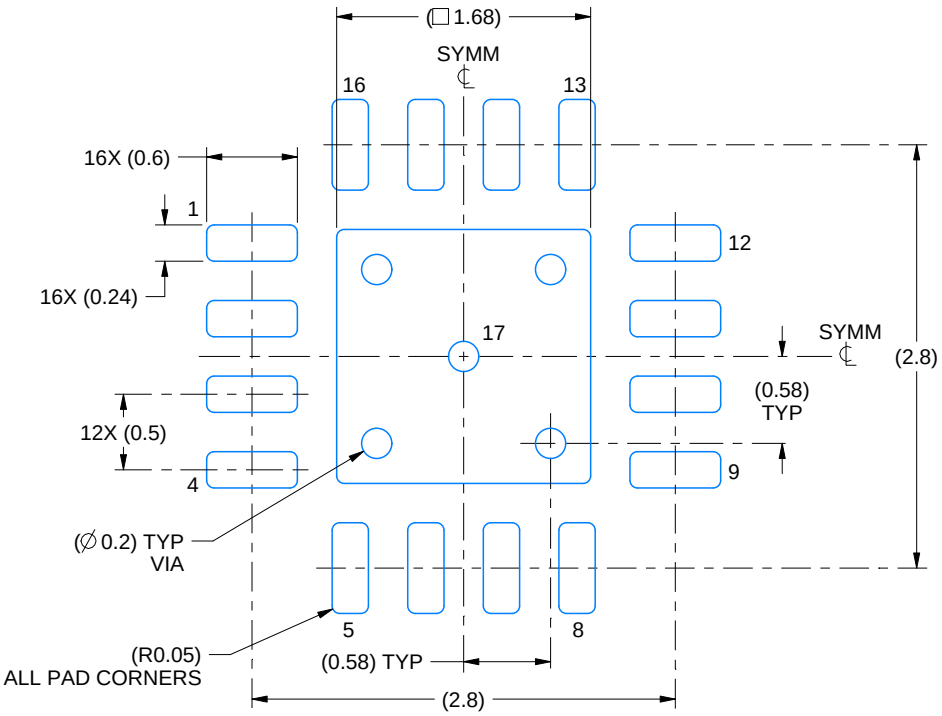
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

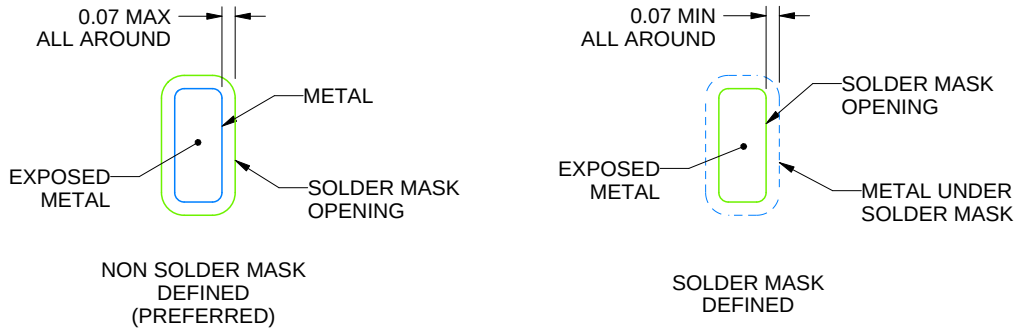


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

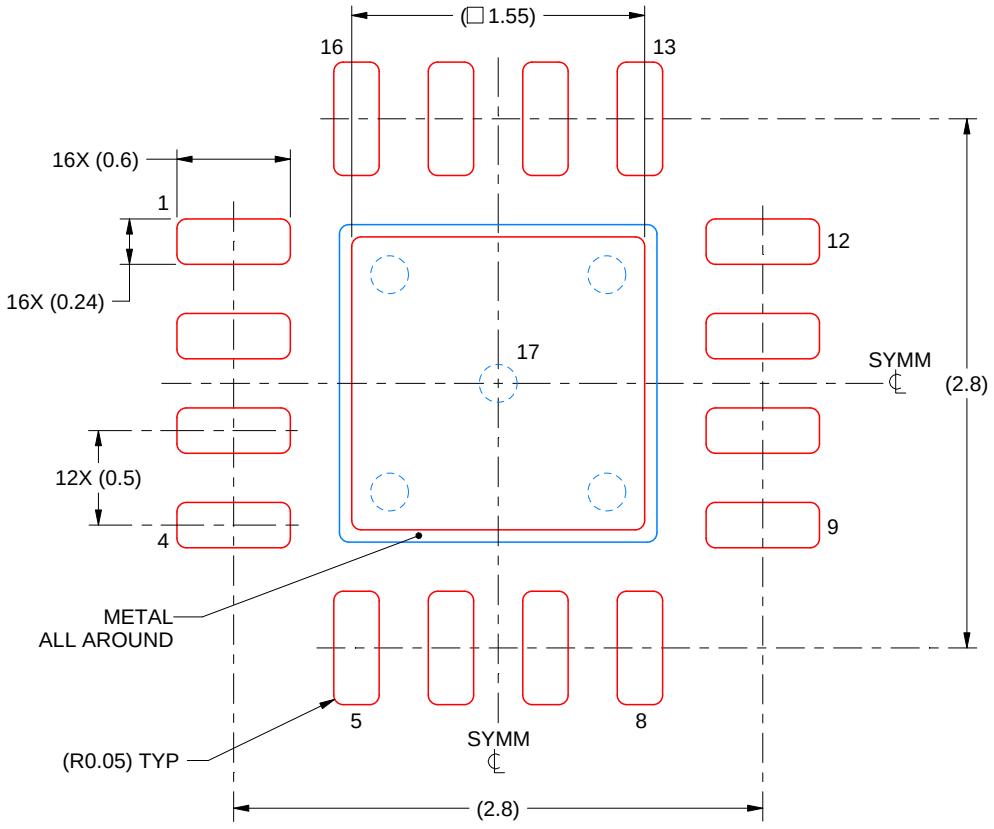


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

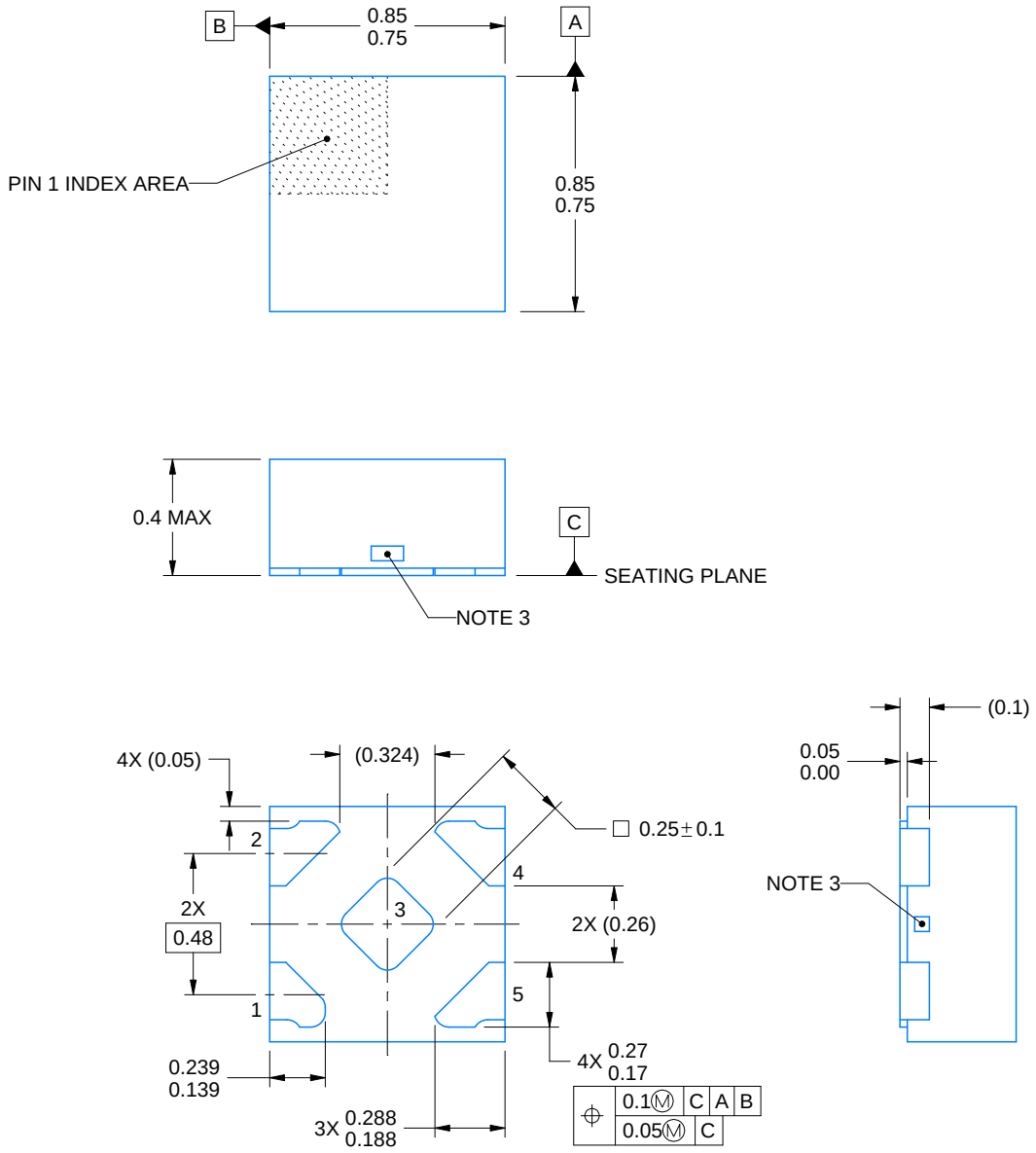
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

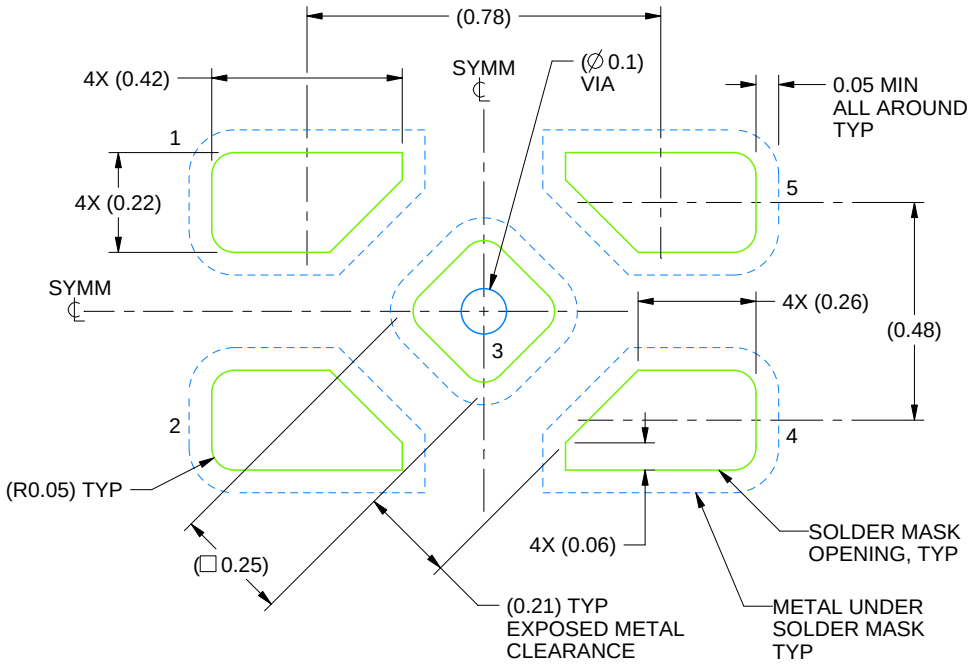
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

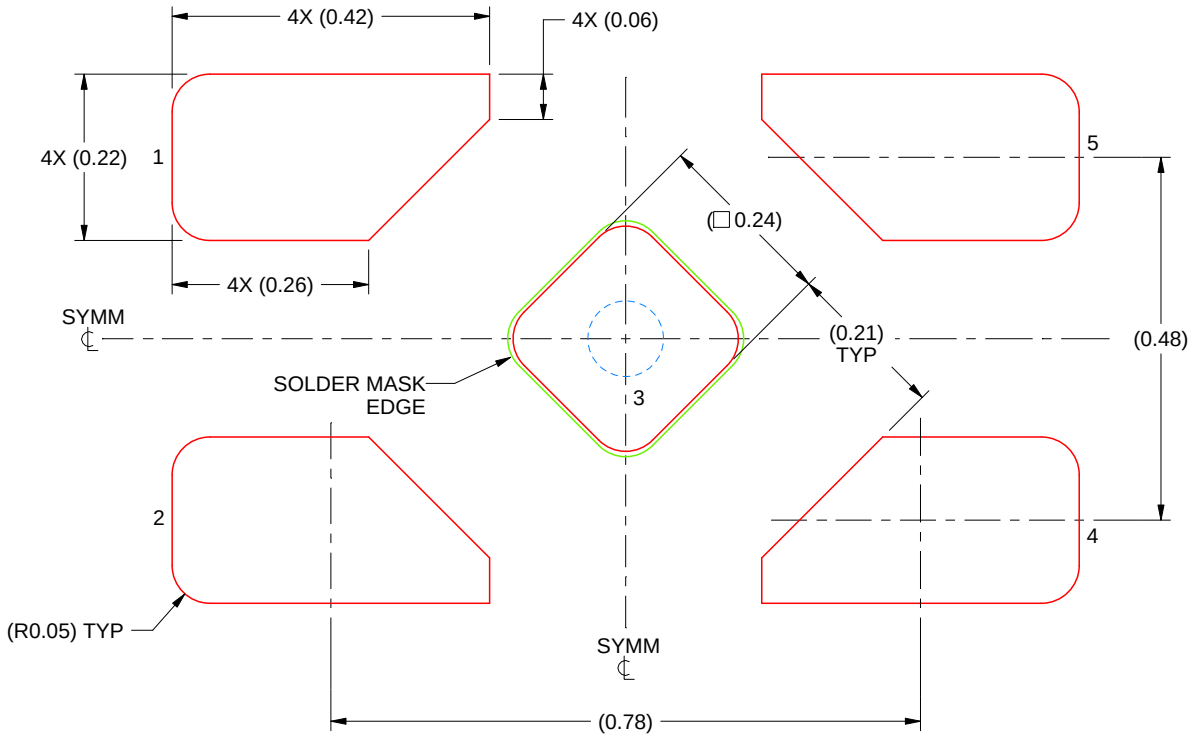
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

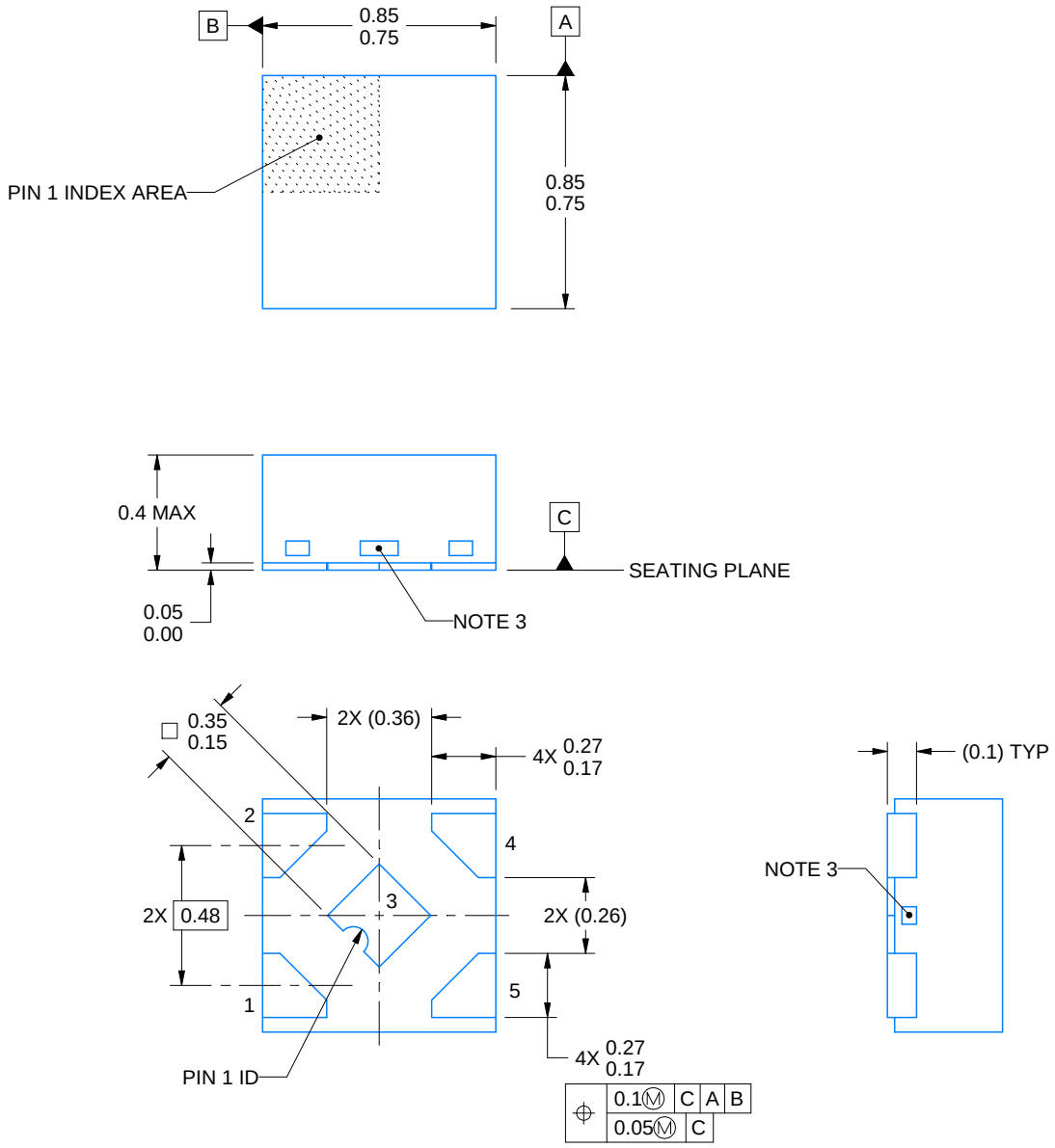
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DPW0005B

X2SON - 0.4 mm max height

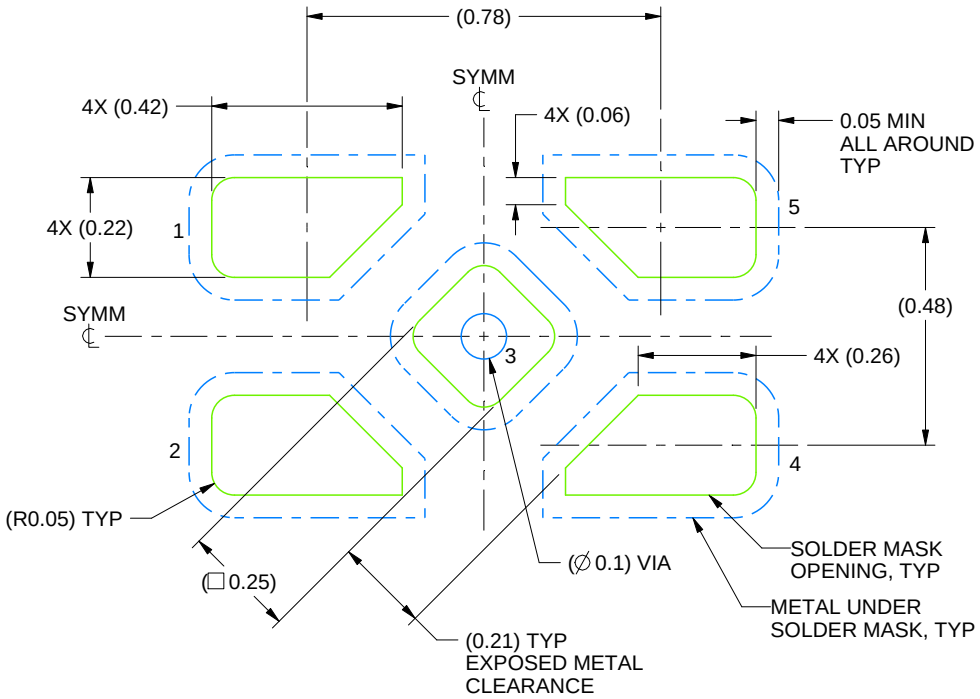
PLASTIC SMALL OUTLINE - NO LEAD



4228233/D 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

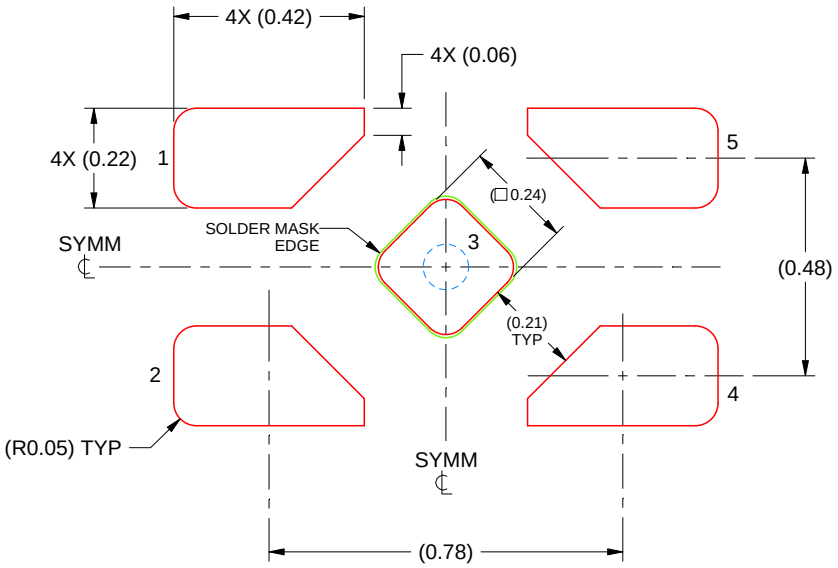


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4228233/D 09/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:60X

4228233/D 09/2023

NOTES: (continued)

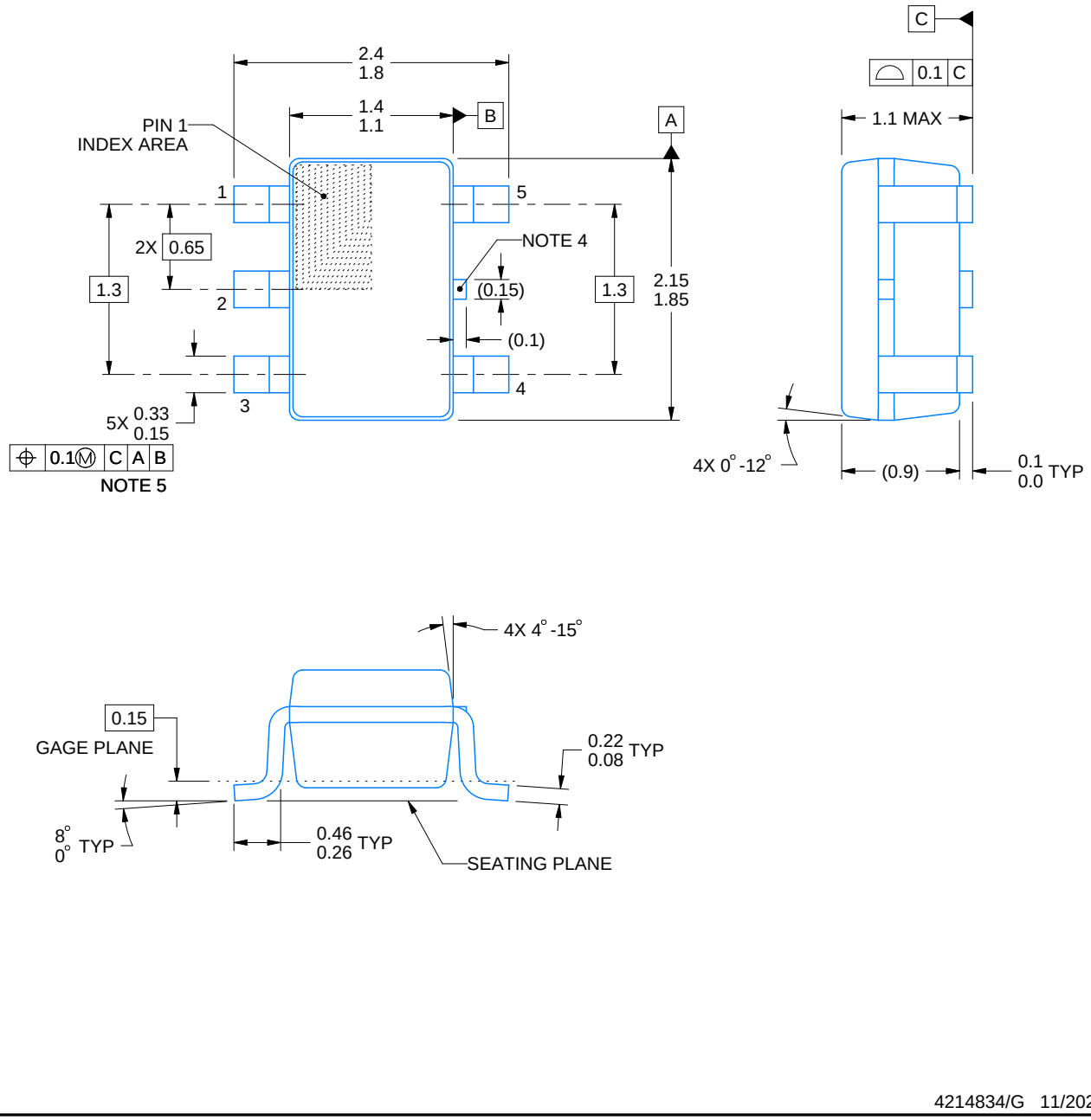
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

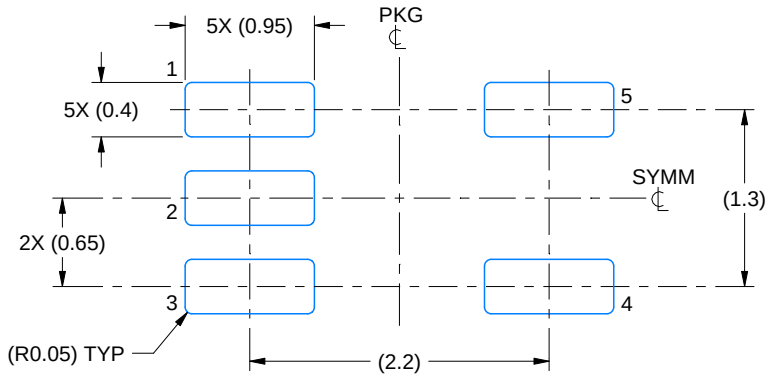
SMALL OUTLINE TRANSISTOR



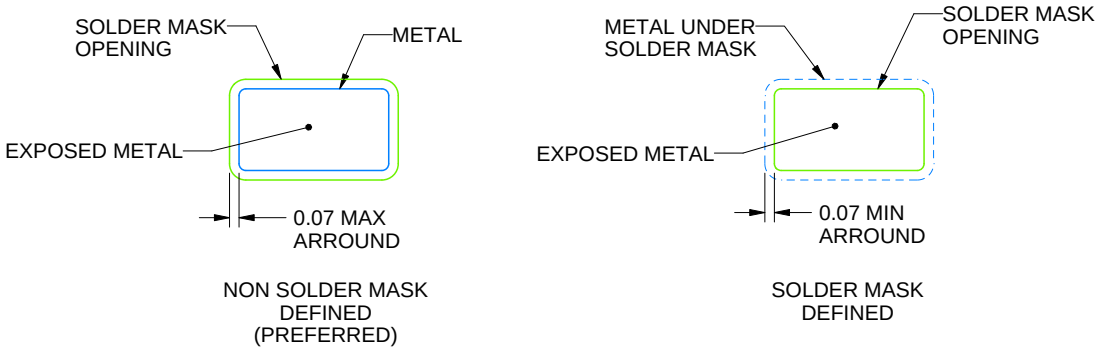
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

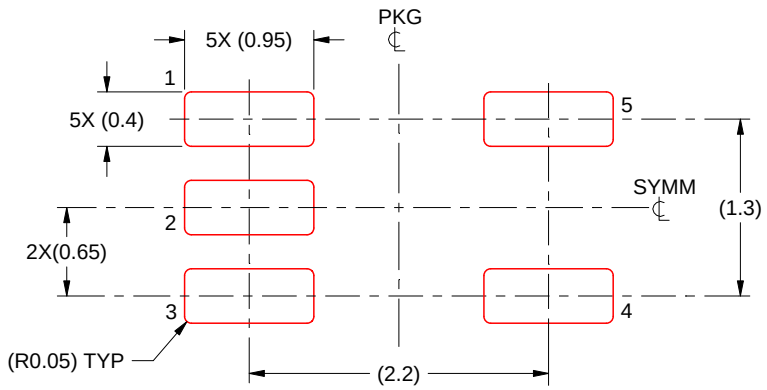


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

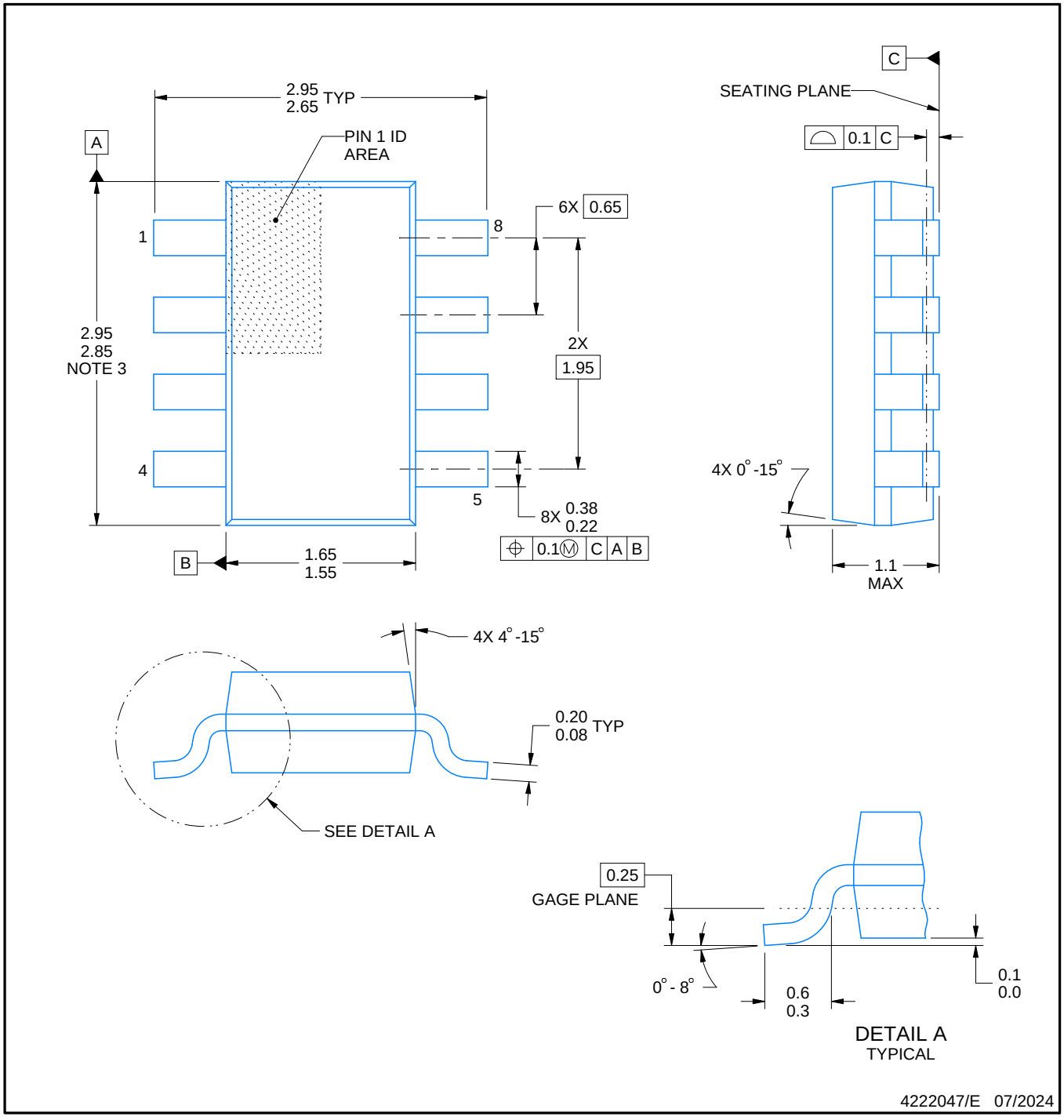
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

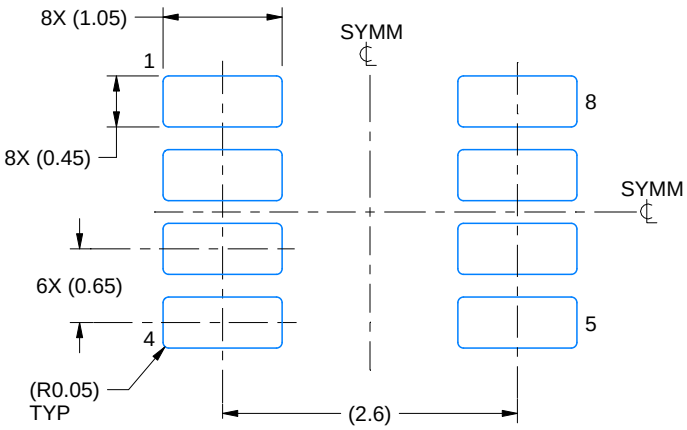
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

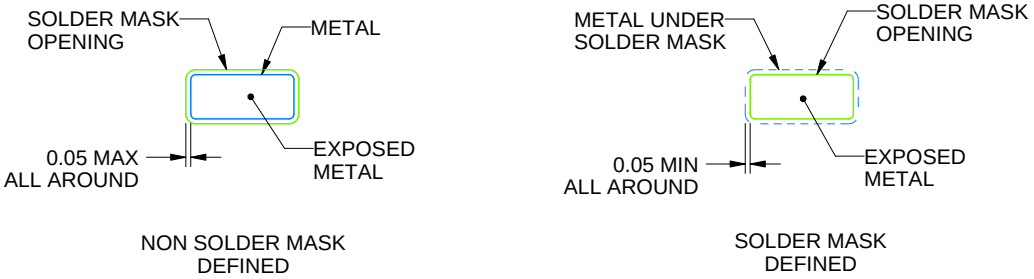


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

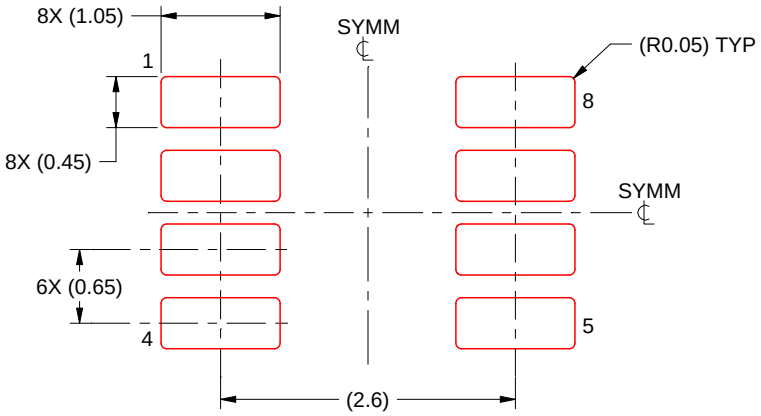
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

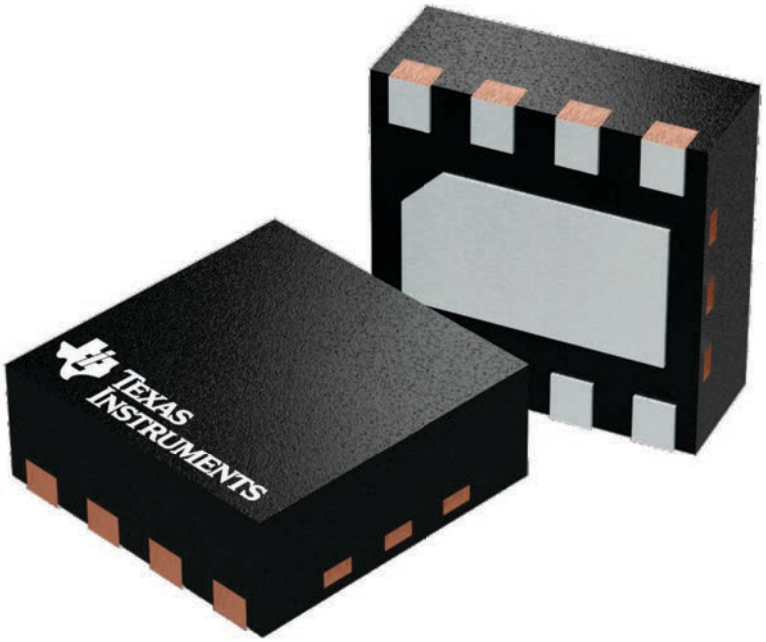
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



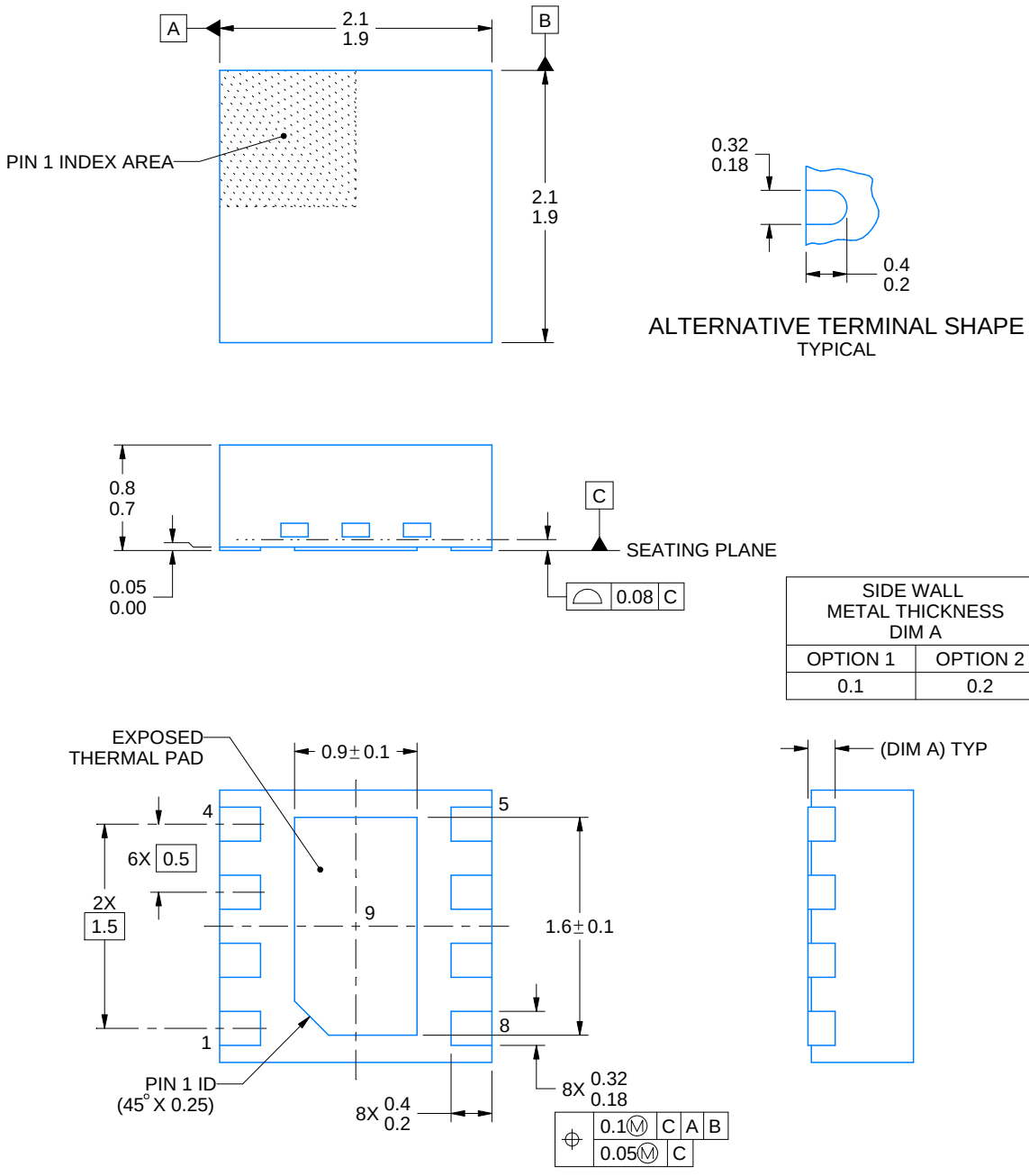
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

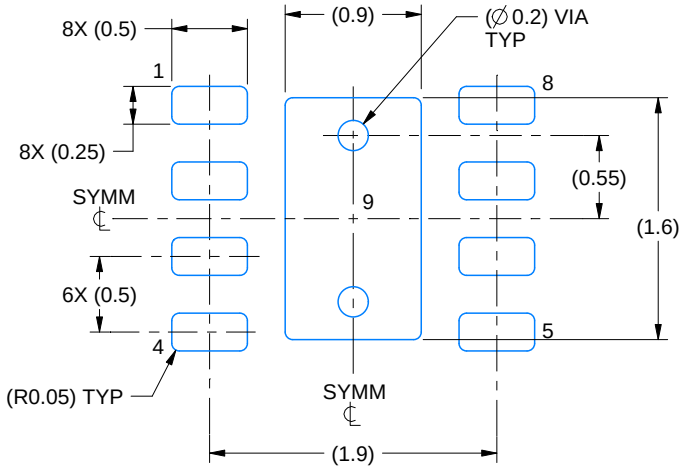
PLASTIC SMALL OUTLINE - NO LEAD



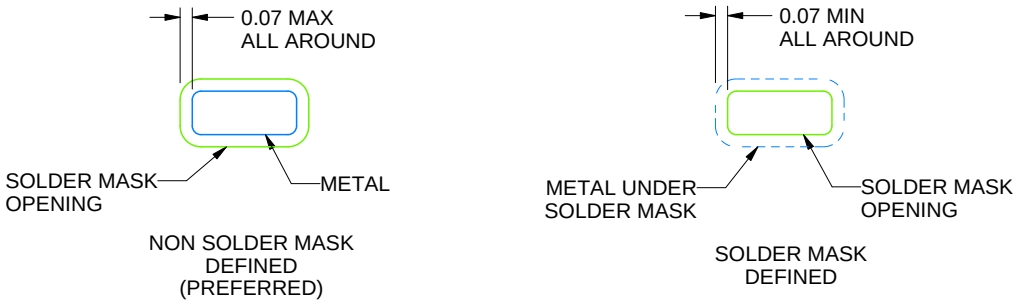
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

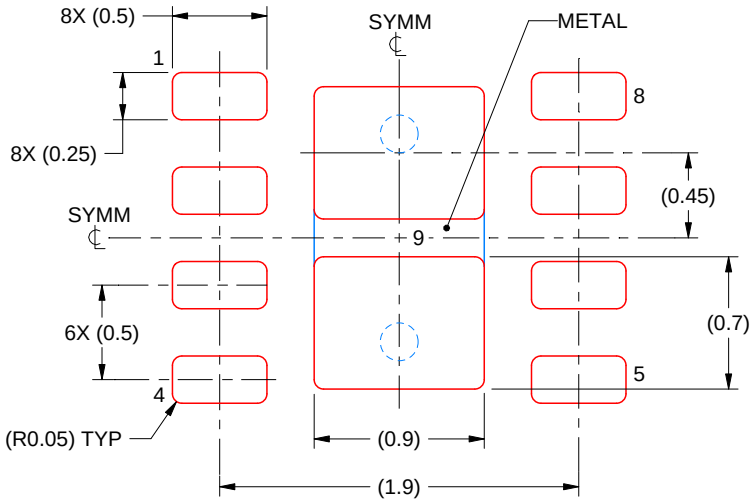


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

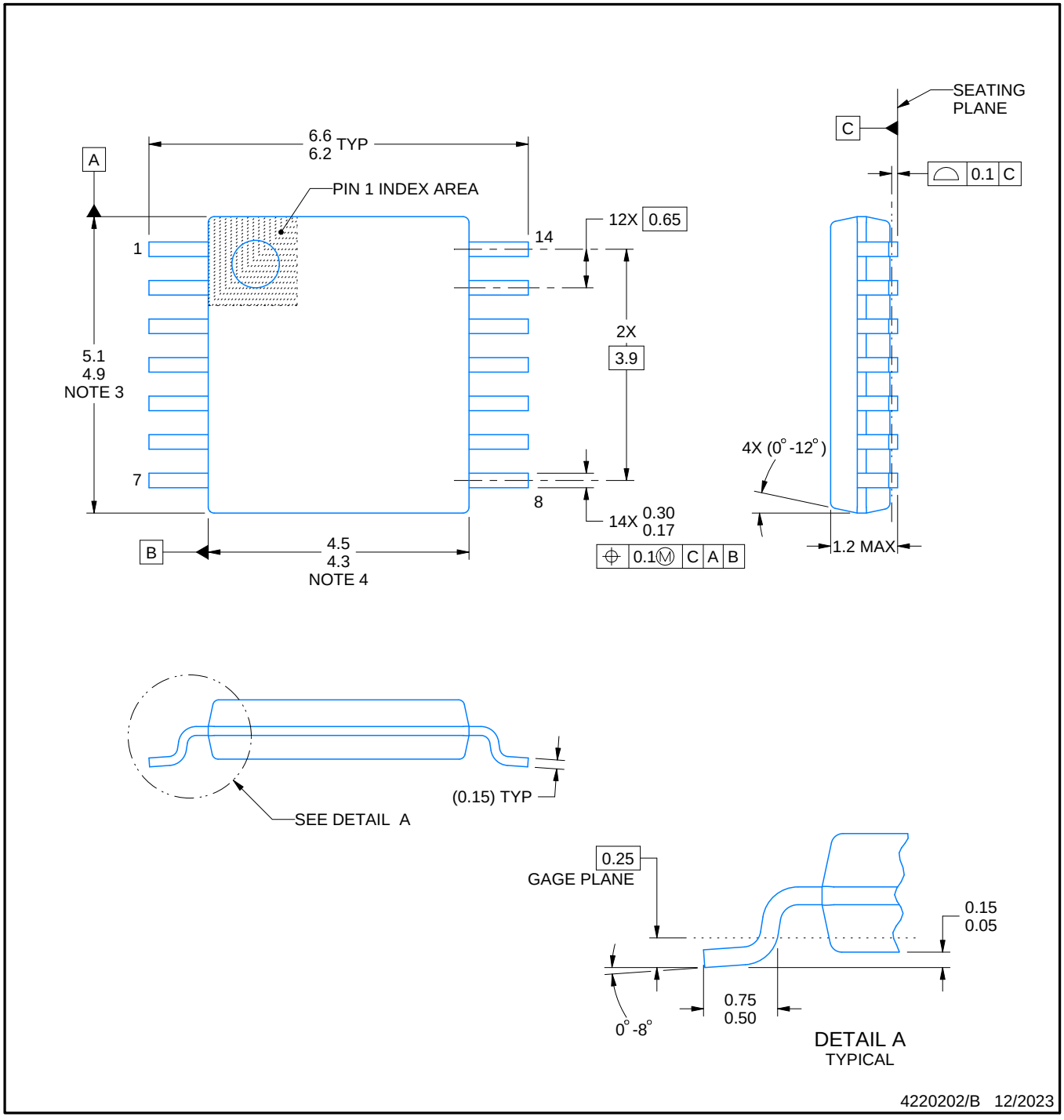
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0014A

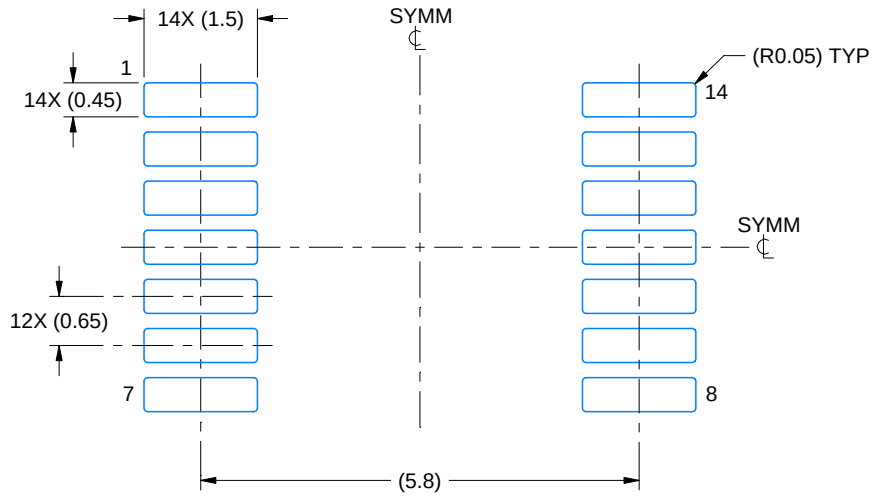
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

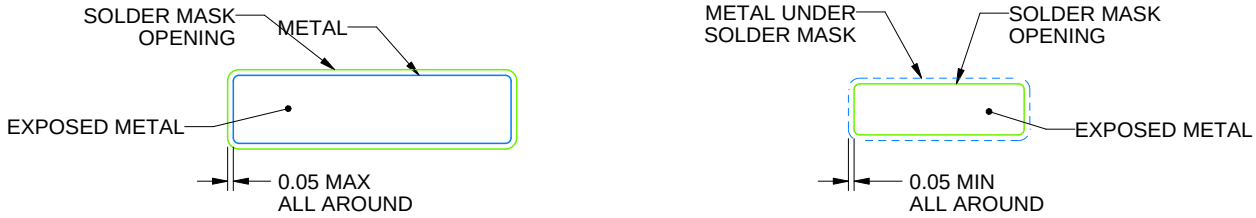


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

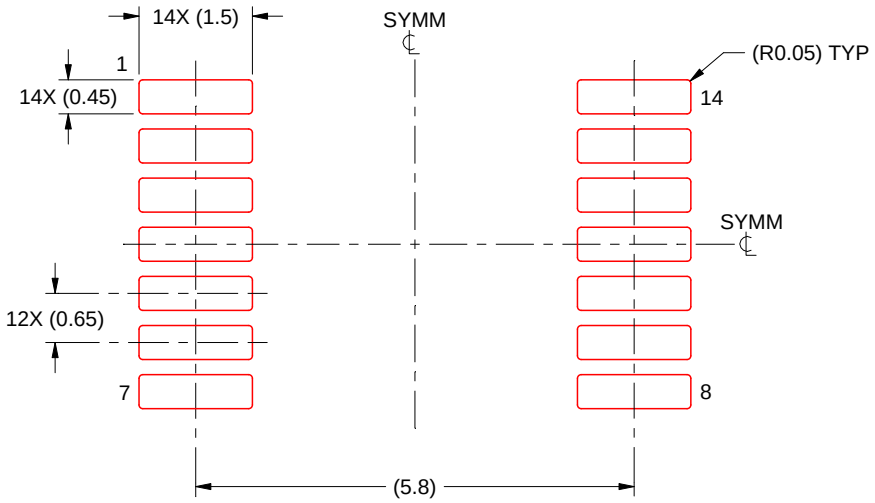


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月