用于便携式器件的双路，200mA，低 I_Q 低压降稳压器

查询样品: TLV7103318-Q1 , TLV7101828-Q1

特性

- 符合汽车应用要求
- 具有符合 **AEC-Q100** 的下列结果：
  - 器件温度 **1** 级：**-40°C** 至 **125°C** 的环境运行温度范围
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H2**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C4B**
- 极低压降：
  - 在 $I_{输出}$ **= 200mA** 并且 $V_{输出}$ **= 2.8V** 时，为 **150mV**
  - 在 $I_{输出}$ **= 100mA** 并且 $V_{输出}$ **= 2.8V** 时，为 **75mV**
  - 在 $I_{输出}$ **= 50mA** 并且 $V_{输出}$ **= 2.8V** 时，为 **40mV**
- 温度范围内的精度为 **2%**
- 每个稳压器 **35µA** 的低 I_Q
- 可提供 **1.2V** 至 **4.8V** 间的多个固定输出电压组合
- 高电源抑制比 **(PSRR)**：频率 **1kHz** 时为 **70dB**
- 与 **0.1µF**(1)高效电容一起使用时保持稳定
- 短路和热保护
- 专用 V_{REF}，以大大减少每个输出的串扰
- 采用 **1.5mm x 1.5mm** 小外形尺寸无引线 **(SON)-6** 封装

(1) 参见*应用信息*部分中的 *输入和输出电容器要求*

应用范围

- 汽车应用
- 无线听筒、智能电话、掌上电脑 **(PDA)**
- **MP3** 播放器和其它手持类产品

说明

TLV7103318-Q1 和 TLV7101828-Q1 系列双路、低压降 (LDO) 线性稳压器是具有出色线路和负载瞬态性能的低静态电流器件。 这些 LDO 设计用于功率敏感类应用。 这些器件在温度范围内提供典型值为 2% 的精度。

TLV7103318-Q1 和 TLV7101828-Q1 系列采用 1.5mm x 1.5mm SON-6 封装，并且非常适合于手持类应用。

TLV7103318-Q1
TLV7101828-Q1
1,5-mm × 1,5-mm SON-6
(TOP VIEW)

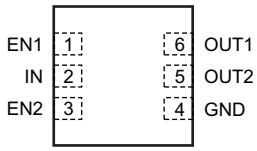
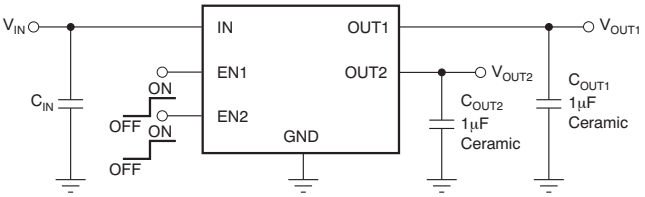


图 **1.** 典型应用电路



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE DETAILS

PRODUCT	V_{OUT} (1)
TLV710xxyyqwwwz	XX is nominal output voltage of channel 1 (for example 18 = 1.8 V). YY is nominal output voltage of channel 2 (for example 28 = 2.8V). Q is optional. Use "U" for devices with EN pin pull-up resistor, and "D" for devices with EN pin pull-down resistor. WWW is package designator. Z is package quantity. Use "R" for reel (3000 pieces), and "T" for tape (250 pieces).

(1) Output voltages from 1.2V to 4.8V in 50mV increments are available through the use of innovative factory OTP programming; minimum order quantities may apply. Contact factory for details and availability.

ORDERING INFORMATION(1)

ORDERABLE PART NUMBER	T_A	PACKAGE(2)		TOP-SIDE MARKING
TLV7103318QDSERQ1	–40°C to 125°C	WSON-DSE	Reel of 3000	ZD
TLV7101828QDSERQ1				CP

(1) For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

At T_A = –40°C to 125°C (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	IN	–0.3	6	V
	EN	–0.3	V_{IN} 0.3	V
	OUT	–0.3	6	V
Current	OUT	Internally limited		A
Output short-circuit duration		Indefinite		s
Temperature	Operating ambient, T_A	–40	125	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	–55	150	°C
Electrostatic Discharge (ESD) rating	Human-Body Model (HBM) AEC-Q100 Classification Level H2		2	kV
	Charged-Device Model (CDM) AEC-Q100 Classification Level C4B		750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages with respect to ground.

THERMAL INFORMATION

THERMAL METRIC(1)		TLV7103318-Q1, TLV7101828-Q1 DSE 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	190.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	94.9	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	149.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	6.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	152.8	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	N/A	°C/W

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(6) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

RECOMMENDED OPERATING CONDITIONS

At T_A = –40°C to 125ºC, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN1} = V_{EN2} = 0.9 V, and C_{OUT1} = C_{OUT2} = 1 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TLV710xxx8-Q1 MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			2		5.5	V
V_O	Output voltage range			1.2		4.8	V
V_{OUT}	DC output accuracy	–40°C ≤ T_A ≤ 125°C		–2		2	%
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤			1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 200 mA			5	15	mV
V_{DO}	Dropout voltage	V_{IN} = 0.98 V × $V_{OUT(NOM)}$, I_{OUT} = 200 mA, 2V ≤ V_{OUT} < 2.4V			200	285	mV
		V_{IN} = 0.98 V × $V_{OUT(NOM)}$, I_{OUT} = 200 mA, 2.4 V ≤ V_{OUT} < 2.8 V			175	250	mV
		V_{IN} = 0.98 V × $V_{OUT(NOM)}$, I_{OUT} = 200 mA, 2.8 V ≤ V_{OUT} < 3.3 V			150	215	mV
		V_{IN} = 0.98 V × $V_{OUT(NOM)}$, I_{OUT} = 200 mA, 3.3 V ≤ V_{OUT} ≤ 4.8 V			140	200	mV
I_{CL}	Output current limit	V_{OUT} = 0.9V × $V_{OUT(NOM)}$		220	350	550	mA
I_Q	Quiescent current	V_{EN1} = high, V_{EN2} = low, I_{OUT1} = 0 mA			35		µA
		V_{EN1} = low, V_{EN2} = high, I_{OUT2} = 0 mA			35		µA
		V_{EN1} = high, V_{EN2} = high, I_{OUT} = 0 mA			70	110	µA
I_{GND}	Ground pin current	I_{OUT1} = I_{OUT2} = 200mA			360		µA
$I_{SHUTDOWN}$	Shutdown current	$V_{EN1,2}$ ≤ 0.4 V, 2 V ≤ V_{IN} ≤ 4.5 V			2.5	4	µA
PSRR	Power-supply rejection ratio	V_{OUT} = 1.8 V	f = 10 Hz		80		dB
			f = 100 Hz		75		dB
			f = 1k Hz		70		dB
			f = 10 kHz		70		dB
			f = 100 kHz		50		dB
V_N	Output noise voltage	BW = 100 Hz to 100 kHz, V_{OUT} = 1.8 V			48		μV_{RMS}
t_{STR}	Startup time(1)	C_{OUT} = 1 µF, I_{OUT} = 200 mA			100		µs
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V

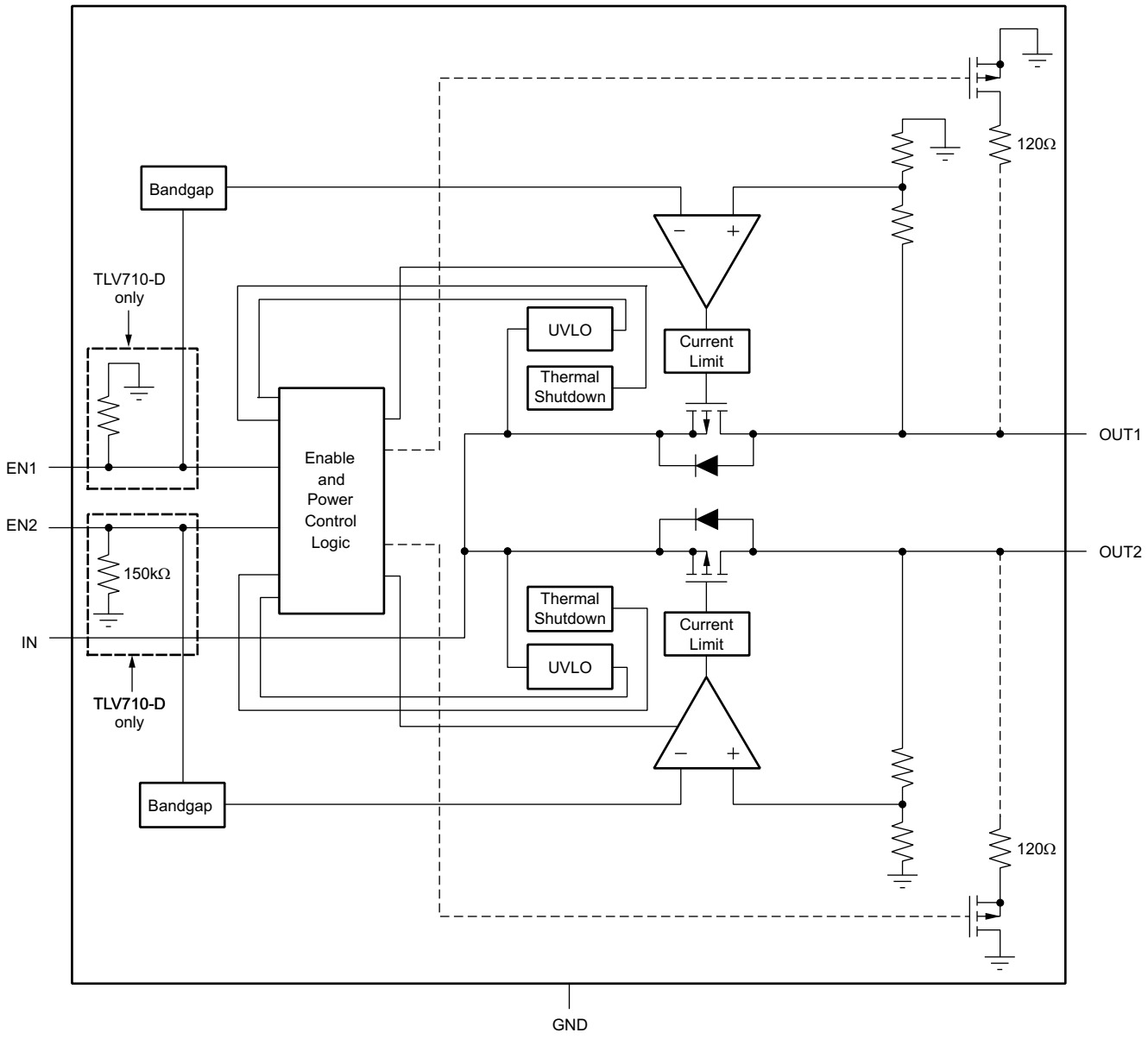
(1) Startup time = time from EN assertion to 0.98 x $V_{OUT(NOM)}$.

RECOMMENDED OPERATING CONDITIONS (continued)

At T_A = –40°C to 125ºC, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V (whichever is greater), I_{OUT} = 10 mA, V_{EN1} = V_{EN2} = 0.9 V, and C_{OUT1} = C_{OUT2} = 1 µF, unless otherwise noted.

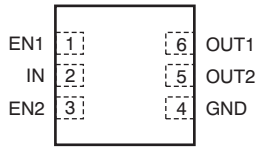
PARAMETER		TEST CONDITIONS	TLV710xxx8-Q1			UNIT
			MIN	TYP	MAX	
V_{LO}	Enable low (shutdown)		0		0.4	V
I_{EN}	Enable pin current, enabled	TLV7103318-Q1, TLV7101828-Q1		0.04		µA
		TLV710-D		6		µA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
T_A	Operating ambient temperature		–40		125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		145		°C

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

DSE PACKAGE
1.5mm x 1.5mm SON-6
(TOP VIEW)



PIN DESCRIPTIONS

NAME	PIN NO.	DESCRIPTION
EN1	1	Enable pin for regulator 1. Driving EN1 over 0.9V turns on regulator 1. Driving EN below 0.4V puts regulator 1 into shutdown mode.
IN	2	Input pin. A small capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
EN2	3	Enable pin for regulator 2. Driving EN2 over 0.9V turns on regulator 2. Driving EN2 below 0.4V puts regulator2 into shutdown mode.
GND	4	Ground pin.
OUT2	5	Regulated output voltage pin. A small 1µF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
OUT1	6	Regulated output voltage pin. A small 1µF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

TYPICAL CHARACTERISTICS

Over operating temperature range of T_A = –40°C to 125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Typical values are at T_A = 25°C.

LINE REGULATION: V_{OUT1} (TLV7101828-Q1)

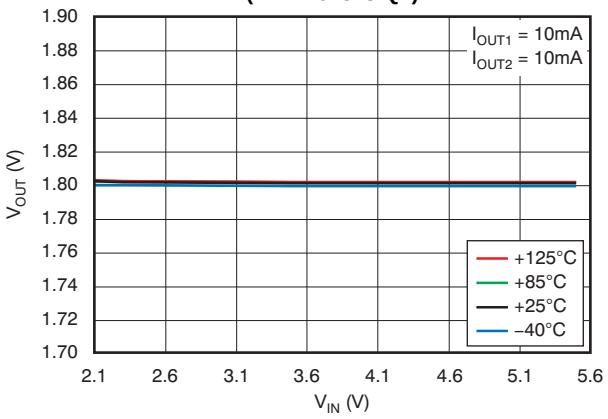


Figure 2.

LINE REGULATION: V_{OUT2} (TLV7101828-Q1)

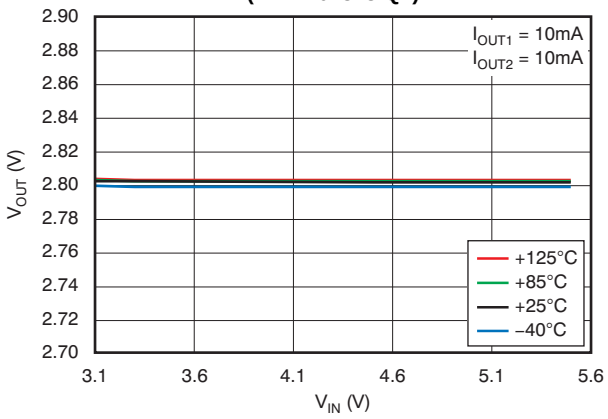


Figure 3.

LINE REGULATION: V_{OUT1} (TLV7101828-Q1)

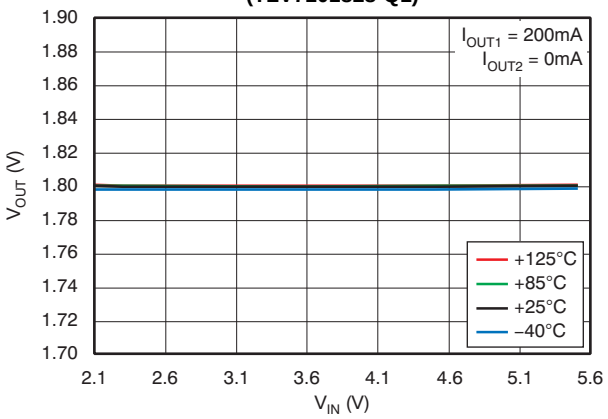


Figure 4.

LINE REGULATION: V_{OUT2} (TLV7101828-Q1)

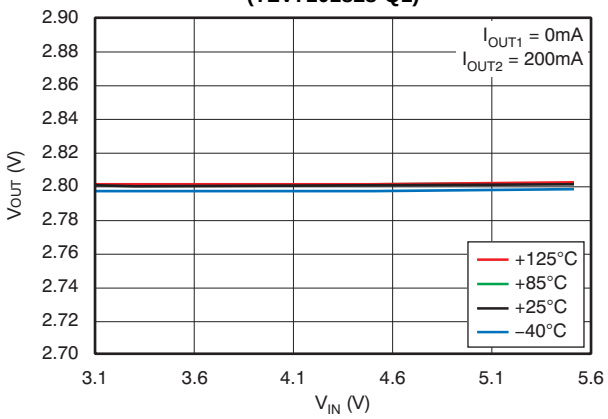


Figure 5.

LINE REGULATION: V_{OUT1} (TLV7103333)

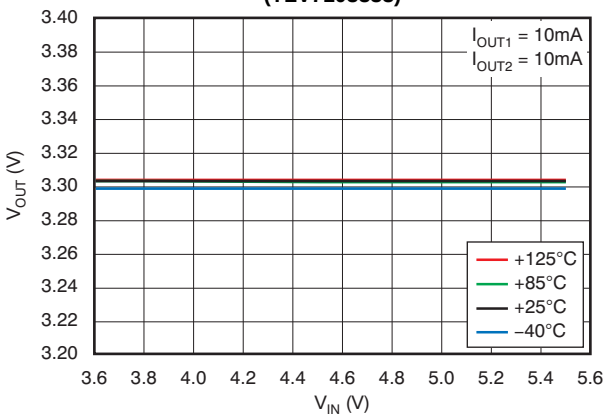


Figure 6.

LINE REGULATION: V_{OUT2} (TLV7103333)

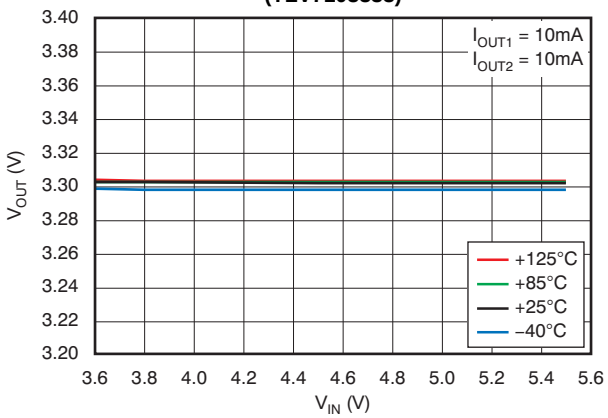


Figure 7.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_A = –40°C to 125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Typical values are at T_A = 25°C.

LINE REGULATION: V_{OUT1} (TLV7103333)

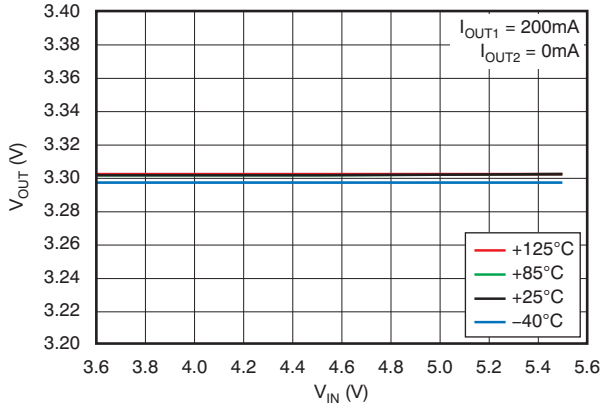


Figure 8.

LINE REGULATION: V_{OUT2} (TLV7103333)

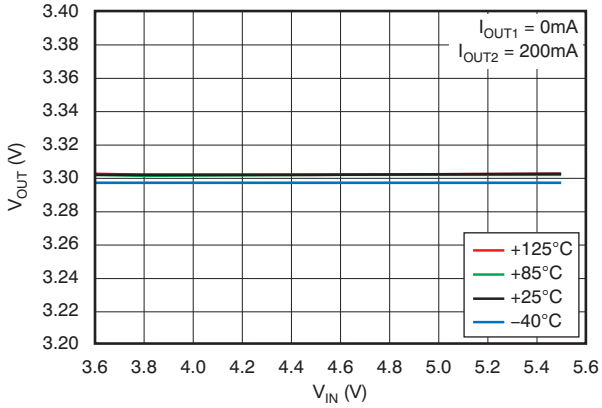


Figure 9.

LOAD REGULATION: V_{OUT1} (TLV7101828-Q1)

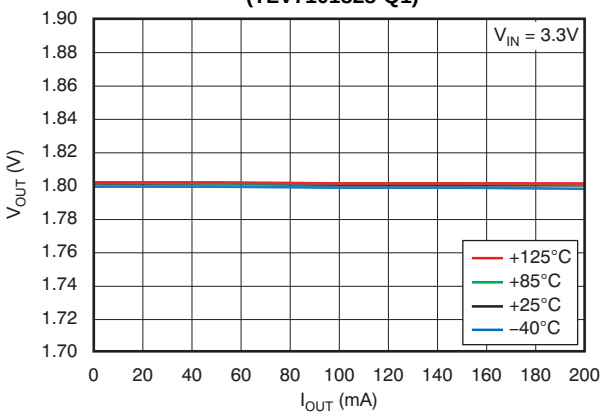


Figure 10.

LOAD REGULATION: V_{OUT2} (TLV7101828-Q1)

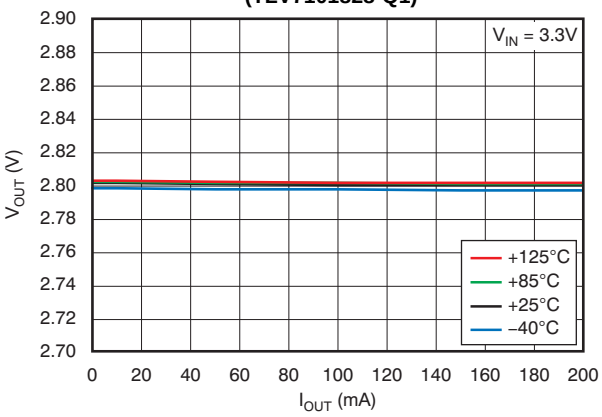


Figure 11.

LOAD REGULATION: V_{OUT1} (TLV7103333)

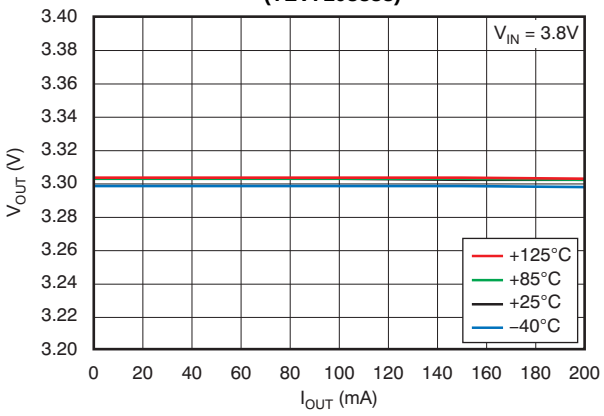


Figure 12.

LOAD REGULATION: V_{OUT2} (TLV7103333)

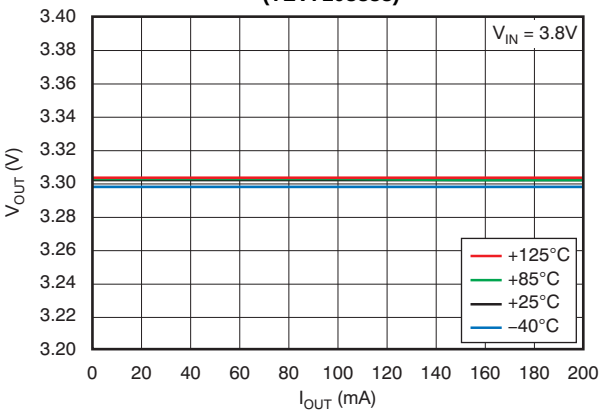


Figure 13.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_A = –40°C to 125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Typical values are at T_A = 25°C.

DROPOUT VOLTAGE versus INPUT VOLTAGE

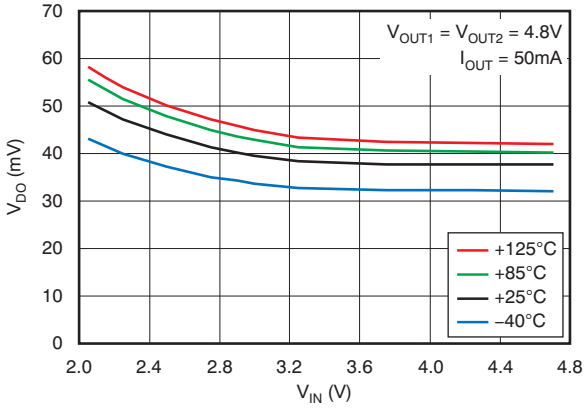


Figure 14.

DROPOUT VOLTAGE versus INPUT VOLTAGE

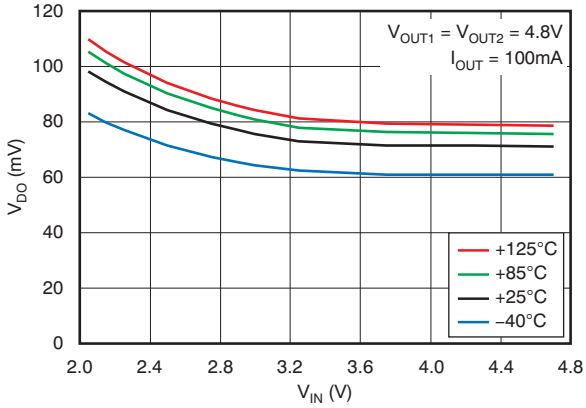


Figure 15.

DROPOUT VOLTAGE versus INPUT VOLTAGE

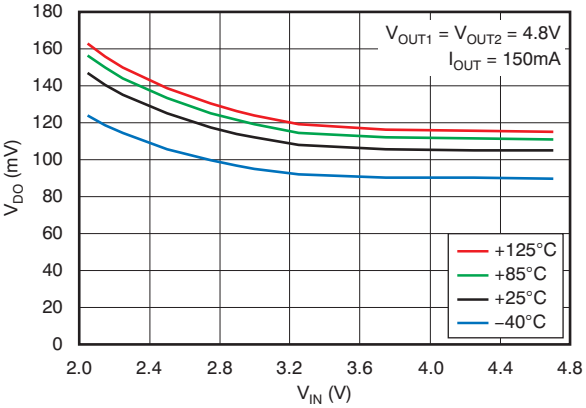


Figure 16.

DROPOUT VOLTAGE versus INPUT VOLTAGE

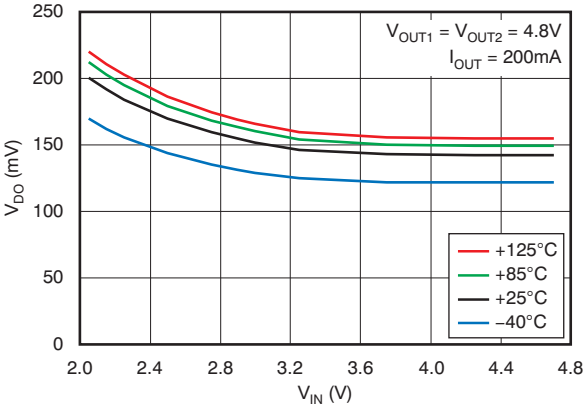


Figure 17.

DROPOUT VOLTAGE versus OUTPUT CURRENT: V_{OUT2} (TLV7101828-Q1)

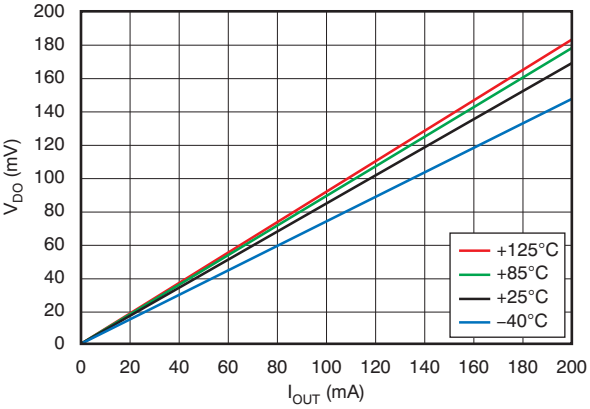


Figure 18.

DROPOUT VOLTAGE versus OUTPUT CURRENT: V_{OUT1}/V_{OUT2} (TLV7103333)

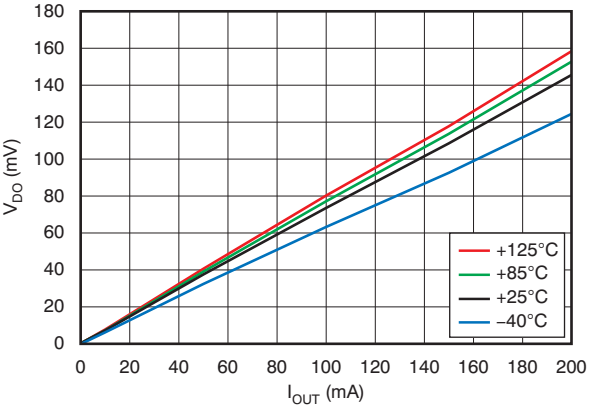


Figure 19.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_A = –40°C to 125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Typical values are at T_A = 25°C.

OUTPUT VOLTAGE versus TEMPERATURE: V_{OUT1} (TLV7101828-Q1)

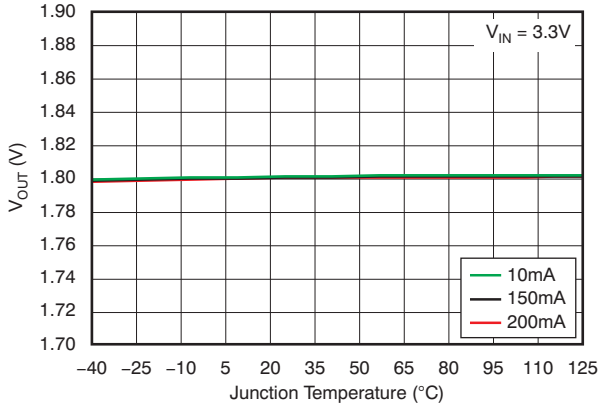


Figure 20.

OUTPUT VOLTAGE versus TEMPERATURE: V_{OUT2} (TLV7101828-Q1)

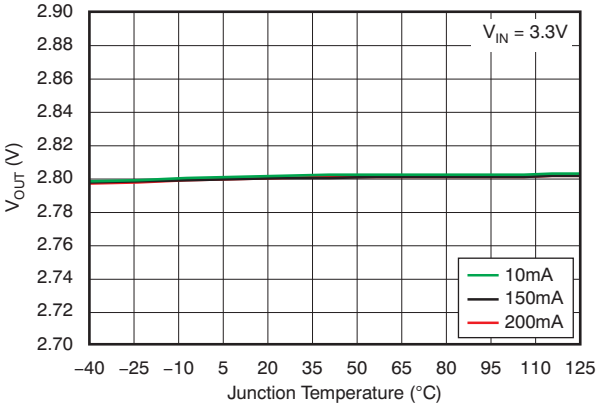


Figure 21.

OUTPUT VOLTAGE versus TEMPERATURE: V_{OUT1} (TLV7103333)

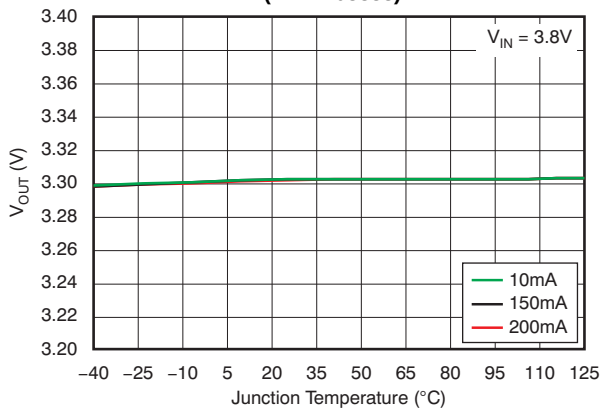


Figure 22.

OUTPUT VOLTAGE versus TEMPERATURE: V_{OUT2} (TLV7103333)

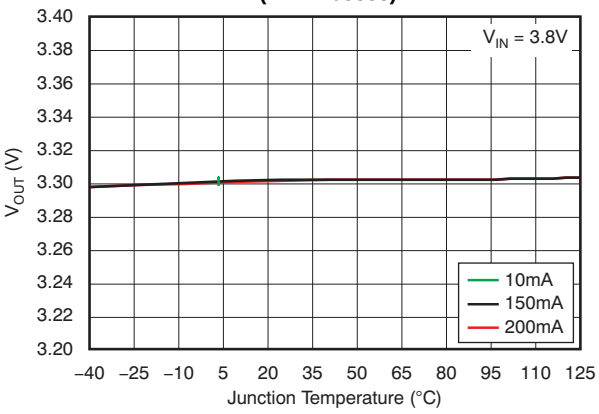


Figure 23.

GROUND PIN CURRENT versus INPUT VOLTAGE: I_{Q1} (TLV7101828)

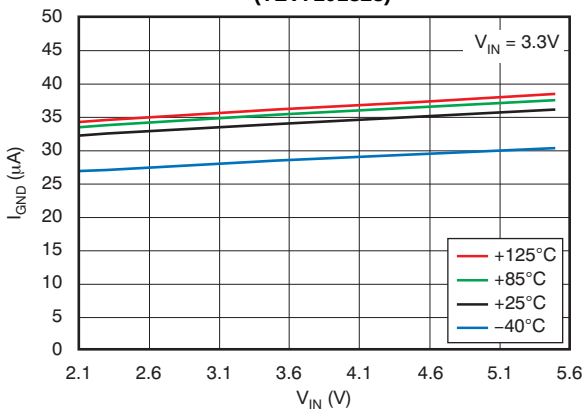


Figure 24.

GROUND PIN CURRENT versus INPUT VOLTAGE: I_{Q2} (TLV7101828)

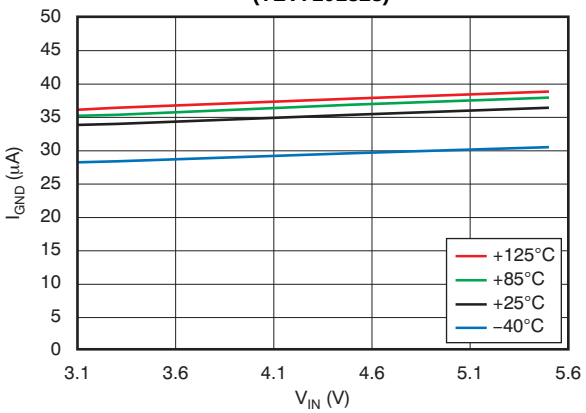


Figure 25.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_A = –40°C to 125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Typical values are at T_A = 25°C.

GROUND PIN CURRENT versus INPUT VOLTAGE: I_{Q1} (TLV7103333)

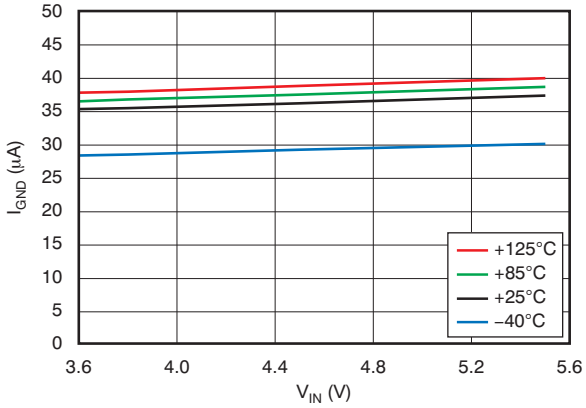


Figure 26.

GROUND PIN CURRENT versus INPUT VOLTAGE: I_{Q2} (TLV7103333)

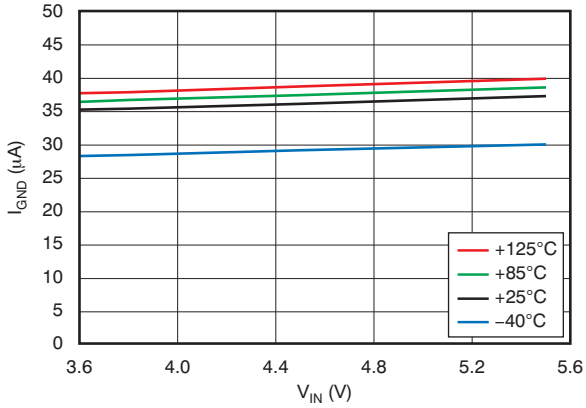


Figure 27.

GROUND PIN CURRENT versus LOAD: I_{Q1} (TLV7101828)

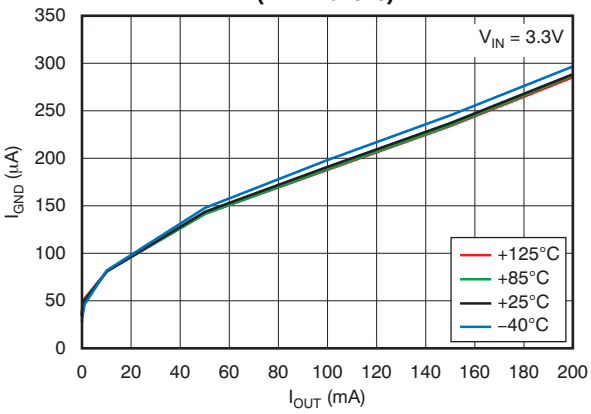


Figure 28.

GROUND PIN CURRENT versus LOAD: I_{Q2} (TLV7103333)

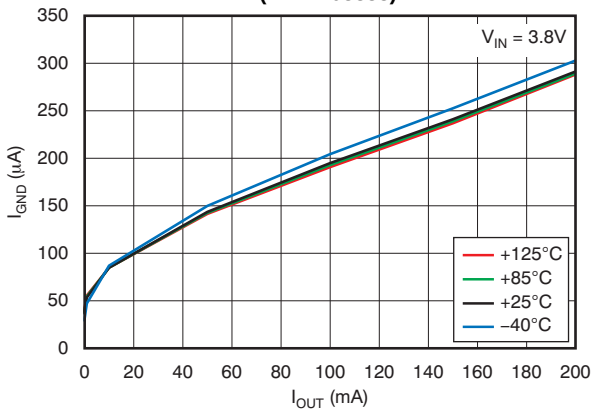


Figure 29.

SHUTDOWN CURRENT versus INPUT VOLTAGE (TLV7101828)

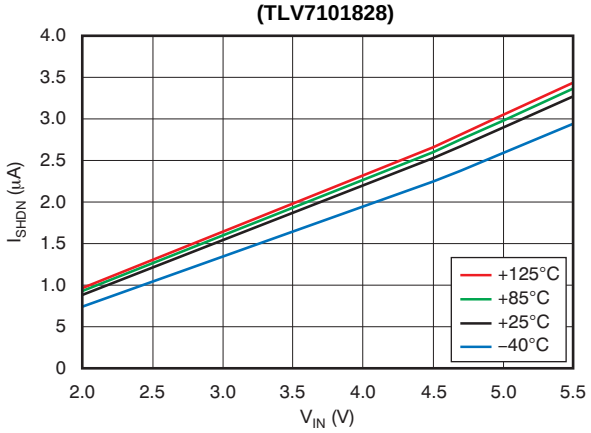


Figure 30.

SHUTDOWN CURRENT versus INPUT VOLTAGE (TLV7103333)

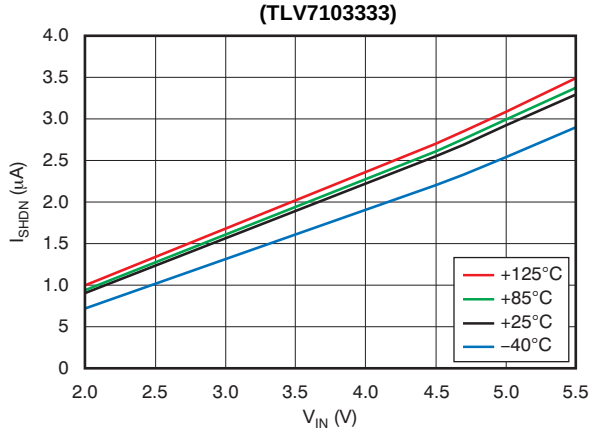


Figure 31.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_A = –40°C to 125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Typical values are at T_A = 25°C.

CURRENT LIMIT versus INPUT VOLTAGE: I_{CL1} (TLV7101828)

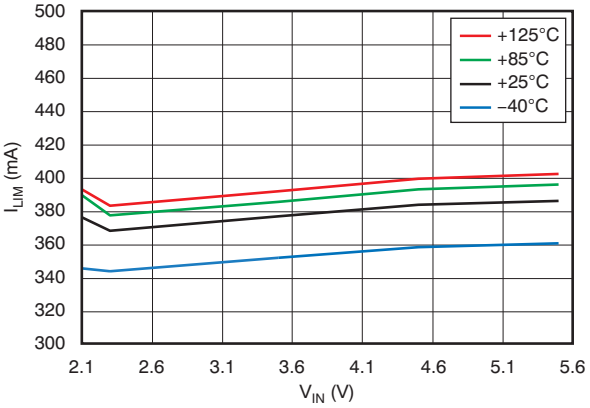


Figure 32.

CURRENT LIMIT versus INPUT VOLTAGE: I_{CL2} (TLV7101828)

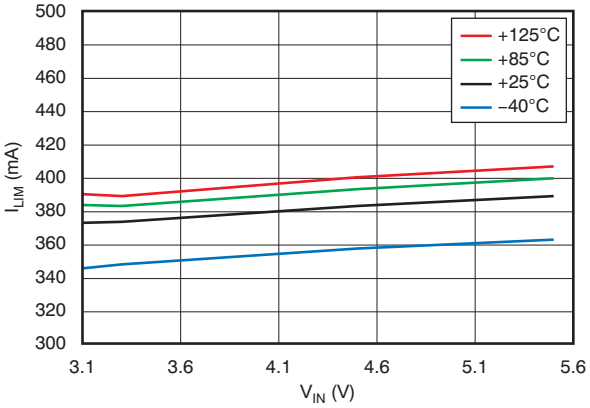


Figure 33.

CURRENT LIMIT versus INPUT VOLTAGE: I_{CL1} (TLV7103333)

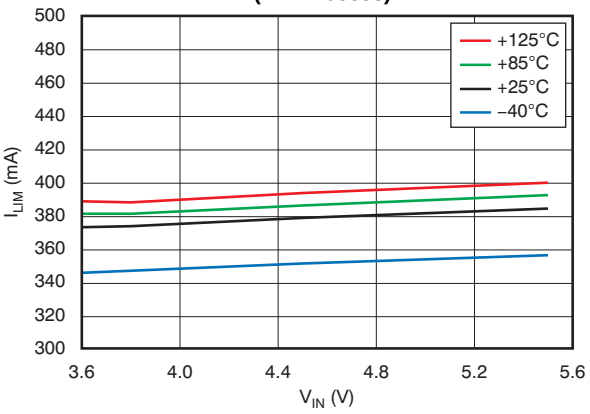


Figure 34.

CURRENT LIMIT versus INPUT VOLTAGE: I_{CL2} (TLV7103333)

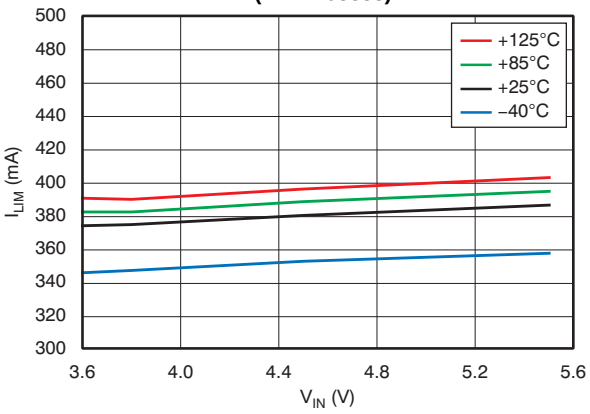


Figure 35.

POWER-SUPPLY RIPPLE REJECTION versus FREQUENCY (TLV7101828)

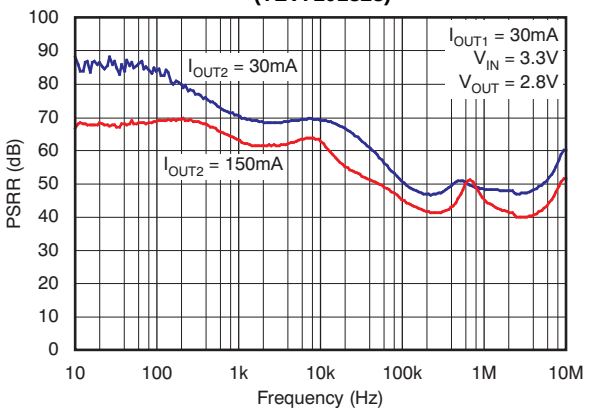


Figure 36.

POWER-SUPPLY RIPPLE REJECTION versus FREQUENCY (TLV7103333)

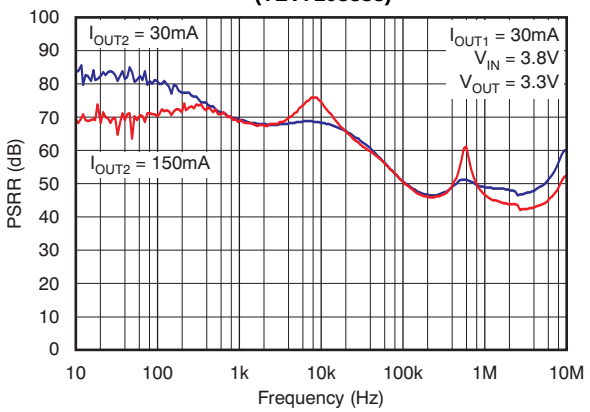


Figure 37.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_A = –40°C to 125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Typical values are at T_A = 25°C.

OUTPUT SPECTRAL NOISE DENSITY versus FREQUENCY (TLV7101828)

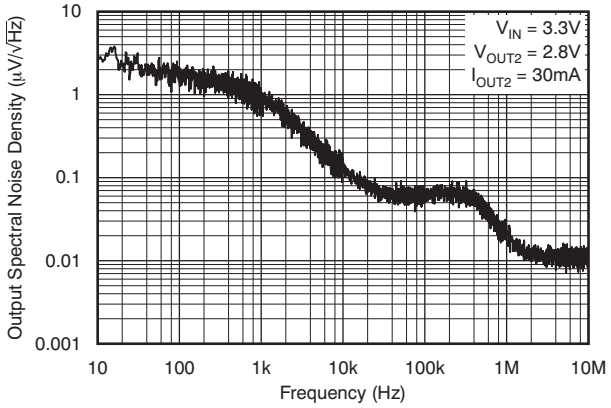


Figure 38.

OUTPUT SPECTRAL NOISE DENSITY versus FREQUENCY (TLV7103333)

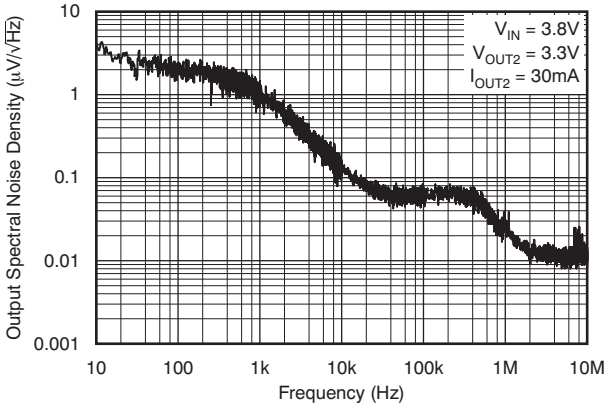


Figure 39.

LINE TRANSIENT RESPONSE
V_{OUT1} = 1.2 V, V_{OUT2} = 1.2 V

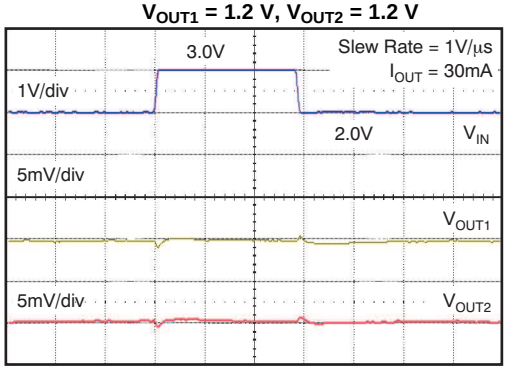


Figure 40.

LINE TRANSIENT RESPONSE
V_{OUT1} = 1.2V, V_{OUT2} = 1.2V

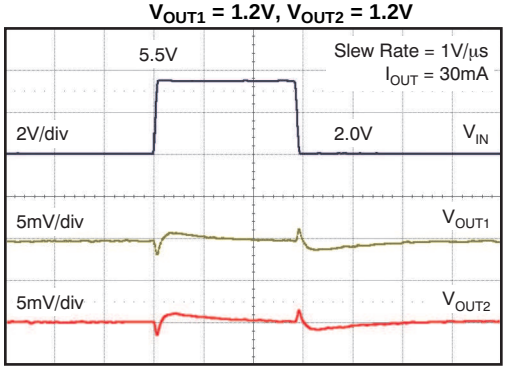


Figure 41.

LINE TRANSIENT RESPONSE
V_{OUT1} = 1.8V, V_{OUT2} = 2.8V

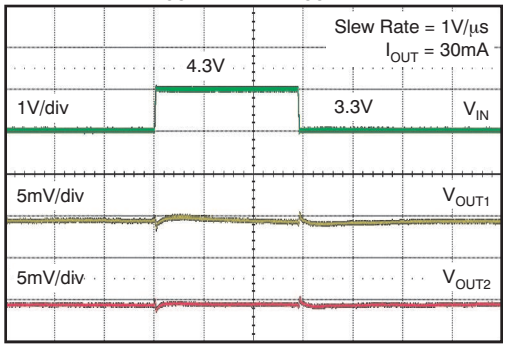


Figure 42.

LINE TRANSIENT RESPONSE
V_{OUT1} = 1.8V, V_{OUT2} = 2.8V

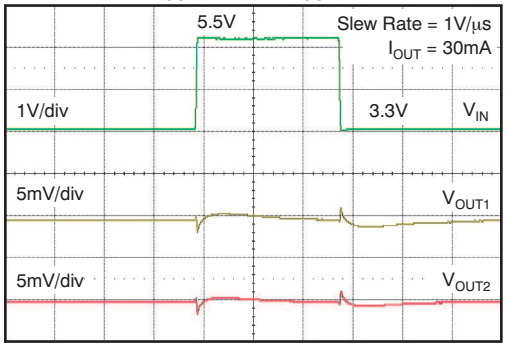


Figure 43.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_A = –40°C to 125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Typical values are at T_A = 25°C.

LINE TRANSIENT RESPONSE
V_{OUT1} = 4.8V, V_{OUT2} = 4.8V

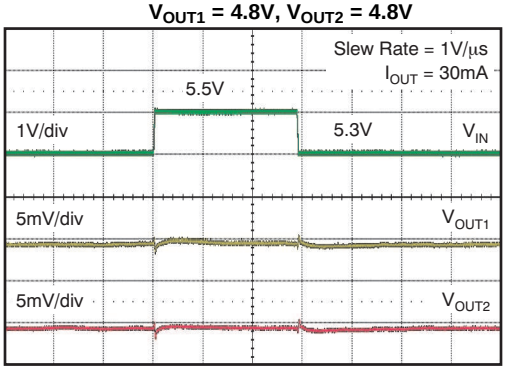


Figure 44.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 1.2V, V_{OUT2} = 1.2V

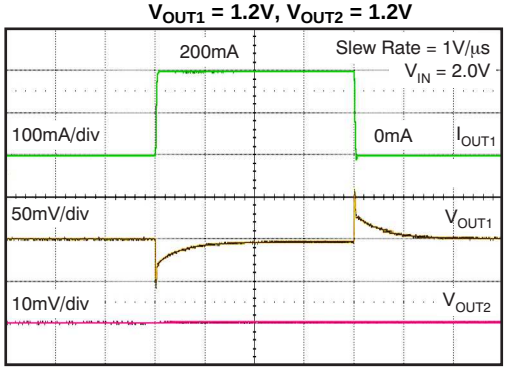


Figure 45.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 1.2V, V_{OUT2} = 1.2V

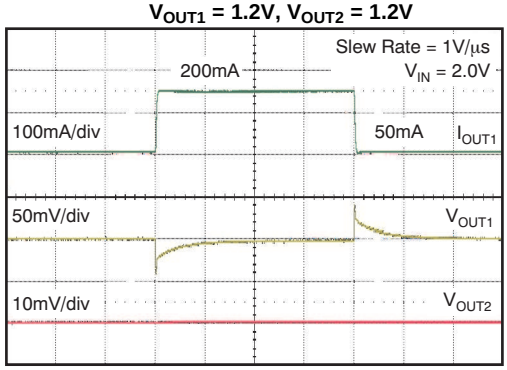


Figure 46.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 1.8V, V_{OUT2} = 2.8V

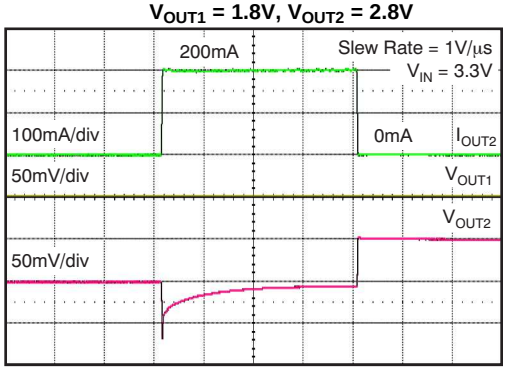


Figure 47.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 1.8V, V_{OUT2} = 2.8V

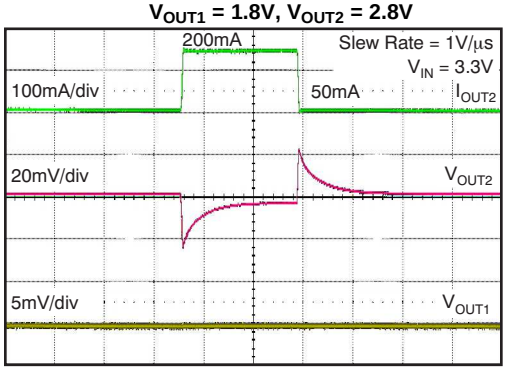
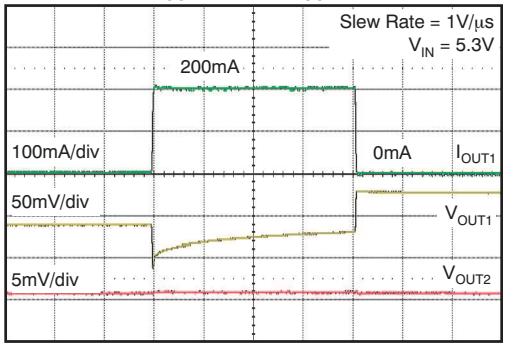


Figure 48.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_A = –40°C to 125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Typical values are at T_A = 25°C.

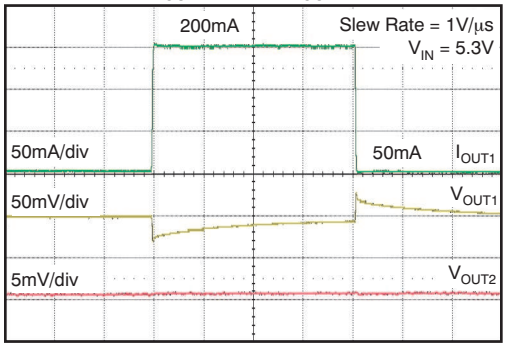
LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 4.8V, V_{OUT2} = 4.8V



Time (50µs/div)

Figure 49.

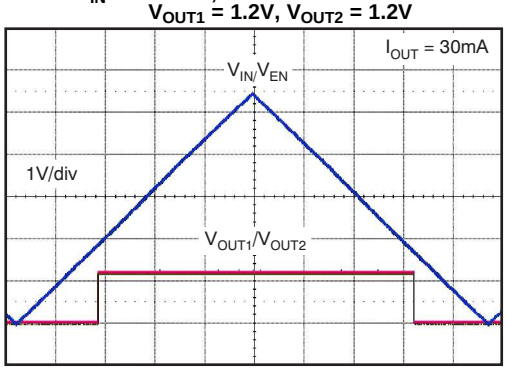
LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 4.8V, V_{OUT2} = 4.8V



Time (50µs/div)

Figure 50.

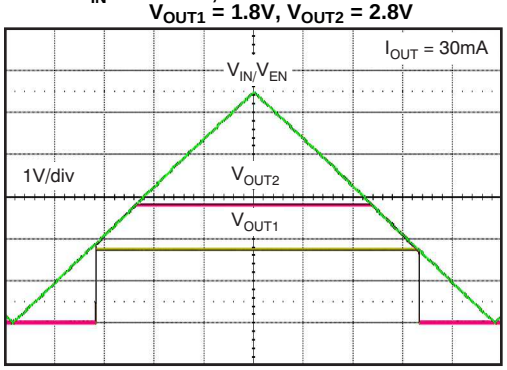
V_{IN} RAMP UP, RAMP DOWN RESPONSE
V_{OUT1} = 1.2V, V_{OUT2} = 1.2V



Time (200ms/div)

Figure 51.

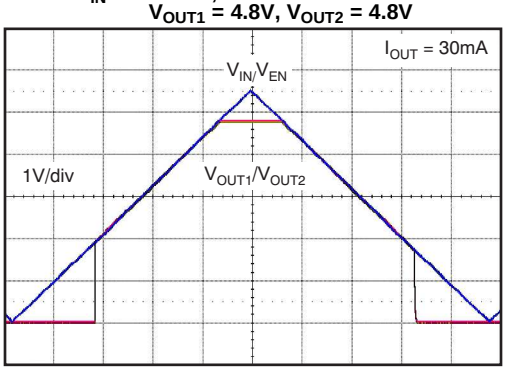
V_{IN} RAMP UP, RAMP DOWN RESPONSE
V_{OUT1} = 1.8V, V_{OUT2} = 2.8V



Time (200ms/div)

Figure 52.

V_{IN} RAMP UP, RAMP DOWN RESPONSE
V_{OUT1} = 4.8V, V_{OUT2} = 4.8V



Time (200ms/div)

Figure 53.

APPLICATION INFORMATION

The TLV7103318-Q1 and TLV7101828-Q1 devices belong to a new family of next-generation, value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These features, combined with low noise, very good PSRR with little (V_{IN} to V_{OUT}) headroom, make these devices ideal for RF portable applications. This family of LDO regulators offers current limit and thermal protection, and is specified from –40°C to 125°C.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

1.0µF X5R- and X7R-type ceramic capacitors are recommended because they have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV7103318-Q1 and TLV7101828-Q1 are designed to be stable with an effective capacitance of 0.1 µF or larger at the output. Thus, the device would also be stable with capacitors of other dielectrics, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the device sees under operating bias voltage and temperature conditions (that is, the capacitance after taking bias voltage and temperature derating into consideration.)

In addition to allowing the use of cost-effective dielectrics, these devices also enable using smaller footprint capacitors that have a higher derating in size-constrained applications.

Note that using a 0.1-µF rating capacitor at the output of the LDO regulator does not ensure stability because the effective capacitance under operating conditions would be less than 0.1 µF. The maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1.0µF low ESR capacitor across the IN and GND pins of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast-rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is more than 2Ω, a 0.1µF input capacitor may be necessary to ensure stability.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The TLV7103318-Q1 and TLV7101828-Q1 internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$.

The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device is turned off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details. The PMOS pass element in the TLV7103318-Q1 and TLV7101828-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when EN pin goes above 0.9V. This relatively lower value of voltage needed to turn the LDO regulator on can be used to enable the device with the GPIO of recent processors whose GPIO voltage is lower than traditional microcontrollers.

The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, the EN pin can be connected to the IN pin.

DROPOUT VOLTAGE

The TLV7103318-Q1 and TLV7101828-Q1 use a PMOS pass transistor to achieve low dropout. When $(V_{IN} – V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with the output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

The TLV7103318-Q1 and TLV7101828-Q1 each have a dedicated V_{REF}. Consequently, crosstalk from one channel to the other as a result of transients is close to 0V.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV7103318-Q1and TLV7101828-Q1 use an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV7103318-Q1 and TLV7101828-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV710-Q1 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from a die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Performance data for the TLV710-Q1 evaluation module (EVM) are shown in Table 1. The EVM is a 2-layer board with 2 ounces of copper per side. The dimension and layout are shown in Figure 54 and Figure 55. Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes in the heat-dissipating layer also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions.

Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 1:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (1)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TLV7103318-Q1 and TLV7101828-Q1 are available from the Texas Instruments Web site at www.ti.com. The recommended land pattern for the DSE (SON-6) package is shown in .

Table 1. TLV7103318-Q1 and TLV7101828-Q1 EVM Dissipation Ratings

PACKAGE	$R_{\theta JA}$	T_A < 25°C	T_A = 85°C	T_A = 125°C
DSE	170°C/W	585 mW	235 mW	mW

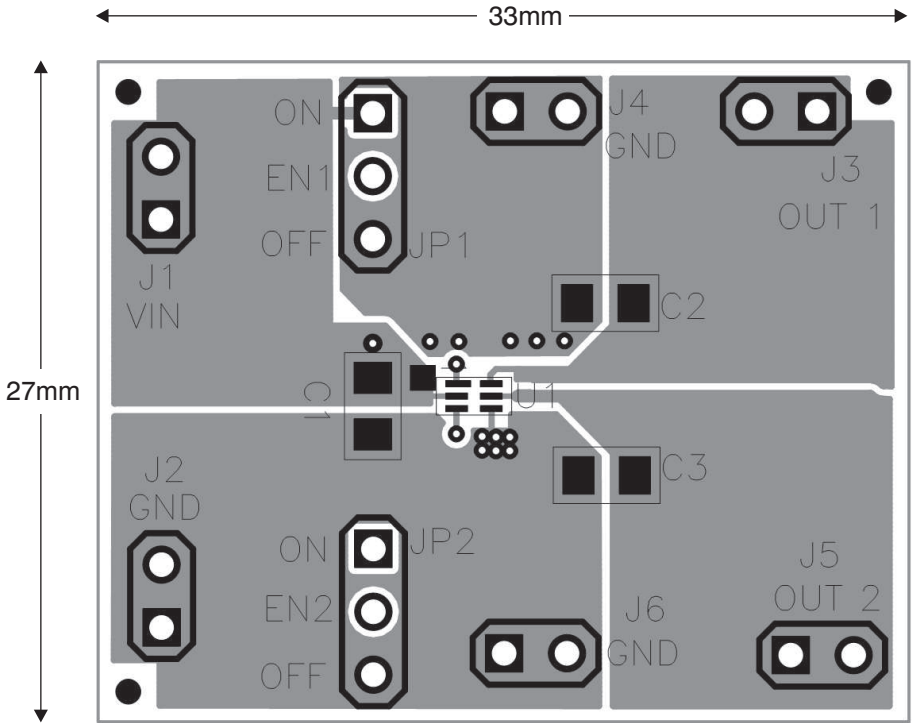


Figure 54. Top Layer

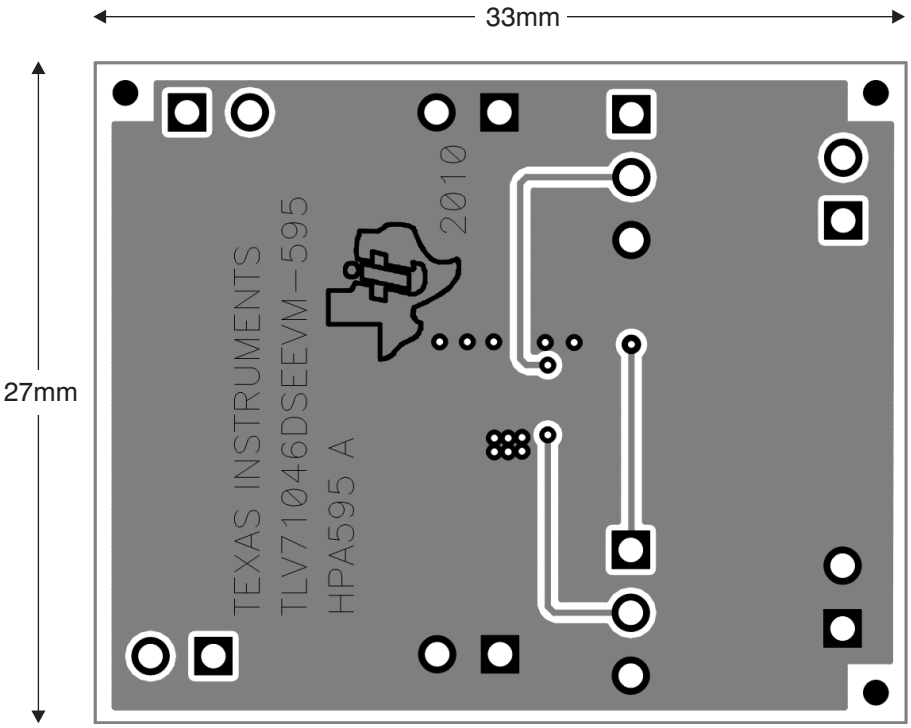


Figure 55. Bottom Layer

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7101828QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CP
TLV7101828QDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CP
TLV7103318QDSERQ1	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZD
TLV7103318QDSERQ1.B	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLV710-Q1 :

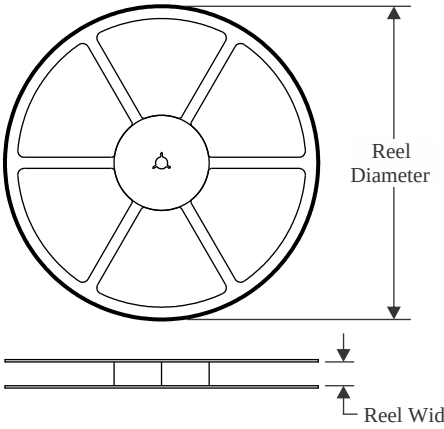
- Catalog : TLV710

NOTE: Qualified Version Definitions:

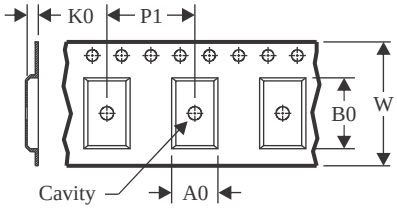
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

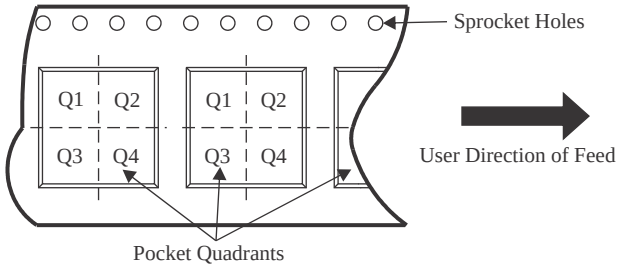


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

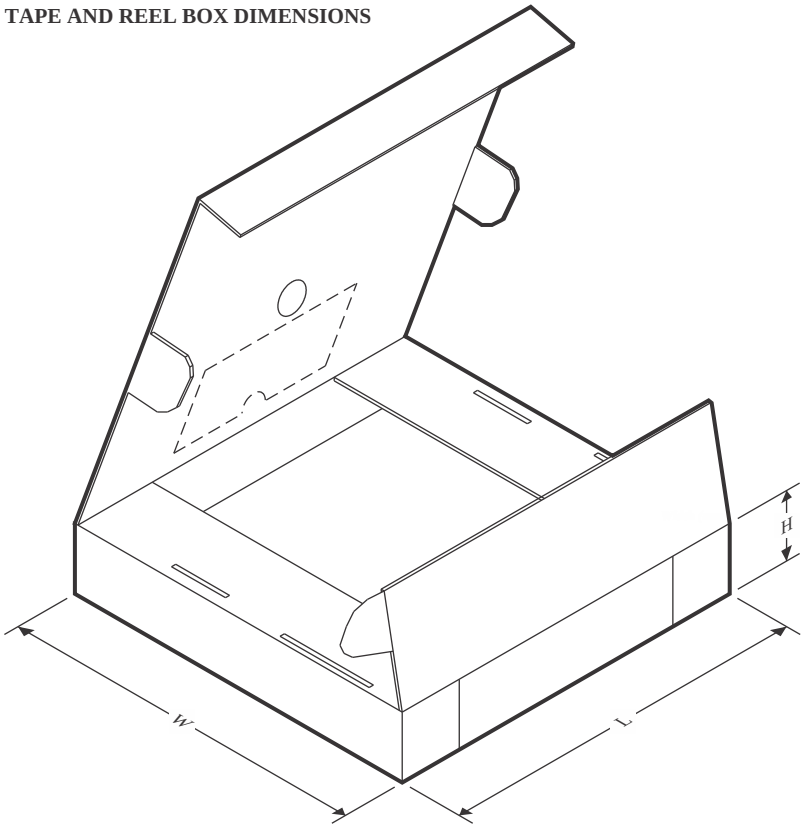
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7101828QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7103318QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

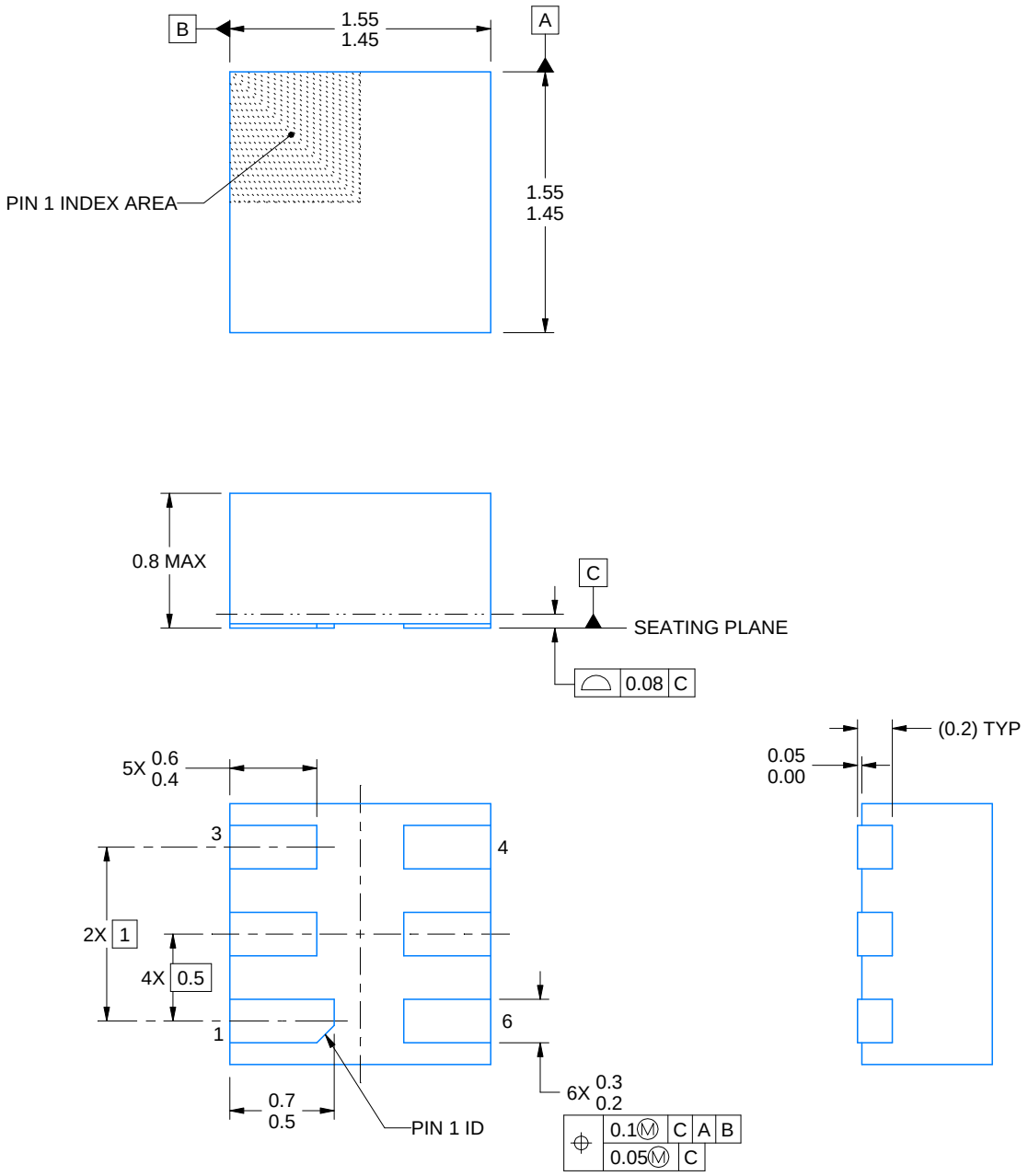
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7101828QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0
TLV7103318QDSERQ1	WSON	DSE	6	3000	200.0	183.0	25.0

DSE0006A

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

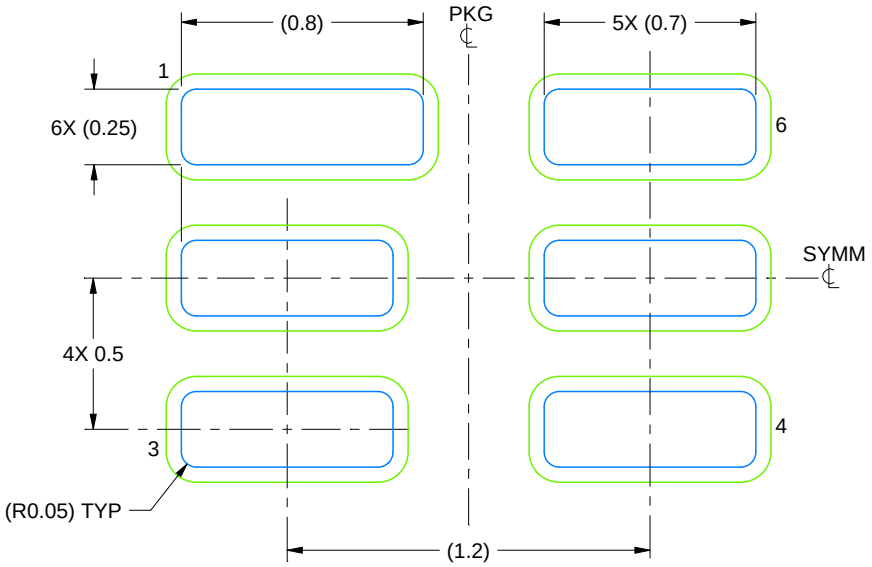
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

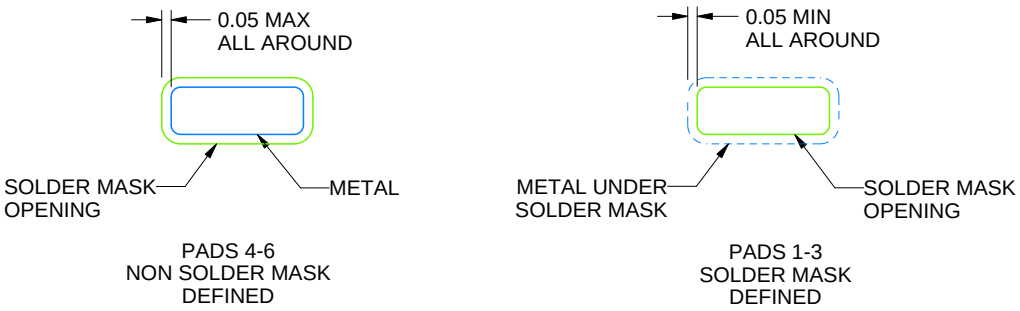
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

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NOTES: (continued)

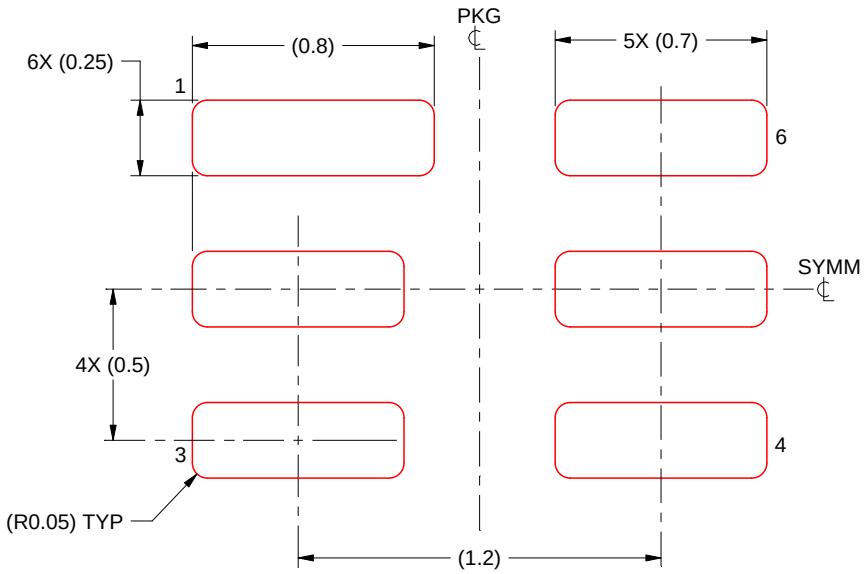
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月