TMP20 ±2.5°C 低功耗模拟输出温度传感器

1 特性

- ±2.5°C 精度（–55°C 至 130°C）
- 电源电压范围：1.8V 至 5.5V
- 低功耗：4μA（最大值）
- 微型封装：SOT-563，SC70-5
- SC70 与 LM20 引脚兼容

2 应用

- 手机
- 台式机和笔记本电脑
- 便携式设备
- 消费类电子产品
- 电池管理
- 电源
- HVAC
- 过热监控
- 磁盘驱动器
- 电器和白色家电
- 汽车

3 说明

TMP20 器件是采用微型 SOT-563 封装的 CMOS 精确模拟输出温度传感器。TMP20 的电源电压为 2.7V 至 5.5V，电源电流为 4μA 时，可在 –55°C 至 +130°C 的温度范围内运行。当工作温度范围为 15°C 至 130°C 时，工作电压可低至 1.8V。线性传递函数的斜率为 –11.77mV/°C（典型值），0°C 时输出电压为 1.8639V（典型值）。在 -55°C 至 130°C 的完整额定温度范围内，TMP20 精度为 ±2.5°C。

TMP20 的 4μA（最大）电源电流会将器件的自发热限制为低于 0.01°C。当 V+ 低于 0.5V 时，器件处于关断模式，耗电不到 20nA（典型值）。

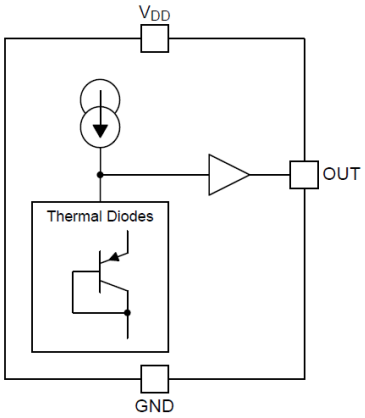
TMP20 采用 5 引线 SC70 或 6 引线 SOT-563 封装，可降低所需的总体布板空间。

器件信息(1)

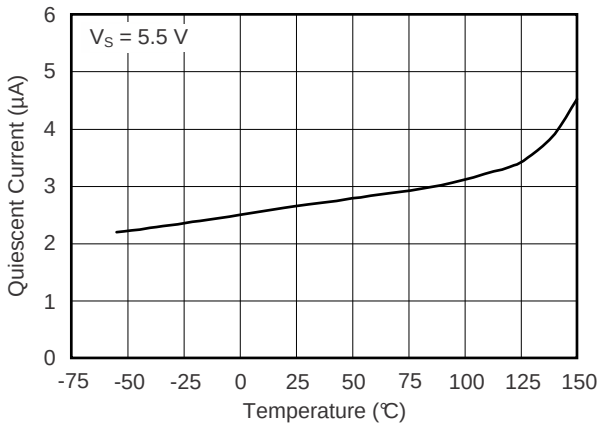
器件型号	封装	封装尺寸（标称值）
TMP20	SOT-563 (6)	1.60mm × 1.20mm
	SC70 (5)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

器件框图



器件静态电流与温度间的关系



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (October 2017) to Revision B **Page**

- 将*器件静态电流与温度间的关系* 图的 y 轴单位从 mA 更改为 µA ... 1
- Changed the y-axis unit of *Device Quiescent Current vs Temperature* graph from: mA to: µA ... 6
- Changed the y-axis unit of *Device Quiescent Current vs Temperature* graph from: mA to: µA ... 12
- 添加了*接收文档更新通知* 部分 ... 16

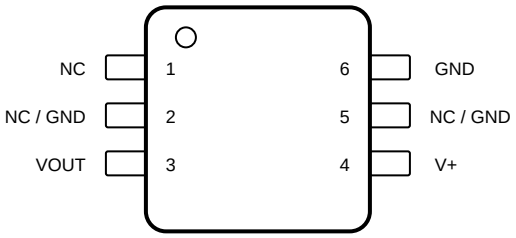
Changes from Original (December 2009) to Revision A **Page**

- 根据最新 TIS 文档和转化标准更新了数据表格式和内容 ... 1
- 在*器件信息* 部分添加了封装尺寸信息 ... 1
- 更新了 器件框图 ... 1
- 更新了 器件静态电流与温度间的关系 ... 1
- Reformatted *Absolute Maximum Ratings* table ... 4
- Changed *Thermal Information* table and added thermal information ... 4
- Changed minimum temperature sensitivity value from –11.4 mV/°C to –12.2 mV/°C in *Electrical Characteristics* table ... 5
- Changed maximum temperature sensitivity value from –12.2 mV/°C to –11.4 mV/°C in *Electrical Characteristics* table ... 5
- Updated 图 1 ... 6
- Updated 图 3 ... 6
- Updated 图 7 ... 6
- 已添加 *Functional Block* diagram, key graphics on front page, typical application schematic, application curves, and updated layout images ... 8
- Reformatted equations in *Transfer Function* section ... 9
- Corrected 公式 2 in *Transfer Function* section ... 9

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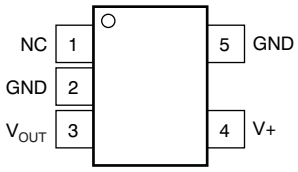
5 Pin Configuration and Functions

DRL Package
6-Pin SOT-563
Top View



Not to scale

DCK Package
5-Pin SC70
Top View



NC- no internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DRL (SOT-563)	DCK (SC70)		
GND	6	5	—	Ground pin
NC	1	1	—	This pin must be grounded or left floating. See *Layout Example* for more information.
NC / GND	2, 5	2	—	This pin must be grounded or left floating. For best thermal response, connect to GND plane. See *Layout Example* for more information.
V_{OUT}	3	3	O	Analog output
V+	4	4	I	Positive supply voltage

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V+		7	V
Operating temperature	–55	150	°C
Junction temperature, $T_{J(max)}$		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
	Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage range	1.8	5.5	V
T_A	Specified temperature range	–55	130	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP20		UNIT
		DRL (SOT563)	DCK (SC70)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	238	185	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	253	263.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	126.4	76.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	126	51.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13	1.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	125.9	50.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE MEASUREMENT (1)						
	Accuracy (2)	T_A = –55°C to 130°C	–2.5		2.5	°C
	vs supply	V+ = 1.8 V to 5.5 V T_A = 15°C to 130°C	–0.05		0.05	°C/V
		V+ = 2.7 V to 5.5 V T_A = –50°C to 130°C	–0.05		0.05	°C/V
	Temperature sensitivity (3)	T_A = –30°C to 100°C	–12.2	–11.77	–11.4	mV/°C
	Output voltage (4)	T_A = 0°C		1863.9		mV
		T_A = 25°C		1574		
	Nonlinearity (5)	–20°C ≤ T_A ≤ 80°C		±0.4%		
ANALOG OUTPUT						
	Output resistance	–600 µA ≤ I_{LOAD} ≤ 600 µA		10		Ω
	Load regulation	–600 µA ≤ I_{LOAD} ≤ 600 µA		6		mV
	Maximum capacitive load		1			nF
POWER SUPPLY						
V_S	Specified voltage	T_A = –55°C to 130°C	2.7		5.5	V
		T_A = 15°C to 130°C (6)	1.8		5.5	
I_Q	Quiescent current	V+ = 5.5 V T_A = 25°C		2.6	4	µA
	Over temperature	V+ = 5.5 V T_A = –55°C to 130°C			6	µA
I_{SD}	Shutdown current	V+ < 0.5 V		20		nA
TEMPERATURE RANGE						
	Specified operating	T_A = –55°C to 130°C	–55		130	°C
		T_A = 15°C to 130°C (6)	15		130	°C
	Operating range	V+ = 2.7 V to 5.5 V	–55		150	°C
θ_{JA}	Thermal resistance	SC70		185		°C/W
		SOT-563		238		°C/W
	Self-heating	SC70			0.01	°C
		SOT-563			0.01	°C

(1) 100% production tested at T_A = 25°C. Specifications over temperature range are assured by design.
(2) Power-supply rejection is encompassed in the accuracy specification.
(3) Temperature sensitivity is the average slope to the equation $V_O = (–11.77 \times T) + 1.860$ V.
(4) V_{OUT} is calculated from temperature with the following equation:
$V_O = (–3.88 \times 10^{–6} \times T^2) + (–1.15 \times 10^{–2} \times T) + 1.8639$ V,
where T is in °C.
(5) Nonlinearity is the deviation of the calculated output voltage from the best fit straight line.
(6) The TMP20 transfer function requires the output voltage to rise above the 1.8-V supply as the temperature decreases below 15°C. When operating at a 1.8-V supply, it is normal for the TMP20 output to approach 1.8 V and remain at that voltage as the temperature continues to decrease below 15°C. This condition does not damage the device. Once the temperature rises above 15°C, the output voltage resumes changing as the temperature changes, according to the transfer function specified in this document. For more information about the transfer function, see *Transfer Function* .

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6.6 Typical Characteristics

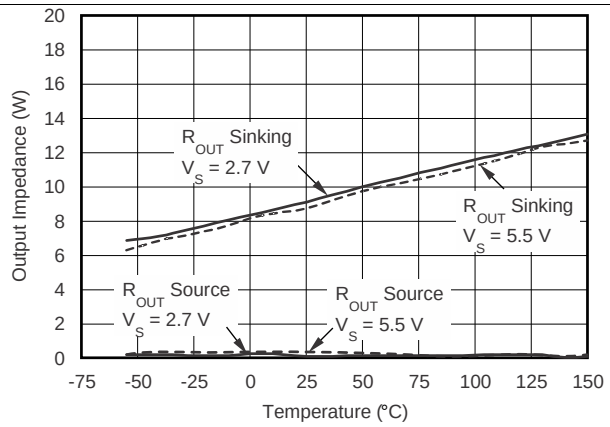


图 1. Output Impedance vs Temperature

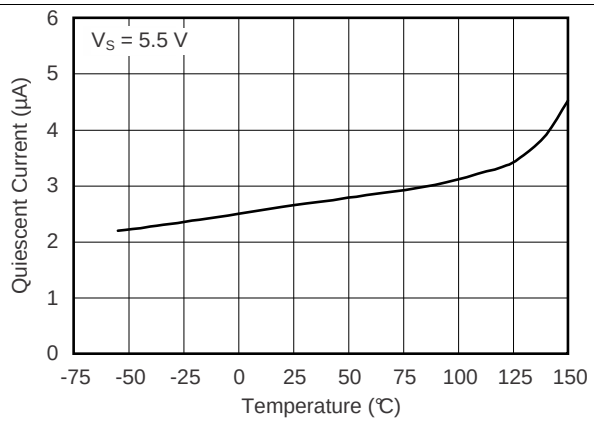


图 2. Quiescent Current vs Temperature

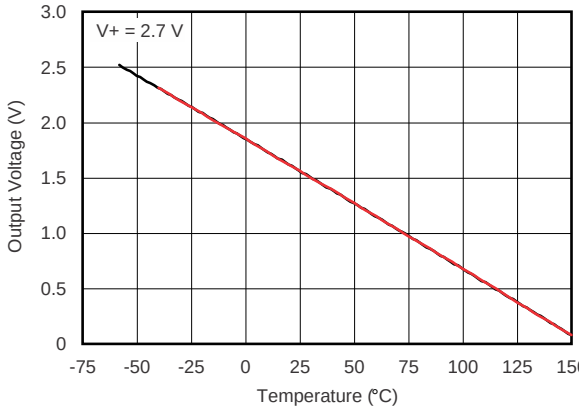


图 3. Output Voltage vs Temperature

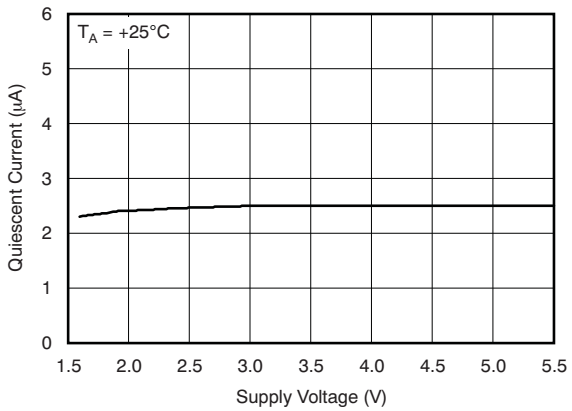


图 4. Quiescent Current vs Supply Voltage

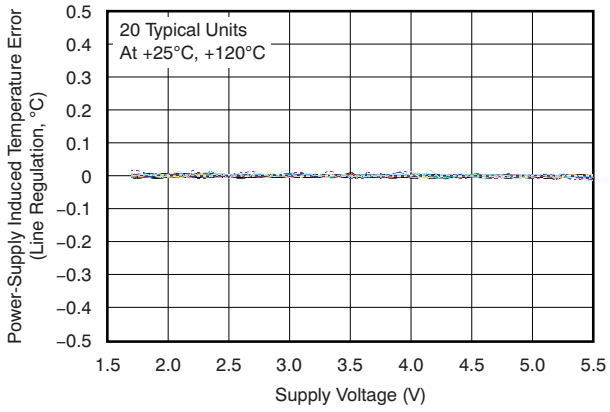


图 5. Power-Supply Rejection vs Temperature

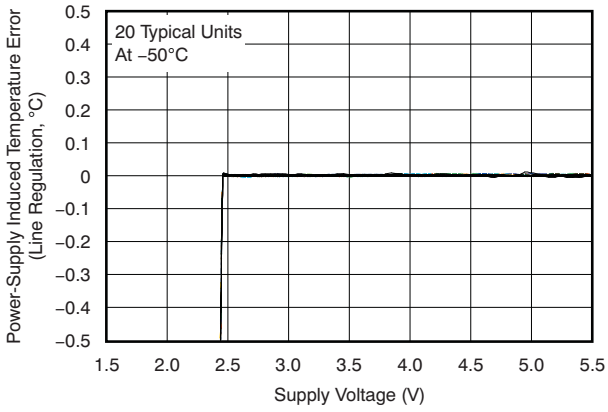


图 6. Power-Supply Rejection vs Temperature

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Typical Characteristics (接下页)

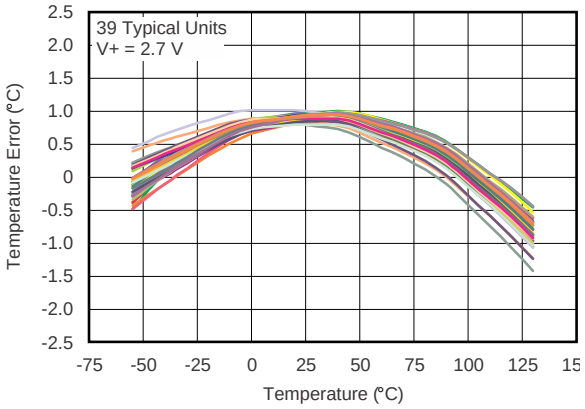


图 7. Temperature Error vs Temperature

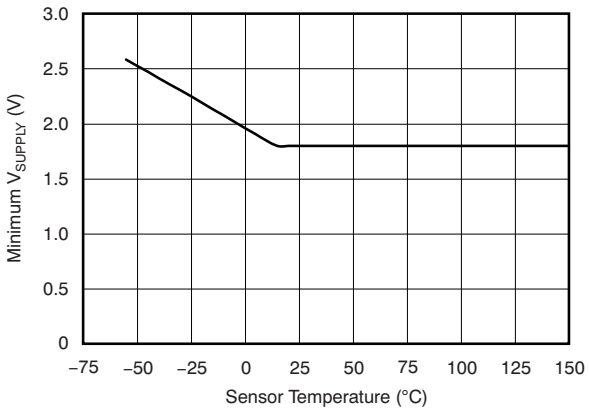


图 8. Minimum Supply Voltage vs Temperature

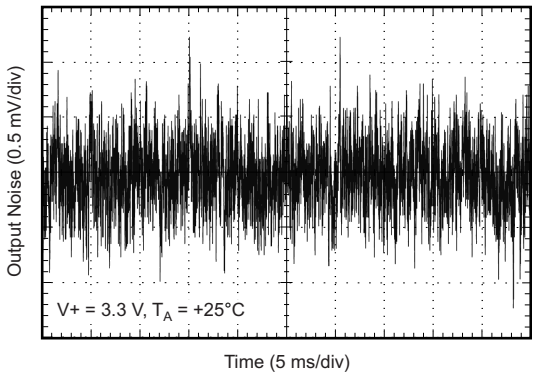


图 9. Wideband Output Noise Voltage

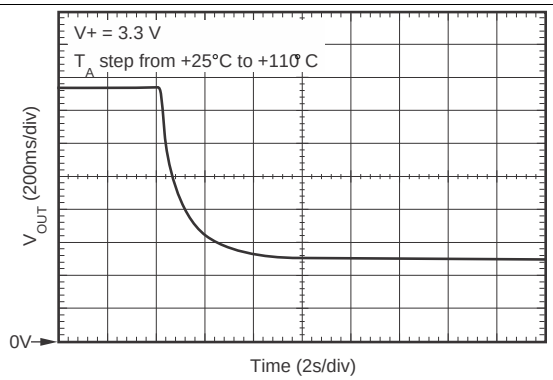


图 10. Thermal Settling (Fluid-Filled Temperature Bath)

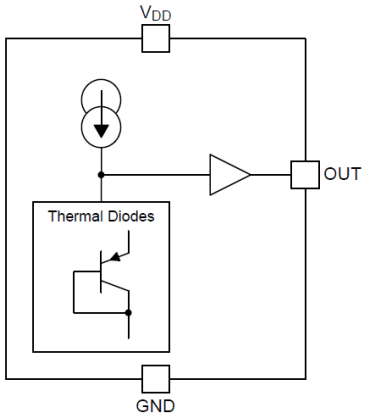
7 Detailed Description

7.1 Overview

The TMP20 device is a precision analog output temperature sensor. The temperature range of operation is –55°C to +130°C with supply voltages of 2.7 V to 5.5 V. The TMP20 operates from power-supply voltages as low as 1.8 V over a temperature range of 15°C to 130°C.

TI recommends power supply bypassing; use a 100-nF capacitor placed as closely as possible to the supply pin.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Transfer Function

The analog output of the TMP20 over the –55°C to +130°C temperature range corresponds to the parabolic transfer function shown in
添加了接收文档更新通知 部分:

$$V_{OUT} = \left(-3.88 \times 10^{-6} \times T^2\right) + \left(-1.15 \times 10^{-2} \times T\right) + 1.8639\ V$$

Where:

- the temperature (T) is in °C. (1)

When solving for temperature, the equation is shown as 公式 2:

$$T = -1481.96 + \sqrt{2.1962 \times 10^{6} + \frac{(1.8639 - V_O)}{3.88 \times 10^{-6}}} \quad (2)$$

These equations apply over the entire operating range of –55°C to +130°C.

A simplified linear transfer function referenced at 25°C is shown in 公式 3:

$$V_{OUT} = -11.69\ mV/°C \times T + 1.8863\ V \quad (3)$$

Linear transfer functions are calculated for limited temperature ranges by calculating the slope and offset for that limited range, where slope is calculated by 公式 4:

$$m = -7.76 \times 10^{-6} \times T - 0.0115$$

Where:

- T equals the temperature at the middle of the temperature range of interest (4)

The offset in the linear transfer function is calculated with 公式 5:

$$b = \left(V_{OUT}(T_{MAX}) + V_{OUT}(T) - m \times (T_{MAX} + T)\right) / 2$$

where

- $V_{OUT}(T_{MAX})$ is the calculated output voltage at T_{MAX} as determined from
  添加了接收文档更新通知 部分. (5)

$V_{OUT}(T)$ is the calculated output voltage at T as calculated by
添加了接收文档更新通知 部分.

7.3.1.1 Example 1

Determine the linear transfer function for –40°C to +110°C.

T_{MIN} = –40°C; T_{MAX} = 110°C; therefore, T = 35°C

m = –11.77mV/°C
V_{OUT} (110°C) = 0.5520 V
V_{OUT} (35°C) = 1.4566 V
b = 1.8576 V

The linear transfer function for –40°C to +110°C is shown in 公式 6:

$$V_{OUT} = -11.77\ mV/°C \times T + 1.8576\ V \quad (6)$$

Feature Description (接下页)

表 1 lists common temperature ranges of interest and the corresponding linear transfer functions for these ranges. Note that the error (maximum deviation) of the linear equation from the parabolic equation increases as the temperature ranges widen.

表 1. Common Temperature Ranges and Corresponding Linear Transfer Functions

TEMPERATURE RANGE		LINEAR EQUATION (V)	MAXIMUM DEVIATION OF LINEAR EQUATION FROM PARABOLIC EQUATION (°C)
T_{MIN} (°C)	T_{MAX} (°C)		
–55	130	V_{OUT} = –11.79 mV/°C × T + 1.8528	±1.41
–40	110	V_{OUT} = –11.77 mV/°C × T + 1.8577	±0.93
–30	100	V_{OUT} = –11.77 mV/°C × T + 1.8605	±0.70
–40	85	V_{OUT} = –11.67 mV/°C × T + 1.8583	±0.65
–10	65	V_{OUT} = –11.71 mV/°C × T + 1.8641	±0.23
35	45	V_{OUT} = –11.81 mV/°C × T + 1.8701	±0.004
20	30	V_{OUT} = –11.69 mV/°C × T + 1.8663	±0.004

7.4 Device Functional Modes

The singular functional mode of the TMP20 is an analog output inversely proportional to temperature.

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8 Application and Implementation

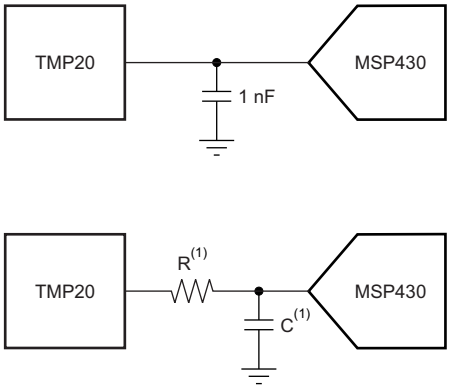
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Output Drive and Capacitive Loads

When used in noisy environments, adding a capacitor from the output to ground with a series resistor filters the TMP20 output; this configuration is shown in 图 11. The TMP20 can drive up to 1 nF of load capacitance while sourcing and sinking 600 μA. Under this condition, capacitive loads in the range of 1 nF to 10 μF require a 150-Ω series output resistor to achieve a stable temperature measurement. The output impedance of the TMP20 is typically 10 Ω when sinking currents and less than 1 Ω when sourcing current, as shown in 图 1.

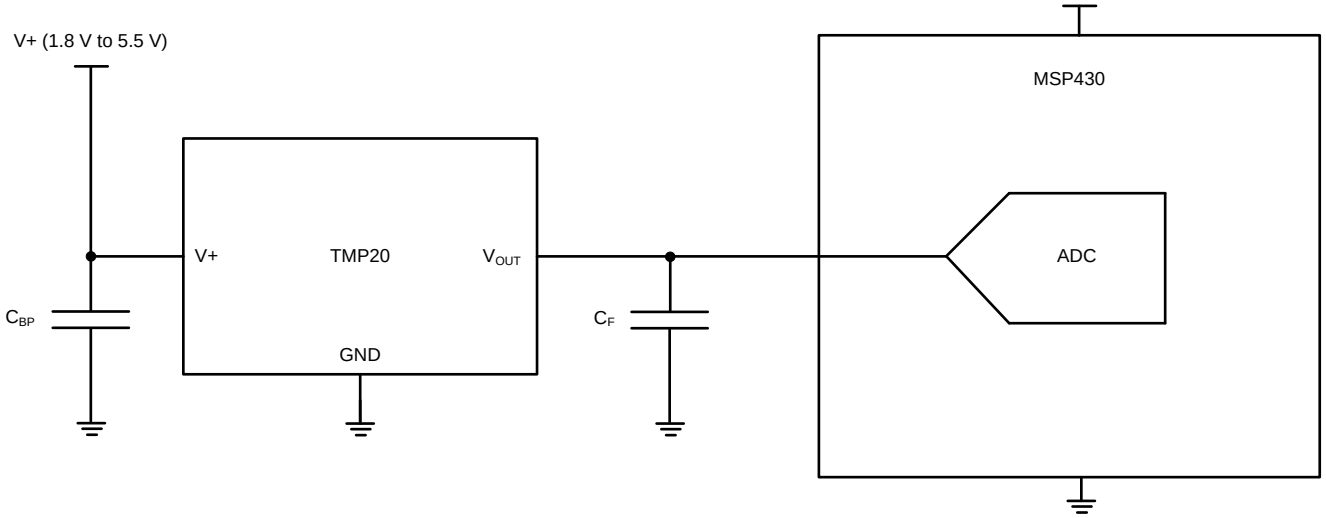


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(1) A series resistor (R) may be required depending upon the amount of capacitance (C) and the amount of source and sink current drawn from the output of the TMP20.

图 11. TMP20 Output Filtering

8.2 Typical Application



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图 12. Suggested Connections to a MCU ADC

8.2.1 Design Requirements

ADCs that are found in microcontrollers (such as the MSP430 line of microcontrollers) take charge during the sampling phase. A high sampling frequency results in too much charge pulled into the ADC and sags the output voltage of the TMP20, which results in a reading that is hotter than normal. To mitigate this, place a capacitor (C_F) between the TMP20 and the ADC. The capacitor functions as a charge reservoir.

8.2.2 Detailed Design Procedure

The size of C_F depends on the size of the internal sampling capacitor and the sampling frequency. The charge requirements may vary because not all ADCs have identical input stages. This general ADC application is shown as an example only.

8.2.3 Application Curves

图 13 shows the quiescent current versus temperature.

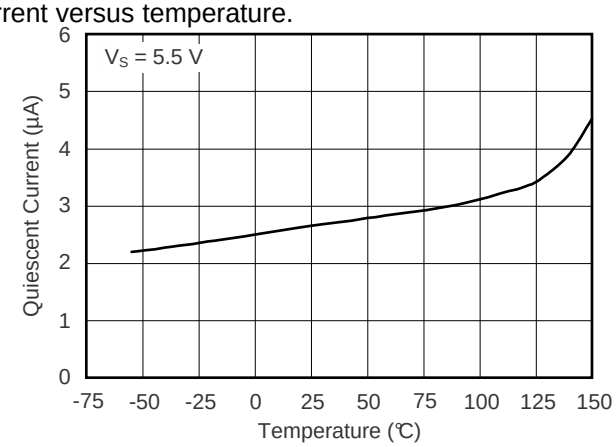


图 13. Quiescent Current vs Temperature

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9 Power Supply Recommendations

The low supply current and supply range of 1.8 V to 5.5 V enable the TMP20 to be powered from multiple supply sources.

Power supply bypassing is optional and is typically dependent on the noise of the power supply. In noisy systems, adding bypass capacitors may be necessary to decrease the noise that couples to the output of the TMP20.

10 Layout

10.1 Layout Guidelines

The substrate on the TMP20AIDCK package is directly connected through conductive epoxy to the flag that connects pin 2 on the lead frame. Consequently, pin 2 is the best lead for a conductive thermal connection to the TMP20 die. The optimal electrical connection for this pin is ground (GND).

CAUTION

Do not attempt to connect pin 2 (DCK package) to any electrical potential other than ground.

If it is not possible to connect pin 2 to ground, it is possible to electrically isolate this pin (that is, leave it floating). Take care when electrically isolating this pin because any noise or electromagnetic interference or radio frequency interference (EMI or RFI) spikes that couple in through this pin can cause erroneous temperature results.

shows a proper layout of the TMP20 with correct electrical and thermal connections to pin 2.

10.2 Layout Example

图 14 shows a layout of the TMP20 with proper electrical and thermal connections to pin 2.

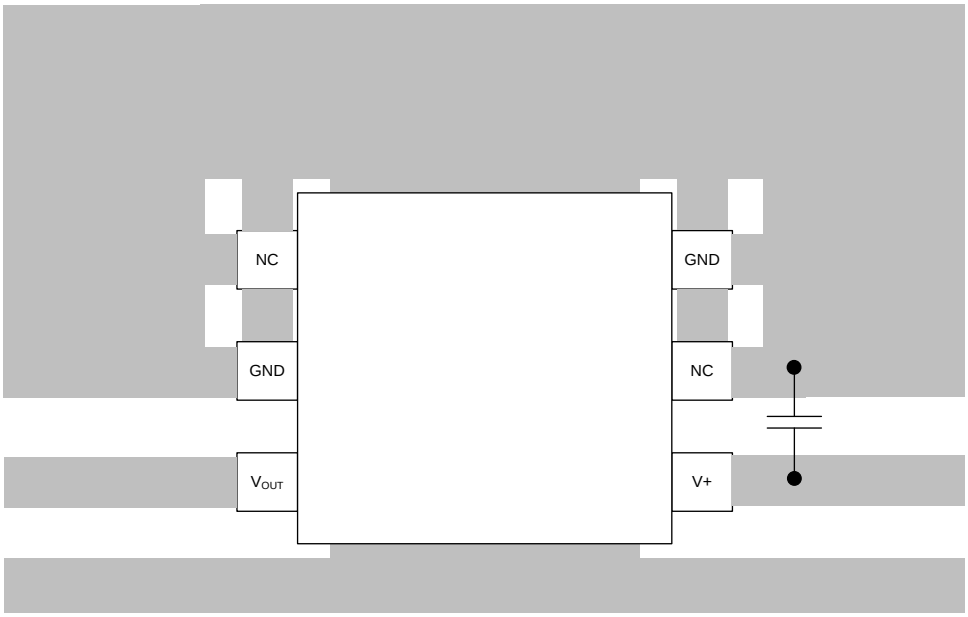


图 14. TMP20 Layout With Proper Electrical and Thermal Connections

11 器件和文档支持

11.1 器件支持

11.1.1 TINA-TI（免费下载软件）

TINA 是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。它提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从WEBENCH® 设计中心免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。

虚拟仪器为用户提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

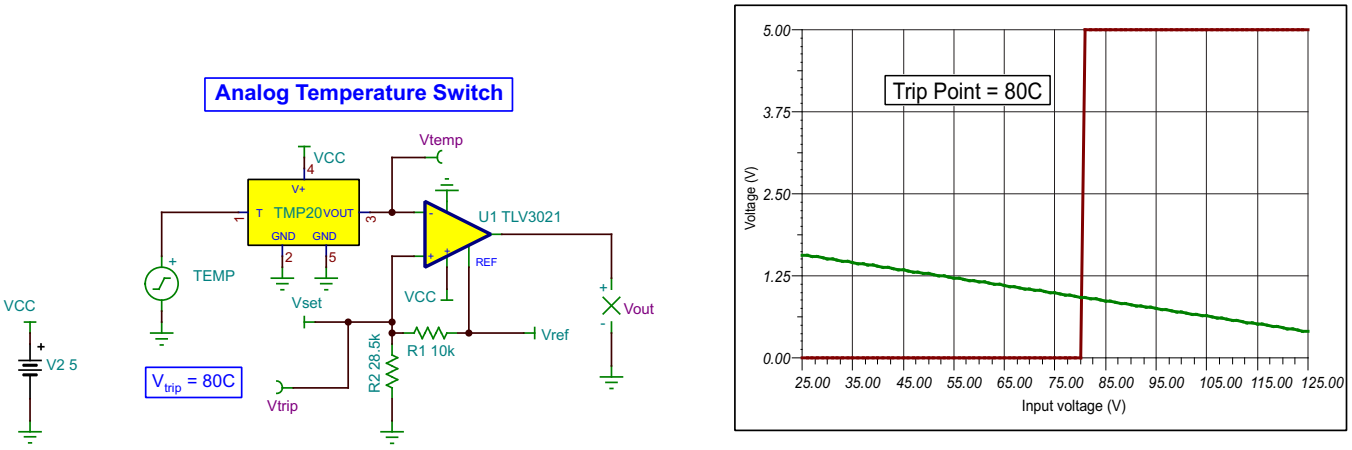
图 15 和 图 16 提供了适用于 TMP20 的 TINA-TI 电路示例，可针对特定应用开发、修改和评估 电路。下面给出了这些仿真文件的下载链接。

11.1.1.1 针对 TMP20 使用基于 SPICE 的 TINA-TI 模拟仿真程序

注

这些文件需要安装 TINA 软件（从 DesignSoft）或 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

中添加了版权声明



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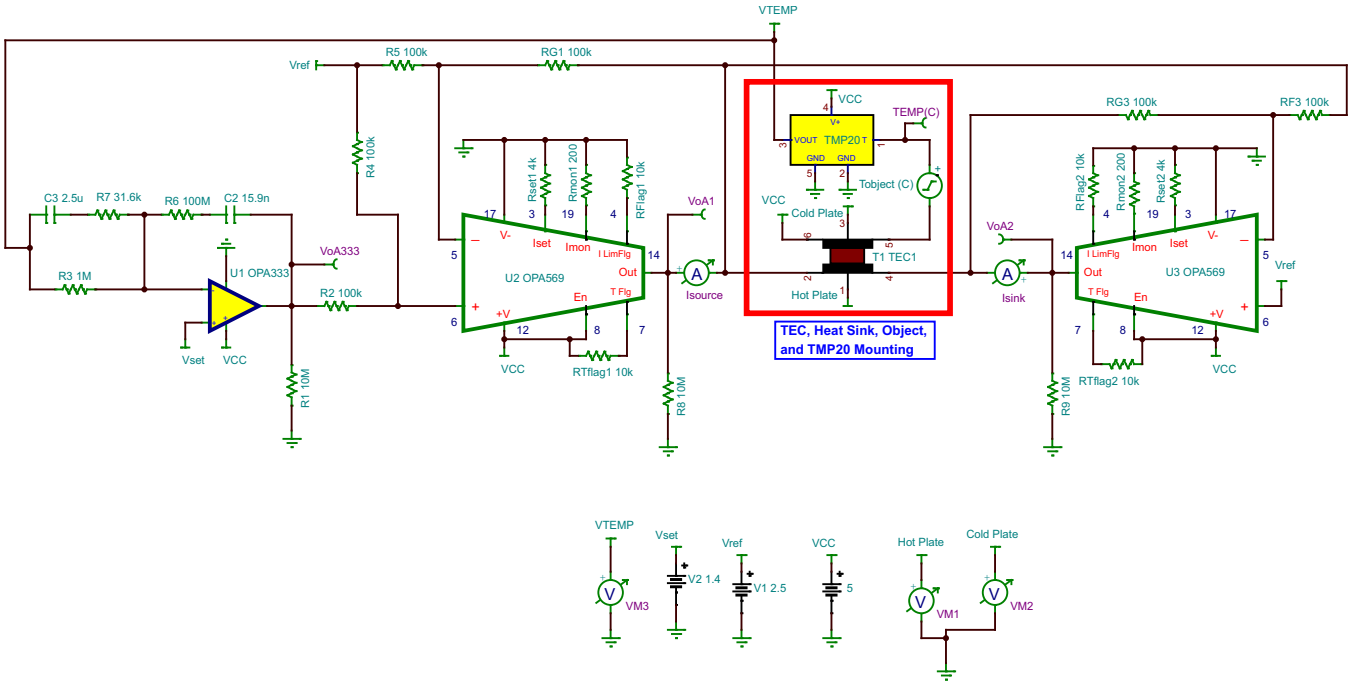
Note: TMP20 TINA 模型仅为初步模型。

图 15. 模拟温度开关

要下载包含适用于此电路的 TINA-TI 模拟文件的压缩文件，请访问 WEBENCH® 设计中心。

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器件支持 **(接下页)**



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(1) TMP20 TINA 模型仅为初步模型。

(2) 参数和定义：

a. T_{object} = 待冷却物体的温度（单位 °C）

b. V_{set} = 与 TMP20 所需输出温度对应的电压

c. VTEMP = TMP20 的电压输出

d. 热板 = 物体对侧的 TEC 板

e. 冷板 = 与物体接触的 TEC 板

(3) 在此配置中，TEC 驱动器能冷却至 –T°C，可加热至 41 °C；V_{set} 范围为 1.38V 至 1.95V。OPA569 器件输出 = ± 1.65A、±0.5V 至 ±4.5V。10-MΩ 电阻器用于 TINA 聚合。

(4) 对于 TINA 软件中的聚合：在 **Analysis/Set Analysis Parameters** 菜单中，设置 *shunt conductance* = 1p。

图 16. 热电冷却器

要下载包含适用于此电路的 TINA-TI 模拟文件的压缩文件，请参阅热电冷却器。

器件支持 **(接下页)**

11.1.2 开发支持

WEBENCH® 设计中心

TINA-TI 文件夹

模拟温度开关

热电冷却器

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

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11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

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12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP20AIDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	ODB
TMP20AIDCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	ODB
TMP20AIDRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	ODA
TMP20AIDRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ODA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

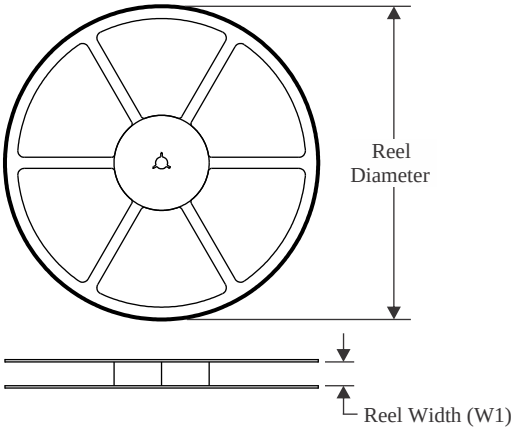
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

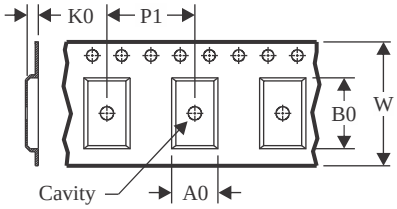
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

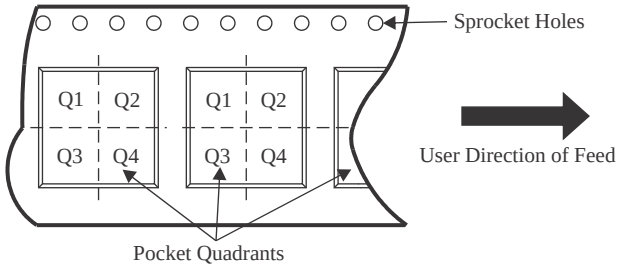


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

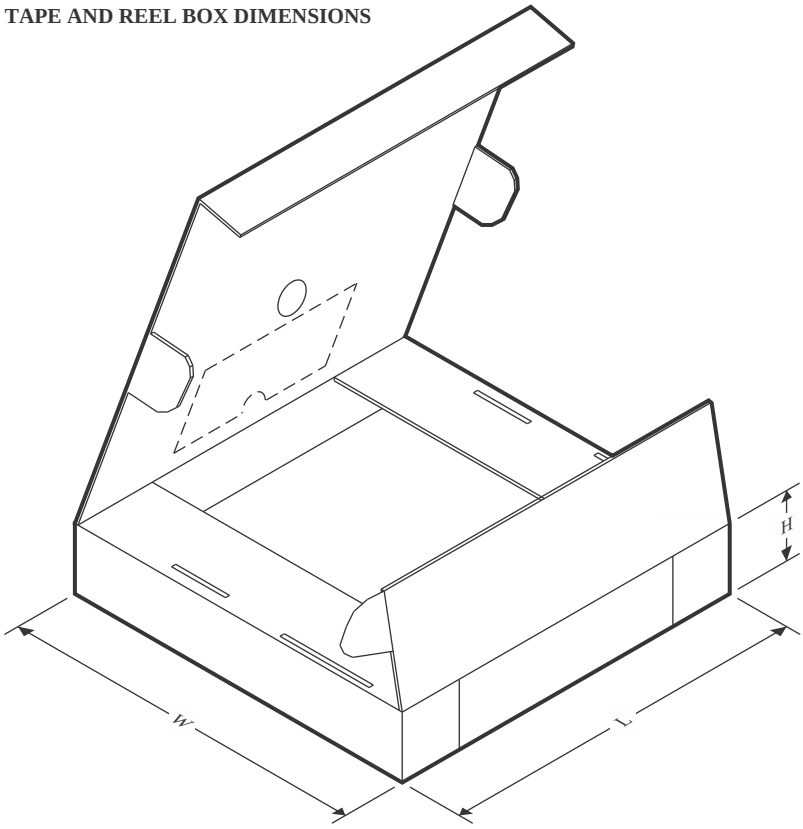
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP20AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMP20AIDCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TMP20AIDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TMP20AIDRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

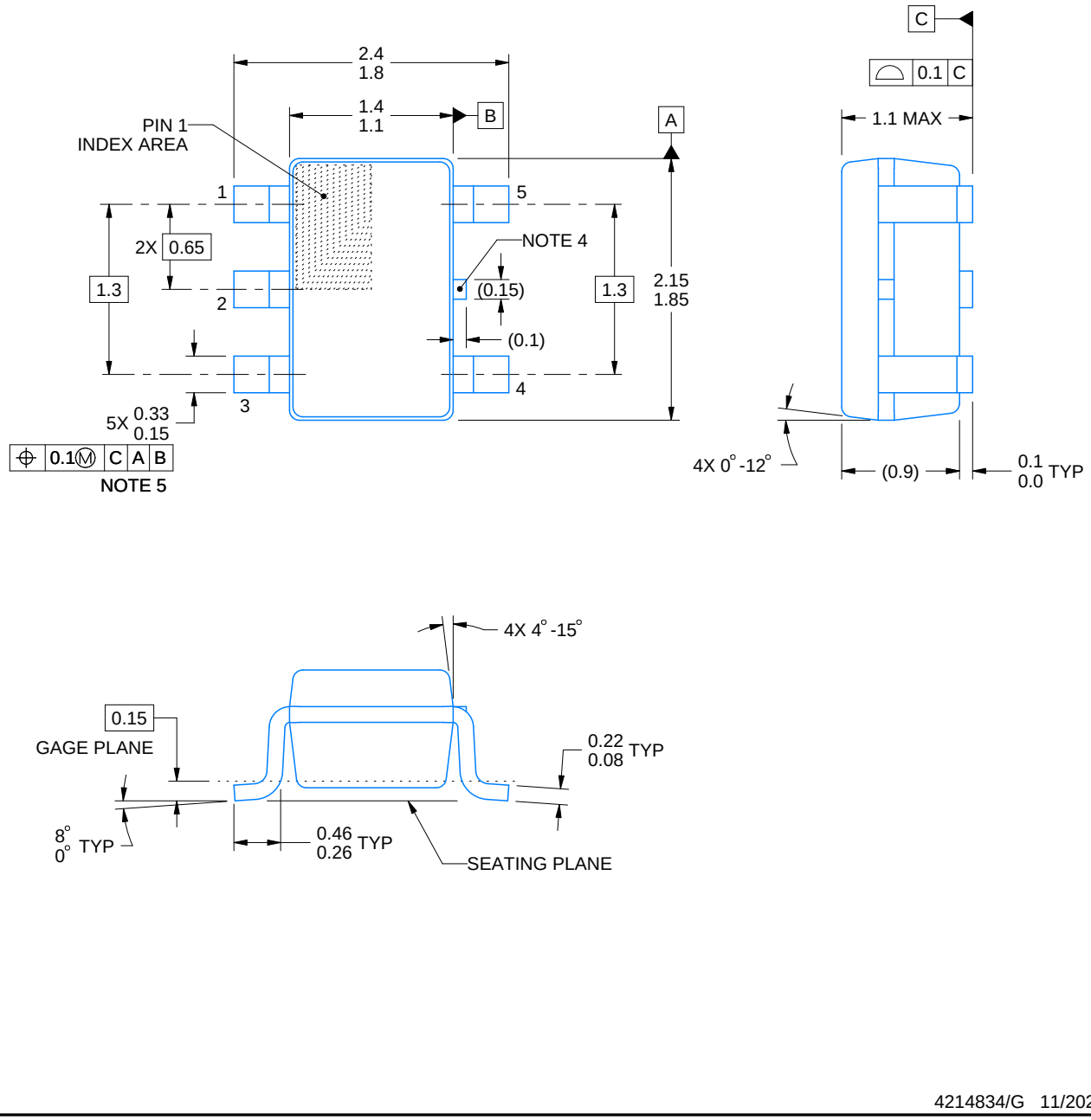
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP20AIDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TMP20AIDCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TMP20AIDRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TMP20AIDRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

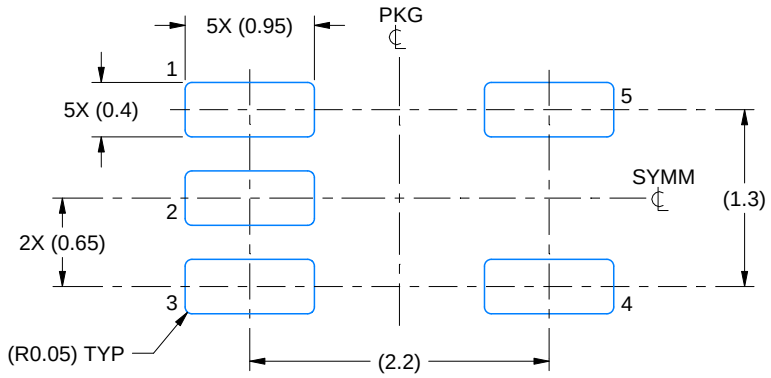
SMALL OUTLINE TRANSISTOR



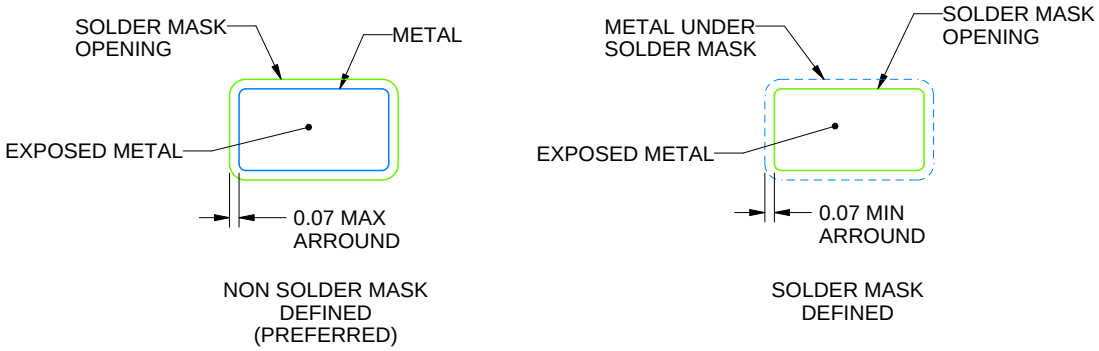
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

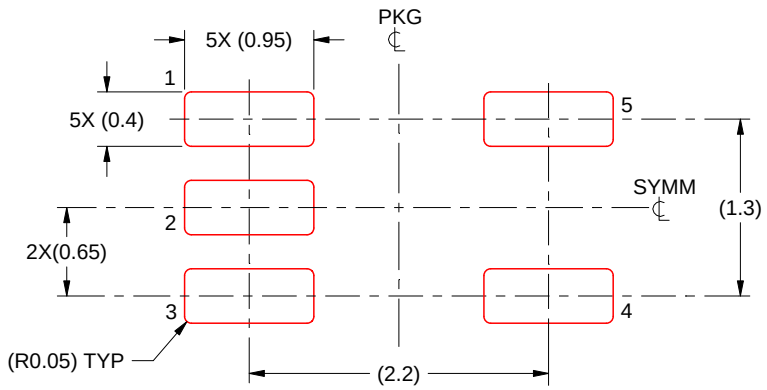


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

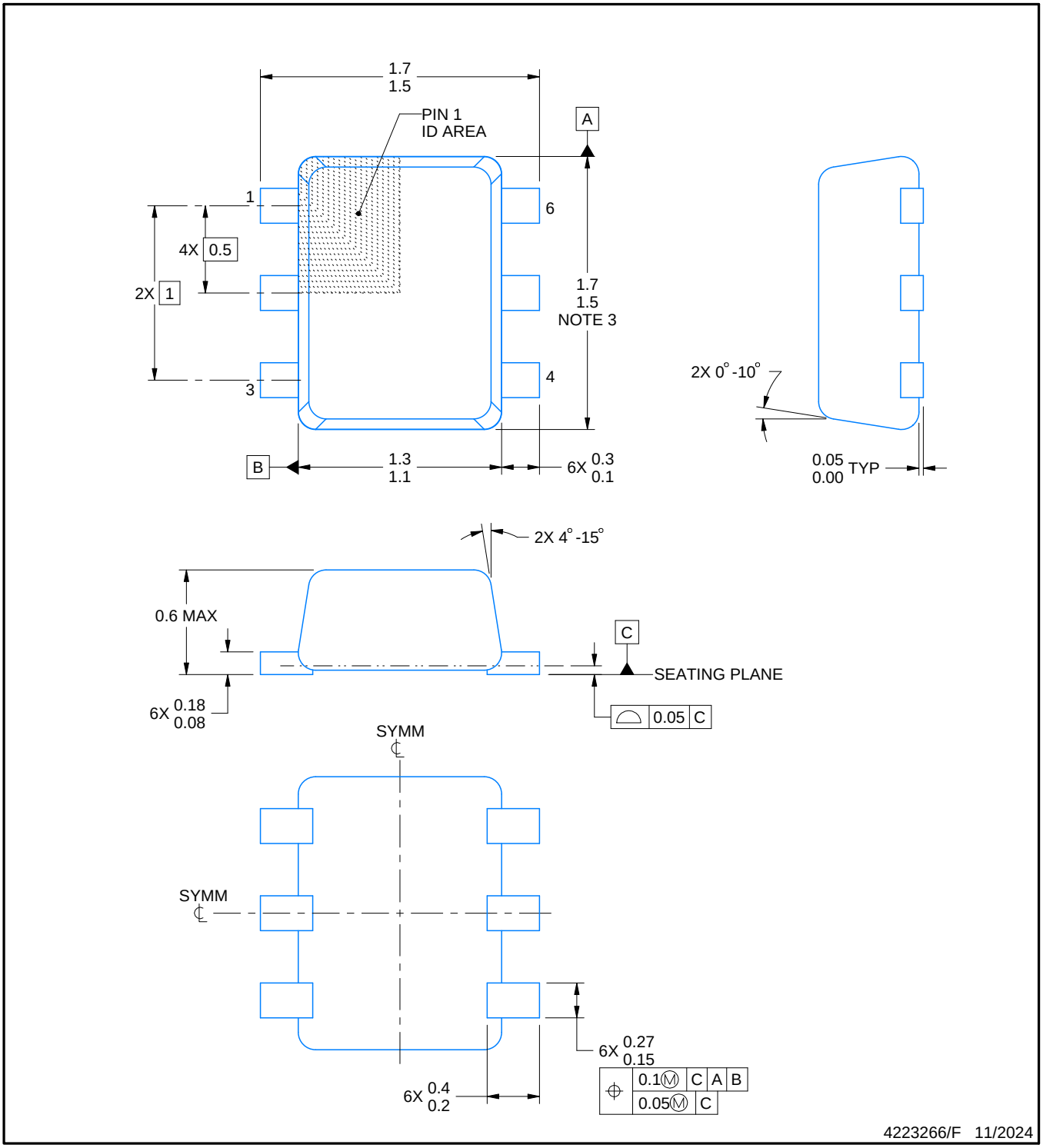


PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

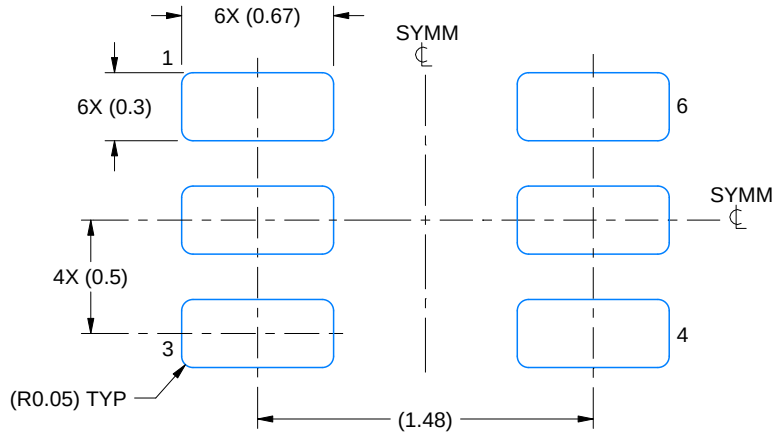
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

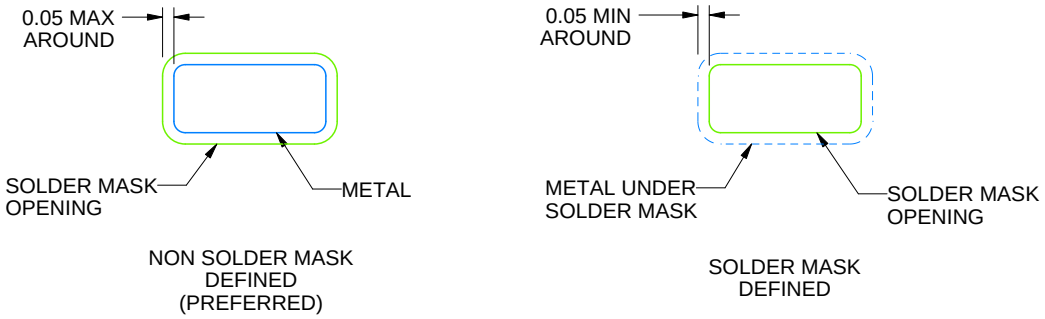
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

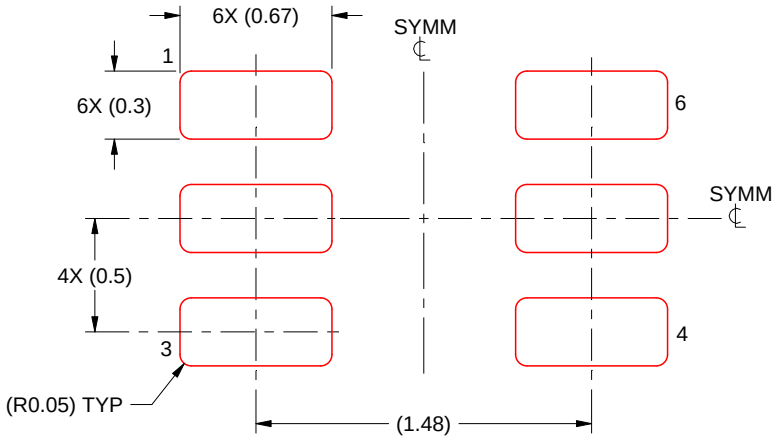
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月