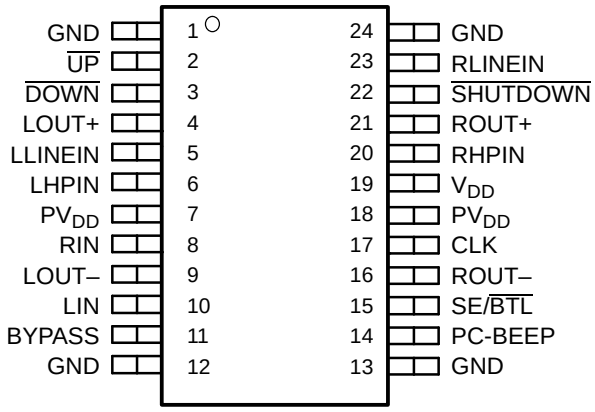
2.8-W STEREO AUDIO POWER AMPLIFIER WITH DIGITAL VOLUME CONTROL

FEATURES

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **Digital Volume Control From 20 dB to -40 dB**
- **2.8-W/Ch Output Power Into a 3-Ω Load**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



DESCRIPTION

The TPA0152 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2.8 W of continuous RMS power per channel into 3-Ω loads.

This device minimizes the number of external components needed, which simplifies the design and frees up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0152 has less than 0.3% THD+N across its specified frequency range. The integrated depop circuitry virtually eliminates transients that cause noise in the speakers.

The overall gain of the amplifier is controlled digitally by the $\overline{UP}$ and $\overline{DOWN}$ terminals. At power up, the gain is set at the lowest level which is -85 dB. It can then be adjusted to any of 31 discrete steps by pulling the voltage down at the desired pin to logic low. The gain is adjusted in the initial stage of the amplifier as opposed to the power output stage. As a result, the THD changes little over all volume levels.

An internal input MUX allows two sets of stereo inputs to the amplifier. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0152 automatically switches into SE mode when the SE/$\overline{BTL}$ input is activated. This effectively reduces the gain by 6 dB. The TPA0152 consumes only 10 mA of supply current during normal operation. A shutdown mode is included that reduces the supply current to 150 µA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are truly realized in multilayer PCB applications. This allows the TPA0152 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

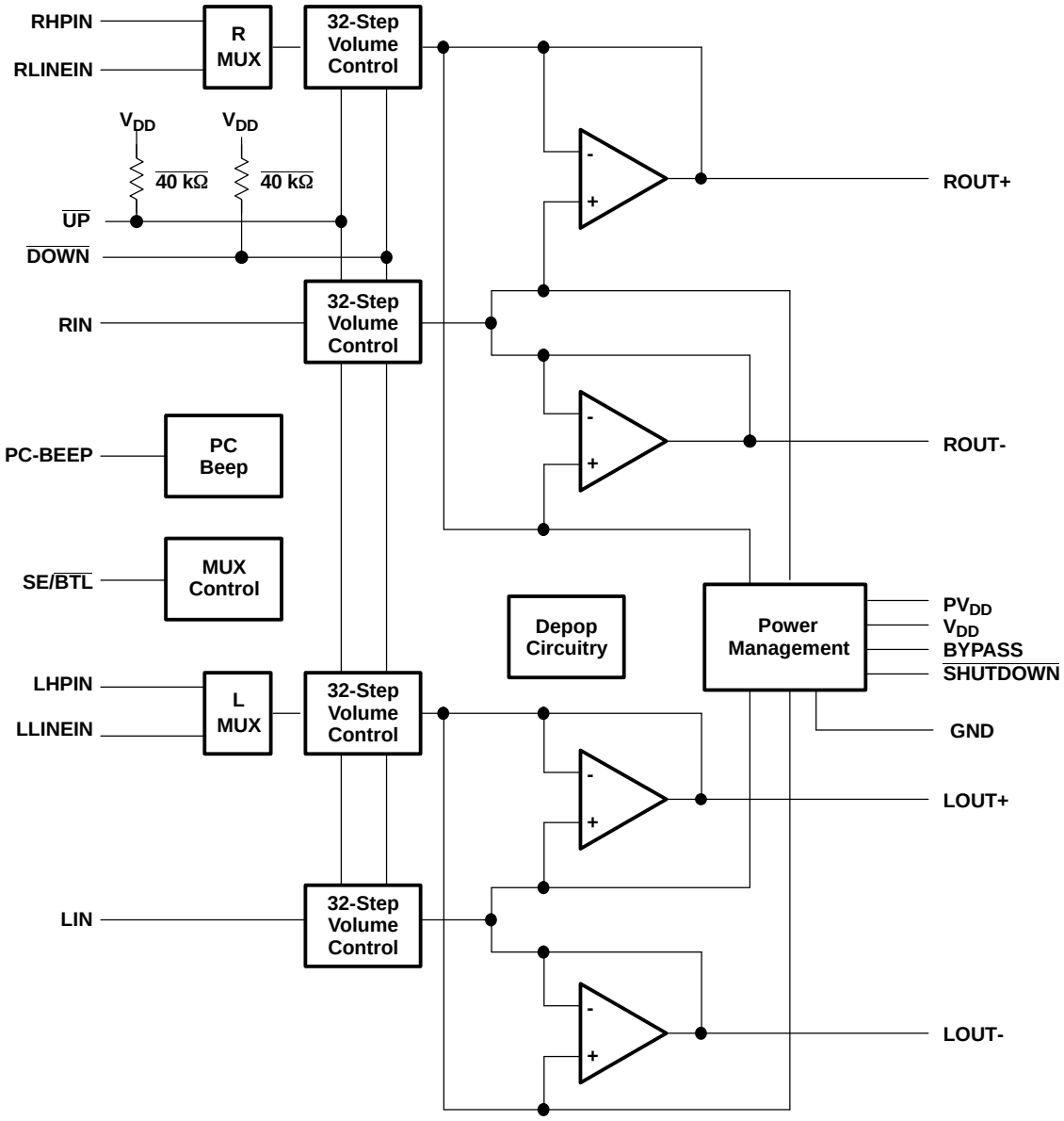
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGED DEVICE
	TSSOP(1) (PWP)
-40°C to 85°C	TPA0152PWP

(1) The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0152PWPR).

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
CLK	17	I	If a 47-nF capacitor is attached, the TPA0152 generates an internal clock. An external clock can override the internal clock input to this terminal.
$\overline{\text{DOWN}}$	3	I	A momentary pulse on this terminal decreases the volume level by 2 dB. Holding the terminal low for a period of time will step the amplifier through the volume levels at a rate determined by the capacitor on the CLK terminal.
GND	1, 12, 13, 24	I	Ground connection for circuitry. Connected to thermal pad
LHPIN	6	I	Left-channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs
LLINEIN	5	I	Left-channel line negative input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left-channel positive output in $\overline{\text{BTL}}$ mode and positive in SE mode
LOUT-	9	O	Left-channel negative output in $\overline{\text{BTL}}$ mode and high impedance in SE mode
PC-BEEP	14	I	The input for PC-Beep mode. PC-BEEP is enabled when a > 1.5-V (peak-to-peak) square wave is input to PC-BEEP or PCB ENABLE is high.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs
RLINEIN	23	I	Right-channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right-channel positive output in $\overline{\text{BTL}}$ mode and positive in SE mode
ROUT-	16	O	Right-channel negative output in $\overline{\text{BTL}}$ mode and high impedance in SE mode
SE/$\overline{\text{BTL}}$	15	I	Input and output MUX control. When this terminal is held high, the LHPIN or RHPIN and SE output is selected. When this terminal is held low, the LLINEIN or RLINEIN and $\overline{\text{BTL}}$ output are selected.
$\overline{\text{SHUTDOWN}}$	22	I	When held low, this terminal places the entire device, except PC-BEEP detect circuitry, in shutdown mode.
$\overline{\text{UP}}$	2	I	A momentary pulse on this terminal increases the volume level by 2 dB. Holding the terminal low for a period of time will step the amplifier through the volume levels at a rate determined by the capacitor on the CLK terminal.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.
Thermal Pad			Connect to ground. Must be soldered down in all applications to properly secure device on PC board.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	UNIT
Supply voltage, V_{DD}	6 V
Input voltage, V_I	-0.3 V to V_{DD} 0.3 V
Continuous total power dissipation	Internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A	-40°C to 85°C
Operating junction temperature range, T_J	-40°C to 150°C
Storage temperature range, T_{stg}	-65°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W(1)	21.8 mW/°C	1.7 W	1.4 W

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD™ package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{\text{BTL}}$	$0.8 \times V_{DD}$		V
	$\overline{\text{SHUTDOWN}}$	2		
	$\overline{\text{UP}}$, $\overline{\text{DOWN}}$	4		
Low-level input voltage, V_{IL}	SE/$\overline{\text{BTL}}$		$0.6 \times V_{DD}$	V
	$\overline{\text{SHUTDOWN}}$		0.8	
	$\overline{\text{UP}}$, $\overline{\text{DOWN}}$		0.5	
Operating free-air temperature, T_A		-40	85	°C

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	V_I = 0 V, A_V = 6dB			35	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		67		dB
$\lvert I_{IH} \rvert$	High-level input current - $\overline{\text{SHUTDOWN}}$, SE/$\overline{\text{BTL}}$, $\overline{\text{UP}}$, $\overline{\text{DOWN}}$	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\lvert I_{IL} \rvert$	Low-level input current - $\overline{\text{SHUTDOWN}}$, SE/$\overline{\text{BTL}}$	V_{DD} = 5.5 V, V_I = 0 V			900	nA
	Low-level input current - $\overline{\text{UP}}$, $\overline{\text{DOWN}}$	V_{DD} = 5.5 V, V_I = 0 V			125	µA
I_{DD}	Supply current	BTL mode - $\overline{\text{SHUTDOWN}}$ = 2 V, SE/$\overline{\text{BTL}}$ = $0.6 \times V_{DD}$		9	15	mA
		SE mode - $\overline{\text{SHUTDOWN}}$ = 2 V, SE/$\overline{\text{BTL}}$ = $0.8 \times V_{DD}$		4.5	7.5	
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{\text{SHUTDOWN}}$ = 0 V, SE/$\overline{\text{BTL}}$ = 0 V		150	300	µA

OPERATING CHARACTERISTICS

V_{DD} = 5 V, T_A= 25°C, R_L = 4 Ω, Gain = 20 dB, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	R_L = 3 Ω, f = 1 kHz	THD = 10%		2.8		W
			THD = 1%		2.3		
THD + N	Total harmonic distortion plus noise	P_O = 1 W, f = 20 Hz to 15 kHz			0.3%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	$C_{(BYP)}$ = 0.47 µF, f = 1 kHz	BTL mode		-65		dB
			SE mode, Gain = 14 dB		-60		
V_n	Noise output voltage	$C_{(BYP)}$ = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode, Gain = 6 dB		42		μV_{RMS}
			SE mode, Gain = 0 dB		44		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4, 6, 8, 10
		vs Voltage gain	2
		vs Frequency	3, 5, 7, 9, 11, 12
V_n	Output noise voltage	vs Frequency	13
	Supply ripple rejection ratio	vs Frequency	14, 15
	Crosstalk	vs Frequency	16, 17, 18
	Shutdown attenuation	vs Frequency	19
SNR	Signal-to-noise ratio	vs Frequency	20
	Closed loop response		21, 22
P_O	Output power	vs Load resistance	23, 24
P_D	Power dissipation	vs Output power	25, 26
		vs Ambient temperature	27
Z_i	Input impedance	vs Gain	28

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

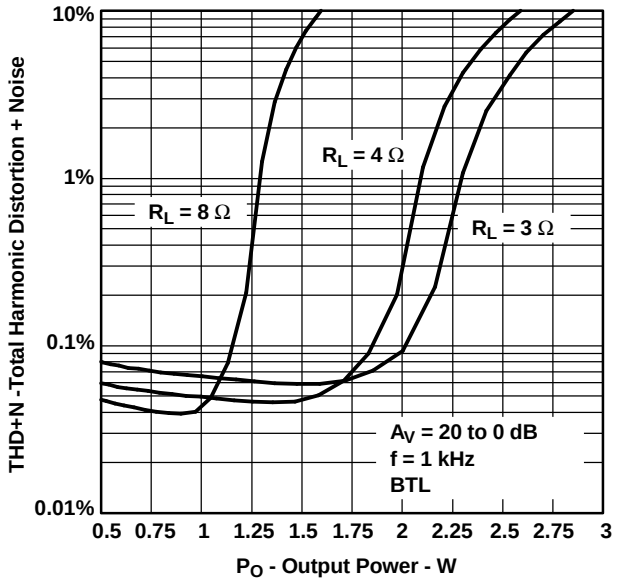


Figure 1.

TOTAL HARMONIC DISTORTION PLUS NOISE vs VOLTAGE GAIN

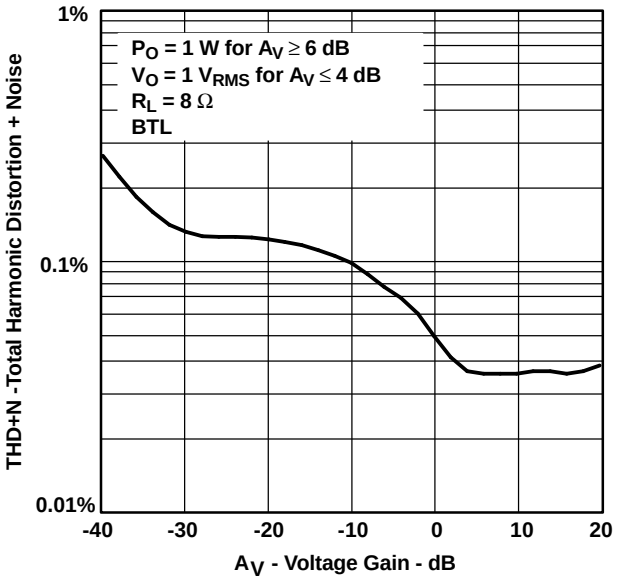


Figure 2.

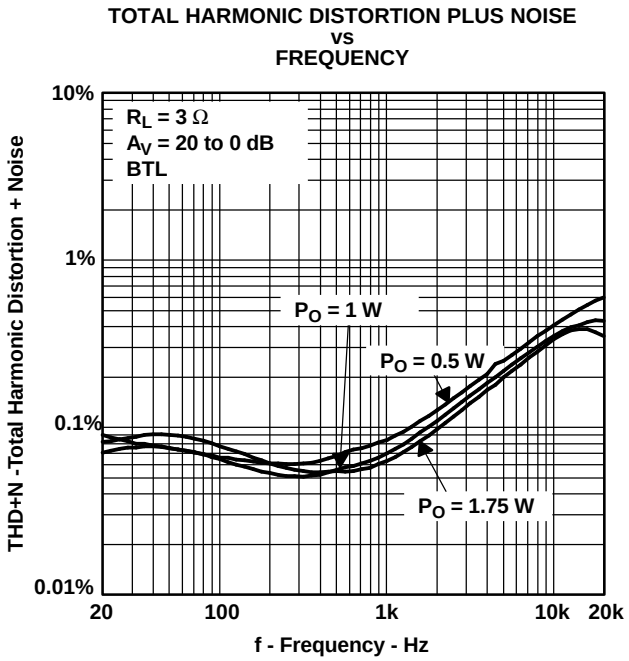


Figure 3.

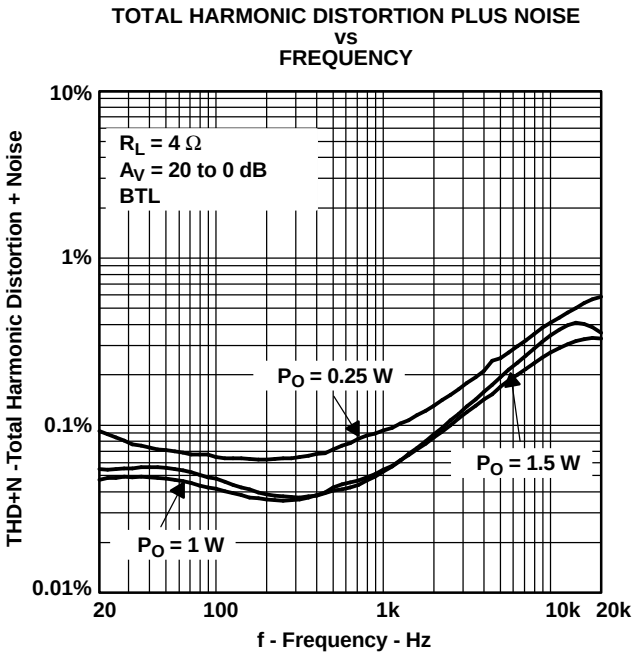


Figure 4.

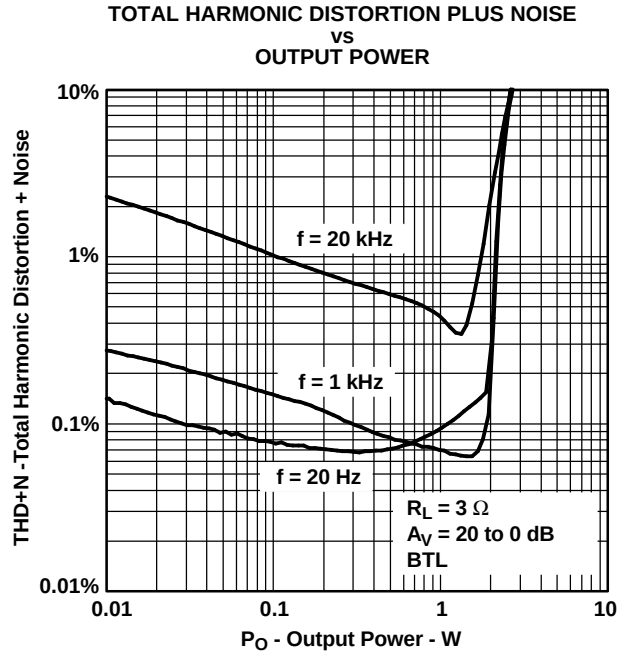
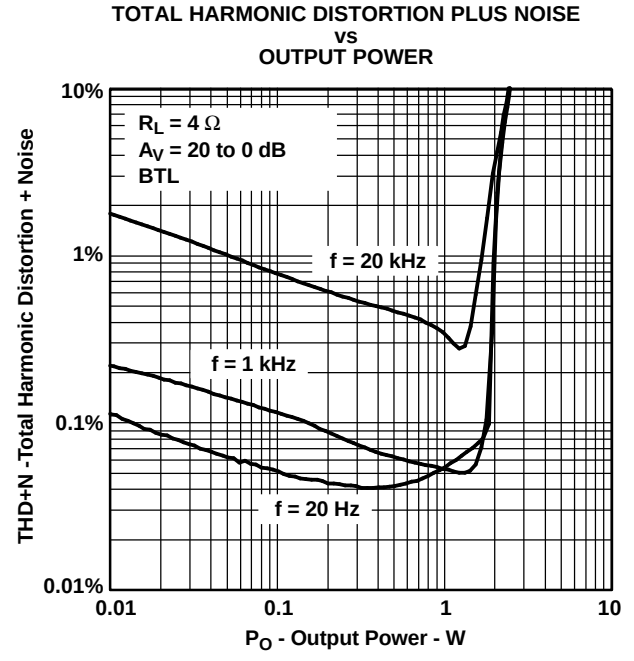


Figure 5.



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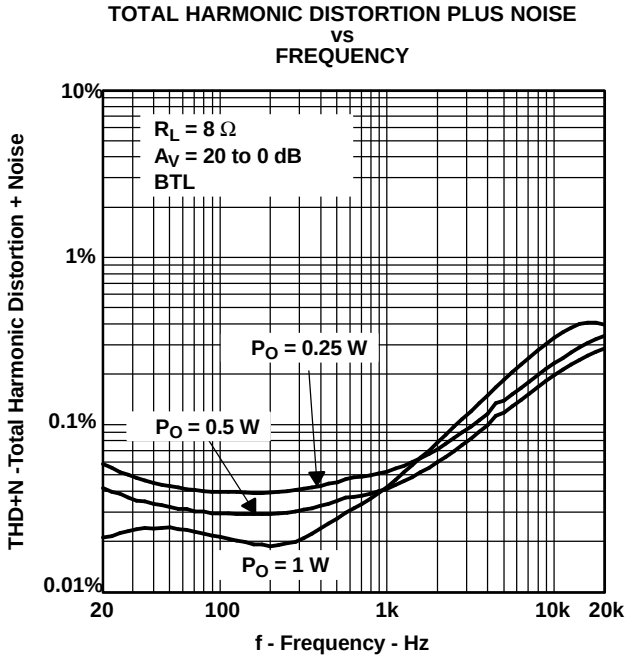

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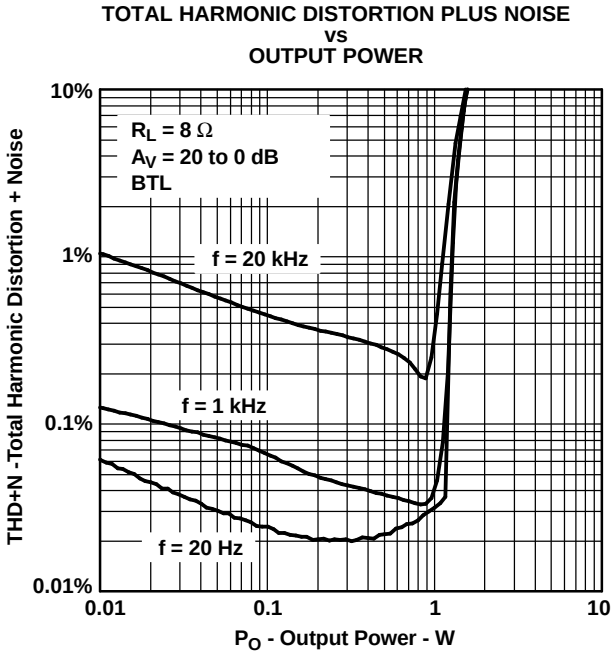
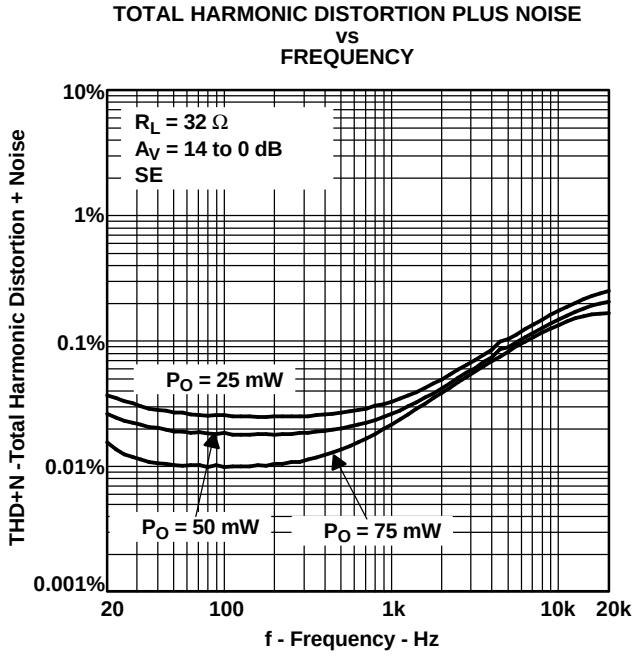


Figure 8.



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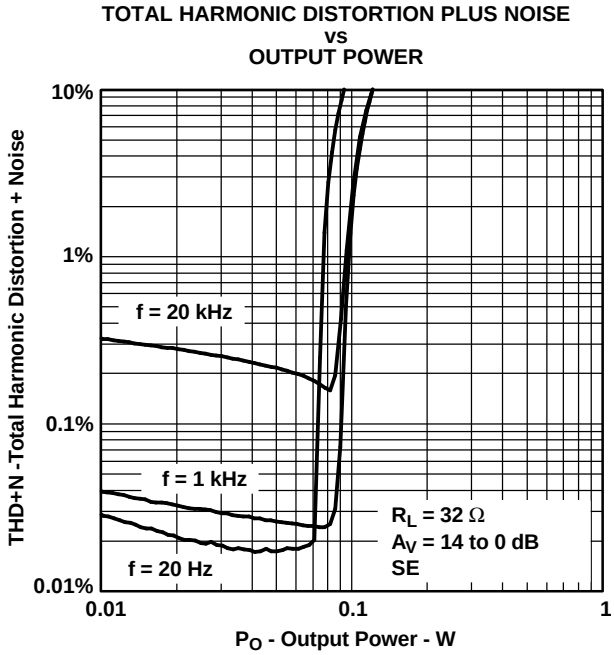


Figure 10.

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

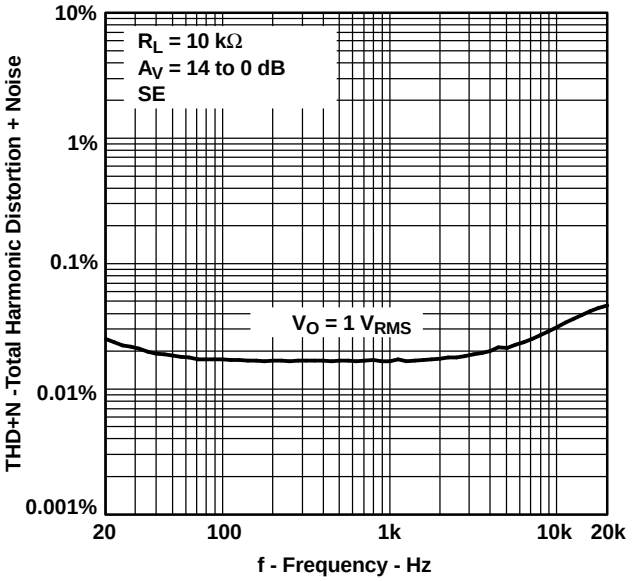


Figure 11.

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT VOLTAGE

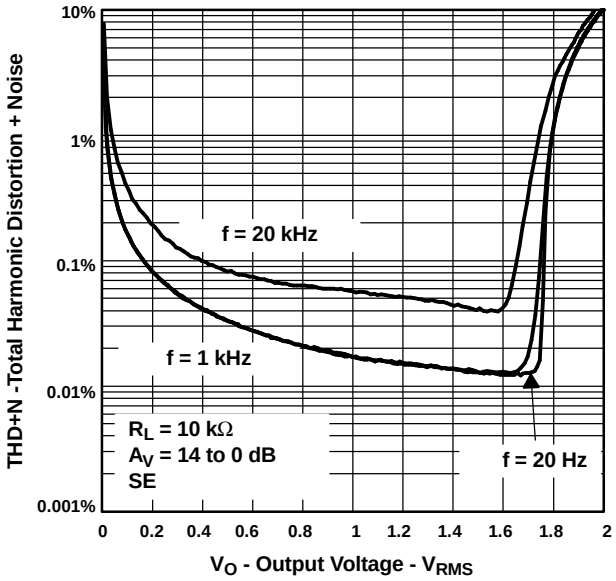


Figure 12.

OUTPUT NOISE VOLTAGE
vs
BANDWIDTH

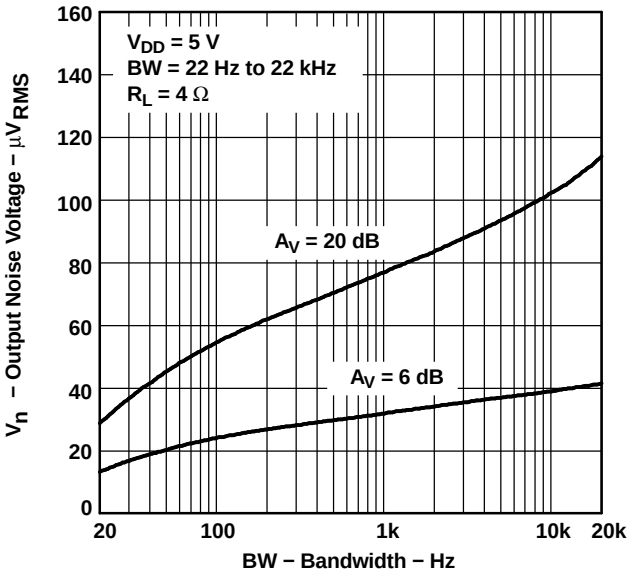
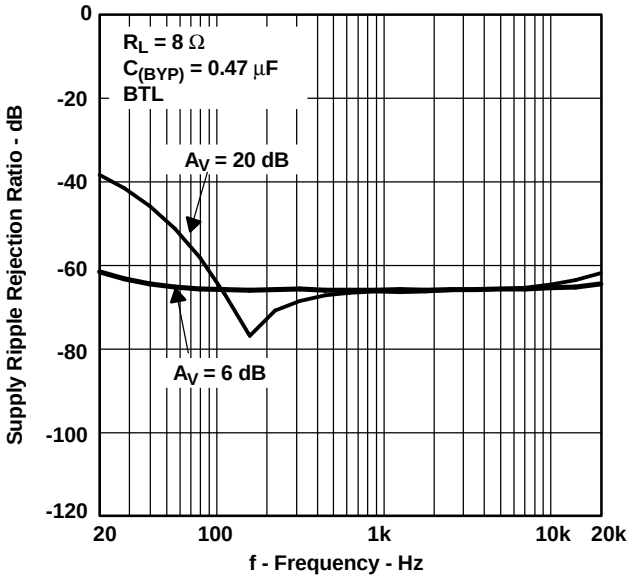


Figure 13.

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY



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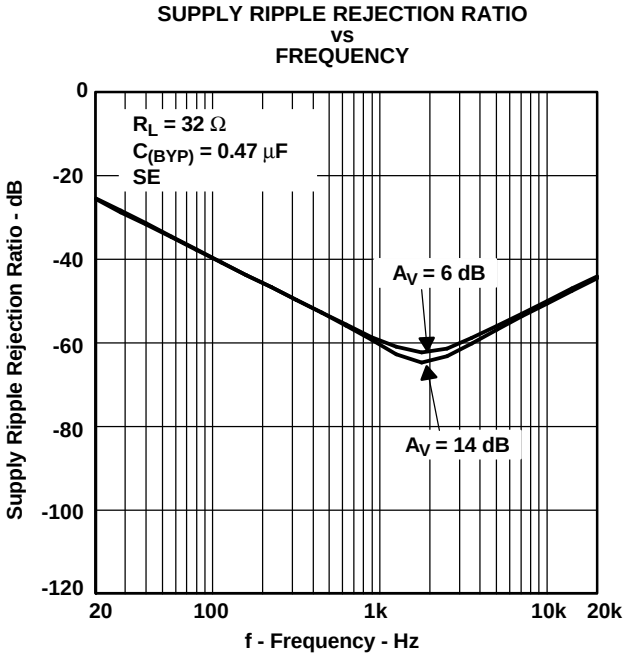


Figure 15.

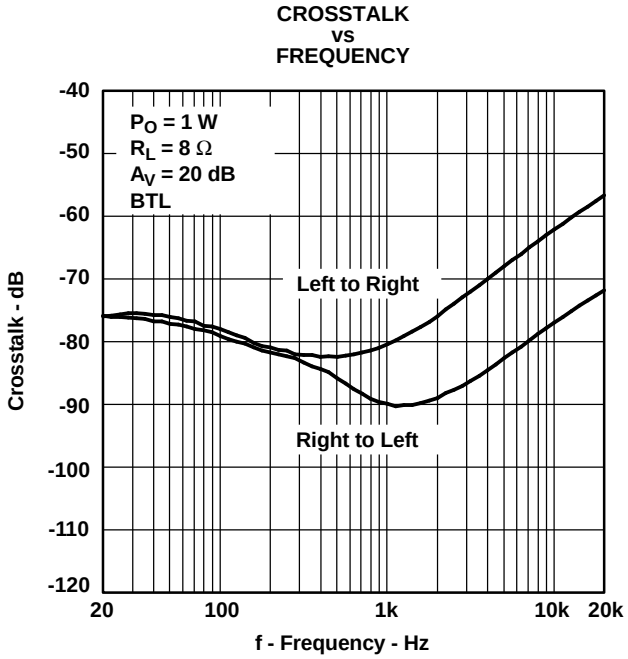


Figure 16.

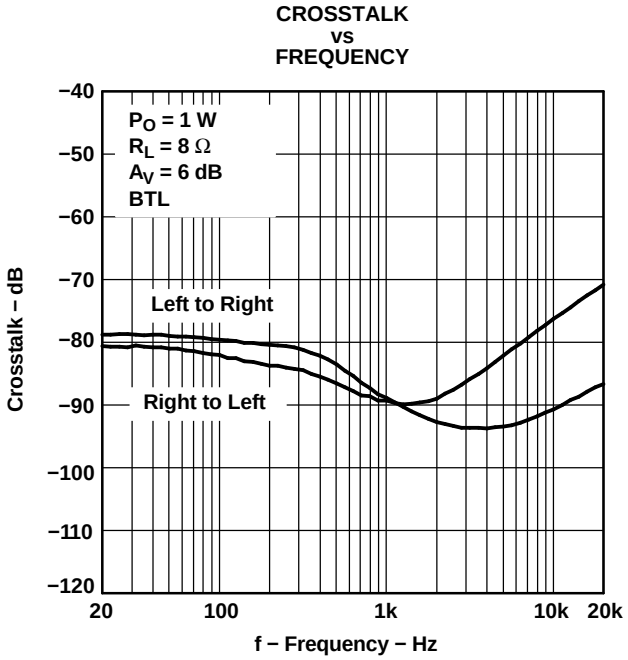
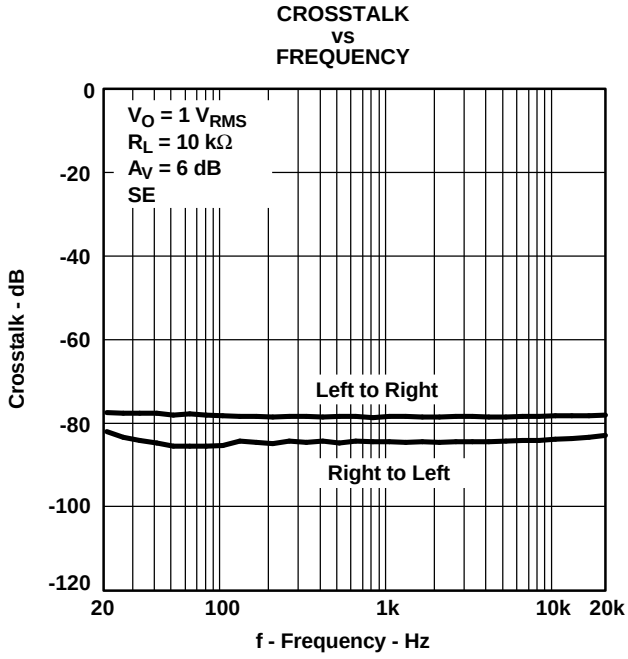


Figure 17.



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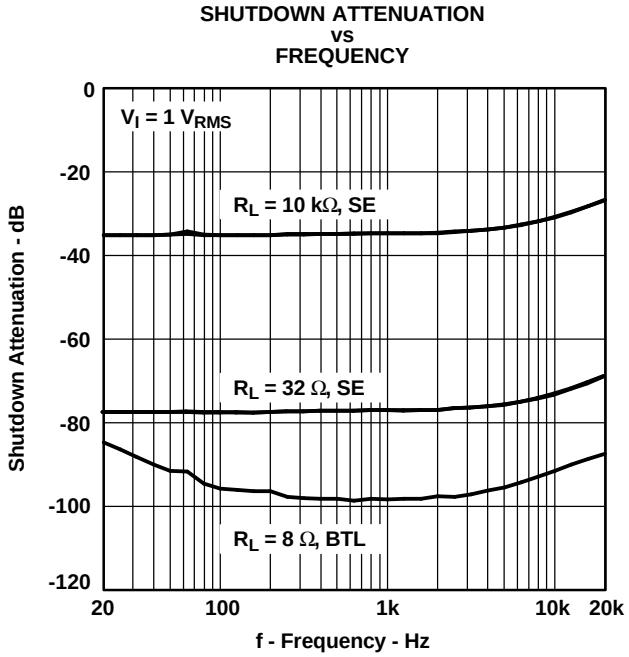


Figure 19.

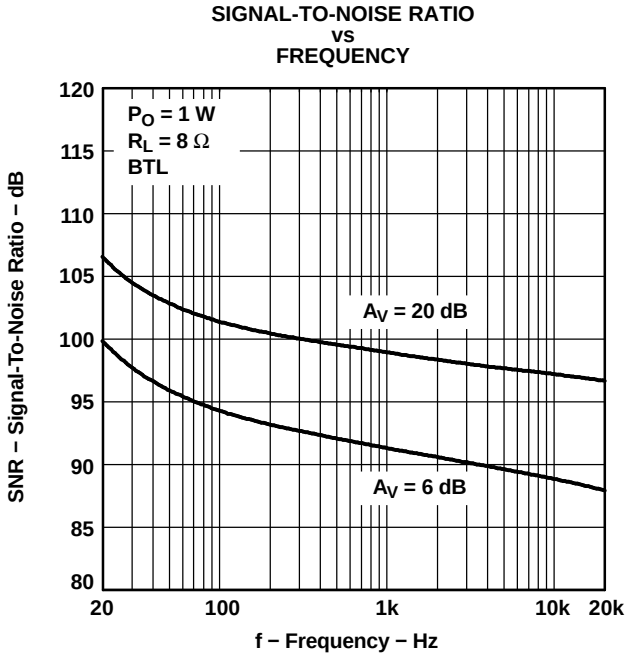


Figure 20.

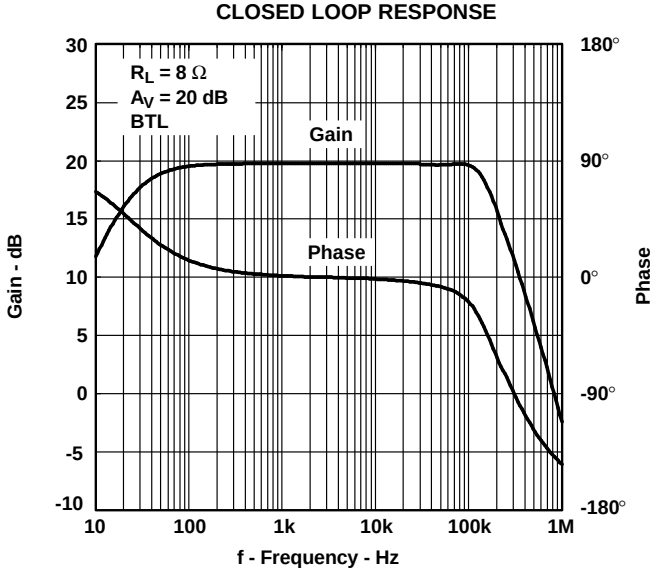


Figure 21.

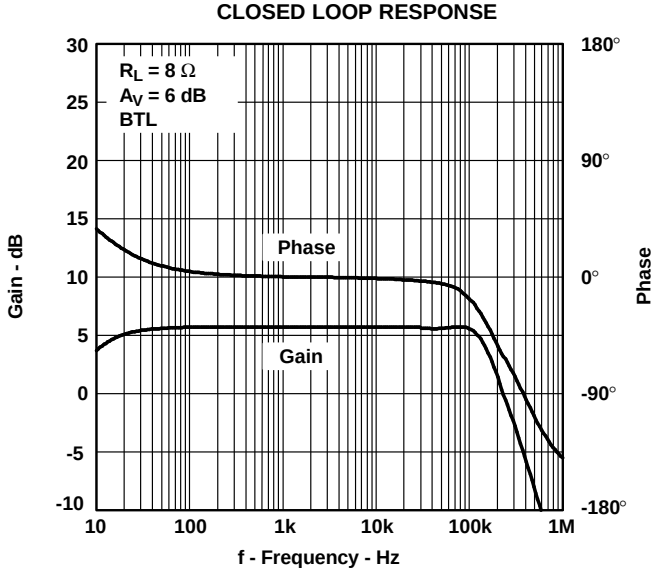


Figure 22.

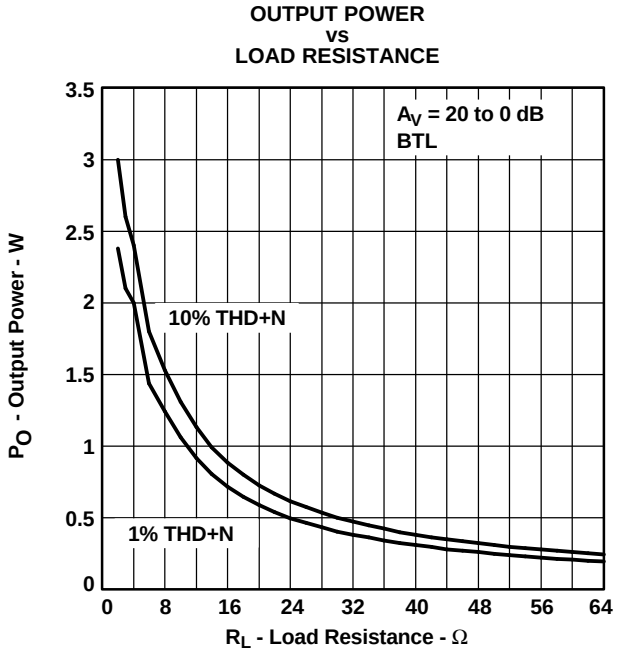
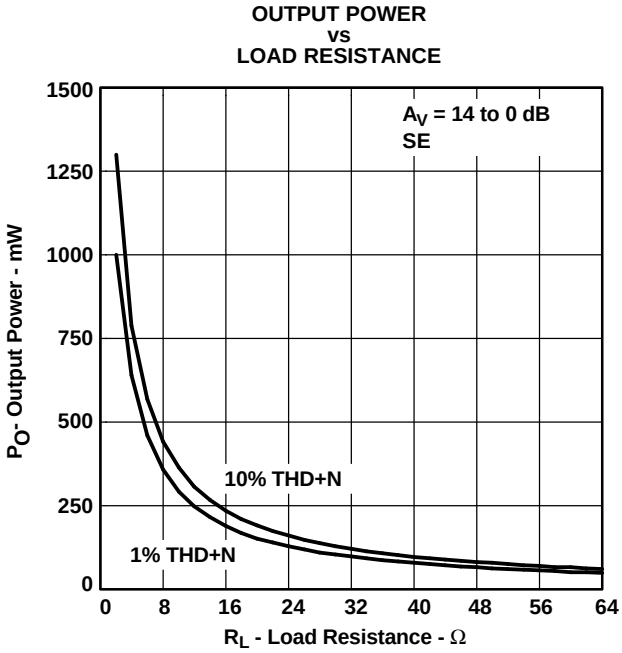


Figure 23.



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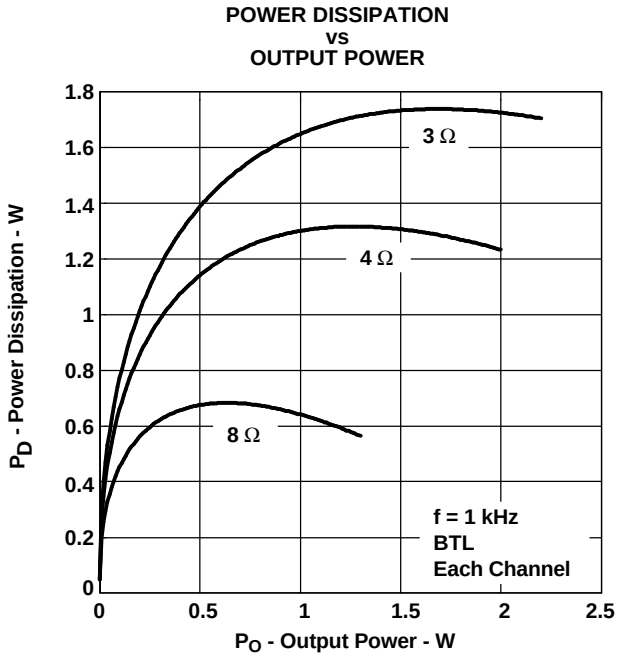
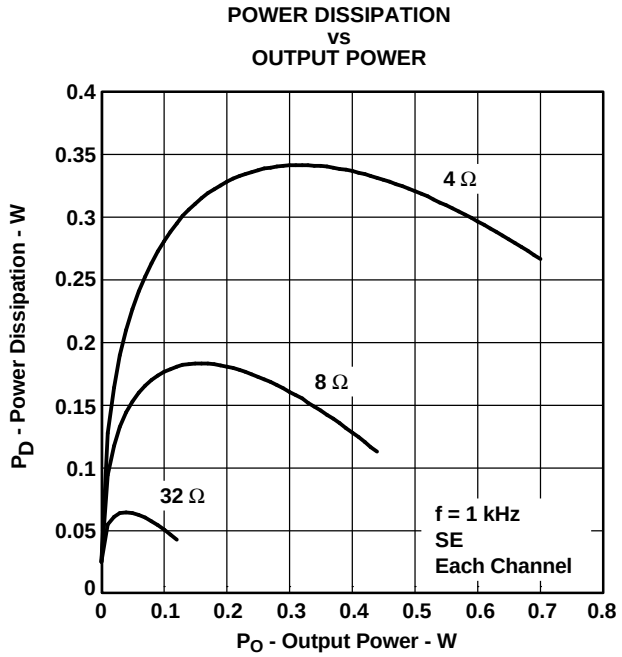


Figure 25.



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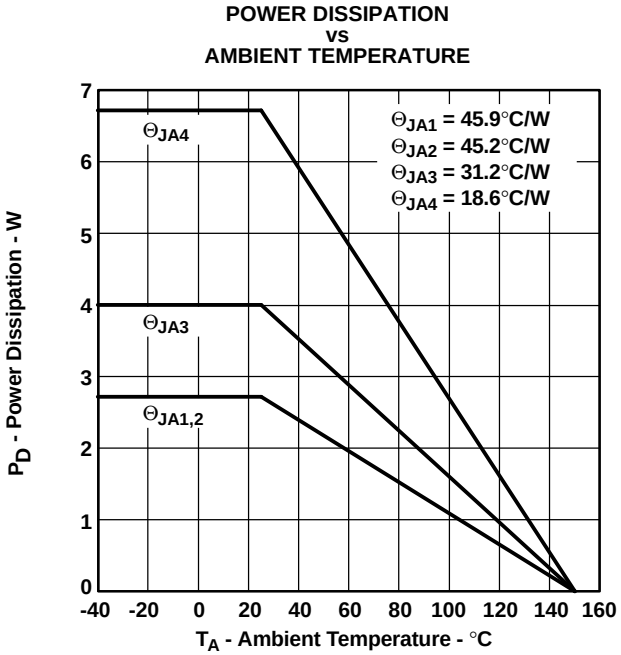

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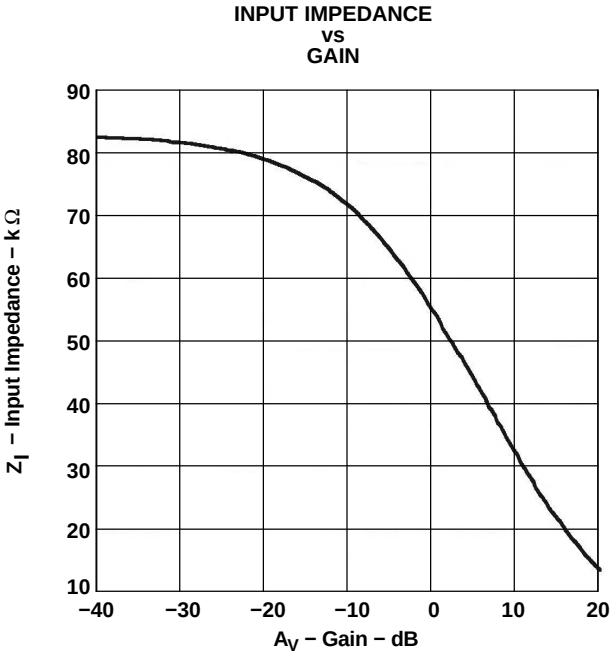


Figure 28.

APPLICATION INFORMATION

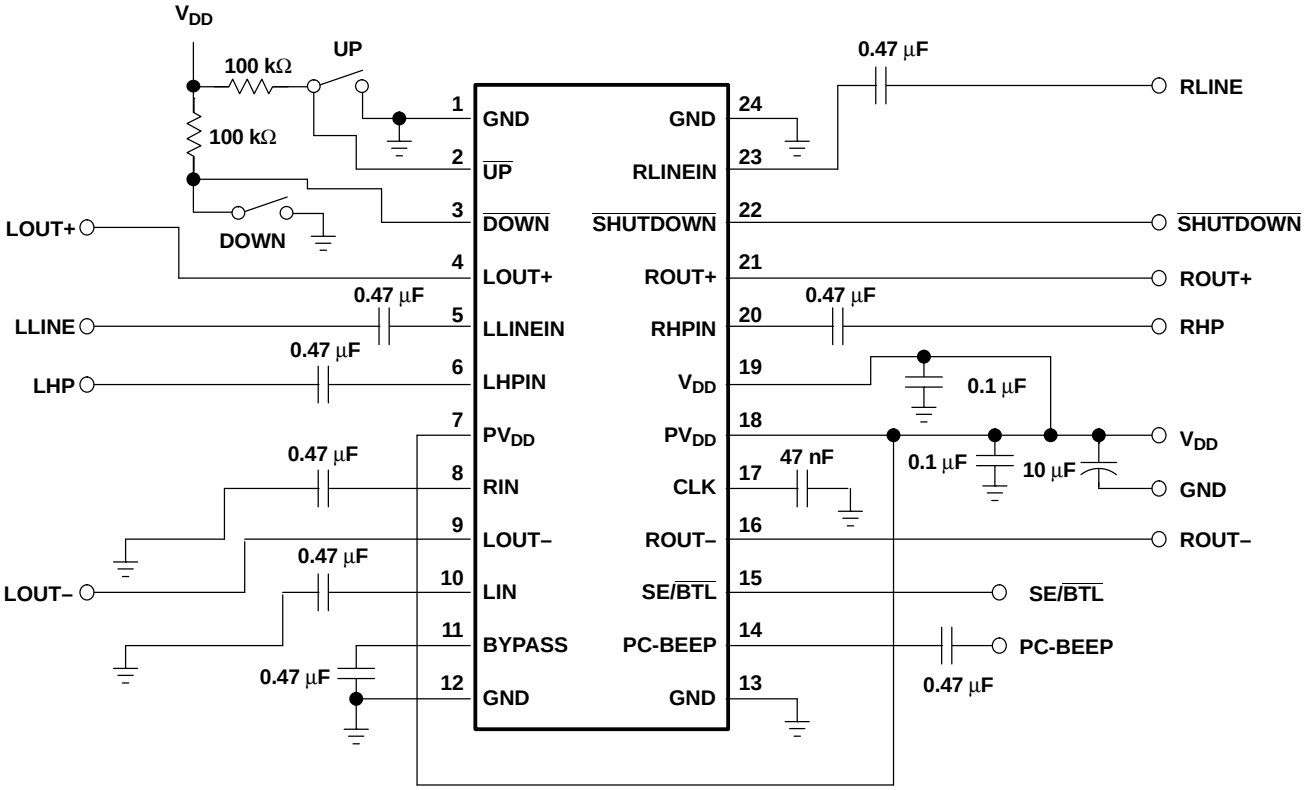
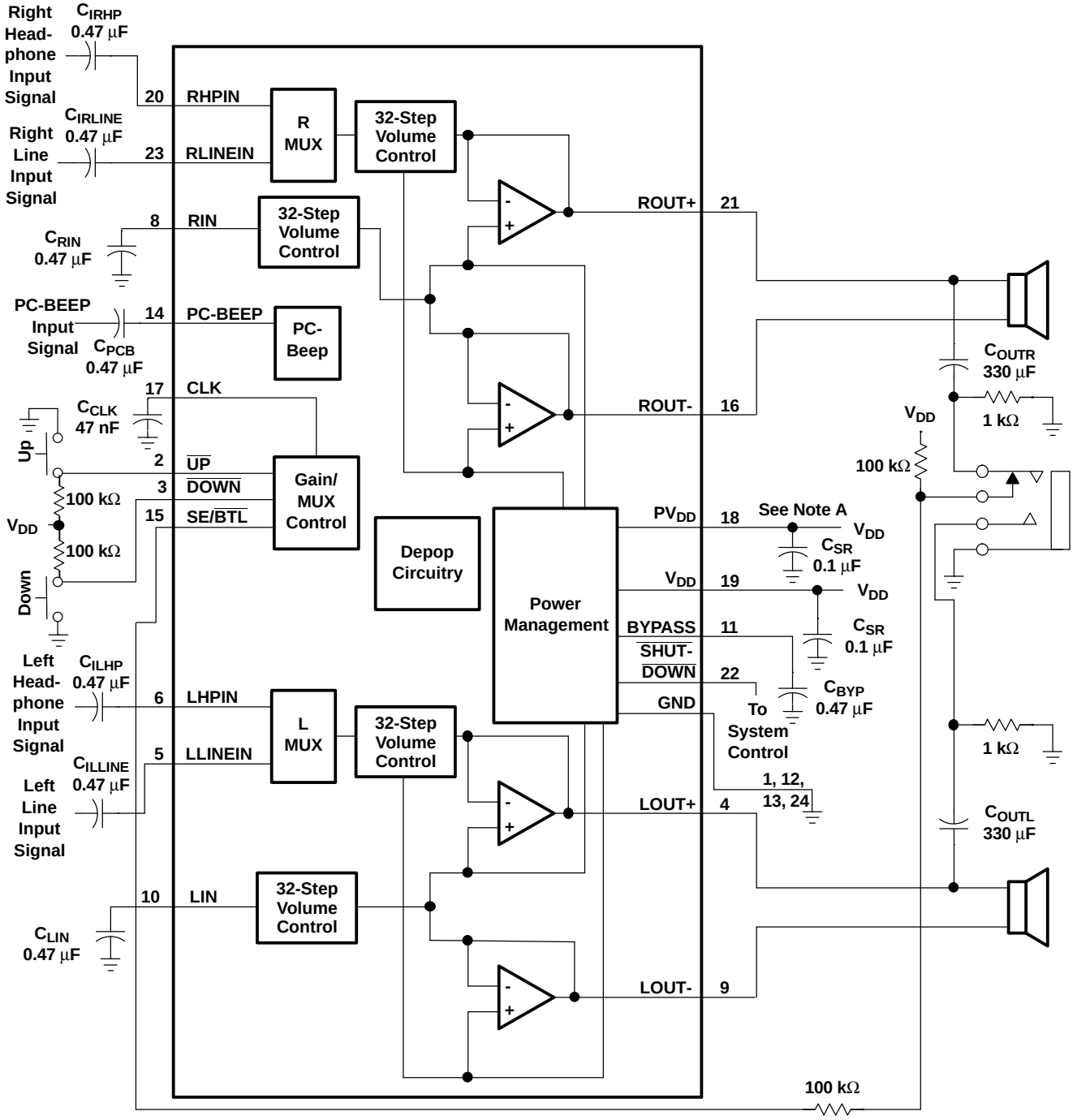


Figure 29. Typical TPA0152 Application Circuit

APPLICATION INFORMATION (continued)

COMPONENT SELECTION

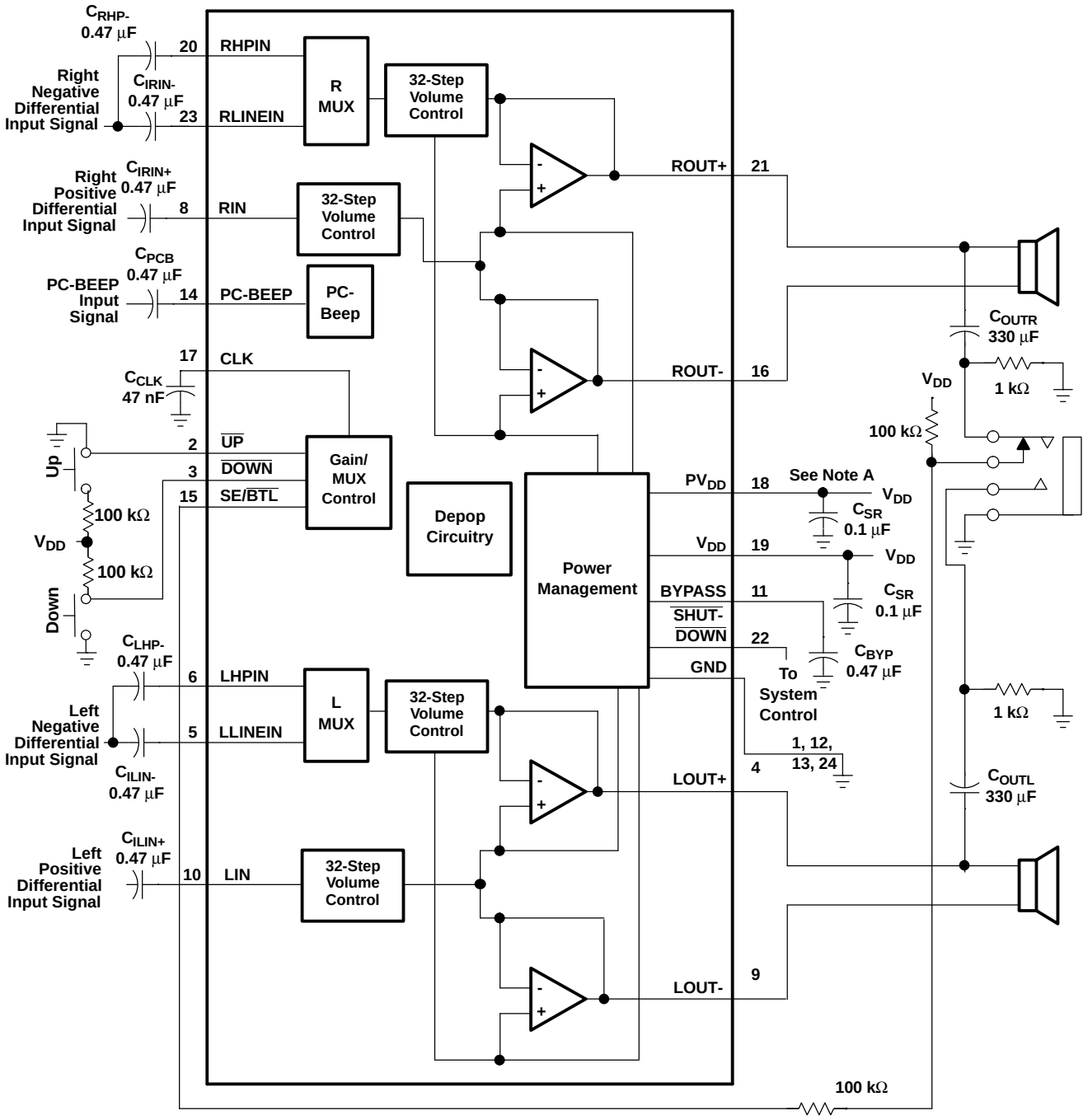
Figure 30 and Figure 31 are schematic diagrams of typical notebook computer application circuits.



NOTE: A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 30. Typical TPA0152 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION (continued)



NOTE: A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 31. Typical TPA0152 Application Circuit Using Differential Inputs

APPLICATION INFORMATION (continued)

UP/DOWN VOLUME CONTROL

Changing Volume

The default volume is set at mute mode. The volume is increased in 2-dB steps by pulling the $\overline{UP}$ terminal low. The volume is decreased in 2-dB steps by pulling the $\overline{DOWN}$ terminal low. If power is removed, the device resets to mute mode.

Volume Settings

VOLUME CONTROL	
BTL (dB)	**SE (dB)**
20	14
18	12
16	10
14	8
12	6
10	4
8	2
6	0
4	-2
2	-4
0	-6
-2	-8
-4	-10
-6	-12
-8	-14
-10	-16
-12	-18
-14	-20
-16	-22
-18	-24
-20	-26
-22	-28
-24	-30
-26	-32
-28	-34
-30	-36
-32	-38
-34	-40
-36	-42
-38	-44
-40	-46
-85	-91

Changing Volume When Using the Internal Clock

If using the internal clock, the maximum clock frequency is 500 Hz and the recommended frequency is 100 Hz using a 47-nF capacitor. Use Equation 1 to calculate the clock frequency if using a capacitor to generate the clock.

$$f_{CLK} = \frac{4.7 \times 10^{-6}}{C_{CLK}} \quad (1)$$

When the desired volume-control signal is pulled low for four clock cycles, the volume increments by one step, followed by a short delay. This delay decreases the longer the line is held low, eventually reaching a delay of zero. The delay allows the user to pull the $\overline{UP}$ or $\overline{DOWN}$ terminal low once for one volume change, or hold down to ramp several volume changes. The delay is optimally configured for push button volume control.

Holding either $\overline{UP}$ or $\overline{DOWN}$ low continuously causes the volume to change at an exponentially increasing rate. When f_{CLK} = 100 Hz, the first change in the volume occurs approximately 40 ms after either pin is initially pulled low. If the pin stays low for approximately 400 more ms, the volume changes again. The next change occurs 200 ms after this change. The fourth change occurs 120 ms after the third change. The fifth volume change occurs 80 ms after the fourth change. Thereafter, the volume changes at 1/4 the rate of the clock (every 40 ms).

Each cycle is registered on the rising clock edge and the volume is changed after the rising edge.

Figure 32 shows increasing volume using $\overline{UP}$, however, the volume is decreased using $\overline{DOWN}$ with the same timing.

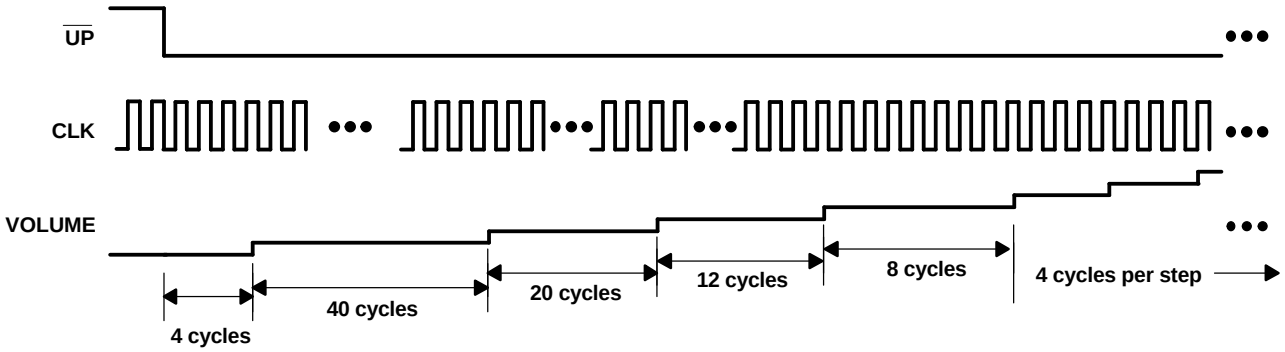


Figure 32. Internal Clock Timing Diagram

Changing Volume When Using the External Clock (Microprocessor Mode)

The user may remove the capacitor and run the external clock directly into the clock pin to override the internal clock generator. The maximum clock frequency is 10 kHz if using an external clock; however, a clock frequency less than 200 Hz is recommended in normal operation so the gain does not change too quickly causing a pop at the output. A 5-V, 50% duty-cycle clock must be used because the trip levels are 0.5 V and 4.5 V. The recommended way to adjust the volume is to use a gated clock and hold $\overline{UP}$ or $\overline{DOWN}$ low and cycle the clock pin four times to adjust the volume. The volume change is clocked in at the rising edge, so CLK should be held low when not changing volume. No delay is added when using an external clock, so it is very important to input only four clock cycles per volume change. Additional clock cycles per volume change are added to the next volume change. For example, if five clock cycles are input while $\overline{UP}$ is held low the first volume change, the volume change occurs after the third clock cycle the next time $\overline{UP}$ is held low. The figure below shows how volume increases with $\overline{UP}$ when an external clock is used. The sample and hold times for $\overline{UP}$ and $\overline{DOWN}$ are 100 ns. The same timing applies if using an external clock and decreasing the volume with $\overline{DOWN}$.

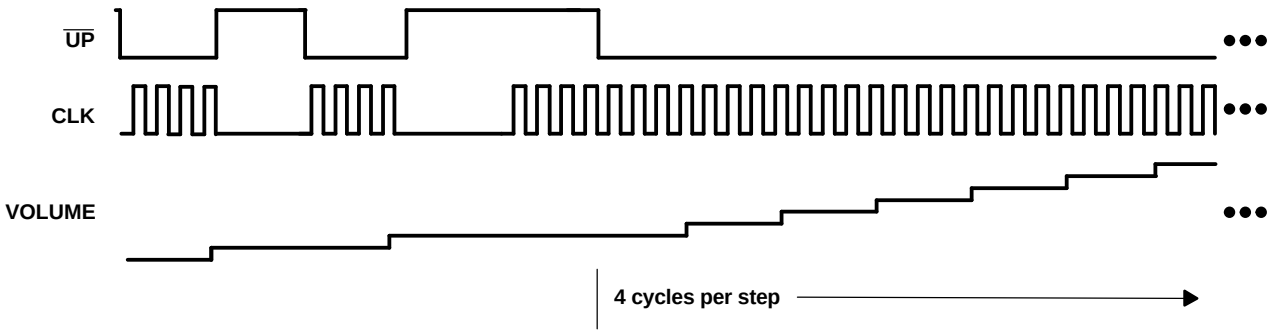


Figure 33. External Clock (4 Cycles Per Volume Change)

INPUT RESISTANCE

The gain is set by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency also changes by over six times. Connecting an additional resistor from the input pin of the amplifier to ground, as shown in Figure 34, reduces the cutoff-frequency variation.

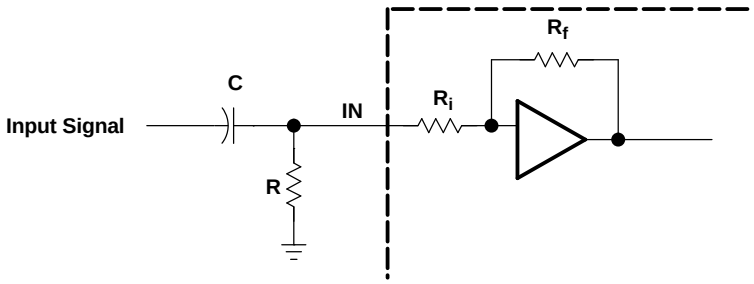


Figure 34. Resistor on Input for Cut-Off Frequency

The input resistance at each gain setting is given in the graph for Input Impedance vs Gain in the Typical Characteristics section.

The –3-dB frequency can be calculated using Equation 2.

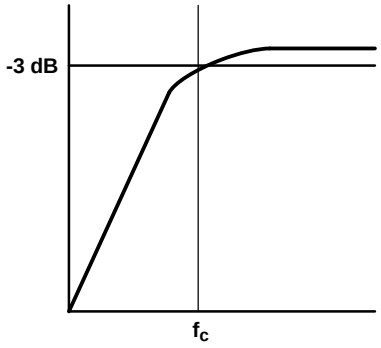
$$f_{-3\ dB} = \frac{1}{2\pi C\left(R \parallel R_i\right)} \quad (2)$$

To increase filter accuracy, increase the value of the capacitor and decrease the value of the resistor to ground. In addition, the order of the filter can be increased.

INPUT CAPACITOR, C_i

In the typical application an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_i) form a high-pass filter with the corner frequency determined in Equation 3.

$$f_{c(highpass)} = \frac{1}{2\pi Z_i C_i} \quad (3)$$



The value of C_i is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_i is 15 kΩ (see Figure 28) and the specification calls for a flat-bass response down to 40 Hz. Equation 3 is reconfigured as Equation 4.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (4)$$

In this example, C_i is 0.27 µF so one would likely choose a value in the range of 0.24 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher that the source dc level. Note that it is important to confirm the capacitor polarity in the application.

POWER SUPPLY DECOUPLING, $C_{(S)}$

This high-performance CMOS audio amplifier requires adequate power-supply decoupling to minimize output total harmonic distortion (THD). Power-supply decoupling also prevents oscillations with long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power-supply leads. To filter high-frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering low-frequency noise signals, an aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, $C_{(BYP)}$

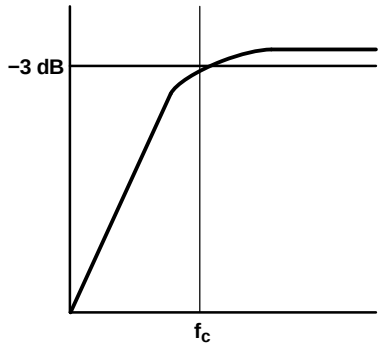
The midrail bypass capacitor, $C_{(BYP)}$, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, $C_{(BYP)}$ determines the rate at which the amplifier starts up. The second function is to reduce power-supply noise coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, and appears as degraded PSRR and THD+N.

Bypass capacitor ($C_{(BYP)}$) values of 0.47-µF to 1-µF, and ceramic or tantalum low-ESR capacitors are recommended for best THD and noise performance.

OUTPUT COUPLING CAPACITOR, $C_{(C)}$

In a typical single-supply SE configuration, an output coupling capacitor ($C_{(C)}$) is required to block the dc bias at the output of the amplifier to prevent dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 5.

$$f_{c(high)} = \frac{1}{2\pi R_L C_{(C)}} \quad (5)$$



The main disadvantage, from a performance standpoint, is that load impedances are typically small, driving the low-frequency corner higher, degrading the bass response. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 330 µF is chosen and loads include 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	$C_{(C)}$	LOWEST FREQUENCY
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 1 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

BRIDGED-TIED LOAD VS SINGLE-ENDED MODE

Figure 35 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA0152 amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but, initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Substituting $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see Equation 6).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \quad (6)$$

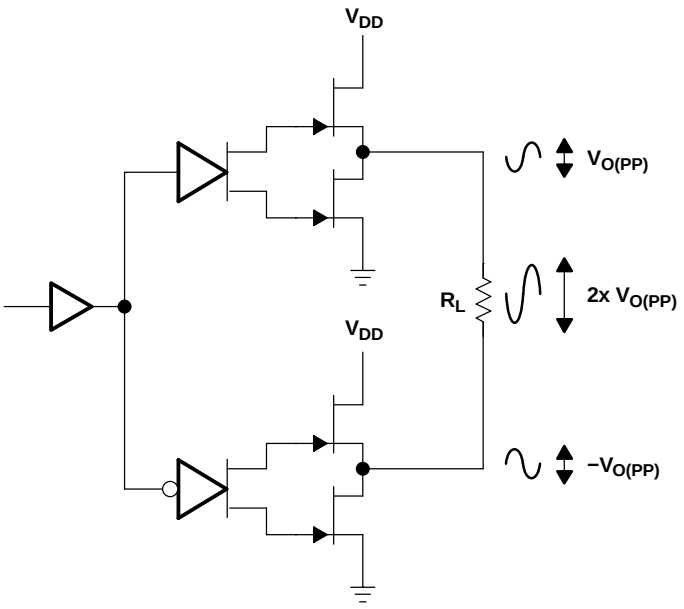


Figure 35. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power, this is a 6-dB improvement — loudness that can be heard. In addition to increased power there are frequency-response concerns. Consider the single-supply SE configuration shown in Figure 36. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF), so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting the low-frequency performance of the system. This frequency-limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance, and is calculated with Equation 7.

$$f_{(c)} = \frac{1}{2\pi R_L C_{(C)}} \quad (7)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, eliminating the need for blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

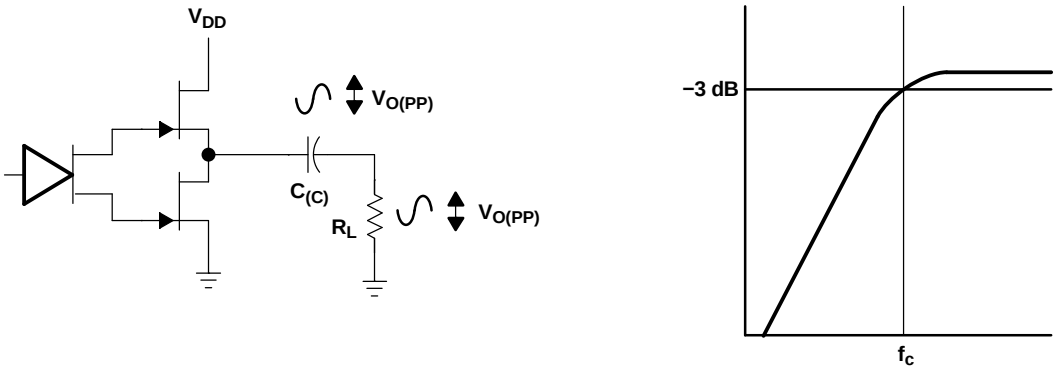


Figure 36. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable, since the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *Crest Factor and Thermal Considerations* section.

Single-Ended Operation

In SE mode (see Figure 36), the load is driven from the primary amplifier output for each channel (LOUT+ and ROUT+).

The amplifier switches to single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain by 6 dB.

BTL AMPLIFIER EFFICIENCY

Class-AB amplifiers are inefficient, primarily because of voltage drop across the output-stage transistors. The two components of the internal voltage drop are the headroom or dc voltage drop that varies inversely to output power, and the sine wave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current (I_{DD}rms) determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency begins as the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveforms must be understood (see Figure 37).

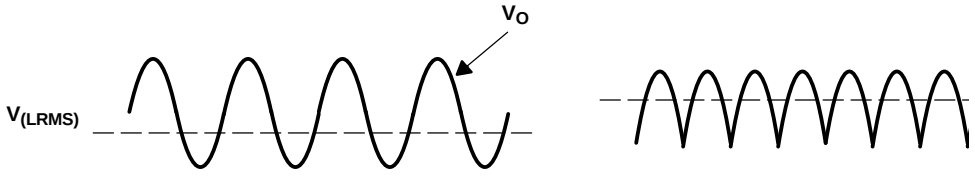


Figure 37. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application, the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. Therefore, RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. Equation 8 and Equation 9 are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and} \quad P_{SUP} = V_{DD}\, I_{DD}avg \qquad \text{and} \qquad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = -\frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

Where:

$$V_P = \sqrt{2\, P_L\, R_L} \tag{8}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2\, P_L\, R_L}}{4\, V_{DD}}$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

(9)

Table 2 employs Equation 9 to calculate efficiencies for four different output-power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half-power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 2. Efficiency vs Output Power in 5-V, 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47(1)	0.53

(1) High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in Equation 9, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

CREST FACTOR AND THERMAL CONSIDERATIONS

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom, above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the data sheet, one can see that when the device is operating from a 5-V supply into a 3-Ω speaker that 4-W peaks are available. Use Equation 10 to convert watts to dB.

$$P_{dB} = 10 \text{Log} \frac{P_W}{P_{ref}} = 10 \text{Log} \frac{4\ W}{1\ W} = 6\ dB \quad (10)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB - 15 dB = -9 dB (15-dB crest factor)
6 dB - 12 dB = -6 dB (12-dB crest factor)
6 dB - 9 dB = -3 dB (9-dB crest factor)
6 dB - 6 dB = 0 dB (6-dB crest factor)
6 dB - 3 dB = 3 dB (3-dB crest factor)

Converting dB back into watts:

$P_W = 10^{PdB/10} \times P_{ref}$
= 63 mW (18-dB crest factor)
= 125 mW (15-dB crest factor)
= 250 mW (9-dB crest factor)
= 500 mW (6-dB crest factor)
= 1000 mW (3-dB crest factor)
= 2000 mW (0-dB crest factor)

This is valuable information to consider when estimating the heat-dissipation requirements for the amplifier system. Comparing the worst case, 2 W of continuous power output with a 3-dB crest factor, against 12-dB and 15-dB applications, drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation and maximum ambient temperatures are shown in the table below.

Table 3. TPA0152 Power Rating, 5-V, 3-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	-3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.3	24°C
4	250 mW (12 dB)	1	51°C
4	125 mW (15 dB)	0.9	78°C
4	63 mW (18 dB)	0.6	85°C(1)

(1) Package limited to 85°C ambient.

Table 4. TPA0152 Power Rating, 5-V, 8-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
2.5	1250 mW (3-dB crest factor)	0.53	85°C(1)
2.5	1000 mW (4-dB crest factor)	0.59	85°C(1)
2.5	500 mW (7-dB crest factor)	0.62	85°C(1)
2.5	250 mW (10-dB crest factor)	0.55	85°C(1)

(1) Package limited to 85°C ambient.

The maximum dissipated power (P_{Dmax}) is reached at a much lower output power level for a 3-Ω load than for an 8-Ω load. As a result, the formula in Equation 11for calculating P_{Dmax} may be used for a 3-Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{11}$$

However, in the case of an 8-Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for an 8-Ω load, but do not exceed the maximum ambient temperature of 85°.

The maximum ambient temperature depends on the heatsinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table. Converting this to θ_{JA}:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \tag{12}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per-channel, so the dissipated heat is doubled for two-channel operation. Given θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated using Equation 13. The maximum recommended junction temperature for the device is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$\begin{aligned} T_A\,\text{Max} &= T_J\,\text{Max} - \theta_{JA} P_D \\ &= 150 - 45(0.6 \times 2) = 96°C \text{ (15-dB crest factor)} \end{aligned} \tag{13}$$

NOTE:

Internal dissipation of 0.6 W is estimated for a 2-W system with 15-dB crest factor per channel.
Due to package limitiations, the actual T_{AMAX} is 85°C.

The power rating tables show that for some applications, no airflow is required to keep junction temperatures in the specified range. The internal thermal protection turns the device off at junction temperatures higher than 150°C to prevent damage to the IC. The power rating tables in this section were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

SE/$\overline{\text{BTL}}$ OPERATION

The ability of the TPA0152 to easily switch between BTL and SE modes is one of its most important cost-saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Two separate internal amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input controls the operation of the follower amplifier that drives LOUT– and ROUT–. When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the device is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output-impedance state, which configures the device outputs as SE drivers from LOUT+ and ROUT+. I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor-divider network as shown in Figure 38.

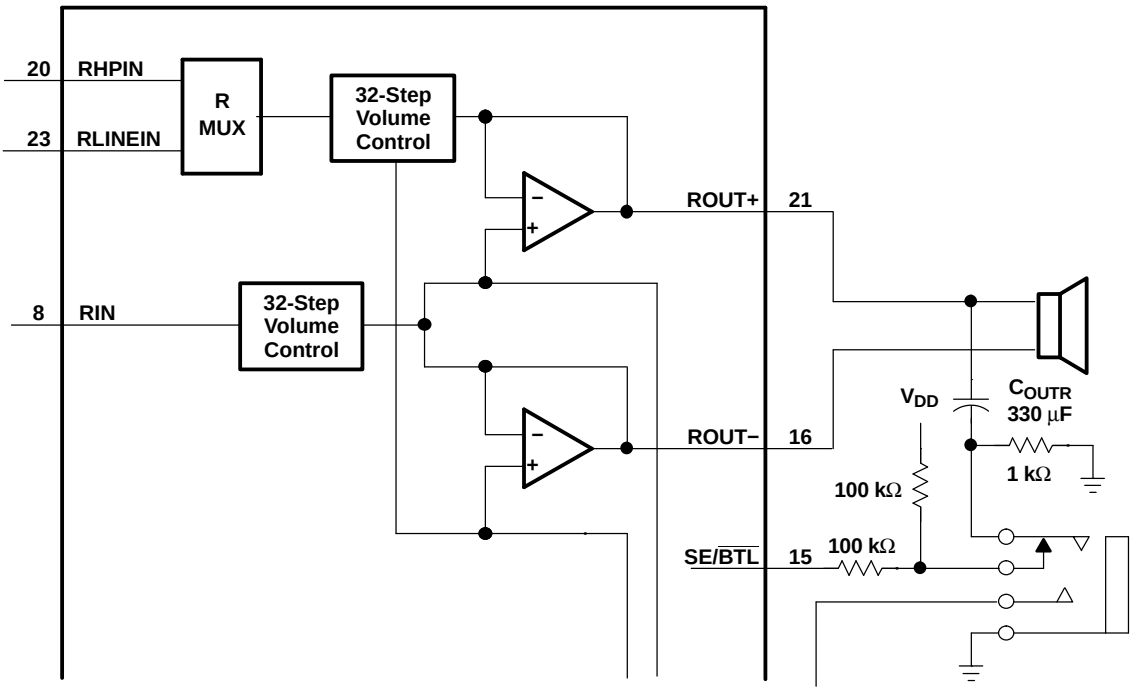


Figure 38. TPA0152 Resistor Divider Network Circuit

Using a readily-available 1/8-in. (3,5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed, the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shut down, muting the speaker (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

PC-BEEP OPERATION

The PC-BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is activated automatically. When the PC-BEEP input is active, both LINEIN and HPIN inputs are deselected, and both the left and right channels are driven in BTL mode with the signal from PC-BEEP. The gain from the PC-BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC-BEEP input is deselected, the amplifier returns to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC-BEEP takes the device out of shutdown, outputs the PC-BEEP signal, then returns the amplifier to shutdown mode.

The preferred input signal is a square wave or pulse train. To be accurately detected, the signal must have a minimum of 1.5-V_{pp} amplitude, rise and fall times of less than 0.1 µs and a minimum of eight rising edges. When the signal is no longer detected, the amplifier returns to its previous operating mode and volume setting.

To ac-couple the PC-BEEP input, choose a coupling-capacitor value to satisfy Equation 14.

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB}(100\ k\Omega)} \quad (14)$$

The PC-BEEP input can also be dc-coupled to avoid using this coupling capacitor. The pin normally rests at midrail when no signal is present.

INPUT MUX OPERATION

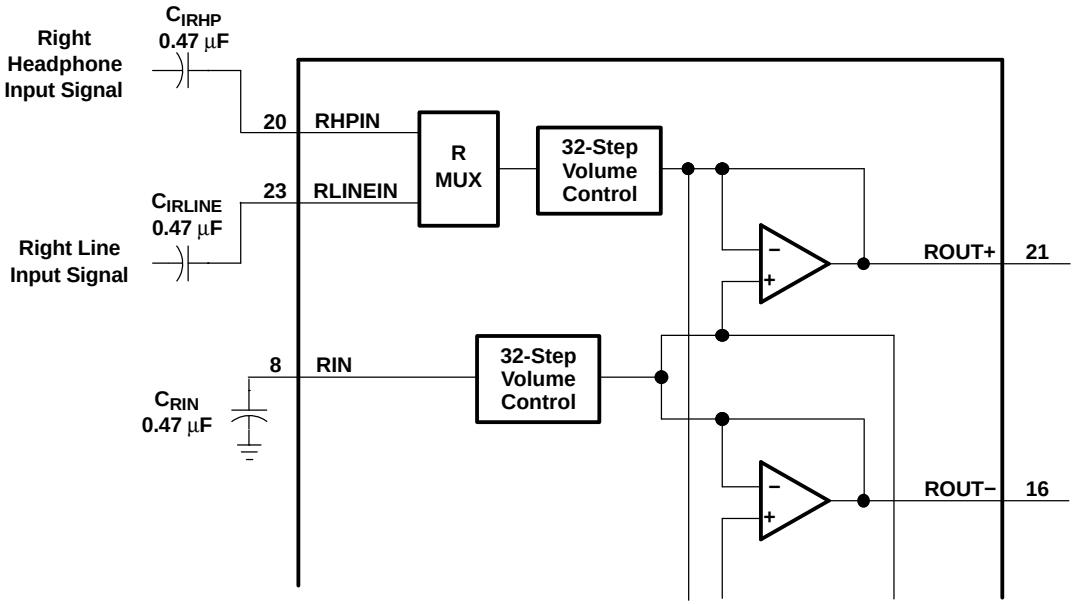


Figure 39. TPA0152 Example Input MUX Circuit

The input MUX provides the user with a means to select from two different audio sources. In BTL mode, the LINE input is selected. In SE mode, the HP inputs are selected. RLINEIN and LLINEIN must be AC-grounded in SE mode.

SHUTDOWN MODES

The TPA0152 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 150 µA. $\overline{\text{SHUTDOWN}}$ must not be left unconnected because amplifier operation would be unpredictable.

Shutdown and Mute Mode Functions

INPUTS(1)		AMPLIFIER STATE	
SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
Low	High	Line	BTL
X	Low	X	Mute
High	High	HP	SE

(1) Do not leave inputs unconnected.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA0152PWP	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0152
TPA0152PWP.A	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0152
TPA0152PWPR	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0152
TPA0152PWPR.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0152

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

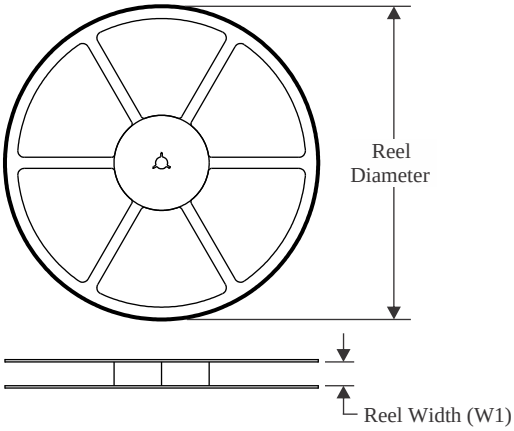
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

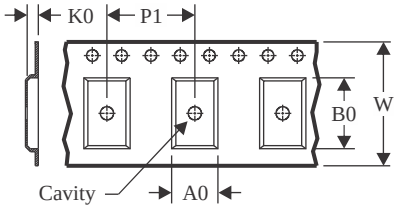
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

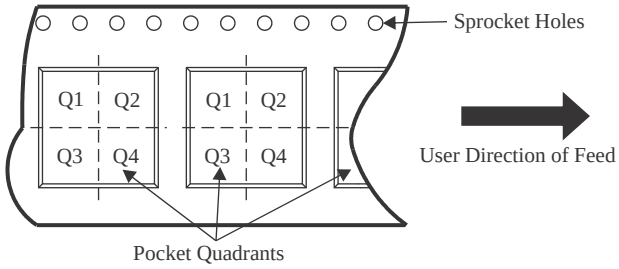


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

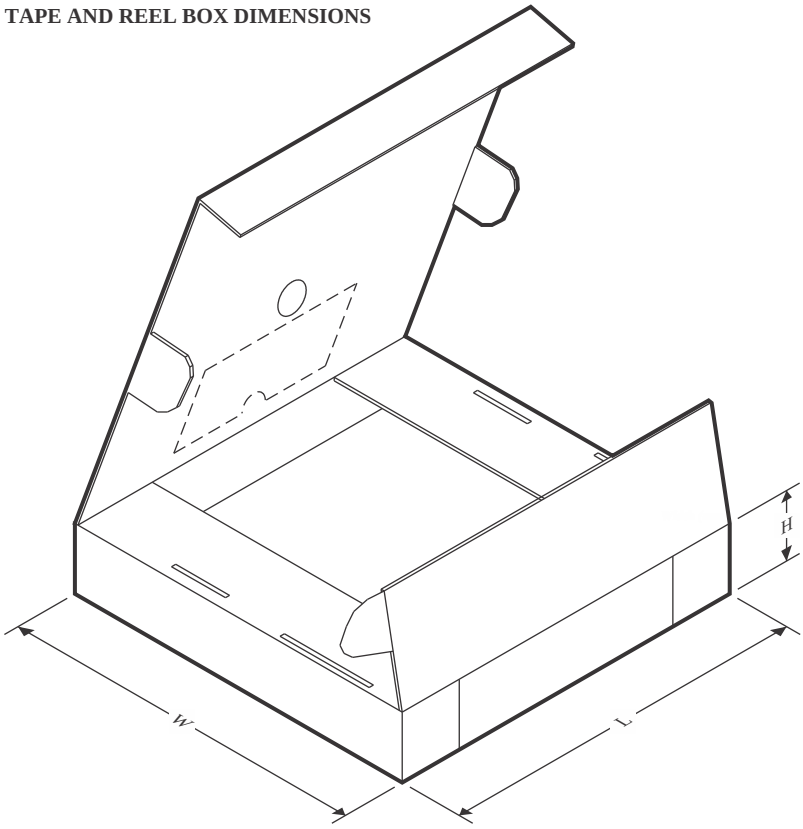
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA0152PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

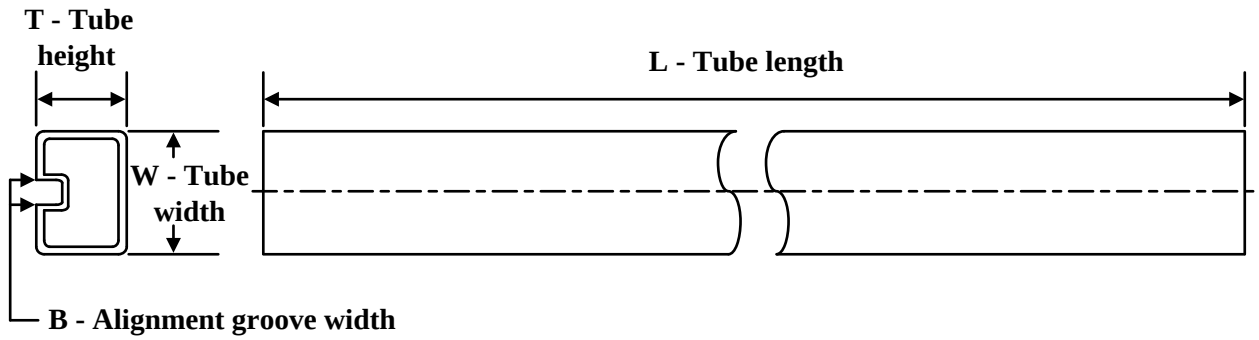
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA0152PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA0152PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TPA0152PWP.A	PWP	HTSSOP	24	60	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

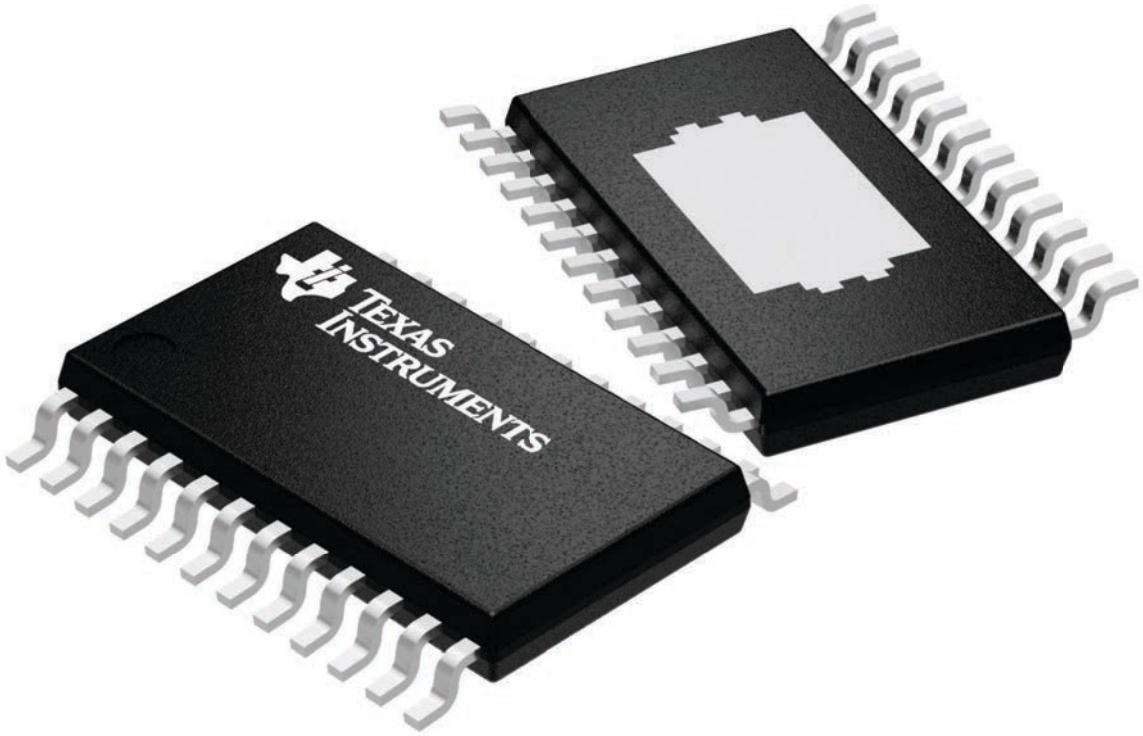
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

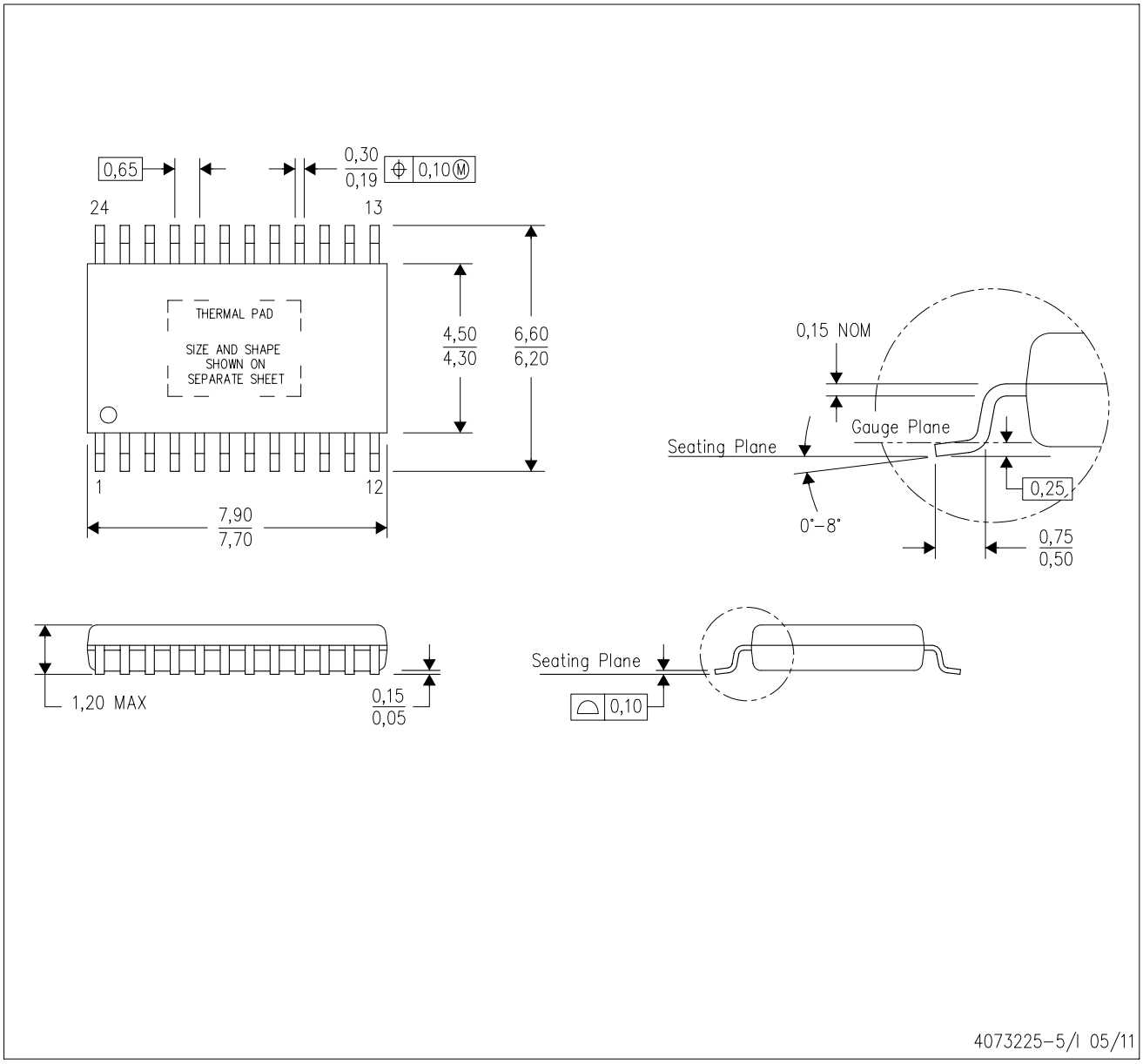
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

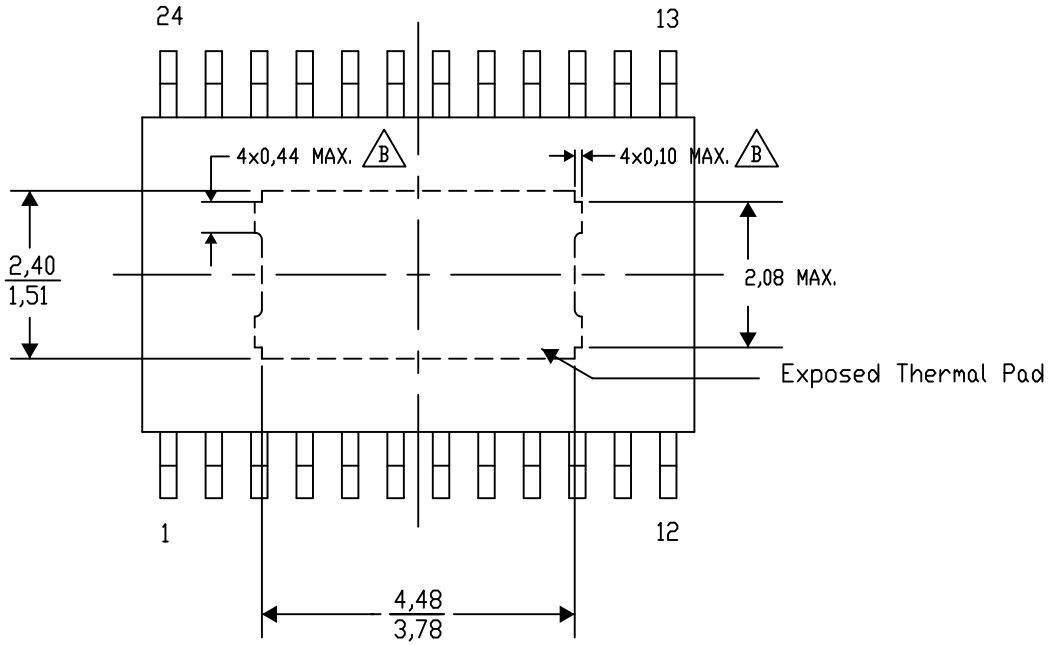
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–42/AO 01/16

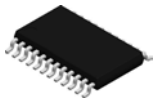
NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

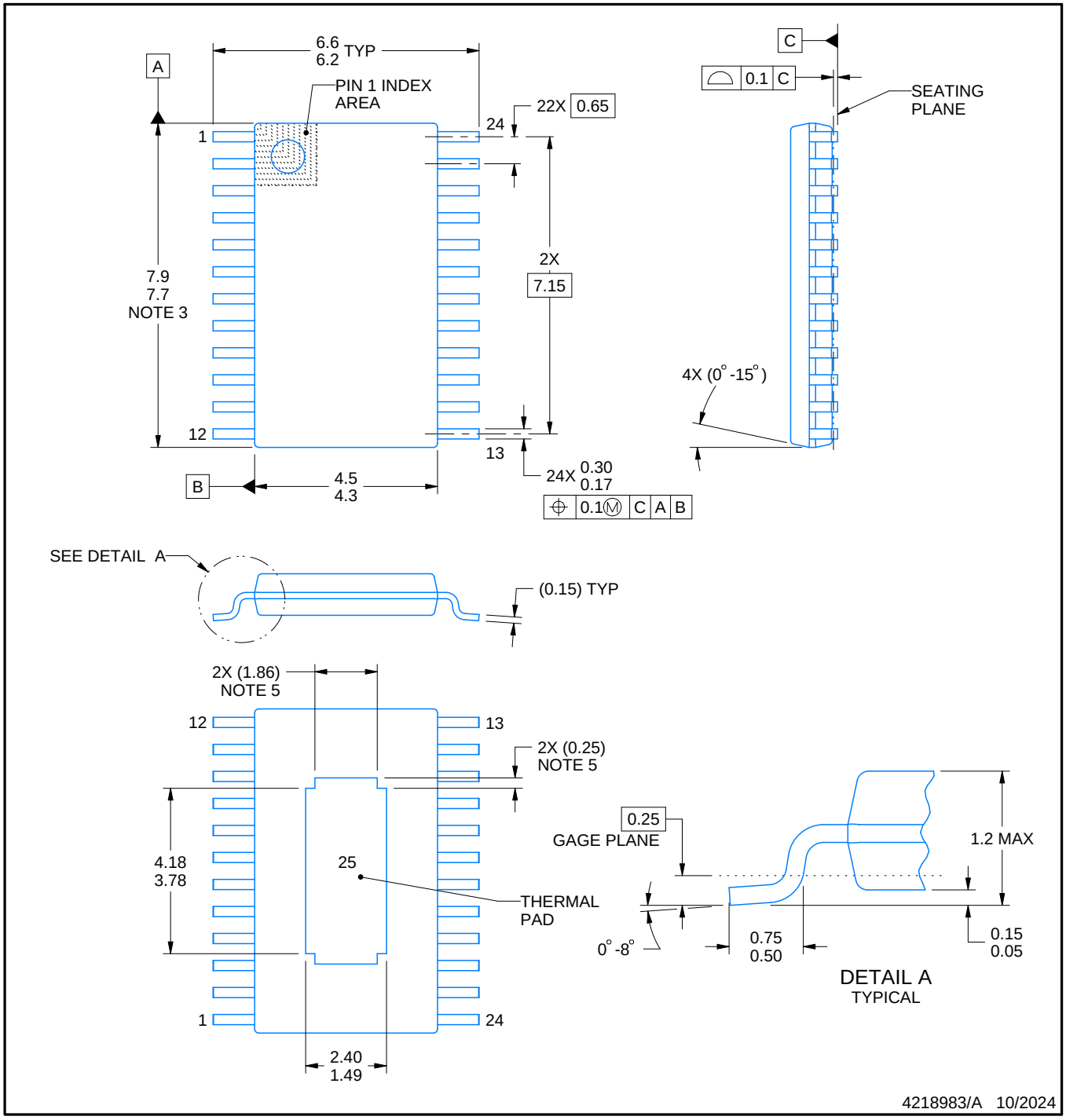
PACKAGE OUTLINE

PWP0024A



PowerPAD™ TSSOP - 1.2 mm max height

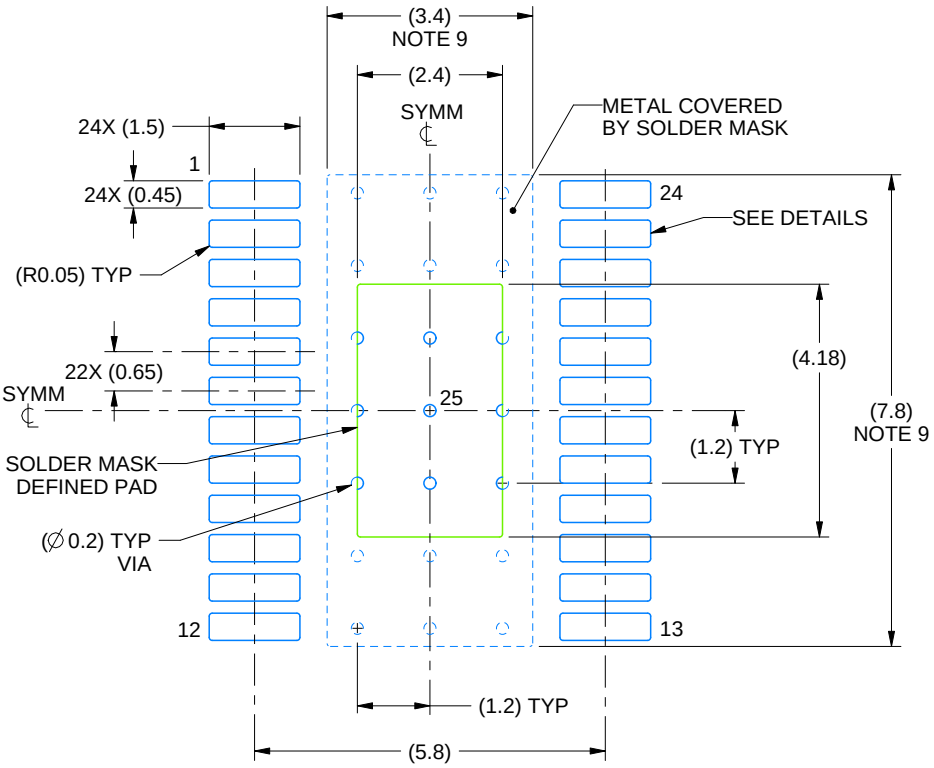
SMALL OUTLINE PACKAGE



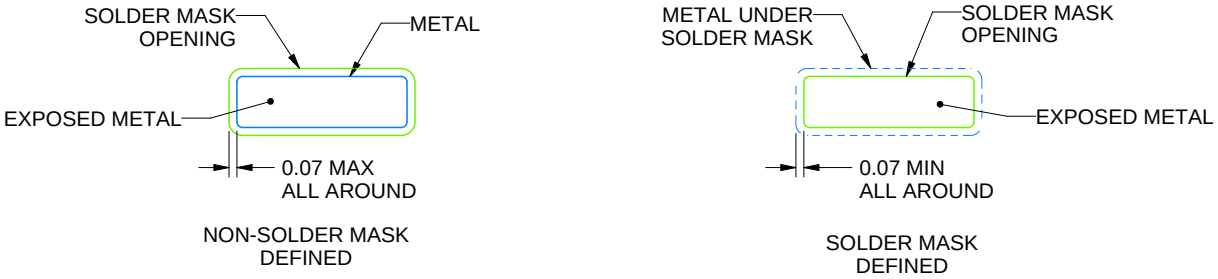
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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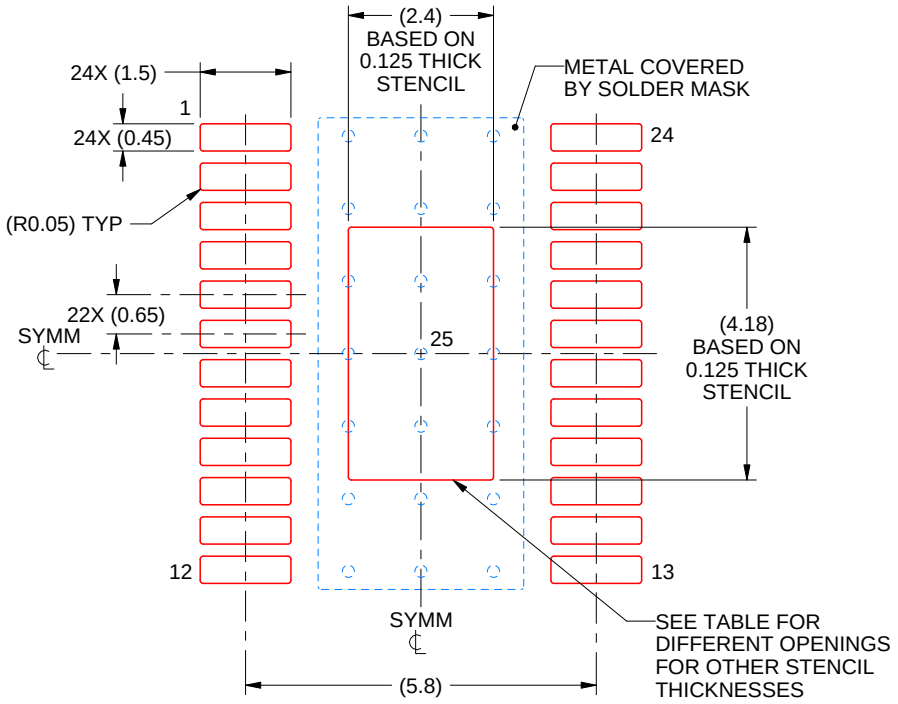
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 4.67
0.125	2.40 X 4.18 (SHOWN)
0.15	2.19 X 3.82
0.175	2.03 X 3.53

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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