TPA3138D2 10W、3.5V 至 14.4V、无电感器、立体声 D 类扬声器放大器

1 特性

- 宽电源电压范围 3.5V 至 14.4V
  - 6Ω、1% THD+N、12V 电源条件下，功率为 2 × 10W
  - 4Ω、10% THD+N、12V 电源条件下，功率为 1 x 18.5W
  - 1W、1kHz 输入、6Ω 条件下，THD+N 为 0.04%
- 电池寿命更长，适用于便携式 应用：
  - 1SPW 模式下，空闲电流为 20mA (12V)
  - >90% D 类效率
- 降低了解决方案尺寸和成本：
  - 无电感器运行
  - 不使用电感器时，符合 EN55013 和 EN55022 EMC 标准
  - 无需外部散热器
- 灵活的音频解决方案：
  - 单端或差动模拟输入
  - 可选增益：20dB 和 26dB
  - 启动时无喀哒声
- 综合保护和自动恢复：
  - 引脚对引脚、引脚对地、引脚对电源短路保护
  - 热保护、欠压保护和过压保护
  - 功率限制器和直流扬声器保护
- 与 TPA3110D2、TPA3136D2 和 TPA3136AD2 引脚对引脚兼容

2 应用

- 电视和监控器
- Bluetooth®扬声器和无线扬声器
- 智能设备中的音频放大器
- 物联网中的音频扬声器
- 消费类音频设备

3 说明

TPA3138D2 是一款每通道功率为 10W 的高效率、低空闲电流 D 类立体声音频放大器。它可驱动负载低至 3.2Ω 的立体声扬声器。在 1SPW 模式下，它仅消耗 21mA (12V) 的低空闲电流，且可在低至 3.5V 条件下运行，从而可实现更长的音频播放时间并改善蓝牙扬声器、电池供电设备和其他功率敏感性应用中的 热性能范围内实现精确性能。

利用扩频控制实现先进的 EMI 抑制功能，允许在满足 EMC 降低系统成本要求的同时，使用价格低廉的铁氧体磁珠滤波器。

为了进一步简化设计，TPA3138D2 集成了重要的保护特性， 包括欠压、过压、功率限制、短路、过热以及直流扬声器保护。所有这些保护都可以自动恢复。

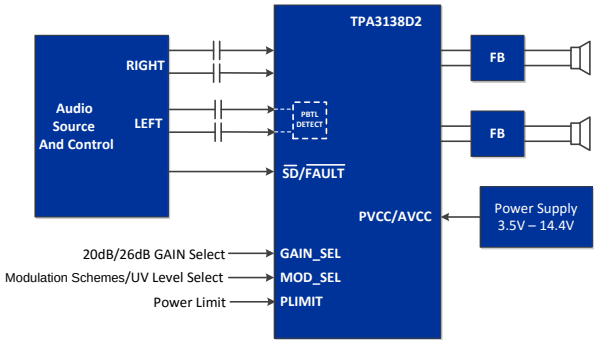
客户可以利用现有设计中的每个 TPA3138D2 特性，因为它与 TI 的 TPA3110D2、TPA3136D2 和 TPA3136AD2 完全引脚对引脚兼容。

器件信息(1)

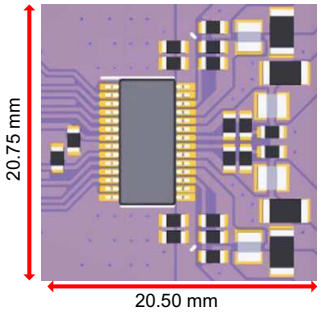
器件型号	封装	封装尺寸（标称值）
TPA3138D2	HTSSOP (28)	9.70mm × 4.40mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图



采用铁氧体磁珠的 **TPA3138** 布局



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (March 2018) to Revision A	**Page**
• 更改了器件状态：将“*预告信息*”更改成了“*生产数据*”	1

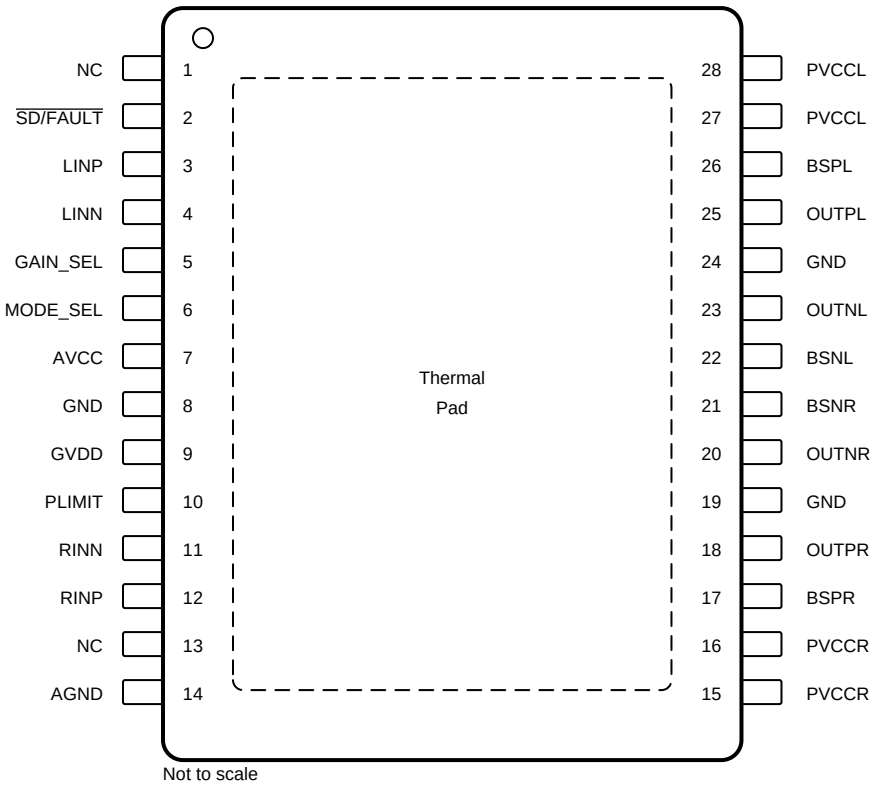
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5 Device Comparison Table

Product	Supply Voltage	Modulation Scheme	Package	Rdson	Gain	Inductor Free
TPA3138D2	3.5-V to 14.4-V	BD, 1SPW	HTSSOP-28	180-mΩ	20-dB, 26-dB	YES
TPA3110D2	8-V to 26-V	BD	HTSSOP-28	240-mΩ	20-dB, 26-dB, 32-dB, 36-dB	NO
TPA3136D2	4.5-V to 14.4-V	BD	HTSSOP-28	240-mΩ	26-dB	YES
TPA3136AD2	8-V to 14.4-V	BD	HTSSOP-28	240-mΩ	26-dB	YES

6 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP
(Top View)



Not to scale

Pin Functions

PIN		I/O/P(1)	DESCRIPTION
NAME	NO.		
NC	1	–	No Connect Pin. Can be shorted to PVCC or shorted to GND or left open.
SD/FAULT	2	IO	TTL logic levels with compliance to AVCC. Shutdown logic input for audio amp (LOW , outputs Hi-Z; HIGH , outputs enabled). General fault reporting including Over-Temp, Over-Current, DC Detect. SD/FAULT= High, normal operation, SD/FAULT= Low, fault condition Device will auto-recover once the OT/OC/DC Fault has been removed.
LINP	3	I	Positive audio input for left channel. Biased at 2.5 V. Connect to GND for PBTL mode.
LINN	4	I	Negative audio input for left channel. Biased at 2.5 V. Connect to GND for PBTL mode.
GAIN_SEL	5	I	Gain select least significant bit. TTL logic levels with compliance to AVDD. Low = 20 dB Gain, High = 26 dB Gain, Floating = 26 dB Gain.

(1) I = Input, O = Output, IO = Input and Output, P = Power

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Pin Functions (continued)

PIN		I/O/P[1]	DESCRIPTION
NAME	NO.		
MODE_SEL	6	I	Mode select least significant bit. TTL logic levels with compliance to AVDD. Low = BD Mode/UV Threshold = 7.5 V, High = Low-Idle-Current 1SPW Mode/UV Threshold = 3.4V, Floating = Low-Idle-Current 1SPW Mode/UV threshold = 3.4V
AVCC	7	P	Analog supply.
GND	8	–	Analog signal ground.
GVDD	9	O	FET gate drive supply. Nominal voltage is 5 V.
PLIMIT	10	I	Power limiter level control. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
RINN	11	I	Negative audio input for right channel. Biased at 2.5 V.
RINP	12	I	Positive audio input for right channel. Biased at 2.5 V.
NC	13	–	No Connect Pin. Can be shorted to PVCC or shorted to GND or left open.
AGND	14	–	Analog signal ground. Connect to the thermal pad.
PVCCR	15, 16	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connected internally.
BSPR	17	P	Bootstrap supply (BST) for right channel, positive high-side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
GND	19	–	Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	P	Bootstrap supply (BST) for right channel, negative high-side FET.
BSNL	22	P	Bootstrap supply (BST) for left channel, negative high-side FET.
OUTNL	23	O	Class-D H-bridge negative output for left channel.
GND	24	–	Power ground for the H-bridges.
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	P	Bootstrap supply (BST) for left channel, positive high-side FET.
PVCCL	27, 28	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connected internally.
Thermal Pad		–	Connect to GND for best thermal and electrical performance

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVCC to GND, PVCC to GND	–0.3	20	V
Input current	To any pin except supply pins		10	mA
Interface pin voltage	$\overline{SD}$/$\overline{FAULT}$ to GND(2), GAIN_SEL, MODE_SEL	–0.3	AVCC + 0.3	V
			10	V/ms
	PLIMIT	-0.3	GVDD + 0.3	V
	RINN, RINP, LINN, LINP	–0.3	5.5	V
Minimum load resistance, R_L	BTL, (10 V < PVCC < 14.4 V)	4.8		Ω
	BTL, (3.5 V < PVCC < 10 V)	3.2		
	PBTL, (10 V < PVCC < 14.4 V)	2.4		
	PBTL, (3.5 V < PVCC < 10 V)	1.6		
Continuous total power dissipation		See the Thermal Information Table		
Operating Juncation Temperature range		–25	150	°C
Storage temperature range, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage slew rate of these pins must be restricted to no more than 10 V/ms. For higher slew rates, use a 100 kΩ resister in series with the pins.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	3.5	14.4	V
V_{IH}	High-level input voltage	$\overline{SD}$/$\overline{FAULT}$ (1), GAIN_SEL, MODE_SEL	2	AVCC	V
V_{IL}	Low-level input voltage	$\overline{SD}$/$\overline{FAULT}$, GAIN_SEL, MODE_SEL (2)		0.8	V
V_{OL}	Low-level output voltage	$\overline{SD}$/$\overline{FAULT}$, $R_{PULL-UP}$ =100 kΩ, PVCC = 14.4 V		0.8	V
I_{IH}	High-level input current	$\overline{SD}$/$\overline{FAULT}$, GAIN_SEL, MODE_SEL, V_I = 2 V, AVCC = 12 V		50	μA
I_{IL}	Low-level input current	$\overline{SD}$/$\overline{FAULT}$, GAIN_SEL, MODE_SEL, V_I = 0.8 V, AVCC = 12 V		5	μA
T_A	Operating free-air temperature (3)		–10	85	°C
T_J	Operating junction temperature (3)		-10	150	°C

(1) Set $\overline{SD}$/$\overline{FAULT}$ to high level, make sure the pull-up resistor is larger than 4.7 kΩ and smaller than 500 kΩ
(2) Set GAIN_SEL and MODE_SEL to low level, make sure pull down resistor<10kΩ
(3) The TPA3138D2 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Briefs SLMA002 for more information about using the TSSOP thermal pad.

7.4 Thermal Information

THERMAL METRIC (1)		TPA3138D2 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

T_A = 25°C, AVCC = PVCC = 12 V, RL = 6 Ω. Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC CHARACTERISTICS							
PSRR	Power supply ripple rejection	200-mV_{PP} ripple at 1 kHz, Gain = 26 dB, Inputs ac-coupled to GND			–70		dB
P_O	Continuous output power, BTL	THD+N = 1%, f = 1 kHz, PV_{CC} = 12 V, R_L = 6 Ω			10		W
P_O	Continuous output power, BTL	THD+N = 10%, f = 1 kHz, PV_{CC} = 12 V, R_L = 6 Ω			12		W
P_O	Continuous output power, BTL	THD+N = 1%, f = 1 kHz, PV_{CC} = 12 V, R_L = 8 Ω			8		W
P_O	Continuous output power, BTL	THD+N = 10%, f = 1 kHz, PV_{CC} = 12 V, R_L = 8 Ω			9.9		W
P_O	Continuous output power, PBTL (mono)	THD+N = 10%, f = 1 kHz, PV_{CC} = 12 V, R_L = 4 Ω			18.5		W
I_O	Maximum output current	f = 1 kHz, R_L = 3 Ω			3.5		A
THD+N	Total harmonic distortion + noise	f = 1 kHz, P_O = 5 W (half-power)			0.04		%
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 26 dB			85		µV
					–81		dBV
		20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB			72		µV
					-82.6		dBV
	Crosstalk	V_O = 1 Vrms, Gain = 26 dB, f = 1 kHz			-95		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 26 dB, A-weighted			102		dB
OTE	Thermal trip point				150		°C
	Thermal hysteresis				15		°C
DC CHARACTERISTICS							
$\lvert V_{OS} \rvert$	Output offset voltage (measured differentially)	V_I = 0 V, Gain = 26 dB			1.5		mV
I_{CC}	Quiescent supply current	$\overline{SD}/\overline{FAULT}$ = 2 V, 10 µF + 680 nF output filter, 1SPW Mode, PV_{CC} = 12 V			20		mA
I_{CC}	Quiescent supply current	$\overline{SD}/\overline{FAULT}$ = 2 V, 10 µF + 680 nF output filter, BD Mode, PV_{CC} = 12 V			37		mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}/\overline{FAULT}$ = 0.8 V, no load			10		µA
$r_{DS(on)}$	Drain-source on-state resistance	I_O = 500 mA, T_J = 25°C excluding metal and bond wire resistance	High Side		180		mΩ
			Low side		180		
G	Gain	GAIN_SEL= 0.8 V		19	20	21	dB
G	Gain	GAIN_SEL= 2 V		25	26	27	dB
t_{ON}	Turn-on time	$\overline{SD}/\overline{FAULT}$ = 2 V			50		ms
t_{OFF}	Turn-off time	$\overline{SD}/\overline{FAULT}$ = 0.8 V			2.9		µs
GVDD	Gate drive supply	I_{GVDD} = 2 mA		4.8	5	5.2	V
t_{DCDET}	DC detect time	V_{RINP} = 2.6 V and V_{RINN} = 2.4 V, or V_{RINP} = 2.4 V and V_{RINN} = 2.6 V			800		ms
OVP	Over Voltage Protection				15.8		V
UVP	Under Voltage Protection	MODE_SEL = 0.8 V (BD mode)			7.5		V
UVP	Under Voltage Protection	MODE_SEL = 2 V, or floating (1SPW mode)			3.4		V

7.6 Switching Characteristics

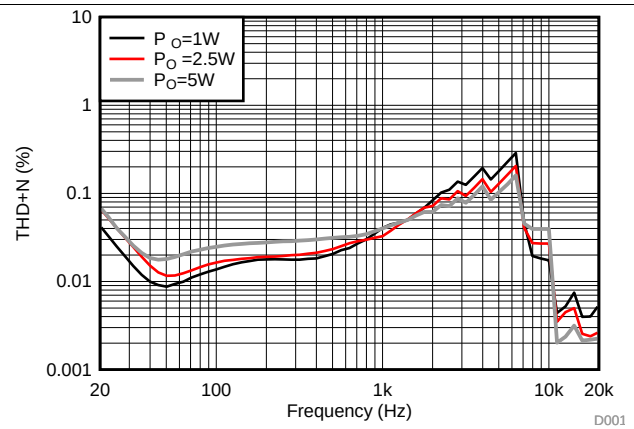
over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
$f_{OSC, SS}$	Oscillator frequency, Spread Spectrum ON	305		340	kHz

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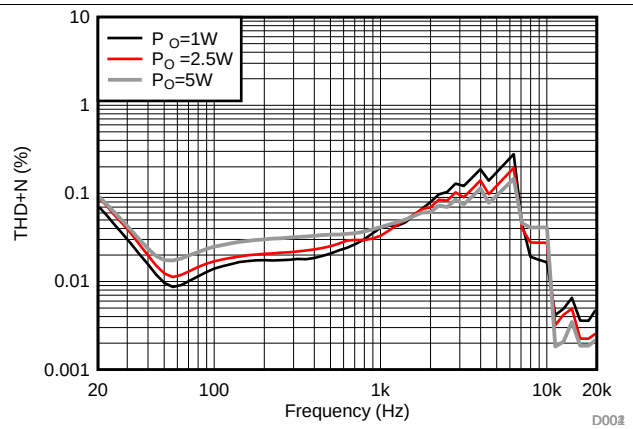
7.7 Typical Characteristics

All measurements taken at audio frequency = 1 kHz, closed-loop gain = 26 dB, BD mode, T_A = 25°C, AES17 filter using the TPA3138D2EVM, unless otherwise noted.



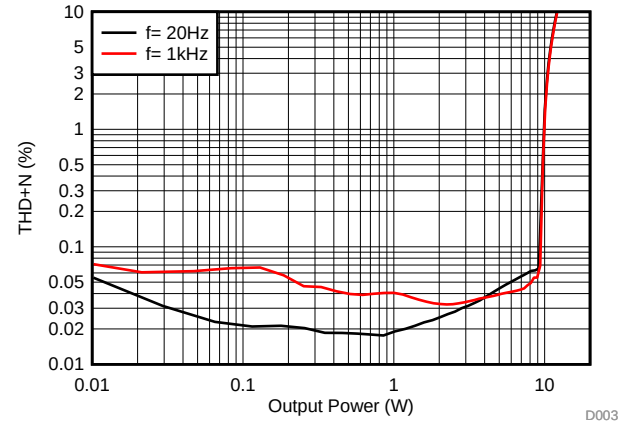
AVCC=PVCC = 12 V, Load = 6 Ω + 47 µH, 1 W, 2.5 W, 5 W

图 1. THD+N vs Frequency (BTL)



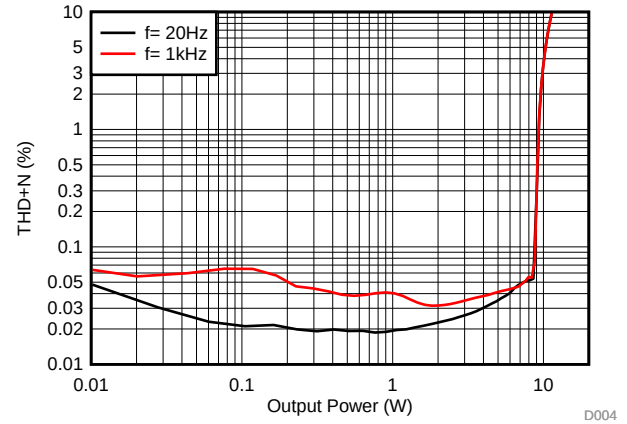
AVCC=PVCC = 13 V, Load = 8 Ω + 66 µH, 1 W, 2.5 W, 5 W

图 2. THD+N vs Frequency (BTL)



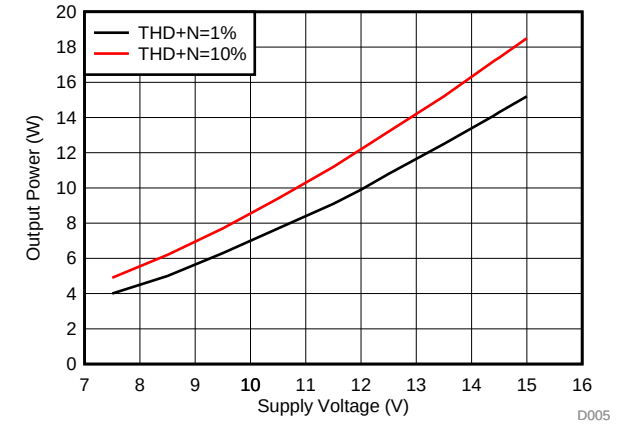
AVCC=PVCC = 12 V, Load = 6 Ω + 47 µH, 20 Hz, 1 kHz

图 3. THD+N vs Output Power (BTL)



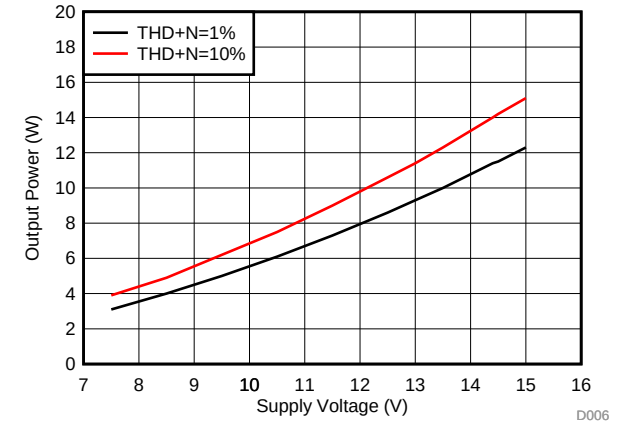
AVCC=PVCC = 13 V, Load = 8 Ω + 66 µH, 20 Hz, 1 kHz

图 4. THD+N + Noise vs Output Power (BTL)



AVCC=PVCC = 7.5 V to 15 V, Load = 6 Ω + 47 µH

图 5. Output Power vs Supply Voltage (BTL)



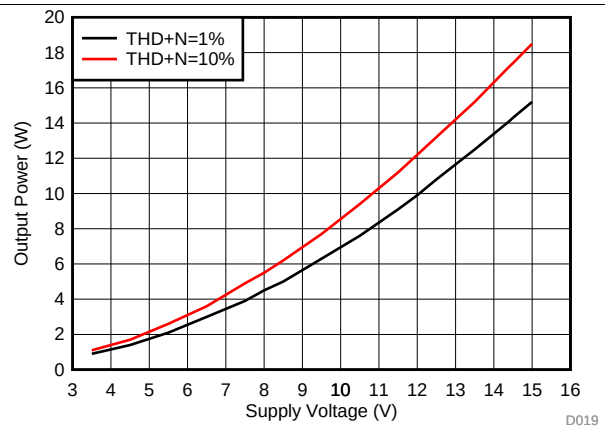
AVCC=PVCC = 7.5 V to 15 V, Load = 8 Ω + 66 µH

图 6. Output Power vs Supply Voltage (BTL)

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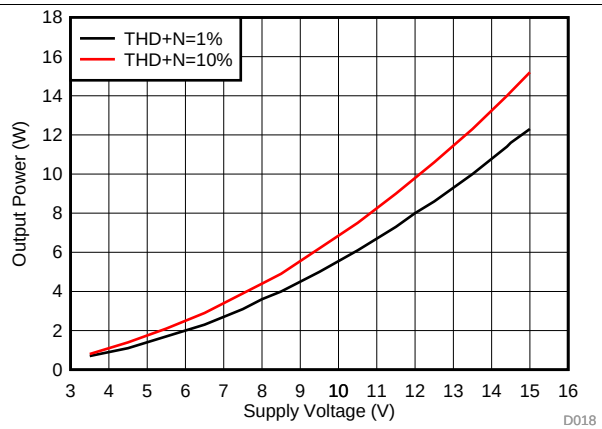
Typical Characteristics (接下页)

All measurements taken at audio frequency = 1 kHz, closed-loop gain = 26 dB, BD mode, T_A = 25°C, AES17 filter using the TPA3138D2EVM, unless otherwise noted.



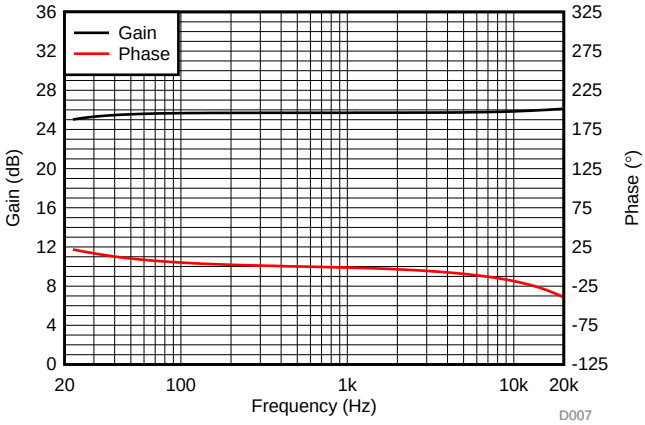
AVCC=PVCC = 3.5 V to 15 V, Load = 6 Ω + 47 µH, Low-Idle-Current 1SPW Mode

图 7. Output Power vs Supply Voltage (BTL)



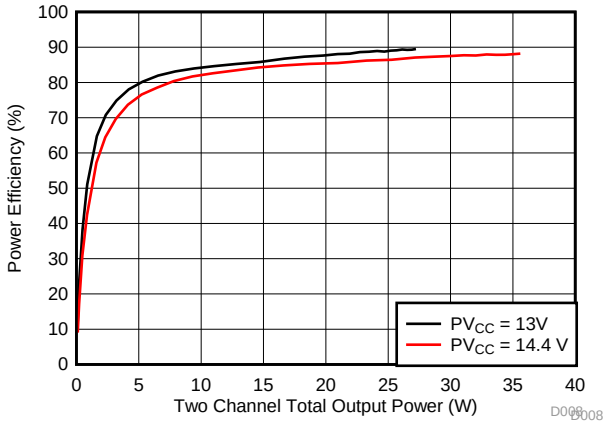
AVCC= PVCC = 3.5 V to 15 V, Load = 8 Ω + 66 µH, Low-Idle-Current 1SPW Mode

图 8. Output Power vs Supply Voltage (BTL)



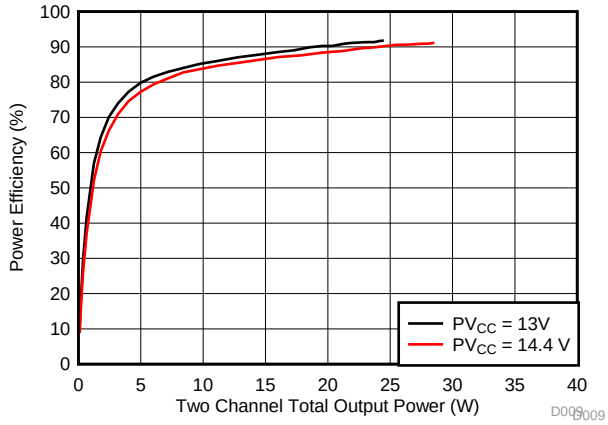
AVCC= PVCC = 12 V, Load = 6 Ω + 47 µH

图 9. Gain and Phase vs Frequency (BTL)



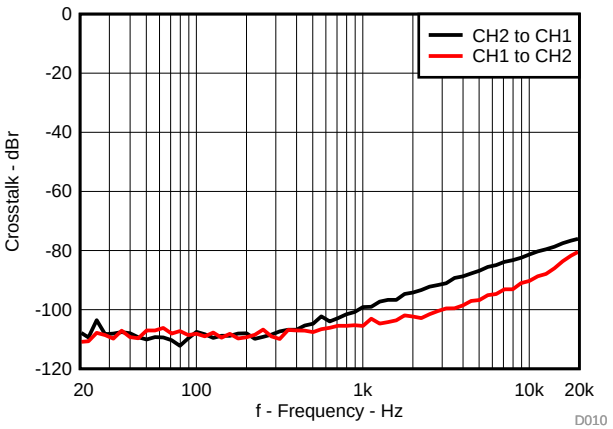
AVCC=PVCC = 12 V, 14.4 V, Load = 6 Ω + 47 µH

图 10. Efficiency vs Output Power (BTL)



AVCC=PVCC= 13 V, 14.4 V, Load = 8 Ω + 66 µH

图 11. Efficiency vs Output Power (BTL)

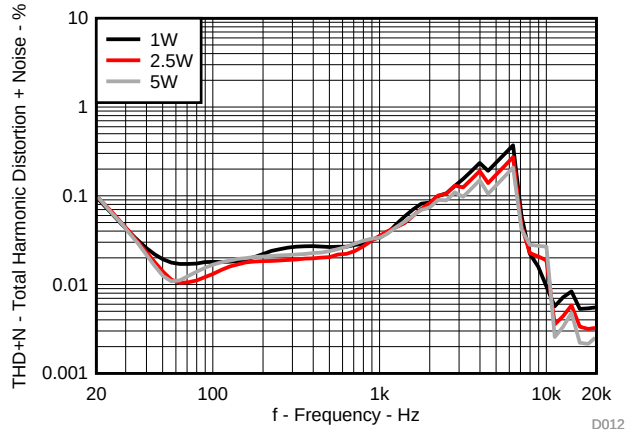


AVCC=PVCC = 12 V, 1 W, Load = 6 Ω + 47 µH

图 12. Crosstalk vs Frequency (BTL)

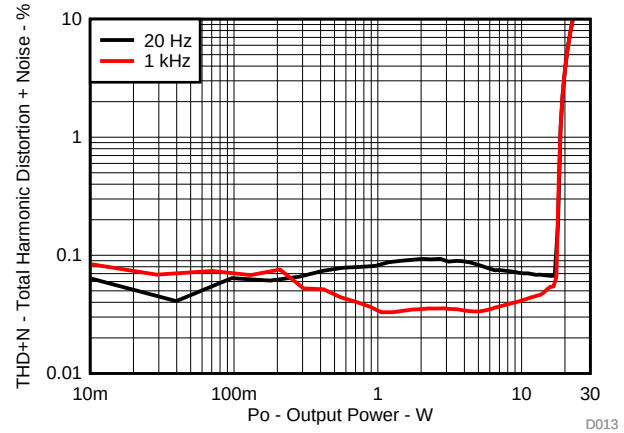
Typical Characteristics (接下页)

All measurements taken at audio frequency = 1 kHz, closed-loop gain = 26 dB, BD mode, T_A = 25°C, AES17 filter using the TPA3138D2EVM, unless otherwise noted.



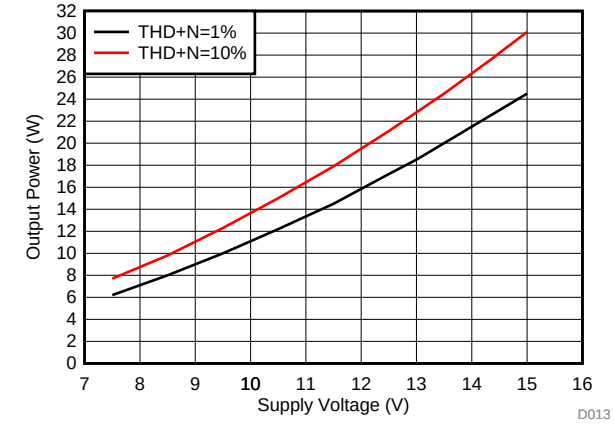
AVCC=PVCC = 13 V, Load = 4 Ω + 33 µH, 1 W, 2.5 W, 5 W

图 13. THD+N vs Frequency (PBTL)



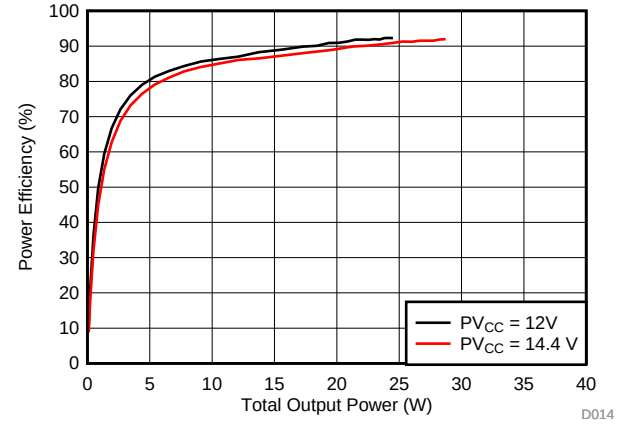
AVCC=PVCC = 13 V, Load = 4 Ω + 33 µH, 20 Hz, 1 kHz

图 14. THD+N vs Output Power (PBTL)



AVCC=PVCC = 7.5 V to 14.4 V, Load = 4 Ω + 33 µH

图 15. Output Power vs Supply Voltage (PBTL)



AVCC=PVCC = 13 V, 14.4 V, Load = 4 Ω + 33 µH

图 16. Efficiency vs Output Power (PBTL)

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Specifications* section.

Most audio analyzers does not give correct readings of Class-D amplifiers' performance due to their sensitivity to the out-of-band noise present at the amplifier outputs. An AES-17 pre-analyzer filter is recommended to use for Class-D amplifier measurements. In absence of such filters, a 30-kHz low-pass filter (10 Ω + 47 nF) can be used to reduce the out-of-band noise remaining on the amplifier outputs.

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9 Detailed Description

9.1 Overview

The TPA3138D2 is designed as a low-idle-power, cost-effective, general-purpose Class-D audio amplifier. The built-in spread spectrum control efficiently reduces EMI and enables the use of the ferrite beads instead of the inductors for ≤2x10W applications.

To facilitate system design, the TPA3138D2 needs only a single power supply between 3.5 V and 14.4 V for operation. An internal voltage regulator provides suitable voltage levels for the gate driver, digital, and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, as in the high-side gate drive, is accommodated by built-in bootstrap circuitry with integrated boot strap diodes requiring only an external capacitor for each half-bridge.

The audio signal path, including the gate drive and output stage, is designed as identical, independent full-bridges. All decoupling capacitors should be placed as close as possible to their associated pins. The physical loop with the power supply pins, decoupling capacitors, and GND return path to the device pins must be kept as short as possible, and with as little area as possible to minimize induction (see reference board documentation for additional information).

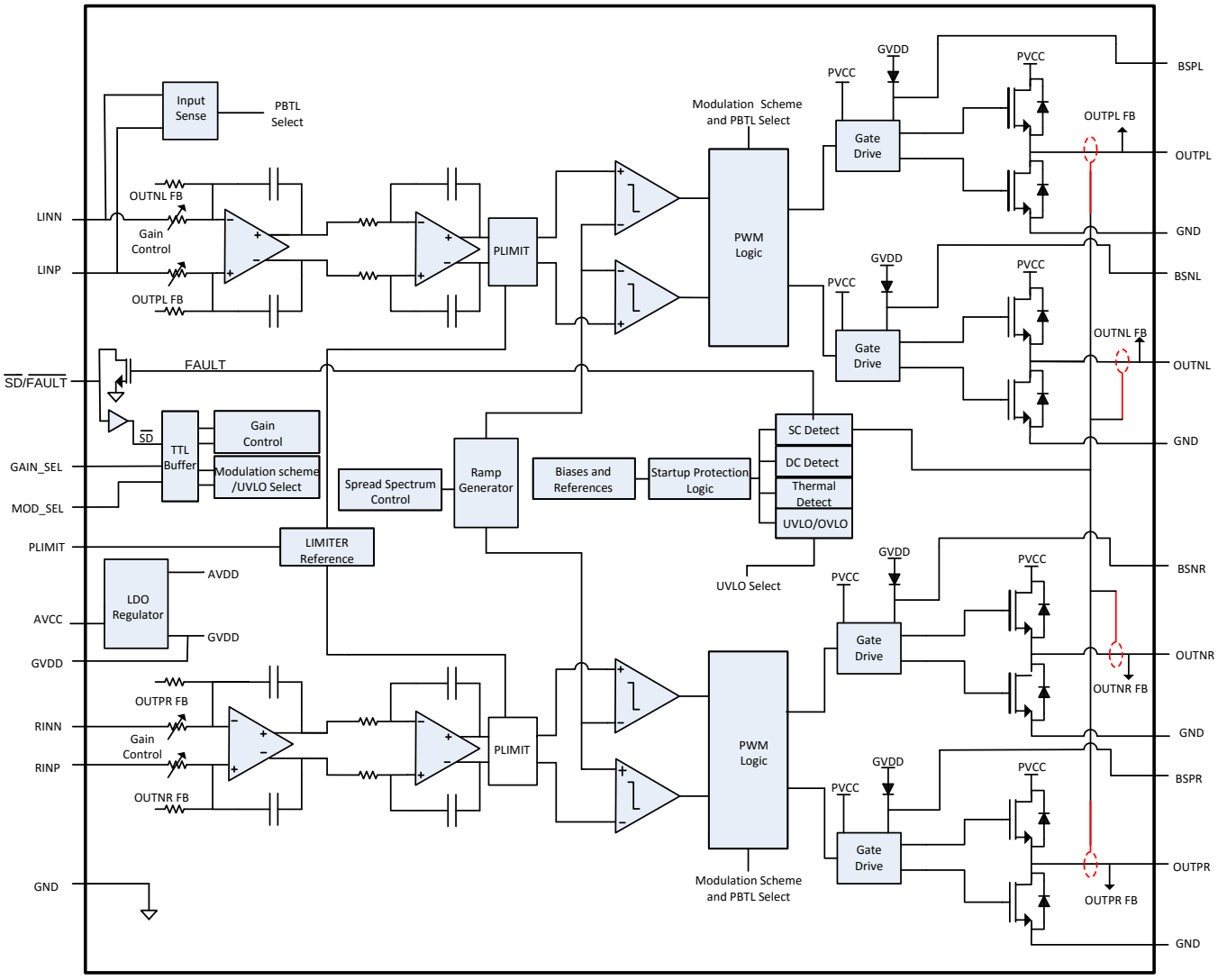
For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BSXX) to the power-stage output pin (OUTXX). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD) and the bootstrap pins. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the datasheet specified range, use ceramic capacitors with at least 220-nF capacitance, size 0603 or 0805, for the bootstrap supply. These capacitors ensure sufficient energy storage, even during clipped low frequency audio signals, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of its ON cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. For optimal electrical performance, EMI compliance, and system reliability, each PVCC pin should be decoupled with ceramic capacitors that are placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The PVCC power supply should have low output impedance and low noise. The power-supply ramp and $\overline{\text{SD}}$/FAULT release sequence is not critical for device reliability as facilitated by the internal power-on-reset circuit, but it is recommended to release $\overline{\text{SD}}$/FAULT after the power supply is settled for minimum turn on audible artifacts.

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9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Analog Gain

The analog gain of the TPA3138D2 can be changed by GAIN_SEL pin. Low Level, Gain = 20 dB; High Level, Gain = 26 dB.

9.3.2 $\overline{SD}$/$\overline{FAULT}$ Operation

The TPA3138D2 device employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{SD}$/$\overline{FAULT}$ input pin should be held high (see Specifications table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{SD}$/$\overline{FAULT}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{SD}$/$\overline{FAULT}$ unconnected, because the amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

9.3.3 PLIMIT

If selected, the PLIMIT operation limits the output voltage level to a voltage level below the supply rail. If the amplifier operates like it is powered by a lower supply voltage, then it limits the output power by voltage clipping. Add a resistor divider from GVDD to ground to set the threshold voltage at the PLIMIT pin.

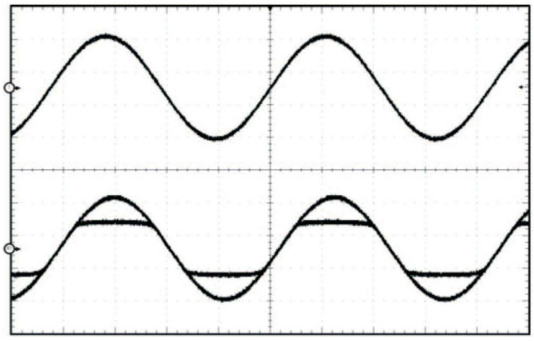


图 17. PLIMIT Circuit Operation

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to a fixed maximum value. The limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. The "virtual" rail is approximately 5.7 times (with BD mode) and 11.4 times (with 1SPW mode) the voltage at the PLIMIT pin. The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

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Feature Description (接下页)

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power}$$

where

- P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)
- R_L is the load resistance.
- R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
- V_P is the peak amplitude, which is limited by "virtual" voltage rail. (1)

9.3.4 Spread Spectrum and De-Phase Control

The TPA3138D2 device has built-in spread spectrum control of the oscillator frequency and de-phase of the PWM outputs to improve EMI performance. The spread spectrum scheme is internally fixed and is always turned on.

De-phase inverts the phase of the output PWM such that the idle output PWM waveforms of the two audio channels are inverted. De-phase does not affect the audio signal, or its polarity. De-phase only works with BD mode, it is auto-disabled in 1SPW mode

9.3.5 GVDD Supply

The GVDD Supply is used to power the gates of the output full-bridge transistors. Add a 1-μF capacitor to ground at this pin.

9.3.6 DC Detect

The TPA3138D2 device integrates a circuitry which protects the speakers from DC current that might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault is reported on the SD/FAULT pin as a low state. The DC Detect fault also causes the amplifier to shutdown by changing the state of the outputs to Hi-Z.

A DC Detect Fault is issued when the output DC voltage sustain for more than 800 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 1 Hz. To avoid nuisance faults due to the DC detect circuit, hold the SD/FAULT pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

9.3.7 PBTL Select

The TPA3138D2 device offers the feature of Parallel BTL operation with two outputs of each channel connected directly. Connecting LINP and LINN directly to Ground (without capacitors) sets the device in Mono Mode during power up. Connect the OUTPR and OUTNR together for the positive speaker terminal and OUTNL and OUTPL together for the negative speaker terminal. Analog input signal is applied to INPR and INNR. For an example of the PBTL connection, see the schematic in the *Typical Applications* section.

9.3.8 Short-Circuit Protection and Automatic Recovery Feature

The TPA3138D2 features over-current conditions against the output stage short-circuit conditions. The short-circuit protection fault is reported on the SD/FAULT pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is triggered .

The device recovers automatically once the over-current condition has been removed.

9.3.9 Over-Temperature Protection (OTP)

Thermal protection on the TPA3138D2 device prevents damage to the device when the internal die temperature exceeds 150°C. This triggering point has a ±15°C tolerance from device to device. Once the die temperature exceeds the thermal triggering point, the device is switched to the shutdown state and the outputs are disabled.

Thermal protection faults are reported on the SD/FAULT pin.

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Feature Description (接下页)

The device recovers automatically once the over temperature condition has been removed.

9.3.10 Over-Voltage Protection (OVP)

The TPA3138D2 device monitors the voltage on PVCC voltage threshold. When the voltage on PVCCL pin and PVCCR pin exceeds the over-voltage threshold (15.8 V typ), the OVP circuit puts the device into shutdown mode.

The device recovers automatically once the over-voltage condition has been removed.

9.3.11 Under-Voltage Protection (UVP)

When the voltage on PVCCL pin and PVCCR pin falls below the under-voltage threshold, the UVP circuit puts the device into shutdown mode. When MODE_SEL pin is set to LOW (BD mode), the under-voltage threshold is 7.5 V typical. When MODE_SEL pin is set to HIGH or floating, the TPA3138D2 operates in 1SPW mode, and the under-voltage threshold is 3.4 V typical.

The device recovers automatically once the under-voltage condition has been removed.

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9.4 Device Functional Modes

9.4.1 MODE_SEL = LOW: BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

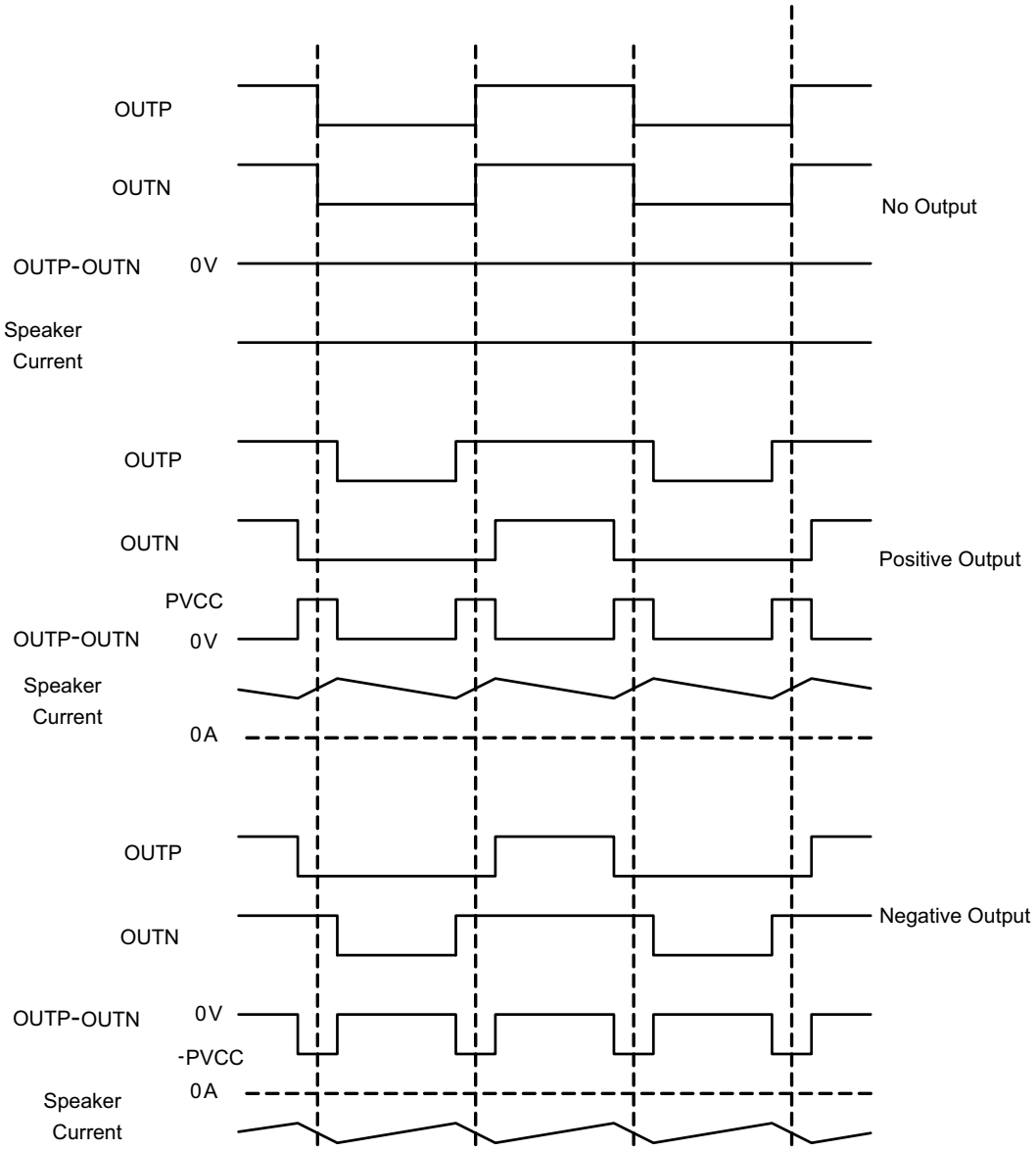


图 18. BD Mode Modulation

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Device Functional Modes (接下页)

9.4.2 MODE_SEL = HIGH: Low-Idle-Current 1SPW Modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In 1SPW mode the outputs operate at ~15% modulation during idle conditions. When an audio signal is applied one output decreases and the other output increases. The decreasing output signal rails to GND. At which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.

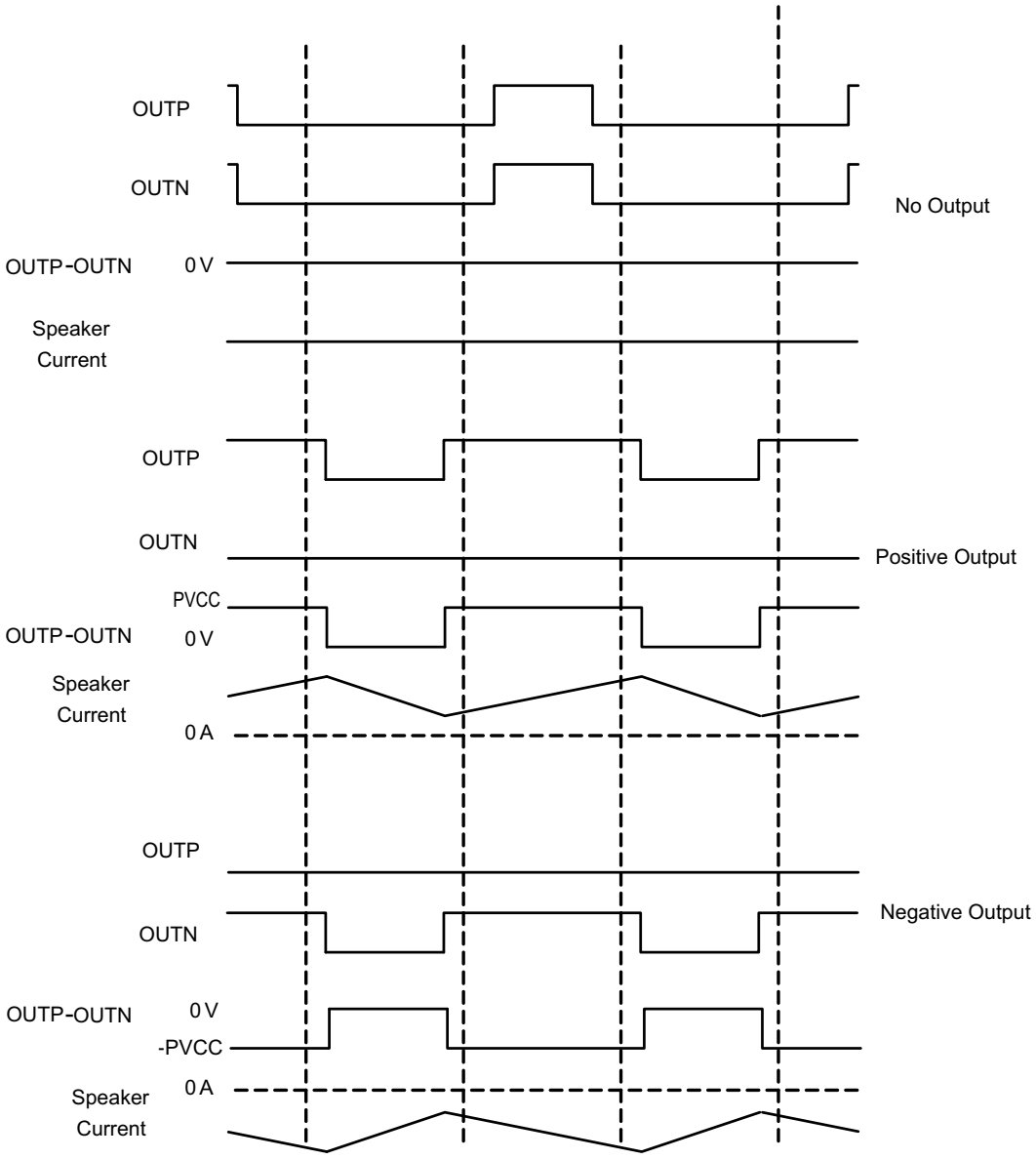


图 19. Low-Idle-Current 1SPW Modulation

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPA3138D2 device is designed for use in inductor-free applications with limited distance wire length between amplifier and speakers, suitable for applications such as TV sets, sound docks and Bluetooth speakers. The TPA3138D2 device can either be configured in stereo or mono mode. Depending on the output power requirements and necessity for (speaker) load protection, the built-in PLIMIT circuit can be used to control the system power, see functional description of these features.

10.2 Typical Applications

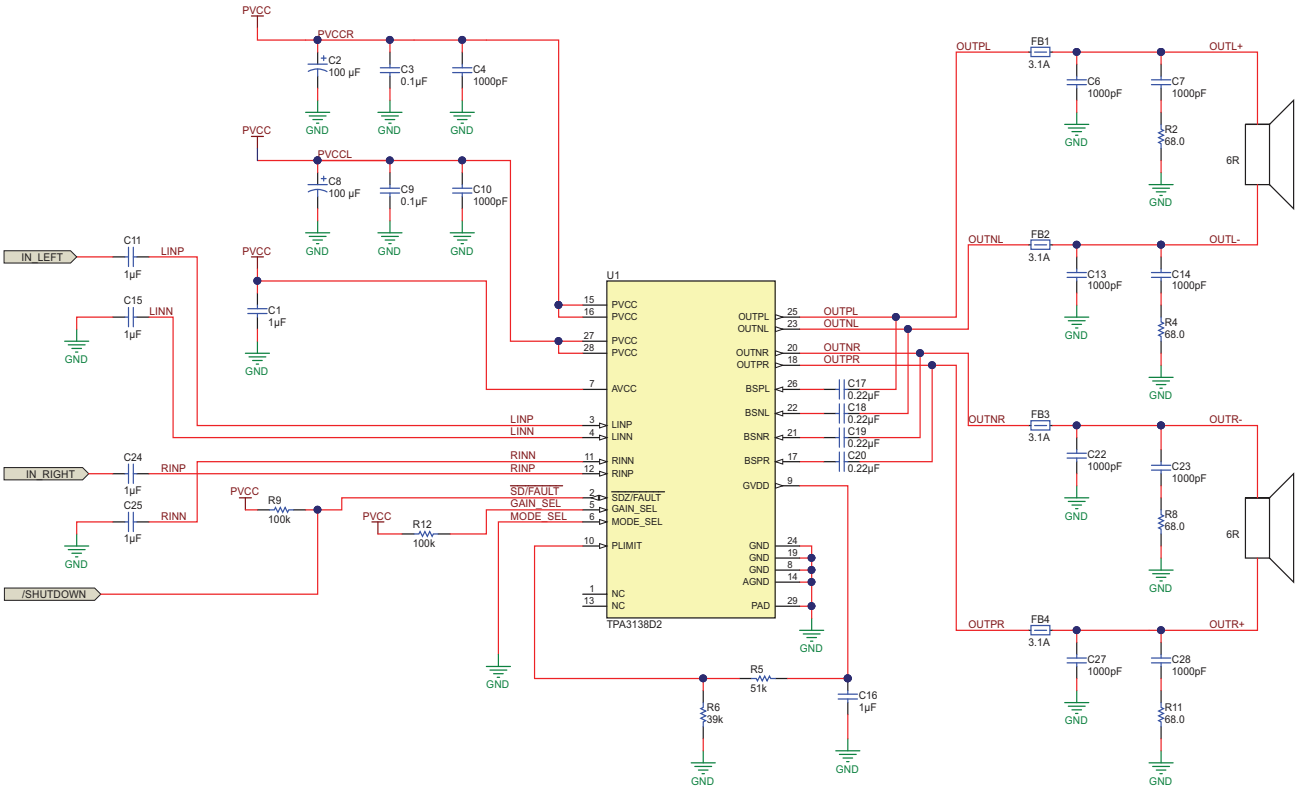


图 20. Stereo Class-D Amplifier in BTL Configuration with Single-Ended Inputs, Spread Spectrum Modulation and BD Mode

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Typical Applications (接下页)

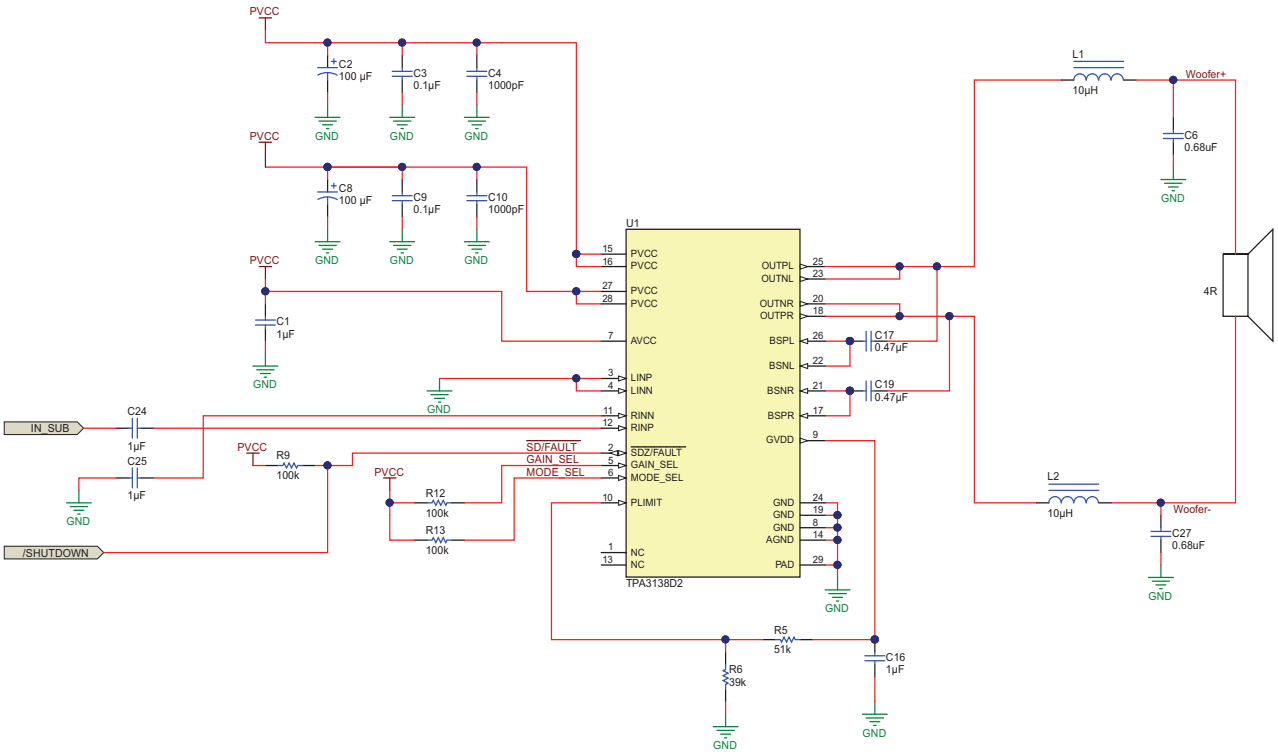


图 21. Stereo Class-D Amplifier in PBTL Configuration with Single-Ended Input, Spread Spectrum Modulation and 1SPW Mode

10.2.1 Design Requirements

10.2.1.1 PCB Material Recommendation

FR-4 Glass Epoxy material with 1 oz. (35 µm) is recommended for use with the TPA3138D2. The use of this material can provide higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance). It is recommended to use several GND underneath the device thermal pad for thermal coupling to a bottom-side copper GND plane for best thermal performance.

10.2.1.2 PVCC Capacitor Recommendation

The large capacitors used in conjunction with each full-bridge, are referred to as the PVCC capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, a capacitor with 100 µF and 16 V supports most applications with 12-V power supply. 25-V capacitor rating is recommended for power supply voltage higher than 12 V. For The PVCC capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

Typical Applications (接下页)

10.2.1.3 Decoupling Capacitor Recommendations

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the ceramic capacitors that are placed on the power supply to each full-bridge. They must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 16 V is required for use with a 12-V power supply.

10.2.2 Detailed Design Procedure

A rising-edge transition on $\overline{\text{SD}}$/$\overline{\text{FAULT}}$ input allows the device to start switching. It is recommended to ramp the PVCC voltage to its desired value before releasing $\overline{\text{SD}}$/$\overline{\text{FAULT}}$ for minimum audible artifacts.

The device is not inverting the audio signal from input to output.

The GVDD pin is not recommended to be used as a voltage source for external circuitry.

10.2.2.1 Ferrite Bead Filter Considerations

With Advanced Emissions Suppression Technology, the TPA3138D2 amplifier delivers high-efficiency Class-D performance while minimizing interference to surrounding circuits, even with a low-cost ferrite bead filter. But couple factors need to be taken into considerations when selecting the ferrite beads.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the Class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30-MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead and capacitor filter should be less than 10 MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. If it is possible, make sure the ferrite bead maintains an adequate amount of impedance at the peak current that the amplifier detects. If these specifications are not available, it is possible to estimate the bead's current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3138D2 device include NFZ2MSM series from Murata.

A high-quality ceramic capacitor is also required for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics works best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class-D outputs to ground. Suggested values for a simple RC series snubber network would be 68 Ω in series with a 100-pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the GND or the thermal pad beneath the chip.

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Typical Applications (接下页)

10.2.2.2 Efficiency: LC Filter Required with the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier requires an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 × V_{CC}, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is required to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3138D2 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{CC} instead of 2 × V_{CC}. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not required.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

10.2.2.3 When to Use an Output Filter for EMI Suppression

The TPA3138D2 device has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 100 cm and high power. The TPA3138D2 EVM passes FCC Class B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases a classic second order Butterworth filter similar to those shown in the figures below can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

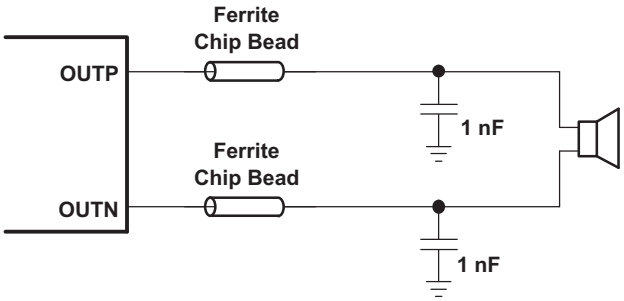


图 22. Typical Ferrite Chip Bead Filter (Chip Bead Example: NFZ2MSM series from Murata)

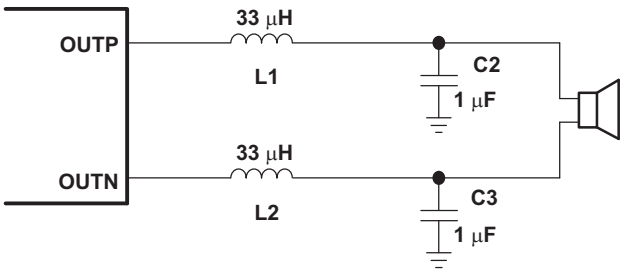


图 23. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 8 Ω

Typical Applications (接下页)

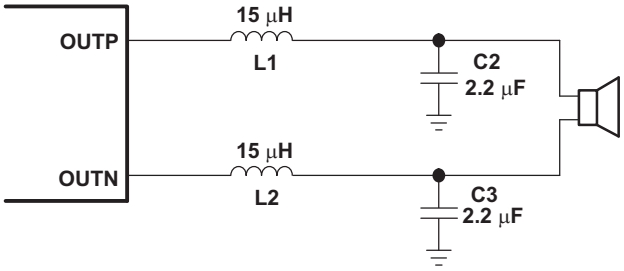
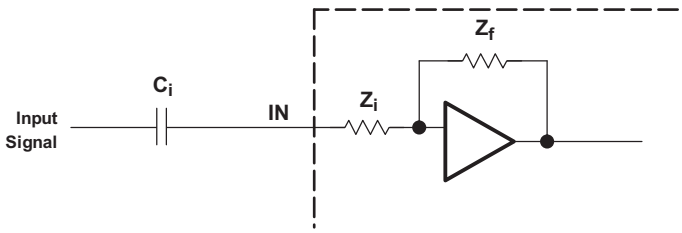


图 24. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 6 Ω

10.2.2.4 Input Resistance

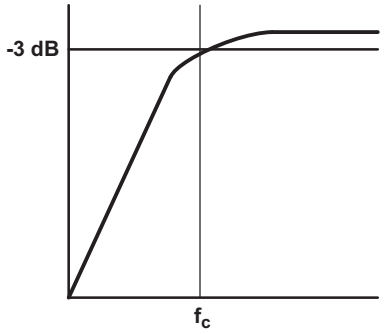
The typical input resistance of the amplifier is fixed to 20 kΩ ±15% for 26dB Gain and 40kΩ ±15% for 20dB Gain .



10.2.2.5 Input Capacitor, C_i

In the typical application, an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_i) form a high-pass filter with the corner frequency determined in 公式 2.

$$f_c = \frac{1}{2\pi Z_i C_i} \quad (2)$$



The value of C_i is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_i is 20 kΩ (26dB Gain) and the specification calls for a flat bass response down to 20 Hz. 公式 2 is reconfigured as 公式 3.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (3)$$

In this example, C_i is 0.4 µF; so, one would likely choose a value of 0.39 µF as this value is commonly used. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 3 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

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Typical Applications (接下页)

10.2.2.6 BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22-μF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22-μF capacitor must be connected from OUTPx to BSPx, and one 0.22-μF capacitor must be connected from OUTNx to BSNx. (See the application circuit diagram in 图 20.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

10.2.2.7 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3138D2 device with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3138D2 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 3 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 50-ms power-up time. If the input capacitors are not allowed to completely charge, there is some additional sensitivity to component matching which can result in pop if the input components are not well matched.

10.2.2.8 Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

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Typical Applications (接下页)

10.2.3 Application Performance Curves

10.2.3.1 EN55013 Radiated Emissions Results

TPA3138D2 EVM, PVCC = 12 V, 8-Ω speakers, P_O = 4 W

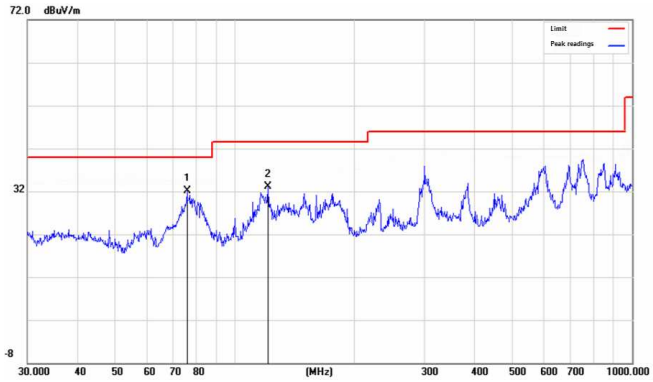


图 25. Radiated Emission - Horizontal

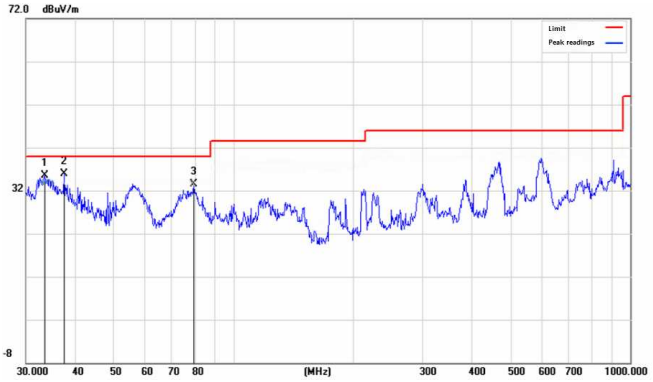


图 26. Radiated Emission - Vertical

10.2.3.2 EN55022 Conducted Emissions Results

TPA3138D2 EVM, PVCC = 12 V, 8-Ω speakers, P_O = 4 W

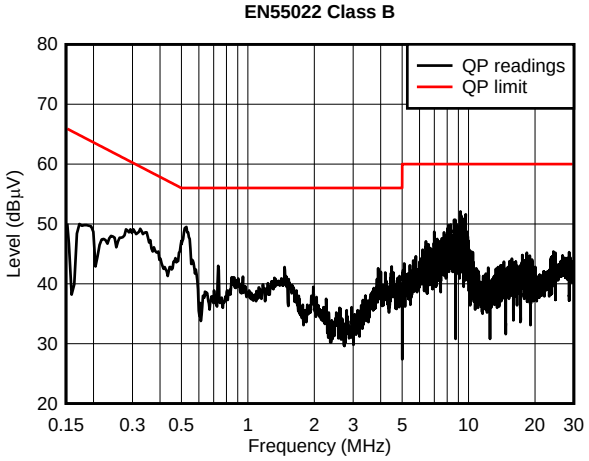


图 27. Conducted Emission - Line

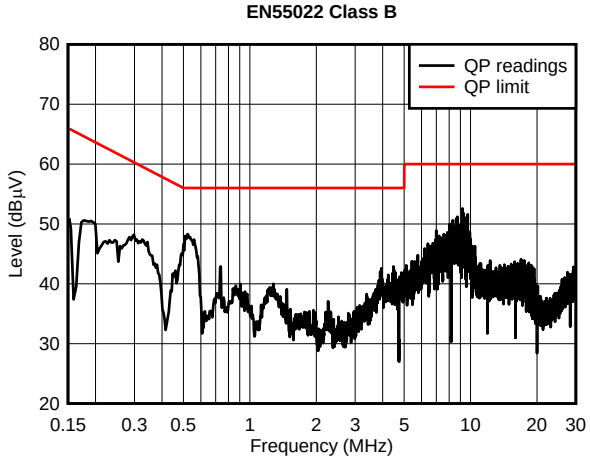


图 28. Conducted Emission - Neutral

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11 Power Supply Recommendations

11.1 Power Supply Decoupling, C_S

The TPA3138D2 device is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either GND pins or thermal pad) as possible. For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 μF to 1 μF placed as close as possible to the device PVCC leads works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 100 μF or greater placed near the audio power amplifier is recommended. The 100-μF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC pins provide the power to the output transistors, so a 100-μF or larger capacitor should be placed on each PVCC pin. A 1-μF capacitor on the AVCC pin is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency class-D noise from entering the linear input amplifiers.

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12 Layout

12.1 Layout Guidelines

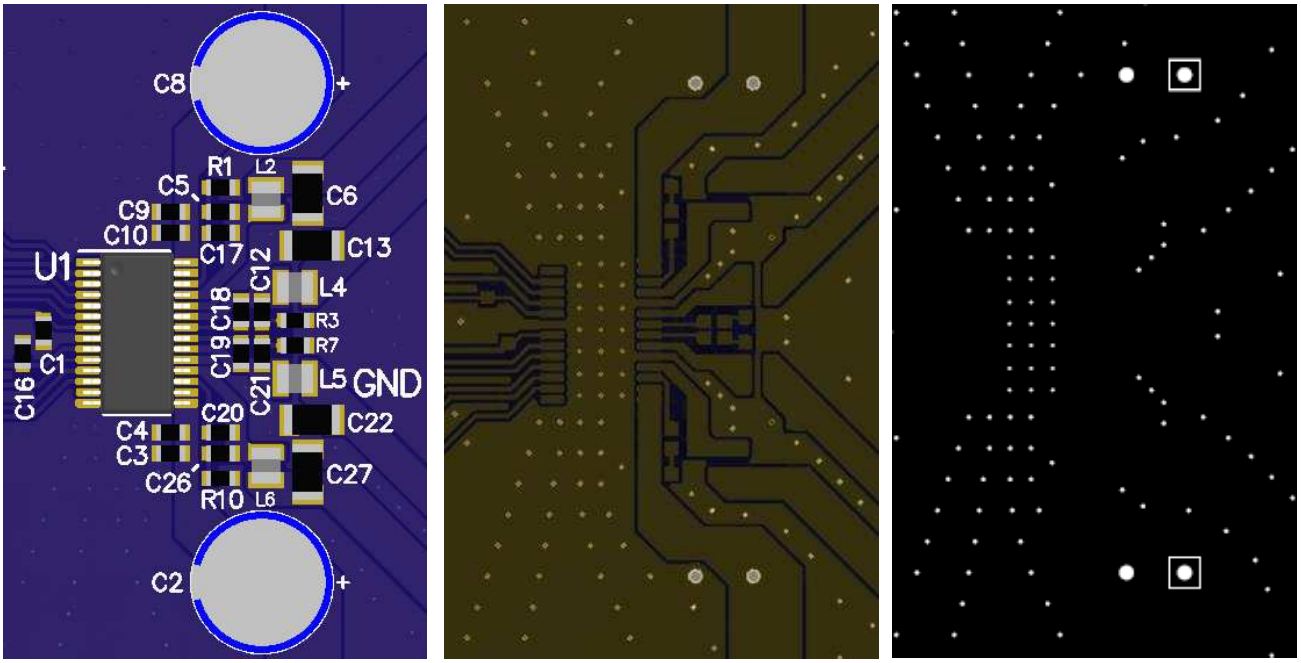
The TPA3138D2 device can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions help meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC pins as possible. Large (100-µF or greater) bulk power supply decoupling capacitors should be placed near the TPA3138D2 device on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1000 pF and a larger mid-frequency cap of value between 0.1 µF and 1 µF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—The AVCC (pin 7) decoupling capacitor should be connected to ground (GND). The PVCC decoupling capacitors should connect to GND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TPA3138D2.
- Output filter—The ferrite EMI filter (图 22) should be placed as close to the output pins as possible for the best EMI performance. The capacitors used in the ferrite should be grounded to power ground.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 3.04 mm × 2.34 mm. Seven rows of solid vias (three vias per row, 0.3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. See the TI Application Report SLMA002 for more information about using the TSSOP thermal pad. For recommended PCB footprints, see figures at the end of this data sheet.

For an example layout, see the TPA3138D2 Evaluation Module (TPA3138D2EVM) User Manual. Both the EVM user manual and the thermal pad application report are available on the TI Web site at http://www.ti.com.

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12.2 Layout Example



Top Layer 3D view　　Top Layer layout view　　Bot Layer layout view

图 29. BTL Layout Example

13 器件和文档支持

13.1 器件支持

13.1.1 第三方产品免责声明

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13.2 文档支持

13.2.1 相关文档

《PowerPAD™ 耐热增强型封装应用报告》（文献编号：SLMA002）

13.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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13.6 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA3138D2PWP	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3138D2
TPA3138D2PWP.A	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3138D2
TPA3138D2PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3138D2
TPA3138D2PWPR.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3138D2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

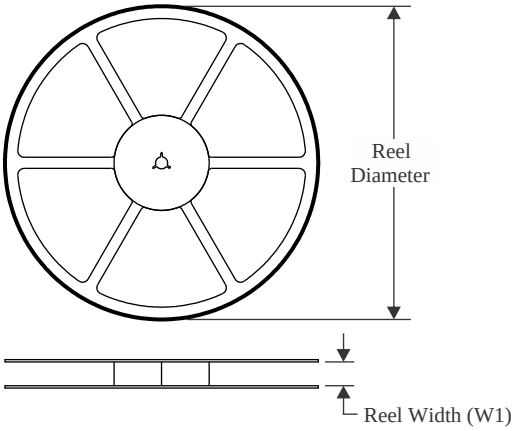
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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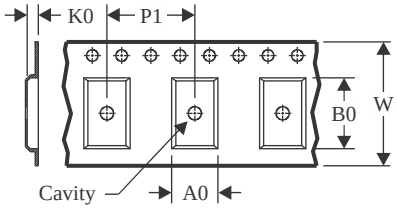
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

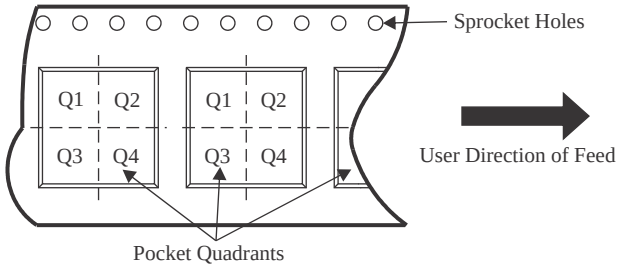


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

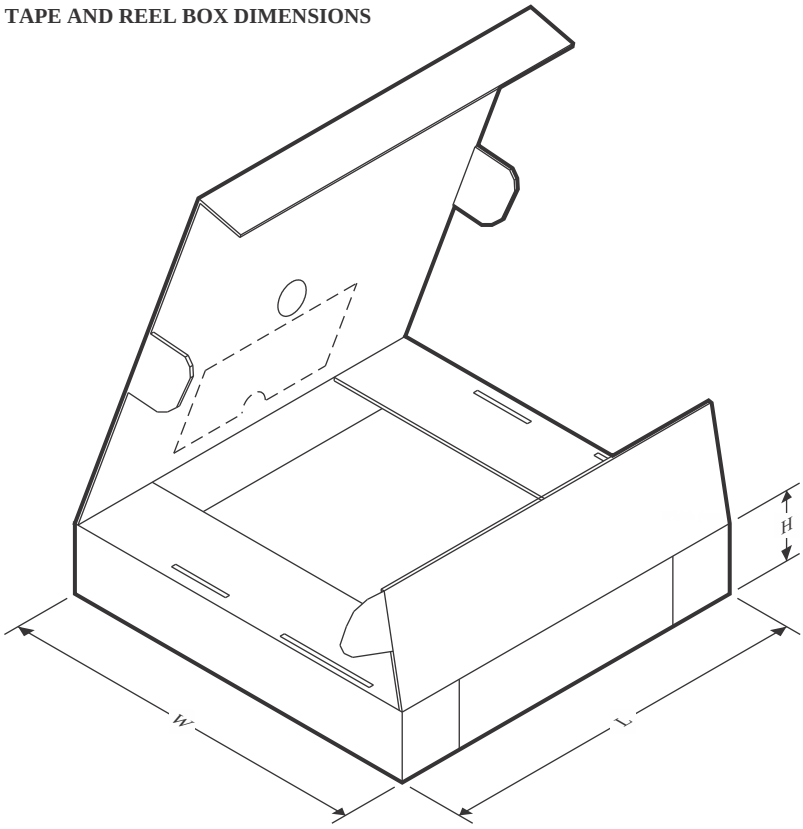
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3138D2PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

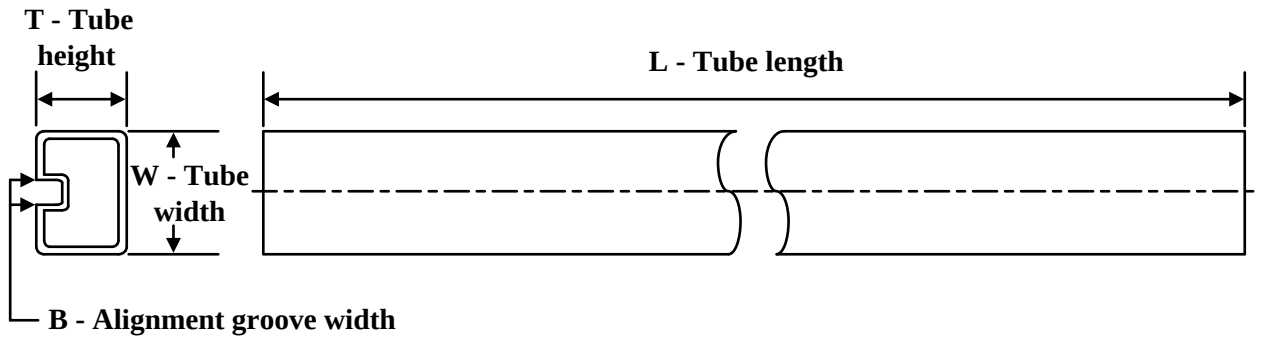
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3138D2PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA3138D2PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
TPA3138D2PWP.A	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

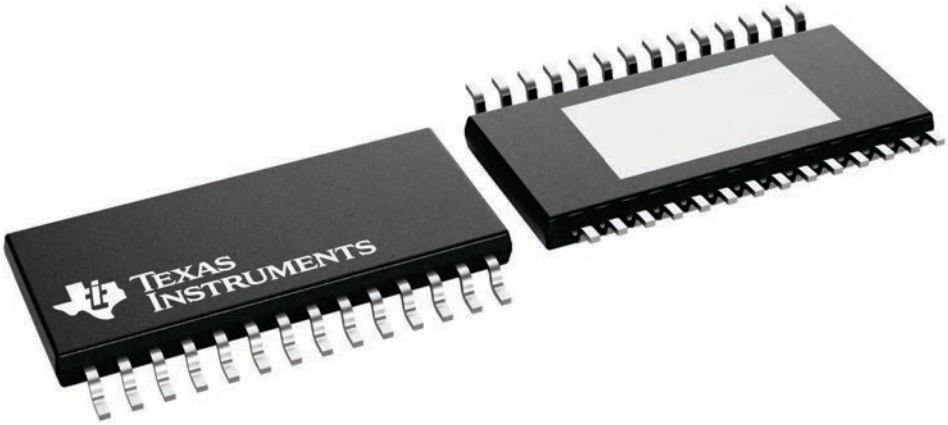
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

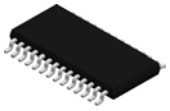
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

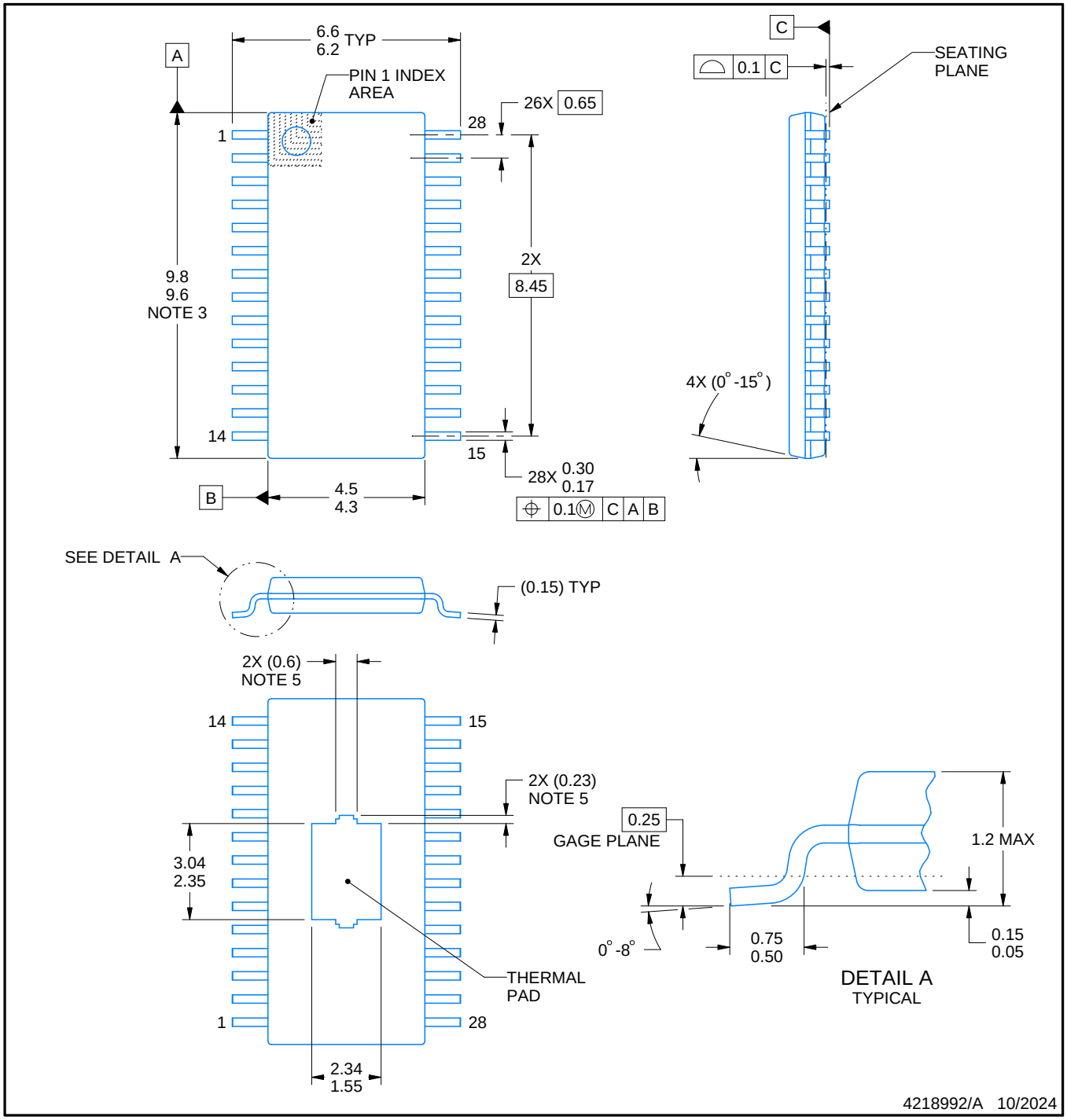
PACKAGE OUTLINE

PWP0028H



PowerPAD™ TSSOP - 1.2 mm max height

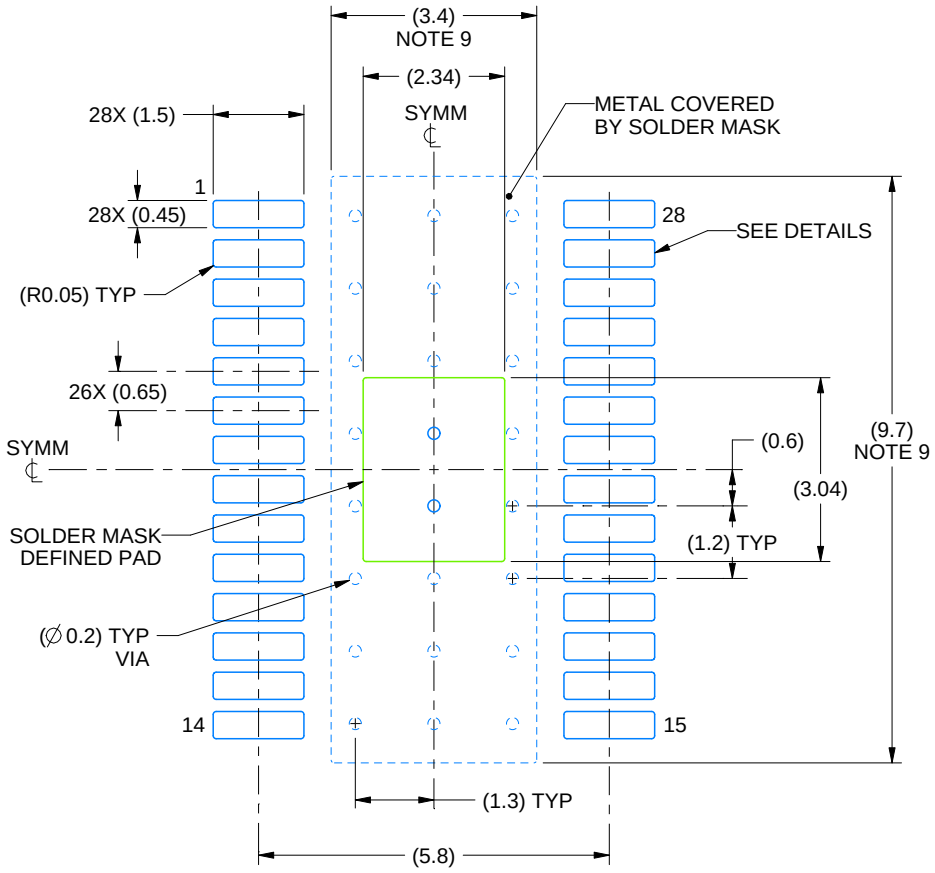
SMALL OUTLINE PACKAGE



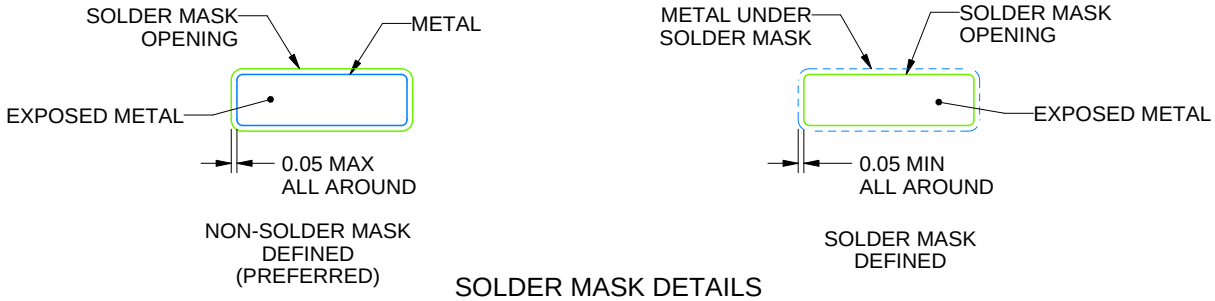
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

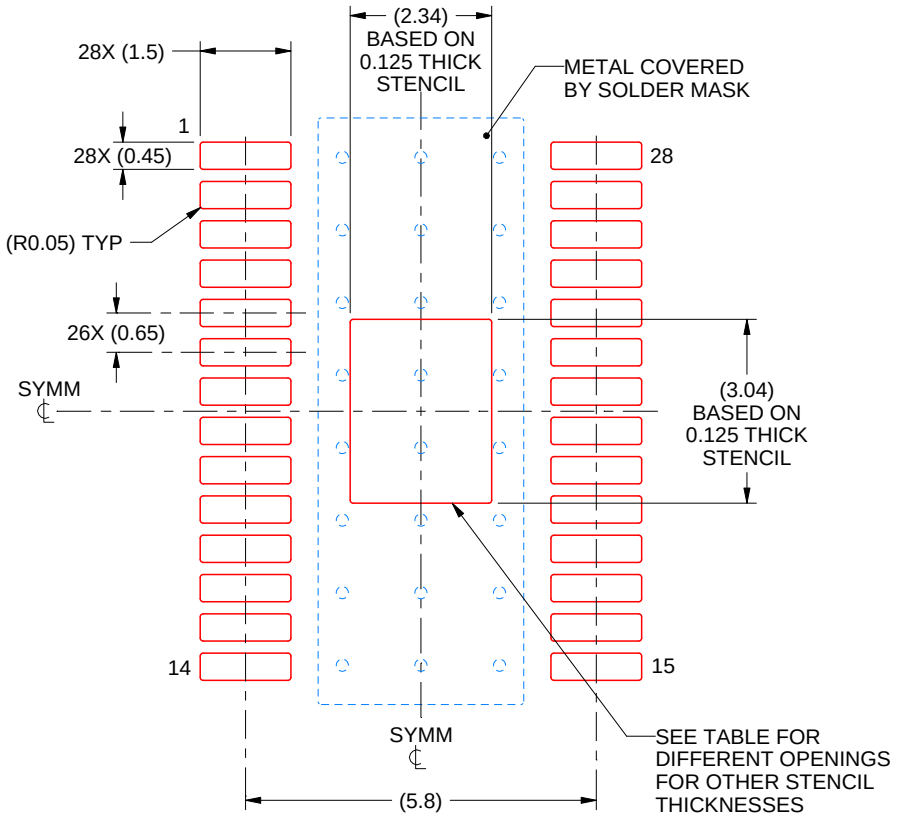


SOLDER MASK DETAILS

4218992/A 10/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 3.40
0.125	2.34 X 3.04 (SHOWN)
0.15	2.14 X 2.78
0.175	1.98 X 2.57

4218992/A 10/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月