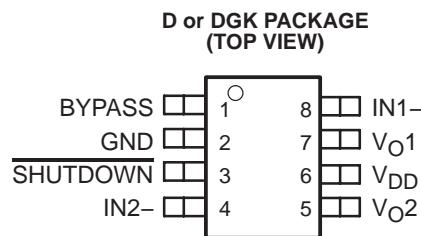


TPA6102A2
50-mW ULTRALOW-VOLTAGE, FIXED-GAIN STEREO HEADPHONE
AUDIO POWER AMPLIFIER
SLOS324B – JUNE 2000 – REVISED SEPTEMBER 2004

- 50-mW Stereo Output
- Low Supply Current . . . 0.75 mA
- Low Shutdown Current . . . 50 nA
- Minimal External Components Required
- Gain Set Internally to 14 dB
- Pop Reduction Circuitry
- Internal Mid-Rail Generation
- Thermal and Short-Circuit Protection
- Surface-Mount Packaging
 - MSOP
 - SOIC
- 1.6-V to 3.6-V Supply Voltage Range



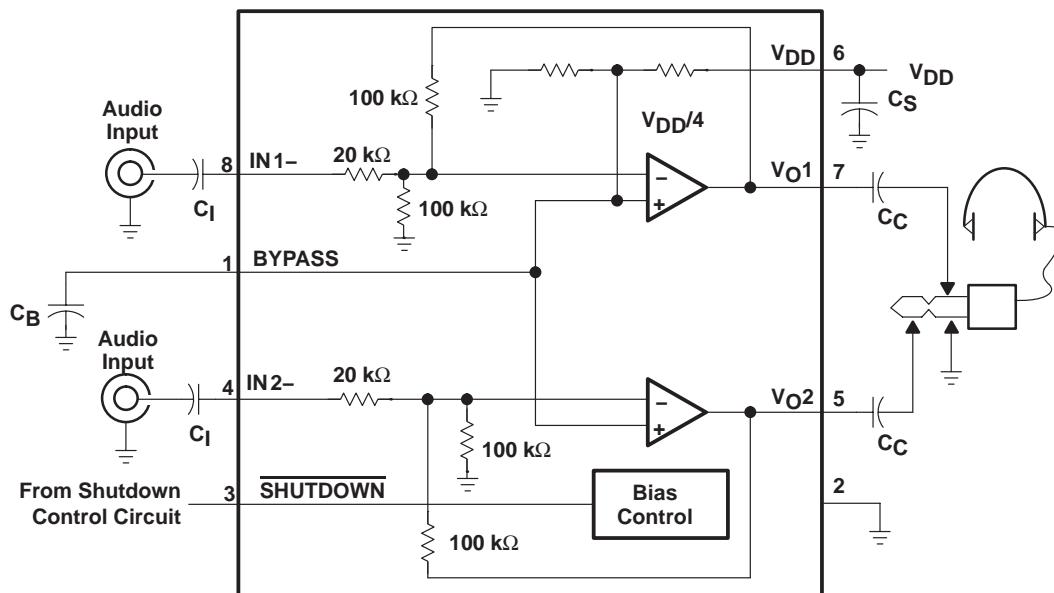
description

The TPA6102A2 is a stereo audio power amplifier packaged in either an 8-pin SOIC package or an 8-pin MOSP package capable of delivering 50 mW of continuous RMS power per channel into 16- Ω loads. Amplifier gain is internally set to 14 dB (inverting) to save board space by eliminating six external resistors.

The TPA6102A2 is optimized for battery applications because of its low-supply current, shutdown current, and THD+N. To obtain the low-supply voltage range, the TPA6102A2 biases BYPASS to $V_{DD}/4$.

When driving a 16- Ω load with 40-mW output power from 3.3 V, THD+N is 0.08% at 1 kHz, and less than 0.2% across the audio band of 20 Hz to 20 kHz. For 30 mW into 32- Ω loads, the THD+N is reduced to less than 0.06% at 1 kHz, and is less than 0.3% across the audio band of 20 Hz to 20 kHz.

typical application circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TPA6102A2**50-mW ULTRALOW-VOLTAGE, FIXED-GAIN STEREO HEADPHONE
AUDIO POWER AMPLIFIER**

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AVAILABLE OPTIONS

T _A	PACKAGED DEVICE		MSOP SYMBOLIZATION
	SMALL OUTLINE (D)	MSOP (DGK)	
–40°C to 85°C	TPA6102A2D	TPA6102A2DGK	AJN

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BYPASS	1	I	Tap to voltage divider for internal mid-supply bias supply. BYPASS is set at V _{DD} /4. Connect to a 0.1-µF to 1-µF low ESR capacitor for best performance.
GND	2	I	GND is the ground connection.
IN1–	8	I	IN1– is the inverting input for channel 1.
IN2–	4	I	IN2– is the inverting input for channel 2.
SHUTDOWN	3	I	Active-low input. When held low, the device is placed in a low supply current mode.
V _{DD}	6	I	V _{DD} is the supply voltage terminal.
V _O 1	7	O	V _O 1 is the audio output for channel 1.
V _O 2	5	O	V _O 2 is the audio output for channel 2.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V _{DD}	4 V
Input voltage, V _I	–0.3 V to V _{DD} + 0.3 V
Continuous total power dissipation	Internally Limited
Operating junction temperature range, T _J	–40°C to 150°C
Storage temperature range, T _{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
			454 mW	369 mW
D	710 mW	5.68 mW/°C		
DGK	469 mW	3.75 mW/°C	300 mW	244 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V _{DD}		1.6	3.6	V
High-level input voltage, V _{IH} (SHUTDOWN)		60% x V _{DD}		V
Low-level input voltage, V _{IL} (SHUTDOWN)			25% x V _{DD}	V
Operating free-air temperature, T _A		–40	85	°C

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**50-mW ULTRALOW-VOLTAGE, FIXED-GAIN STEREO HEADPHONE
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dc electrical characteristics at $T_A = 25^\circ\text{C}$, $V_{DD} = 3.6\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO} Output offset voltage	$A_V = 14\text{ dB}$	5	40		mV
PSRR Power supply rejection ratio	$V_{DD} = 3\text{ V}$ to 3.6 V	72			dB
I_{DD} Supply current	<u>SHUTDOWN</u> = 3.6 V	0.75	1.5		mA
$I_{DD(\text{SD})}$ Supply current in <u>SHUTDOWN</u> mode	<u>SHUTDOWN</u> = 0 V	50	250		nA
$ I_{IH} $ High-level input current (<u>SHUTDOWN</u>)	$V_{DD} = 3.6\text{ V}$, $V_I = V_{DD}$	1			μA
$ I_{IL} $ Low-level input current (<u>SHUTDOWN</u>)	$V_{DD} = 3.6\text{ V}$, $V_I = 0\text{ V}$	1			μA
Z_I Input impedance		20			$\text{k}\Omega$

ac operating characteristics, $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 16\text{ }\Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
G Gain		14			dB
P_O Output power (each channel)	$\text{THD} \leq 0.1\%$, $f = 1\text{ kHz}$	50			mW
THD+N Total harmonic distortion + noise	$P_O = 45\text{ mW}$, 20–20 kHz	0.4%			
B_{OM} Maximum output power BW	$\text{THD} < 0.5\%$	> 20			kHz
k_{SVR} Supply ripple rejection ratio	$f = 1\text{ kHz}$	47			dB
SNR Signal-to-noise ratio	$P_O = 50\text{ mW}$	86			dB
V_n Noise output voltage (no noise weighting filter)		45			$\mu\text{V(rms)}$

ac operating characteristics, $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 32\text{ }\Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
G Gain		14			dB
P_O Output power (each channel)	$\text{THD} \leq 0.1\%$, $f = 1\text{ kHz}$	35			mW
THD+N Total harmonic distortion + noise	$P_O = 30\text{ mW}$, 20–20 kHz	0.4%			
B_{OM} Maximum output power BW	$\text{THD} < 0.4\%$	>20			kHz
k_{SVR} Supply ripple rejection ratio	$f = 1\text{ kHz}$	47			dB
SNR Signal-to-noise ratio	$P_O = 30\text{ mW}$	86			dB
V_n Noise output voltage (no noise weighting filter)		50			$\mu\text{V(rms)}$

TPA6102A2**50-mW ULTRALOW-VOLTAGE, FIXED-GAIN STEREO HEADPHONE
AUDIO POWER AMPLIFIER**

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dc electrical characteristics at $T_A = 25^\circ\text{C}$, $V_{DD} = 1.6\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	$A_V = 14\text{ dB}$	5	40		mV
PSRR	$V_{DD} = 1.4\text{ V}$ to 1.8 V	80			dB
I_{DD}	<u>SHUTDOWN</u> = 1.6 V	0.65	1.2		mA
$I_{DD(\text{SD})}$	<u>SHUTDOWN</u> = 0 V	50	250		nA
$ I_{IH} $	$V_{DD} = 1.6\text{ V}$, $V_I = V_{DD}$	1			μA
$ I_{IL} $	$V_{DD} = 1.6\text{ V}$, $V_I = 0\text{ V}$	1			μA
Z_I		20			$\text{k}\Omega$

ac operating characteristics, $V_{DD} = 1.6\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 16\text{ }\Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
G		14			dB
P_O	THD $\leq 0.5\%$, $f = 1\text{ kHz}$	10			mW
THD+N	$P_O = 9.5\text{ mW}$, 20–20 kHz	0.06%			
BOM	THD $< 1\%$	> 20			kHz
k _{SVR}	$f = 1\text{ kHz}$	47			dB
SNR	$P_O = 10\text{ mW}$	82			dB
V_n		32			$\mu\text{V(rms)}$

ac operating characteristics, $V_{DD} = 1.6\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 32\text{ }\Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
G		14			dB
P_O	THD $\leq 0.5\%$, $f = 1\text{ kHz}$	7.5			mW
THD+N	$P_O = 6.5\text{ mW}$, 20–20 kHz	0.05%			
BOM	THD $< 1\%$	> 20			kHz
k _{SVR}	$f = 1\text{ kHz}$	47			dB
SNR	$P_O = 7.5\text{ mW}$	84			dB
V_n		32			$\mu\text{V(rms)}$

TYPICAL CHARACTERISTICS**Table of Graphs**

		FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency
		vs Output power
		vs Output voltage
P_O	Output power	vs Load resistance
k _{SVR}	Supply ripple rejection ratio	vs Frequency
V_n	Output noise voltage	vs Frequency
	Crosstalk	vs Frequency
	Closed-loop gain and phase	vs Frequency
I_{DD}	Supply current	vs Supply voltage
P_D	Power dissipation	vs Output power

TYPICAL CHARACTERISTICS

**TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY**

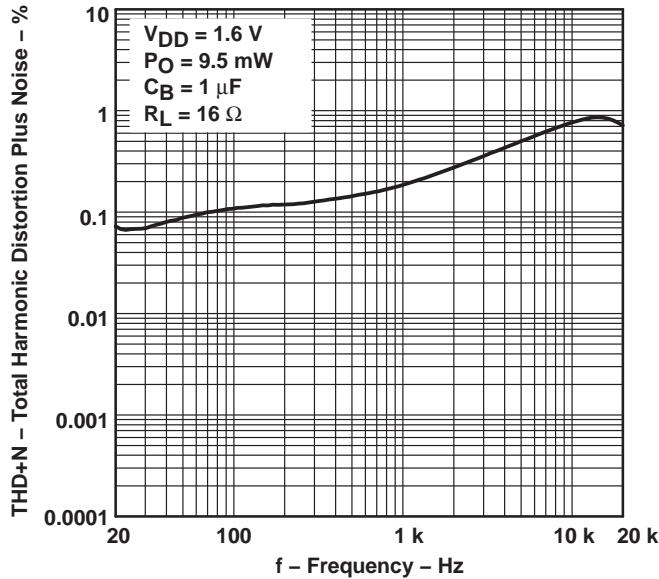


Figure 1

**TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER**

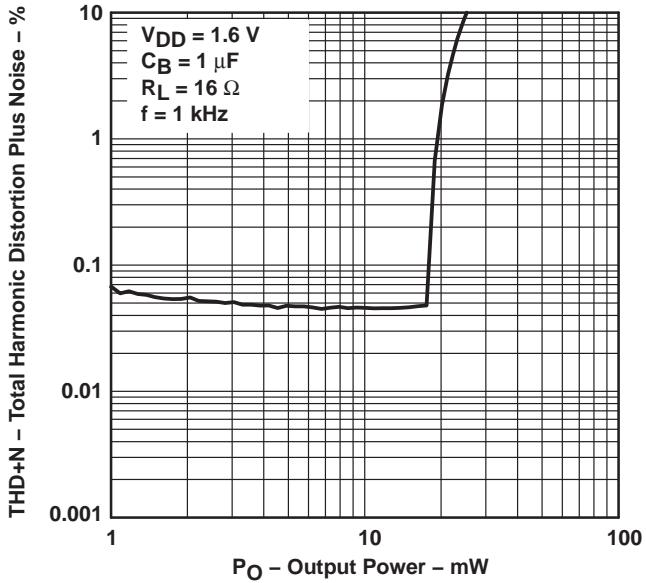


Figure 2

**TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY**

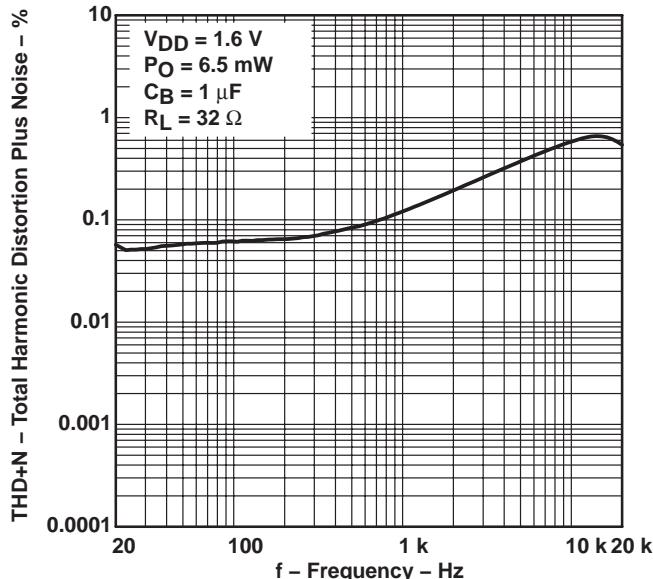


Figure 3

**TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER**

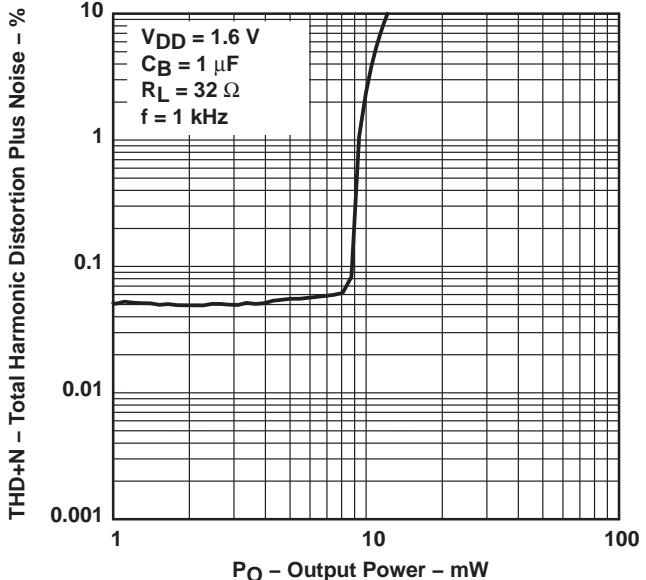


Figure 4

TYPICAL CHARACTERISTICS

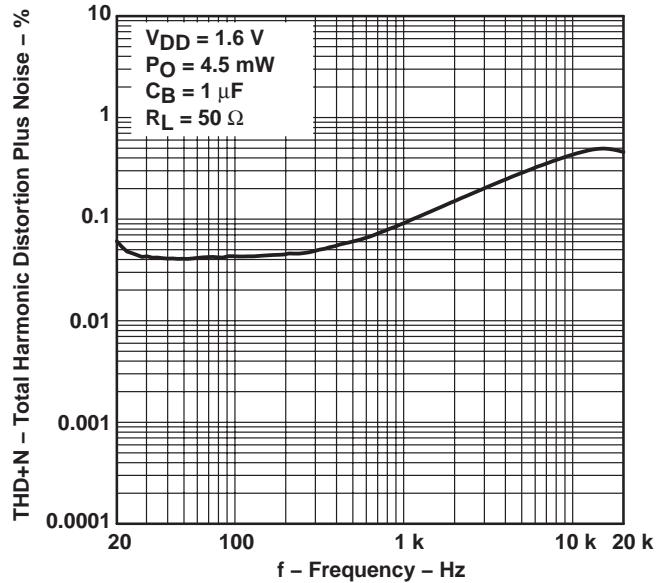
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 5

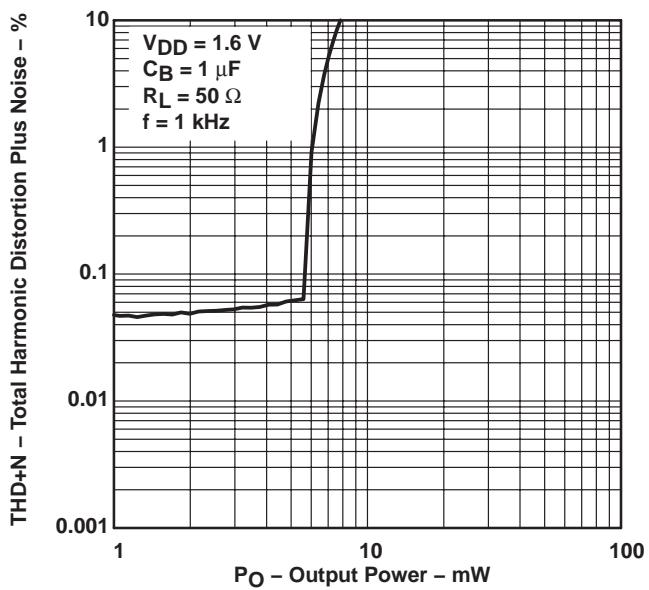
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 6

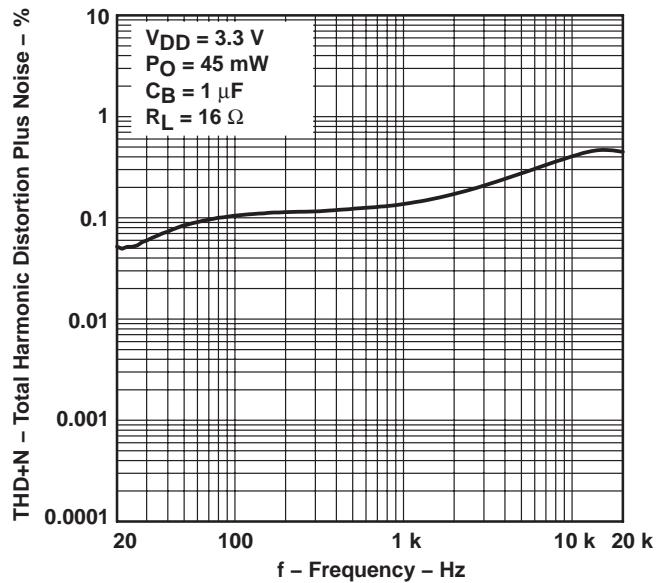
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 7

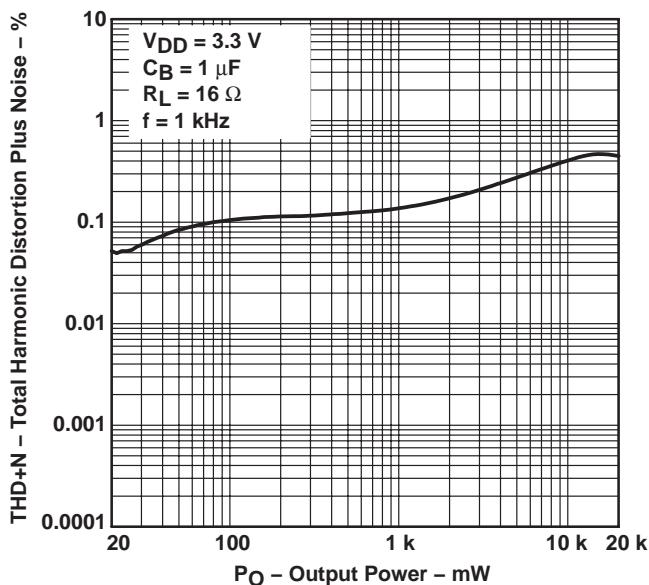
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 8

TYPICAL CHARACTERISTICS

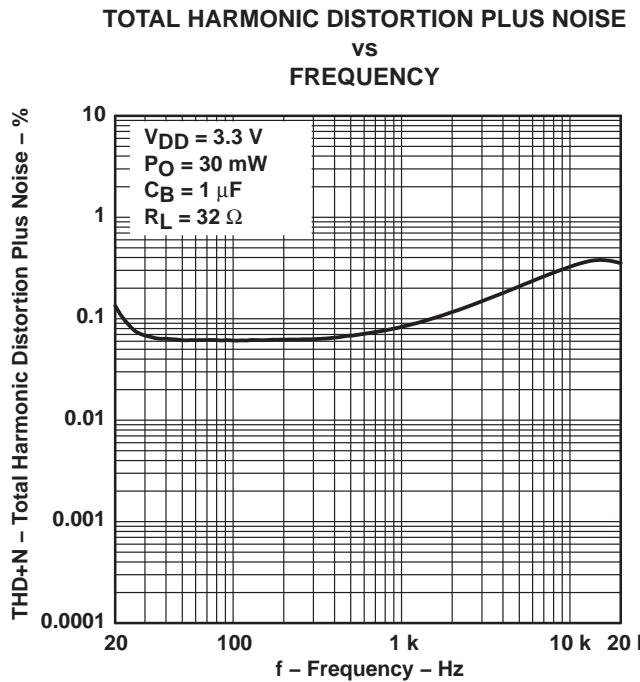


Figure 9

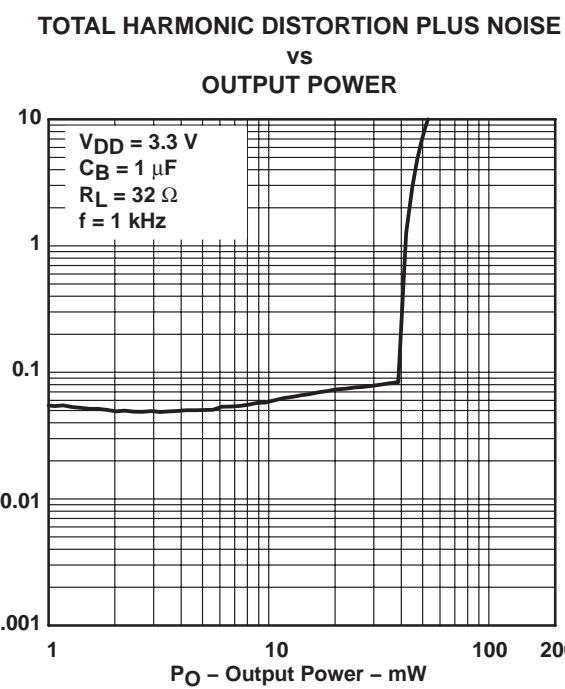


Figure 10

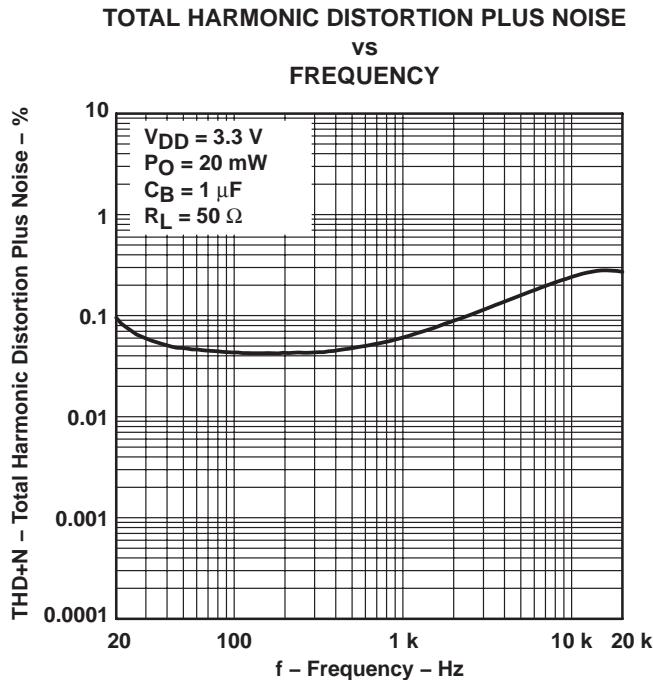


Figure 11

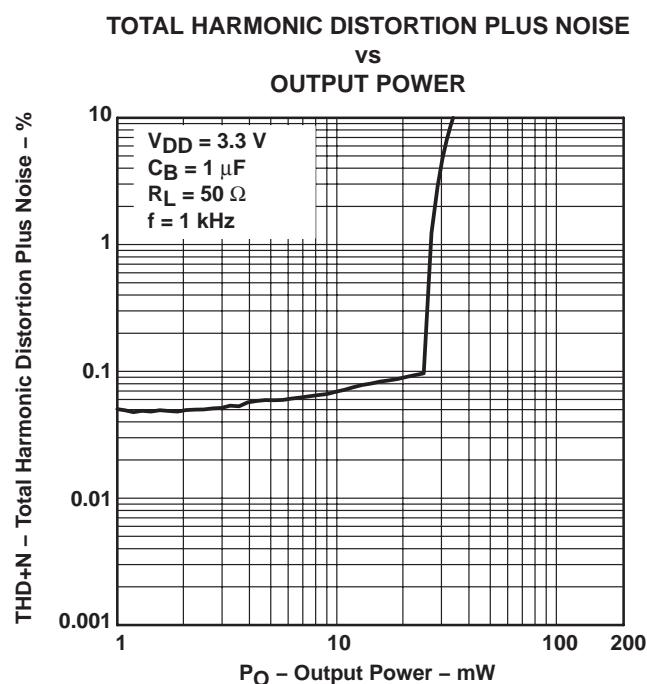


Figure 12

TYPICAL CHARACTERISTICS

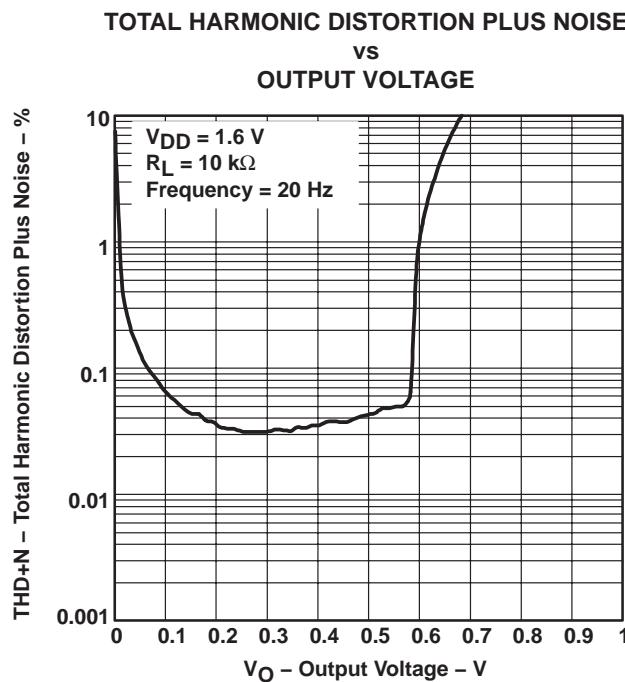


Figure 13

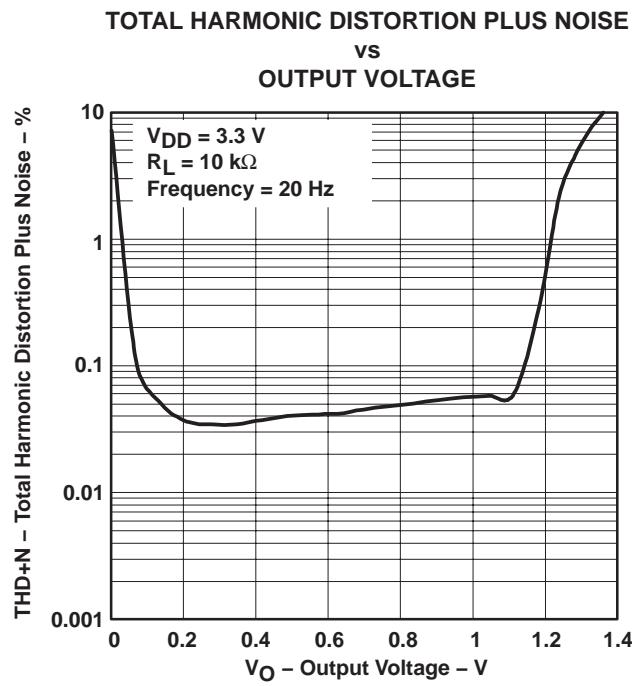


Figure 14

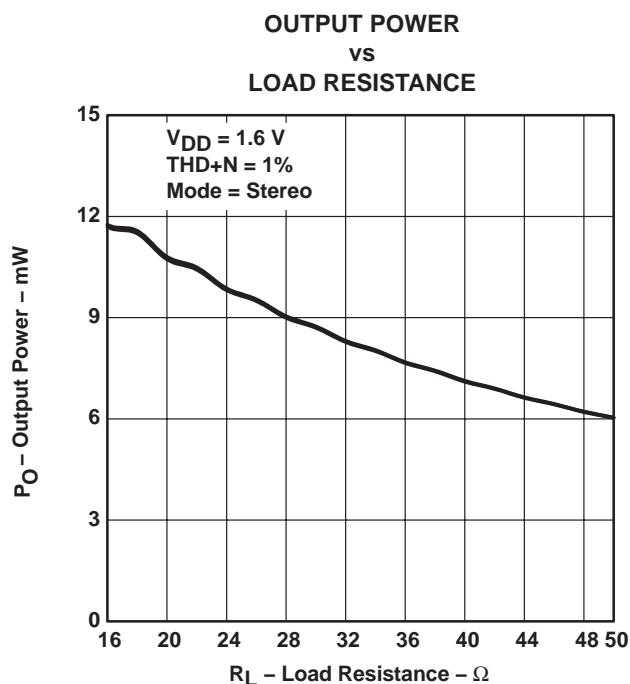


Figure 15

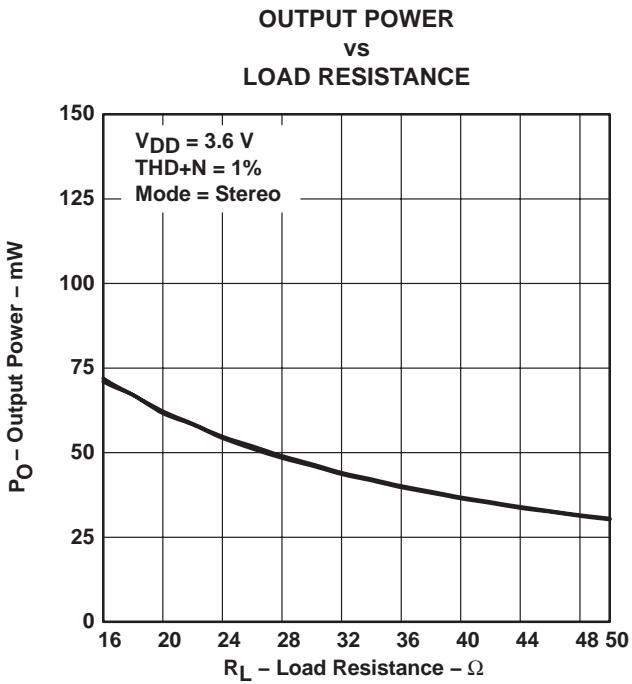


Figure 16

TYPICAL CHARACTERISTICS

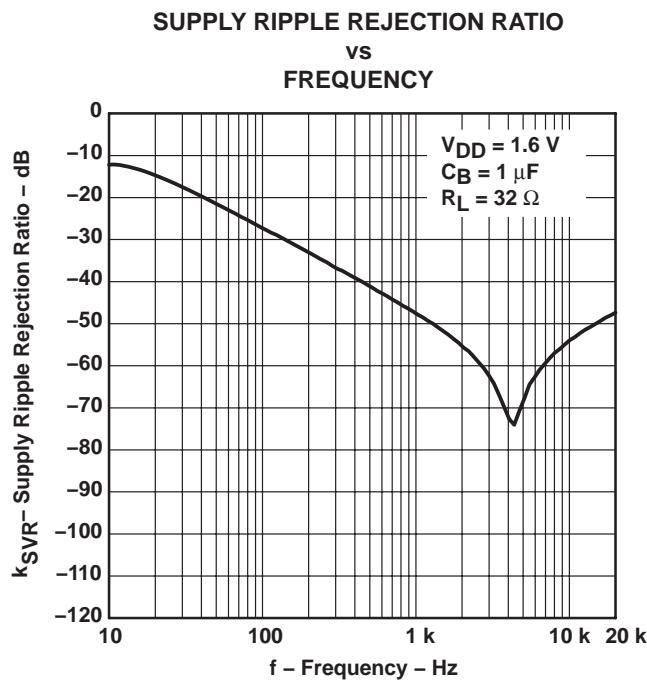


Figure 17

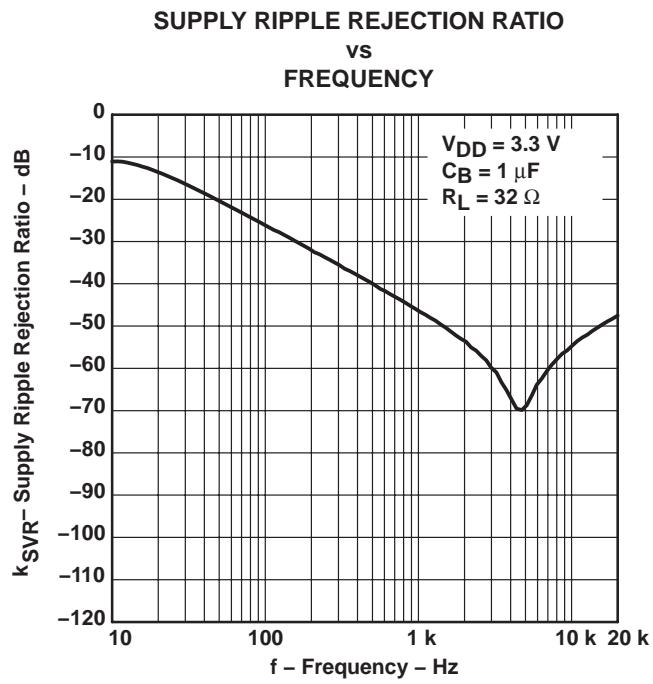


Figure 18

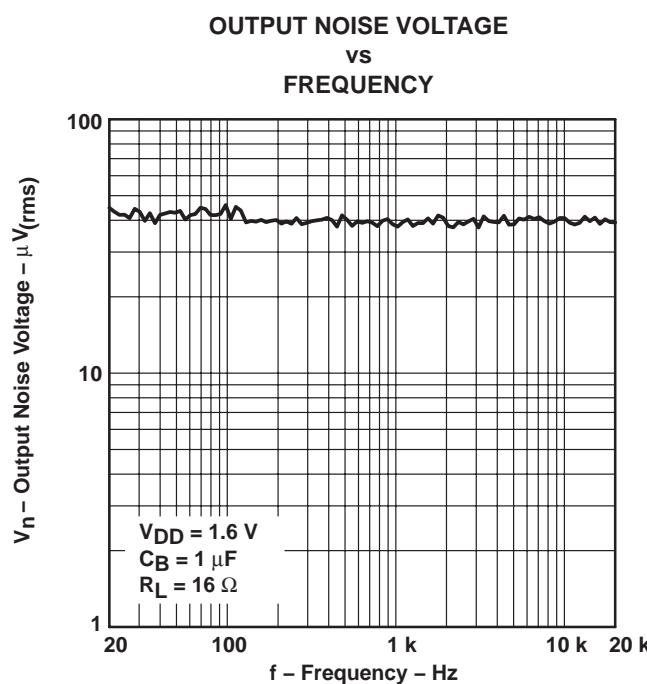


Figure 19

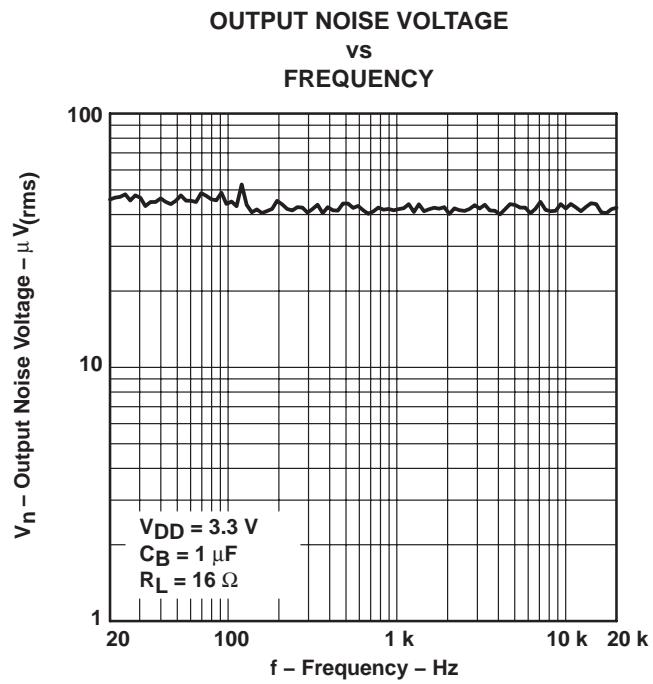
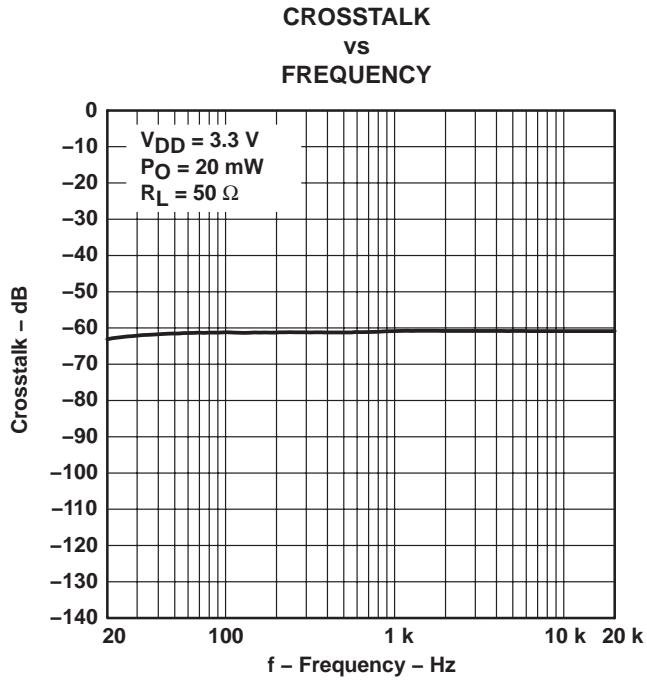
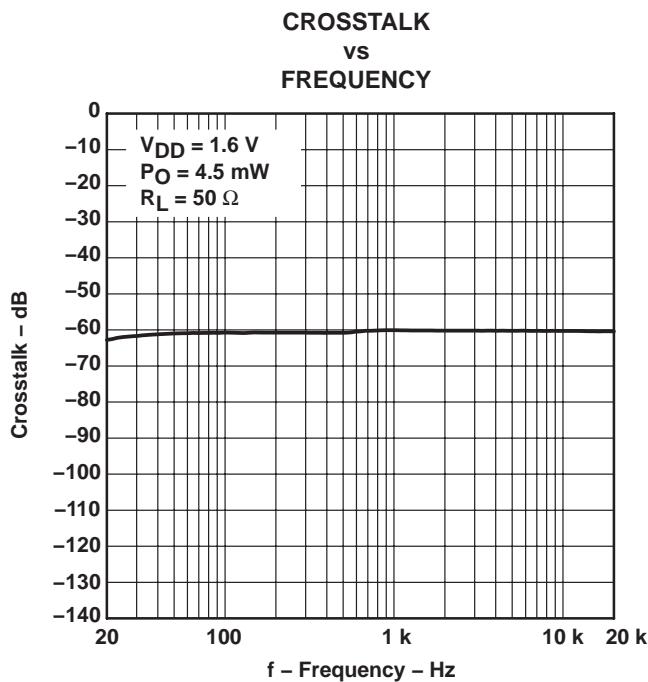
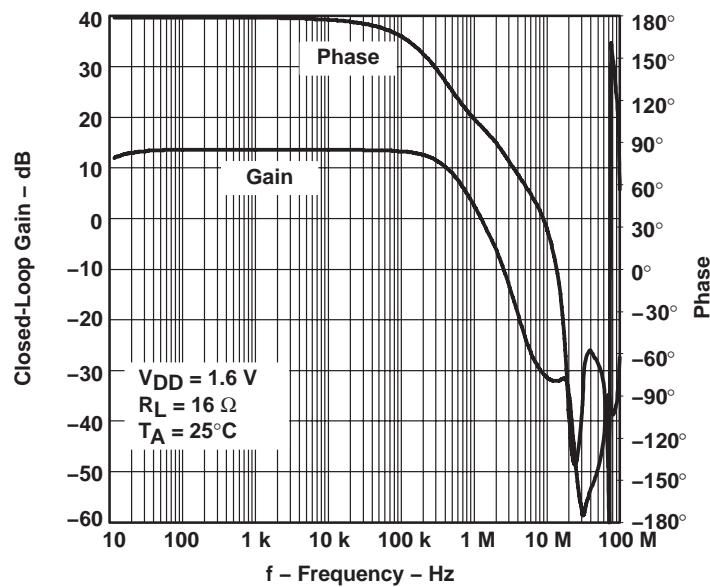


Figure 20

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE

vs
FREQUENCY

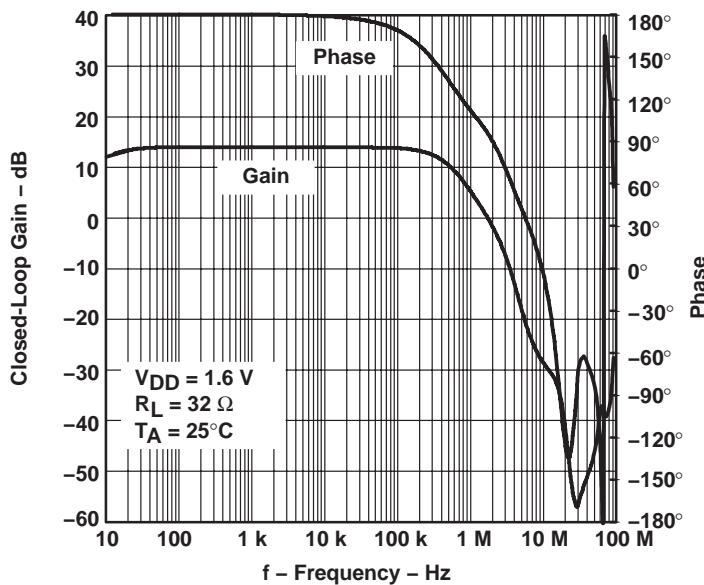


Figure 24

CLOSED-LOOP GAIN AND PHASE

vs
FREQUENCY

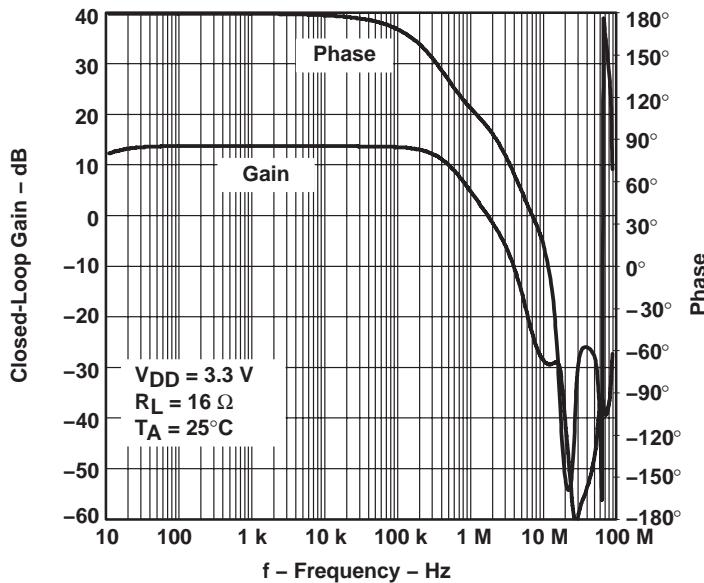


Figure 25

TYPICAL CHARACTERISTICS

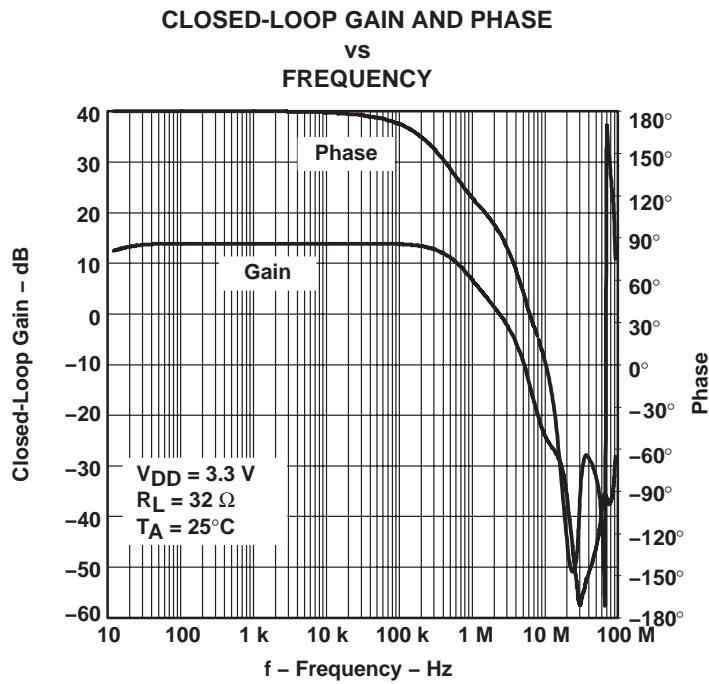


Figure 26

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

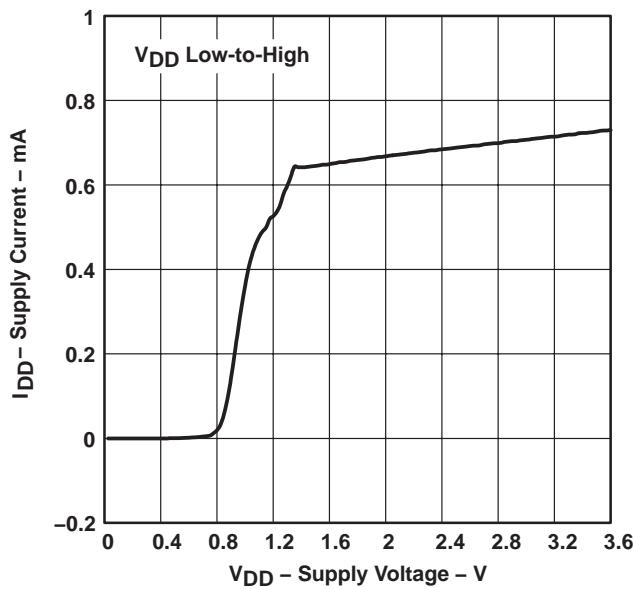


Figure 27

**POWER DISSIPATION
vs
OUTPUT POWER**

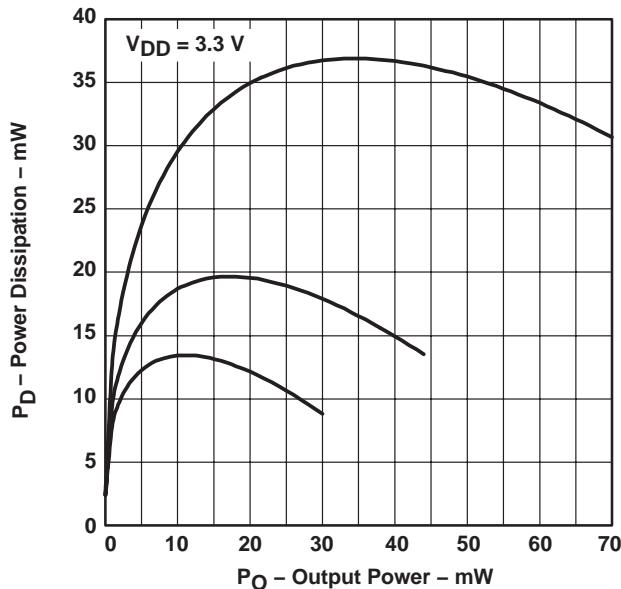


Figure 28

APPLICATION INFORMATION

input capacitor, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 1. R_I is set internally and is fixed at 20 k Ω .

$$f_C = \frac{1}{2\pi R_I C_I} \quad (1)$$

The value of C_I is important to consider, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where the specification calls for a flat bass response down to 20 Hz. Equation 1 is reconfigured as equation 2.

$$C_I = \frac{1}{2\pi R_I f_C} \quad (2)$$

In this example, C_I is 0.40 μ F, so one would likely choose a value in the range of 0.47 μ F to 1 μ F. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I , C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/4$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA6102A2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μ F, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μ F or greater placed near the power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor (C_B) serves several important functions. During start-up, C_B determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 55-k Ω source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 3 should be maintained.

$$\frac{1}{(C_B \times 55 \text{ k}\Omega)} \leq \frac{1}{(C_I R_I)} \quad (3)$$

As an example, consider a circuit where C_B is 1 μ F, C_I is 1 μ F, and R_I is 20 k Ω . Inserting these values into the equation 3 results in: $18.18 \leq 50$ which satisfies the rule. Bypass capacitor (C_B) with values of 0.47- μ F to 1- μ F ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

APPLICATION INFORMATION

output coupling capacitor, C_C

In the typical single-supply single-ended (SE) configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 4.

$$f_C = \frac{1}{2\pi R_L C_C} \quad (4)$$

The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher. Large values of C_C are required to pass low-frequencies into the load. Consider the example where a C_C of 68 μ F is chosen and loads vary from 32 Ω to 47 k Ω . Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common-Load Impedances vs Low-Frequency Output Characteristics in SE Mode

R_L	C_C	Lowest Frequency
32 Ω	68 μ F	73 Hz
10,000 Ω	68 μ F	0.23 Hz
47,000 Ω	68 μ F	0.05 Hz

As Table 1 indicates, headphone response is adequate and drive into line level inputs (a home stereo for example) is very good.

The output-coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{(C_B \times 55 \text{ k}\Omega)} \leq \frac{1}{(C_I R_I)} \ll \frac{1}{R_L C_C} \quad (5)$$

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

3.3-V versus 1.6-V operation

The TPA6102A2 was designed for operation over a supply range of 1.6 V to 3.6 V. There are no special considerations for 1.6-V versus 3.3-V operation as far as supply bypassing, gain setting, or stability. Supply current is slightly reduced from 0.75 mA (typical) to 0.65 mA (typical). The most important consideration is that of output power. Each amplifier can produce a maximum output voltage swing within a few hundred millivolts of the rails with a 10-k Ω load. However, this voltage swing decreases as the load resistance decreases and the $r_{DS(on)}$ as the output stage transistors becomes more significant. For example, for a 32- Ω load, the maximum peak output voltage with $V_{DD} = 1.6$ V is approximately 0.7 V with no clipping distortion. This reduced voltage swing effectively reduces the maximum undistorted output power.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA6102A2D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6102A2
TPA6102A2D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6102A2
TPA6102A2DGK	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJN
TPA6102A2DGK.A	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJN
TPA6102A2DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJN
TPA6102A2DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

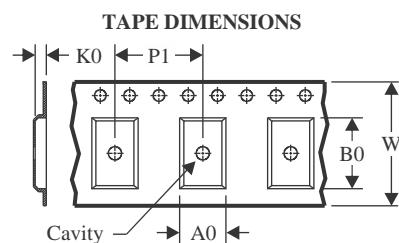
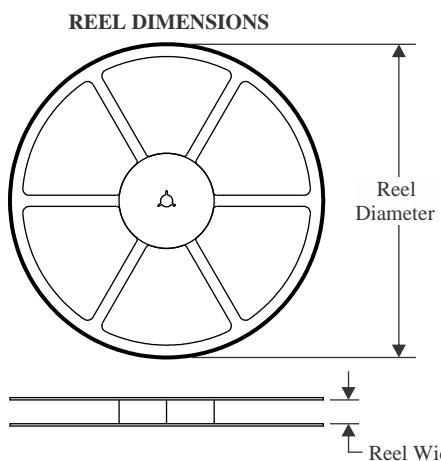
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6102A2DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6102A2DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPA6102A2D	D	SOIC	8	75	505.46	6.76	3810	4
TPA6102A2D.A	D	SOIC	8	75	505.46	6.76	3810	4

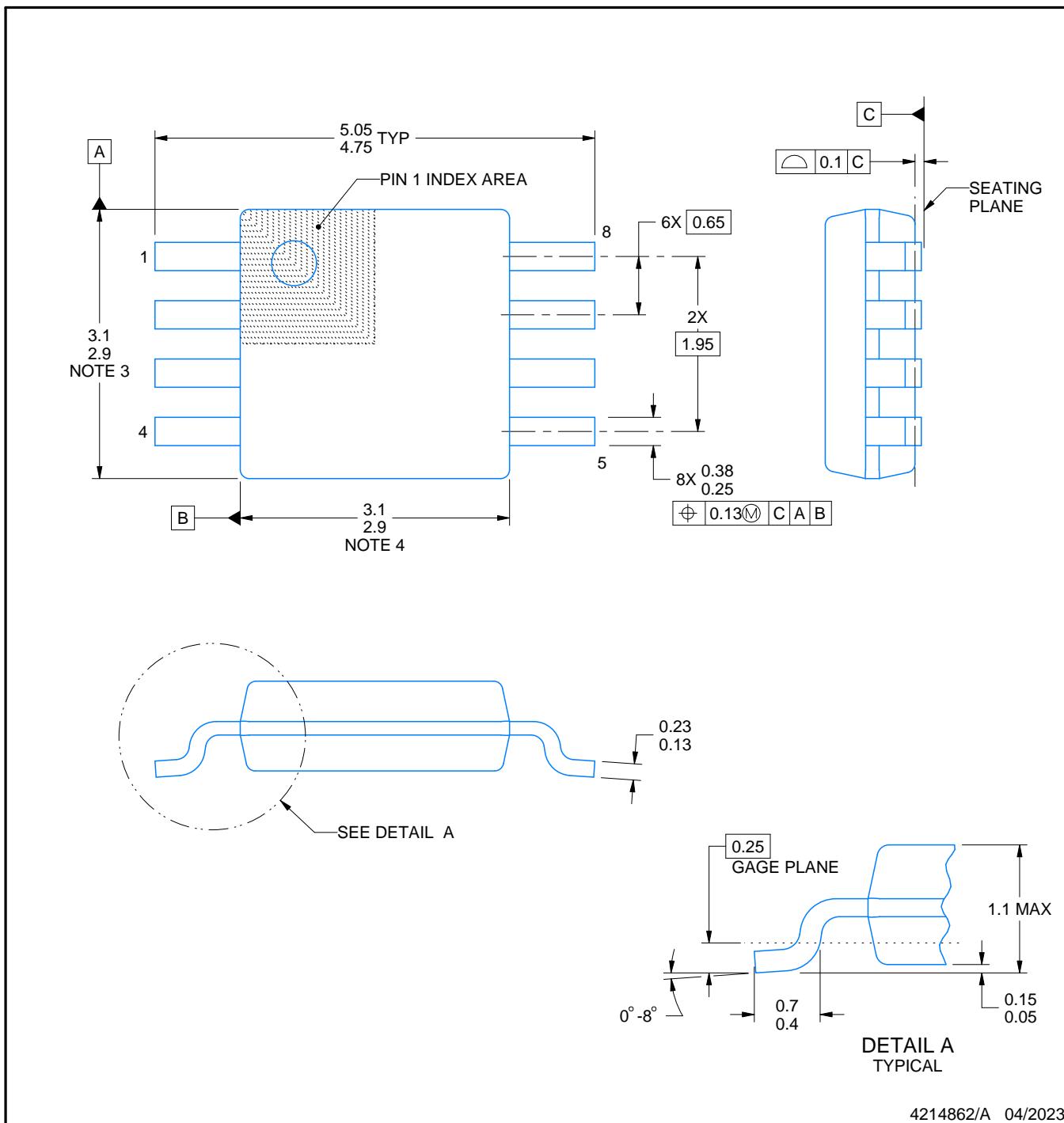
PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

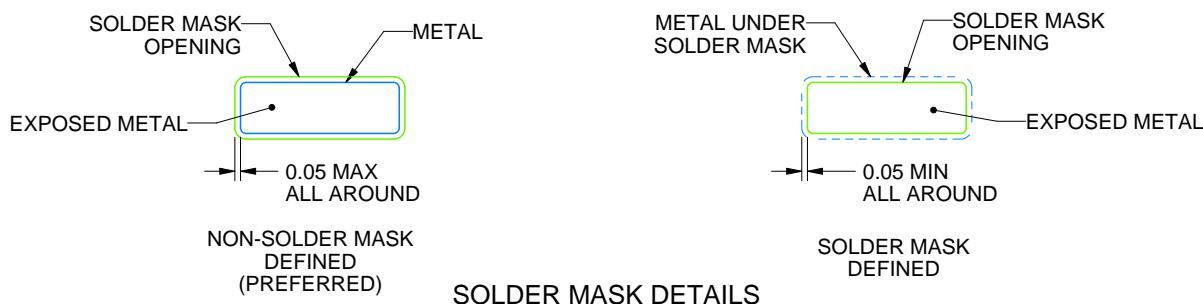
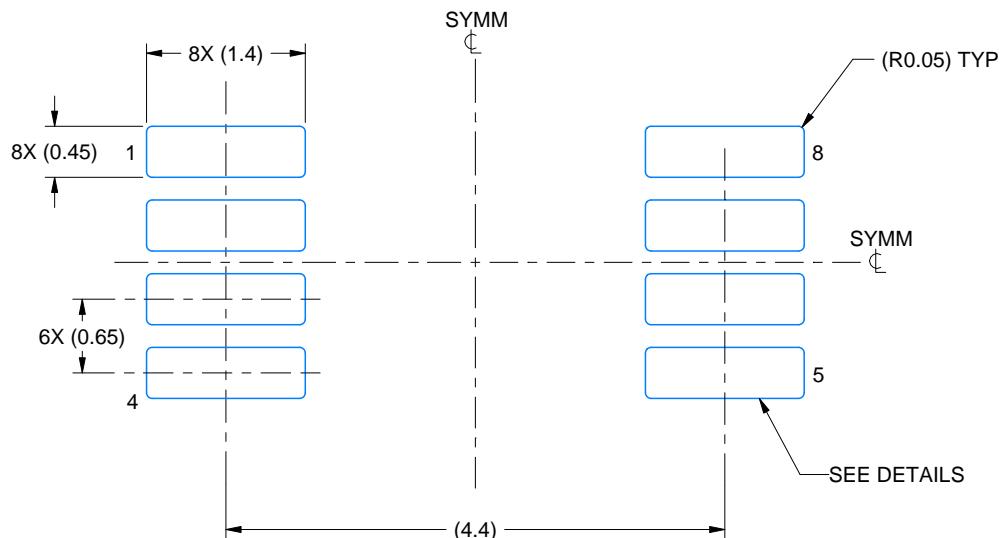
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES: (continued)

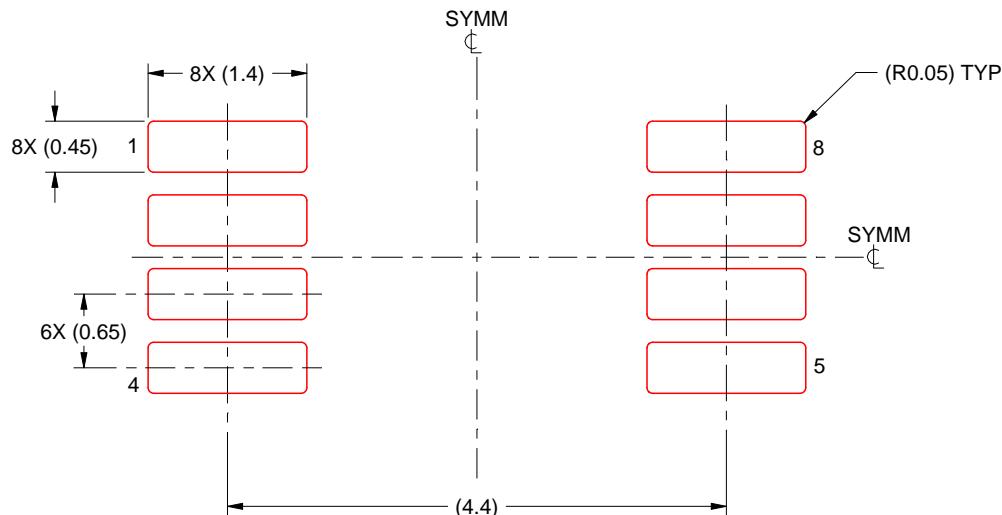
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

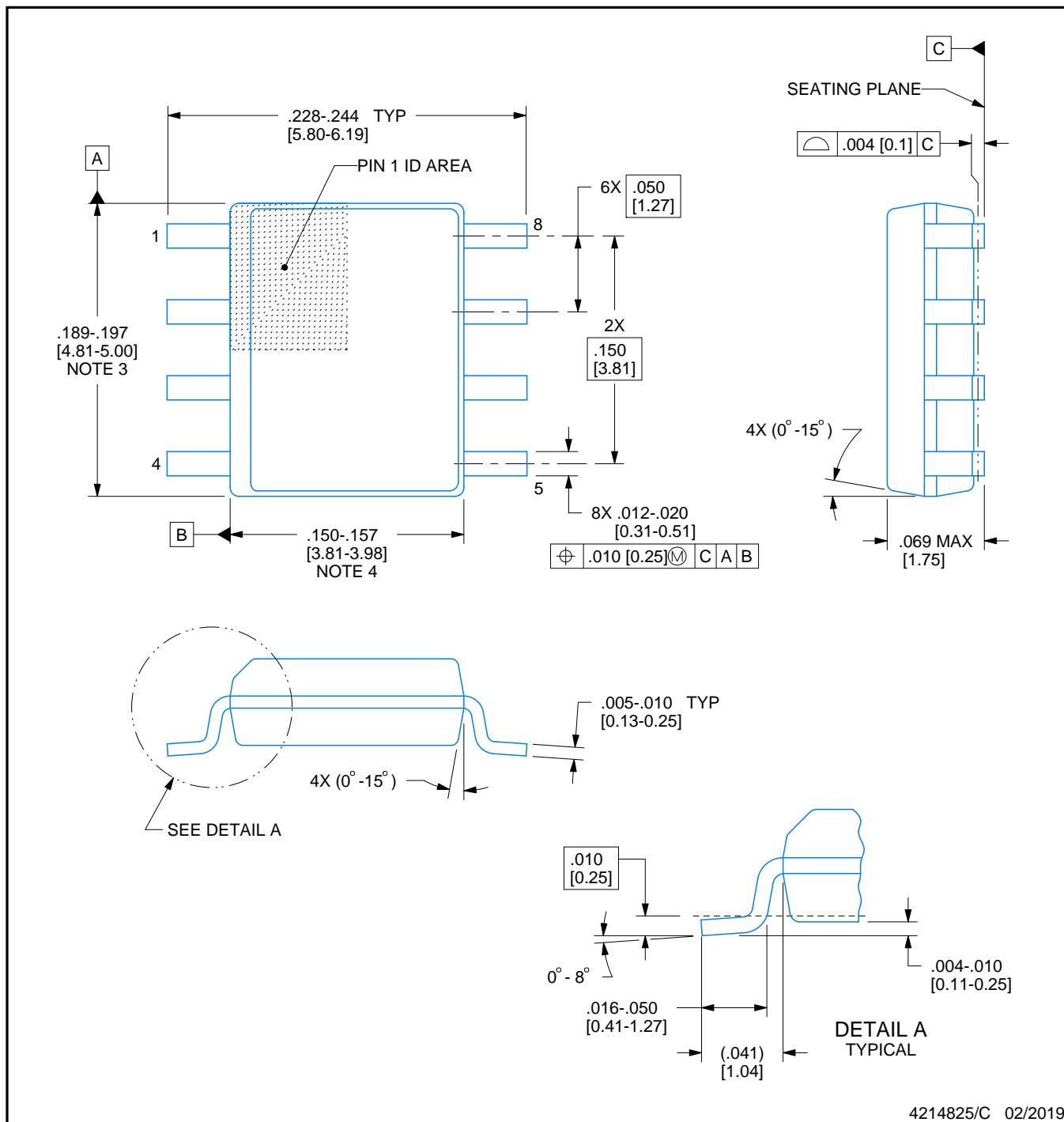


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

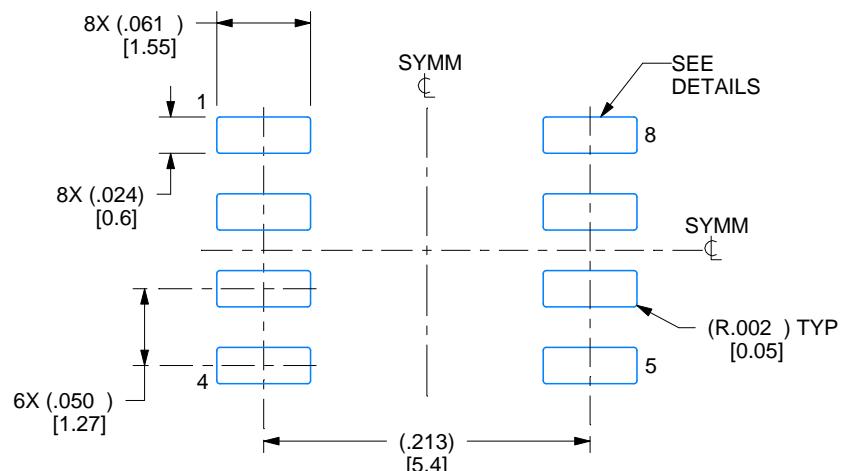
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

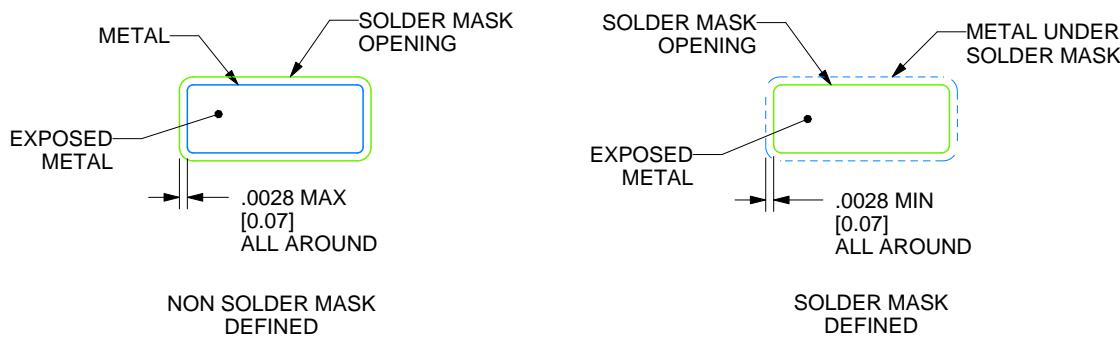
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

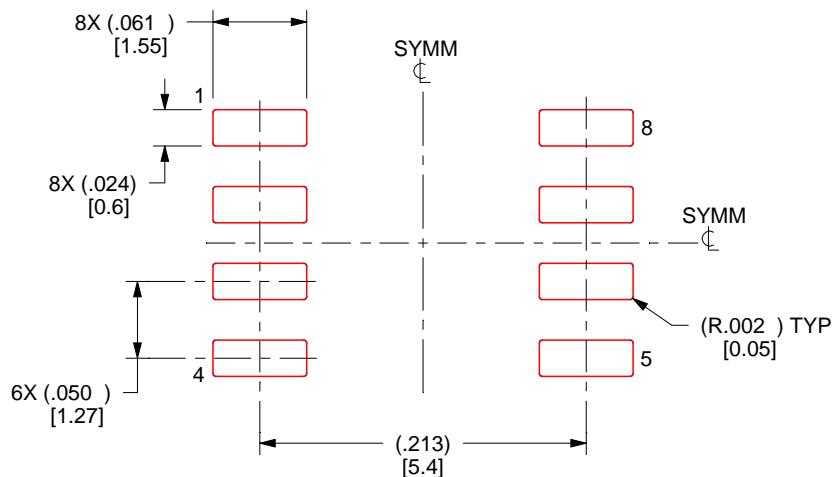
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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