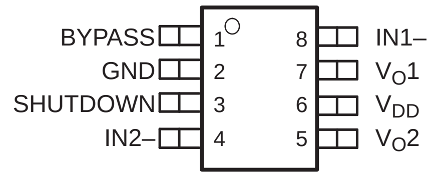
150-mW STEREO AUDIO POWER AMPLIFIER

Check for Samples: TPA6110A2

FEATURES

- **150 mW Stereo Output**
- **PC Power Supply Compatible**
  - **Fully Specified for 3.3 V and 5 V Operation**
  - **Operation to 2.5 V**
- **Pop Reduction Circuitry**
- **Internal Mid-Rail Generation**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **PowerPAD™ MSOP**
- **Pin Compatible With LM4881**

DGN PACKAGE
(TOP VIEW)

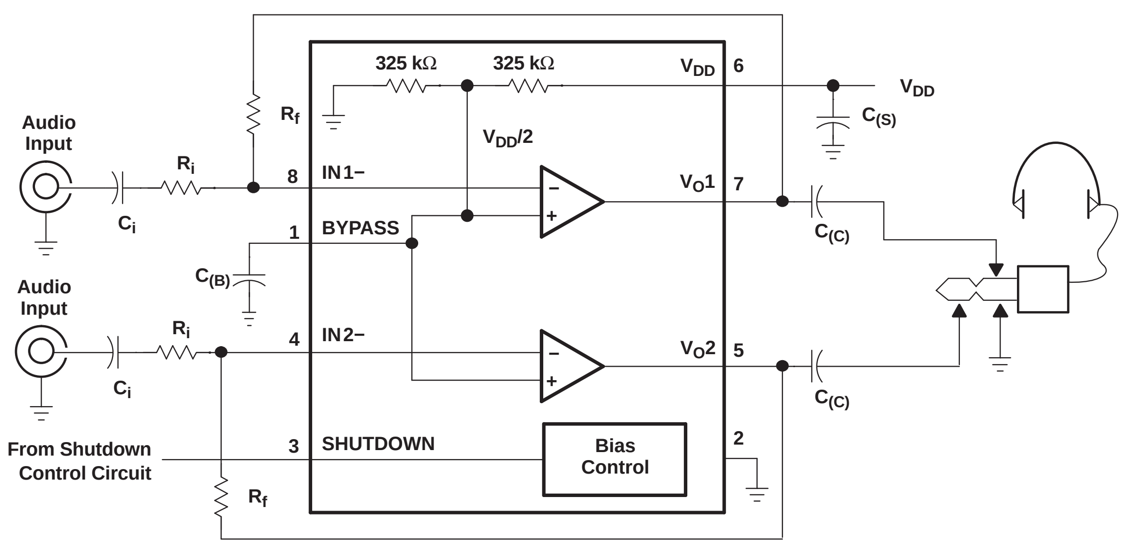


DESCRIPTION

The TPA6110A2 is a stereo audio power amplifier packaged in an 8-pin PowerPAD™ MSOP package capable of delivering 150 mW of continuous RMS power per channel into 16-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10.

THD+N when driving a 16-Ω load from 5 V is 0.03% at 1 kHz, and less than 1% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.02% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz. For 10-kΩ loads, the THD+N performance is 0.005% at 1 kHz, and less than 0.5% across the audio band of 20 Hz to 20 kHz.

TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE MSOP(1)	MSOP SYMBOLIZATION
-40°C to 85°C	TPA6110A2DGN	TI AIZ

(1) The DGN package is available in left-ended tape and reel only (e.g., TPA6110A2DGNR).

PinFunctions

PIN NAME	PIN NO.	I/O	DESCRIPTION
BYPASS	1	I	Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1 µF to 1 µF low ESR capacitor for best performance.
GND	2	I	GND is the ground connection.
IN1–	8	I	IN1– is the inverting input for channel 1.
IN2–	4	I	IN2– is the inverting input for channel 2.
SHUTDOWN	3	I	Puts the device in a low quiescent current mode when held high.
V_{DD}	6	I	V_{DD} is the supply voltage terminal.
V_O1	7	O	V_O1 is the audio output for channel 1.
V_O2	5	O	V_O2 is the audio output for channel 2.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		UNIT
V_{DD}	Supply voltage	6 V
V_I	Input voltage	–0.3 V to V_{DD} + 0.3 V
	Continuous total power dissipation	Internally limited
T_J	Operating junction temperature range	-40°C to 150°C
T_{stg}	Storage temperature range	-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGN	2.14 W(1)	17.1 mW/°C	1.37 W	1.11 W

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), for more information on the PowerPAD™ package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2.5	5.5	V
T_A	Operating free-air temperature	-40	85	°C
V_{IH}	High-level input voltage (SHUTDOWN)	60% x V_{DD}		V
V_{IL}	Low-level input voltage (SHUTDOWN)		25% x V_{DD}	V

DC ELECTRICAL CHARACTERISTICS

at T_A = 25°C, V_{DD} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage	A_v = 2 V/V			15	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		83		dB
I_{DD}	Supply current	SHUTDOWN = 0 V		1.5	3	mA
$I_{DD(SD)}$	Supply current in shutdown mode	SHUTDOWN = V_{DD}		1	10	µA

AC OPERATING CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD≤ 0.1%, f = 1 kHz		60		mW
THD+N	Total harmonic distortion + noise	P_O = 40 mW, 20 - 20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 10, THD < 5%		> 20		kHz
	Phase margin	Open loop		96°		
	Supply ripple rejection ratio	f = 1 kHz		71		dB
	Channel/channel output separation	f = 1 kHz, P_O = 40 mW		89		dB
SNR	Signal-to-noise ratio	P_O = 50 mW, A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1		11		µV(rms)

DC ELECTRICAL CHARACTERISTICS

at T_A = 25°C, V_{DD} = 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage	A_V = 2 V/V			15	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		76		dB
I_{DD}	Supply current	SHUTDOWN = 0 V		1.5	3	mA
$I_{DD(SD)}$	Supply current in shutdown mode	SHUTDOWN = V_{DD}		1	10	µA
$\lvert I_{IH} \rvert$	High-level input current (SHUTDOWN)	V_{DD} = 5.5 V, V_I = V_{DD}			1	µA
$\lvert I_{IL} \rvert$	Low-level input current (SHUTDOWN)	V_{DD} = 5.5 V, V_I = 0 V			1	µA
Z_i	Input impedance			>1		MΩ

AC OPERATING CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD≤ 0.1%, f = 1 kHz		150		mW
THD+N	Total harmonic distortion + noise	P_O = 100 mW, 20 - 20 kHz		0.6%		
B_{OM}	Maximum output power BW	G = 10, THD < 5%		> 20		kHz
	Phase margin	Open loop		96°		
	Supply ripple rejection ratio	f = 1 kHz		61		dB
	Channel/Channel output separation	f = 1 kHz, P_O = 100 mW		90		dB
SNR	Signal-to-noise ratio	P_O = 100 mW, A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1		11.7		µV(rms)

AC OPERATING CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD≤ 0.1%, f = 1 kHz		40		mW
THD+N	Total harmonic distortion + noise	P_O = 30 mW, 20 - 20 kHz		0.4%		
B_{OM}	Maximum output power BW	A_V = 10, THD < 2%		> 20		kHz

AC OPERATING CHARACTERISTICS (continued)

V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Phase margin	Open loop		96°		
	Supply ripple rejection ratio	f = 1 kHz		71		dB
	Channel/channel output separation	f = 1 kHz		95		dB
SNR	Signal-to-noise ratio	P_O = 40 mW, A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1		11		μV(rms)

AC OPERATING CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD≤ 0.1%, f = 1 kHz		90		mW
THD+N	Total harmonic distortion + noise	P_O = 60 mW, 20 - 20 kHz		0.4%		
B_{OM}	Maximum output power BW	A_V = 10, THD < 2%		> 20		kHz
	Phase margin	Open loop		97°		
	Supply ripple rejection ratio	f = 1 kHz		61		dB
	Channel/channel output separation	f = 1 kHz		98		dB
SNR	Signal-to-noise ratio	P_O = 90 mW, A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1		11.7		μV(rms)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1, 3, 5, 6, 7, 9, 11, 13
		vs Output power	2, 4, 8, 10, 12, 14
	Supply ripple rejection ratio	vs Frequency	15, 16
V_n	Output noise voltage	vs Frequency	17, 18
	Crosstalk	vs Frequency	19–24
	Shutdown attenuation	vs Frequency	25, 26
	Open-loop gain and phase margin	vs Frequency	27, 28
	Output power	vs Load resistance	29, 30
I_{DD}	Supply current	vs Supply voltage	31
SNR	Signal-to-noise ratio	vs Voltage gain	32
	Power dissipation/amplifier	vs Load power	33, 34

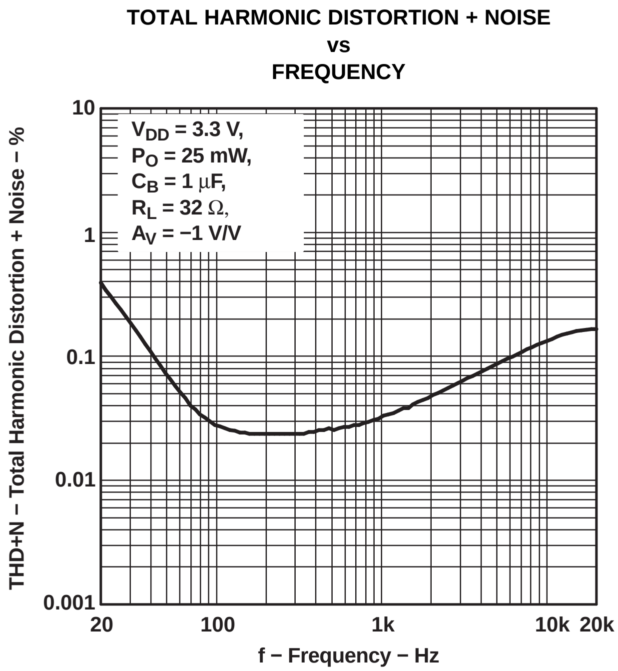


Figure 1.

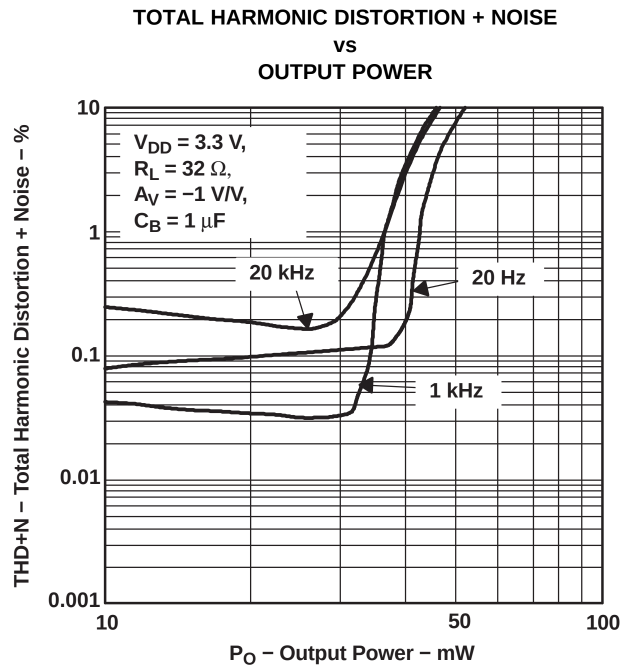


Figure 2.

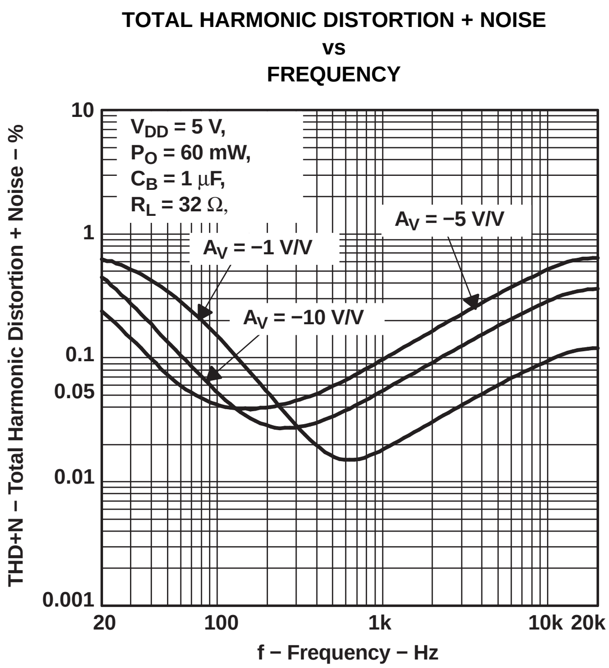


Figure 3.

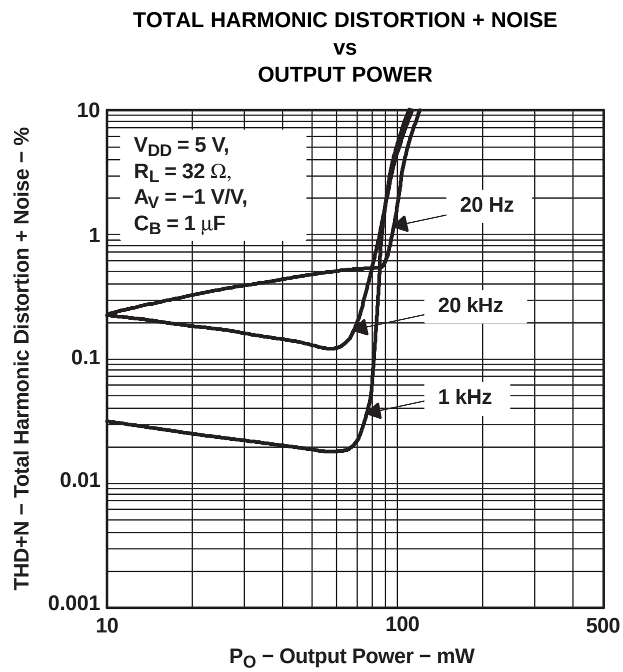


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

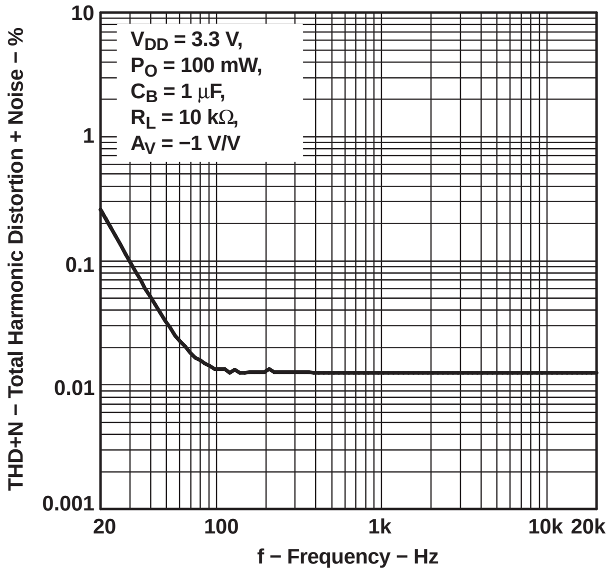


Figure 5.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

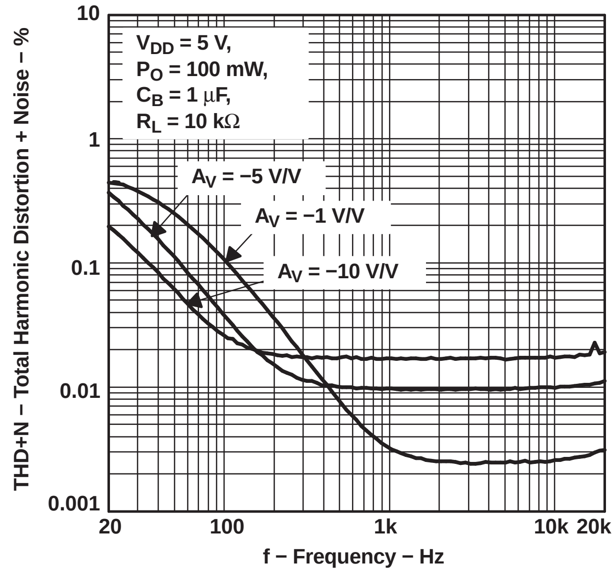


Figure 6.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

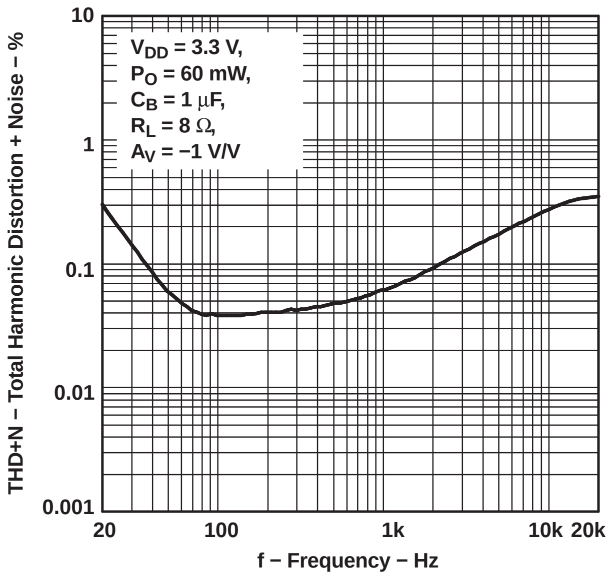


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

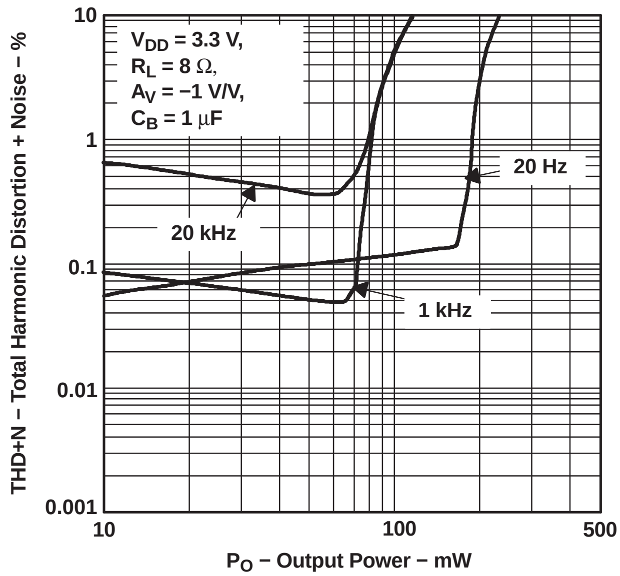


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

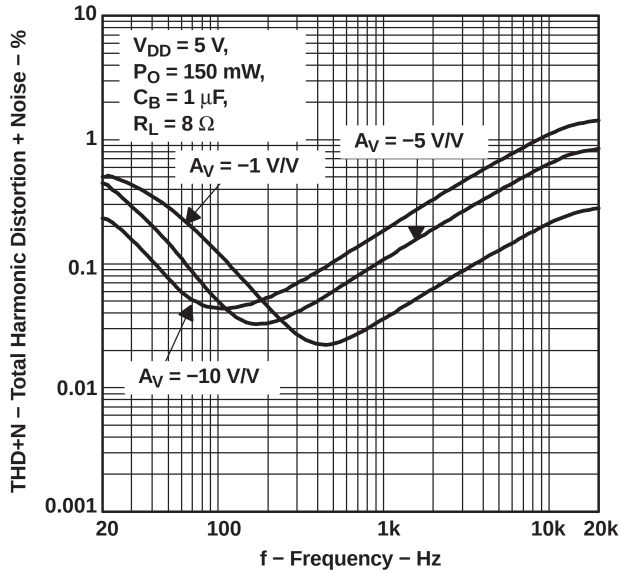


Figure 9.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

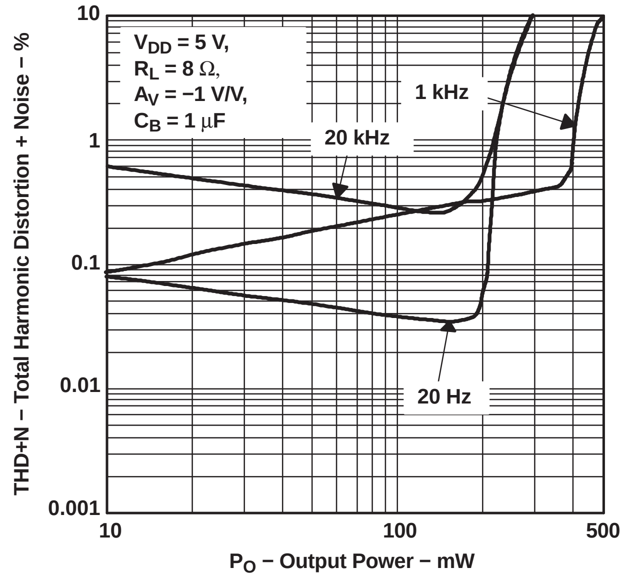


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

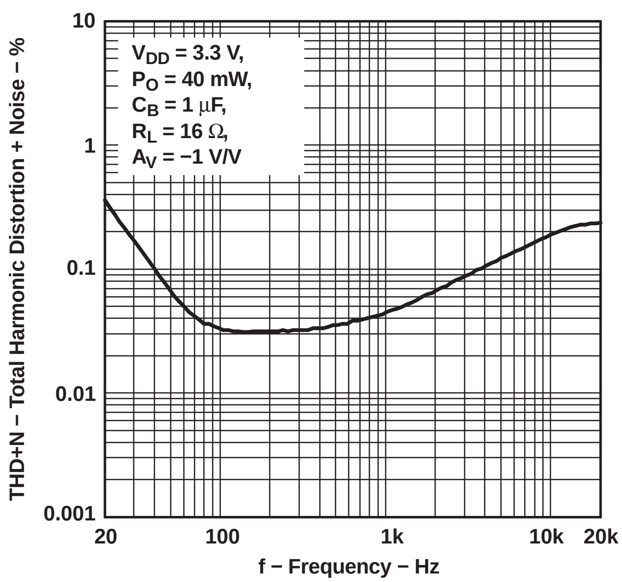


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

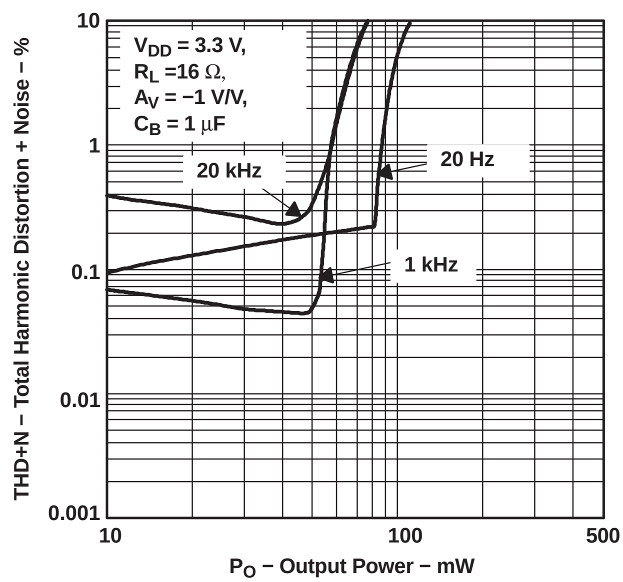


Figure 12.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

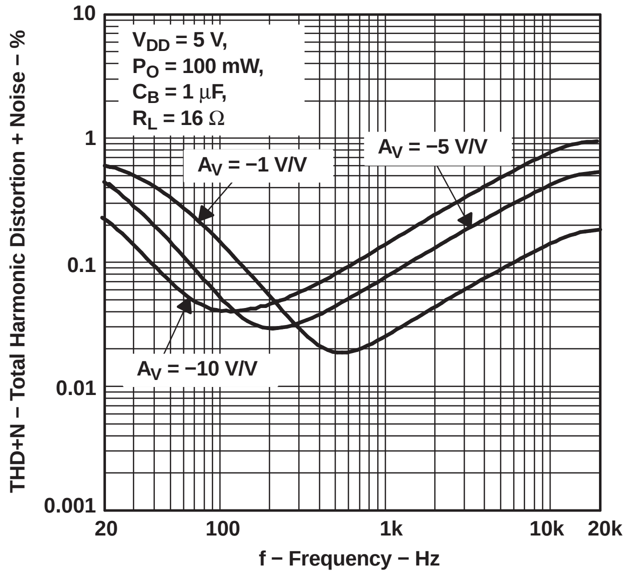


Figure 13.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER

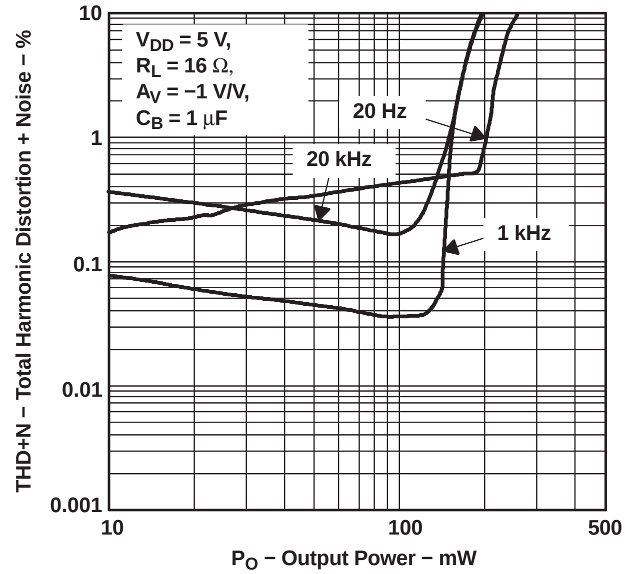


Figure 14.

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

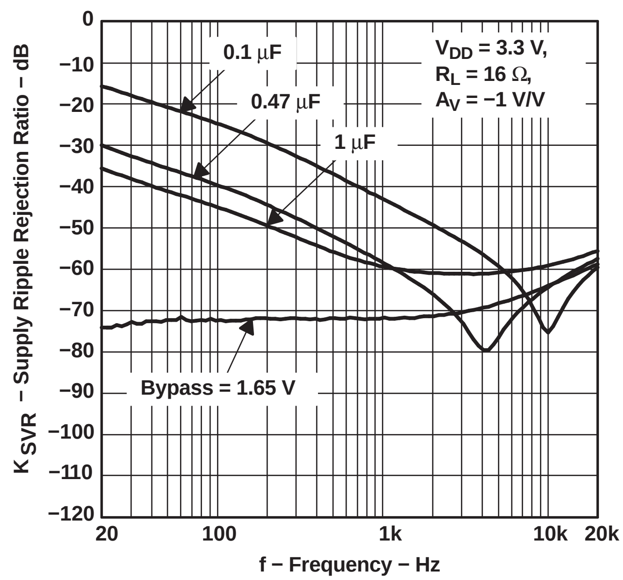


Figure 15.

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

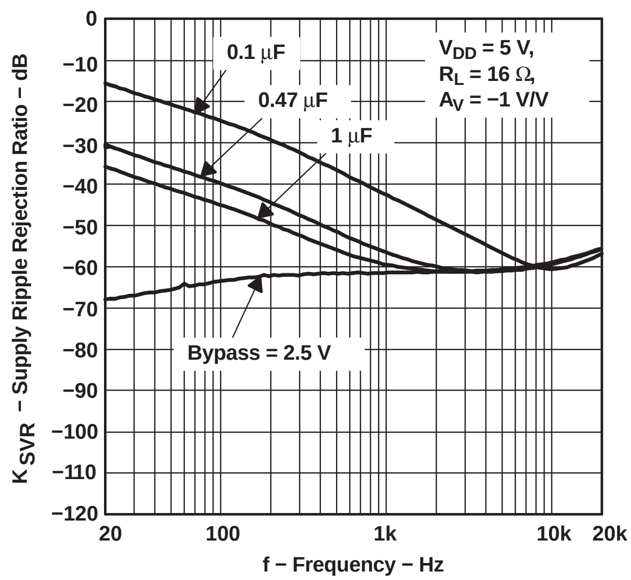


Figure 16.

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

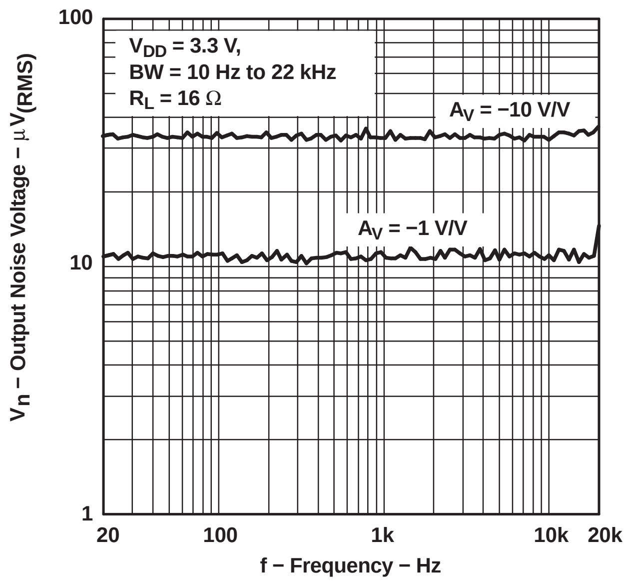


Figure 17.

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

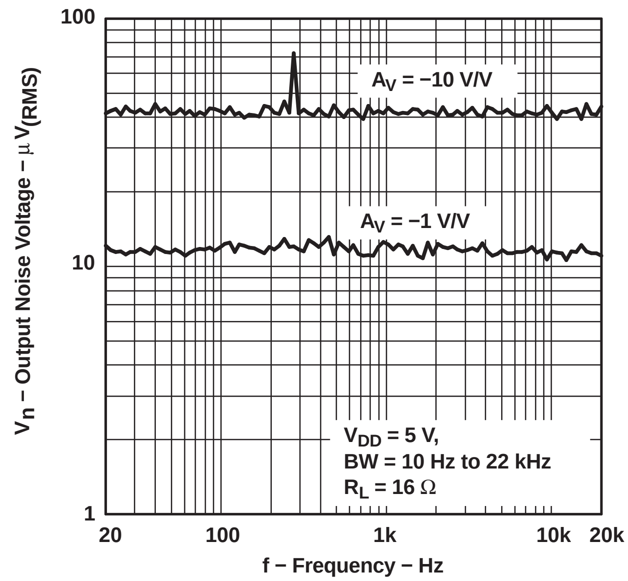


Figure 18.

CROSSTALK
vs
FREQUENCY

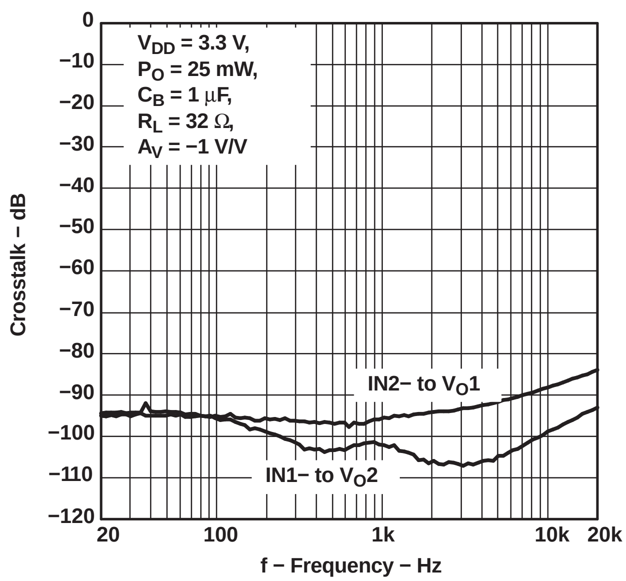


Figure 19.

CROSSTALK
vs
FREQUENCY

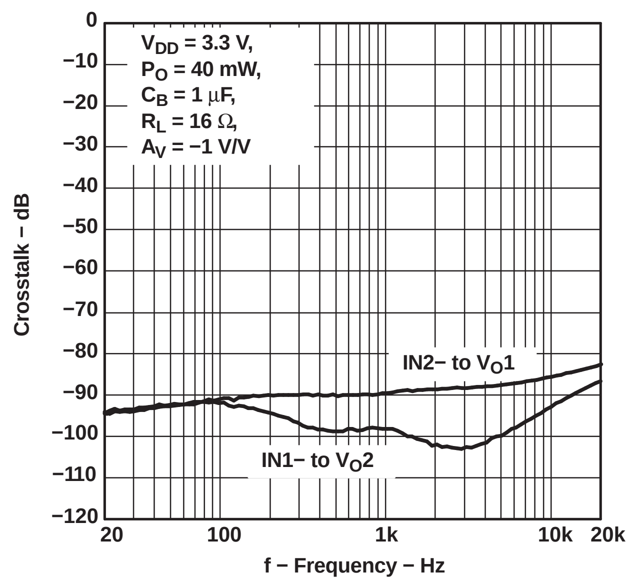


Figure 20.

CROSSTALK vs FREQUENCY

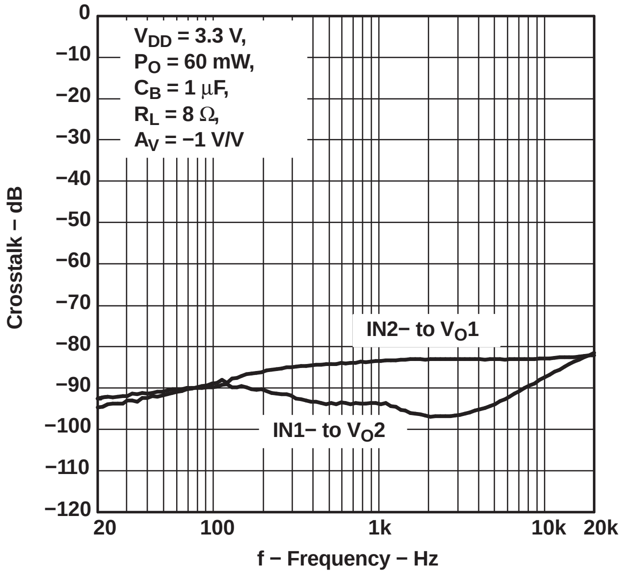


Figure 21.

CROSSTALK vs FREQUENCY

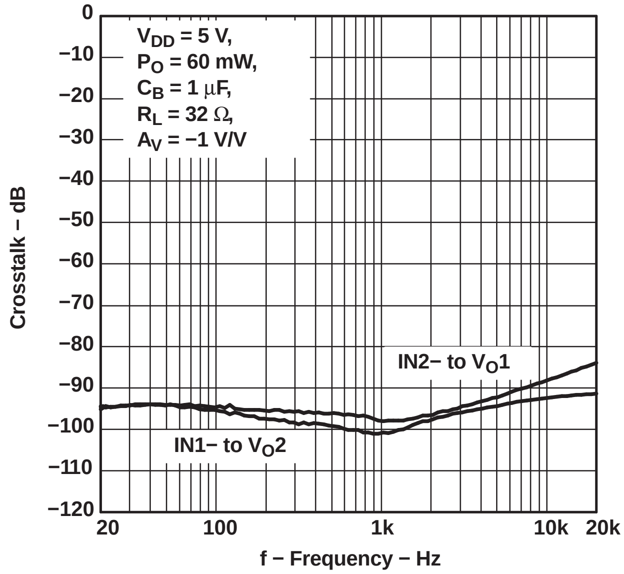


Figure 22.

CROSSTALK vs FREQUENCY

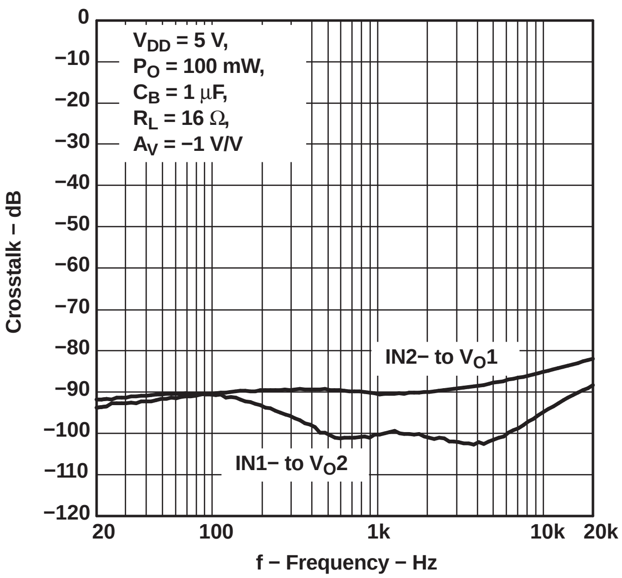


Figure 23.

CROSSTALK vs FREQUENCY

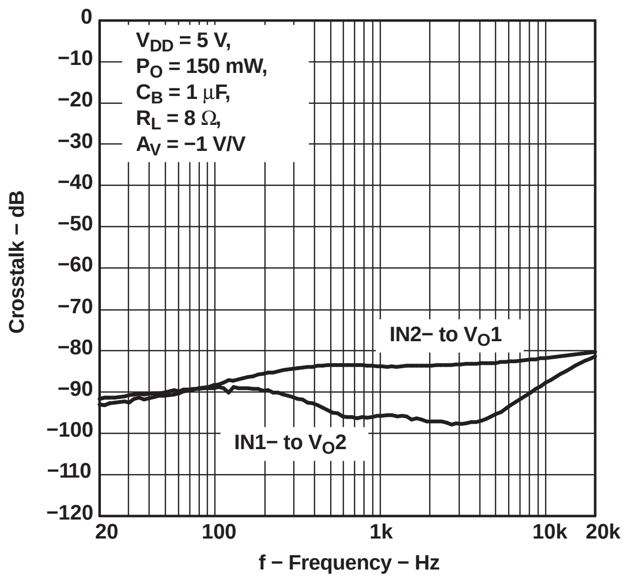


Figure 24.

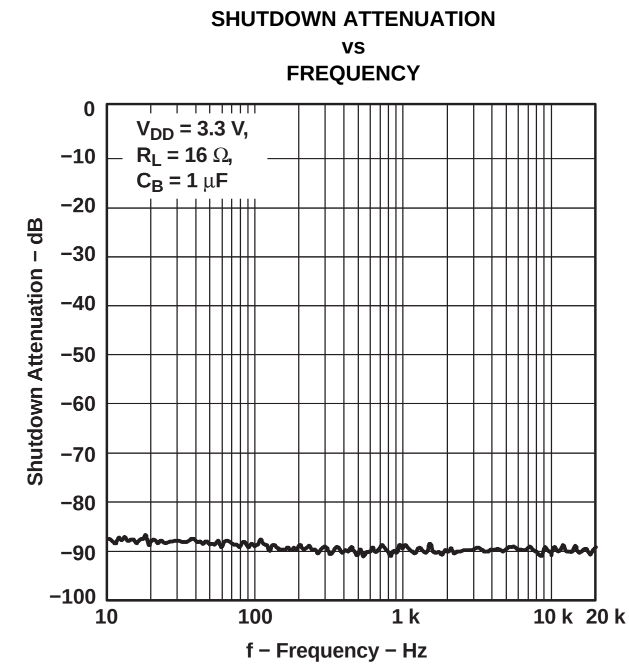
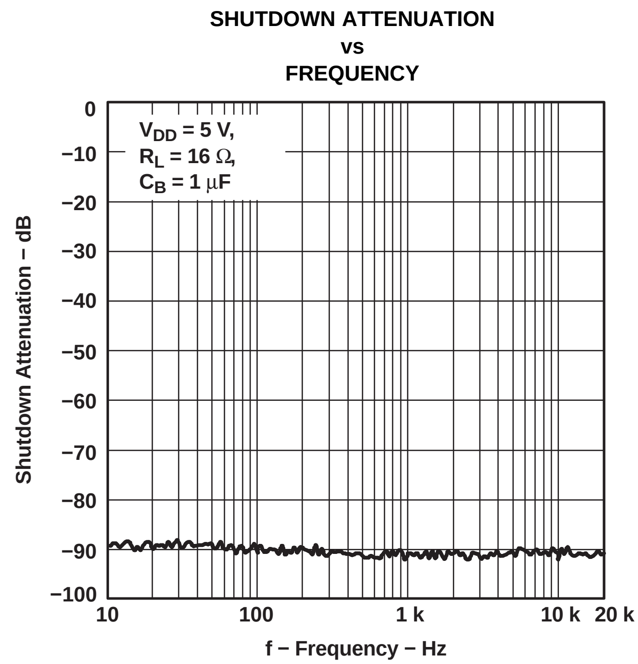


Figure 25.



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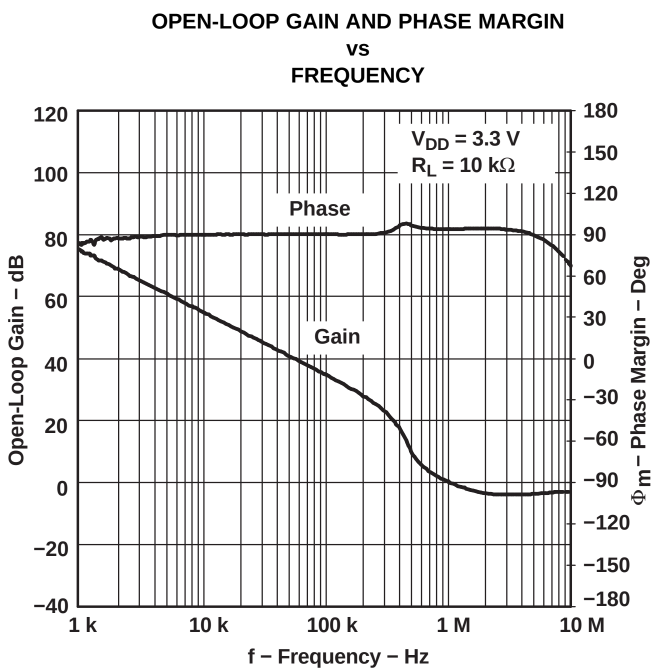

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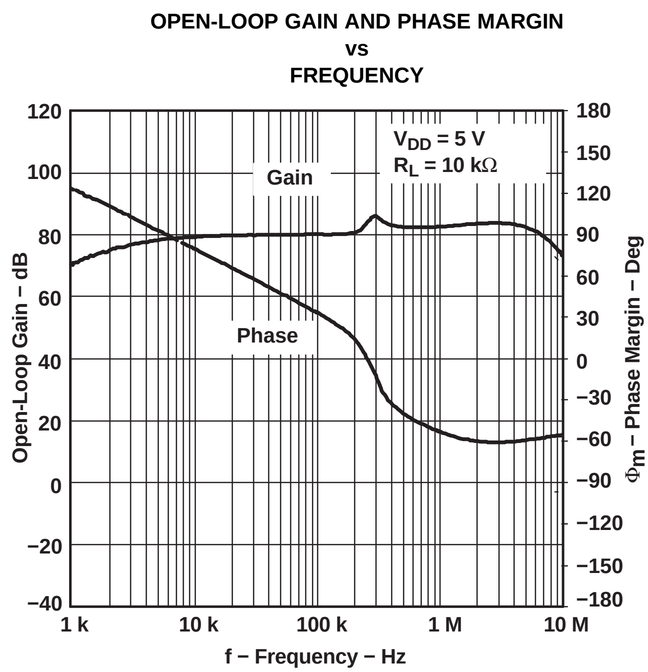


Figure 28.

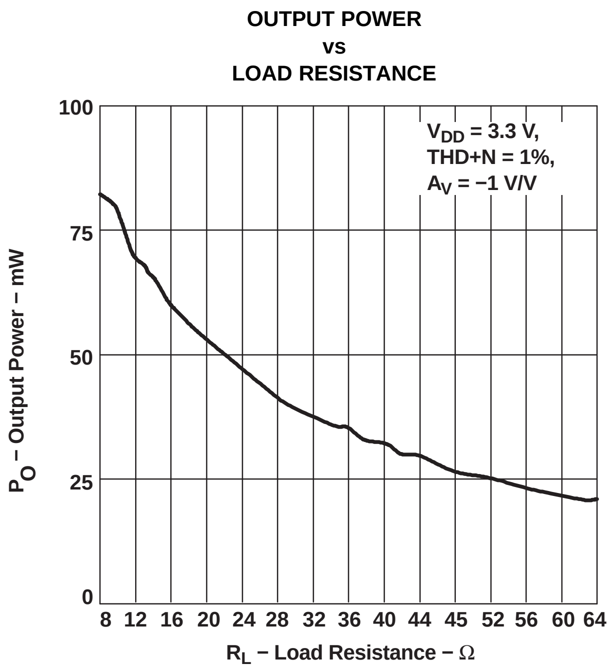
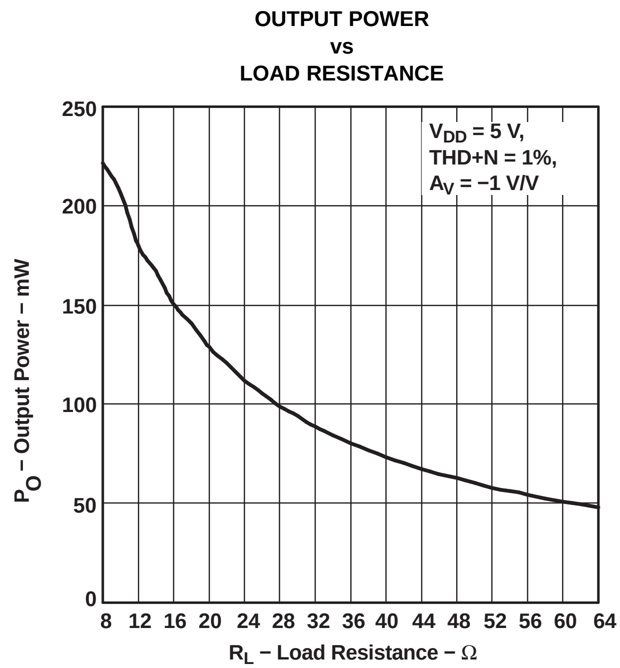


Figure 29.



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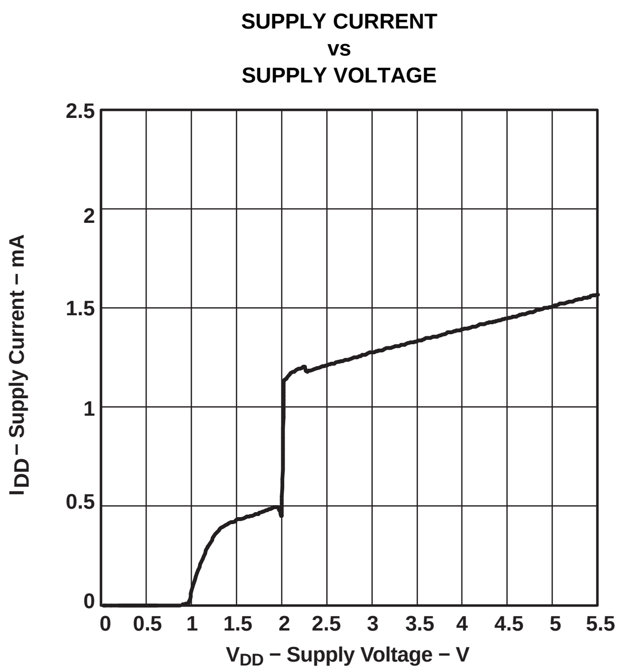

Figure 31.

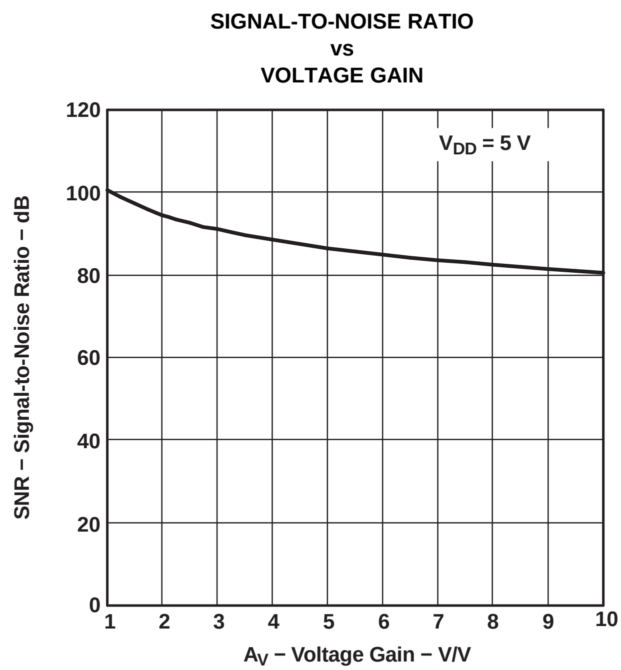

Figure 32.

POWER DISSIPATION/AMPLIFIER vs LOAD POWER

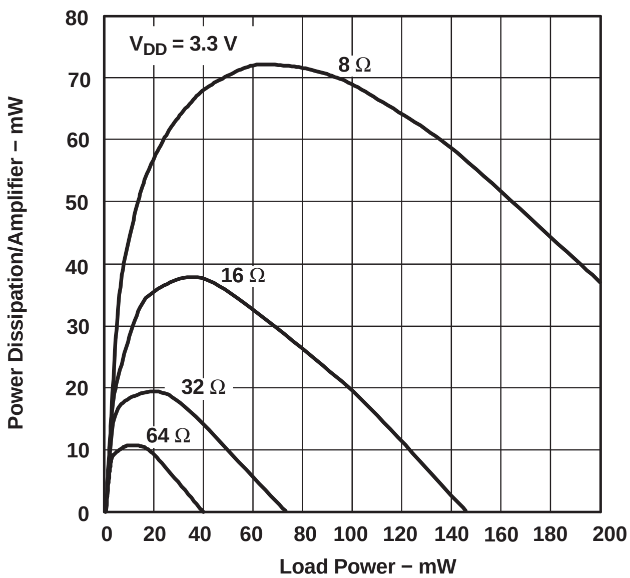

Figure 33.

POWER DISSIPATION/AMPLIFIER vs LOAD POWER

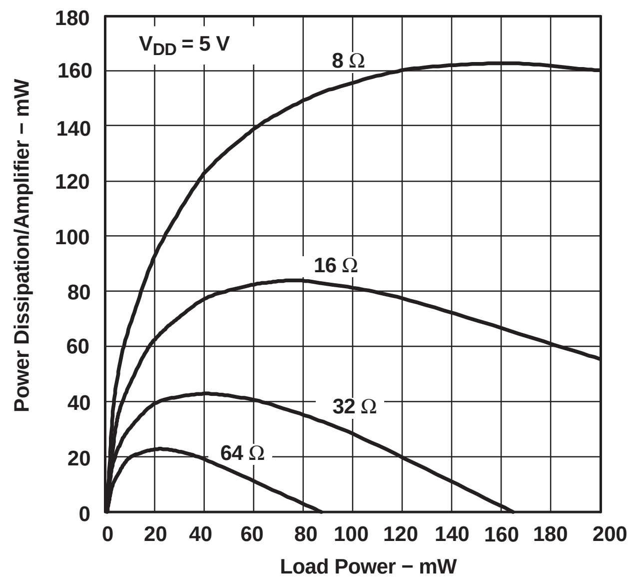

Figure 34.

APPLICATION INFORMATION

GAIN SETTING RESISTORS, R_f and R_i

The gain for the TPA6110A2 is set by resistors R_f and R_i according to Equation 1.

$$\text{Gain} = -\left(\frac{R_f}{R_i}\right) \quad (1)$$

Given that the TPA6110A2 is a MOS amplifier, the input impedance is very high. Consequently input leakage currents are not generally a concern. However, noise in the circuit increases as the value of R_f increases. In addition, a certain range of R_f values is required for proper start-up operation of the amplifier. Considering these factors, it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated using Equation 2.

$$\text{Effective Impedance} = \frac{R_f R_i}{R_f + R_i} \quad (2)$$

For example, if the input resistance is 20 kΩ and the feedback resistor is 20 kΩ, the gain of the amplifier is -1, and the effective impedance at the inverting terminal is 10 kΩ, a value within the recommended range.

For high performance applications, metal-film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_f above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_f and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_f. This, in effect, creates a low-pass filter network with the cutoff frequency defined by Equation 3.

$$f_{c(lowpass)} = \frac{1}{2\pi R_f C_F} \quad (3)$$

For example, if R_f is 100 kΩ and C_F is 5 pF then $f_{c(lowpass)}$ is 318 kHz, which is well outside the audio range.

INPUT CAPACITOR, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and R_i form a high-pass filter with the corner frequency determined in Equation 4.

$$f_{c(highpass)} = \frac{1}{2\pi R_i C_i} \quad (4)$$

The value of C_i directly affects the bass (low frequency) performance of the circuit. Consider the example where R_i is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as Equation 5.

$$C_i = \frac{1}{2\pi R_i f_{c(highpass)}} \quad (5)$$

In this example, C_i is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network formed by R_i, C_i, and the feedback resistor (R_f) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (gain >10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, connect the positive side of the capacitor to the amplifier input in most applications. The dc level there is held at $V_{DD}/2$—likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

POWER SUPPLY DECOUPLING, $C_{(S)}$

The TPA6110A2 is a high-performance CMOS audio amplifier that requires adequate power-supply decoupling to minimize the output total harmonic distortion (THD). Power-supply decoupling also prevents oscillations when long lead lengths are used between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, $C_{(B)}$

The midrail bypass capacitor, $C_{(B)}$, serves several important functions. During start up, $C_{(B)}$ determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 230-kΩ source inside the amplifier. To keep the start-up pop as low as possible, maintain the relationship shown in Equation 6.

$$\frac{1}{\left(C_{(B)} \times 230\ k\Omega\right)} \leq \frac{1}{\left(C_i R_i\right)} \tag{6}$$

Consider an example circuit where $C_{(B)}$ is 1 μF, C_i is 1 μF, and R_i is 20 kΩ. Subsitituting these values into the equation 9 results in: 6.25 ≤ 50 which satisfies the rule. Bypass capacitor, $C_{(B)}$, values of 0.1 μF to 1 μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

OUTPUT COUPLING CAPACITOR, $C_{(C)}$

In a typical single-supply, single-ended (SE) configuration, an output coupling capacitor ($C_{(C)}$) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 7.

$$f_c = \frac{1}{2\pi R_L C_{(C)}} \tag{7}$$

The main disadvantage, from a performance standpoint, is that the typically-small load impedance drives the low-frequency corner higher. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 68 μF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances vs Low-Frequency Output Characteristics in SE Mode

R_L	$C_{(C)}$	LOWEST FREQUENCY
32 Ω	68 μF	73 Hz
10,000 Ω	68 μF	0.23 Hz
47,000 Ω	68 μF	0.05 Hz

As Table 1 indicates, headphone response is adequate, and drive into line level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{\left(C_{(B)} \times 230\ k\Omega\right)} \leq \frac{1}{\left(C_i R_i\right)} \ll \frac{1}{R_L C_{(C)}} \tag{8}$$

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

5-V VERSUS 3.3-V OPERATION

The TPA6110A2 was designed for operation over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, since these are considered to be the two most common supply voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in theTPA6110A2 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion becomes significant.

REVISION HISTORY

Changes from Original (December 2000) to Revision A — Page

- Change the DC ELECTRICAL CHARACTERISTICS table From T_A = 25°C, V_{DD} = 3.3 V To: T_A = 25°C, V_{DD} = 2.5 V, updated values 3
- Change the DC ELECTRICAL CHARACTERISTICS table From T_A = 25°C, V_{DD} = 5 V To: T_A = 25°C, V_{DD} = 5.5 V, updated values 3
- Changed Figure 8, From: R_L = 8kΩ To: R_L = 8Ω 6
- Changed Figure 24, From: frequency limit at 1M To: frequency limit at 20K 10
- Changed Figure 25, From: frequency limit at 1M To: frequency limit at 20K 11

Changes from Revision A (September 2004) to Revision B — Page

- Changed the DC Electrical Characteristice (V_{DD} = 2.5V) for $I_{DD(SD)}$ From: Typ = 10 Max = 50 To: Typ = 1 Max = 10 3
- Changed the DC Electrical Characteristice (V_{DD} = 5.5V) for $I_{DD(SD)}$ From: Typ = 60 Max = 100 To: Typ = 1 Max = 10 3

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA6110A2DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIZ
TPA6110A2DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIZ
TPA6110A2DGNG4	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIZ
TPA6110A2DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIZ
TPA6110A2DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIZ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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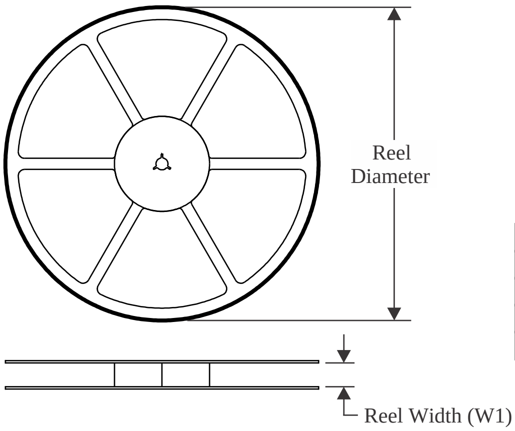
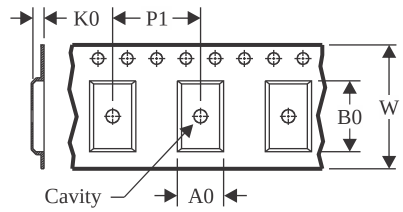
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

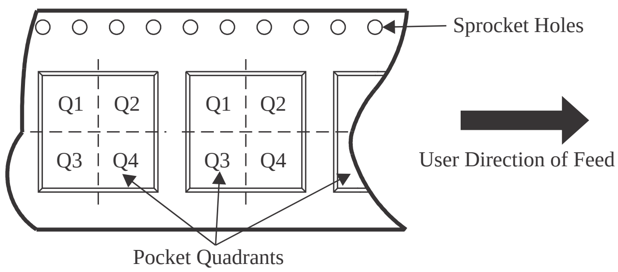


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

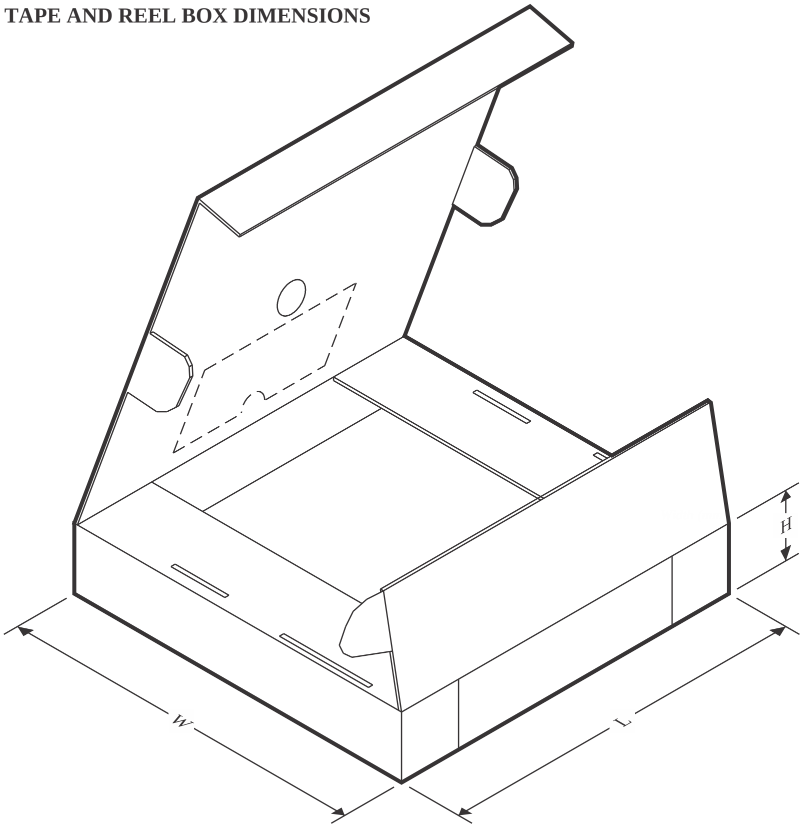
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6110A2DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6110A2DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

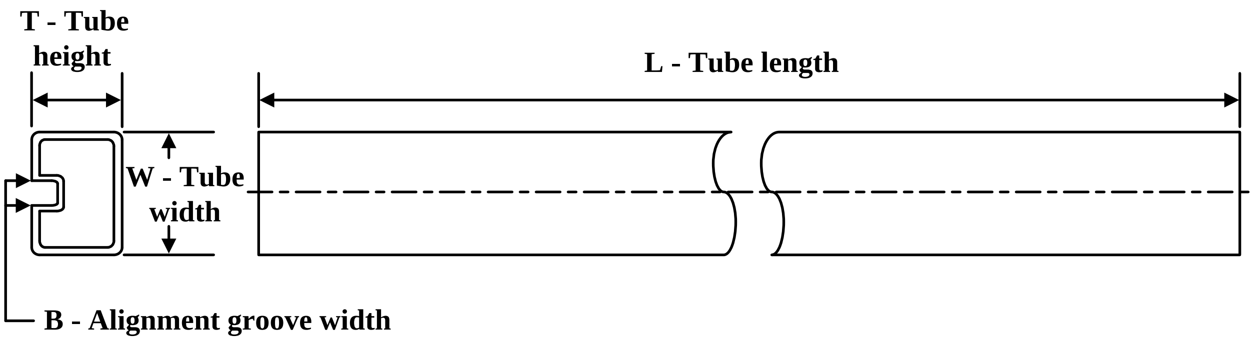
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6110A2DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPA6110A2DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0

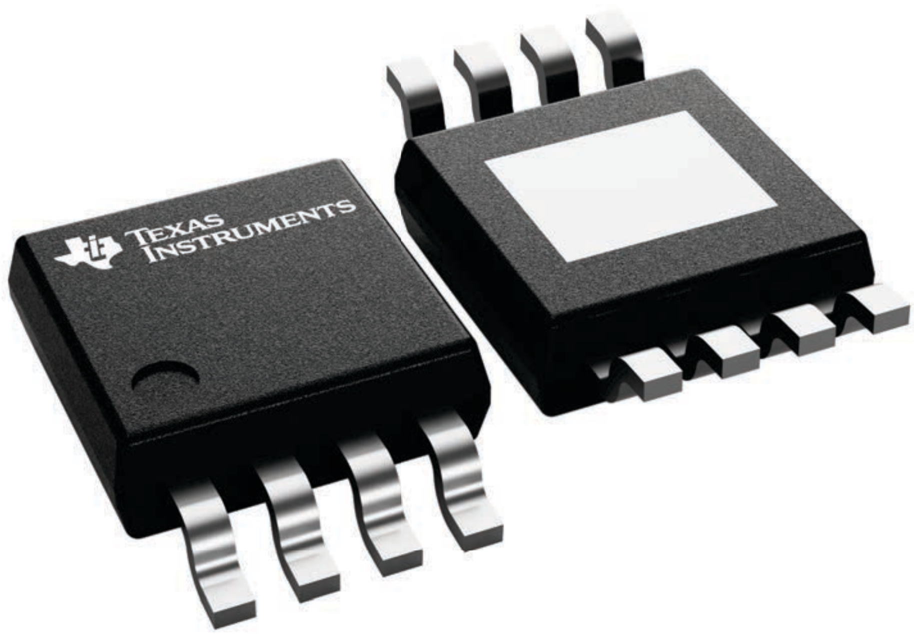
TUBE

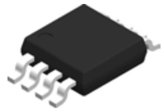


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA6110A2DGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPA6110A2DGN.A	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPA6110A2DGNG4	DGN	HVSSOP	8	80	330	6.55	500	2.88

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

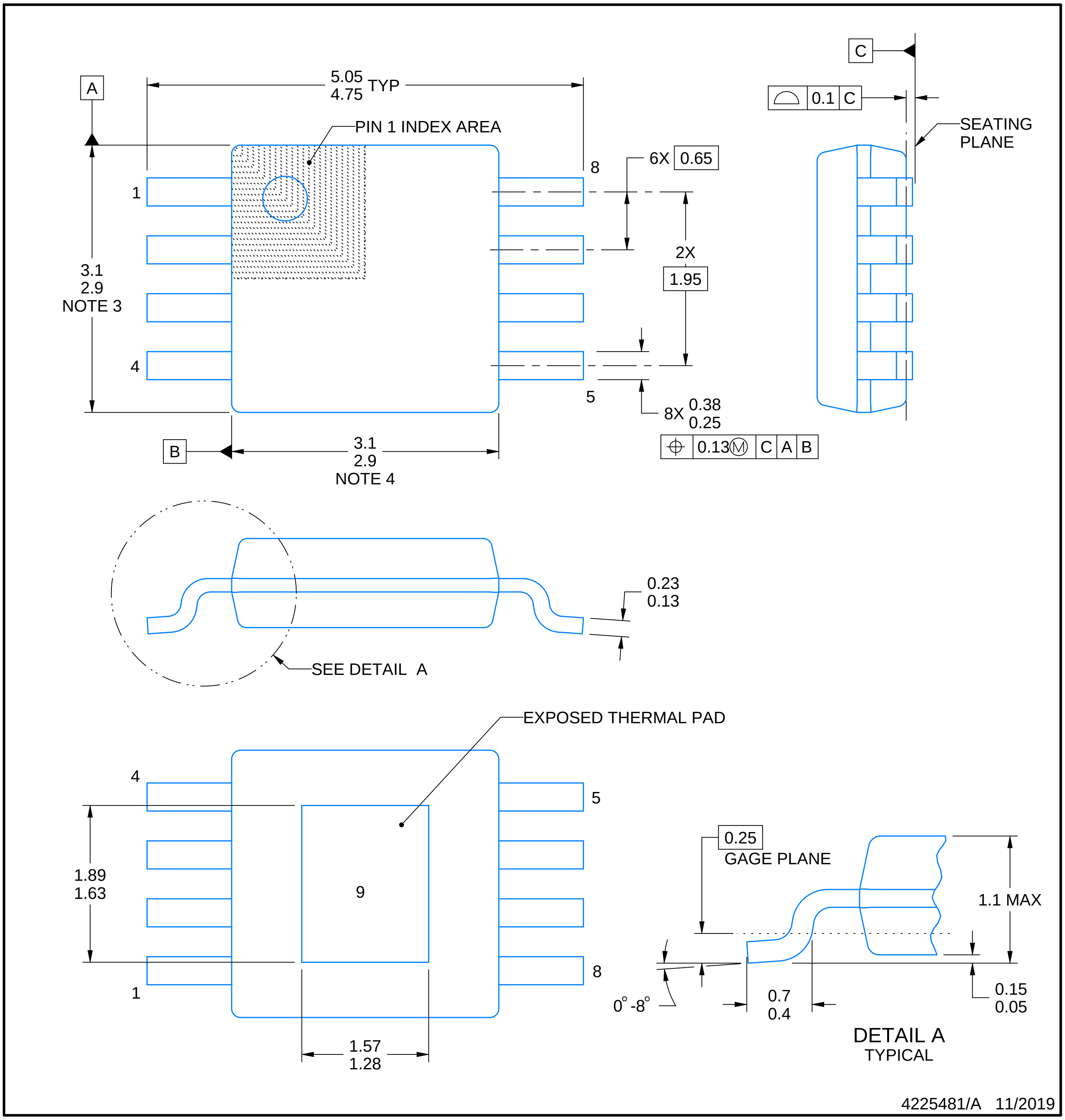




PACKAGE OUTLINE

PowerPAD™ VSSOP - 1.1 mm max height

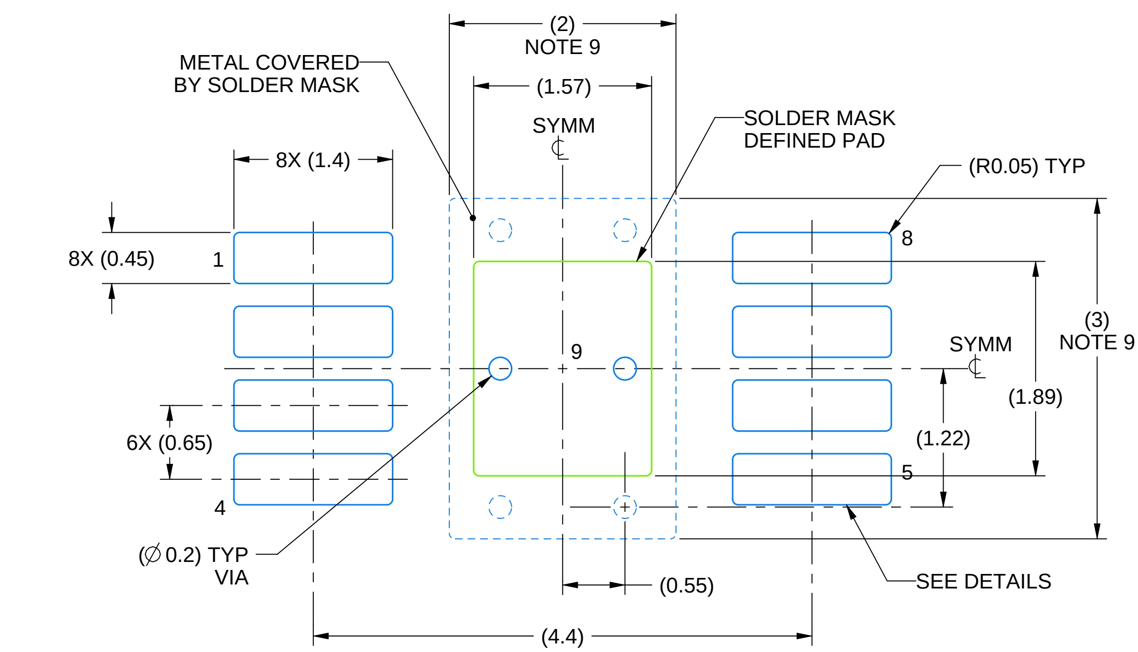
SMALL OUTLINE PACKAGE



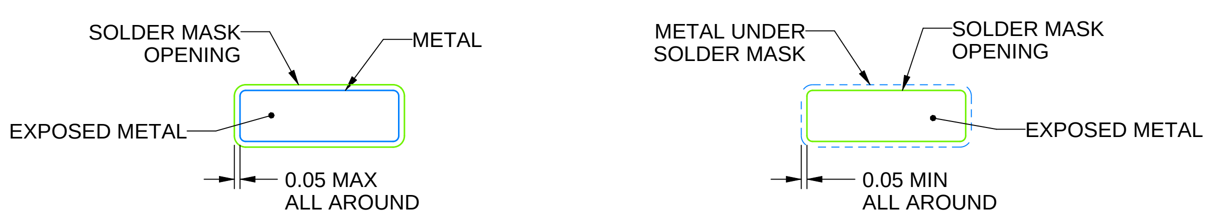
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

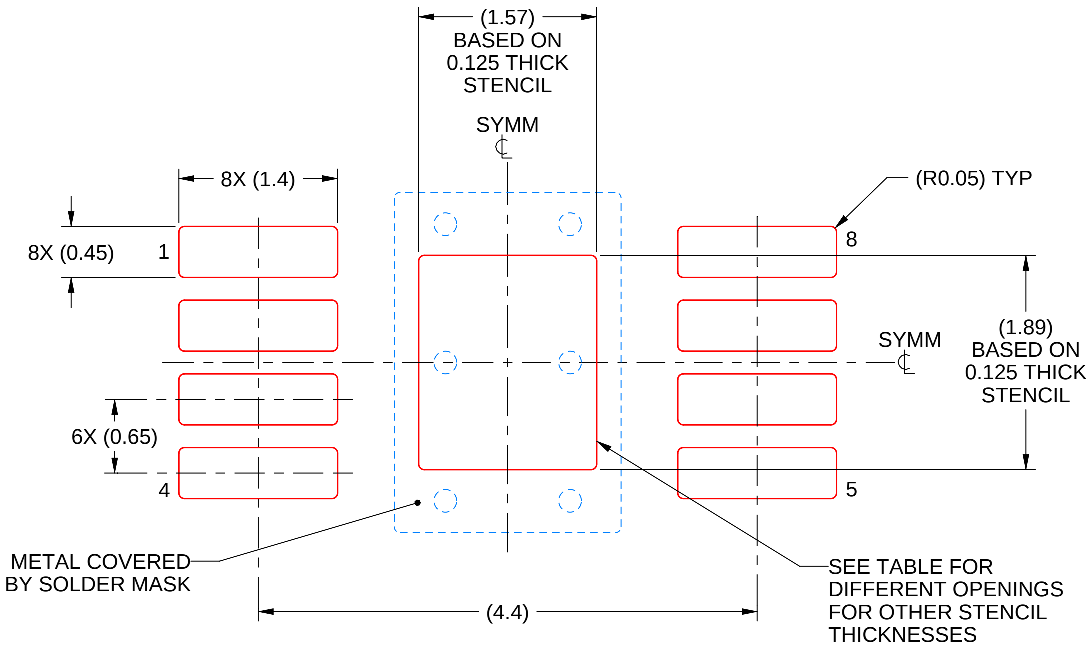
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

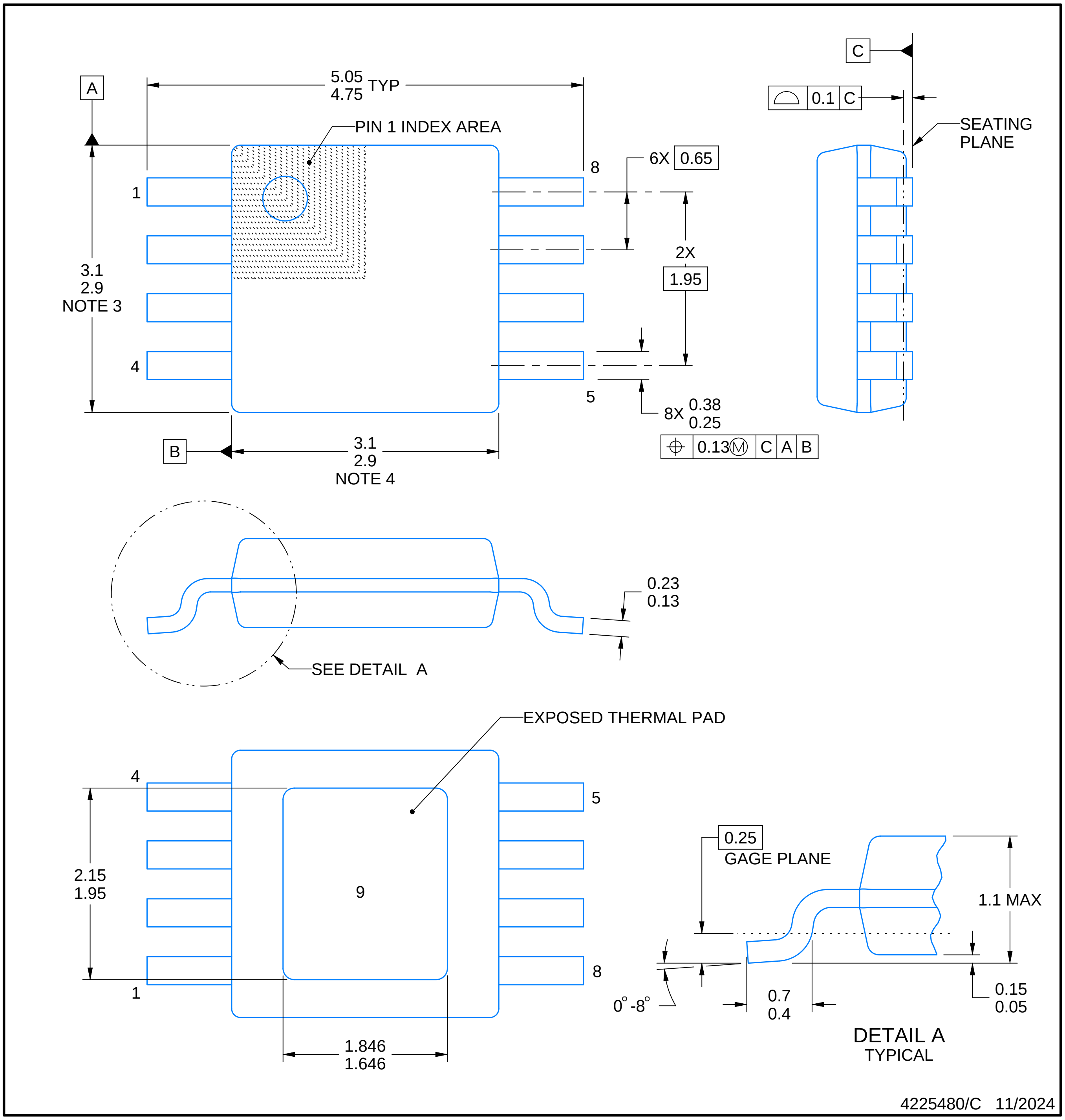
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

DGN0008G

PowerPAD™ HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

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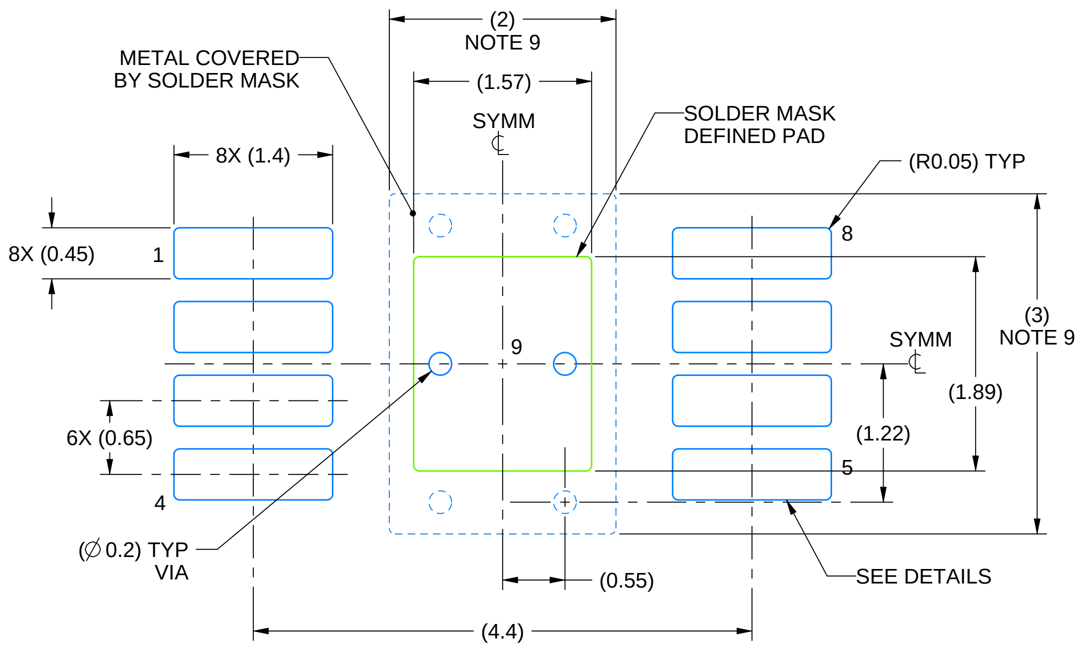
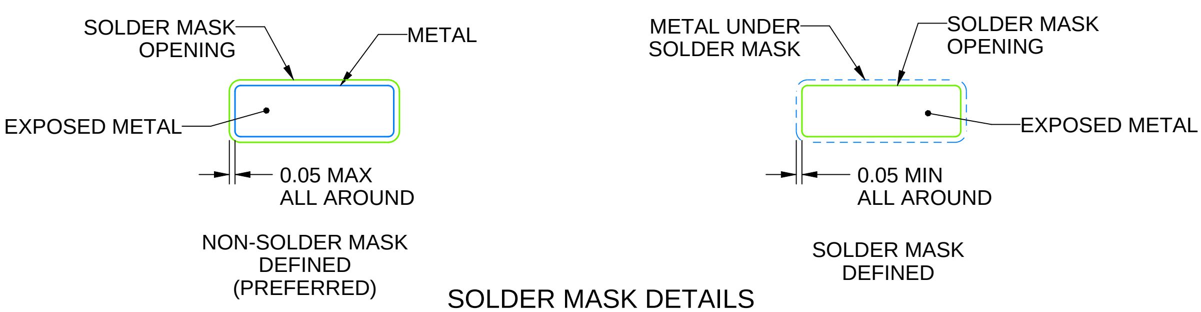


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

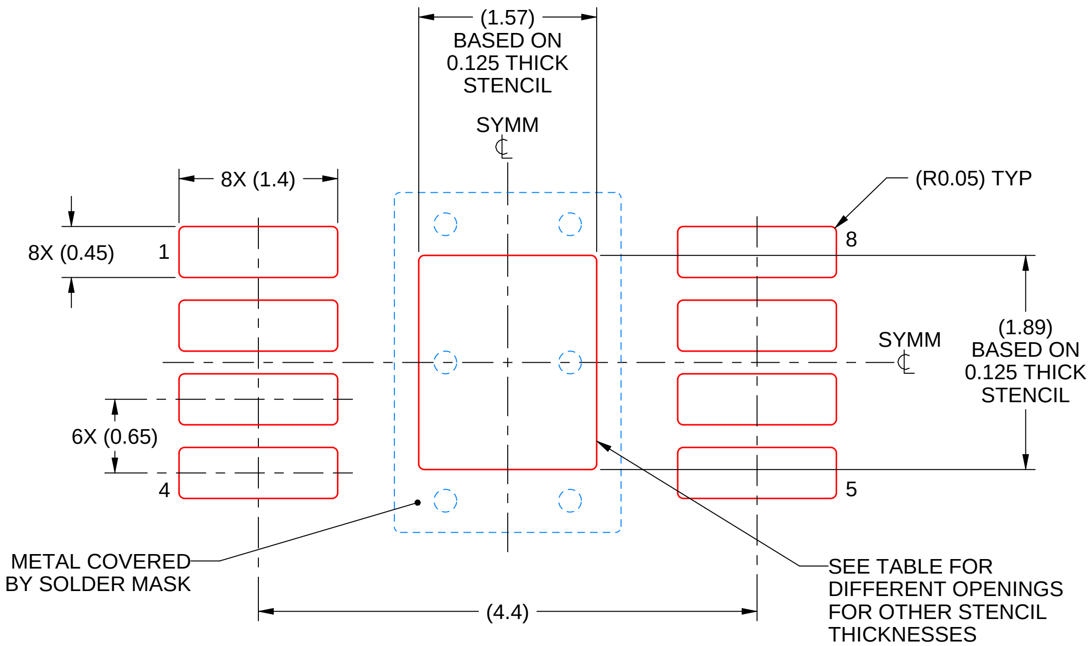


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C   11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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