

# TPD3S014-Q1 适用于汽车 USB 主机端口的限流开关和 D+/D- ESD 保护

## 1 特性

- 符合 AEC-Q100 标准 (2 级)
  - 环境温度范围: -40°C 至 +105°C
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 持续电流额定值为 0.5A
- 固定的恒流限值为 0.85A (典型值)
- 快速过流响应 - 2  $\mu$ s
- 集成输出放电
- 反向电流阻断
- 短路保护
- 带有自动重启的过热保护
- 内置软启动
- IEC 61000-4-2 4 级静电放电 (ESD) 保护 (外部引脚)
  - $\pm 12$ kV 接触放电 (IEC 61000-4-2)
  - $\pm 15$ kV 空气间隙放电 (IEC 61000-4-2)
- ISO 10605 330pF, 330 $\Omega$  ESD 保护 (外部引脚)
  - $\pm 8$ kV 接触放电
  - $\pm 15$ kV 气隙放电
- 6 引脚小外形尺寸晶体管 (SOT)-23 封装 (2.90mm  $\times$  1.60mm)

## 2 应用

- 终端设备:
  - 音响主机
  - 后座娱乐系统
  - 远程信息处理
  - USB 集线器
  - 导航模块
- 接口:
  - USB 2.0
  - USB 3.0

## 3 说明

TPD3S014-Q1 是一款集成器件, 具有一个限流负载开关和一个基于双通道瞬态电压抑制器 (TVS)、用于 USB 接口的静电放电 (ESD) 保护二极管阵列。

TPD3S014-Q1 器件适用于很可能出现大容量负载和短路情况的 USB 等应用, 可提供短路保护和过流保护。当输出负载超过电流限制阈值时, TPD3S014-Q1 通过在恒定电流模式下运行即可将输出电流限制到安全水平。快速过载响应特性有助于减轻 5V 主电源的负担, 当输出短路时可以快速调节电源。电流限制开关的上升和下降此时受到控制, 力求尽量减小器件开关过程中的浪涌电流。

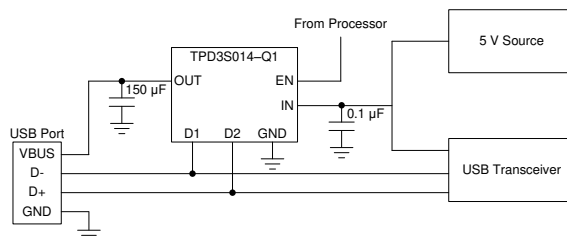
TPD3S014-Q1 支持 0.5A 的持续电流。TVS 二极管阵列的额定 ESD 冲击消散值高于 IEC 61000-4-2 国际标准中规定的最高水平。

此器件高度集成, 并且采用易于布线的 DBV 封装, 可对音响主机、USB 集线器和媒体接口等应用中的 USB 接口提供强力的电路保护。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TPD3S014-Q1	SOT-23 (6)	2.90mm $\times$ 1.60mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



Copyright © 2016, Texas Instruments Incorporated

简化版原理图



## Table of Contents

<b>1 特性</b> .....	1	8.2 Functional Block Diagram.....	11
<b>2 应用</b> .....	1	8.3 Feature Description.....	11
<b>3 说明</b> .....	1	8.4 Device Functional Modes.....	14
<b>4 Revision History</b> .....	2	<b>9 Application and Implementation</b> .....	15
<b>5 Pin Configuration and Functions</b> .....	3	9.1 Application Information.....	15
Pin Functions.....	3	9.2 Typical Application.....	15
<b>6 Specifications</b> .....	4	<b>10 Power Supply Recommendations</b> .....	18
6.1 Absolute Maximum Ratings.....	4	<b>11 Layout</b> .....	18
6.2 ESD Ratings—AEC Specification.....	4	11.1 Layout Guidelines.....	18
6.3 ESD Ratings—IEC Specification.....	4	11.2 Layout Example.....	18
6.4 ESD Ratings—ISO Specification.....	4	11.3 Power Dissipation and Junction Temperature.....	18
6.5 Recommended Operating Conditions.....	4	<b>12 Device and Documentation Support</b> .....	21
6.6 Thermal Information.....	5	12.1 Documentation Support.....	21
6.7 Electrical Characteristics: $T_J = T_A = 25^{\circ}\text{C}$ .....	5	12.2 支持资源.....	21
6.8 Electrical Characteristics: $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ .....	6	12.3 Trademarks.....	21
6.9 Typical Characteristics.....	7	12.4 静电放电警告.....	21
<b>7 Parameter Measurement Information</b> .....	10	12.5 术语表.....	21
<b>8 Detailed Description</b> .....	11	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	21
8.1 Overview.....	11		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision B (April 2016) to Revision C (August 2020)</b>	<b>Page</b>
• 向 <a href="#">特性</a> 部分添加了功能安全链接.....	1
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
<b>Changes from Revision A (April 2016) to Revision B (April 2016)</b>	<b>Page</b>
• 更改了 <a href="#">电气特性</a> ： $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ 表将 $T_A$ 从 $125^{\circ}\text{C}$ 更改为 $105^{\circ}\text{C}$ .....	1
• 将 <a href="#">功率耗散和结温</a> 部分中的温度从 $125^{\circ}\text{C}$ 更改为 $105^{\circ}\text{C}$ .....	1
<b>Changes from Revision * (March 2016) to Revision A (April 2016)</b>	<b>Page</b>
• 将器件状态从 <a href="#">产品预发布</a> 更改为 <a href="#">量产数据</a> .....	1

## 5 Pin Configuration and Functions

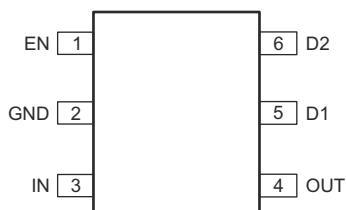


图 5-1. DBV Package 6-Pin SOT-23 Top View

### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
D1	5	I/O	USB data+ or USB data -
D2	6		
EN	1	I	Enable input, logic high turns on power switch
GND	2	—	Ground
IN	3	I	Input voltage and power-switch drain; Connect a 0.1-μF or greater ceramic capacitor from IN to GND close to the IC
OUT	4	O	Power-switch output, connect to load

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
Input voltage <sup>(3)</sup>	V <sub>IN</sub>	– 0.3	6	V
	V <sub>OUT</sub>	– 0.3	6	
	EN	– 0.3	6	
	D1	– 0.3	6	
	D2	– 0.3	6	
Voltage from V <sub>IN</sub> to V <sub>OUT</sub>		– 6	6	V
Junction temperature	T <sub>J</sub>	Internally limited		
Storage temperature	T <sub>stg</sub>	– 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Voltages are with respect to GND unless otherwise noted.
- (3) See the [Input and Output Capacitance](#) section.

### 6.2 ESD Ratings—AEC Specification

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per AEC Q100-011	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	IEC 61000-4-2, V <sub>OUT</sub> , Dx pins	Contact discharge <sup>(1)</sup>	±12000	V
		Air-gap discharge <sup>(1)</sup>	±15000	

- (1) V<sub>OUT</sub> was tested on a PCB with input and output bypassing capacitors of 0.1 μF and 120 μF, respectively.

### 6.4 ESD Ratings—ISO Specification

			VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	ISO 10605 330 pF, 330 Ω, V <sub>OUT</sub> , Dx pins	Contact discharge <sup>(1)</sup>	±8000	V
		Air-gap discharge <sup>(1)</sup>	±15000	

- (1) V<sub>OUT</sub> was tested on a PCB with input and output bypassing capacitors of 0.1 μF and 120 μF, respectively.

### 6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	4.5	5.5	V
V <sub>EN</sub>	Input voltage, EN	0	5.5	V
V <sub>IH</sub>	High-level Input voltage, EN	2		V
V <sub>IL</sub>	Low-level Input voltage, EN		0.7	V
C <sub>IN</sub>	Input decoupling capacitance, IN to GND	0.1		μF
I <sub>OUT</sub> <sup>(1)</sup>	Continuous output current (TPD3S014-Q1)		0.5	A
T <sub>J</sub>	Operating junction temperature	– 40	125	°C

- (1) Package and current ratings may require an ambient temperature derating of 85°C

## 6.6 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPD3S014-Q1	UNIT
		DBV (SOT-23)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.0	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	23.7	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	31.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W
$R_{\theta JA}$ (Custom)	See the <a href="#">Power Dissipation and Junction Temperature</a> section	120.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.7 Electrical Characteristics: $T_J = T_A = 25^\circ\text{C}$

$V_{IN} = 5\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 0\text{ A}$  (unless otherwise noted). Parameters over a wider operational range are shown in [Electrical Characteristics:  \$-40^\circ\text{C} \leq T\_A \leq 105^\circ\text{C}\$](#)  table.

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
POWER SWITCH						
R <sub>DS(on)</sub>	Input - Output resistance			97	120	m Ω
		- 40°C ≤ (T <sub>J</sub> , T <sub>A</sub> ) ≤ +85°C		97	140	
CURRENT LIMIT						
I <sub>OS</sub> <sup>(2)</sup>	Current limit, see 图 8-3		0.67	0.85	1.01	A
SUPPLY CURRENT						
I <sub>SD</sub>	Supply current, switch disabled	I <sub>OUT</sub> = 0 A		0.02	1	μA
		- 40°C ≤ (T <sub>J</sub> , T <sub>A</sub> ) ≤ +85°C, V <sub>IN</sub> = 5.5 V, I <sub>OUT</sub> = 0 A			2	
I <sub>SE</sub>	Supply current, switch enabled	I <sub>OUT</sub> = 0 A		66	74	μA
		- 40°C ≤ (T <sub>J</sub> , T <sub>A</sub> ) ≤ +85°C, V <sub>IN</sub> = 5.5 V, I <sub>OUT</sub> = 0 A			85	
I <sub>REV</sub>	Reverse leakage current	V <sub>OUT</sub> = 5 V, V <sub>IN</sub> = 0 V, Measure I <sub>VOUT</sub>		0.2	1	μA
		- 40°C ≤ (T <sub>J</sub> , T <sub>A</sub> ) ≤ +85°C, V <sub>OUT</sub> = 5 V, V <sub>IN</sub> = 0 V, Measure I <sub>VOUT</sub>			5	
OUTPUT DISCHARGE						
R <sub>PD</sub>	Output pull-down resistance <sup>(3)</sup>	V <sub>IN</sub> = V <sub>OUT</sub> = 5 V, disabled	400	456	600	Ω
ESD PROTECTION						
Δ C <sub>IO</sub>	Differential capacitance between the D1, D2 lines	f = 1 MHz, V <sub>IO</sub> = 2.5 V		0.02		pF
C <sub>IO</sub>	(D1, D2 to GND)	f = 1 MHz, V <sub>IO</sub> = 2.5 V		1.4		pF
R <sub>DYN</sub>	Dynamic on-resistance D1, D2 IEC clamps <sup>(4)</sup>	Dx to GND		0.2		Ω
		GND to Dx		0.2		Ω

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature

(2) See the [Current Limit](#) for explanation of this parameter.

(3) These Parameters are provided for reference only, and do not constitute a part of TI's published device specifications for purposes of TI's product warranty.

(4) RDYN was extracted using the least squares first of the TLP characteristics between  $I = 20\text{ A}$  and  $I = 30\text{ A}$ .

## 6.8 Electrical Characteristics: $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$

$4.5\text{ V} \leq V_{\text{IN}} \leq 5.5\text{ V}$ ,  $V_{\text{EN}} = V_{\text{IN}}$ ,  $I_{\text{OUT}} = 0\text{ A}$ , typical values are at  $5\text{ V}$  and  $25^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
POWER SWITCH						
R <sub>DS(on)</sub>	Input – output resistance			97	164	m Ω
ENABLE INPUT (EN)						
	Threshold	Input rising	1	1.45	2	V
	Hysteresis			0.13		V
	Leakage current	V <sub>EN</sub> = 0 V	– 1	0	1	μA
t <sub>ON</sub>	Turnon time	V <sub>IN</sub> = 5 V, C <sub>L</sub> = 1 μF, R <sub>L</sub> = 100 Ω, EN ↑ See 图 8-2	1	1.6	2.2	ms
t <sub>OFF</sub>	Turnoff time	V <sub>IN</sub> = 5 V, C <sub>L</sub> = 1 μF, R <sub>L</sub> = 100 Ω, EN ↓ See 图 8-2	1.7	2.1	2.7	ms
t <sub>R</sub>	Rise time, output	C <sub>L</sub> = 1 μF, R <sub>L</sub> = 100 Ω, V <sub>IN</sub> = 5 V, See 图 8-1	0.4	0.64	0.9	ms
t <sub>F</sub>	Fall time, output	C <sub>L</sub> = 1 μF, R <sub>L</sub> = 100 Ω, V <sub>IN</sub> = 5 V, See 图 8-1	0.25	0.4	0.8	ms
CURRENT LIMIT						
I <sub>OS</sub> <sup>(2)</sup>	Current limit, see 图 8-3		0.65	0.85	1.05	A
t <sub>IOS</sub>	Short-circuit response time <sup>(2)</sup>	V <sub>IN</sub> = 5 V (see 图 8-3) One Half full load → R <sub>SHORT</sub> = 50 m Ω Measure from application to when current falls below 120% of final value		2		μs
SUPPLY CURRENT						
I <sub>SD</sub>	Supply current, switch disabled	I <sub>OUT</sub> = 0 A		0.02	10	μA
I <sub>SE</sub>	Supply current, switch enabled	I <sub>OUT</sub> = 0 A		66	94	μA
I <sub>REV</sub>	Reverse leakage current	V <sub>OUT</sub> = 5.5 V, V <sub>IN</sub> = 0 V, Measure I <sub>VOUT</sub>		0.2	20	μA
UNDERVOLTAGE LOCKOUT						
V <sub>UVLO</sub>	Rising threshold	V <sub>IN</sub> ↑	3.5	3.77	4	V
	Hysteresis	V <sub>IN</sub> ↓		0.14		V
OUTPUT DISCHARGE						
R <sub>PD</sub>	Output pull-down resistance	V <sub>IN</sub> = 4 V, V <sub>OUT</sub> = 5 V, Disabled	350	545	1200	Ω
		V <sub>IN</sub> = 5 V, V <sub>OUT</sub> = 5 V, Disabled	300	456	800	
THERMAL SHUTDOWN						
T <sub>SHDN</sub>	Rising threshold (T <sub>J</sub> )	In current limit	135			°C
		Not in current limit	155			
	Hysteresis <sup>(3)</sup>			20		°C
ESD PROTECTION						
I <sub>I</sub>	Input leakage current (D1, D2)	V <sub>I</sub> = 3.3 V		0.02	1	μA
V <sub>D</sub>	Diode forward voltage (D1, D2); Lower clamp diode	I <sub>O</sub> = 8 mA			0.95	V
V <sub>BR</sub>	Breakdown voltage (D1, D2)	I <sub>BR</sub> = 1 mA	6			V

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature

(2) See the [Current Limit](#) section for explanation of this parameter.

(3) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

## 6.9 Typical Characteristics

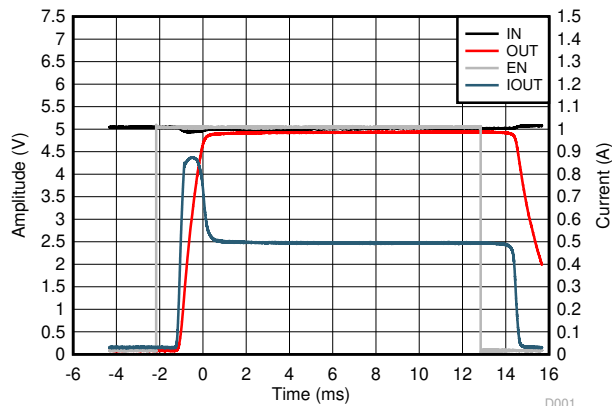


图 6-1. Turn ON into 10 Ω

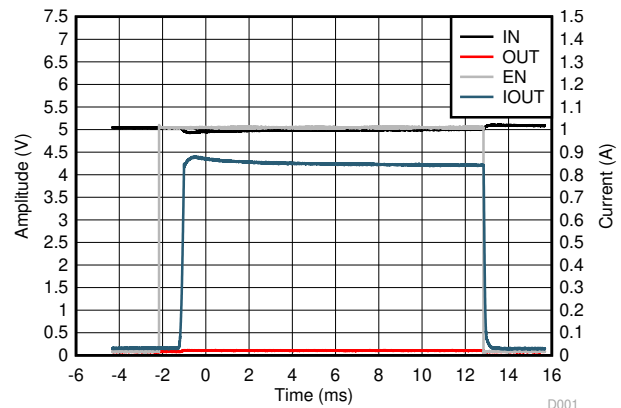


图 6-2. Enable into Short

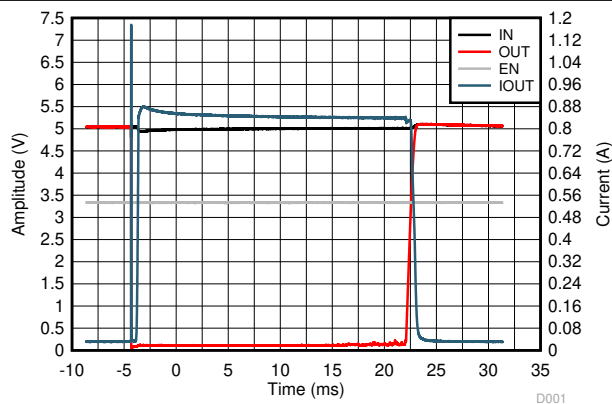


图 6-3. Pulsed Output Short

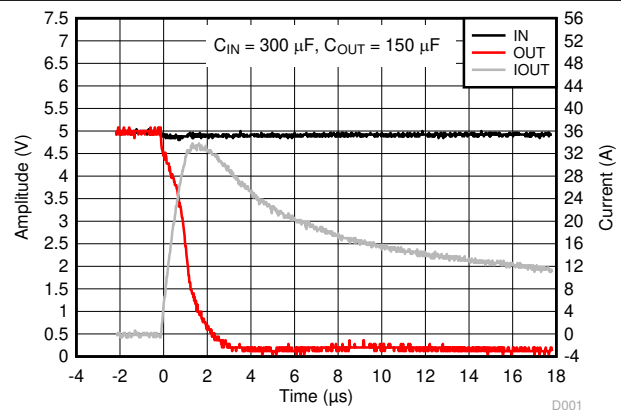


图 6-4. Short Applied

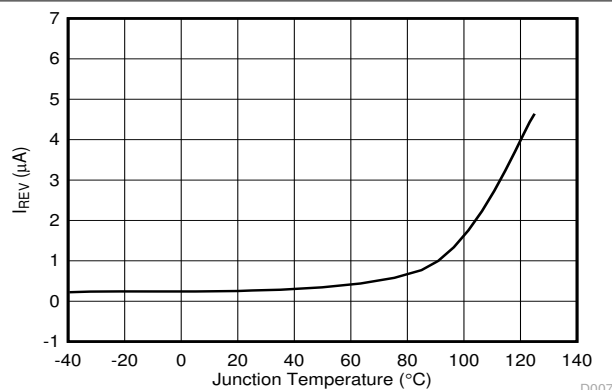


图 6-5. Reverse Leakage Current ( $I_{REV}$ ) vs Temperature

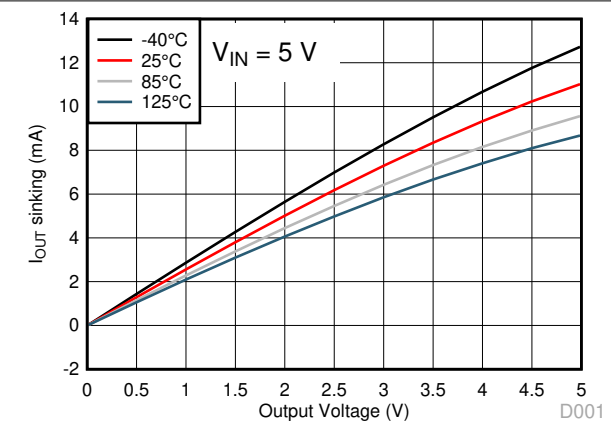
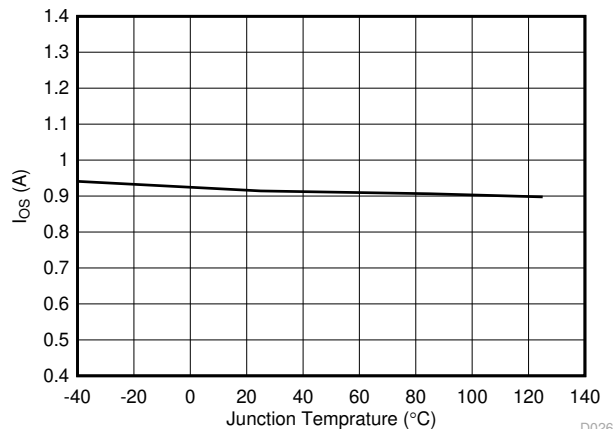
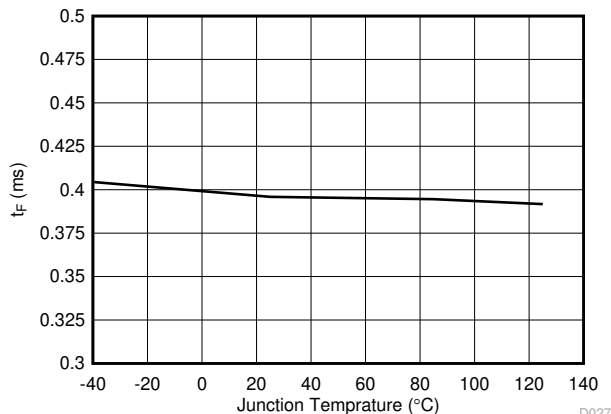
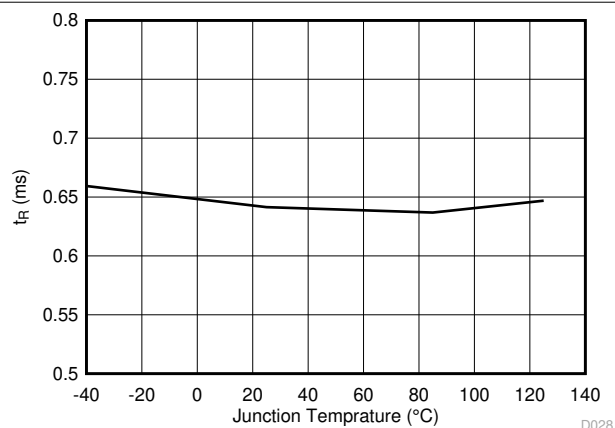
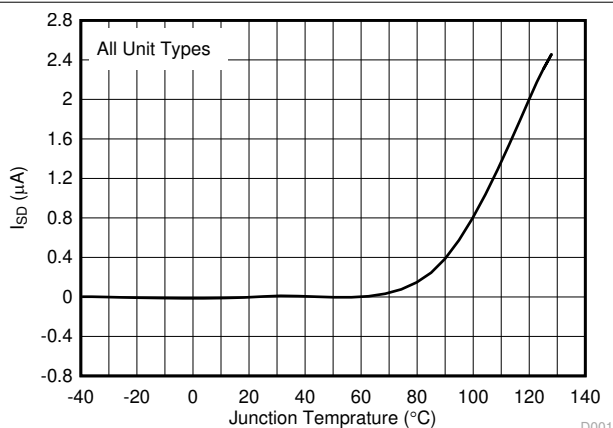
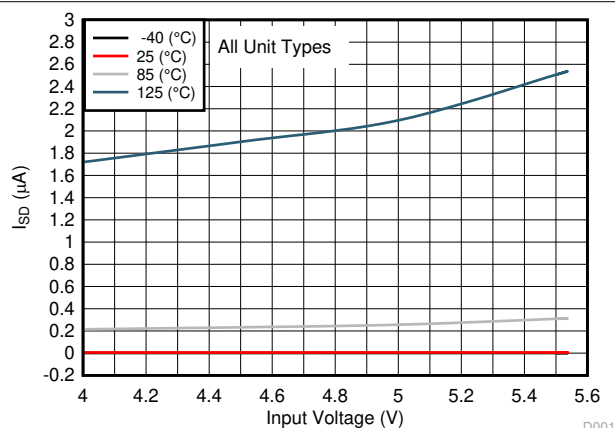
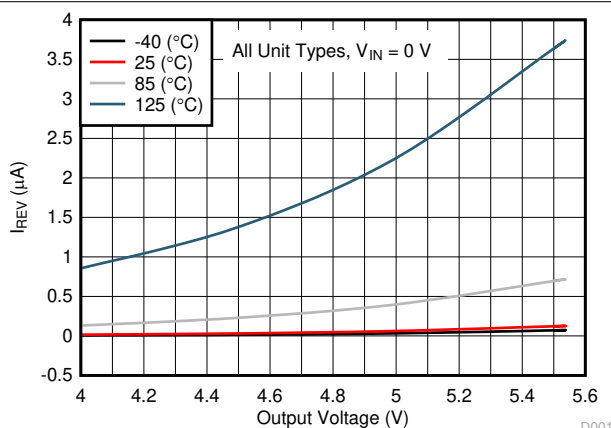


图 6-6. Output Discharge Current vs Output Voltage

图 6-7. Short Circuit Current ( $I_{OS}$ ) vs Temperature图 6-8. Output Fall Time ( $t_F$ ) vs Temperature图 6-9. Output Rise Time ( $t_R$ ) vs Temperature图 6-10. Disabled Supply Current ( $I_{SD}$ ) vs Temperature图 6-11. Disabled Supply Current ( $I_{SD}$ ) vs Input Voltage图 6-12. Reverse Leakage Current ( $I_{REV}$ ) vs Output Voltage



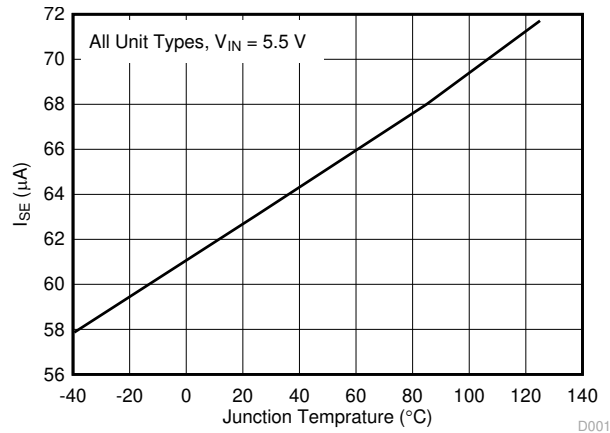


图 6-13. Enabled Supply Current ( $I_{SE}$ ) vs Temperature

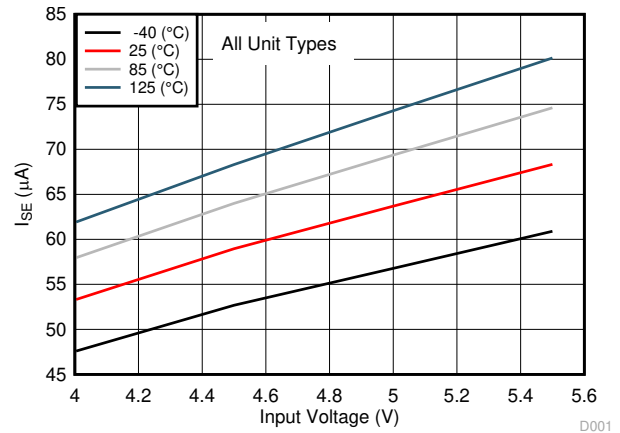


图 6-14. Enabled Supply Current ( $I_{SE}$ ) vs Input Voltage

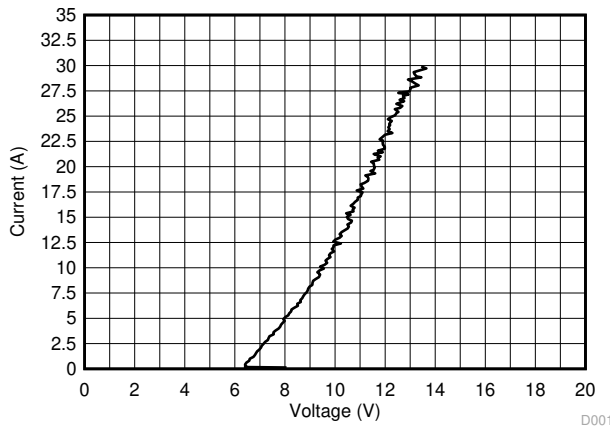


图 6-15. D1/D2 Positive TLP Curve

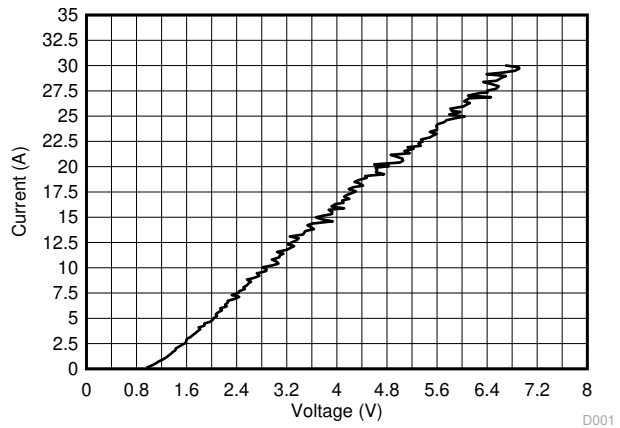


图 6-16. D1/D2 Negative TLP Curve

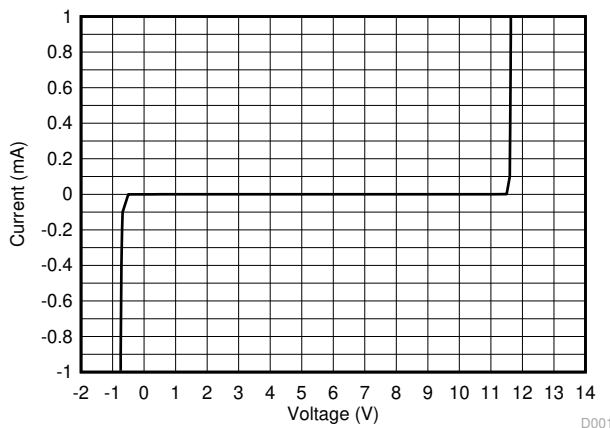


图 6-17. D1/D2 I-V Curve

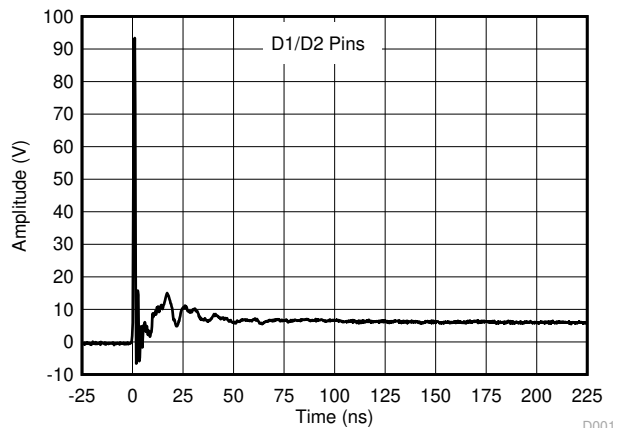


图 6-18. D1/D2 IEC 61000-4-2 8-kV Contact

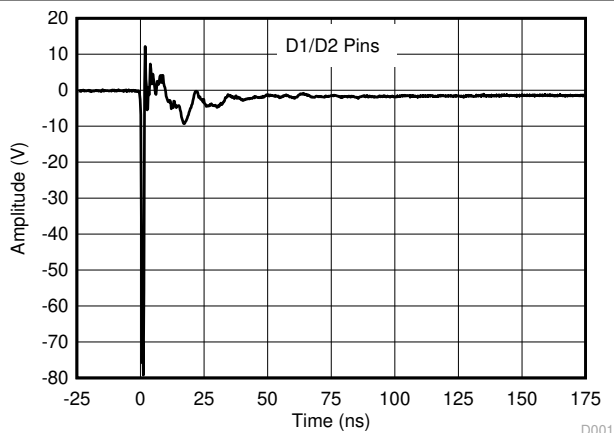
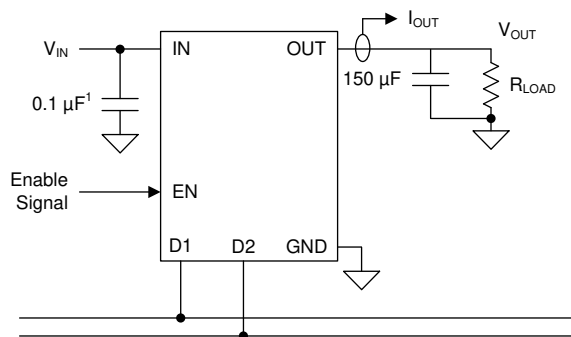


图 6-19. D1/D2 IEC 61000-4-2 - 8-kV Contact

## 7 Parameter Measurement Information



Copyright © 2016, Texas Instruments Incorporated

- A. During the short applied tests, 300  $\mu\text{F}$  is used because of the use of an external supply.

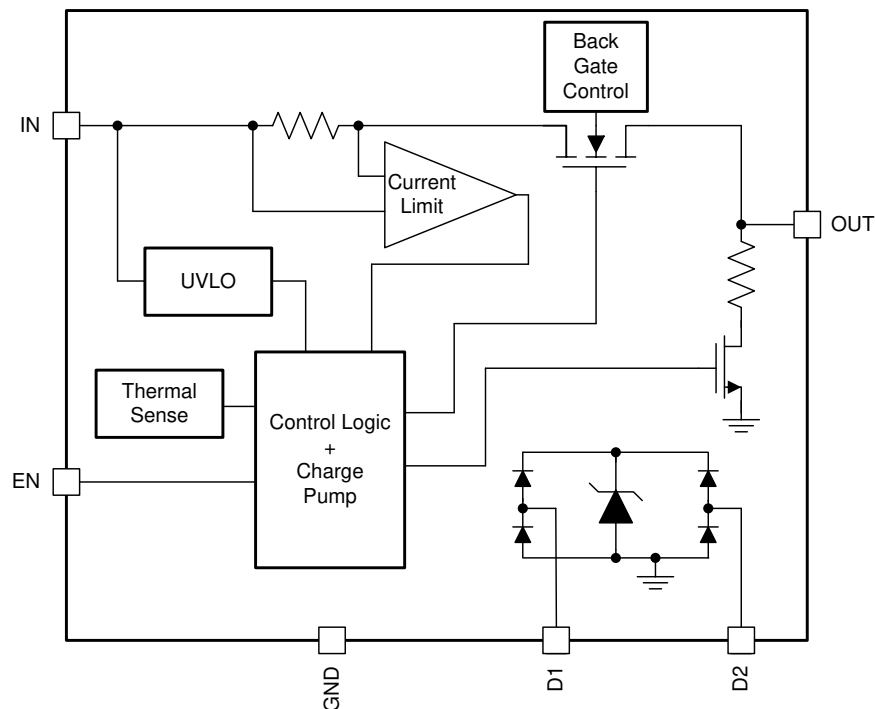
图 7-1. Test Circuit for System Operation

## 8 Detailed Description

### 8.1 Overview

The TPD3S014-Q1 is a highly integrated device that features a current limited load switch and a two-channel TVS based ESD protection diode array for USB interfaces. The TPD3S014-Q1 provides 0.5 A of continuous load current in 5 V circuits. This part uses N-channel MOSFETs for low resistance, maintaining voltage regulation to the load. It is designed for applications where short circuits or heavy capacitive loads will be encountered. Device features include enable, reverse blocking when disabled, output discharge pull-down, over-current protection, and over-temperature protection. Finally, with two channels of TVS ESD protection diodes integrated, the TPD3S014-Q1 provides system level ESD protection to all the pins of the USB port.

### 8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

### 8.3 Feature Description

#### 8.3.1 Undervoltage Lockout (UVLO)

The UVLO circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted on and off cycling because of input voltage drop from large current surges.

#### 8.3.2 Enable

The logic enable input (EN) controls the power switch, bias for the charge pump, driver, and other circuits. The supply current is reduced to less than 1  $\mu$ A when the TPD3S014-Q1 is disabled. The enable input is compatible with both TTL and CMOS logic levels.

The turnon and turnoff times ( $t_{ON}$ ,  $t_{OFF}$ ) are composed of a delay and a rise or fall time ( $t_R$ ,  $t_F$ ). The delay times are internally controlled. The rise time is controlled by both the TPD3S014-Q1 and the external loading (especially capacitance). The TPD3S014-Q1 fall time is controlled by the loading (R and C), and the output discharge ( $R_{PD}$ ). An output load consisting of only a resistor experiences a fall time set by the TPD3S014-Q1. An output load with parallel R and C elements experiences a fall time determined by the ( $R \times C$ ) time constant if it is longer than the TPD3S014-Q1  $t_F$ . See [Figure 8-1](#) and [Figure 8-2](#) showing  $t_R$ ,  $t_F$ ,  $t_{ON}$ , and  $t_{OFF}$ . The enable must not be left open; it may be tied to  $V_{IN}$ .

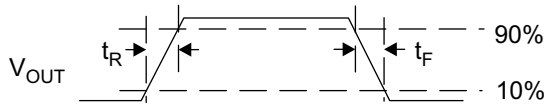


图 8-1. Power-On and Power-Off Timing

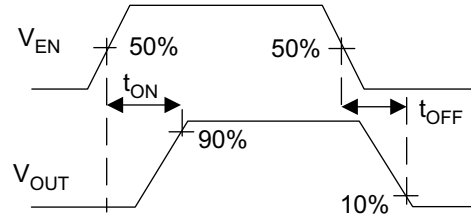


图 8-2. Enable Timing, Active-High Enable

### 8.3.3 Internal Charge Pump

The TPD3S014-Q1 incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the gate driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start functionality. The MOSFET power switch blocks current from OUT to IN when turned off by the UVLO or disabled.

### 8.3.4 Current Limit

The TPD3S014-Q1 responds to overloads by limiting output current to the static current-limit ( $I_{OS}$ ) levels shown in the [Electrical Characteristics:  \$T\_J = T\_A = 25^\circ\text{C}\$](#)  table. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by ( $I_{OS} \times R_{LOAD}$ ). Two possible overload conditions can occur.

The first overload condition occurs when either:

1. The input voltage is first applied, enable is true, and a short circuit is present (load which draws  $I_{OUT} > I_{OS}$ ) or
2. The input voltage is present and the TPD3S014-Q1 is enabled into a short circuit.

The output voltage is held near zero potential with respect to ground and the TPD3S014-Q1 ramps the output current to  $I_{OS}$ . The TPD3S014-Q1 limits the current to  $I_{OS}$  until the overload condition is removed or the device begins to thermal cycle. The device subsequently cycles current off and on as the thermal protection engages.

The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within  $t_{IOS}$  when the specified overload (per [Electrical Characteristics:  \$T\_J = T\_A = 25^\circ\text{C}\$](#) , [Electrical Characteristics:  \$-40^\circ\text{C} \leq T\_A \leq 105^\circ\text{C}\$](#)  tables) is applied (See 图 8-3 and 图 8-4). The response speed and shape varies with the overload level, input circuit, and rate of application. The current-limit response varies between simply settling to  $I_{OS}$ , or turnoff and controlled return to  $I_{OS}$ . Similar to the previous case, the TPD3S014-Q1 limits the current to  $I_{OS}$  until the overload condition is removed or the device begins to thermal cycle.

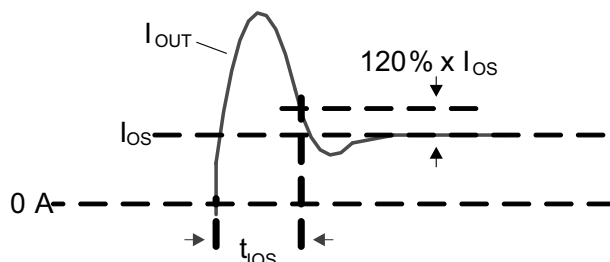


图 8-3. Output Short Circuit Parameters

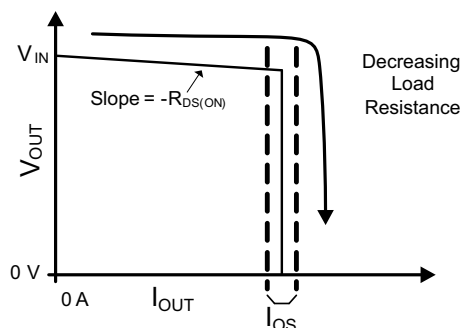


图 8-4. Output Characteristic Showing Current Limit

The TPD3S014-Q1 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the cases shown in 图 8-3 and 图 8-4. This is because of the relatively large power dissipation  $[(V_{IN} - V_{OUT}) \times I_{OS}]$  driving the junction temperature up. The devices turn off when the junction temperature exceeds 135°C (minimum) while in current limit. The devices remains off until the junction temperature cools down to 20°C and then restarts.

There are two kinds of current limit profiles typically available in TI switch products similar to the TPD3S014-Q1. Many older designs have an output I vs V characteristic similar to the plot labeled "Current Limit with Peaking" in 图 8-5. This type of limiting can be characterized by two parameters, the current limit corner ( $I_{OC}$ ), and the short circuit current ( $I_{OS}$ ).  $I_{OC}$  is often specified as a maximum value. The TPD3S014-Q1 part does not present noticeable peaking in the current limit, corresponding to the characteristic labeled "Flat Current Limit" in 图 8-5. This is why the  $I_{OC}$  parameter is not present in the [Electrical Characteristics:  \$T\_J = T\_A = 25^\circ\text{C}\$](#) , [Electrical Characteristics:  \$-40^\circ\text{C} \leq T\_A \leq 105^\circ\text{C}\$](#)  tables.

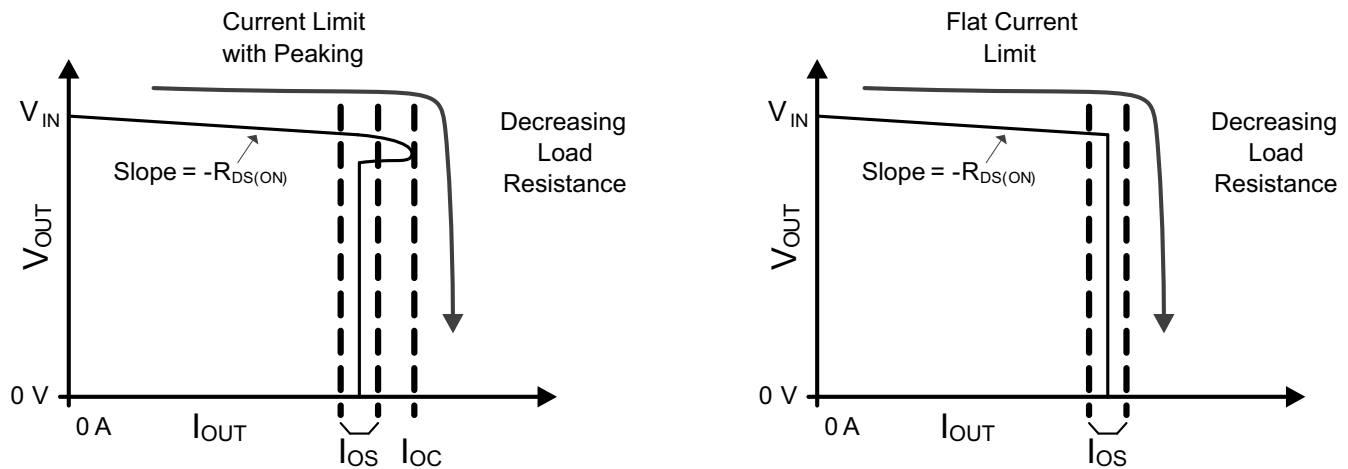


图 8-5. Current Limit Profiles

### 8.3.5 Output Discharge

A 470  $\Omega$  (typical) output discharge resistance dissipates stored charge and leakage current on OUT when the TPD3S014-Q1 is in UVLO or disabled. The pull-down circuit loses bias gradually as  $V_{IN}$  decreases, causing a rise in the discharge resistance as  $V_{IN}$  falls towards 0 V.

### 8.3.6 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, a 0.1  $\mu\text{F}$  or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.

All protection circuits such as the TPD3S014-Q1 has the potential for input voltage overshoots and output voltage undershoots.

Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power bus inductance and input capacitance when the IN terminal is high impedance (before turnon). Theoretically, the peak voltage is 2 times the applied. The second cause is because of the abrupt reduction of output short circuit current when the TPD3S014-Q1 turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the TPD3S014-Q1 output is shorted. Applications with large input inductance (for example, connecting the evaluation board to the bench power-supply through long cables) may require large input capacitance reduce the voltage overshoot from exceeding the absolute maximum voltage of the device. The fast current-limit speed of the TPD3S014-Q1 to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1  $\mu\text{F}$  to 22  $\mu\text{F}$  adjacent to the TPD3S014-Q1 input aids in both speeding the response time and limiting the transient seen on the input power bus. Momentary input transients to 6.5 V are permitted.

Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPD3S014-Q1 has abruptly reduced OUT current. Energy stored in the inductance drives the OUT voltage down and potentially negative as it discharges. Applications with large output inductance (such as from a cable) benefit from use of a high-value output capacitor to control the voltage undershoot. When implementing USB standard applications, a 120- $\mu$ F minimum output capacitance is required. Typically a 150- $\mu$ F electrolytic capacitor is used, which is sufficient to control voltage undershoots. However, if the application does not require 120  $\mu$ F of capacitance, and there is potential to drive the output negative, a minimum of 10- $\mu$ F ceramic capacitance on the output is recommended. The voltage undershoot must be controlled to less than 1.5 V for 10  $\mu$ s.

## 8.4 Device Functional Modes

### 8.4.1 Operation With $V_{IN} < 4$ V (Minimum $V_{IN}$ )

These devices operate with input voltages above 4 V. The maximum UVLO voltage on IN is 4 V and the devices will operate at input voltages above 4 V. Any voltage below 4 V may not work with these devices. The minimum UVLO is 3.5 V, so some devices may work between 3.5 V and 4 V. At input voltages below the actual UVLO voltage, these devices will not operate.

### 8.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.45 V typical and 2 V maximum. With EN held below that voltage the device is disabled and the load switch will be open. The IC quiescent current is reduced in this state. When the EN pin is above its rising edge threshold and the input voltage on the IN pin is above its UVLO threshold, the device becomes active. The load switch is closed, and the current limit feature is enabled. The output voltage on OUT ramps up with the soft start value  $T_{ON}$  in order to prevent large inrush current surges on  $V_{BUS}$  because of a heavy capacitive load. When EN voltage is lowered below its falling edge threshold, the device output voltage also ramps down with soft turnoff value  $T_{OFF}$  to prevent large inductive voltages being presented to the system in the case a large load current is following through the device.

### 8.4.3 Operation of Level 4 IEC 61000-4-2 ESD Protection

Regardless of which functional mode the devices are in, the TPD3S014-Q1 provides Level 4 IEC 61000-4-2 ESD Protection on the pins of the USB connector.

## 9 Application and Implementation

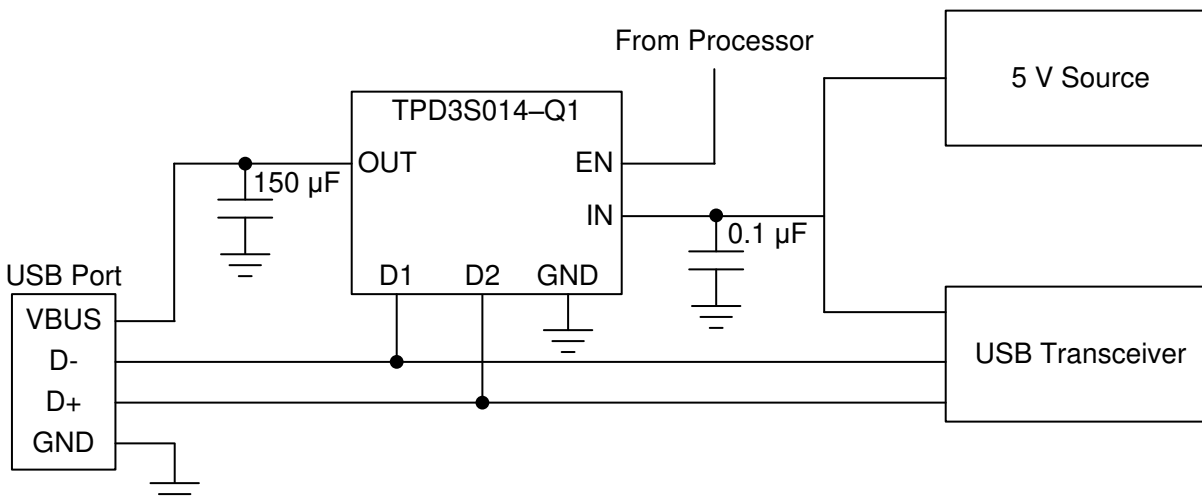
### Note

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

The TPD3S014-Q1 is a device that features a current limited load switch and a two-channel TVS based ESD protection diode array. It is typically used to provide a complete protection solution for USB host ports. USB host ports are required by the USB specification to provide a current limit on the VBUS path in order to protect the system from overcurrent conditions on the port that could lead to system damage and user injury. Additionally, USB ports typically require system level IEC ESD protection because of direct end-user interaction. The following design procedure can be used to determine how to properly implement the TPD3S014-Q1 in your systems to provide a complete, one-chip solution for your USB ports.

### 9.2 Typical Application



Copyright © 2016, Texas Instruments Incorporated

图 9-1. USB2.0 Application Schematic

#### 9.2.1 Design Requirements

For this design example, design parameters shown in 表 9-1 are used.

表 9-1. Design Parameters

DESIGN PARAMETER	VALUE
USB port type	Standard downstream port
Signal voltage range on V <sub>BUS</sub>	0 V to 5.25 V
Current range on V <sub>BUS</sub>	0 mA to 500 mA
Drive EN low (disabled)	0 V to 0.7 V <sup>(1)</sup>
Drive EN high (enabled)	2 V to 5.5 V <sup>(1)</sup>
Maximum voltage droop allowed on adjacent USB port	330 mV
Maximum data rate	480 Mbps

(1) If active low logic is desired, see the [Implementing Active Low Logic](#) section.

### 9.2.2 Detailed Design Procedure

To properly implement your USB port with the TPD3S014-Q1, the first step is to determine what type of USB port is implemented in the system, whether it be a Standard Downstream Port (SDP), Charging Downstream Port (CDP), or Dedicated Charging Port (DCP); this informs us what maximum continuous operating current will be on VBUS. In our example, we are implementing an SDP port, so the maximum continuous current allowed to be pulled by a device is 500 mA. Therefore, we must choose a current limit switch that is 5.25 V tolerant, can handle 500 mA continuous DC current, and has a current limit point is above 500 mA so it will not current limit during normal operation. The TPD3S014-Q1 is therefore the best choice for this application, as it has these features, and in fact was specifically designed for this application.

The next decision point is choosing the input and output capacitors for the current limit switch. A minimum of 0.1  $\mu\text{F}$  is always recommended on the IN pin. For the OUT pin on VBUS, USB standard requires a minimum of 120  $\mu\text{F}$ ; typically a 150  $\mu\text{F}$  capacitor is used. The purpose of the capacitance requirement on the VBUS line in the USB specification is to prevent the adjacent USB port's VBUS voltage from dropping more than 330 mV during a hot-plug or fault occurrence on the VBUS pin of one USB port. Hot-plugs and fault conditions on one USB port must not disturb the normal operation of an adjacent USB port; therefore, it is possible to use an output capacitance lower than 120  $\mu\text{F}$  if the system is able to keep voltage droops on adjacent USB ports less than or equal to 330 mV. For example, if the DC/DC powering VBUS has a fast transient response, 120  $\mu\text{F}$  may not be required.

If the USB port is powered from a shared system 5 V rail, a system designer may desire to use an input capacitor larger than 0.1  $\mu\text{F}$  on the IN pin. This is largely dependent on the PCB layout and parasitics, as well as your maximum tolerated voltage droop on the shared rail during transients. For more information on choosing input and output capacitors, see the [Input and Output Capacitance](#) section.

The EN pin controls the on and off state of the device, and typically is connected to the system processor for power sequencing. However, the EN pin can also be shorted to the IN pin to always have the TPD3S014-Q1 on when 5 V power supply on; this also saves a GPIO pin on your processor.

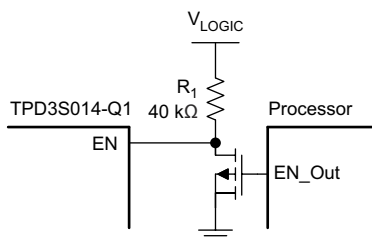
For a USB port with High-Speed 480 Mbps operation, low capacitance TVS ESD protection diodes are required to protect the D+ and D– lines in the event of system level ESD event. The TPD3S014-Q1 has 2-channels of low capacitance TVS ESD protection diodes integrated. When placed near the USB connector, the TPD3S014-Q1 offers little or no signal distortion during normal operation. The TPD3S014-Q1 also ensures that the core system circuitry is protected in the event of an ESD strike. PCB layout is critical when implementing TVS ESD protection diodes in your system. See the [Layout](#) section for proper guidelines on routing your USB lines with the TPD3S014-Q1.

### 9.2.3 Implementing Active Low Logic

For active low logic, a transistor can be used with the TPD3S014-Q1 EN Pin. [图 9-2](#) shows how to implement Active low logic for EN pin.

Using an nFET transistor, when the Processor sends a low signal, the transistor is switched off, and  $V_{\text{LOGIC}}$  pulls up EN through  $R_1$ . When the Processor sends a “high” signal, the nFET is switched on and sinks current from the EN Pin and  $R_1$ . For 5 V  $V_{\text{LOGIC}}$ , with the appropriate on-resistance ( $R_{\text{ON}}$ ) value in the nFET and resistance for  $R_1$ , the  $V_{\text{IL}}$  for EN can be met. For example, with a transistor with  $R_{\text{ON}}$  of 3  $\Omega$ , a pull-up resistor as low as 11  $\Omega$  provides a logic level of 0.7 V. For power-budgeting concerns, a better choice is  $R_1$  of 40 k $\Omega$  which provides 0.25 V for EN when the Processor asserts high, and 4.96 V when the Processor asserts low.

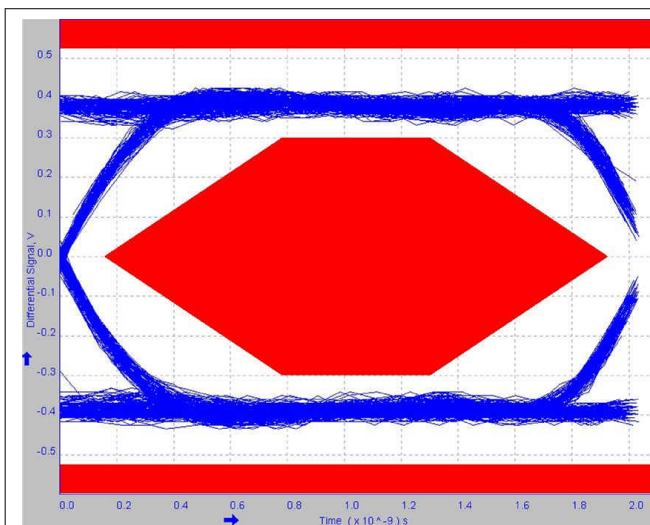




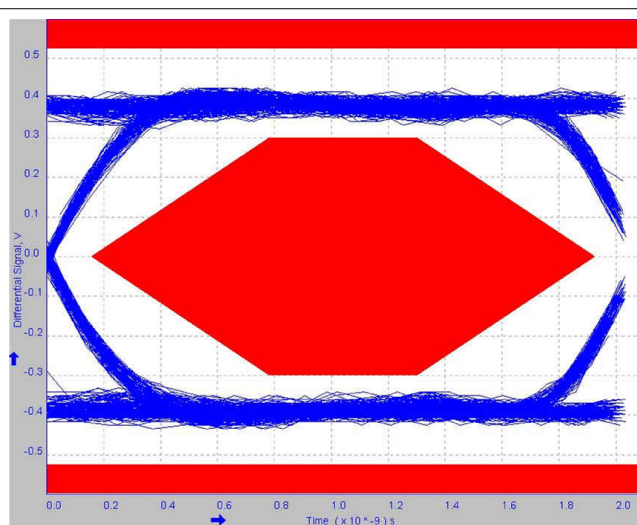
Copyright © 2016, Texas Instruments Incorporated

**图 9-2. Implementing Active Low Logic for EN Pin**

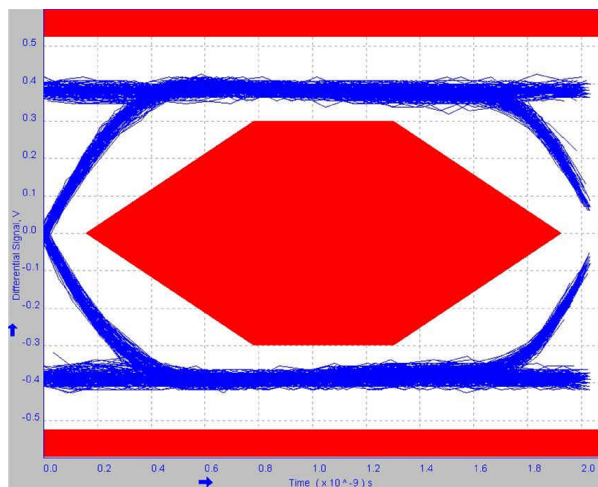
## 9.2.4 Application Curves



**图 9-3. Eye-Diagram Without EVM**



**图 9-4. Eye-Diagram With EVM, Without TPD3S014-Q1**



**图 9-5. Eye-Diagram of TPD3S014-Q1 on EVM**

## 10 Power Supply Recommendations

The TPD3S014-Q1 is designed to operate from a 5-V input voltage supply. This input must be well regulated. If the input supply is located more than a few inches away from the TPD3S014-Q1, additional bulk capacitance may be required in addition to the recommended minimum 0.1- $\mu$ F bypass capacitor on the IN pin to keep the input rail stable during fault events.

## 11 Layout

### 11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

### 11.2 Layout Example

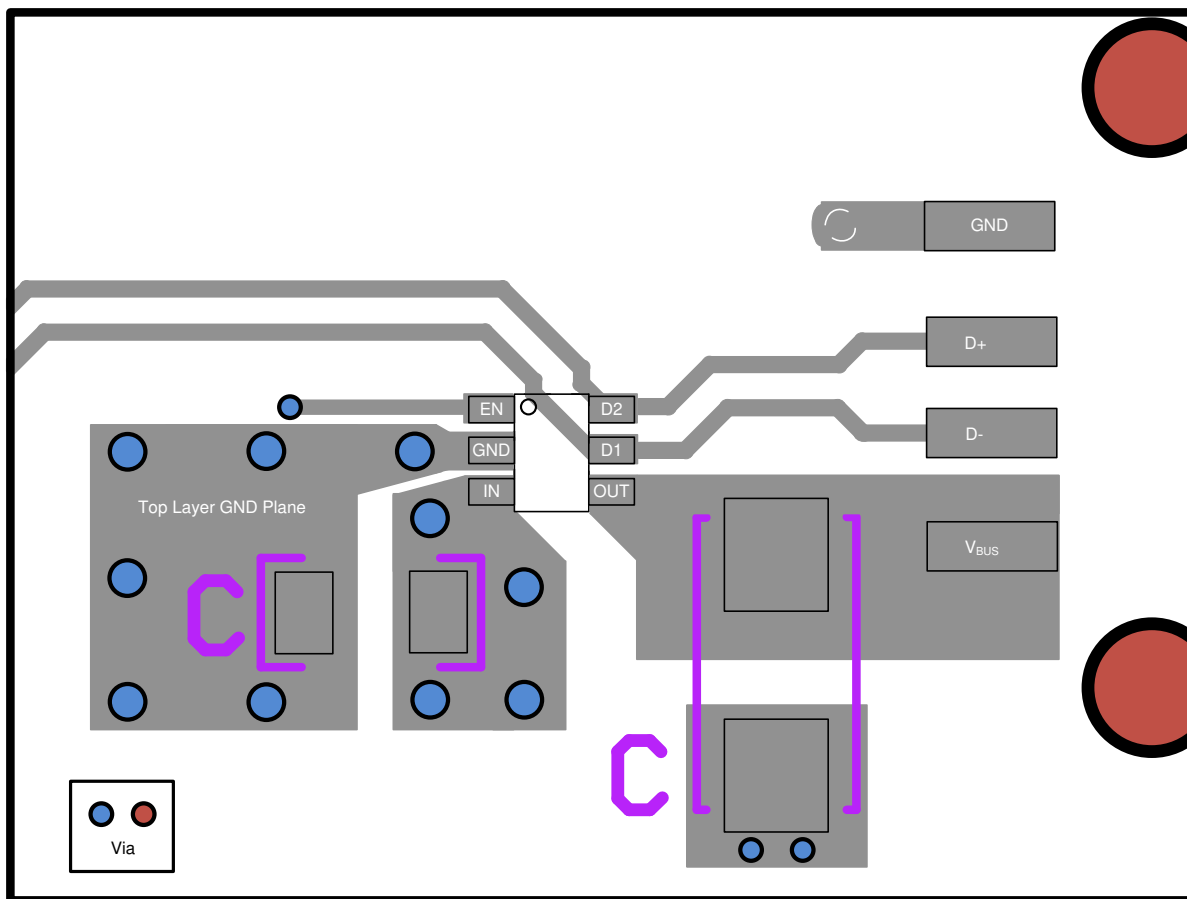


图 11-1. USB2.0 Type A TPD3S014-Q1 Board Layout

### 11.3 Power Dissipation and Junction Temperature

anged Temperature from 125°C to 105°C in Power Dissipation and Junction Temperature section

It is good design practice to estimate power dissipation and maximum expected junction temperature of the TPD3S014-Q1. The system designer can control choices of the devices proximity to other power dissipating devices and printed circuit board (PCB) design based on these calculations. These have a direct influence on maximum junction temperature. Other factors, such as airflow and maximum ambient temperature, are often determined by system considerations. It is important to remember that these calculations do not include the effects of adjacent heat sources, and enhanced or restricted air flow. Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical. In particular, connect the GND pin to a large ground plane for the best thermal dissipation. The following PCB layout example in 图 11-2 was used to determine the  $R_{\theta JA}$ . Custom thermal impedances noted in the [Thermal Information](#) table. It is based on the use of the JEDEC high-k circuit board construction with 4, 1 oz. copper weight layers (2 signal and 2 plane).

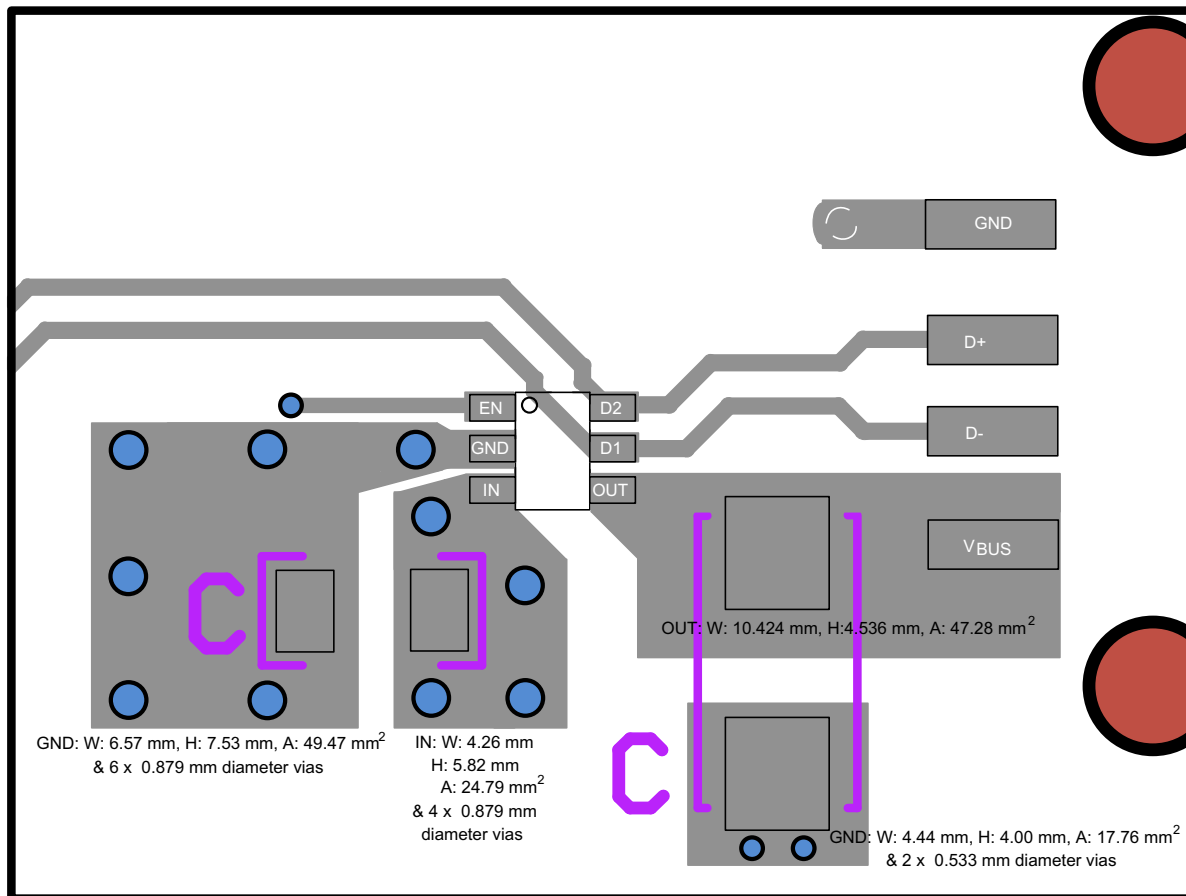


图 11-2. PCB Layout Example

The following procedure requires iteration a power loss is because of the internal MOSFET  $I^2 \times R_{DS(ON)}$ , and  $R_{DS(ON)}$  is a function of the junction temperature. See 方程式 1. As an initial estimate, use the  $R_{DS(ON)}$  at 105°C from the [Typical Characteristics](#), and the preferred package thermal resistance for the preferred board construction from the [Thermal Information](#) table.

$$T_J = T_A + [(I_{OUT}^2 \times R_{DS(ON)}) \times R_{\theta JA}] \quad (1)$$

where

- $I_{OUT}$  = Rated OUT pin current (A)
- $R_{DS(ON)}$  = Power switch on-resistance at an assumed  $T_J$  ( $\Omega$ )
- $T_A$  = Maximum ambient temperature ( $^{\circ}\text{C}$ )
- $T_J$  = Maximum junction temperature ( $^{\circ}\text{C}$ )

- $R_{\theta JA}$  = Thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

If the calculated  $T_J$  is substantially different from the original assumption, estimate a new value of  $R_{DS(ON)}$  using the typical characteristic plot and recalculate.

If the resulting  $T_J$  is not less than  $125^{\circ}\text{C}$ , try a PCB construction with a lower  $R_{\theta JA}$ . The junction temperature derating curve based on the TI standard reliability duration is shown in 图 11-3.

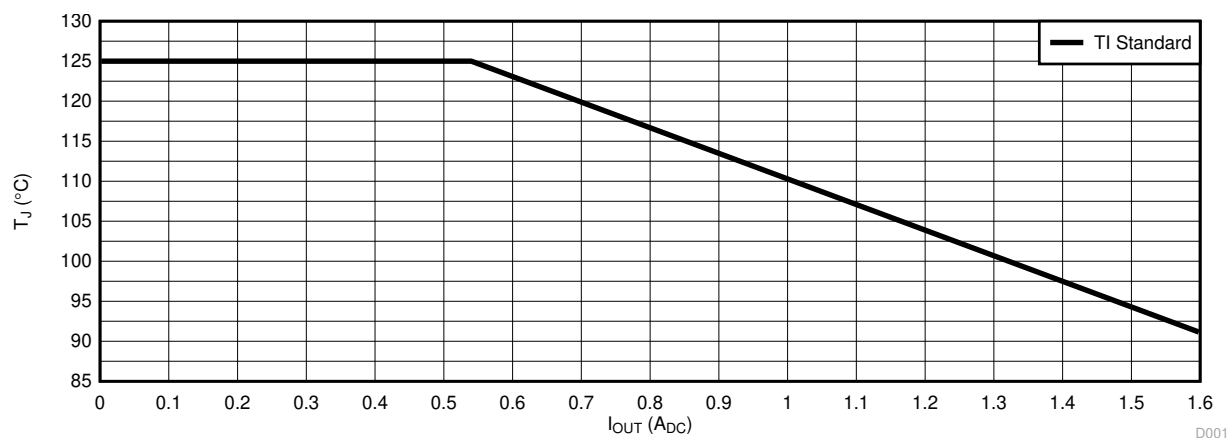


图 11-3. Junction Temperature Derating Curve

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

*TPD3S014-Q1EVM User's Guide*, [SLVUAQ0](#).

### 12.2 支持资源

[TI E2E™ 中文支持论坛](#)是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 12.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPD3S014TDBVRQ1</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	13WW
TPD3S014TDBVRQ1.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	13WW

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

### OTHER QUALIFIED VERSIONS OF TPD3S014-Q1 :

- Catalog : [TPD3S014](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD3S014TDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD3S014TDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0

**DBV0006A****PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月