具有 15kV 接触放电和超低钳位电压的 TPD4E6B06 四通道双向低电容 ESD 保护器件

1 特性

- IEC 61000-4-2 4 级
  - ±15kV 接触放电
  - ±15kV 气隙放电
- IEC 61000-4-5（浪涌）：3A (8/20μs)
- IO 电容值：4.8pF（典型值）
- R_{DYN}：0.75Ω（典型值）
- 直流击穿电压：±6V（最小值）
- 超低泄漏电流：100nA（最大值）
- 钳位电压：10V（I_{PP} = 1A 时的最大值）
- 工业温度范围：-40°C 至 +125°C
- 节省空间的 DPW 封装 (0.8mm × 0.8mm)

2 应用

- 音频线路
  - 麦克风
  - 耳机
  - 免提电话
- SD 接口
- SIM 接口
- 移动键盘或其它按钮
- 手机
- 电子书
- 便携式媒体播放器
- 数码摄像机
- 平板个人电脑
- 可佩带产品

3 说明

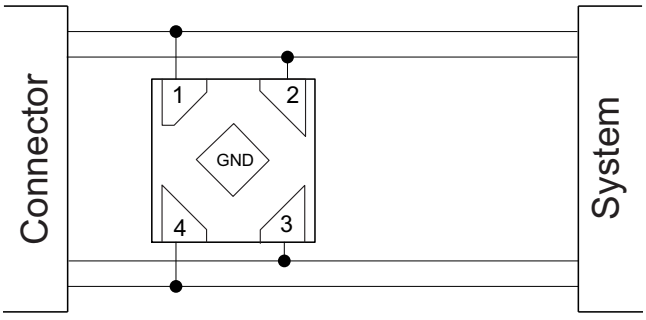
TPD4E6B06 是一款采用超小型 DPW 封装的四通道静电放电 (ESD) 保护器件。此器件是业内领先的小型 4 通道瞬态电压抑制器 (TVS) 二极管，间距为 0.48mm。这种较大的间距有助于节省印刷电路板 (PCB) 的制造成本。此器件提供符合 IEC61000-4-2 标准的高达 15kV 的接触放电要求。此器件具有 ESD 钳位电路，该电路的背对背二极管支持双极双向信号。4.8pF（典型值）的线路电容使得此器件适用于 支持高达 700MHz 数据速率的广泛应用。

器件信息(1)

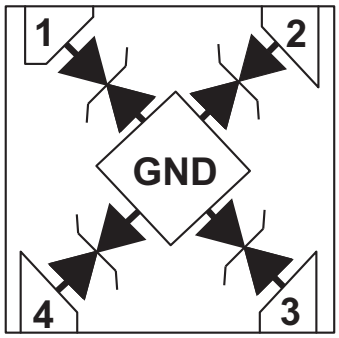
器件型号	封装	封装尺寸（标称值）
TPD4E6B06	X2SON (4)	0.80mm × 0.80mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化电路原理图



引脚分配



0.8 mm x 0.8mm X2SON Package
(Bottom View)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (February 2017) to Revision C — **Page**

- Added "Power Supply Recommendations" section ... 12

Changes from Revision A (December 2015) to Revision B — **Page**

- Changed the value of R_{DYN} from 0.75 and 0.65 to 0.45 and 0.42 respectively, in the *Electrical Characteristics* table ... 5

Changes from Original (May 2014) to Revision A — **Page**

- Updated the *Handling Ratings* table into an *ESD Ratings* table and moved T_{stg} to the *Absolute Maximum Ratings* table ... 4
- Added new note to *Absolute Maximum Ratings* table ... 4
- Added frequency test condition to *IO capacitance* in the *Electrical Characteristics* table ... 5
- 已添加 *社区资源* ... 14

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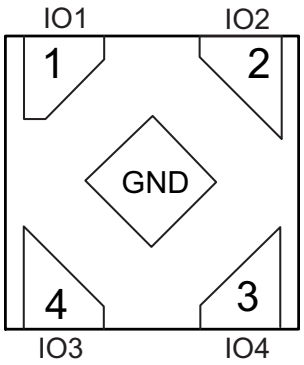
5 Pin Configuration and Functions

DPW Package
5-Pin X2SON
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NO	NAME		
1	IO1	IO	ESD protected line
2	IO2	IO	ESD protected line
3	IO3	IO	ESD protected line
4	IO4	IO	ESD protected line
5	GND	—	Ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 Current (t_p – 8/20 µs)(4)		3	A
	IEC 61000-4-5 Power (t_p – 8/20 µs)(4)		40	W
Operating temperature		–40	125	°C
Storage temperature	T_{stg}	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute maximum ratings apply over recommended junction temperature range.
(3) Voltages are with respect to GND unless otherwise noted.
(4) Measured at 25°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–5.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPD4E6B06 DPW (X2SON) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	291.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	224.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	245.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	245.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	195.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

T_A = –40°C to +125°C (unless otherwise specified)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} = 10 µA	–5.5		5.5	V
V_{BRF}	Break-down voltage	$I_{IO\ to\ GND}$ = 1 mA	6			V
V_{BRR}	Break-down voltage	$I_{GND\ to\ IO}$ = 1 mA	6			V
I_{LEAK}	Leakage current	V_{IO} = 5 V			100	nA
V_{CLAMP}	Clamp voltage with ESD strike	I = 1 A, IO to GND, 8/20 µs(1)		10		V
		I = 5 A, IO to GND, 8/20 µs(1)		13		V
		I = 1 A, IO to GND, 8/20 µss(1)		9		V
		I = 5 A, IO to GND, 8/20 µs(1)		13		V
R_{DYN}	Dynamic resistance	Any IO to GND pin(2)		0.45		Ω
		GND to any IO pin(2)		0.42		Ω
C_L	IO capacitance	V_{IO} = 2.5 V; f = 10 MHz		4.8	7	pF

(1) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC61000-4-5.
(2) Extraction of RDYN using least squares fit of TLP characteristics between I = 10 A and I = 20 A.

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6.6 Typical Characteristics

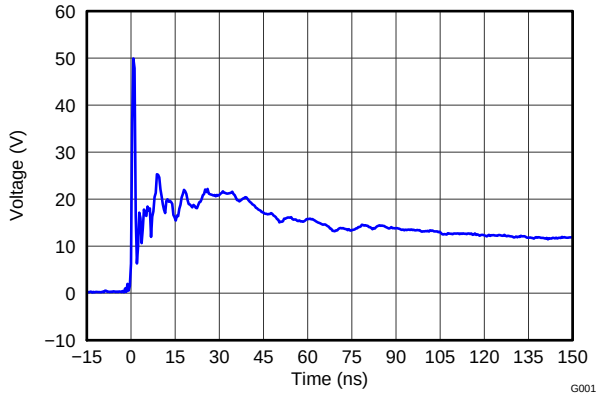

Figure 1. IEC 61000-4-2 Clamping Voltage, 8-kV Contact

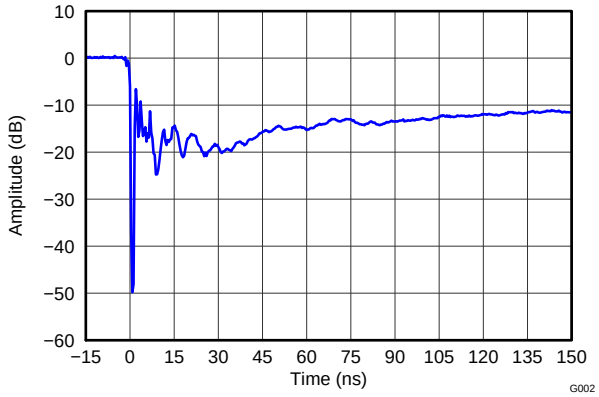

Figure 2. IEC 61000-4-2 Clamping Voltage, –8-kV Contact

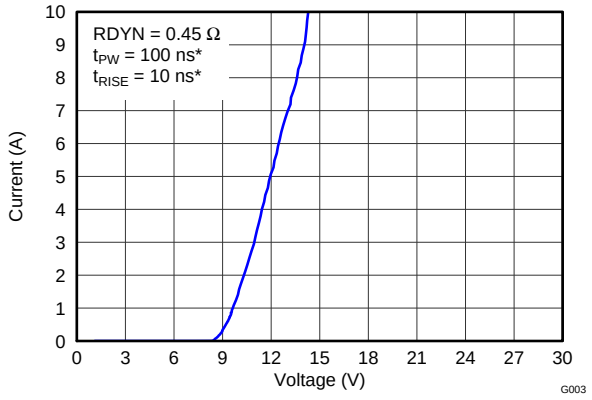

Figure 3. TLP, t_{PW} = 100 ns, t_{RISE} = 10 ns, IO to GND

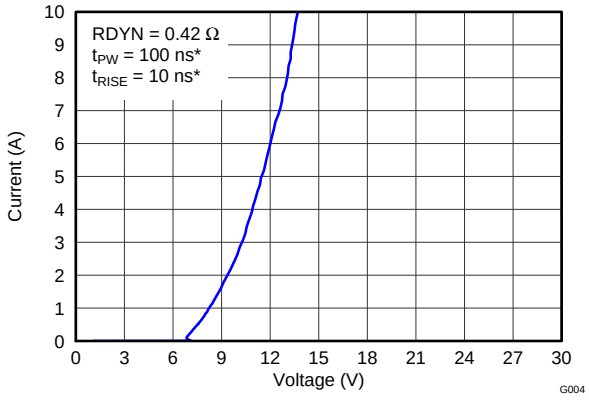

Figure 4. TLP, t_{PW} = 100 ns, t_{RISE} = 10 ns, GND to IO

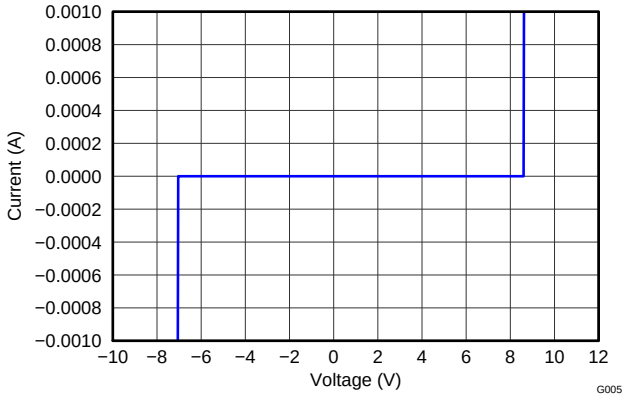

Figure 5. IV Curve

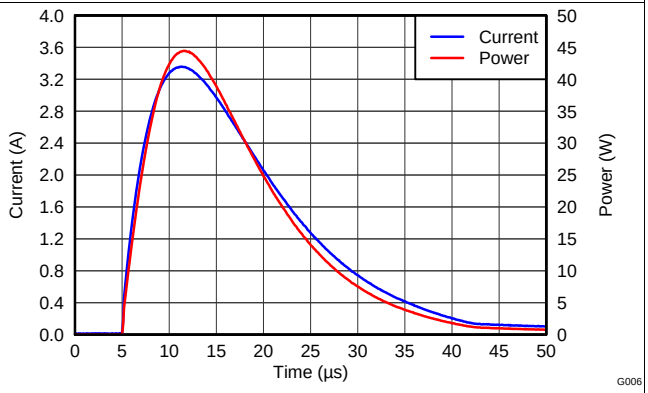

Figure 6. Surge Curves, IO to GND

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Typical Characteristics (continued)

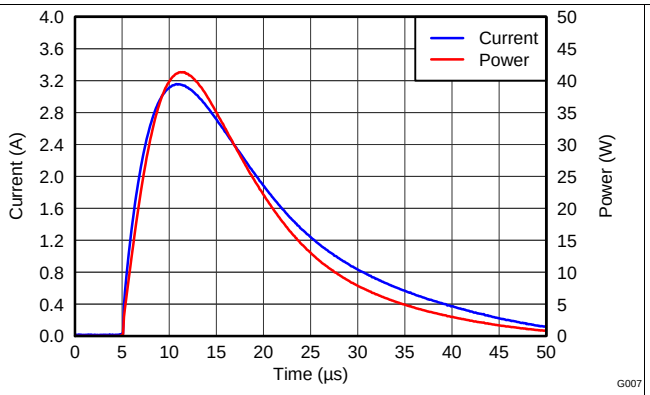

Figure 7. Surge Curves, GND to IO

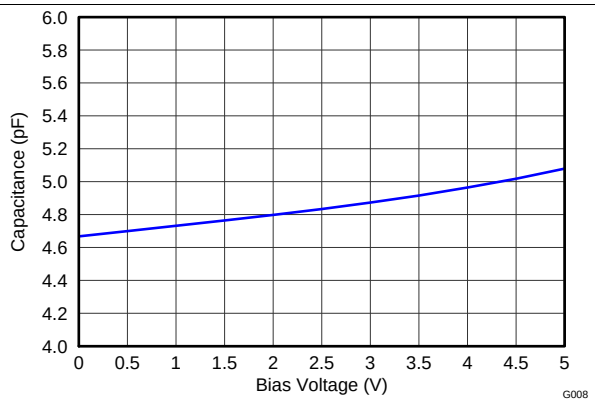

Figure 8. Capacitance

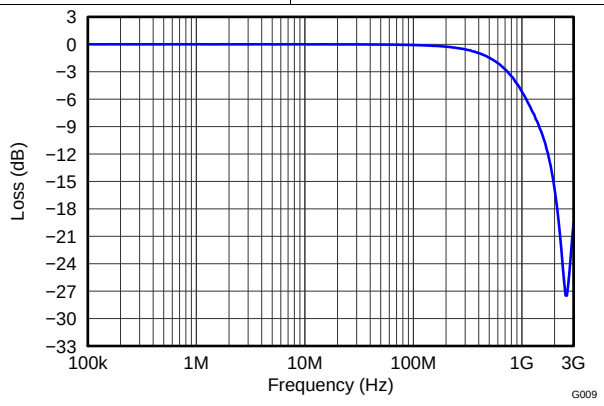

Figure 9. Insertion Loss

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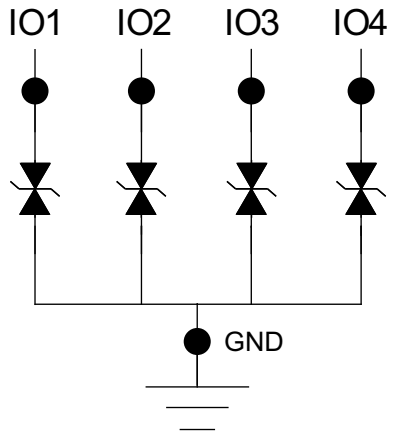
7 Detailed Description

7.1 Overview

The TPD4E6B06 is a four channel ESD Protection device in an ultra small DPW package. It is the industry's smallest 4-CH ESD protection device with 0.48-mm pitch. This larger pitch helps save on PCB manufacturing costs. The device provides IEC61000-4-2 compliance up to 15-kV contact discharge. It has an ESD clamp circuit with back-to-back diodes for bipolar/bidirectional signal support. The 4.8-pF (Typical) line capacitance is suitable for a wide range of applications supporting frequencies up to 700 MHz.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 Level 2 ESD Protection

The IO pins can withstand ESD events up to ±15-kV contact and ±15-kV air. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 3 A and 40 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.3 IO Capacitance

The capacitance between any IO pin to ground is 4.8 pF (typical). This capacitance supports frequencies up to 700 MHz.

7.3.4 R_{DYN}

The low R_{DYN} of 0.75 Ω (typical) allows for lower clamping voltages.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of any IO pin is a minimum of ±6 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±5.5 V (minimum).

7.3.6 Ultra-Low Leakage Current

The IO pins feature an ultra-low leakage current of 100 nA (maximum) with a bias of 2.5 V.

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Feature Description (continued)

7.3.7 Clamping Voltage

The IO pins feature an ESD clamp capable of clamping the voltage to 10 V (IO to GND) or 9 V (GND to IO) of IEC61000-4-5 surge when I_{PP} = 1 A.

7.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.9 Space Saving DPW Package

The small 0.8 mm × 0.8 mm package size saves board space and makes it easy to add ESD protection.

7.4 Device Functional Modes

The TPD4E6B06 is a passive integrated circuit that triggers when voltages are above V_{BRF} or V_{BRR}. During ESD events, voltages as high as ±15 kV (air) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of the TPD4E6B06 (usually within 10s of nano-seconds) the device reverts to passive.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4E6B06 is a diode array type TVS. These low capacitance types of TVSs are typically used to provide a path to ground for dissipating ESD events on hi speed signal lines between a human interface connector and a system. During high voltage ESD strikes, the device clamps to a safe voltage level to protect the system.

The typical application of the TPD4E6B06 is to be placed in between the connector and the system. The low capacitance of the TPD4E6B06 gives flexibility in the end application, as it can be used on many different high speed interfaces.

8.2 Typical Application

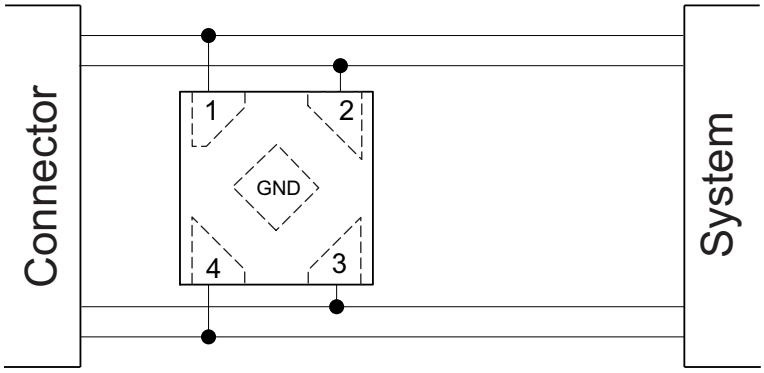

Figure 10. Protecting Data Lines

8.2.1 Design Requirements

Table 1 shows the design parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Signal range on data lines	–5.5 V to 5.5 V
Operating frequency	Up to 700 MHz

8.2.2 Detailed Design Procedure

The designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

8.2.2.1 Signal Range

The TPD4E6B06 has 4 protection channels for signal lines. Any I/O supports a signal range of –5.5 V to 5.5 V.

8.2.2.2 Operating Frequency

The TPD4E6B06 has 4.8 pF of capacitance (Typical), supporting up to 700 MHz frequencies.

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8.2.3 Application Curve

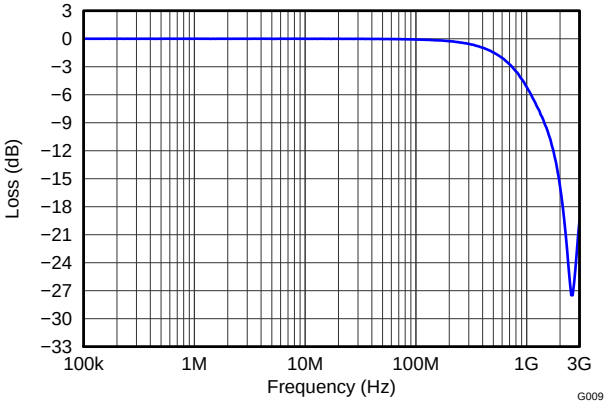

Figure 11. Insertion Loss (Any IO to GND)

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9 Power Supply Recommendations

The TPD4E6B06 is a passive TVS diode-based ESD protection device, so there is no need to power it. Ensure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- Place the device as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Examples

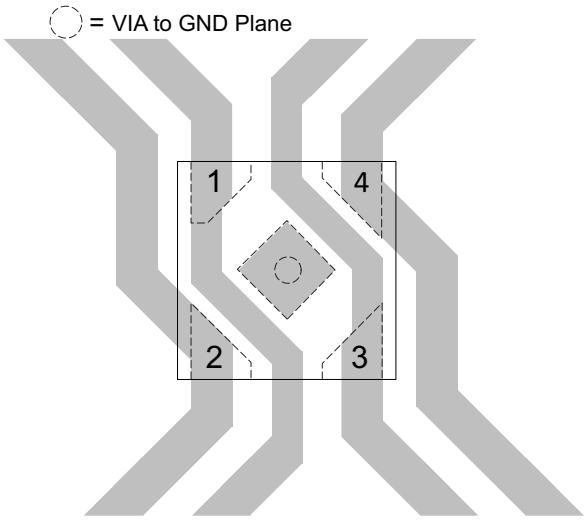

Figure 12. Single Layer Routing

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Layout Examples (接下页)

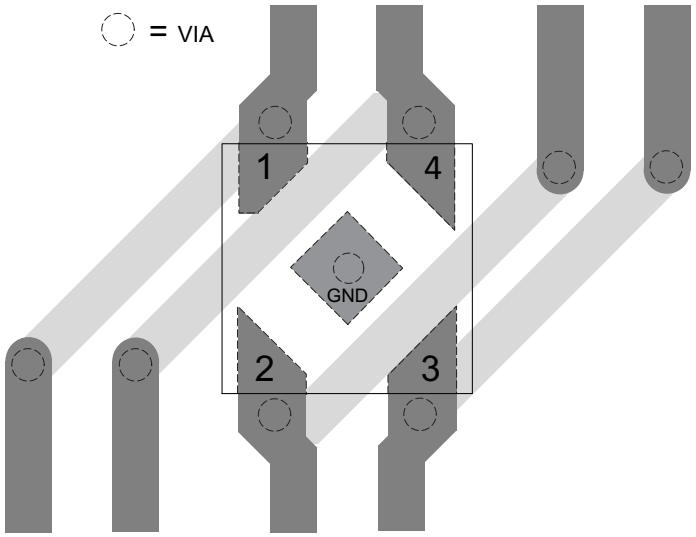

Figure 13. Double Layer Routing

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- *阅读和理解 ESD 保护数据表*
- *《ESD 布局指南》*

11.2 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

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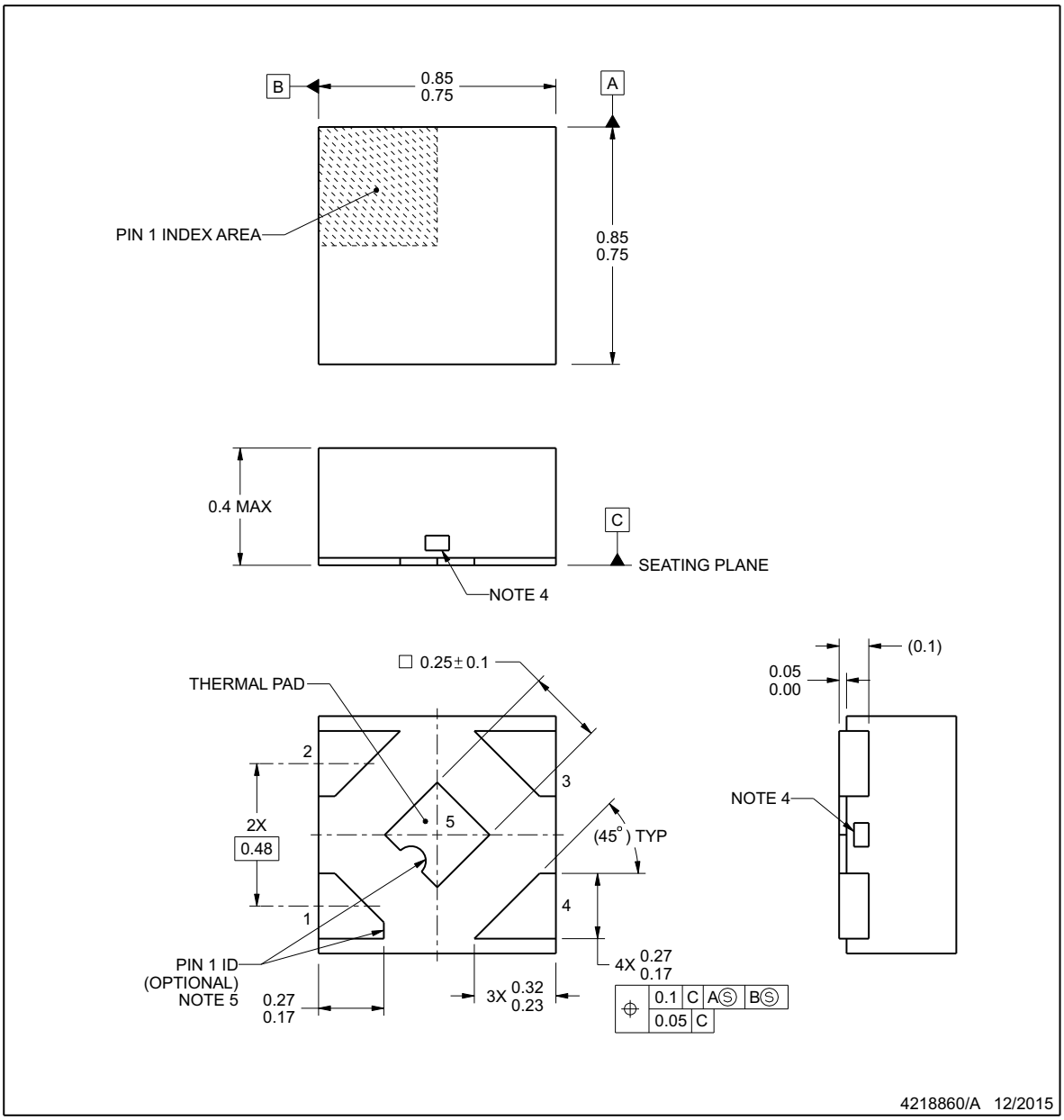
PACKAGE OUTLINE

DPW0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

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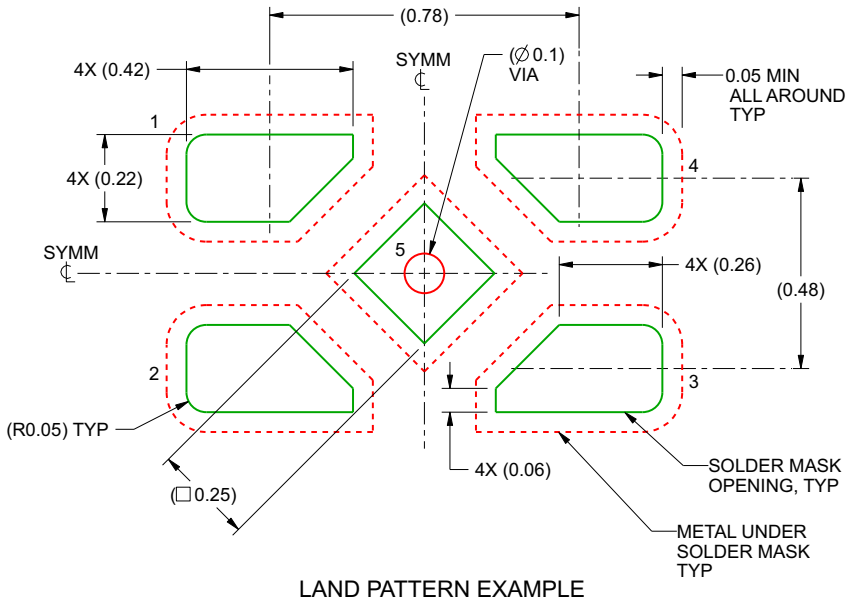
EXAMPLE BOARD LAYOUT

DPW0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4218860/A 12/2015

NOTES: (continued)

6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

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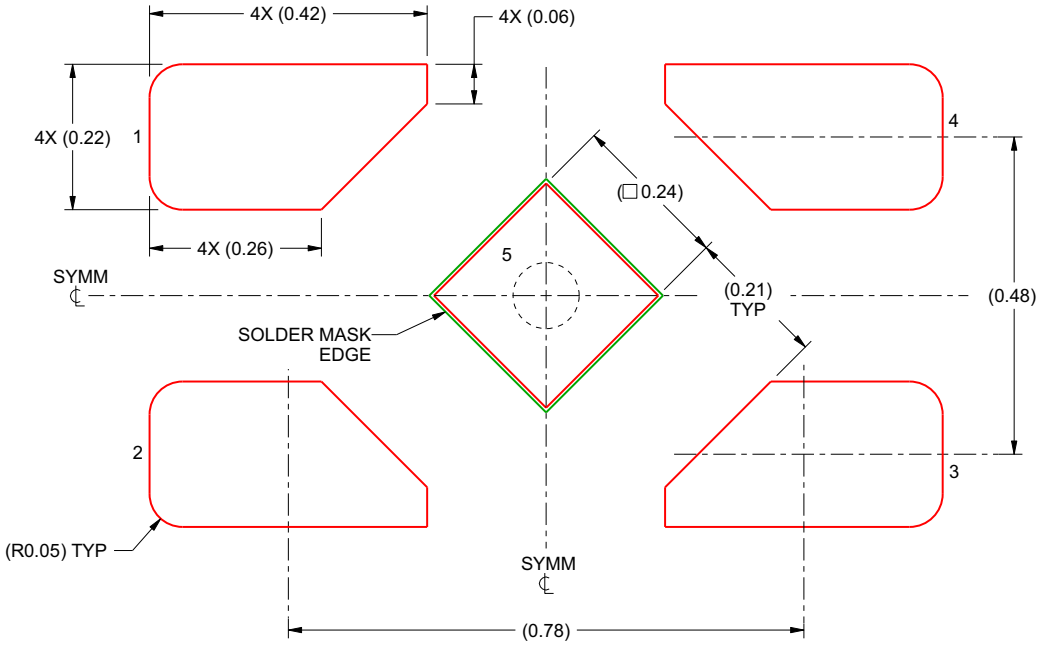
EXAMPLE STENCIL DESIGN

DPW0004A — **X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5:
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

4218860/A 12/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4E6B06DPWR	Active	Production	X2SON (DPW) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(B1, B5) B2
TPD4E6B06DPWR.B	Active	Production	X2SON (DPW) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(B1, B5) B2
TPD4E6B06DPWRG4	Active	Production	X2SON (DPW) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B1 B2
TPD4E6B06DPWRG4.B	Active	Production	X2SON (DPW) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B1 B2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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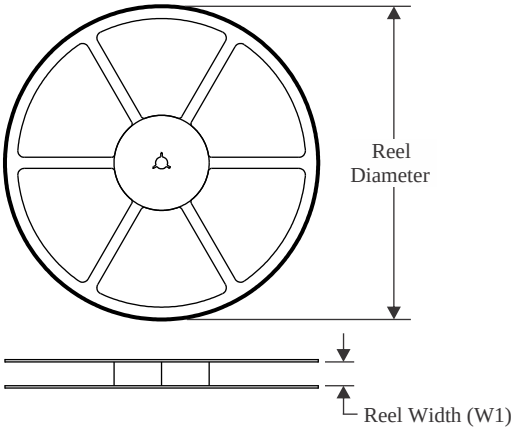
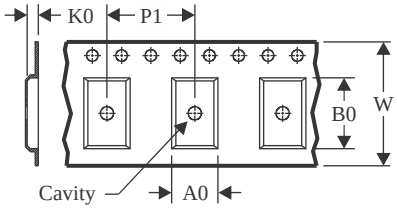
TAPE AND REEL INFORMATION

REEL DIMENSIONS

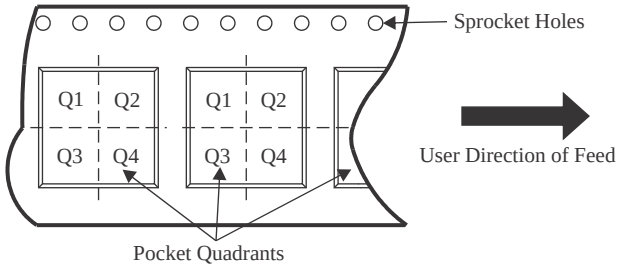


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

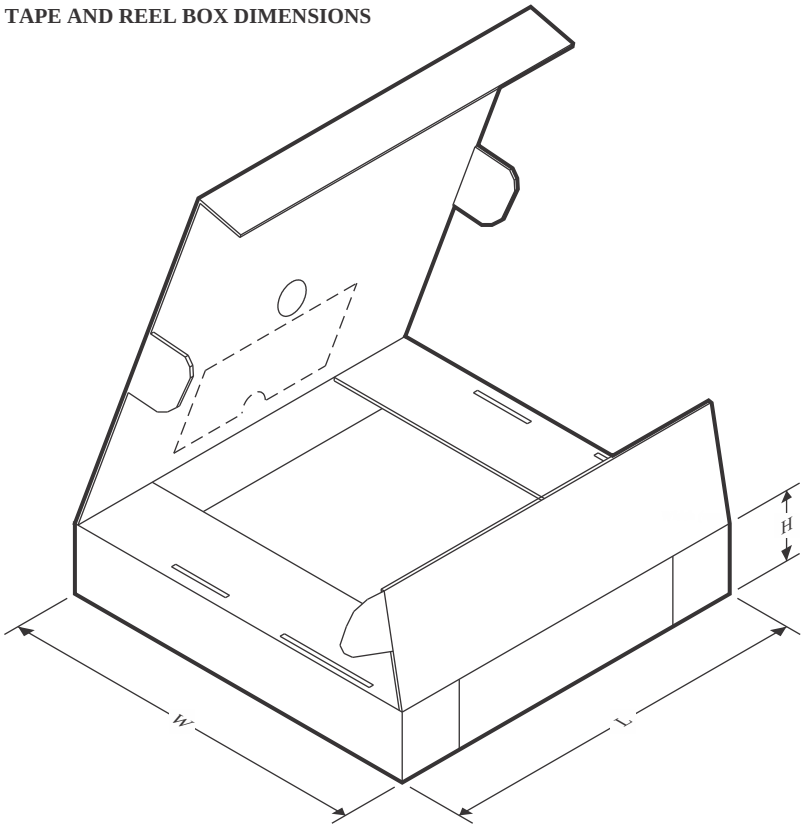
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E6B06DPWR	X2SON	DPW	4	3000	180.0	9.5	0.94	0.94	0.5	2.0	8.0	Q1
TPD4E6B06DPWRG4	X2SON	DPW	4	3000	180.0	9.5	0.94	0.94	0.5	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E6B06DPWR	X2SON	DPW	4	3000	184.0	184.0	19.0
TPD4E6B06DPWRG4	X2SON	DPW	4	3000	184.0	184.0	19.0

GENERIC PACKAGE VIEW

DPW 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

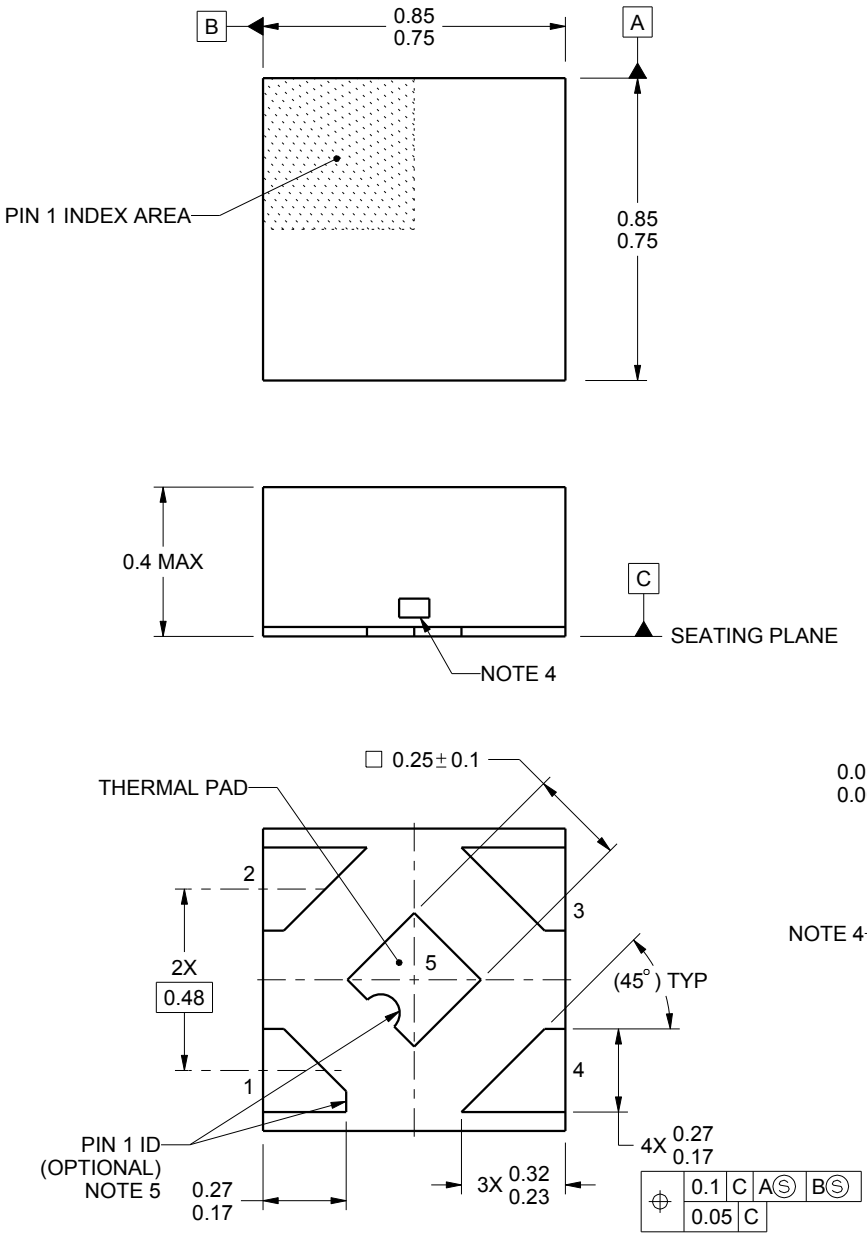
4211218-2/D

PACKAGE OUTLINE

DPW0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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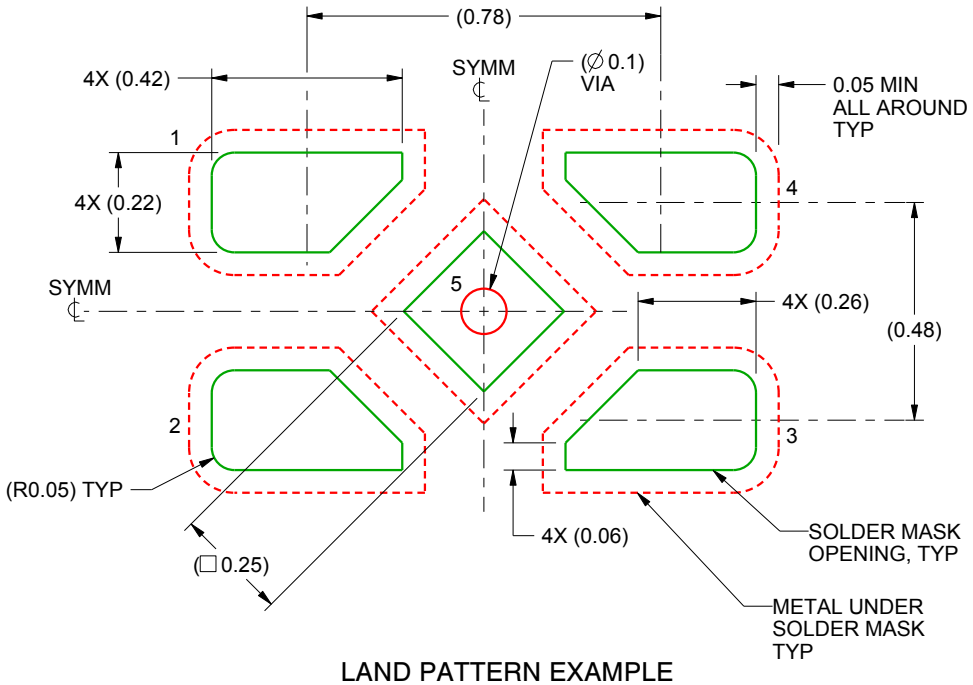
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

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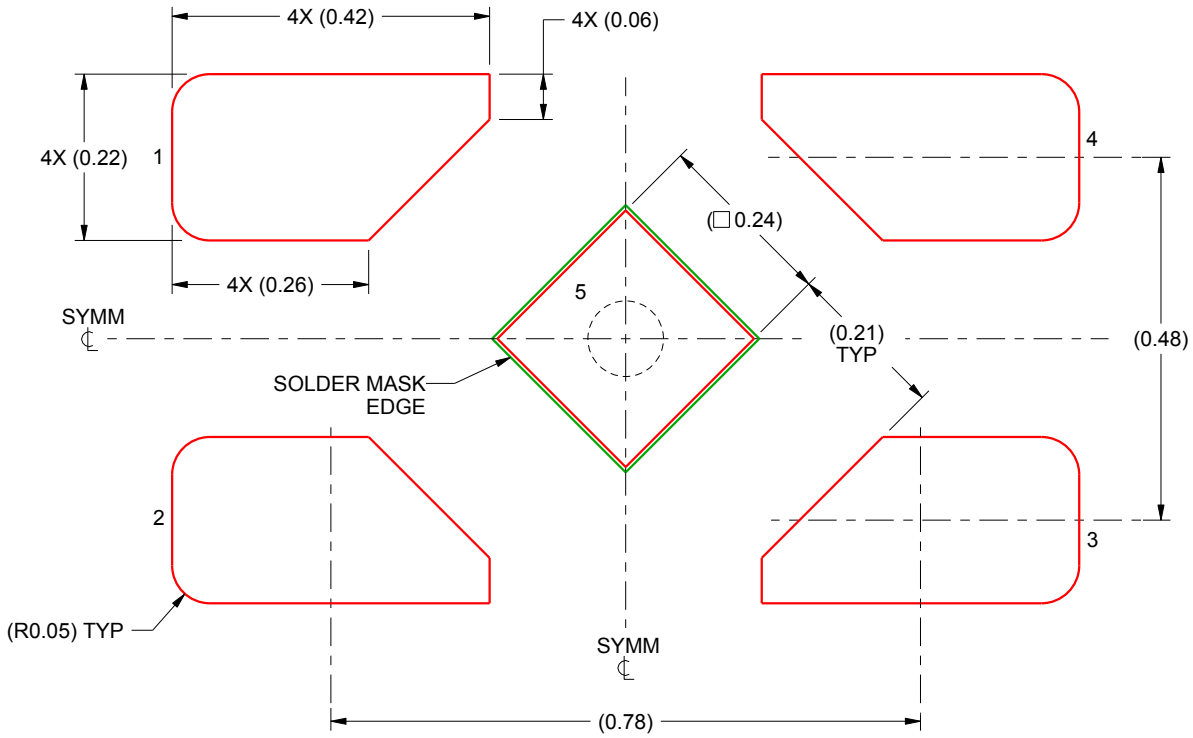
NOTES: (continued)

6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5:
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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