


# CURRENT-LIMITED, POWER-DISTRIBUTION SWITCHES

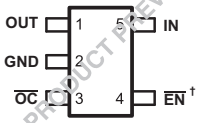
## FEATURES

- **70-mΩ High-Side MOSFET**
- **250-mA Continuous Current**
- **Thermal and Short-Circuit Protection**
- **Accurate Current Limit (0.3 A min, 0.7 A max)**
- **Operating Range: 2.7 V to 5.5 V**
- **0.6-ms Typical Rise Time**
- **Undervoltage Lockout**
- **Deglitched Fault Report ($\overline{OC}$)**
- **No $\overline{OC}$ Glitch During Power Up**
- **Maximum Standby Supply Current: 1-µA (Single and Dual) or 2-µA (Triple)**
- **Bidirectional Switch**
- **Ambient Temperature Range: –40°C to 85°C**
- **ESD Protection**
- **UL Pending**

## APPLICATIONS

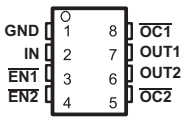
- **Heavy Capacitive Loads**
- **Short-Circuit Protections**

**TPS2045B/TPS2055B DBV PACKAGE (TOP VIEW)**

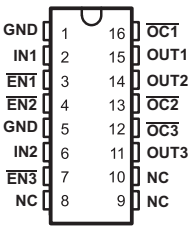





**TPS2046B D PACKAGE (TOP VIEW)**

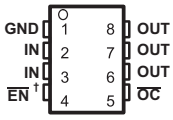



**TPS2047B D PACKAGE (TOP VIEW)**




NC - No Connection

**TPS2045B/TPS2055B D PACKAGE (TOP VIEW)**




†All enable inputs are active high (EN) for the TPS2055B.

## DESCRIPTION

The TPS204xB/TPS2055B power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices incorporate 70-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic-enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 0.5 A typically.

**GENERAL SWITCH CATALOG**

| 33 mΩ, Single | 80 mΩ, Single | 80 mΩ, Dual | 80 mΩ, Dual | 80 mΩ, Triple | 80 mΩ, Quad | 80 mΩ, Quad |
|---|---|---|---|---|---|---|
| TPS201xA 0.2 A to 2 A | TPS2014 600 mA | TPS2042B 500 mA | TPS2080 500 mA | TPS2043B 500 mA | TPS2044B 500 mA | TPS2085 500 mA |
| TPS202x 0.2 A to 2 A | TPS2015 1 A | TPS2052B 500 mA | TPS2081 500 mA | TPS2053B 500 mA | TPS2054B 500 mA | TPS2086 500 mA |
| TPS203x 0.2 A to 2 A | TPS2041B 500 mA | TPS2046B 250 mA | TPS2082 500 mA | TPS2047B 250 mA | TPS2048A 250 mA | TPS2087 500 mA |
| | TPS2051B 500 mA | TPS2056 250 mA | TPS2090 250 mA | TPS2057A 250 mA | TPS2058 250 mA | TPS2095 250 mA |
| | TPS2045A 250 mA | TPS2062 1 A | TPS2091 250 mA | TPS2063 1 A | | TPS2096 250 mA |
| | TPS2049 100 mA | TPS2066 1 A | TPS2092 250 mA | TPS2067 1 A | | TPS2097 250 mA |
| | TPS2055A 250 mA | TPS2060 1.5 A | | | | |
| | TPS2061 1 A | TPS2064 1.5 A | | | | |
| | TPS2065 1 A | | | | | |
| | TPS2068 1.5 A | | | | | |
| | TPS2069 1.5 A | | | | | |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## AVAILABLE OPTIONS

| $T_A$ | ENABLE | RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A) | TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A) | NUMBER OF SWITCHES | PACKAGED (1) | DEVICES |
|---|---|---|---|---|---|---|
| –40°C to 85°C | Active low | 0.25 | 0.5 | Single | SOIC (D) | TPS4045BD |
| | | | | | SOT-23 (DBV) | TPS4045BDBV |
| | Active high | 0.25 | 0.5 | Single | SOIC (D) | TPS4055BD |
| | | | | | SOT-23 (DBV) | TPS4055BDBV |
| | Active low | 0.25 | 0.5 | Dual | SOIC (D) | TPS2046BD |
| | | | | Triple | SOIC (D) | TPS2047BD |

(1) The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2046BDR)

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | | UNIT |
|---|---|---|---|
| $V_{I(IN)}$, $V_{I(INx)}$ | Input voltage range(2) | | –0.3 V to 6 V |
| $V_{O(OUTx)}$ | Output voltage range (2) | | –0.3 V to 6 V |
| $V_{I(/ENx)}$ | Input voltage range | | –0.3 V to 6 V |
| $V_{I(/OCx)}$ | Voltage range | | –0.3 V to 6 V |
| $I_{O(OUTx)}$ | Continuous output current | | Internally limited |
| | Continuous total power dissipation | | See Dissipation Rating Table |
| $T_J$ | Operating virtual junction temperature range | | –40°C to 125°C |
| $T_{stg}$ | Storage temperature range | | –65°C to 150°C |
| ESD | Electrostatic discharge protection | Human body model MIL-STD-883C | 2 kV |
| | | Charge device model (CDM) | 500 V |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

## DISSIPATING RATING TABLE

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| D-8 | 585.82 mW | 5.8582 mW/°C | 322.2 mW | 234.32 mW |
| D-16 | 898.47 mW | 8.9847 mW/°C | 494.15 mW | 359.38 mW |
| DBV-5 | 308.6419 mW | 3.086419 mW/°C | 169.753 mW | 123.4567 mW |

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{I(IN)}$, $V_{I(INx)}$ | Input voltage | 2.7 | 5.5 | V |
| $V_{I(/ENx)}$, $V_{I(ENx)}$ | Input voltage | 0 | 5.5 | V |
| $I_{O(OUT)}$, $I_{O(OUTx)}$ | Continuous output current | 0 | 250 | mA |
| $T_J$ | Operating virtual junction temperature | -40 | 125 | °C |

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, $I_O$ = 0.25 A, $V_{I(\overline{ENx})}$ = 0 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS(1) | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | | | |
| $r_{DS(on)}$ | Static drain-source on-state resistance, 5-V operation and 3.3-V operation | $V_{I(IN)}$ = 5 V or 3.3 V, $I_O$ = 0.25 A | | –40°C ≤ $T_J$ ≤ 125°C | | 70 | 135 | mΩ |
| | Static drain-source on-state resistance, 2.7-V operation(2) | $V_{I(IN)}$ = 2.7 V, | $I_O$ = 0.25 A | –40°C ≤ $T_J$ ≤ 125°C | | 75 | 150 | mΩ |
| $t_r$(2) | Rise time, output | $V_{I(IN)}$ = 5.5 V | $C_L$ = 1 µF, $R_L$ = 20 Ω | $T_J$ = 25°C | | 0.6 | 1.5 | ms |
| | | $V_{I(IN)}$ = 2.7 V | | | | 0.4 | 1 | |
| $t_f$(2) | Fall time, output | $V_{I(IN)}$ = 5.5 V | | | 0.05 | | 0.5 | |
| | | $V_{I(IN)}$ = 2.7 V | | | 0.05 | | 0.5 | |
| **ENABLE INPUT $\overline{ENx}$** | | | | | | | | |
| $V_{IH}$ | High-level input voltage | 2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | 2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V | | | | | 0.8 | |
| $I_I$ | Input current | $V_{I(/ENx)}$ = 0 V or 5.5 V | | | -0.5 | | 0.5 | µA |
| $t_{on}$(2) | Turnon time | $C_L$ = 100 µF, $R_L$ = 20 Ω | | | | | 3 | ms |
| $t_{off}$(2) | Turnoff time | $C_L$ = 100 µF, $R_L$ = 20 Ω | | | | | 10 | |
| **CURRENT LIMIT** | | | | | | | | |
| $I_{OS}$ | Short-circuit output current | $V_{I(IN)}$ = 5 V, OUT connected to GND, device enabled into short-circuit | | | 0.3 | 0.5 | 0.7 | A |
| **SUPPLY CURRENT (TPS2045B, TPS2055B)** | | | | | | | | |
| | Supply current, low-level output | No load on OUT, $V_{I(/ENx)}$ = 5.5 V or $V_{I(/ENx)}$ = 0 V | | $T_J$ = 25°C | | 0.5 | 1 | µA |
| | | | | –40°C ≤ $T_J$ ≤ 125°C | | 0.5 | 5 | |
| | Supply current, high-level output | No load on OUT, $V_{I(/ENx)}$ = 0 V or $V_{I(/ENx)}$ = 5.5 V | | $T_J$ = 25°C | | 43 | 60 | µA |
| | | | | –40°C ≤ $T_J$ ≤ 125°C | | 43 | 70 | |
| | Leakage current | OUT connected to ground, $V_{I(/ENx)}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V | | –40°C ≤ $T_J$ ≤ 125°C | | 1 | | µA |
| | Reverse leakage current | $V_{I(OUTx)}$ = 5.5 V, IN = ground(2) | | $T_J$ = 25°C | | 0 | | µA |
| **SUPPLY CURRENT (TPS2046B)** | | | | | | | | |
| Supply current, low-level output | | No load on OUT, $V_{I(/ENx)}$ = 5.5 V | | $T_J$ = 25°C | | 0.5 | 1 | µA |
| | | | | –40°C ≤ $T_J$ ≤ 125°C | | 0.5 | 5 | |
| Supply current, high-level output | | No load on OUT, $V_{I(/ENx)}$ = 0 V | | $T_J$ = 25°C | | 50 | 70 | µA |
| | | | | -40°C ≤ $T_J$ ≤ 125°C | | 50 | 90 | |
| Leakage current | | OUT connected to ground, $V_{I(ENx)}$ = 5.5 V | | -40°C ≤ $T_J$ ≤ 125°C | | 1 | | µA |
| Reverse leakage current | | $V_{I(OUTx)}$ = 5.5 V, IN = ground(2) | | $T_J$ = 25°C | | 0.2 | | µA |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Not tested in production, specified by design.

## ELECTRICAL CHARACTERISTICS (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, $I_O$ = 0.25 A, $V_{I(\overline{ENx})}$ = 0 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS(1) | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT (TPS2047B)** | | | | | | |
| Supply current, low-level output | No load on OUT, $V_{I(/ENx)}$ = 5.5 V | $T_J$ = 25°C | | 0.5 | 2 | µA |
| | | –40°C ≤ $T_J$ ≤ 125°C | | 0.5 | 10 | |
| Supply current, high-level output | No load on OUT, $V_{I(/ENx)}$ = 0 V | $T_J$ = 25°C | | 65 | 90 | µA |
| | | –40°C ≤ $T_J$ ≤ 125°C | | 65 | 110 | |
| Leakage current | OUT connected to ground, $V_{I(/ENx)}$ = 5.5 V | –40°C≤ $T_J$≤ 125°C | | 1 | | µA |
| Reverse leakage current | $V_{I(OUTx)}$ = 5.5 V, INx = ground(3) | $T_J$ = 25°C | | 0.2 | | µA |
| **UNDERVOLTAGE LOCKOUT** | | | | | | |
| Low-level input voltage, IN, INx | | | 2 | | 2.5 | V |
| Hysteresis, IN, INx | $T_J$ = 25°C | | | 75 | | mV |
| **OVERCURRENT $\overline{OC}$ and $\overline{OCx}$** | | | | | | |
| Output low voltage, $V_{OL(/OCx)}$ | $I_{O(/OCx)}$ = 5 mA | | | | 0.4 | V |
| Off-state current(3) | $V_{O(/OCx)}$ = 5 V or 3.3 V | | | | 1 | µA |
| $\overline{OC}$ deglitch(3) | $\overline{OCx}$ assertion or deassertion | | 4 | 8 | 15 | ms |
| **THERMAL SHUTDOWN(4)** | | | | | | |
| Thermal shutdown threshold(3) | | | 135 | | | °C |
| Recovery from thermal shutdown(3) | | | 125 | | | °C |
| Hysteresis(3) | | | | 10 | | °C |

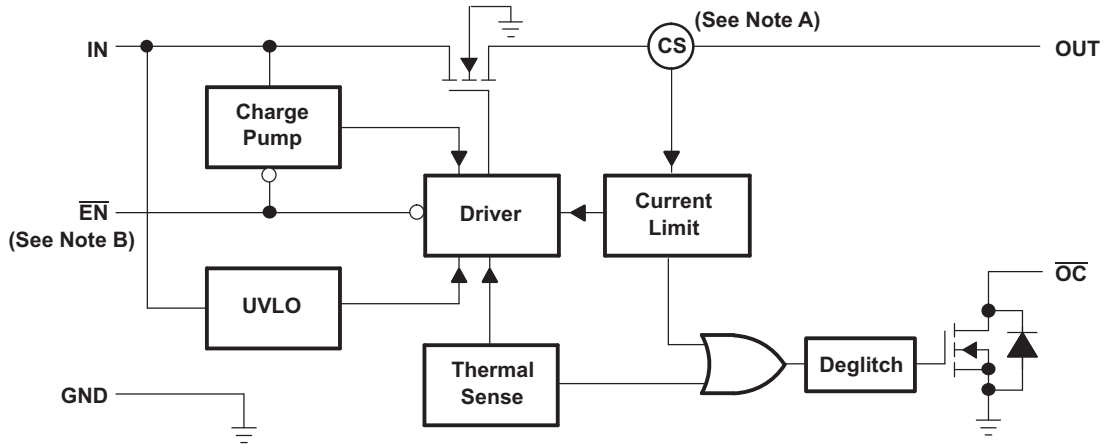
(3) Not tested in production, specified by design.
(4) The thermal shutdown only reacts under overcurrent conditions.

## DEVICE INFORMATION

### Terminal Functions (TPS2045B and TPS2055B)

| TERMINAL | | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|---|
| | D PACKAGE | | DBV PACKAGE | | | |
| NAME | TPS2045B | TPS2055B | TPS2045B | TPS2055B | | |
| $\overline{EN}$ | 4 | - | 4 | - | I | Enable input, logic low turns on power switch |
| EN | - | 4 | - | 4 | I | Enable input, logic high turns on power switch |
| GND | 1 | 1 | 2 | 2 | | Ground |
| IN | 2, 3 | 2, 3 | 5 | 5 | I | Input voltage |
| $\overline{OC}$ | 5 | 5 | 3 | 3 | O | Overcurrent open-drain output, active-low |
| OUT | 6, 7, 8 | 6, 7, 8 | 1 | 1 | O | Power-switch output |

### FUNCTIONAL BLOCK DIAGRAM (TPS2045B and TPS2055B)



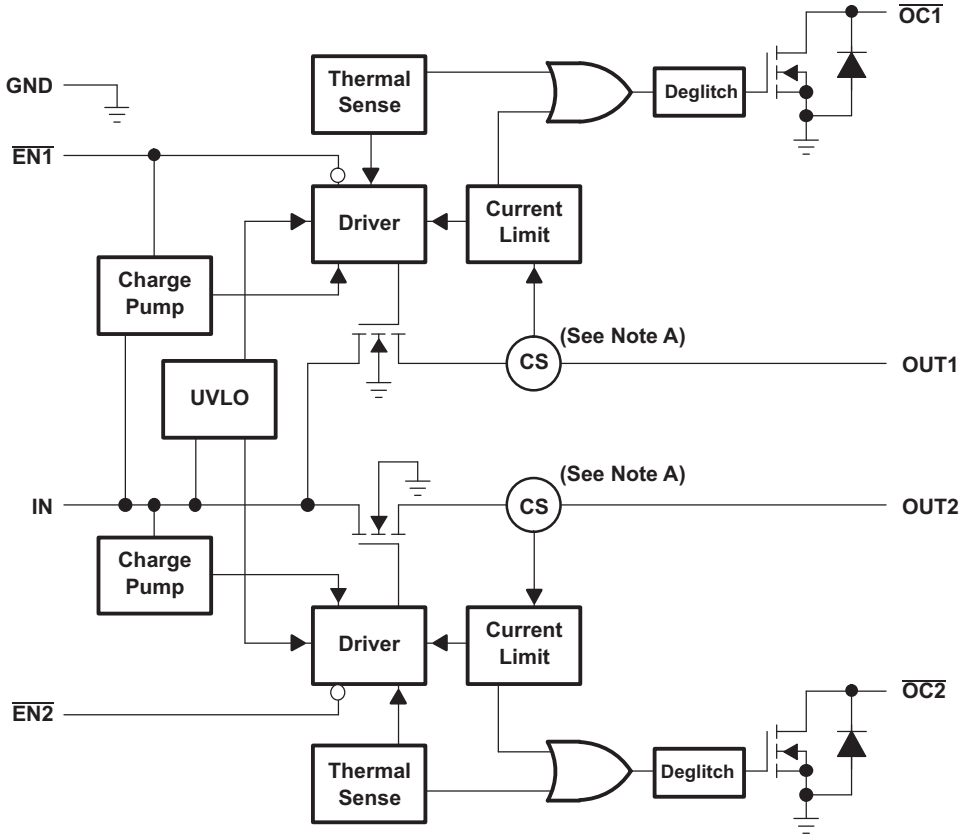

A. Current sense

B. Active low ($\overline{EN}$) for TPS2045B. Active high (EN) for TPS2055B.

## Terminal Functions (TPS2046B)

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| $\overline{EN1}$ | 3 | I | Enable input, logic low turns on power switch IN-OUT1 |
| $\overline{EN2}$ | 4 | I | Enable input, logic low turns on power switch IN-OUT2 |
| GND | 1 | | Ground |
| IN | 2 | I | Input voltage |
| $\overline{OC1}$ | 8 | O | Overcurrent, open-drain output, active low, IN-OUT1 |
| $\overline{OC2}$ | 5 | O | Overcurrent, open-drain output, active low, IN-OUT2 |
| OUT1 | 7 | O | Power-switch output, IN-OUT1 |
| OUT2 | 6 | O | Power-switch output, IN-OUT2 |

## FUNCTIONAL BLOCK DIAGRAM (TPS2046B)

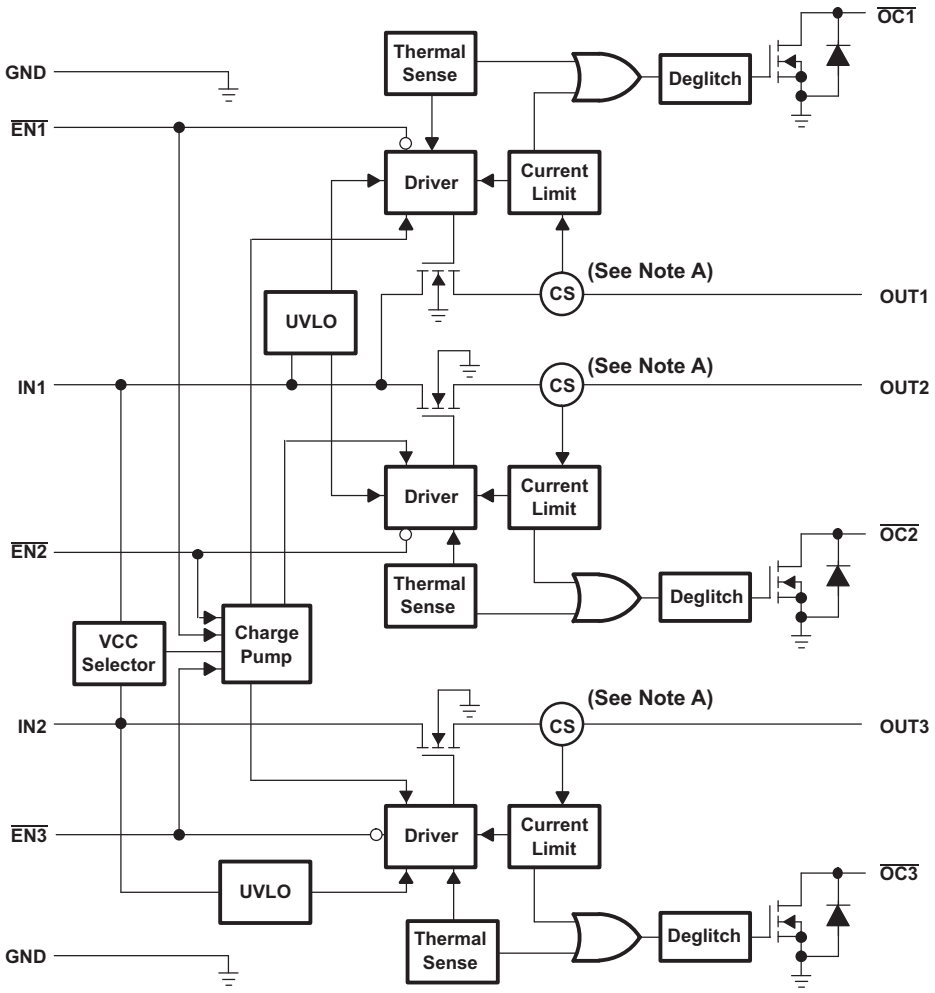



A. Current sense

## Terminal Functions (TPS2047B)

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| $\overline{EN1}$ | 3 | I | Enable input, logic low turns on power switch IN1-OUT1 |
| $\overline{EN2}$ | 4 | I | Enable input, logic low turns on power switch IN1-OUT2 |
| $\overline{EN3}$ | 7 | I | Enable input, logic low turns on power switch IN2-OUT3 |
| GND | 1, 5 | | Ground |
| IN1 | 2 | I | Input voltage for OUT1 and OUT2 |
| IN2 | 6 | I | Input voltage for OUT3 |
| NC | 8, 9, 10 | | No connection |
| $\overline{OC1}$ | 16 | O | Overcurrent, open-drain output, active low, IN1-OUT1 |
| $\overline{OC2}$ | 13 | O | Overcurrent, open-drain output, active low, IN1-OUT2 |
| $\overline{OC3}$ | 12 | O | Overcurrent, open-drain output, active low, IN2-OUT3 |
| OUT1 | 15 | O | Power-switch output, IN1-OUT1 |
| OUT2 | 14 | O | Power-switch output, IN1-OUT2 |
| OUT3 | 11 | O | Power-switch output, IN2-OUT3 |

## FUNCTIONAL BLOCK DIAGRAM (TPS2047B)




A. Current sense

## PARAMETER MEASUREMENT INFORMATION

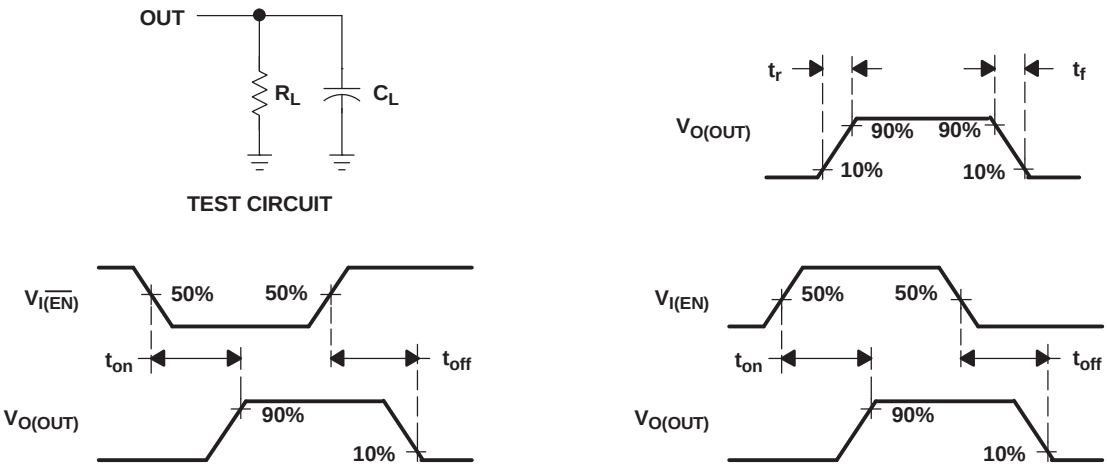



**Figure 1. Test Circuit and Voltage Waveforms**

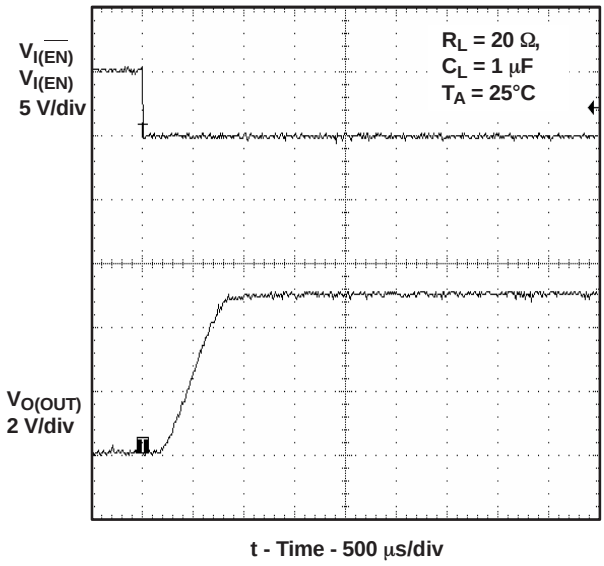



**Figure 2. Turnon Delay and Rise Time With 1-µF Load**

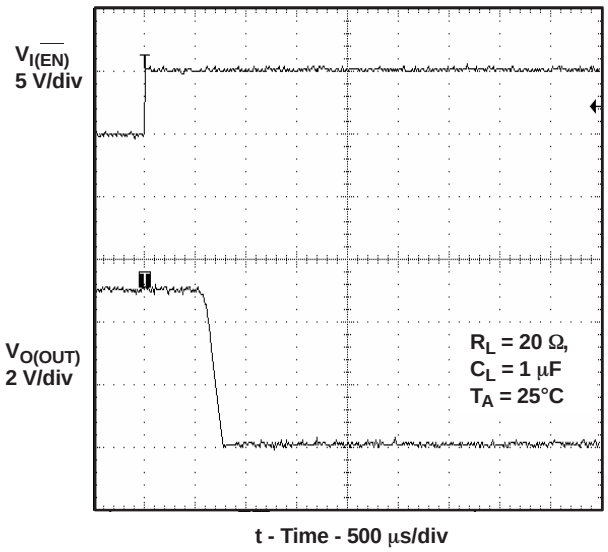



**Figure 3. Turnoff Delay and Fall Time With 1-µF Load**

## PARAMETER MEASUREMENT INFORMATION (continued)

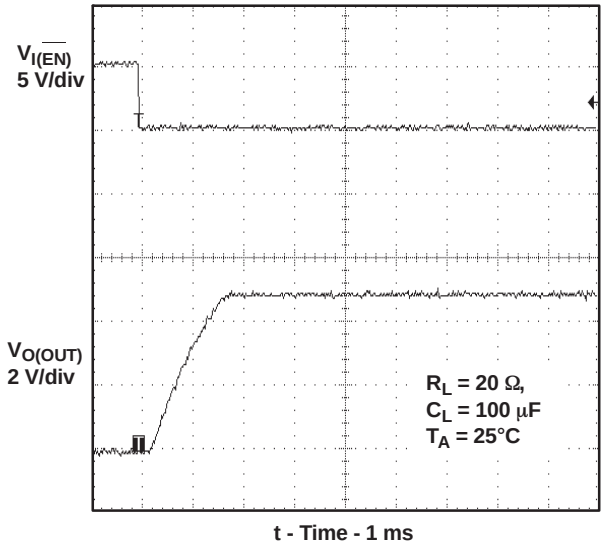



Figure 4. Turnon Delay and Rise Time With 100-μF Load

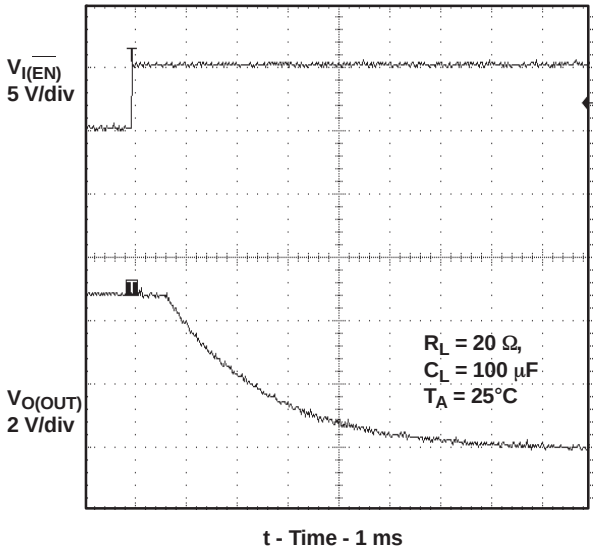



Figure 5. Turnoff Delay and Fall Time With 100-μF Load

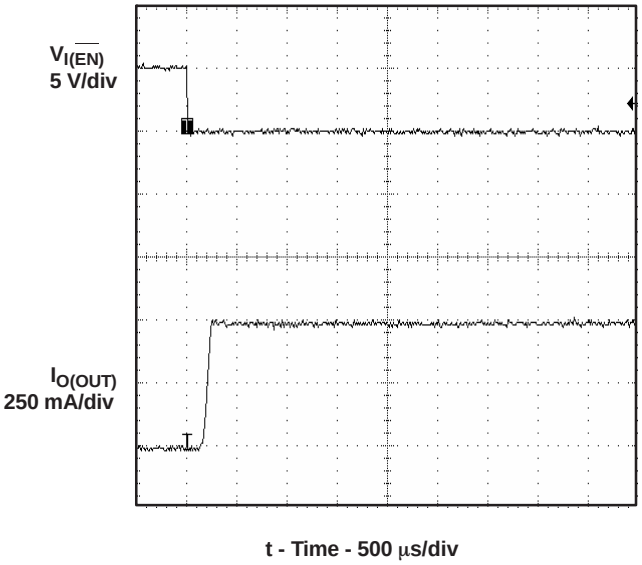



Figure 6. Short-Circuit Current, Device Enabled Into Short

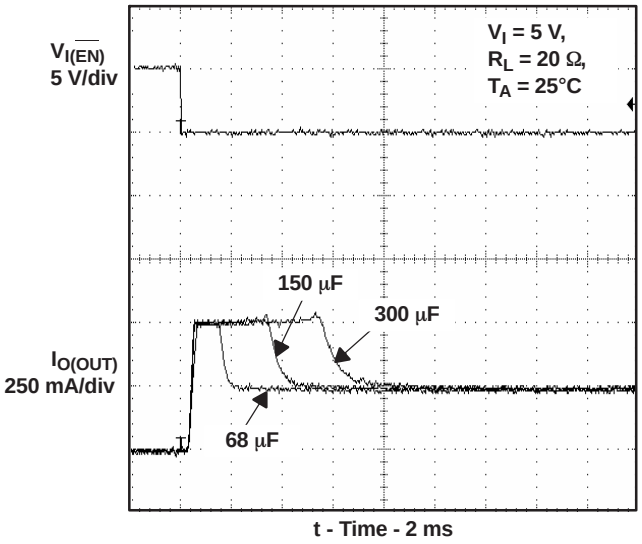



Figure 7. Inrush Current With Different Load Capacitance

## PARAMETER MEASUREMENT INFORMATION (continued)

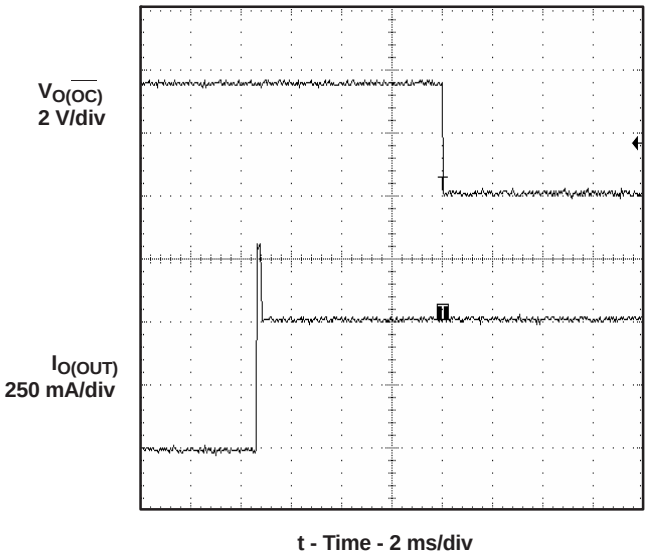



Figure 8. 4-Ω Load Connected to Enabled Device

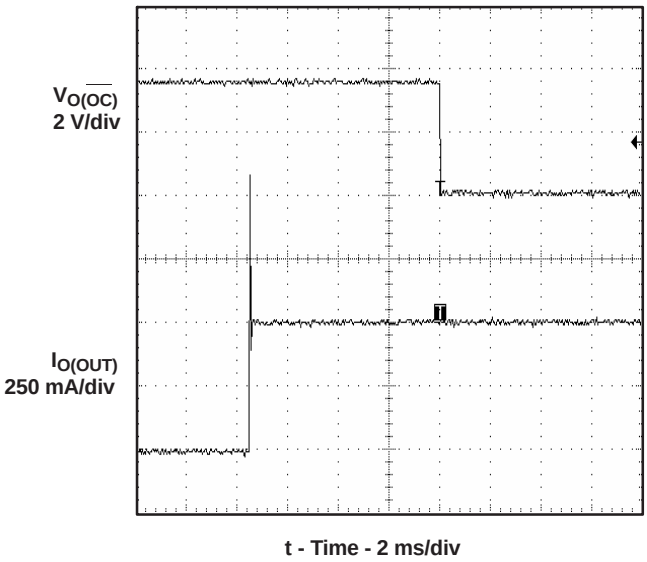



Figure 9. 3-Ω Load Connected to Enabled Device

## TYPICAL CHARACTERISTICS

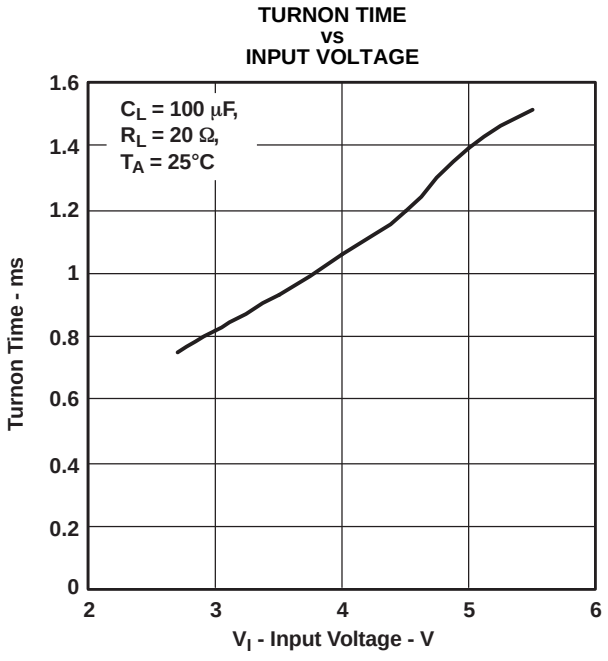



Figure 10.

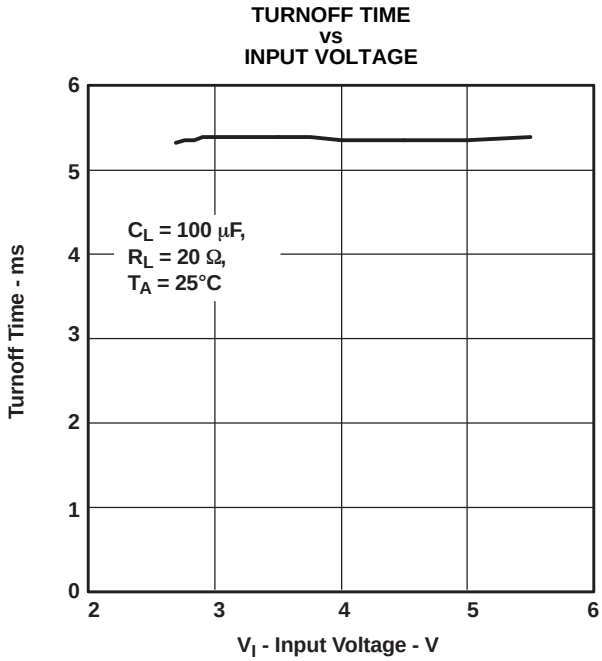



Figure 11.

## TYPICAL CHARACTERISTICS (continued)

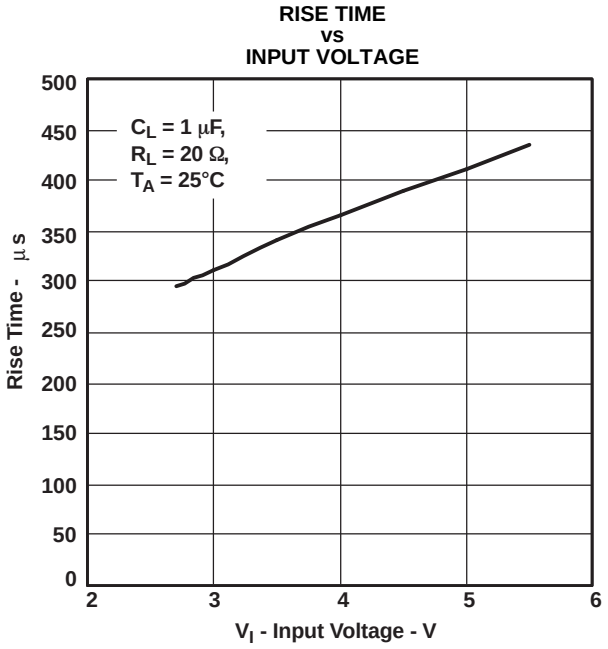



Figure 12.

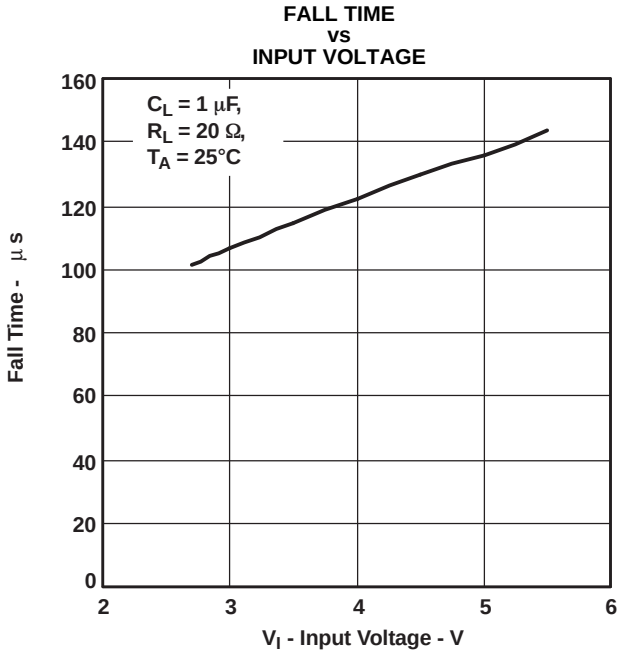



Figure 13.

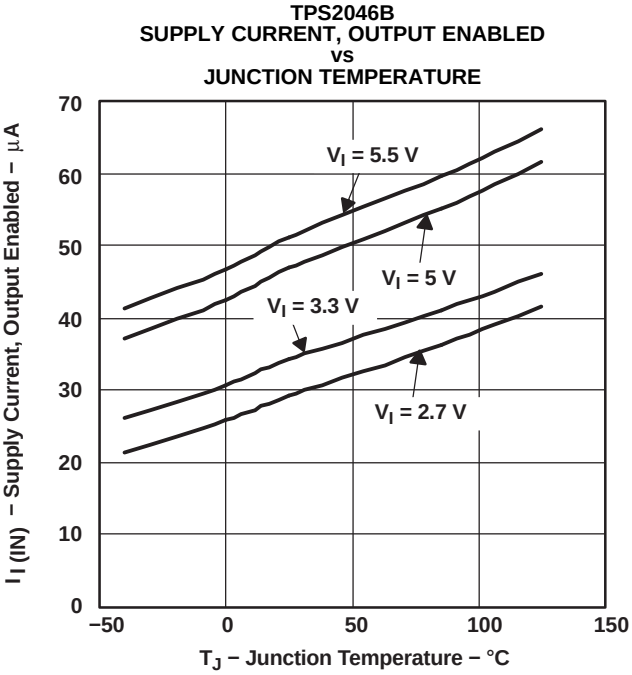



Figure 14.

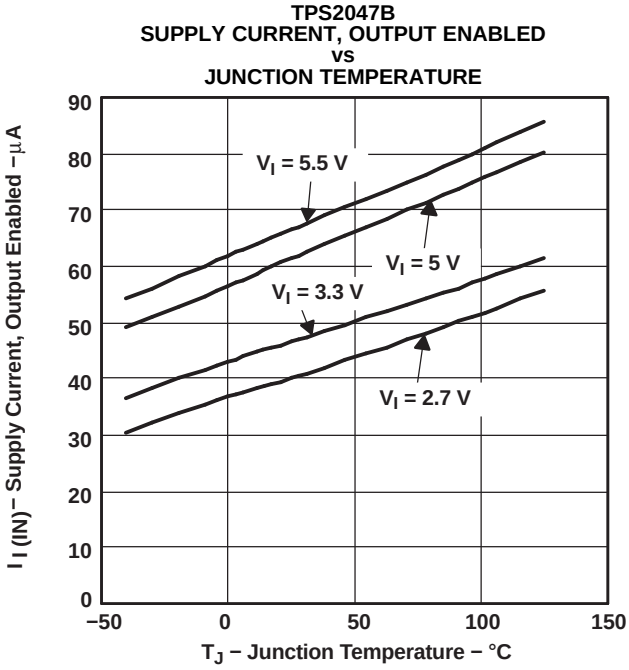



Figure 15.

## TYPICAL CHARACTERISTICS (continued)

TPS2046B
SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

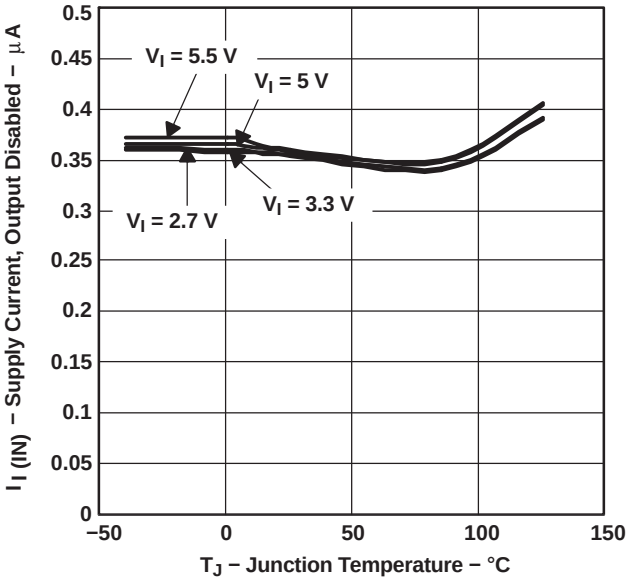



Figure 16.

TPS2047B
SUPPLY CURRENT, OUTPUT DISABLED
vs
JUNCTION TEMPERATURE

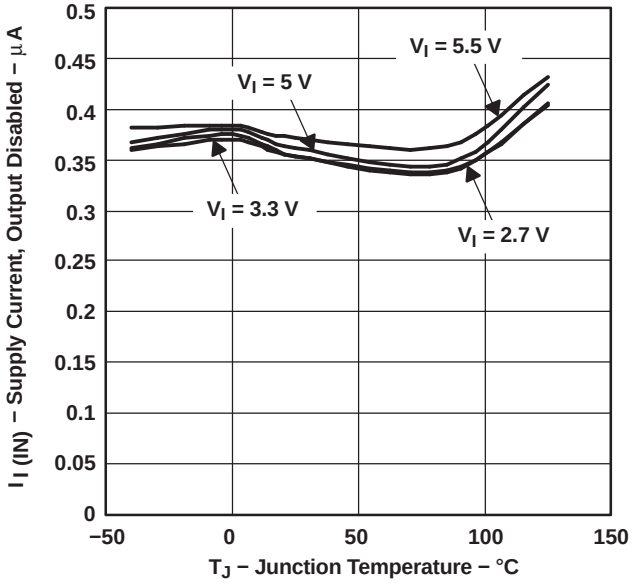



Figure 17.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

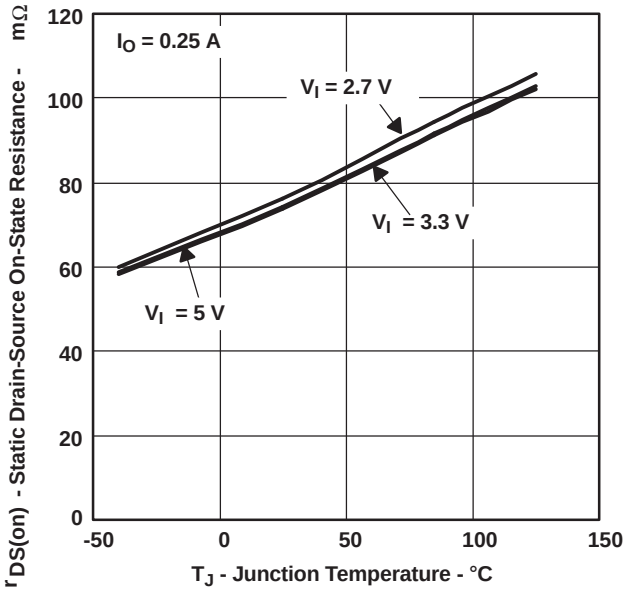



Figure 18.

SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

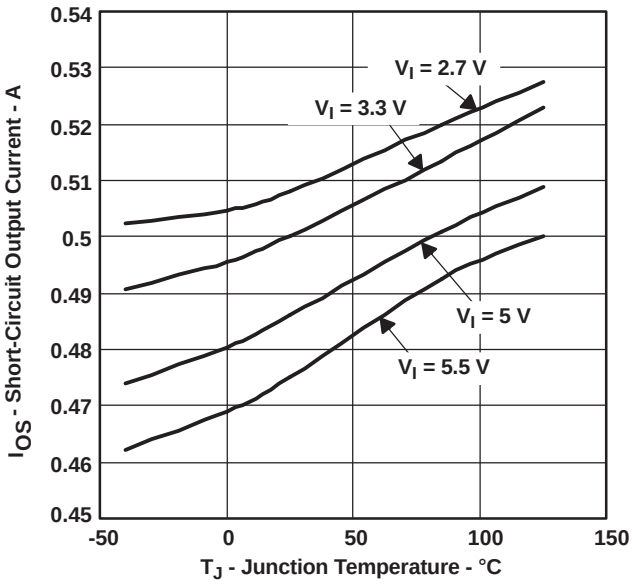



Figure 19.

## TYPICAL CHARACTERISTICS (continued)

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

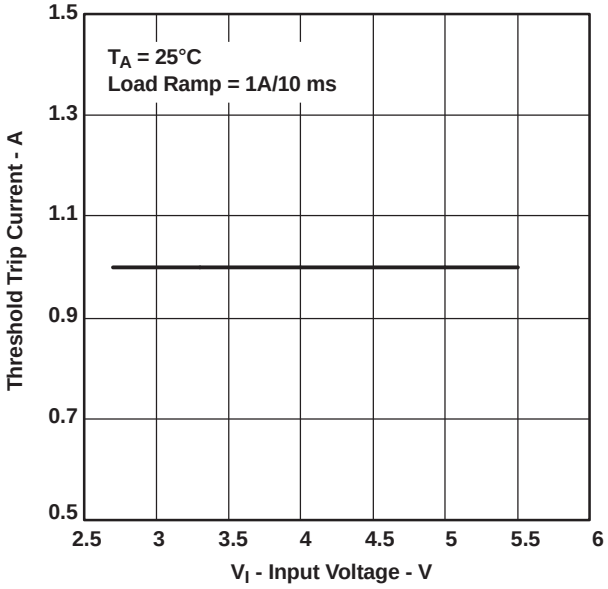



Figure 20.

UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE

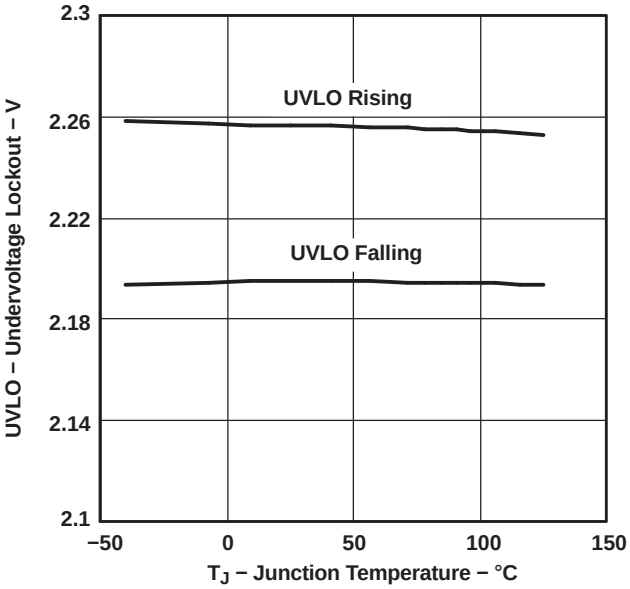



Figure 21.

CURRENT-LIMIT RESPONSE
vs
PEAK CURRENT

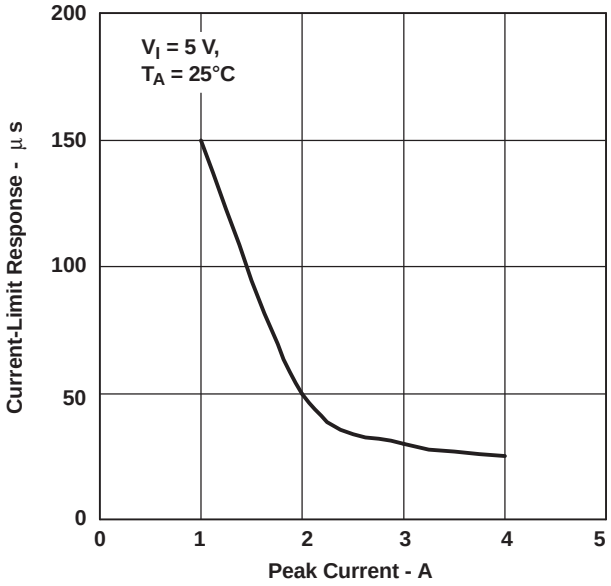



Figure 22.

## APPLICATION INFORMATION

### POWER-SUPPLY CONSIDERATIONS

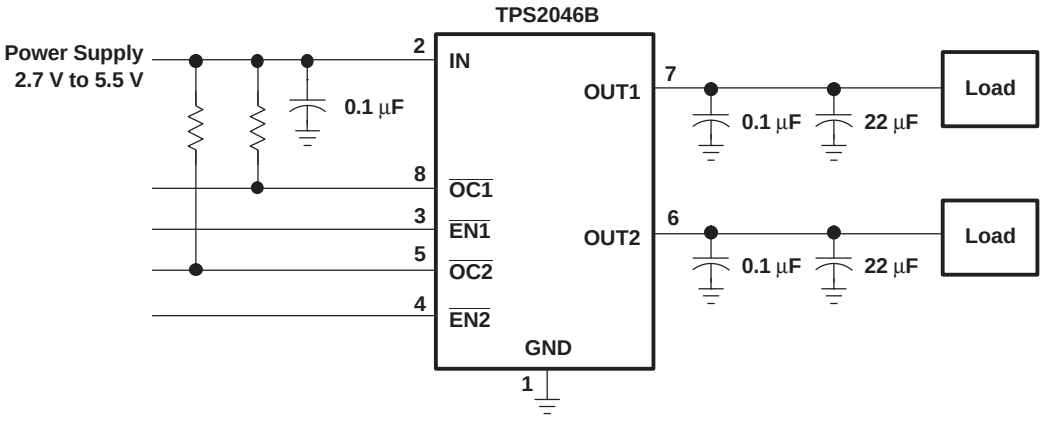



**Figure 23. Typical Application (Example, TPS2046B)**

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

### OVERCURRENT

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS204xB/TPS2055B senses the short, and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The TPS204xB/TPS2055B is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

### $\overline{\text{OC}}$ RESPONSE

The $\overline{\text{OC}}$x open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{\text{OC}}$x occurs due to the 10-ms deglitch circuit. The TPS204xB/TPS2055B is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{\text{OC}}$x is not deglitched when the switch is turned off due to an overtemperature shutdown.

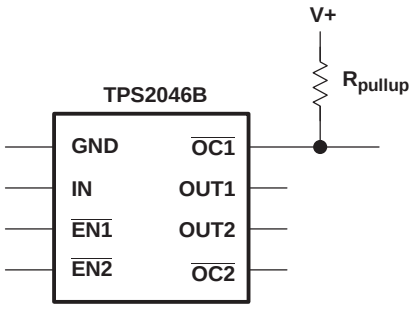



**Figure 24. Typical Circuit for the $\overline{OC}$ Pin (Example, TPS2046B)**

## POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 18. Using this value, the power dissipation per switch can be calculated by:

- $P_D = r_{DS(on)} \times I^2$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature:

- $T_J = P_D \times R_{\theta JA} + T_A$

Where:

- $T_A$= Ambient temperature °C
- $R_{\theta JA}$ = Thermal resistance
- $P_D$ = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

## THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS204xB/TPS2055B implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{OCx}$ open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

## UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

## UNIVERSAL SERIAL BUS (USB) APPLICATIONS

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS204xB/TPS2055B can provide-power distribution solutions to many of these classes of devices.

## HOST/SELF-POWERED AND BUS-POWERED HUBS

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports. This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

## LOW-POWER BUS-POWERED AND HIGH-POWER BUS-POWERED FUNCTIONS

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 25).

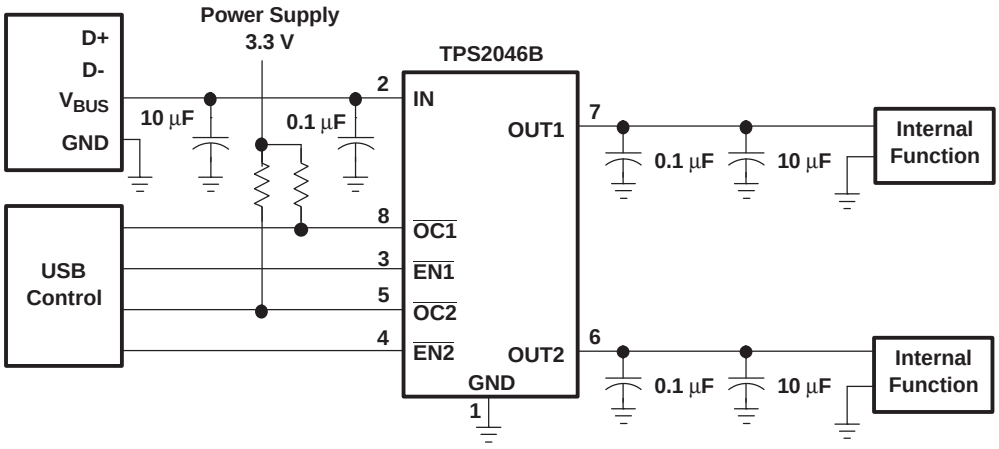


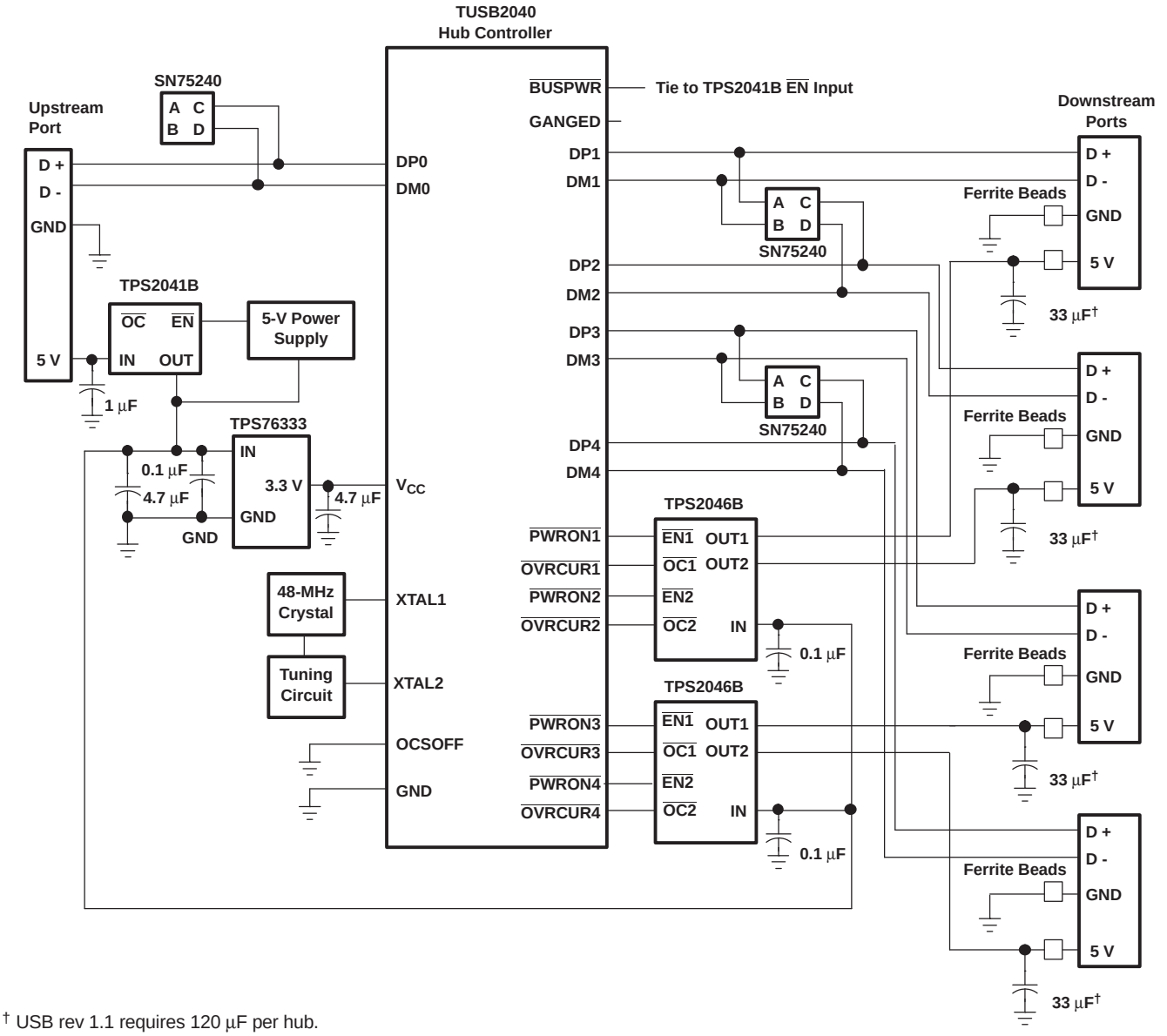

**Figure 25. High-Power Bus-Powered Function (Example, TPS2046B)**

## USB POWER-DISTRIBUTION REQUIREMENTS

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

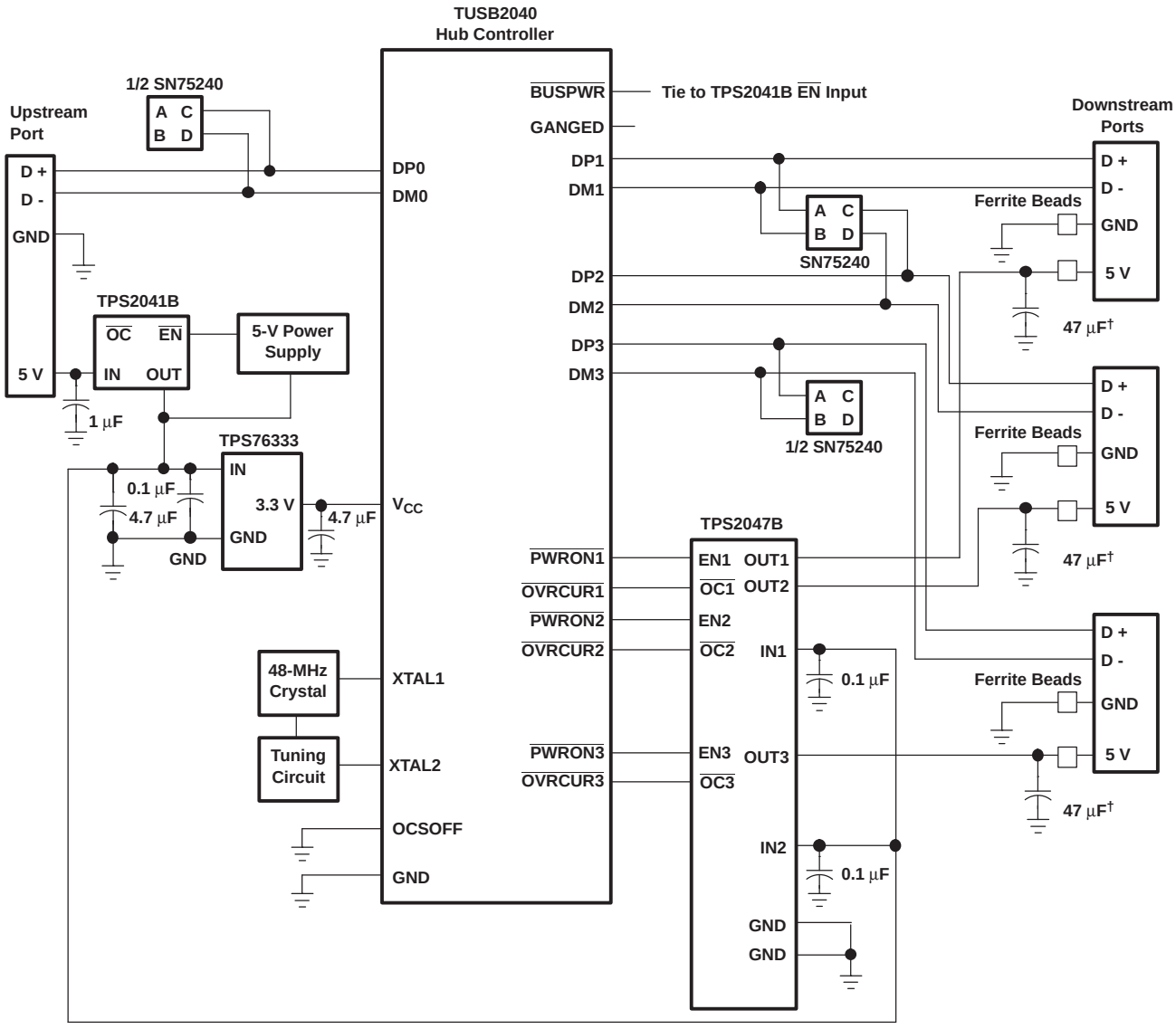
- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB $V_{BUS}$
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS204xB/TPS2055B allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see Figure 26 through Figure 27).




† USB rev 1.1 requires 120 µF per hub.

**Figure 26. Hybrid Self/Bus-Powered Hub Implementation, TPS2046B**




† USB rev 1.1 requires 120 µF per hub.

**Figure 27. Hybrid Self / Bus-Powered Hub Implementation, TPS2047B**

## GENERIC HOT-PLUG APPLICATIONS

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS204xB/TPS2055B, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS204xB/TPS2055B also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

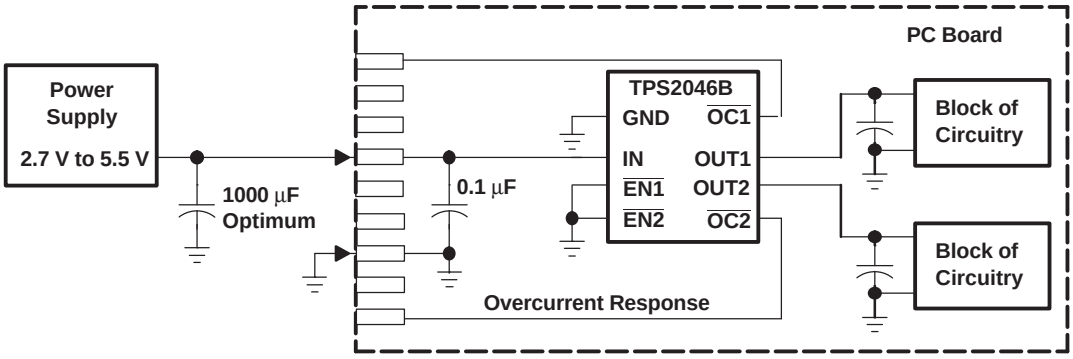



**Figure 28. Typical Hot-Plug Implementation (Example, TPS2046B)**

By placing the TPS204xB/TPS2055B between the $V_{CC}$ input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

# DETAILED DESCRIPTION

## POWER SWITCH

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 250 mA.

## CHARGE PUMP

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

## DRIVER

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

## ENABLE ($\overline{EN}$x)

The logic enable pin disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA or 2 µA when a logic high is present on $\overline{EN}$. A logic zero input on $\overline{EN}$ restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

## ENABLE (ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 μA or 2 μA when a logic low is present on ENx. A logic high input on ENx restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

## OVERCURRENT ($\overline{OCx}$)

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{OCx}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{OCx}$ is asserted instantaneously.

## CURRENT SENSE

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

## THERMAL SENSE

The TPS204xB/TPS2055B implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ($\overline{OCx}$) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

## UNDERVOLTAGE LOCKOUT

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS2046BD | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2046B |
| TPS2046BD.A | Active | Production | SOIC (D) \| 8 | 75 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2046B |
| TPS2046BDR | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2046B |
| TPS2046BDR.A | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2046B |
| TPS2047BD | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2047B |
| TPS2047BD.A | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2047B |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

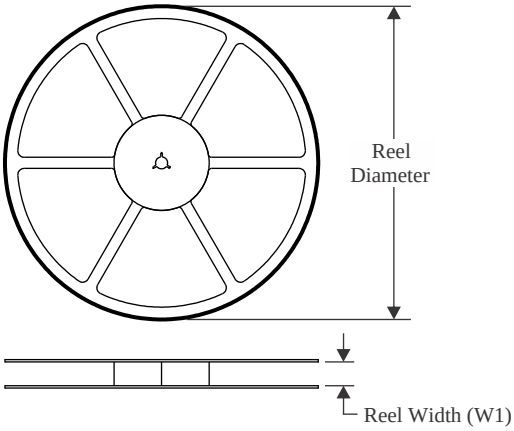
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

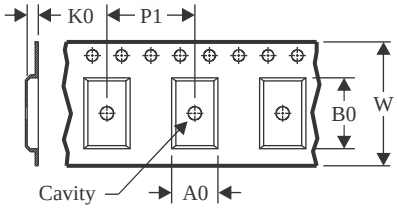
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

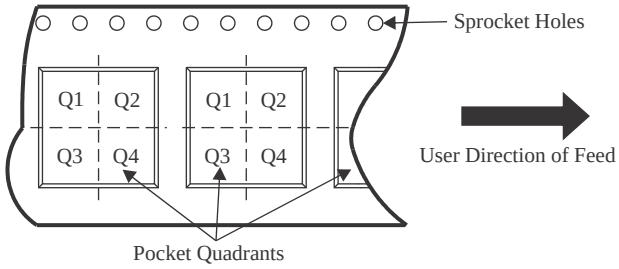



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

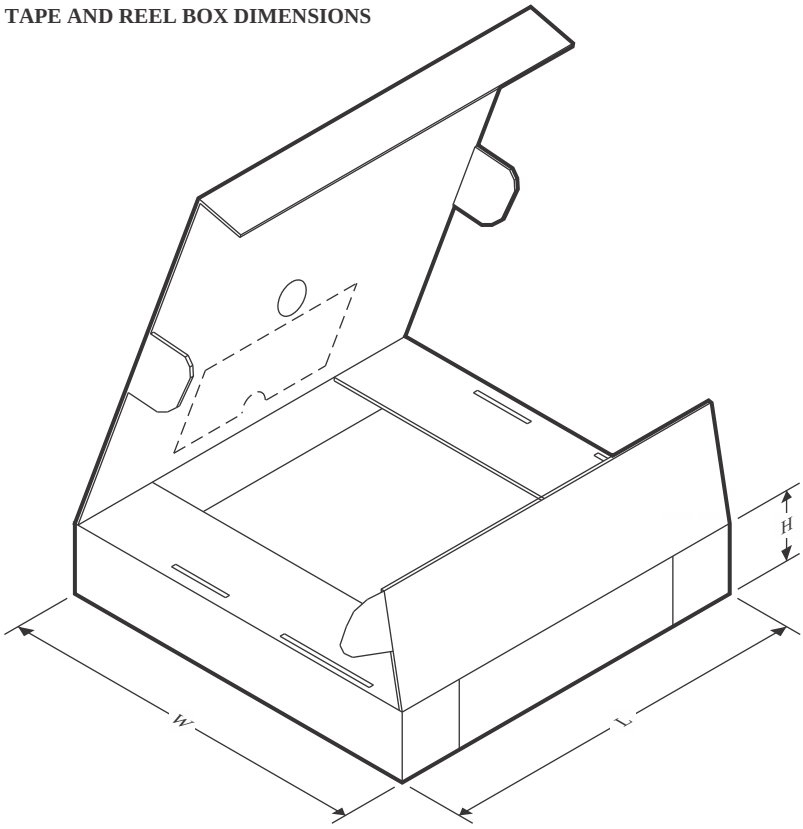
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2046BDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

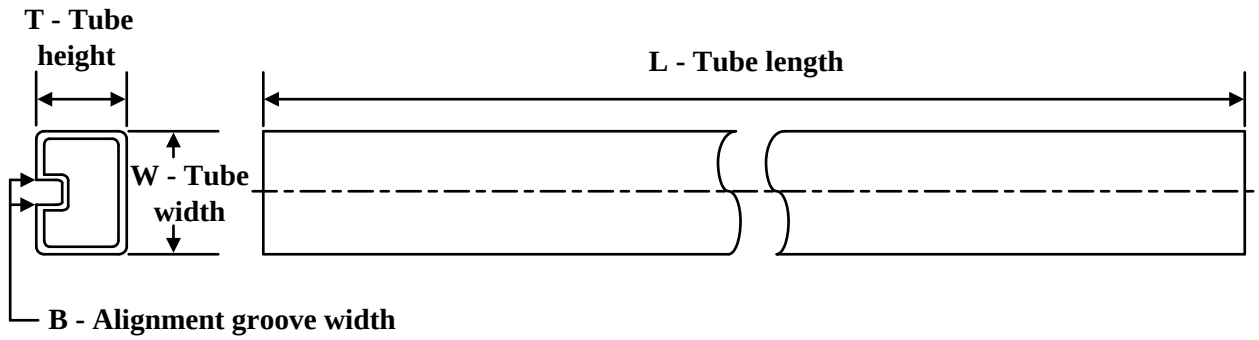
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS2046BDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

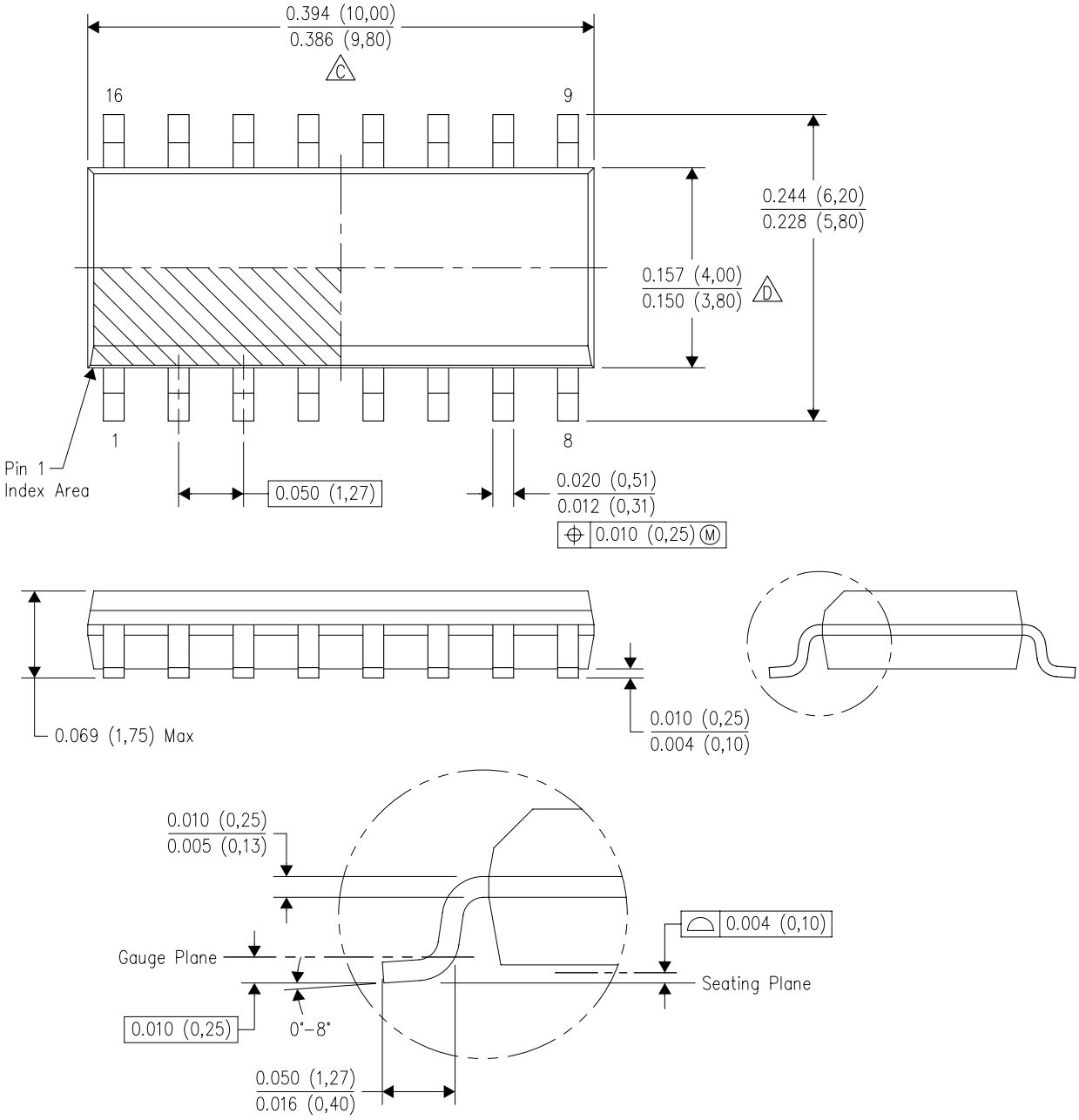
## TUBE



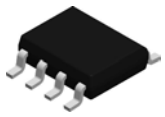

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPS2046BD | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TPS2046BD.A | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TPS2047BD | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| TPS2047BD.A | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

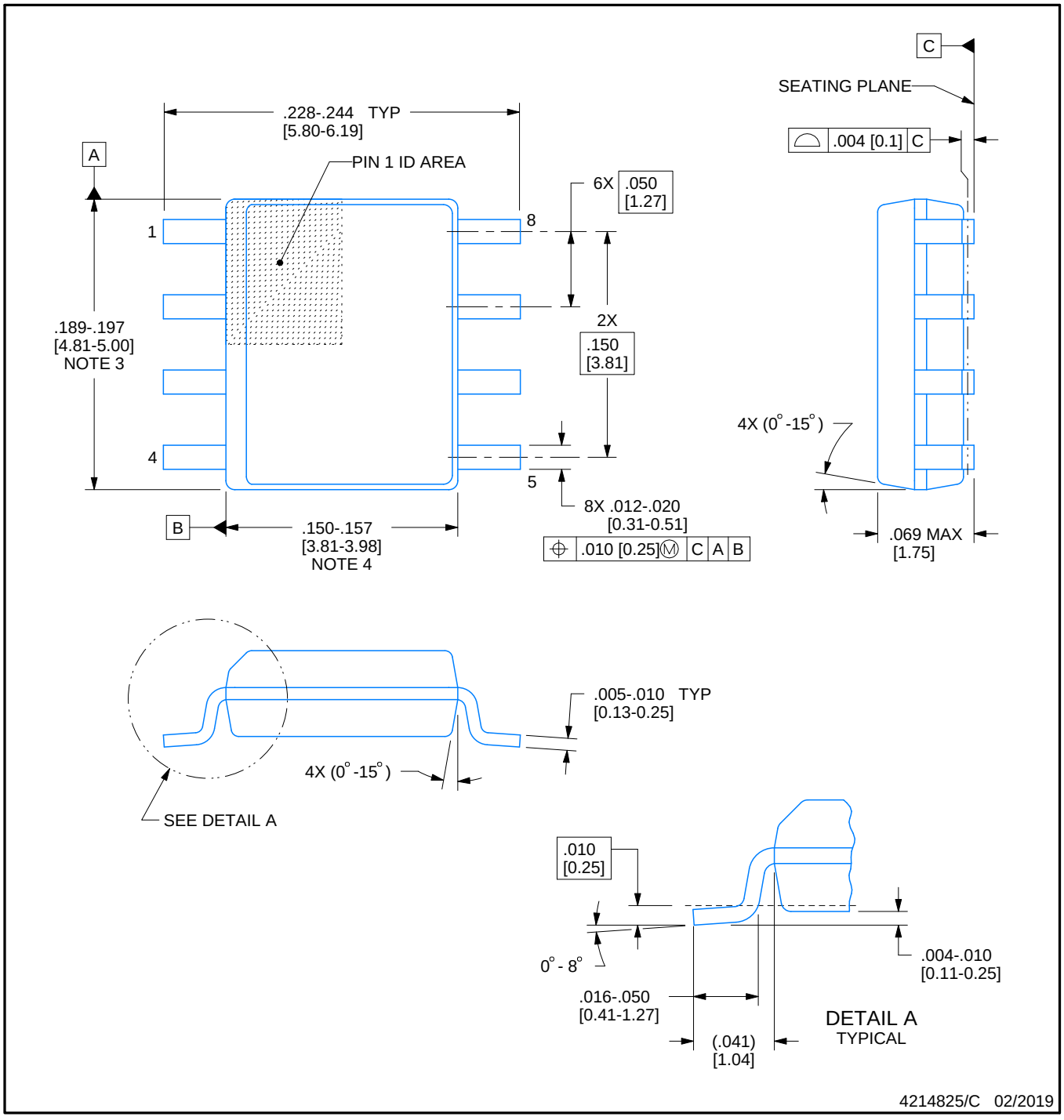


# PACKAGE OUTLINE

## D0008A

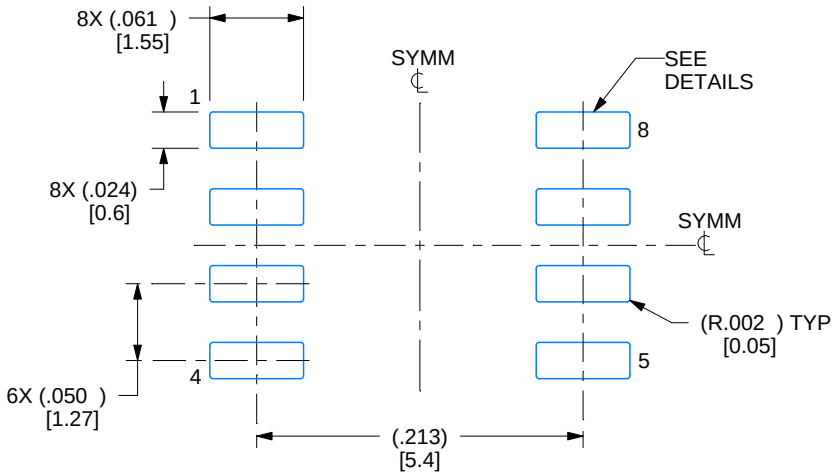
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

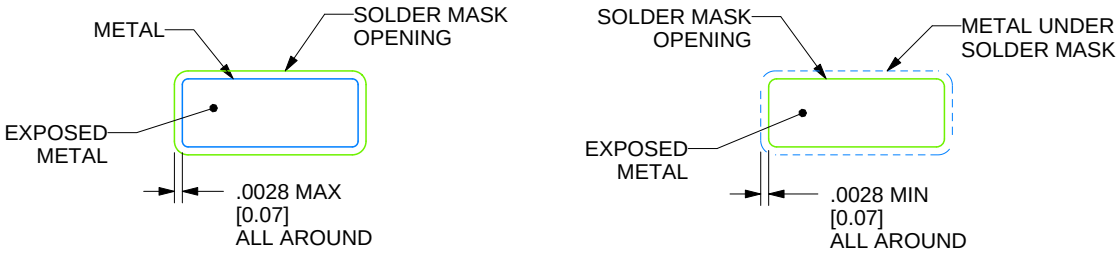



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

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NOTES: (continued)

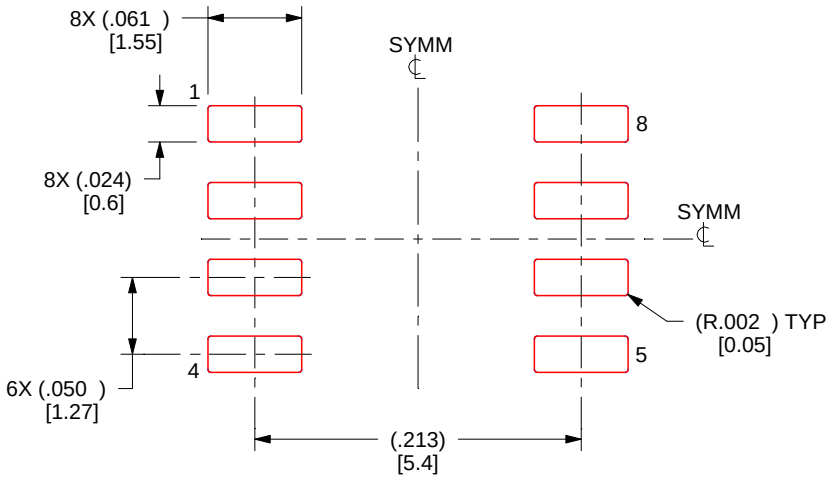
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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