具有受控上升时间的 TPS22919 5.5V、1.5A、90mΩ 自保护负载开关

1 特性

- 输入工作电压范围 (V_{IN})：
  1.6V 至 5.5V
- 最大持续电流 (I_{MAX})：1.5A
- 导通电阻 (R_{ON})：
  - 5V V_{IN}：89mΩ（典型值）
  - 3.6V V_{IN}：90mΩ（典型值）
  - 1.8V V_{IN}：105mΩ（典型值）
- 输出短路保护 (I_{SC})：3A（典型值）
- 低功耗：
  - 导通状态 (I_Q)：8μA（典型值）
  - 关断状态 (I_{SD})：2nA（典型值）
- 智能 ON 引脚下拉电阻 (R_{PD})：
  - ON ≥ V_{IH} (I_{ON})：100nA（最大值）
  - ON ≤ V_{IL} (R_{PD})：530kΩ（典型值）
- 可限制浪涌电流的慢速导通时序 (t_{ON})：
  - 5.0V 导通时间 (t_{ON})：
    3.2mV/μs 下为 1.95ms
  - 3.6V 导通时间 (t_{ON})：
    2.7mV/μs 下为 1.75ms
  - 1.8V 导通时间 (t_{ON})：
    1.8mV/μs 下为 1.5ms
- 可调节输出放电和下降时间：
  - 内部 QOD 电阻 = 24Ω（典型值）

2 应用

- 个人电子产品
- 机顶盒
- 高清电视
- 多功能打印机

3 说明

TPS22919 器件是一款具有受控压摆率的小型单通道负载开关。此器件包含一个可在 1.6V 至 5.5V 输入电压范围内运行的 N 沟道 MOSFET，并且支持 1.5A 的最大持续电流。

开关导通状态由数字输入控制，此输入可与低压控制信号直接连接。首次加电时，此器件使用智能下拉电阻来保持 ON 引脚不悬空，直到系统定序完成。故意将该引脚驱动为高电平 (>V_{IH}) 之后，便会断开智能下拉电阻，以防止不必要的功率损耗。

TPS22919 负载开关也是自保护的，这意味着它可以保护自己免受器件输出上短路事件的影响。它还具有热关断功能，可防止因过热而造成任何损坏。

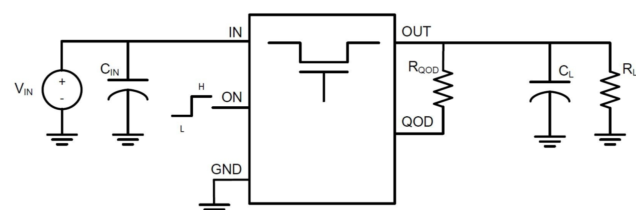
TPS22919 采用标准 SC-70 封装，工作结温范围为 –40°C 至 125°C。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TPS22919DCK	SC-70 (6)	2.1mm × 2.0mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



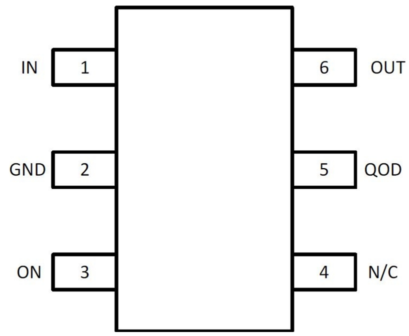
目录

4 修订历史记录

Changes from Original (October 2018) to Revision A	**Page**
• 已更改 将“预告信息”更改为“生产数据”	1

5 Pin Configuration and Functions

DCK Package
6-Pin SC-70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input.
2	GND	—	Device ground.
3	ON	I	Active high switch control input. Do not leave floating.
4	NC	—	No connect pin, leave floating.
5	QOD	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways. • Placing an external resistor between VOUT and QOD • Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) • Disabling QOD by leaving pin floating See the *Fall Time (t_{FALL}) and Quick Output Discharge (QOD)* section for more information.
6	VOUT	O	Switch output.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range	–0.3	6	V
V_{OUT}	Maximum Output Voltage Range	–0.3	6	V
V_{ON}	Maximum ON Pin Voltage Range	–0.3	6	V
V_{QOD}	Maximum QOD Pin Voltage Range	–0.3	6	V
I_{MAX}	Maximum Continuous Current		1.5	A
I_{PLS}	Maximum Pulsed Current (2 ms, 2% Duty Cycle)		2.5	A
T_J	Junction temperature	Internally Limited		°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead Temperature (10 s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less is possible with the necessary precautions. Pins listed may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range	1.6		5.5	V
V_{OUT}	Output Voltage Range	0		5.5	V
V_{IH}	ON Pin High Voltage Range	1		5.5	V
V_{IL}	ON Pin Low Voltage Range	0		0.35	V

6.4 Thermal Information

THERMAL METRIC(1)		TPS22919	UNIT
		DCK (SC-70)	
		PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	142.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	52.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	68.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Typical values at VIN = 3.6V unless otherwise specified

PARAMETER	TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT
Input Supply (VIN)						

Electrical Characteristics (continued)

Typical values at VIN = 3.6V unless otherwise specified

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
$I_{Q,\ VIN}$	VIN Quiescent Current	$V_{ON} \geq V_{IH}$, VOUT = Open		25°C		8	15	µA
				-40°C to 125°C			20	µA
$I_{SD,\ VIN}$	VIN Shutdown Current	$V_{ON} \leq V_{IL}$, VOUT = GND		25°C		2	20	nA
				-40°C to 125°C			800	nA
ON-Resistance (RON)								
R_{ON}	ON-State Resistance	I_{OUT} = -200 mA	V_{IN} = 5 V	25°C		89	125	mΩ
				-40°C to 85°C			150	mΩ
				-40°C to 105°C			175	mΩ
				-40°C to 125°C			200	mΩ
			V_{IN} = 3.6 V	25°C		90	150	mΩ
				-40°C to 85°C			200	mΩ
				-40°C to 105°C			225	mΩ
				-40°C to 125°C			250	mΩ
			V_{IN} = 1.8 V	25°C		105	300	mΩ
				-40°C to 85°C			400	mΩ
				-40°C to 105°C			450	mΩ
				-40°C to 125°C			500	mΩ
Output Short Protection (ISC)								
I_{SC}	Short Circuit Current Limit	$V_{OUT} \leq V_{IN}$ - 1.5 V		-40°C to 125°C		3		A
		$V_{OUT} \leq V_{SC}$		-40°C to 125°C	30			mA
V_{SC}	Output Short Detection Threshold	V_{IN} - V_{OUT}		-40°C to 125°C	0.3	0.36	0.46	V
t_{SC}	Output Short Reponse Time	V_{IN} = 1.6V to 5.5V, 10mΩ short applied		-40°C to 125°C		2		µs
T_{SD}	Thermal Shutdown			Rising		180		℃
				Falling		145		℃
Enable Pin (ON)								
I_{ON}	ON Pin Leakage	$V_{ON} \geq V_{IH}$		-40°C to 125°C			100	nA
$R_{PD,\ ON}$	Smart Pull Down Resistance	$V_{ON} \leq V_{IL}$		-40°C to 125°C		530		kΩ
Quick-output Discharge (QOD)								
$R_{PD,\ QOD}$	QOD Pin Internal Discharge Resistance	$V_{ON} \leq V_{IL}$		-40°C to 125°C		24		Ω

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.6V, an ambient temperature of 25°C, and a load of CL = 0.1 µF, RL = 100 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	VIN = 5.0 V			1950		µs
		VIN = 3.6 V			1750		µs
		VIN = 1.8 V			1500		µs
t_R	Output Rise Time	VIN = 5.0 V			1280		µs
		VIN = 3.6 V			1100		µs
		VIN = 1.8 V			750		µs
SR_{ON}	Turn ON Slew Rate	VIN = 5.0 V			3.2		mV/µs
		VIN = 3.6 V			2.7		mV/µs
		VIN = 1.8 V			1.8		mV/µs
t_{OFF}	Turn OFF Time	VIN = 1.8 V to 5.0V	R_L = 100Ω, C_L = 0.1uF		6		µs

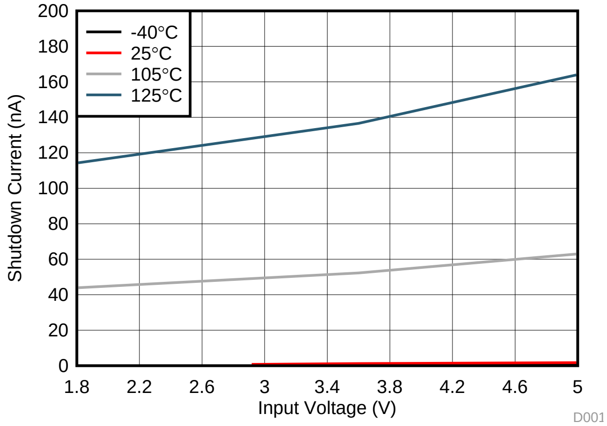
Switching Characteristics (continued)

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.6V, an ambient temperature of 25°C, and a load of CL = 0.1 µF, RL = 100 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{FALL}	Output Fall Time (1)	R_L = 100Ω	C_L = 0.1uF, R_{QOD} = Short		10		µs
		R_L = Open (2)	C_L = 10uF, R_{QOD} = Short		0.4		ms
			C_L = 10uF, R_{QOD} = 100 Ω		3.5		ms
			C_L = 100uF, R_{QOD} = Short		4		ms

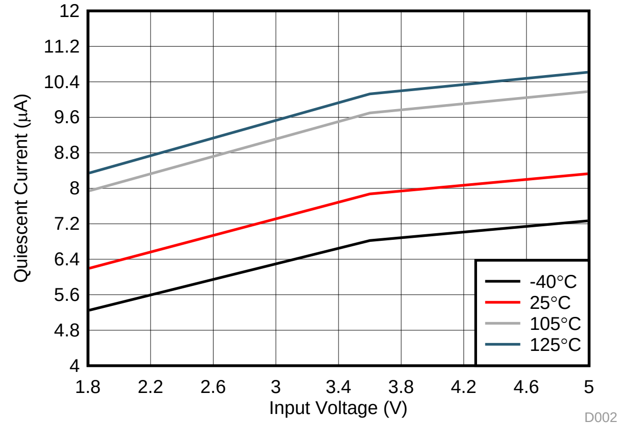
(1) Output may not discharge completely if QOD is not connected to VOUT
(2) See the *Timing Application* section for information on how R_L and C_L affect Fall Time.

6.7 Typical Characteristics



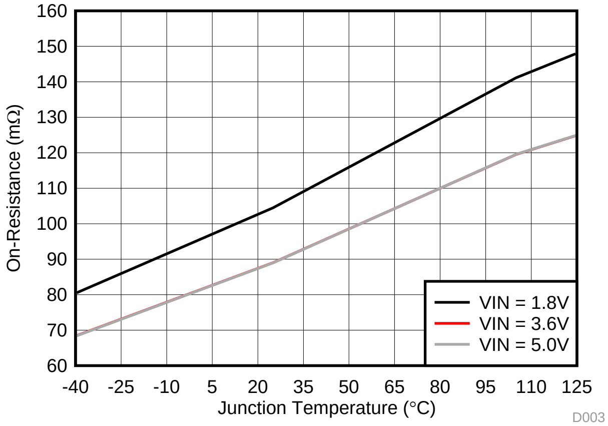
$V_{ON} \le V_{IL}$

图 1. Shutdown Current vs Input Voltage



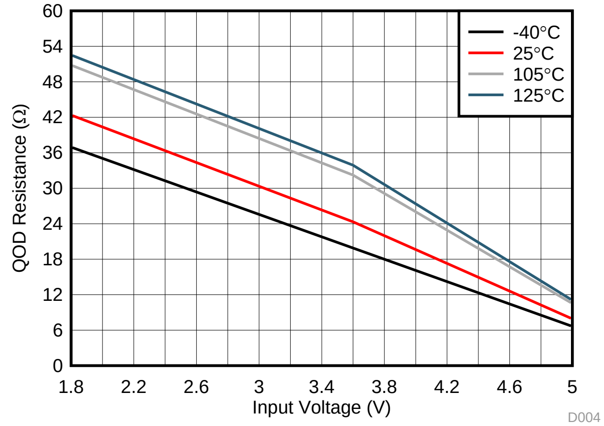
$V_{ON} \ge V_{IH}$

图 2. Quiescent Current vs Input Voltage



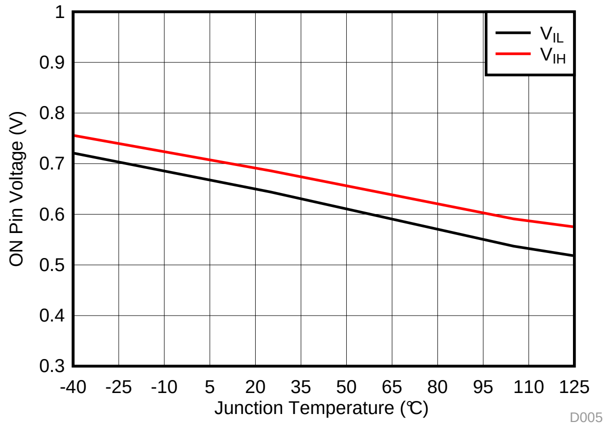
I_{LOAD} = –200 mA

图 3. On-Resistance vs Junction Temperature



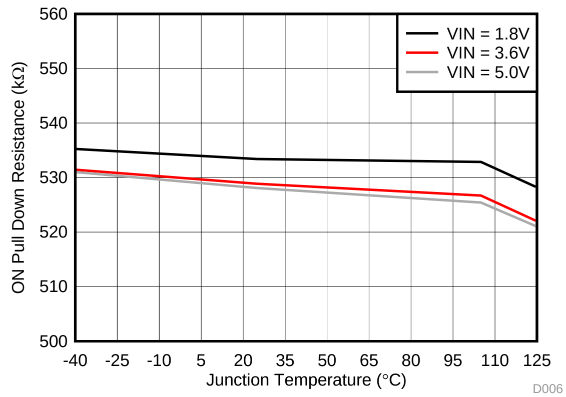
$V_{ON} \le V_{IL}$

图 4. QOD Resistance vs Input Voltage



$V_{ON} \le V_{IL}$

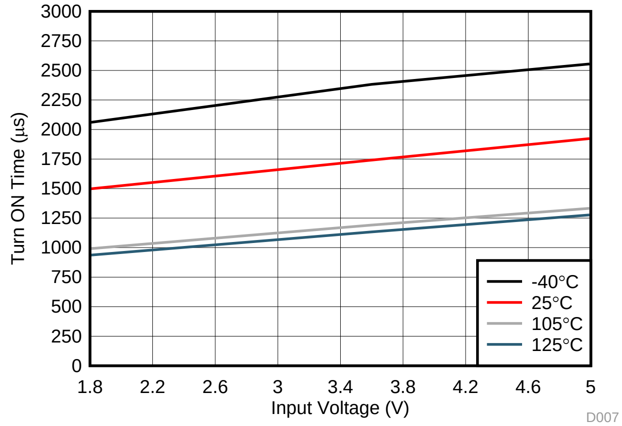
图 5. V_{IH}/V_{IL} vs Junction Temperature



$V_{ON} \le V_{IL}$

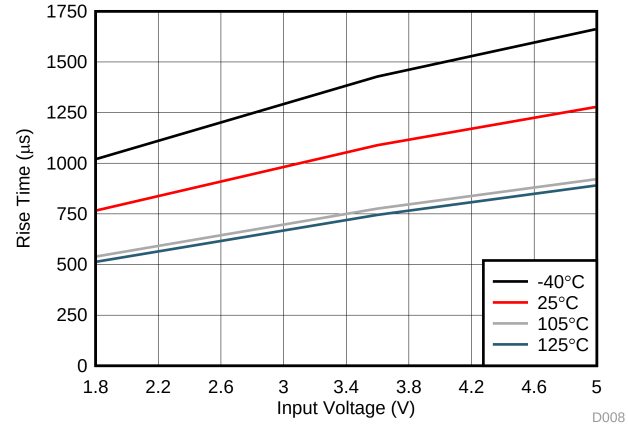
图 6. ON Pull Down Resistance vs Junction Temperature

Typical Characteristics (接下页)



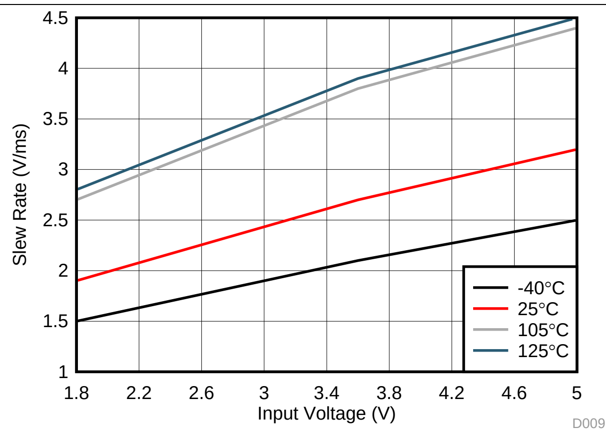
C_L = 0.1 µF R_L = 100 Ω

图 7. Turn ON Time vs Input Voltage



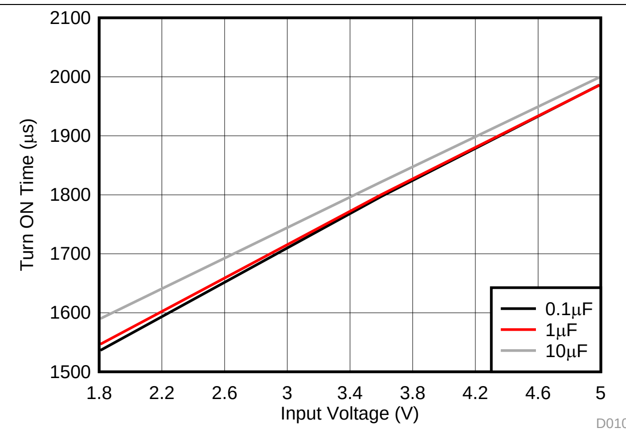
C_L = 0.1 µF R_L = 100 Ω

图 8. Rise Time vs Input Voltage



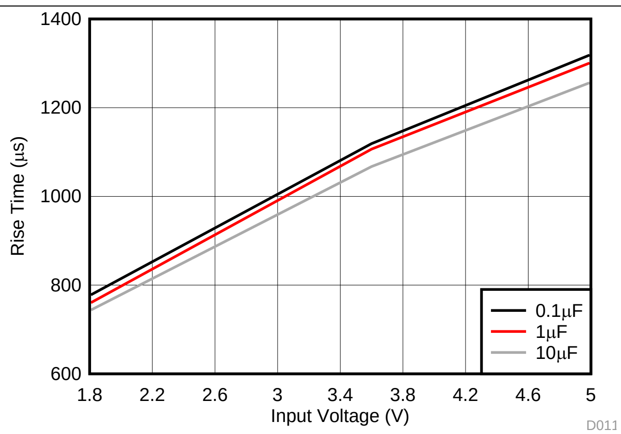
C_L = 0.1 µF R_L = 100 Ω

图 9. Output Slew Rate vs Input Voltage



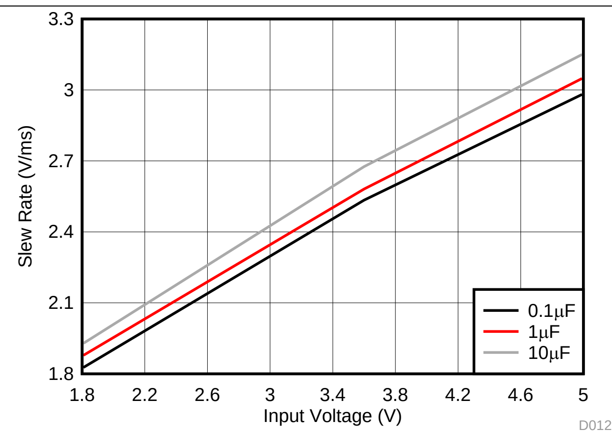
R_L = 100 Ω T_J = 25°C

图 10. Turn ON Time vs Input Voltage Across Load Capacitance



R_L = 100 Ω T_J = 25°C

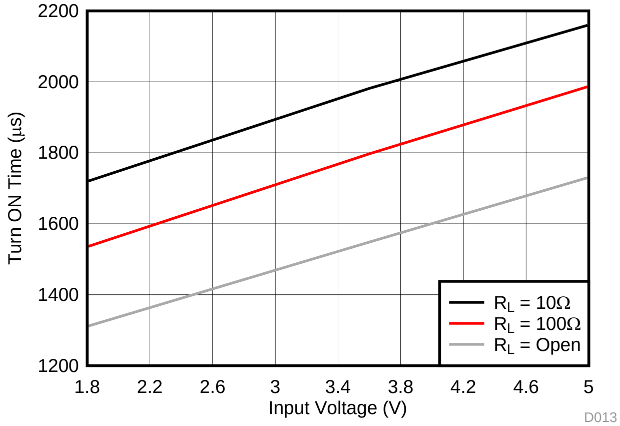
图 11. Rise Time vs Input Voltage Across Load Capacitance



R_L = 100 Ω T_J = 25°C

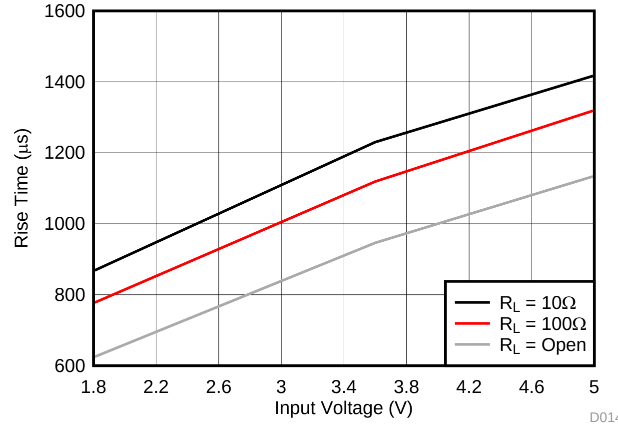
图 12. Slew Rate vs Input Voltage Across Load Capacitance

Typical Characteristics（接下页）



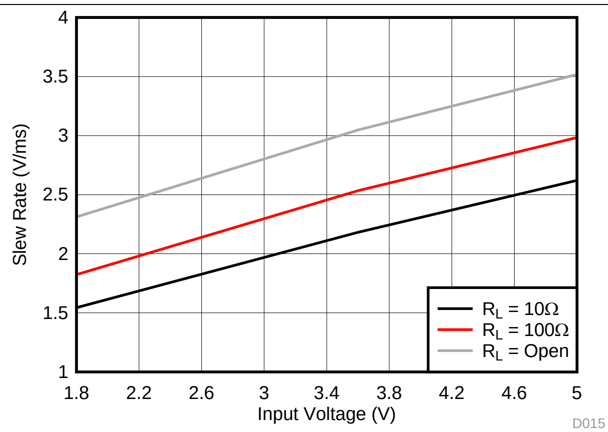
C_L = 0.1 µF T_J = 25°C

图 13. Turn ON Time vs Input Voltage Across Load Resistance



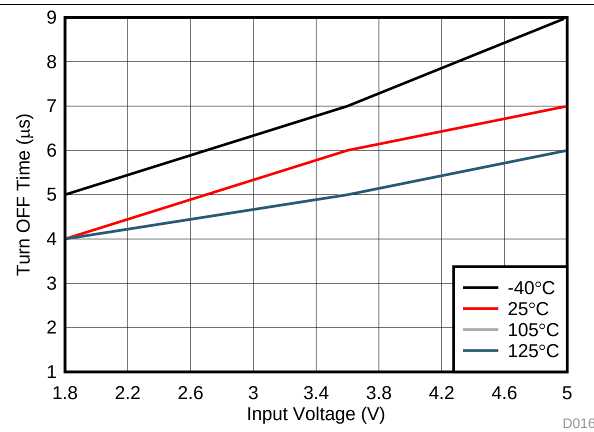
C_L = 0.1 µF T_J = 25°C

图 14. Rise Time vs Input Voltage Across Load Resistance



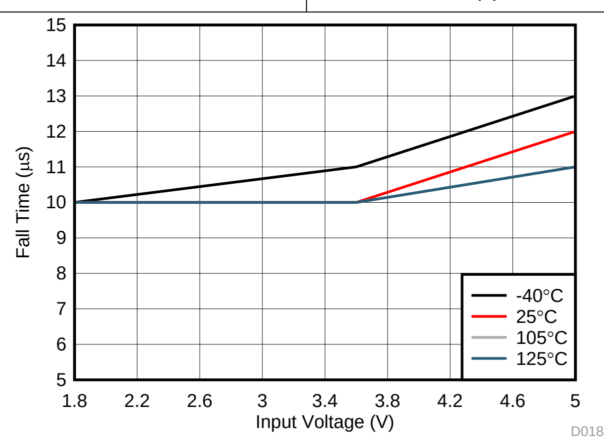
C_L = 0.1 µF T_J = 25°C

图 15. Output Slew Rate vs Input Voltage Across Load Resistance



C_L = 0.1 µF R_L = 100 Ω

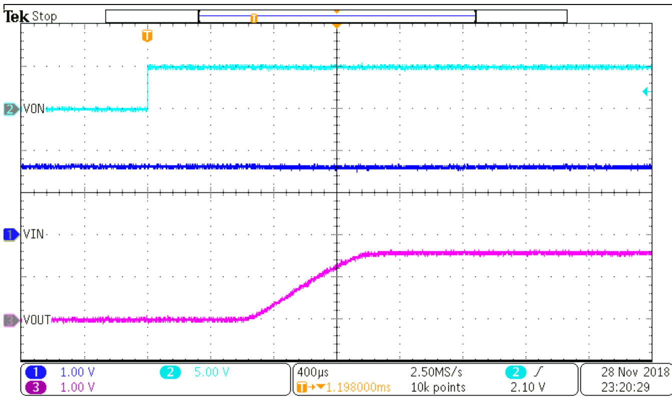
图 16. Turn OFF Time vs Input Voltage



C_L = 0.1 µF R_L = 100 Ω $R_{PD,QOD}$ = Short

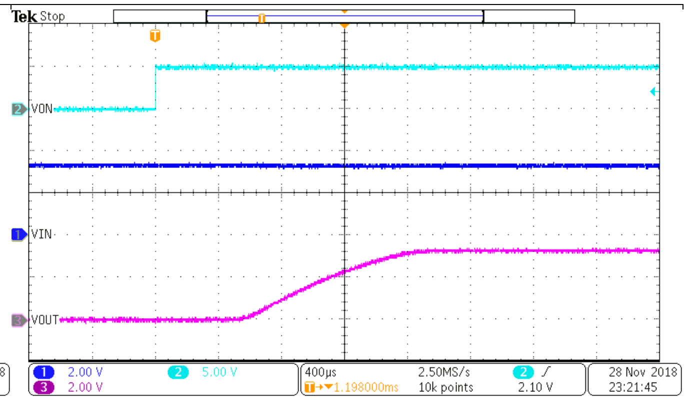
图 17. Fall Time vs Input Voltage

Typical Characteristics（接下页）



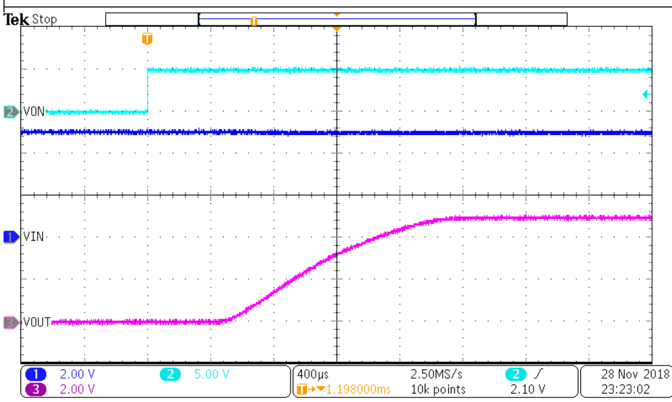
C_L = 0.1 µF R_L = 100 Ω

图 18. Rise Time with VIN = 1.8 V



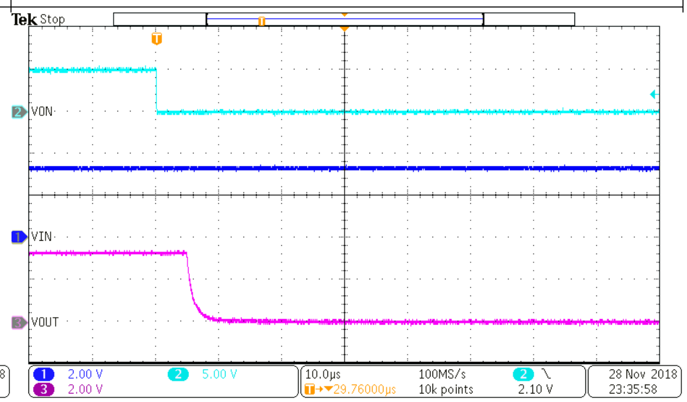
C_L = 0.1 µF R_L = 100 Ω

图 19. Rise Time with VIN = 3.3 V



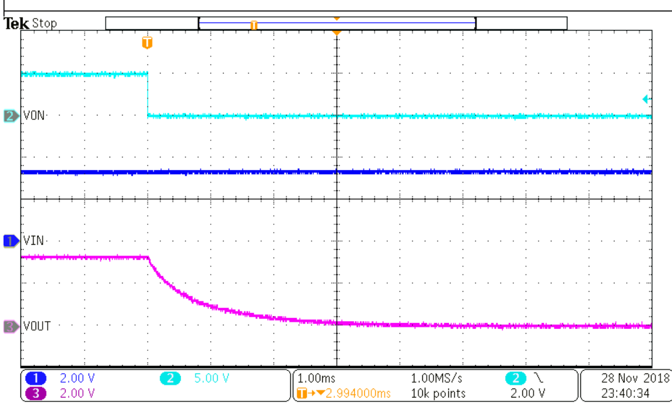
C_L = 0.1 µF R_L = 100 Ω

图 20. Rise Time with VIN = 5 V



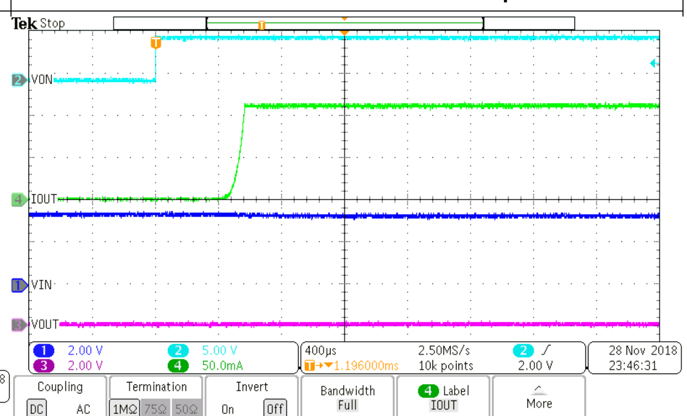
C_L = Open R_L = 100 Ω

图 21. Turn off with a small load capacitance



C_L = 10 µF R_L = 100 Ω

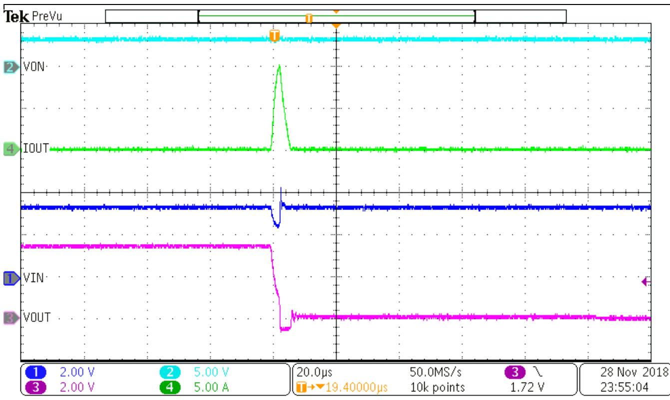
图 22. Turn off with a large load capacitance



V_{IN} = 3.3 V

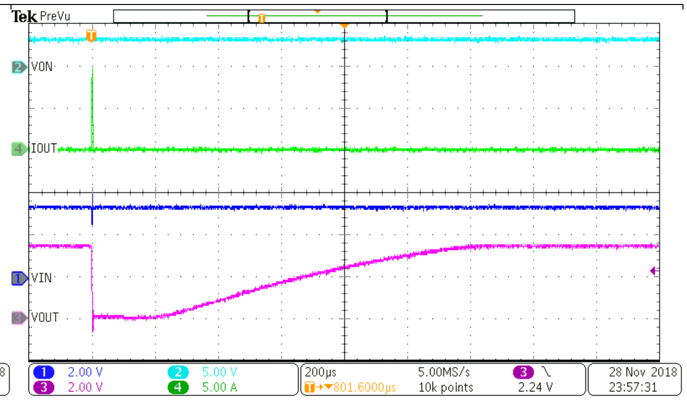
图 23. Turn on into an output short

Typical Characteristics (接下页)



V_{IN} = 3.3 V

图 24. Hot short event when ON

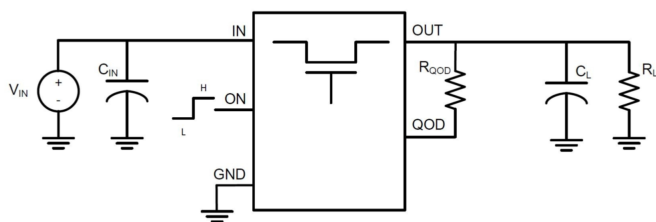


V_{IN} = 3.3 V

图 25. Hot short event when ON and recovery

7 Parameter Measurement Information

7.1 Test Circuit and Timing Waveforms Diagrams



(1) Rise and fall times of the control signal are 100 ns

(2) Turn-off times and fall times are dependent on the time constant at the load. For the TPS22919 devices, the internal pull-down resistance QOD is enabled when the switch is disabled. The time constant is (R_{QOD} + $R_{PD,QOD}$ || R_L) × C_L.

图 26. Test Circuit

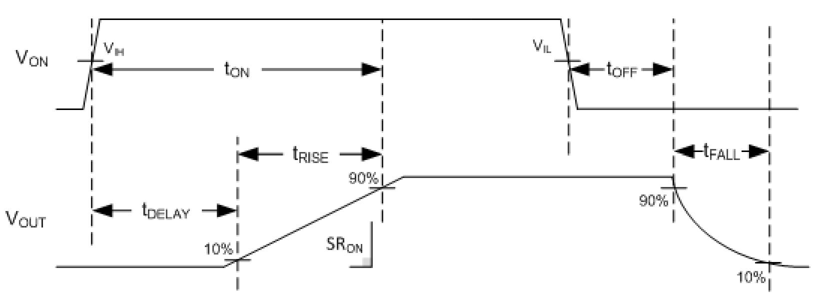


图 27. Timing Waveforms

8 Detailed Description

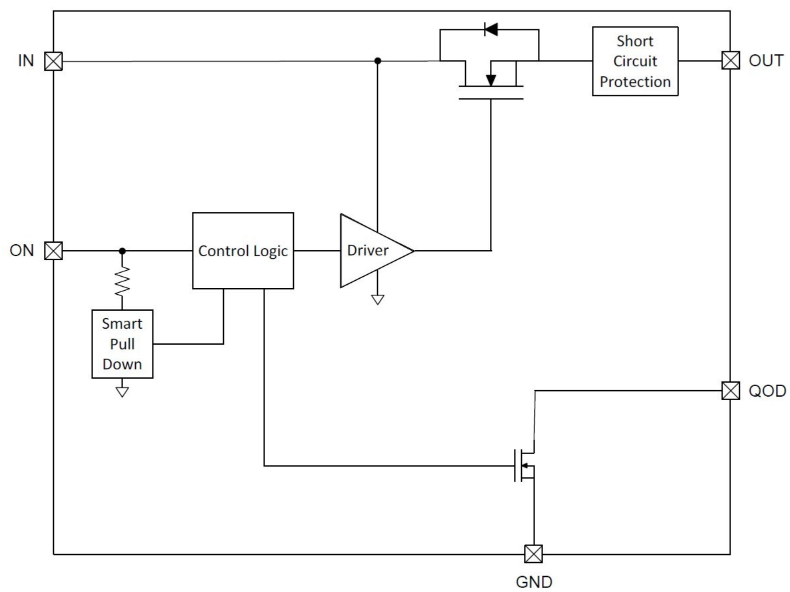
8.1 Overview

The TPS22919 device is a 5.5-V, 1.5-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET which reduces the drop out voltage across the device.

The TPS22919 device has a slow slew rate which helps reduce or eliminate power supply droop because of large inrush currents. Furthermore, the device features a QOD pin, which allows the configuration of the discharge rate of VOUT once the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

The TPS22919 load switch is also self-protected, meaning that it will protect itself from short circuit events on the output of the device. It also has thermal shutdown to prevent any damage from overheating.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold so it can be used in a wide variety of applications. When power is first applied to VIN, a Smart Pull Down is used to keep the ON pin from floating until the system sequencing is complete. Once the ON pin is deliberately driven high (≥V_{IH}), the Smart Pull Down is disconnected to prevent unnecessary power loss. See 表 1 when the ON Pin Smart Pull Down is active.

表 1. Smart-ON Pull Down

VON	Pull Down
≤ V_{IL}	Connected
≥ V_{IH}	Disconnected

8.3.2 Output Short Circuit Protection (I_{SC})

The device will limit current to the output in case of output shorts. When a short occurs, the large VIN to VOUT voltage drop causes the switch to limit the output current (I_{SC}) within (t_{SC}). When the output is below the hard short threshold (V_{SC}), a lower limit is used to minimize the power dissipation while the fault is present. The device will continue to limit the current until it reaches its thermal shutdown temperature. At this time, the device will turn off until its temperature has lowered by the thermal hysteresis (35°C typical) before turning on again.

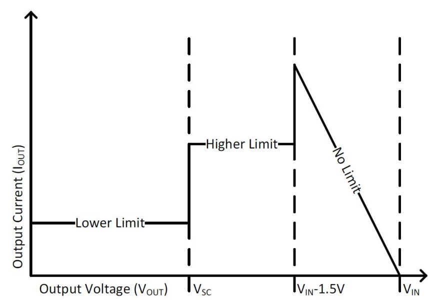


图 28. Output Short Circuit Current Limit

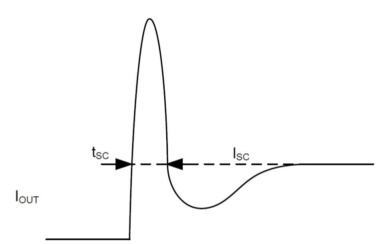


图 29. Output Short Circuit Response

8.3.3 Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

The TPS22919 device includes a QOD pin that can be configured in one of three ways:

- QOD pin shorted to VOUT pin. Using this method, the discharge rate after the switch becomes disabled is controlled with the value of the internal resistance QOD ($R_{PD,QOD}$).
- QOD pin connected to VOUT pin using an external resistor R_{QOD}. After the switch becomes disabled, the discharge rate is controlled by the value of the total discharge resistance. To adjust the total discharge resistance, 公式 1 can be used:

$$R_{DIS} = R_{PD,QOD} + R_{QOD}$$

Where:

- R_{DIS} = Total output discharge resistance (Ω)

  - $R_{PD,QOD}$ = Internal pulldown resistance (Ω)
  - R_{QOD} = External resistance placed between the VOUT and QOD pins (Ω) (1)
- QOD pin is unused and left floating. Using this method, there will be no quick output discharge functionality, and the output will remain floating after the switch is disabled.

The fall times of the device depend on many factors including the total discharge resistance (R_{DIS}) and the output capacitance (C_L). To calculate the approximate fall time of V_{OUT} use 公式 2.

$$t_{FALL} = 2.2 \times (R_{DIS} \,||\, R_L) \times C_L$$

Where:

- t_{FALL} = Output Fall Time from 90% to 10% (μs)
- R_{DIS} = Total QOD + R_{QOD} Resistance (Ω)
- R_L = Output Load Resistance (Ω)
- C_L = Output Load Capacitance (μF) (2)

8.3.3.1 QOD When System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor discharges at V_{IN}. Past a certain V_{IN} level, the strength of the R_{PD} will be reduced. If there is still remaining charge on the output capacitor, this will result in longer fall times. For further information regarding this condition, see the *Setting Fall Time for Shutdown Power Sequencing* section.

8.4 Device Functional Modes

表 2 describes the connection of the VOUT pin depending on the state of the ON pin as well as the various QOD pin configurations.

表 2. VOUT Connection

ON	QOD CONFIGURATION	TPS22919 VOUT
L	QOD pin connected to VOUT with R_{QOD}	GND ($R_{PD,\ QOD}$ + R_{QOD})
L	QOD pin tied to VOUT directly	GND ($R_{PD,\ QOD}$)
L	QOD pin left open	Floating
H	N/A	VIN

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

9.2 Typical Application

This typical application demonstrates how the TPS22919 devices can be used to power downstream modules.

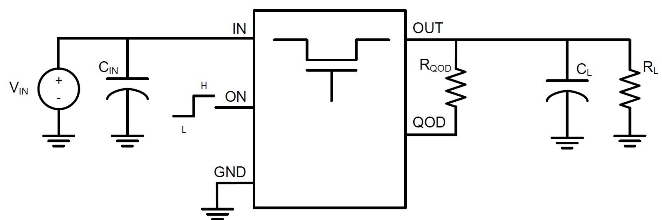


图 30. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in 表 3 as the design parameters:

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	3.6 V
Load Current / Resistance (R_L)	1 kΩ
Load Capacitance (C_L)	47 µF
Minimum Fall Time (t_F)	40 ms
Maximum Inrush Current (I_{RUSH})	150 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Limiting Inrush Current

Use 公式 3 to find the maximum slew rate value to limit inrush current for a given capacitance:

$$(\text{Slew Rate}) = I_{RUSH} \div C_L \quad (3)$$

where
- I_{INRUSH} = maximum acceptable inrush current (mA)
- C_L = capacitance on VOUT (μF)
- Slew Rate = Output Slew Rate during turn on (mV/μs)

Based on 公式 3, the required slew rate to limit the inrush current to 150 mA is 3.2 mV/μs. The TPS22919 has a slew rate of 2.3 mV/μs, so the inrush current will be below 150 mA.

9.2.2.2 Setting Fall Time for Shutdown Power Sequencing

Microcontrollers and processors often have a specific shutdown sequence in which power must be removed. Using the adjustable Quick Output Discharge function of the TPS22919 device, adding a load switch to each power rail can be used to manage the power down sequencing. To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down.

Once the required fall time is determined, the maximum external discharge resistance (R_{DIS}) value can be found using 公式 2:

$$t_{FALL} = 2.2 \times (R_{DIS} \parallel R_L) \times C_L \quad (4)$$

$$R_{DIS} = 630\ \Omega \quad (5)$$

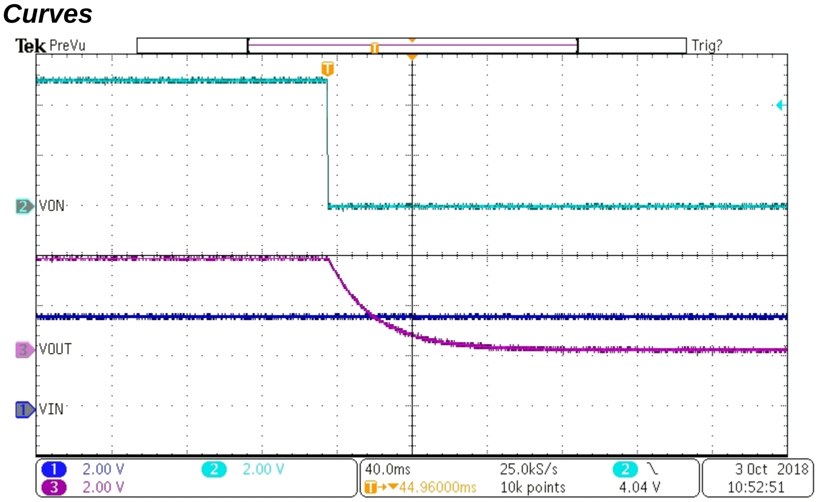
公式 1 can then be used to calculate the R_{QOD} resistance needed to achieve a particular discharge value:

$$R_{DIS} = QOD + R_{QOD} \quad (6)$$

$$R_{QOD} = 600\ \Omega \quad (7)$$

To ensure a fall time greater than, choose an R_{QOD} value greater than 600 Ω.

9.2.2.3 Application Curves



A.

C_L = 47μF

图 31. Fall Time (R_{QOD} = 1 kΩ)

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.6 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 μF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

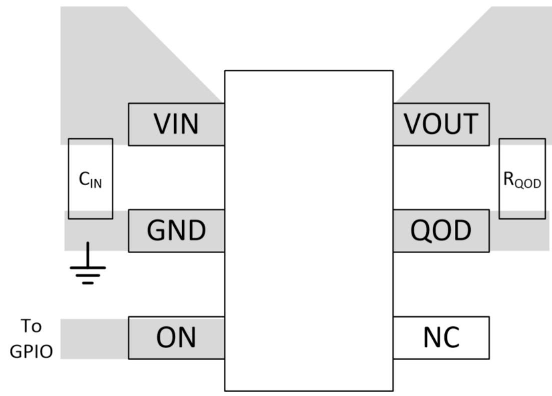


图 32. Recommended Board Layout

11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use 公式 8:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \tag{8}$$

where

- $P_{D(MAX)}$ = maximum allowable power dissipation
- $T_{J(MAX)}$ = maximum allowable junction temperature (125°C for the TPS22919 devices)
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. Refer to the Thermal Parameters table. This parameter is highly dependent upon board layout.

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 商标

E2E is a trademark of Texas Instruments.

12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS22919DCKR	Obsolete	Preproduction	SC70 (DCK) | 6	-	-	Call TI	Call TI	-40 to 125	
TPS22919DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	1CS
TPS22919DCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1CS
TPS22919DCKT	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	1CS
TPS22919DCKT.A	Active	Production	SC70 (DCK) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1CS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS22919 :

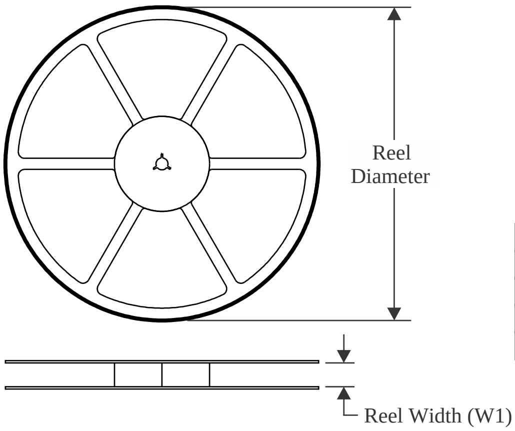
- Automotive : TPS22919-Q1

NOTE: Qualified Version Definitions:

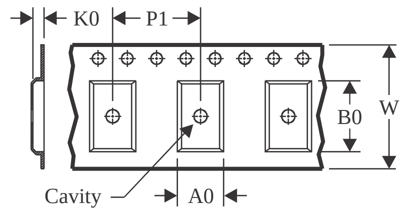
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

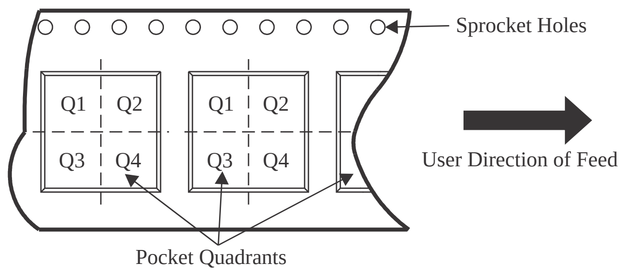


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

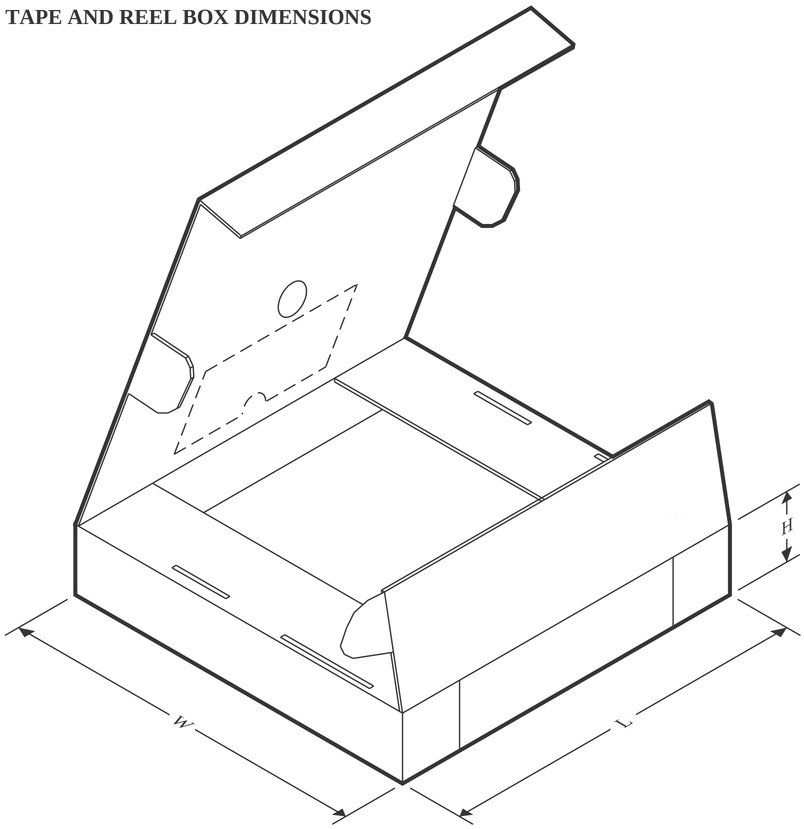
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

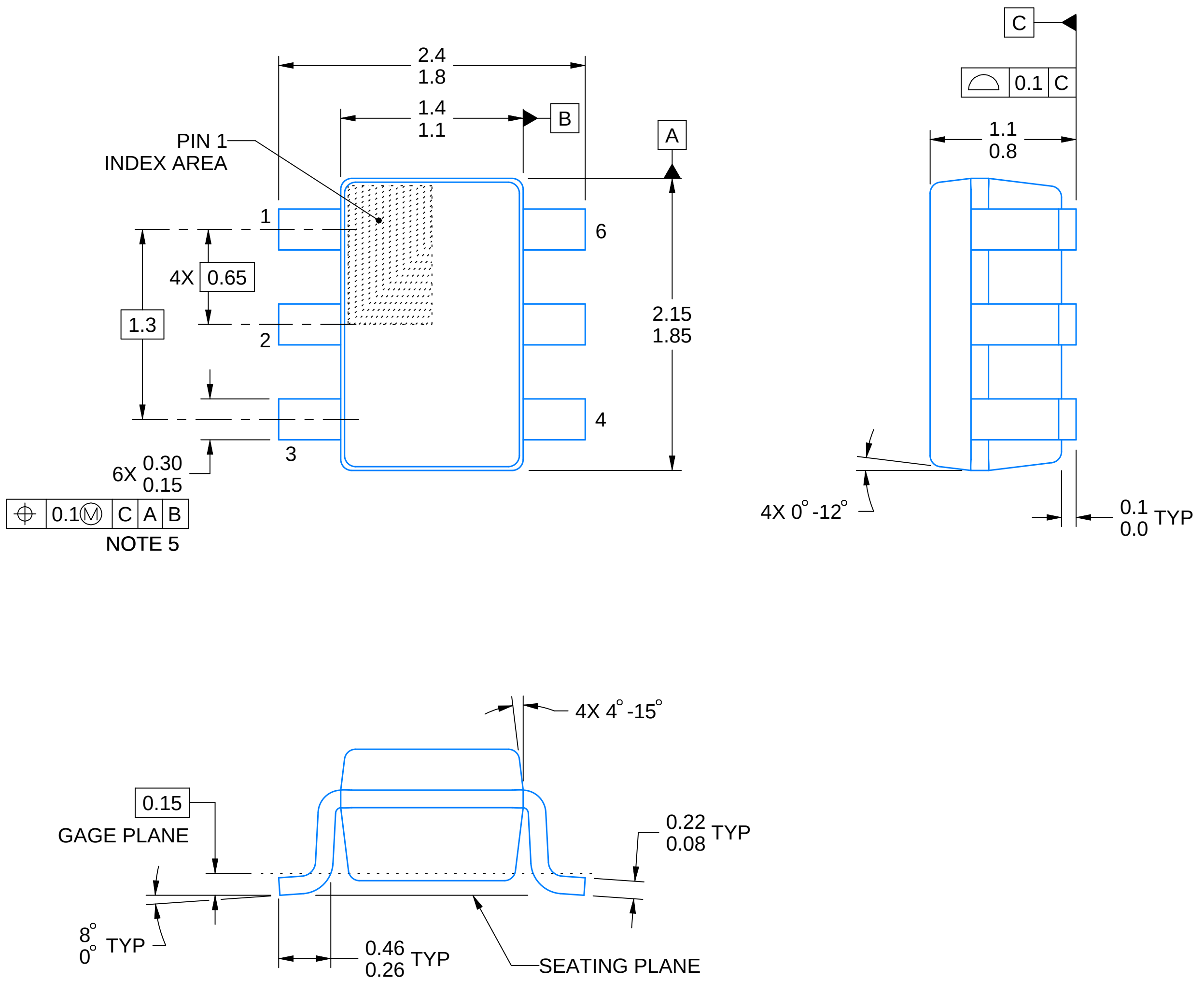
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22919DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
TPS22919DCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22919DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
TPS22919DCKT	SC70	DCK	6	250	210.0	185.0	35.0



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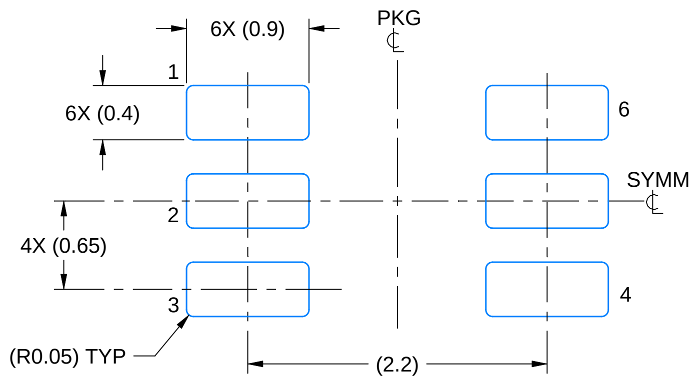
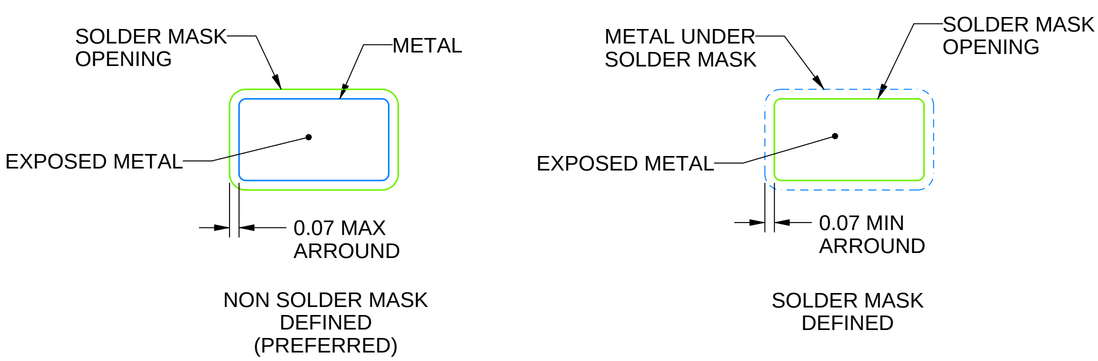
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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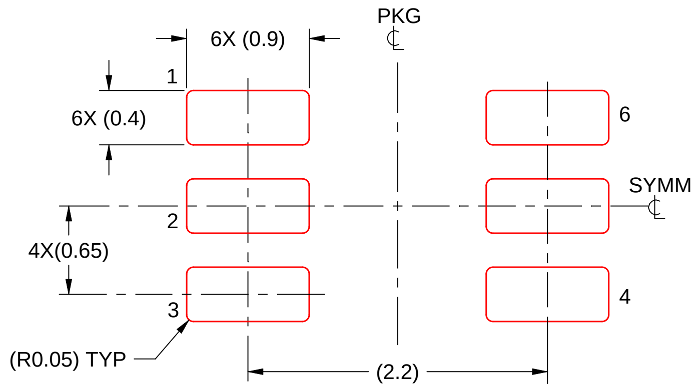
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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