



TPS22958x 具有可调节上升时间的 5.5V、4A/6A、14mΩ 负载开关

1 特性

- 集成 N 通道负载开关
- 输入电压范围: 0.6V 至 5.5V
- VBIAS 电压范围: 2.5V 至 5.5V
- R_{ON} 电阻
 - $V_{IN} = 5V$ ($V_{BIAS} = 5V$) 时, $R_{ON} = 14m\Omega$
 - $V_{IN} = 3.3V$ ($V_{BIAS} = 5V$) 时, $R_{ON} = 13m\Omega$
 - $V_{IN} = 1.8V$ ($V_{BIAS} = 5V$) 时, $R_{ON} = 13m\Omega$
- 4A 最大持续开关电流 (DGK 封装)
- 6A 最大持续开关电流 (DGN 封装)
- 低静态电流
 - $V_{BIAS} = 5V$ 时为 55μA
- 低控制输入阈值支持使用 1.2V/1.8V/2.5V/3.3V 逻辑电路
- 可调节上升时间⁽¹⁾
- 快速输出放电 (QOD)⁽²⁾
- DGK 8 引脚封装:
 - 3.0mm x 4.9mm x 1.1mm, 0.65mm 间距
- 带有散热焊盘的 DGK 8 引脚封装:
 - 3.0mm x 4.9mm x 1.1mm, 0.65mm 间距
- 静电放电 (ESD) 性能经测试符合 JEDEC STD 标准。
 - 2kV 人体模型 (HBM) 和 1kV 器件充电模型 (CDM)
- 闩锁性能超出 100mA, 符合 JESD 78 II 类规范的要求
- 通用输入输出 (GPIO) 使能 - 高电平有效

(1) 有关 CT 值与上升时间的关系, 请参见 [Adjustable Rise Time](#) 部分

(2) TPS22958N 器件不具备该特性。

2 应用

- 电子销售点 (EPOS)
- 工厂自动化/控制
- 楼宇自动化
- 打印机
- 波峰焊制造

3 说明

TPS22958x 是一款具有可调节上升时间的小型单通道负载开关。此器件包含一个可在 0.6V 至 5.5V 输入电压范围内运行的 N 通道 MOSFET, 并且可支持最大 4A (DGK 封装) 或 6A (DGN 封装) 的持续电流。此开关可由一个打开/关闭输入控制, 此输入可与低压控制信号直接对接。

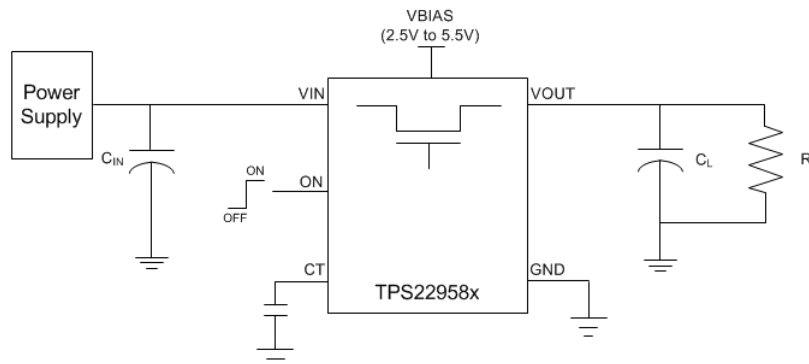
该器件的上升时间可从外部进行控制, 从而避免涌入电流。在 CT 引脚上连接一个电容即可更改上升时间: 电容值越大, 上升时间越长。TPS22958x 提供 DGK 和 DGN 两种节省空间的封装, 其中 DGN 封装带有支持高功率耗散的散热焊盘, 而 DGN 封装则不带有散热焊盘。器件在自然通风环境下的额定运行温度范围为 -40°C 至 105°C。

器件信息⁽¹⁾

器件编号	封装 (引脚)	封装尺寸 (标称值)
TPS22958x	DGK (8)	3.00mm x 4.90mm
	DGN (8)	3.00mm x 4.90mm

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

典型应用电路原理图



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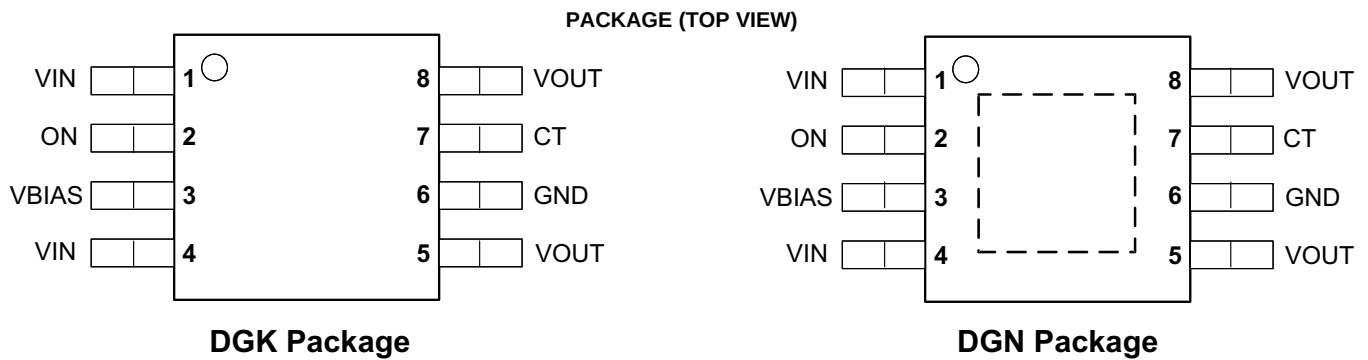
4 修订历史记录

Changes from Original (January 2014) to Revision A	Page
• 完整版的最初发布版本。	1

5 Device Comparison Table

DEVICE	R_{ON} AT $V_{IN} = V_{BIAS} = 5V$	RISE TIME	QUICK OUTPUT DISCHARGE	MAX OUTPUT CURRENT	ENABLE
TPS22958DGK	14 m Ω	Adjustable	Yes	4 A	Active High
TPS22958DGN		Adjustable	Yes	6 A	
TPS22958NDGK		Adjustable	No	4 A	
TPS22958NDGN		Adjustable	No	6 A	

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1, 4	VIN	I	Switch input. Bypass this input with a ceramic capacitor to GND. These pins should be tied together as shown in Layout Information.
2	ON	I	Active-high switch control input. Do not leave floating.
3	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 to 5.5 V. See VIN and VBIAS Voltage Range .
5, 8	VOUT	O	Switch output
6	GND	—	Ground
7	CT	O	Switch slew rate control. Can be left floating.
—	Thermal Pad ⁽¹⁾	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See Layout Guidelines for layout guidelines.

(1) Only available for the DGN package

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted)⁽¹⁾ ⁽²⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage	−0.3	6	V
V _{BIAS}	Bias voltage	−0.3	6	V
V _{OUT}	Output voltage	−0.3	6	V
V _{ON}	ON voltage	−0.3	6	V
I _{MAX}	Maximum continuous switch current, T _A = 65°C (DGK Package)		4	A
	Maximum continuous switch current, T _A = 75°C (DGN Package)		6	A
I _{PLS}	Maximum pulsed switch current, pulse <300 μs, 2% duty cycle (DGK Package)		6	A
	Maximum pulsed switch current, pulse <300 μs, 2% duty cycle (DGN Package)		8	A
T _J	Maximum junction temperature		125	°C
T _{stg}	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V _{IN}	Input voltage range		0.6	V _{BIAS}	V
V _{BIAS}	Bias voltage range		2.5	5.5	V
V _{ON}	ON voltage range		0	5.5	V
V _{OUT}	Output voltage range			V _{IN}	V
V _{IH, ON}	High-level input voltage, ON	V _{BIAS} = 2.5 to 5.5 V	1.2	5.5	V
V _{IL, ON}	Low-level input voltage, ON	V _{BIAS} = 2.5 to 5.5 V	0	0.5	V
T _A	Operating free-air temperature ⁽¹⁾		−40	105	°C
C _{IN}	Input capacitor		1 ⁽²⁾		μF

- (1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T_{A(max)}] is dependent on the maximum operating junction temperature [T_{J(max)}], the maximum power dissipation of the device in the application [P_{D(max)}], and the junction-to-ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A(max)} = T_{J(max)} − (R_{θJA} × P_{D(max)}).
- (2) Refer to the [Application Information](#) section.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾ (2)		TPS22958x		UNIT
		DGK (8 PINS)	DGN (8 PINS)	
R _{θJA}	Junction-to-ambient thermal resistance	185.7	67.0	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	77.3	66.5	
R _{θJB}	Junction-to-board thermal resistance	107.0	46.8	
Ψ _{JT}	Junction-to-top characterization parameter	15.2	5.0	
Ψ _{JB}	Junction-to-board characterization parameter	105.4	46.6	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	14.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) For thermal estimates of this device based on PCB copper area, see the *TI PCB Thermal Calculator*.

7.5 Electrical Characteristics ($V_{BIAS} = 5\text{ V}$)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ and $V_{BIAS} = 5\text{ V}$. Typical values are for $T_A = 25^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T _A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
I _Q , V _{BIAS}	V _{BIAS} quiescent current	I _{OUT} = 0, V _{IN} = V _{ON} = V _{BIAS} = 5 V		-40°C to 85°C	54	60	μA	
				-40°C to 105°C		60		
I _{SD} , V _{BIAS}	V _{BIAS} shutdown current	V _{ON} = 0 V, V _{OUT} = 0 V, V _{BIAS} = 5 V		-40°C to 85°C	0.5	1	μA	
				-40°C to 105°C		1		
I _{SD} , V _{IN}	V _{IN} shutdown current	V _{ON} = 0 V, V _{OUT} = 0 V, V _{BIAS} = 5 V	V _{IN} = 5 V	-40°C to 85°C	0.5	8	μA	
				-40°C to 105°C		10		
			V _{IN} = 3.3 V	-40°C to 85°C	0.1	3		
				-40°C to 105°C		4		
			V _{IN} = 1.8 V	-40°C to 85°C	0.07	2		
				-40°C to 105°C		3		
			V _{IN} = 1.2 V	-40°C to 85°C	0.05	1		
				-40°C to 105°C		2		
			V _{IN} = 0.6 V	-40°C to 85°C	0.04	1		
				-40°C to 105°C		2		
I _{ON}	ON pin input leakage current	V _{ON} = 5.5 V, V _{BIAS} = 5 V		-40°C to 105°C		0.1	μA	
RESISTANCE CHARACTERISTICS								
R _{ON}	ON-state resistance	I _{OUT} = -200 mA, V _{BIAS} = 5 V	V _{IN} = 5 V	25°C	14	18	mΩ	
				-40°C to 85°C		20		
				-40°C to 105°C		24		
			V _{IN} = 3.3 V	25°C	13	17	mΩ	
				-40°C to 85°C		20		
				-40°C to 105°C		23		
			V _{IN} = 2.5 V	25°C	13	17	mΩ	
				-40°C to 85°C		20		
				-40°C to 105°C		23		
			V _{IN} = 1.8 V	25°C	13	17	mΩ	
				-40°C to 85°C		20		
				-40°C to 105°C		23		
			V _{IN} = 1.5 V	25°C	13	17	mΩ	
				-40°C to 85°C		20		
				-40°C to 105°C		23		
			V _{IN} = 1.2 V	25°C	13	17	mΩ	
				-40°C to 85°C		20		
				-40°C to 105°C		23		
			V _{IN} = 0.6 V	25°C	13	17	mΩ	
				-40°C to 85°C		20		
				-40°C to 105°C		23		
R _{PD}	Output pulldown resistance	V _{IN} = V _{BIAS} = 5 V, V _{ON} = 0 V, I _{OUT} = 10 mA		-40°C to 105°C	135	160	Ω	

7.6 Electrical Characteristics ($V_{BIAS} = 3.3\text{ V}$)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ and $V_{BIAS} = 3.3\text{ V}$. Typical values are for $T_A = 25^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS							
I_Q , V_{BIAS}	V_{BIAS} quiescent current	$I_{OUT} = 0$, $V_{IN} = V_{ON} = V_{BIAS} = 3.3\text{ V}$	-40°C to 85°C		23	27	μA
			-40°C to 105°C			27	
I_{SD} , V_{BIAS}	V_{BIAS} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, $V_{BIAS} = 3.3\text{ V}$	-40°C to 85°C		0.3	0.7	μA
			-40°C to 105°C			0.7	
I_{SD} , V_{IN}	V_{IN} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, $V_{BIAS} = 3.3\text{ V}$	$V_{IN} = 3.3\text{ V}$	-40°C to 85°C	0.1	3	μA
			$V_{IN} = 3.3\text{ V}$	-40°C to 105°C		4	
			$V_{IN} = 1.8\text{ V}$	-40°C to 85°C	0.07	2	
			$V_{IN} = 1.8\text{ V}$	-40°C to 105°C		3	
			$V_{IN} = 1.2\text{ V}$	-40°C to 85°C	0.05	1	
			$V_{IN} = 1.2\text{ V}$	-40°C to 105°C		2	
			$V_{IN} = 0.6\text{ V}$	-40°C to 85°C	0.04	1	
			$V_{IN} = 0.6\text{ V}$	-40°C to 105°C		2	
I_{ON}	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$, $V_{BIAS} = 3.3\text{ V}$	-40°C to 105°C			0.1	μA
RESISTANCE CHARACTERISTICS							
R_{ON}	ON-state resistance	$I_{OUT} = -200\text{ mA}$, $V_{BIAS} = 3.3\text{ V}$	$V_{IN} = 3.3\text{ V}$	25°C	14	18	$\text{m}\Omega$
				-40°C to 85°C		20	
				-40°C to 105°C		24	
			$V_{IN} = 2.5\text{ V}$	25°C	13	17	$\text{m}\Omega$
				-40°C to 85°C		20	
				-40°C to 105°C		23	
			$V_{IN} = 1.8\text{ V}$	25°C	13	17	$\text{m}\Omega$
				-40°C to 85°C		20	
				-40°C to 105°C		23	
			$V_{IN} = 1.5\text{ V}$	25°C	13	17	$\text{m}\Omega$
				-40°C to 85°C		20	
				-40°C to 105°C		23	
			$V_{IN} = 1.2\text{ V}$	25°C	13	17	$\text{m}\Omega$
				-40°C to 85°C		20	
				-40°C to 105°C		23	
			$V_{IN} = 0.6\text{ V}$	25°C	13	17	$\text{m}\Omega$
				-40°C to 85°C		20	
				-40°C to 105°C		23	
R_{PD}	Output pulldown resistance	$V_{IN} = V_{BIAS} = 3.3\text{ V}$, $V_{ON} = 0\text{ V}$, $I_{OUT} = 10\text{ mA}$	-40°C to 105°C		135	160	Ω

7.7 Electrical Characteristics ($V_{BIAS} = 2.5\text{ V}$)

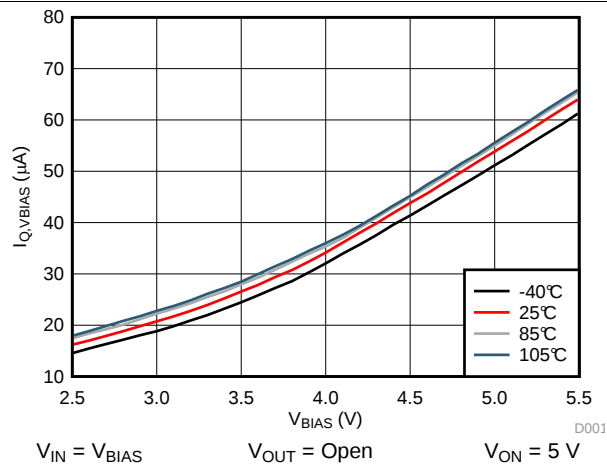
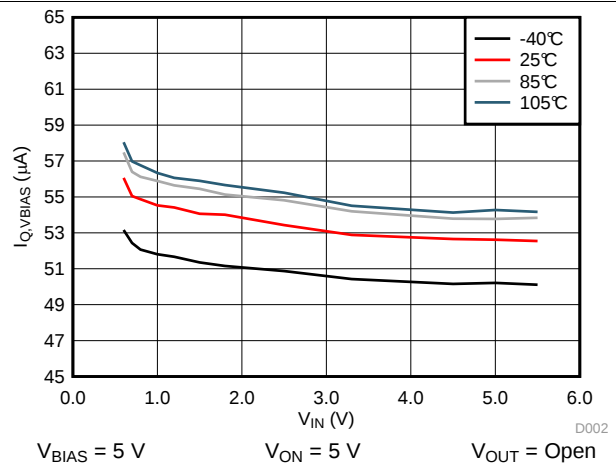
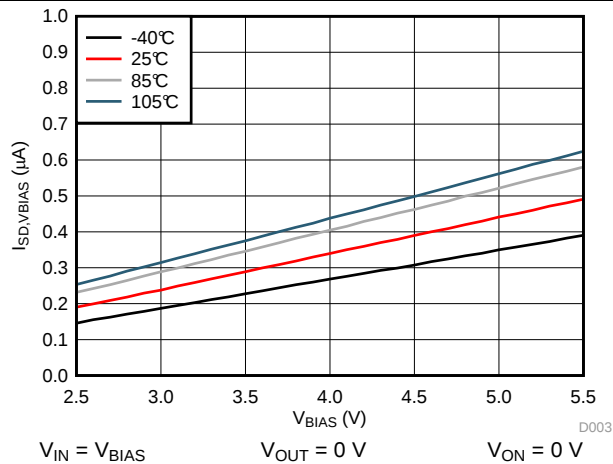
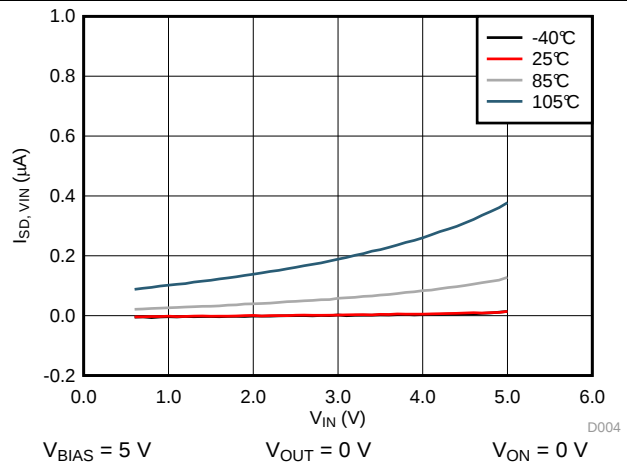
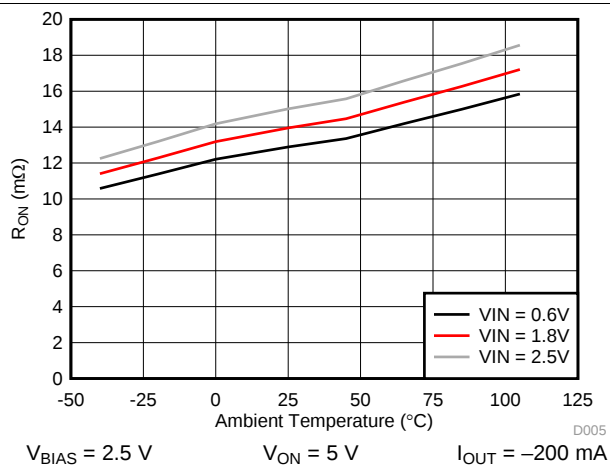
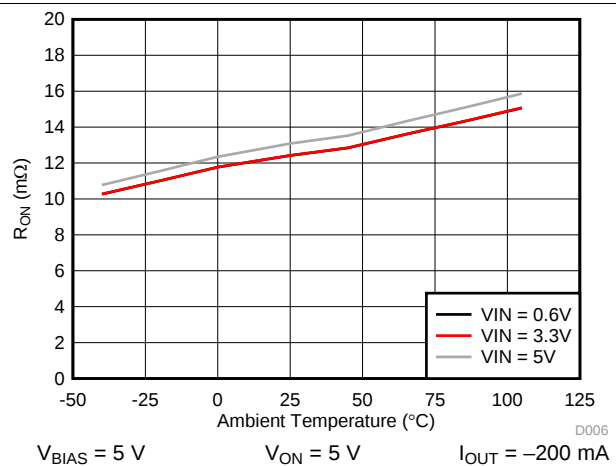
Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$ and $V_{BIAS} = 2.5\text{ V}$. Typical values are for $T_A = 25\text{ }^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS							
I_Q , V_{BIAS}	V_{BIAS} quiescent current	$I_{OUT} = 0$, $V_{IN} = V_{ON} = V_{BIAS} = 2.5\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$		14	17	μA
			$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$			17	
I_{SD} , V_{BIAS}	V_{BIAS} shutdown current	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, $V_{BIAS} = 2.5\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$		0.2	0.5	μA
			$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$			0.5	
I_{SD} , V_{IN}	V_{IN} shutdown current (per channel)	$V_{ON} = 0\text{ V}$, $V_{OUT} = 0\text{ V}$, $V_{BIAS} = 2.5\text{ V}$	$V_{IN} = 2.5\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	0.1	3	μA
			$V_{IN} = 2.5\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$		4	
			$V_{IN} = 1.8\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	0.07	2	
			$V_{IN} = 1.8\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$		3	
			$V_{IN} = 1.2\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	0.05	1	
			$V_{IN} = 1.2\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$		2	
			$V_{IN} = 0.6\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	0.04	1	
			$V_{IN} = 0.6\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$		2	
I_{ON}	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$, $V_{BIAS} = 2.5\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$			0.1	μA
RESISTANCE CHARACTERISTICS							
R_{ON}	ON-state resistance	$I_{OUT} = -200\text{ mA}$, $V_{BIAS} = 2.5\text{ V}$	$V_{IN} = 2.5\text{ V}$	$25\text{ }^{\circ}\text{C}$	15	19	$\text{m}\Omega$
				$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$		23	
				$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$		26	
			$V_{IN} = 1.8\text{ V}$	$25\text{ }^{\circ}\text{C}$	14	18	$\text{m}\Omega$
				$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$		22	
				$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$		25	
			$V_{IN} = 1.5\text{ V}$	$25\text{ }^{\circ}\text{C}$	14	18	$\text{m}\Omega$
				$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$		22	
				$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$		25	
			$V_{IN} = 1.2\text{ V}$	$25\text{ }^{\circ}\text{C}$	14	18	$\text{m}\Omega$
				$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$		22	
				$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$		25	
			$V_{IN} = 0.6\text{ V}$	$25\text{ }^{\circ}\text{C}$	13	18	$\text{m}\Omega$
				$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$		22	
				$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$		25	
R_{PD}	Output pulldown resistance	$V_{IN} = V_{BIAS} = 2.5\text{ V}$, $V_{ON} = 0\text{ V}$, $I_{OUT} = 10\text{ mA}$	$-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$		135	160	Ω

7.8 Switching Characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{IN} = V _{ON} = V _{BIAS} = 5 V, T _A = 25 °C						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		646		μs
t _{OFF}	Turn-off time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		5		
t _R	V _{OUT} rise time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		769		
t _F	V _{OUT} fall time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		2		
t _D	ON delay time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		280		
V _{IN} = 0.6 V, V _{ON} = V _{BIAS} = 5 V, T _A = 25 °C						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		303		μs
t _{OFF}	Turn-off time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		91		
t _R	V _{OUT} rise time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		126		
t _F	V _{OUT} fall time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		7		
t _D	ON delay time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		243		
V _{IN} = 2.5 V, V _{ON} = 5 V, V _{BIAS} = 2.5V, T _A = 25 °C						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		983		μs
t _{OFF}	Turn-off time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		7		
t _R	V _{OUT} rise time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		987		
t _F	V _{OUT} fall time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		2		
t _D	ON delay time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		518		
V _{IN} = 0.6 V, V _{ON} = 5 V, V _{BIAS} = 2.5 V, T _A = 25 °C						
t _{ON}	Turn-on time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		611		μs
t _{OFF}	Turn-off time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		77		
t _R	V _{OUT} rise time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		305		
t _F	V _{OUT} fall time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		7		
t _D	ON delay time	R _L = 10 Ω, C _L = 0.1 μF, CT = 1000 pF		468		

7.9 Typical DC Characteristics


Figure 1. Quiescent Current vs V_{BIAS}

Figure 2. Quiescent Current vs V_{IN}

Figure 3. Shutdown Current vs V_{BIAS}

Figure 4. V_{IN} Shutdown Current vs V_{IN}

Figure 5. R_{ON} vs Temperature

Figure 6. R_{ON} vs Temperature

Typical DC Characteristics (continued)

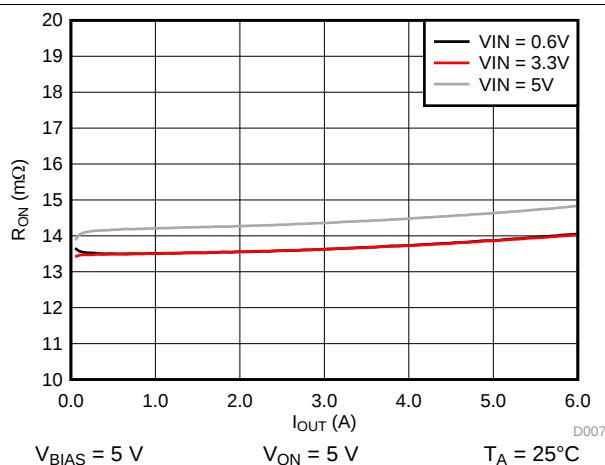


Figure 7. R_{ON} vs I_{OUT} (DGN Package)

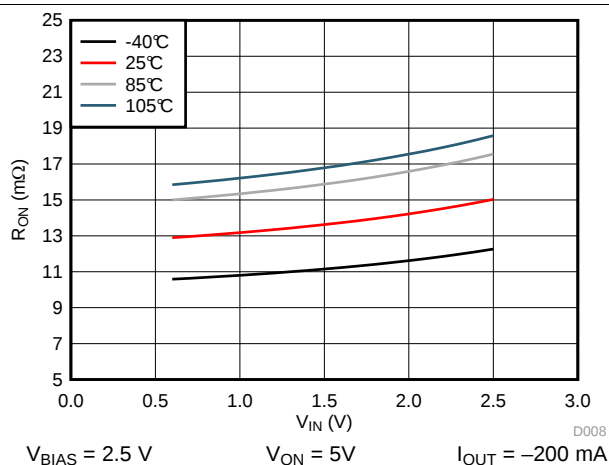


Figure 8. R_{ON} vs V_{IN}

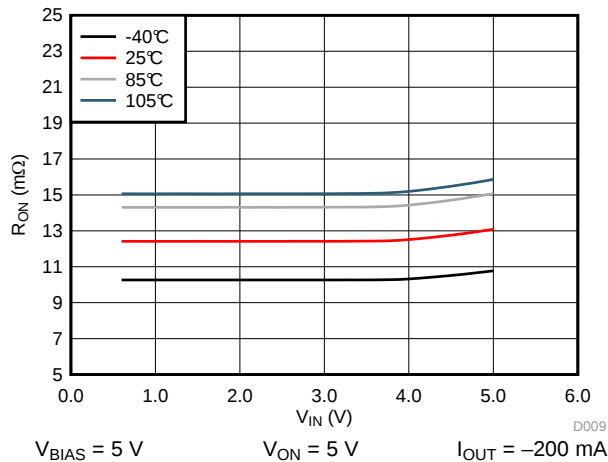


Figure 9. R_{ON} vs V_{IN}

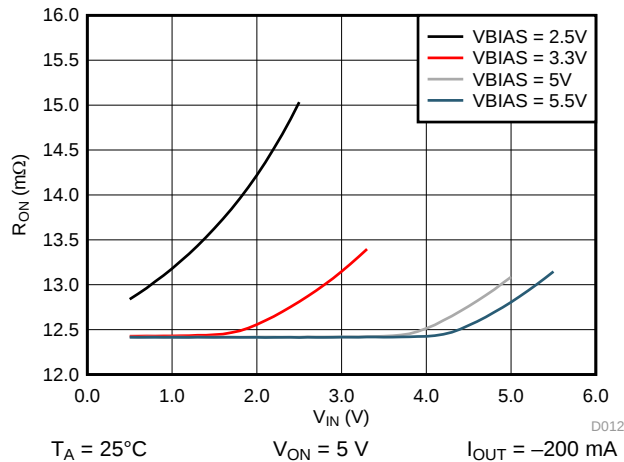


Figure 10. R_{ON} vs V_{IN}

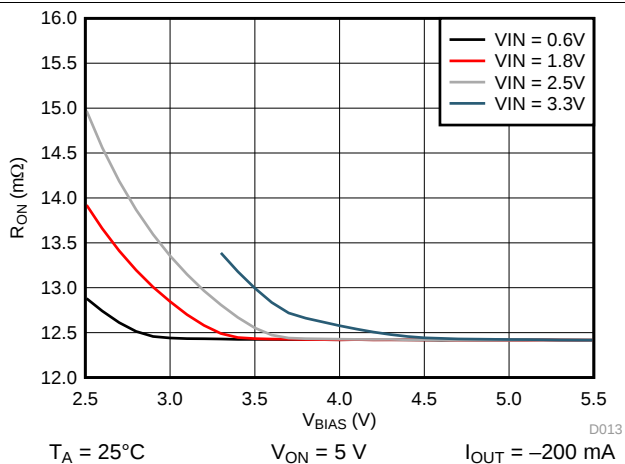


Figure 11. R_{ON} vs V_{BIAS}

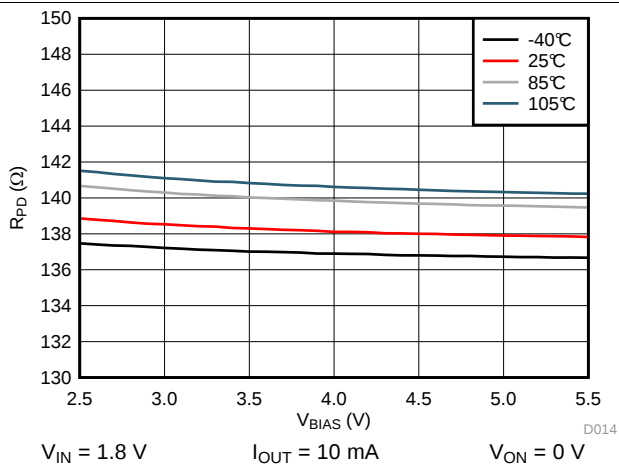
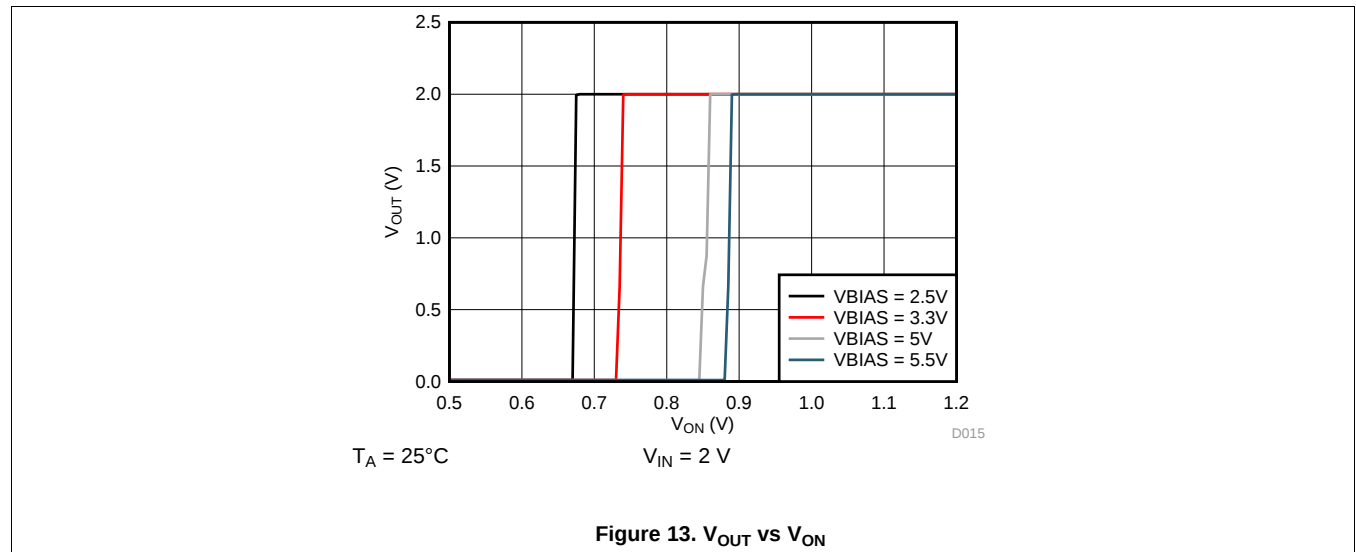


Figure 12. R_{PD} vs V_{BIAS}

Typical DC Characteristics (continued)



7.10 Typical AC Characteristics

$C_{IN} = 1 \mu F$, $C_L = 0.1 \mu F$, $R_L = 10 \Omega$ (unless otherwise specified)

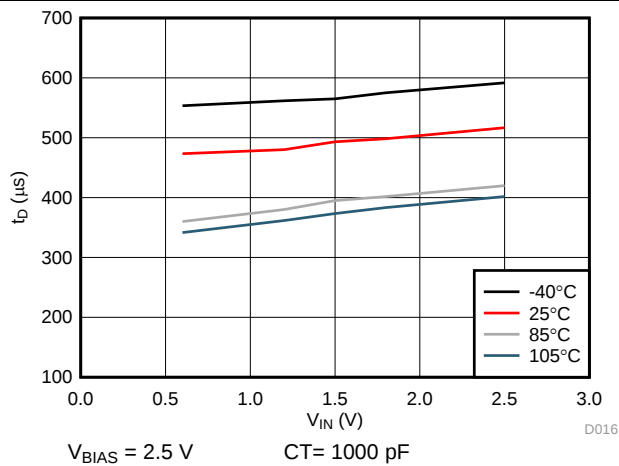


Figure 14. t_D vs V_{IN}

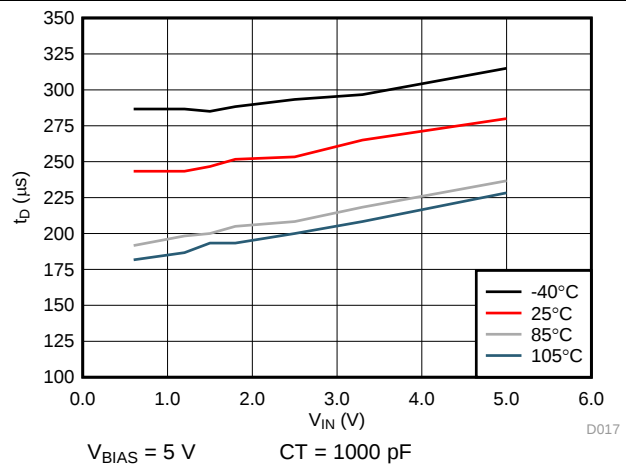


Figure 15. t_D vs V_{IN}

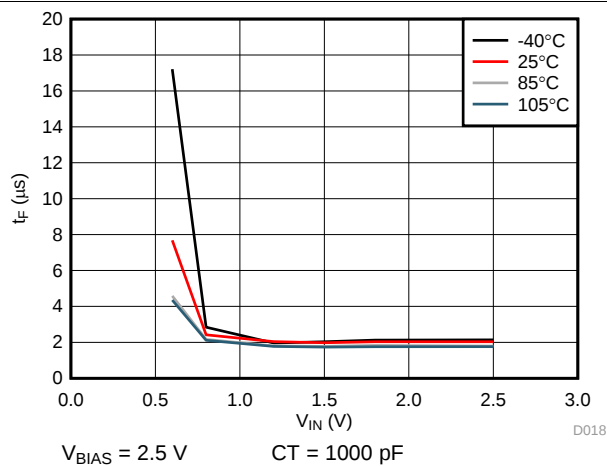


Figure 16. t_F vs V_{IN}

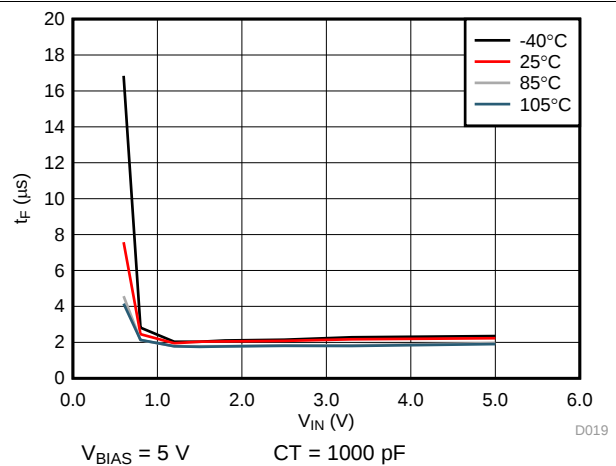


Figure 17. t_F vs V_{IN}

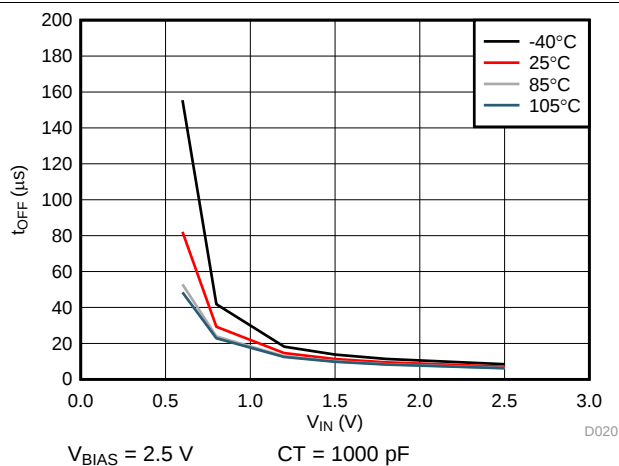


Figure 18. t_{OFF} vs V_{IN}

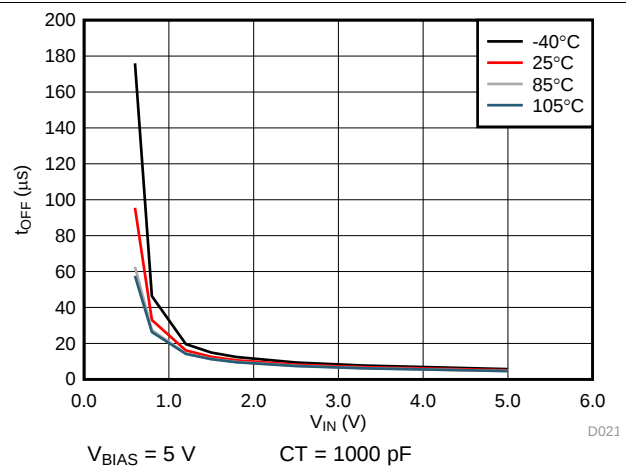
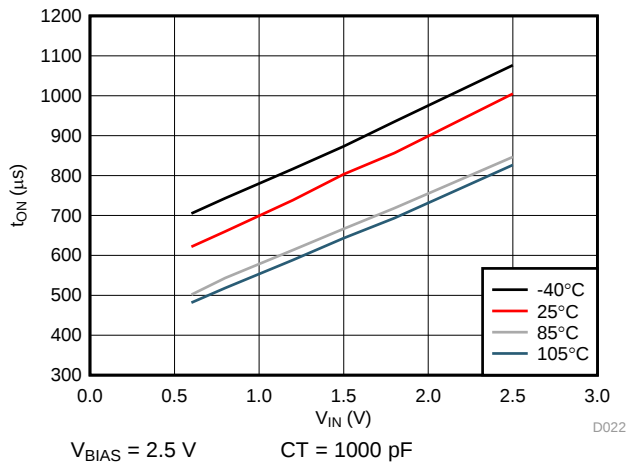
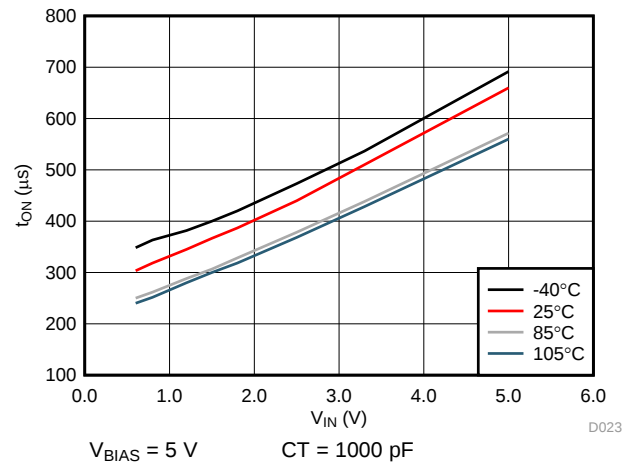
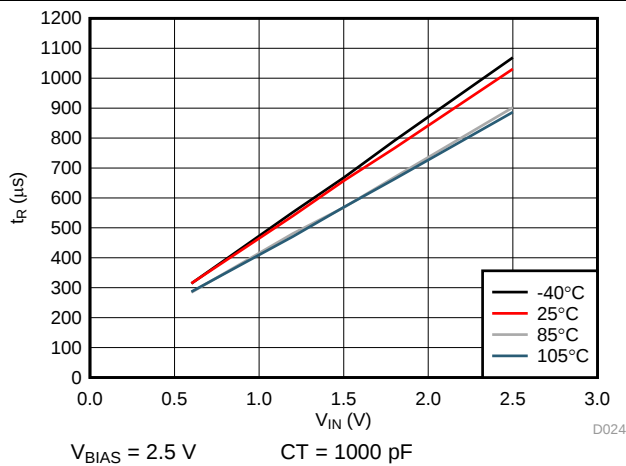
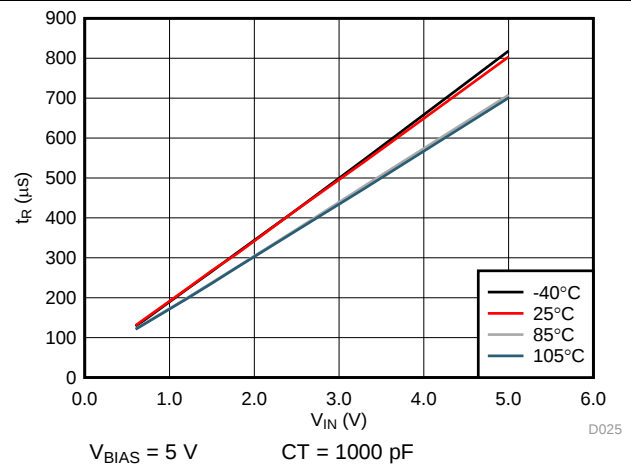
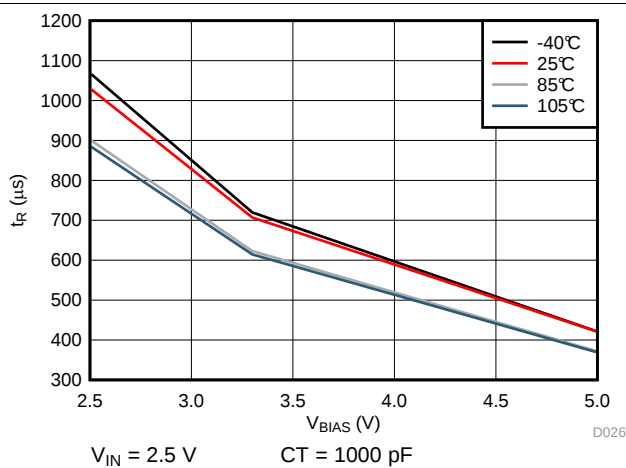
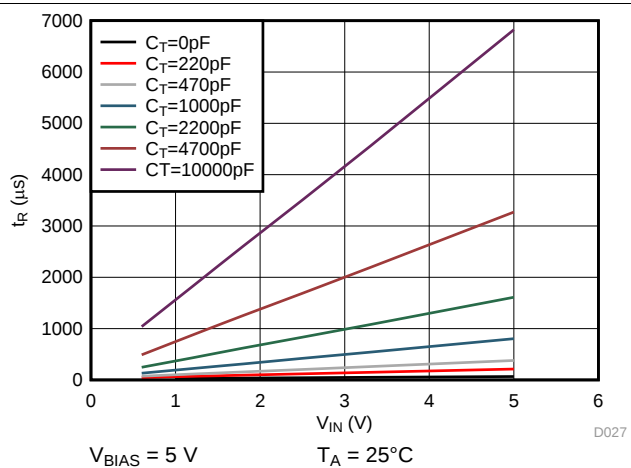


Figure 19. t_{OFF} vs V_{IN}

Typical AC Characteristics (continued)

Figure 20. t_{ON} vs V_{IN}

Figure 21. t_{ON} vs V_{IN}

Figure 22. t_R vs V_{IN}

Figure 23. t_R vs V_{IN}

Figure 24. t_R vs V_{BIAS}

Figure 25. t_R vs V_{IN}

Typical AC Characteristics (continued)

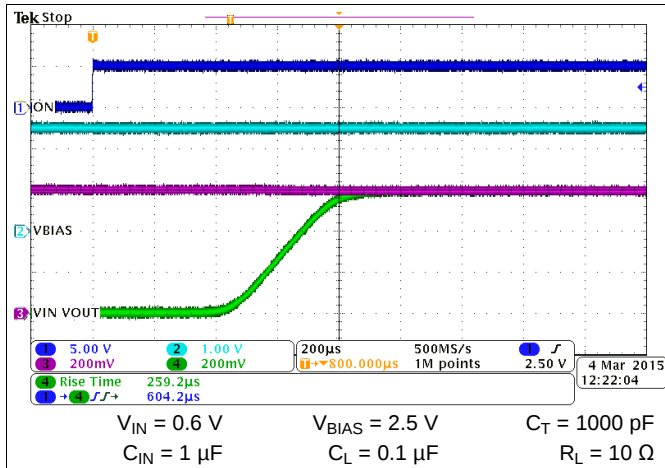


Figure 26. Turn-on Response Time

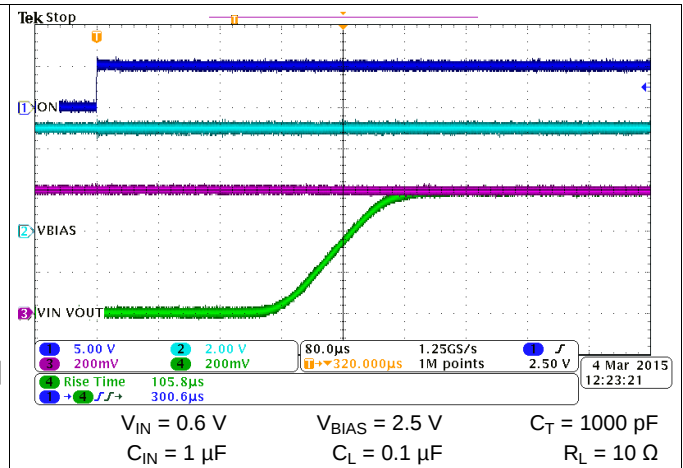


Figure 27. Turn-on Response Time

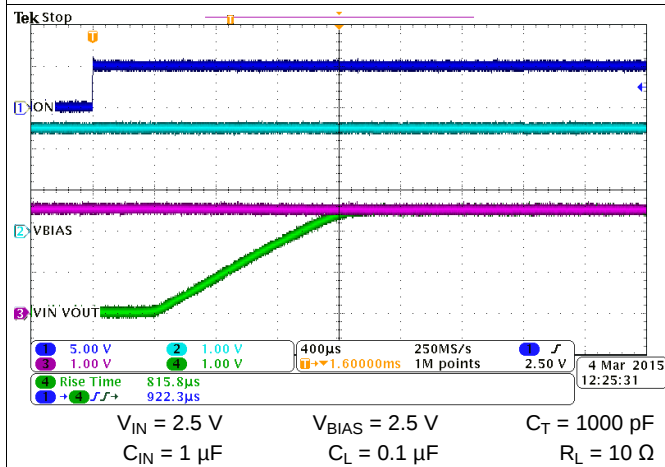


Figure 28. Turn-on Response Time

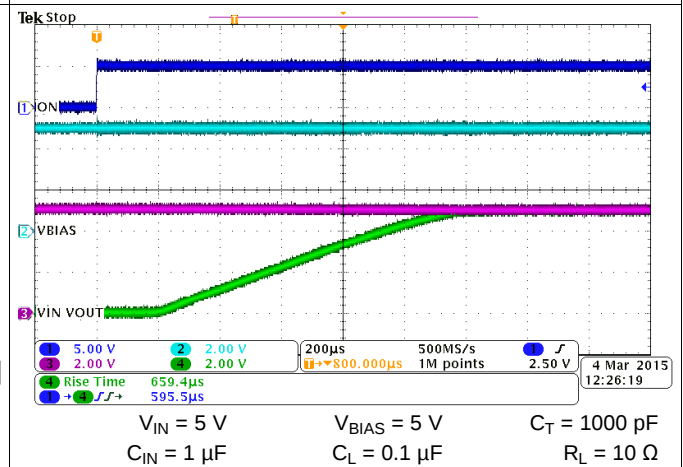


Figure 29. Turn-on Response Time

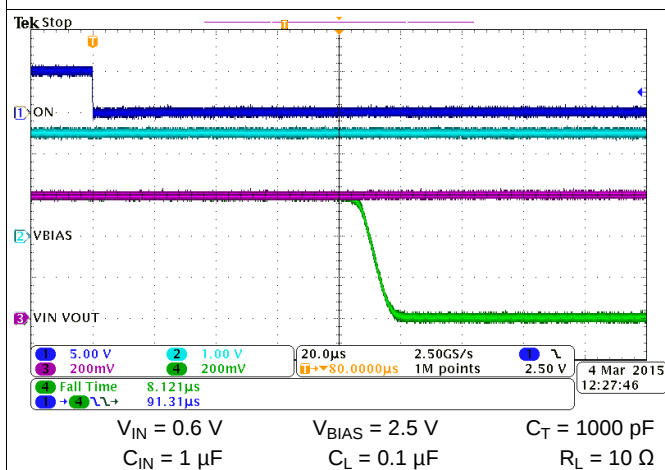


Figure 30. Turn-Off Response Time

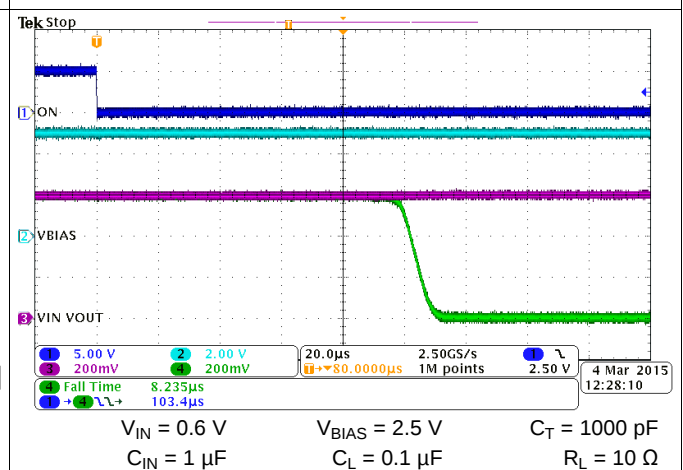


Figure 31. Turn-off Response Time

Typical AC Characteristics (continued)

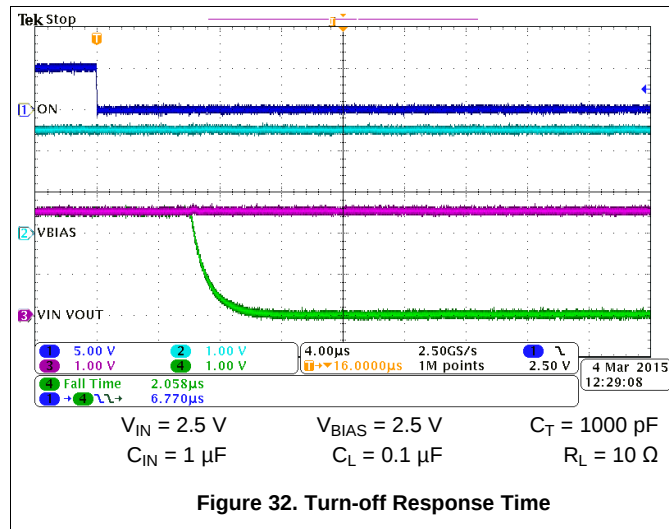


Figure 32. Turn-off Response Time

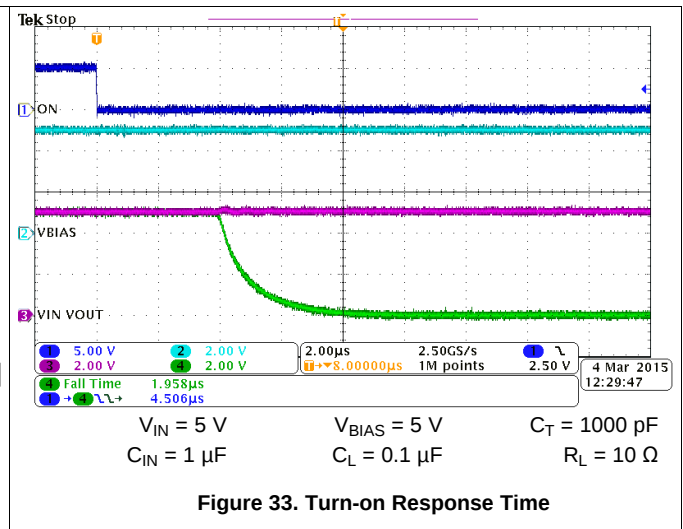
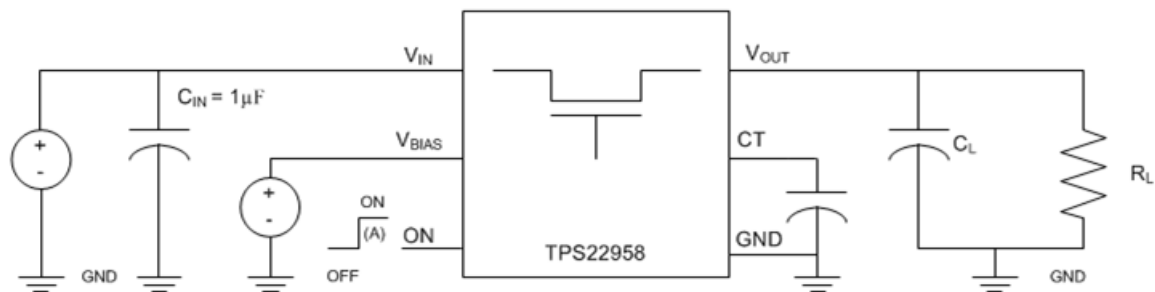
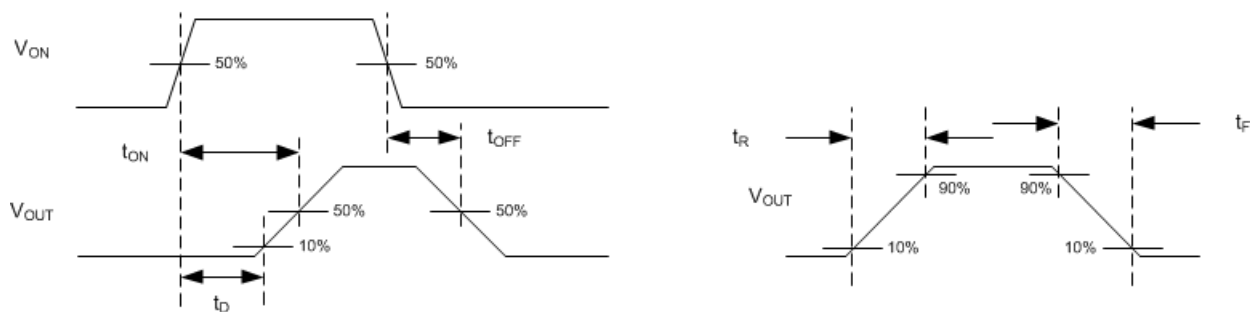


Figure 33. Turn-on Response Time

8 Parameter Measurement Information



Timing test circuit



Timing waveforms

(A) Rise and fall times of the control signal is 100ns.

Figure 34. Test Circuit and Timing Waveforms

9 Detailed Description

9.1 Overview

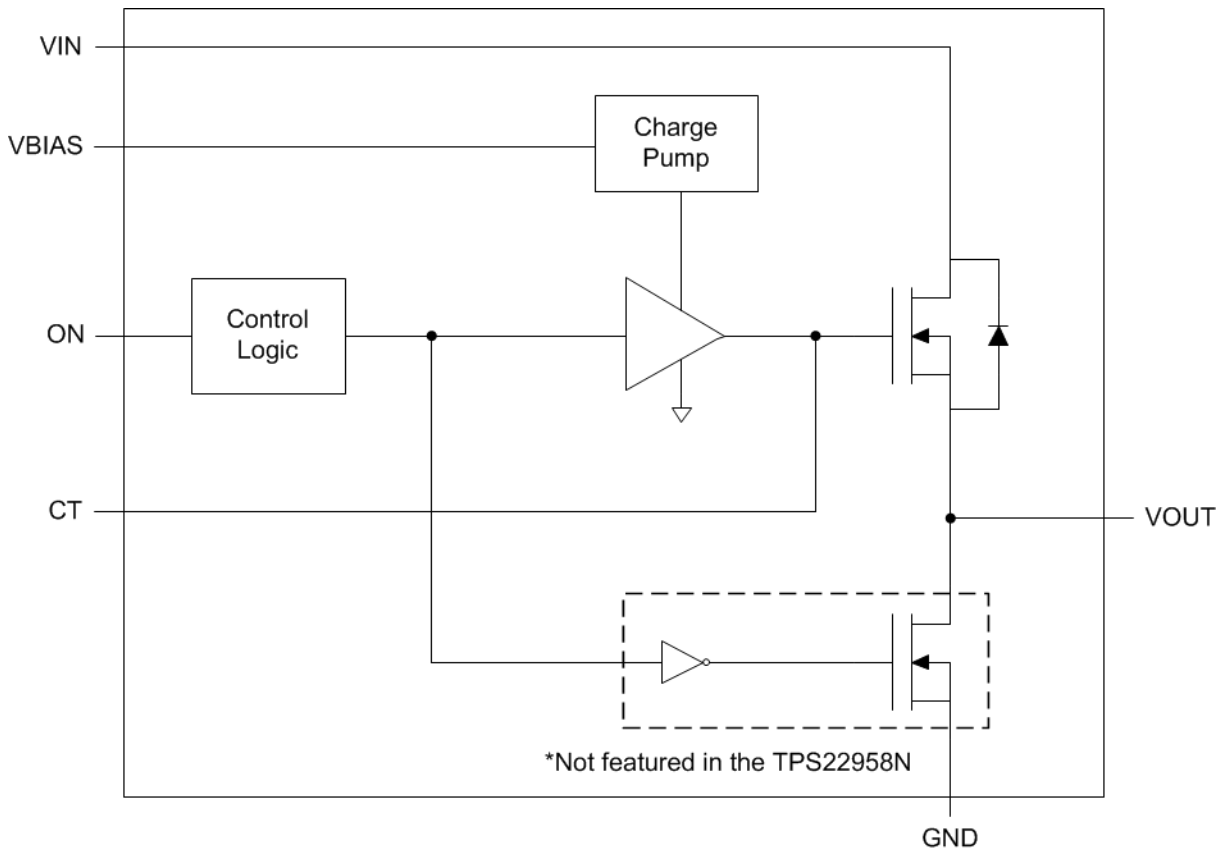
This device is a 5.5 V, 4 A / 6 A, single channel load switch with an adjustable rise time. The device contains an N-channel MOSFET controlled by an on/off GPIO-compatible input. The ON pin must be connected and cannot be left floating. The device is designed to control the turn-on rate and therefore the inrush current. By controlling the inrush current, power supply sag can be reduced during turn on. The slew rate is set by connecting a capacitor from the CT pin to GND.

The slew rate is proportional to the capacitor on the CT pin. Refer to the [Adjustable Rise Time](#) section to determine the correct CT value for a desired rise time.

The internal circuitry is powered by the VBIAS pin, which supports voltages from 2.5 to 5.5 V. This circuitry includes the charge pump, QOD, and control logic. For these internal blocks to function correctly, a voltage between 2.5 and 5.5 V must be supplied to VBIAS.

When a voltage is supplied to VBIAS and the ON pin goes low, the QOD turns on. This connects VOUT to GND through an on-chip resistor and is not a feature for the TPS22958N. The typical pull-down resistance (R_{PD}) is 135 Ω .

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 ON/OFF Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

Feature Description (continued)

9.3.2 Quick Output Discharge (QOD)

The TPS22958 includes a QOD feature while the TPS22958N does not. When the device is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 135 Ω and prevents the output from floating while the switch is disabled.

9.3.3 VIN and VBIAS Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device will still function if $V_{IN} > V_{BIAS}$ but will exhibit an R_{ON} greater than what is listed in the Electrical Characteristics table. See Figure 35 for an example of a typical device. R_{ON} increases as V_{IN} exceeds the V_{BIAS} voltage. For the maximum voltage ratings on the VIN and VBIAS pins, please refer to the [Absolute Maximum Ratings](#) table.

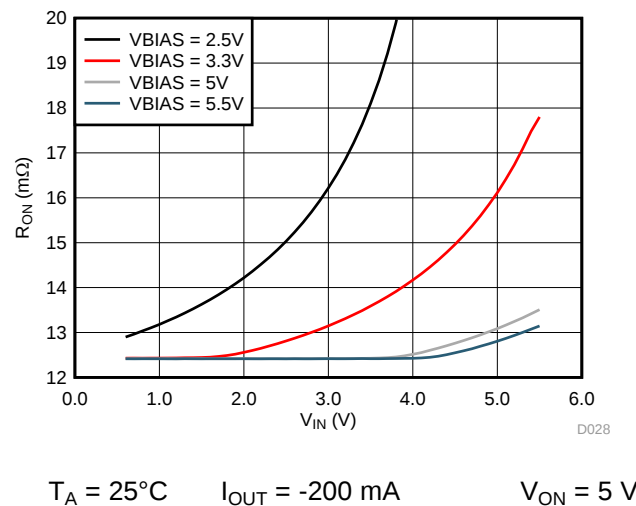


Figure 35. R_{ON} vs V_{IN}

Feature Description (continued)

9.3.4 Adjustable Rise Time

A capacitor from the CT pin to GND sets the slew rate, and it should be rated for 25 V and above. An approximate formula for the relationship between CT and slew rate with $V_{BIAS} = 5\text{ V}$ is:

$$SR = 0.146 \times CT + 14.78$$

where

- SR = slew rate (in $\mu\text{s/V}$)
- CT = the capacitance value on the CT pin (in pF)
- The units for the constant 14.78 is $\mu\text{s/V}$.
- The units for the constant 0.146 is $\mu\text{s}/(\text{V} \times \text{pF})$ (1)

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device.

Table 1. Rise Time Table

CTx (pF)	RISE TIME (μs) 10% - 90%, $C_L = 0.1\text{ }\mu\text{F}$, $C_{IN} = 1\text{ }\mu\text{F}$, $R_L = 10\text{ }\Omega$, $V_{BIAS} = 5\text{ V}$ Typical values at 25°C with a 25-V X7R 10% ceramic capacitor on CT						
	VIN = 5 V	VIN = 3.3 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 0.8 V	VIN = 0.6 V
0	79	59	41	37	33	26	23
220	227	158	97	86	74	55	48
470	397	270	160	139	116	88	72
1000	769	522	301	258	211	153	126
2200	1659	1118	640	548	450	315	256
4700	3445	2314	1315	1128	927	656	528
10000	7310	4884	2778	2372	1950	1379	1103

9.4 Device Functional Modes

The following table lists the VOUT pin connections for a particular device as determined by the ON pin.

Table 2. VOUT Functional Table

ON (Control Input)	TPS22958	TPS22958N
L	GND	Open
H	VIN	VIN

10 Application and Implementation

10.1 Application Information

10.1.1 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor can be placed between VIN and GND. A 1 μ F ceramic capacitor, C_{IN} , placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, TI recommends to have an input capacitor about 10 $\times$ higher than the output capacitor to avoid excessive voltage drop.

10.1.2 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, TI recommends a C_{IN} greater than C_L . A C_L greater than C_{IN} can cause the voltage on VOUT to exceed VIN when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. TI recommends a C_{IN} to C_L ratio of 10 to 1 for minimizing V_{IN} dip caused by inrush currents during startup.

10.1.3 Power Supply Sequencing Without a GPIO Input

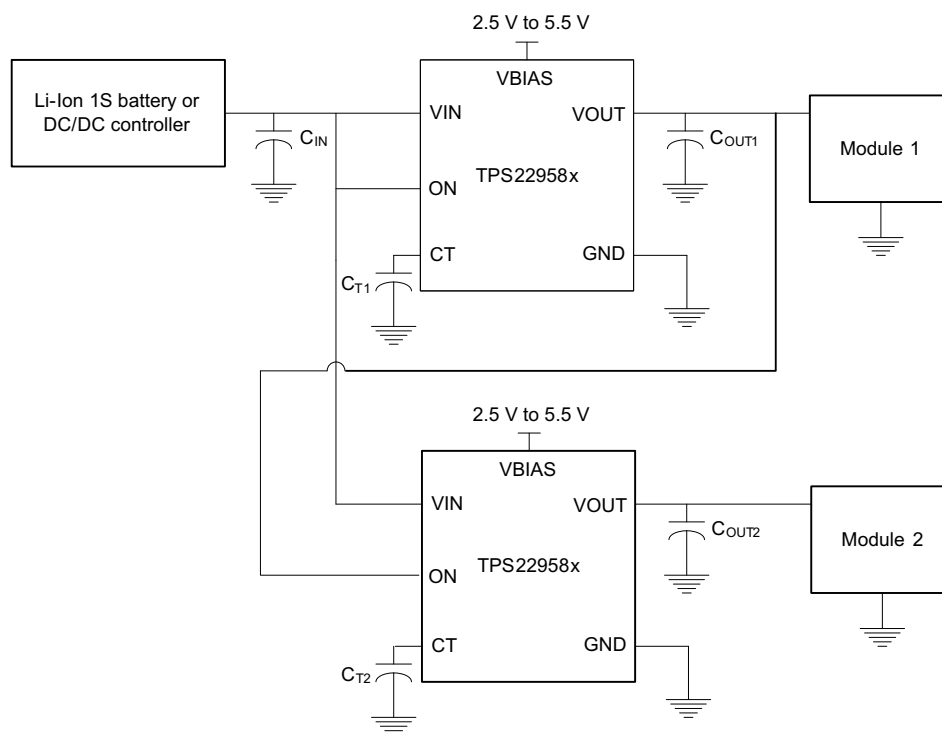


Figure 36. Power Supply Sequencing Without a GPIO Input

In many end equipments, there is a need to power up various modules in a pre-determined manner. The TPS22958x can solve the problem of power sequencing without adding any complexity to the overall system. [Figure 36](#) shows the configuration required for powering up two modules in a fixed sequence. The output of the first load switch is tied to the enable of the second load switch, so when Module 1 is powered the second load switch is enabled and Module 2 is powered.

10.2 Typical Application

This application demonstrates how the TPS22958 can be used to power a downstream load with a large capacitance. The example in Figure 37 is powering a 22 μF capacitive output load.

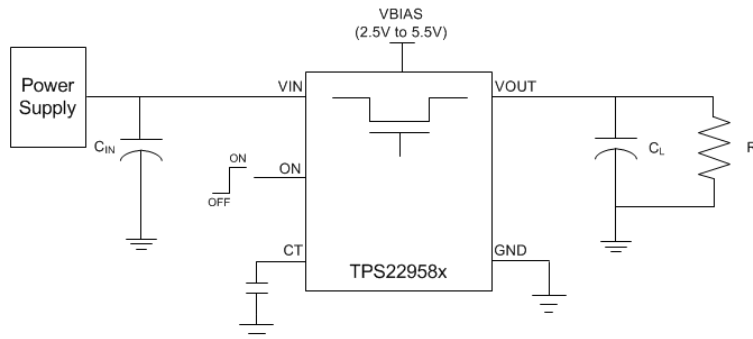


Figure 37. Typical Application Schematic

10.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5.0 V
Load current	4 A
Output capacitance (C_L)	22 μF
Allowable inrush current on VOUT	0.33 A

10.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- V_{IN} voltage
- V_{BIAS} voltage
- Load current
- Allowable inrush current on VOUT due to C_L capacitor

10.2.2.1 V_{IN} to V_{OUT} Voltage Drop

The V_{IN} to V_{OUT} voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table. After the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use Equation 2 to calculate the V_{IN} to V_{OUT} voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON}$$

where

- ΔV = voltage drop from V_{IN} to V_{OUT}
- I_{LOAD} = load current
- R_{ON} = On-resistance of the device for a specific V_{IN} and V_{BIAS} combination

(2)

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.2.2.2 Inrush Current

To determine how much inrush current will be caused by the C_L capacitor, use [Equation 3](#).

$$I_{\text{INRUSH}} = C_L \times \frac{dV_{\text{OUT}}}{dt}$$

where

- I_{INRUSH} = amount of inrush caused by C_L
- C_L = capacitance on VOUT
- dt = time it takes for change in V_{OUT} during the ramp up of VOUT when the device is enabled
- dV_{OUT} = change in V_{OUT} during the ramp up of VOUT when the device is enabled

The device offers adjustable rise time for VOUT and allows the user to control the inrush current during turn-on through the CT pin. The appropriate rise time can be calculated using the design requirements and the inrush current equation ([Equation 3](#)).

$$330 \text{ mA} = 22 \text{ } \mu\text{F} \times 3.3 \text{ V} / dt \quad (4)$$

$$dt = 22 \text{ } \mu\text{F} \times 3.3 \text{ V} / 300 \text{ mA} \quad (5)$$

$$dt = 220 \text{ } \mu\text{s} \quad (6)$$

To ensure an inrush current of less than 330 mA, choose a CT based on [Table 1](#) or [Equation 1](#) value that will yield a rise time of more than 220 μs . See the oscilloscope captures in the [Application Curves](#) for an example of how the CT capacitor can be used to reduce inrush current. See [Table 1](#) for correlation between rise times and CT values.

An appropriate C_L value should be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

10.2.2.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{\text{D(max)}}$ for a given output current and ambient temperature, use [Equation 7](#).

$$P_{\text{D(max)}} = \frac{T_{\text{J(max)}} - T_{\text{A}}}{R_{\theta\text{JA}}}$$

where

- $P_{\text{D(max)}}$ = maximum allowable power dissipation
- $T_{\text{J(max)}}$ = maximum allowable junction temperature (125°C for the TPS22958)
- T_{A} = ambient temperature of the device
- $R_{\theta\text{JA}}$ = junction to air thermal impedance. See [Thermal Information](#). This parameter is highly dependent upon board layout.

For the DGK package, $V_{\text{BIAS}} = 5 \text{ V}$, and $V_{\text{IN}} = 3.3 \text{ V}$, the maximum ambient temperature with a 4 A load can be determined by using the following calculation:

$$P_{\text{D}} = I^2 \times R \quad (8)$$

$$T_{\text{A}} = T_{\text{J(max)}} - R_{\theta\text{JA}} \times P_{\text{D}} \quad (9)$$

$$T_{\text{A}} = T_{\text{J(max)}} - R_{\theta\text{JA}} \times I^2 \times R \quad (10)$$

$$T_{\text{A}} = 125^\circ\text{C} - 185.7^\circ\text{C/W} \times (4 \text{ A})^2 \times 20 \text{ m}\Omega = 65.6^\circ\text{C} \quad (11)$$

Therefore, with the conditions mentioned above, a maximum ambient temperature of 65.6°C is recommended.

For the DGN package, $V_{BIAS} = 5\text{ V}$, and $V_{IN} = 3.3\text{ V}$, the maximum ambient temperature with a 4 A load can be determined by using the following calculation:

$$P_D = I^2 \times R \quad (12)$$

$$T_A = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (13)$$

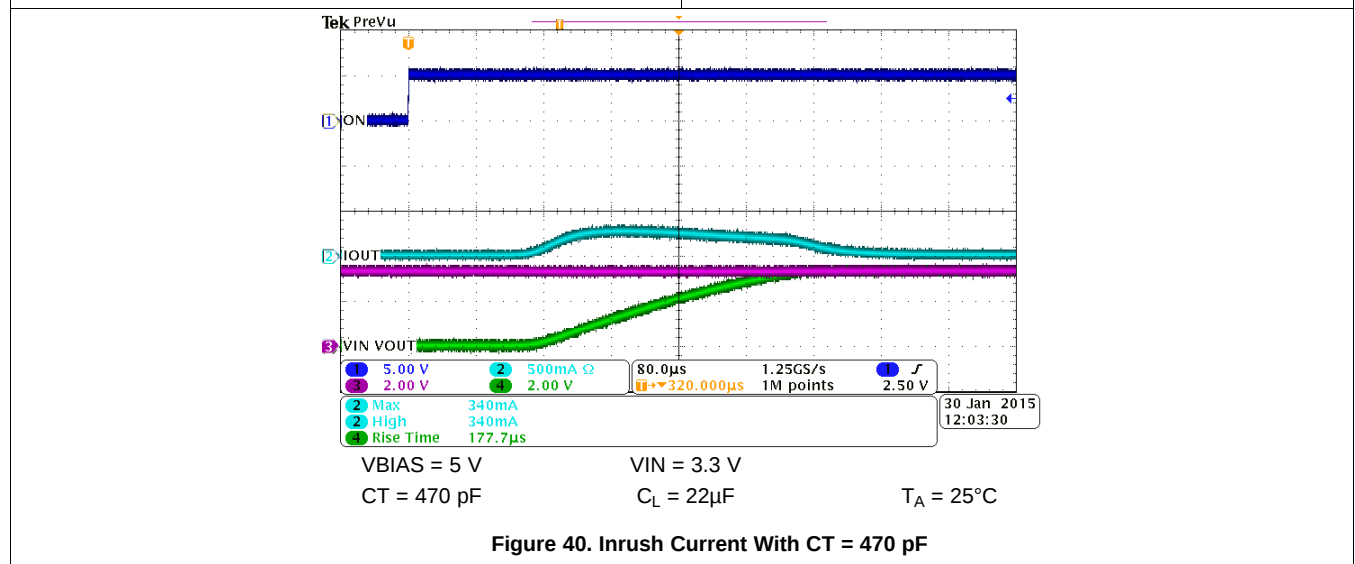
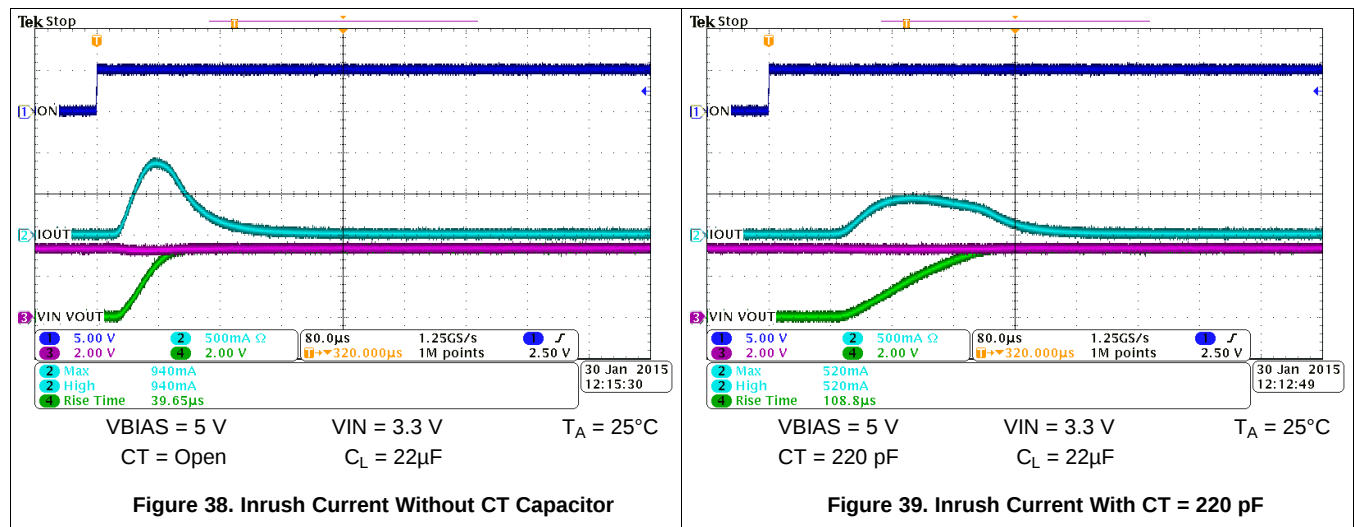
$$T_A = T_{J(MAX)} - R_{\theta JA} \times I^2 \times R \quad (14)$$

$$T_A = 125^\circ\text{C} - 67.0^\circ\text{C/W} \times (4\text{ A})^2 \times 20\text{ m}\Omega = 103.6^\circ\text{C} \quad (15)$$

Therefore, with the conditions mentioned above, a maximum ambient temperature of 103.6°C is recommended.

10.2.3 Application Curves

The three scope captures show the usage of a CT capacitor in conjunction with the device. A higher CT value results in a slower rise and a lower inrush current.



11 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 2.5 to 5.5 V and V_{IN} range of 0.6 to 5.5 V. The power supply should be well regulated and placed as close to the device terminals as possible. It must be able to withstand all transient and load current steps. In most situations, using the minimum recommended input capacitance of 1 μ F is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input. To avoid ringing on the V_{BIAS} pin from a noisy power supply, a bypass capacitance of 0.1 μ F is recommended.

The requirements for large input capacitance can be mitigated by adding additional capacitance to the CT pin. This will cause the load switch to turn on more slowly. Not only will this reduce transient inrush current, but it will also give the power supply more time to respond to the load current step.

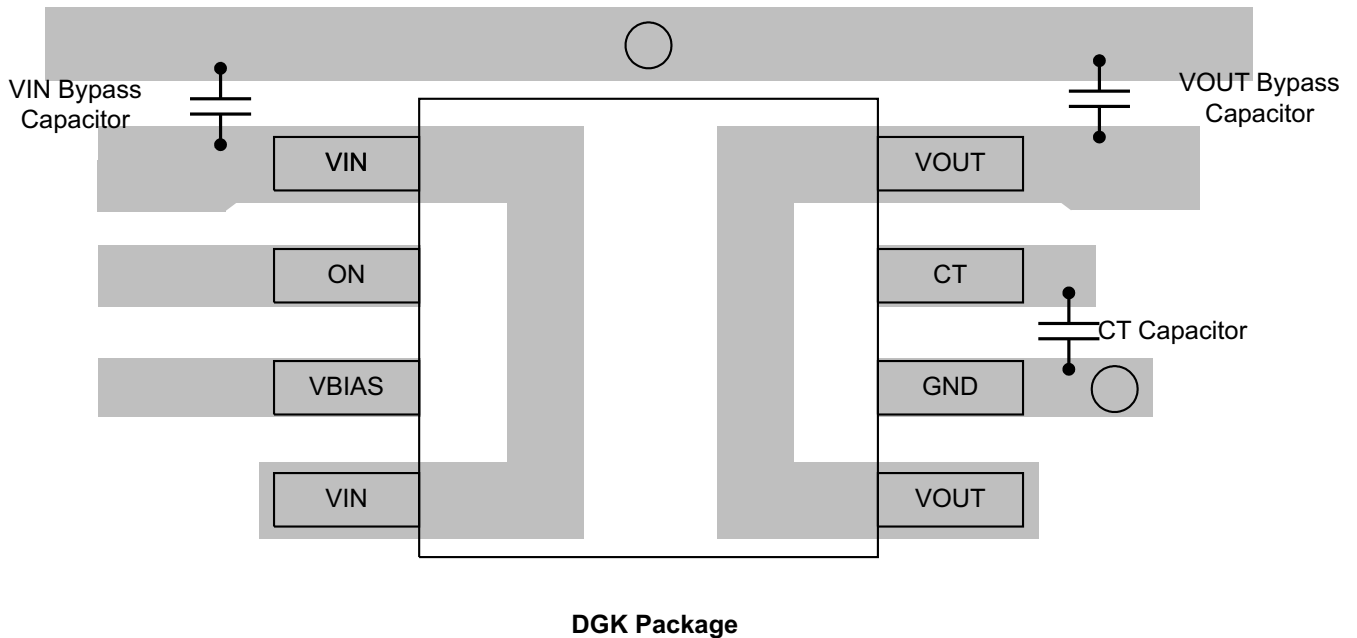
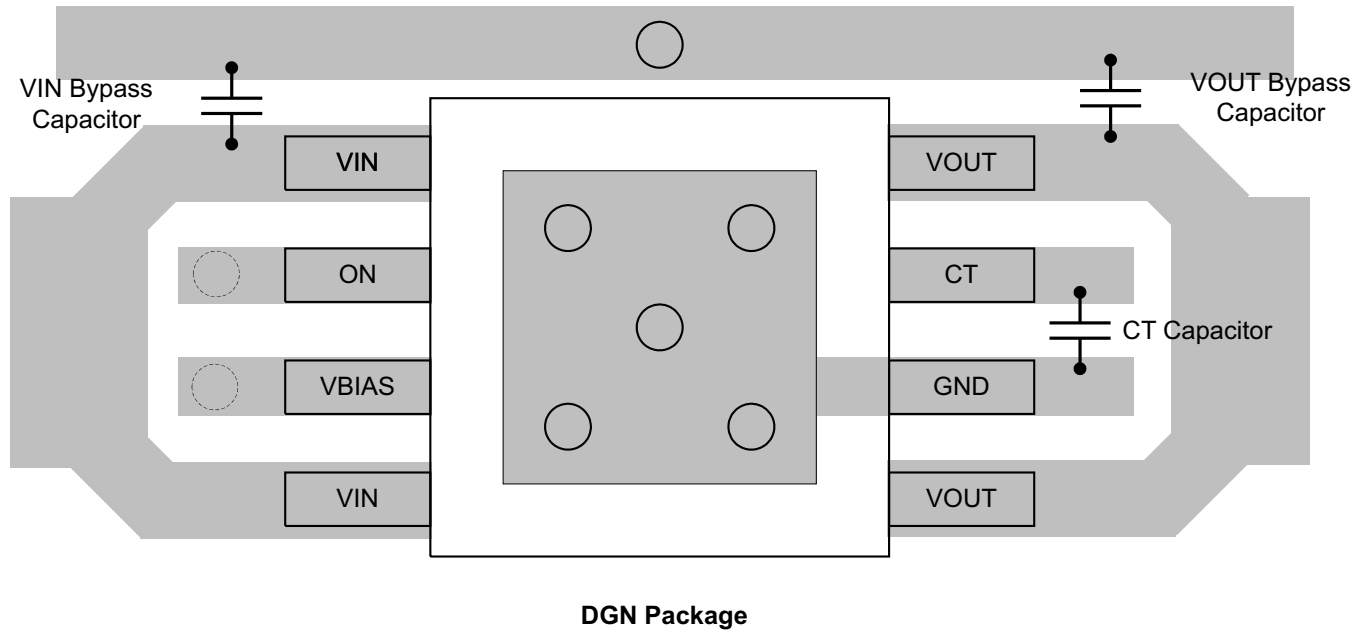
12 Layout

12.1 Layout Guidelines

- V_{IN} and V_{OUT} traces should be as short and wide as possible to accommodate for high current. When connecting the two V_{IN} or V_{OUT} pins together, an equal trace length should be used to avoid an unequal distribution of current through each pin.
- Use vias under the exposed thermal pad to connect to the power ground plane for thermal relief during high current operation.
- V_{IN} pins should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1- μ F ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- V_{OUT} pins should be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the V_{IN} bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device pins as possible.
- The CT capacitor should be placed as close to the device pins as possible. The typical recommended CT capacitance is a capacitor of X5R or X7R dielectric rating with a rating of 25 V or higher.

12.2 Layout Example

○ VIA to Power Ground Plane ○ VIA to another layer



13 器件和文档支持

13.1 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 4. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS22958	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS22958N	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.2 商标

All trademarks are the property of their respective owners.

13.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.4 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22958DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	(ZBUO, ZBUX)
TPS22958DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	(ZBUO, ZBUX)
TPS22958DGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	ZBVX
TPS22958DGNR.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	ZBVX
TPS22958NDGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	ZBWX
TPS22958NDGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	ZBWX
TPS22958NDGNR	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	ZBXX
TPS22958NDGNR.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	ZBXX

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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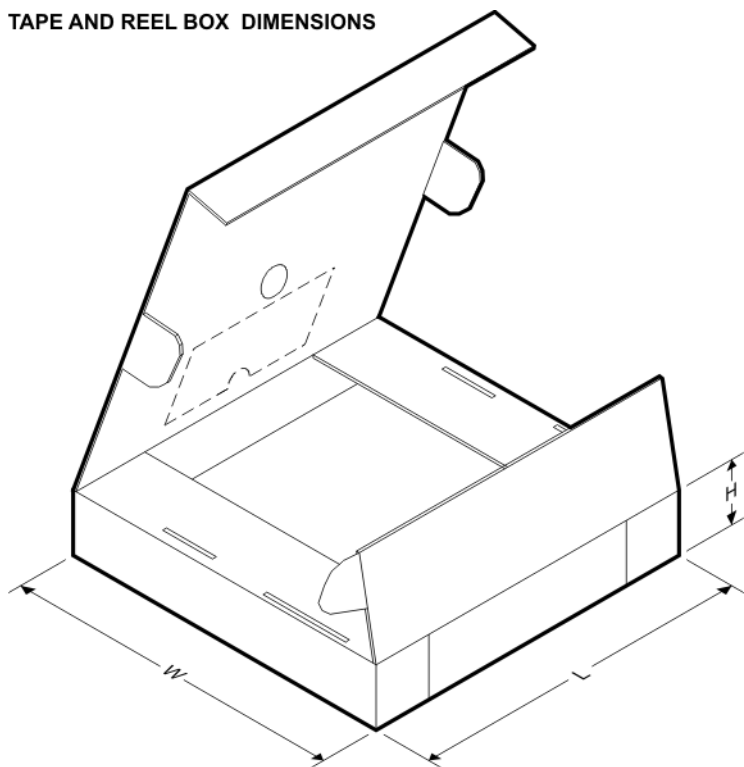
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22958DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS22958DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS22958DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS22958NDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS22958NDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22958DGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0
TPS22958DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TPS22958DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS22958NDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TPS22958NDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0



VSSOP - 1.1 mm max height

Technical drawing of a multi-pin connector. The drawing includes a front view, a side view, and a detail view (Detail A).

Front View Dimensions:

- Overall width: 5.05 TYP (nominal), 4.75 (minimum)
- Pin 1 Index Area: Indicated by a dashed circle.
- Pin 1: 3.1 (nominal), 2.9 (minimum)
- Pin 2: 2.9 (nominal), 2.9 (minimum)
- Pin 3: 2.9 (nominal), 2.9 (minimum)
- Pin 4: 2.9 (nominal), 2.9 (minimum)
- Pin 5: 3.1 (nominal), 2.9 (minimum)
- Pin 6: 3.1 (nominal), 2.9 (minimum)
- Pin 7: 3.1 (nominal), 2.9 (minimum)
- Pin 8: 3.1 (nominal), 2.9 (minimum)

Side View Dimensions:

- Pin 1: 0.65 (nominal), 0.65 (minimum)
- Pin 2: 1.95 (nominal), 1.95 (minimum)
- Pin 3: 0.38 (nominal), 0.25 (minimum)
- Pin 4: 0.38 (nominal), 0.25 (minimum)
- Pin 5: 0.38 (nominal), 0.25 (minimum)
- Pin 6: 0.38 (nominal), 0.25 (minimum)
- Pin 7: 0.38 (nominal), 0.25 (minimum)
- Pin 8: 0.38 (nominal), 0.25 (minimum)

Detail A Dimensions:

- Overall width: 1.1 MAX
- Pin 1: 0.15 (nominal), 0.05 (minimum)
- Pin 2: 0.15 (nominal), 0.05 (minimum)
- Pin 3: 0.15 (nominal), 0.05 (minimum)
- Pin 4: 0.15 (nominal), 0.05 (minimum)
- Pin 5: 0.15 (nominal), 0.05 (minimum)
- Pin 6: 0.15 (nominal), 0.05 (minimum)
- Pin 7: 0.15 (nominal), 0.05 (minimum)
- Pin 8: 0.15 (nominal), 0.05 (minimum)

Callouts:

- NOTE 3: 3.1 (nominal), 2.9 (minimum)
- NOTE 4: 3.1 (nominal), 2.9 (minimum)
- SEATING PLANE: Indicated by a dashed line.
- SEE DETAIL A: Indicated by a dashed circle.

Feature Control Frames:

- Pin 1: $\text{0.13} \text{ (M)} \text{ C A B}$
- Pin 2: $\text{0.13} \text{ (M)} \text{ C A B}$
- Pin 3: $\text{0.13} \text{ (M)} \text{ C A B}$
- Pin 4: $\text{0.13} \text{ (M)} \text{ C A B}$
- Pin 5: $\text{0.13} \text{ (M)} \text{ C A B}$
- Pin 6: $\text{0.13} \text{ (M)} \text{ C A B}$
- Pin 7: $\text{0.13} \text{ (M)} \text{ C A B}$
- Pin 8: $\text{0.13} \text{ (M)} \text{ C A B}$

PowerPAD is a trademark of Texas Instruments.

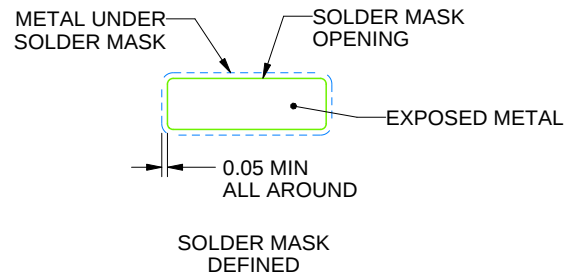
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- TEXAS
INSTRUMENTS
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EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

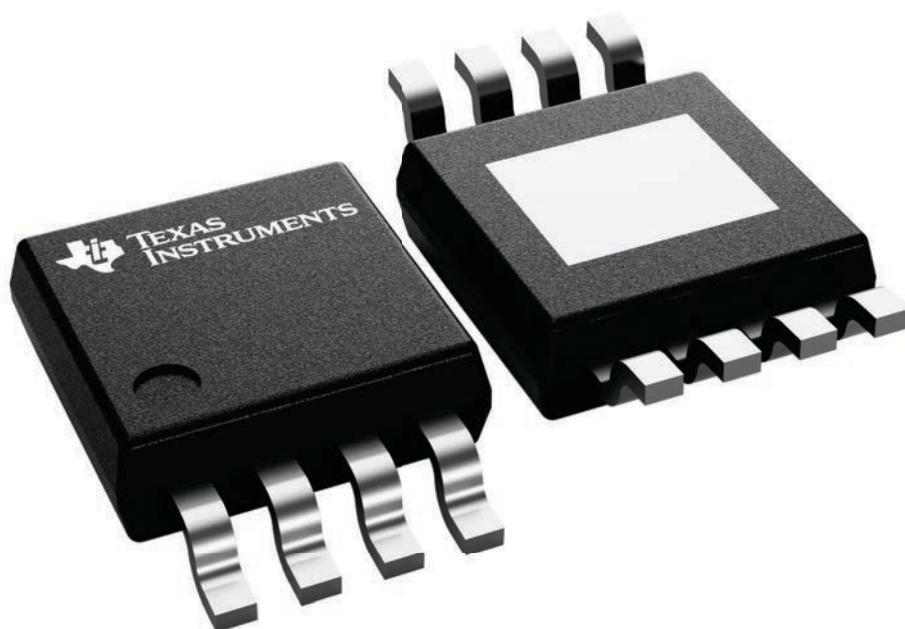
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

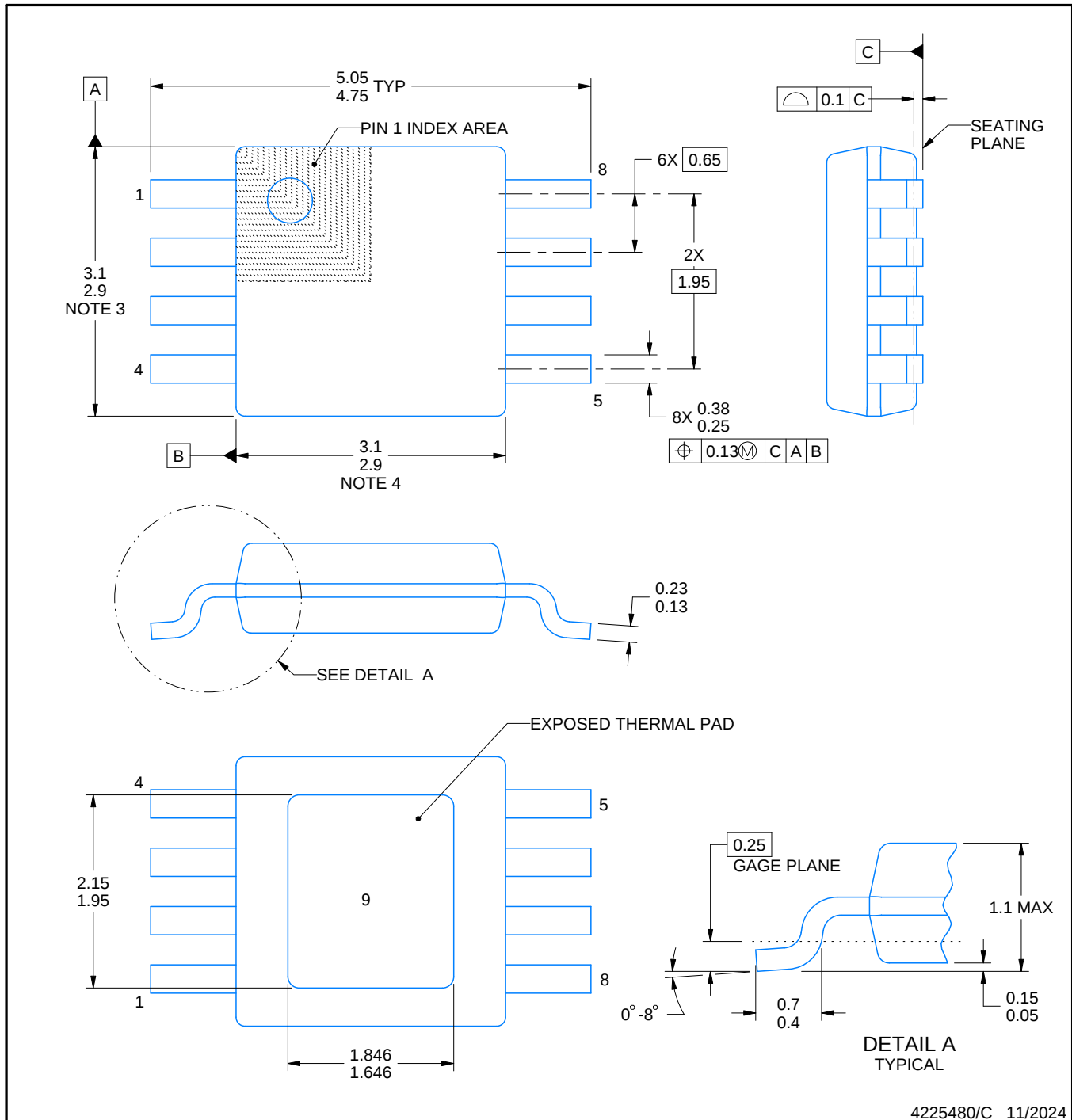
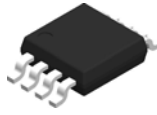
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B



4225480/C 11/2024

NOTES:

PowerPAD is a trademark of Texas Instruments.

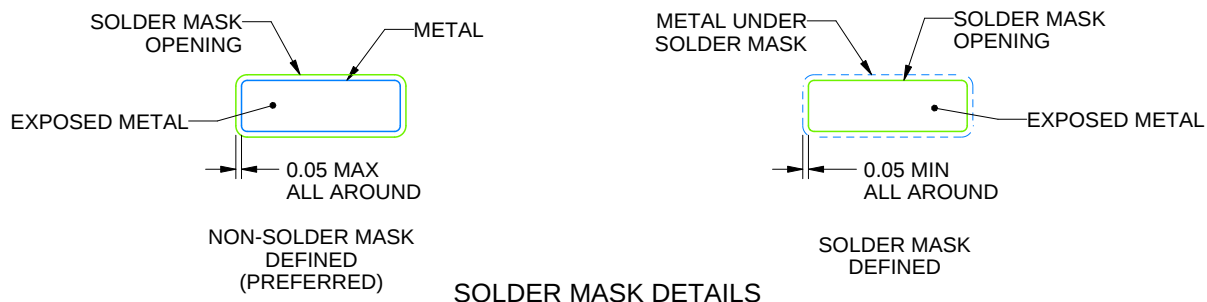
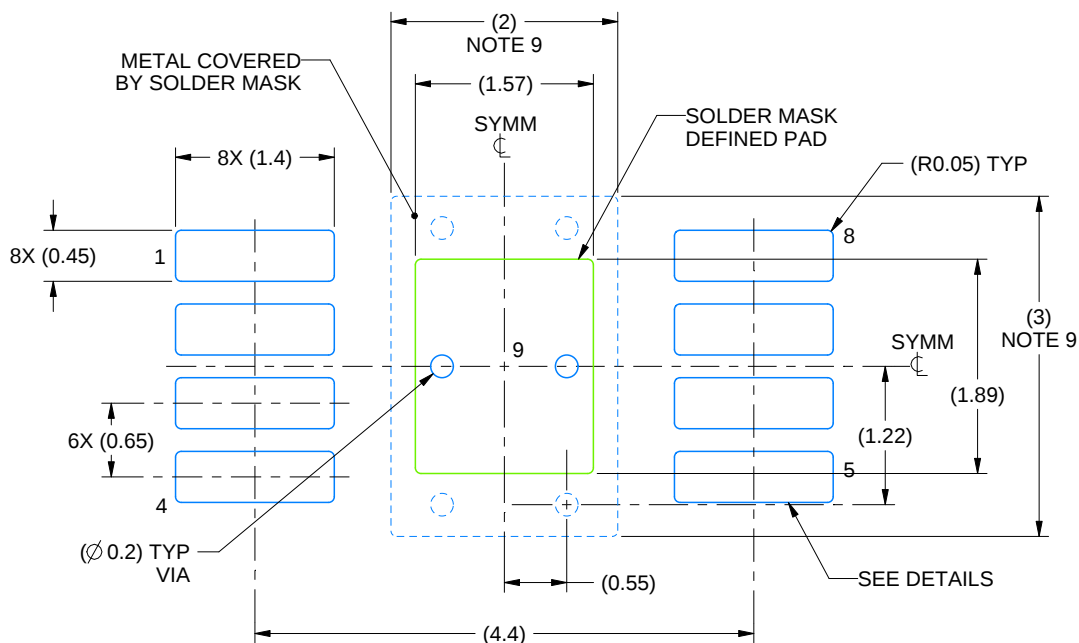
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGN0008G

PowerPAD™ HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4225480/C 11/2024

NOTES: (continued)

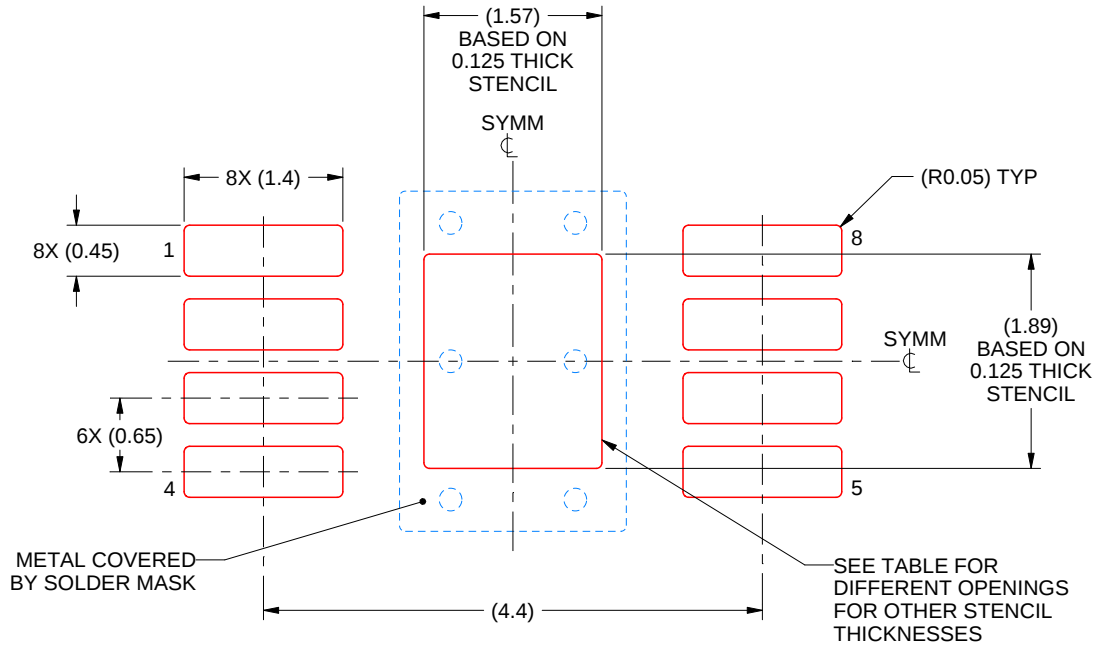
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008G

PowerPAD™ HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月