TPS22960 具有受控开通功能的低输入电压双路负载开关

1 特性

- 集成双路负载开关
- 输入电压范围：1.62V 至 5.5V
- 低导通状态电阻
  - V_{IN} = 5.5V 时，r_{ON} = 342mΩ
  - V_{IN} = 3.3V 时，r_{ON} = 435mΩ
  - V_{IN} = 2.5V 时，r_{ON} = 523mΩ
  - V_{IN} = 1.8V 时，r_{ON} = 737mΩ
- 500mA 最大连续开关电流
- 低静态电流和关断电流
- 受控开关输出上升时间：
  75μs 或 660 μ s
- 集成式快速输出放电晶体管
- ESD 性能测试符合 JESD 22 标准
  - 2000V 人体放电模型
    （A114-B，II 类）
  - 1000V 充电器件模型 (C101)
- 8 引脚 SOT (DCN) 封装：3mm x 3mm
- 8 引脚 UQFN (RSE) 封装：1.5mm x 1.5mm

2 应用

- GPS 器件
- 手机/PDA
- MP3 播放器
- 数码照相机

3 说明

TPS22960 是一款小型、低 r_{ON} 负载开关，具有受控导通功能。该器件包含两个可在 1.62V 至 5.5V 的输入电压范围内运行的 P 沟道 MOSFET。每个开关由一个导通/关断输入（ON1 和 ON2）单独控制，此输入可与低压控制信号直接连接。为能够在开关关断时快速进行输出放电，TPS22960 添加了一个 85Ω 的片上负载电阻。

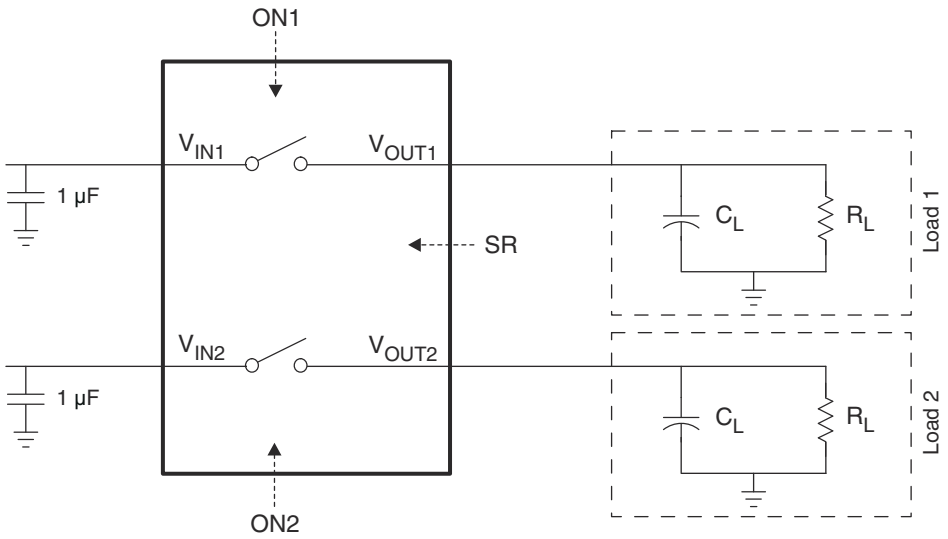
该器件的上升时间（压摆率）由内部控制，以避免浪涌电流，如果需要，可以使用 SR 引脚来减慢该时间：在 3.3V 下，TPS22960 在 SR 引脚接地时具有 75 μ s 上升时间，并在 SR 引脚连接高电平时具有 660 μ s 上升时间。

TPS22960 采用节省空间的 8 引脚 UQFN 封装和 8 引脚 SOT 封装。其在自然通风环境下的额定运行温度范围为 -40°C 至 85°C。

封装信息

器件型号	封装(1)	封装尺寸(2)
TPS22960	DCN（SOT，8）	2.90mm x 1.63mm
	RSE（UQFN，8）	1.50mm x 1.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简图

Table of Contents

4 Pin Configuration and Functions

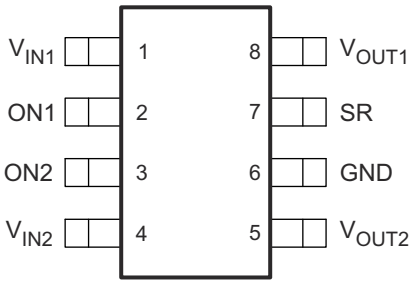


图 4-1. DCN Package, 8-pin SOT (Top View)

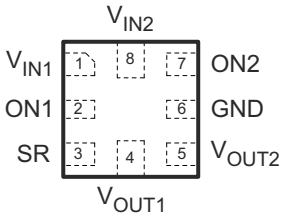


图 4-2. RSE Package, 8-pin UQFN (Top View)

表 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT	UQFN		
V_{IN1}	1	1	I	Switch 1 input; bypass this input with a ceramic capacitor to GND.
ON1	2	2	I	Switch 1 control input, active high. Do not leave floating.
ON2	3	7	I	Switch 2 control input, active high. Do not leave floating.
V_{IN2}	4	8	I	Switch 2 input; bypass this input with a ceramic capacitor to GND.
V_{OUT2}	5	5	O	Switch 2 output.
GND	6	6	—	Ground.
SR	7	3	I	Slew rate control pin. SR = GND translates into a 75-μs rise time; SR = high translates into a 660-μs rise time.
V_{OUT1}	8	4	O	Switch 1 output.

5 Specifications

5.1 Absolute Maximum Ratings

(see (1))

		MIN	MAX	UNIT
V_{IN}	Input voltage	– 0.3	6	V
V_{OUT}	Output voltage		V_{IN} + 0.3	V
V_{ON}	Input voltage	– 0.3	6	V
I_{MAX}	Maximum continuous switch current		0.5	A
T_A	Operating free-air temperature	– 40	85	°C
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature	– 65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{IN}	Input voltage		1.62	5.5	V
V_{OUT}	Output voltage			V_{IN}	V
V_{IH}	High-level input voltage: ON1, ON2, SR	V_{INx} = 3.0 V to 5.5 V	1.5	5.5	V
		V_{INx} = 1.62 V to 3.0 V	1.4	5.5	
V_{IL}	Low-level input voltage: ON1, ON2, SR	V_{INx} = 3.0 V to 5.5 V		0.5	V
		V_{INx} = 1.62 V to 3.0 V		0.4	
C_{IN}	Input capacitor		1(1)		µF

(1) See 节 8.1.

5.4 Thermal Information

THERMAL METRIC(1)		DCN (SOT) 8 PINS	RSE (UQFN) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	254	124	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	122	67	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	181	31.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22	2.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	178	31.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* (SPRA953).

5.5 Electrical Characteristics

V_{IN} = 1.62 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP(1)	MAX	UNIT
I_{IN}	Quiescent current (each switch)	I_{OUTx} = 0, V_{INx} = V_{ON}	V_{INx} = 5.5 V	Full		0.64	2	µA
			V_{INx} = 3.3 V	Full		0.35	1.2	
			V_{INx} = 2.5 V	Full		0.24	0.8	
			V_{INx} = 1.8 V	Full		0.15	0.5	
$I_{IN(OFF)}$	OFF-state supply current (each switch)	V_{ON} = GND, V_{OUTx} = Open	V_{INx} = 5.5 V	Full		0.47	3.6	µA
			V_{INx} = 3.3 V	Full		0.25	1.8	
			V_{INx} = 2.5 V	Full		0.18	1.3	
			V_{INx} = 1.8 V	Full		0.11	1.2	
r_{ON}	ON-state resistance (each switch)	I_{OUT} = –200 mA	V_{INx} = 5.5 V	25°C		342	400	mΩ
				Full			465	
			V_{INx} = 3.3 V	25°C		435	500	
				Full			595	
			V_{INx} = 2.5 V	25°C		523	620	
				Full			720	
			V_{INx} = 1.8 V	25°C		737	1100	
				Full			1300	
			V_{INx} = 1.62 V	25°C		848	1300	
				Full			1500	
r_{PD}	Output pulldown resistance	V_{IN} = 3.3 V, V_{ON} = 0, I_{OUT} = 30 mA		25°C		85	120	Ω
I_{ON}	ON-state input leakage current	V_{ON} = 1.62 V to 5.5 V or GND		Full			0.25	µA

(1) Typical values are at T_A = 25°C.

5.6 Switching Characteristics

V_{IN} = 3.3 V, T_A = 25°C, RL_CHIP = 85 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{ON}	Turn-ON time	R_L = 33 Ω, C_L = 0.1 µF	SR = V_{IN}		635		µs
			SR = GND		67		
t_{OFF}	Turn-OFF time	R_L = 33 Ω, C_L = 0.1 µF	SR = V_{IN}		4.5		µs
			SR = GND		4.2		
t_r	V_{OUT} rise time	R_L = 33 Ω, C_L = 0.1 µF	SR = V_{IN}		660		µs
			SR = GND		75		
t_f	V_{OUT} fall time	R_L = 33 Ω, C_L = 0.1 µF	SR = V_{IN}		4.5		µs
			SR = GND		4.5		

(1) Typical values are at the specified V_{IN} = 3.3 V and T_A = 25°C.

5.7 Typical DC Characteristics

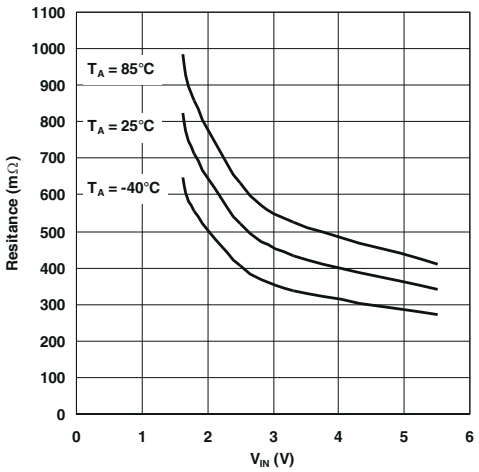


图 5-1. ON Resistance vs Input Voltage

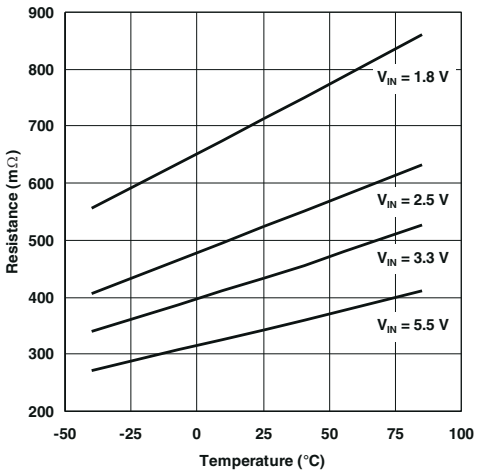


图 5-2. ON Resistance vs Temperature

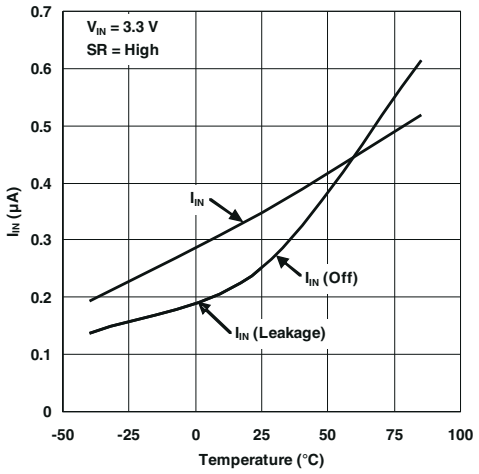


图 5-3. Quiescent Current vs Temperature

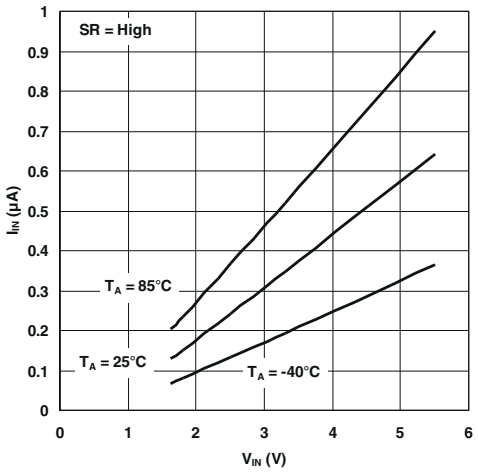


图 5-4. Quiescent Current vs Input Voltage

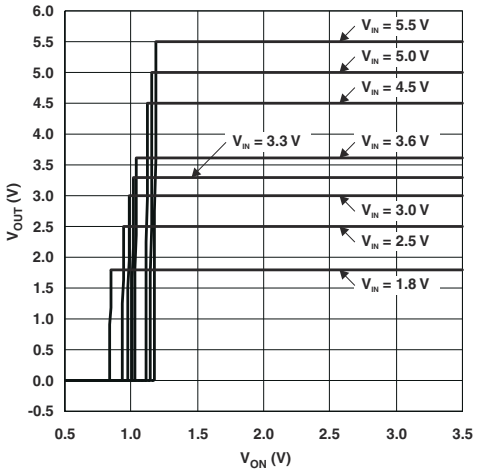


图 5-5. ON Threshold

5.8 Typical Switching Characteristics

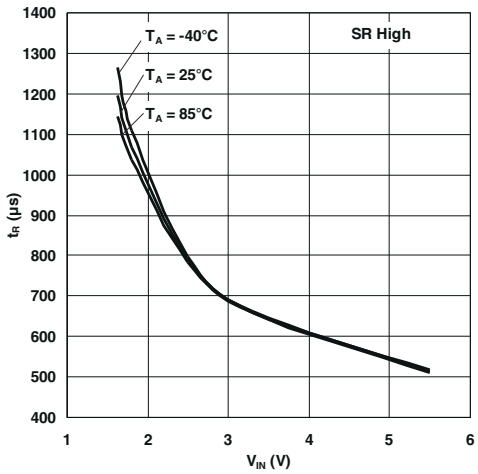


图 5-6. Rise Time vs Input Voltage

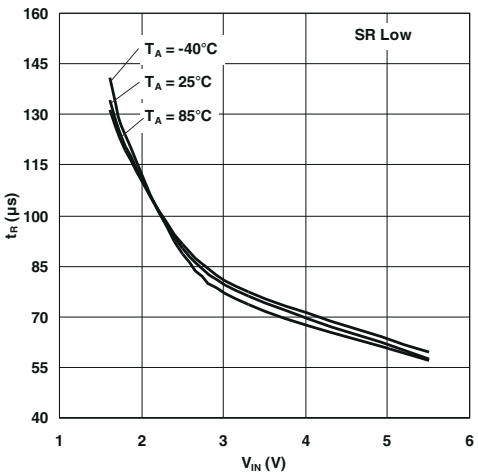


图 5-7. Rise Time vs Input Voltage

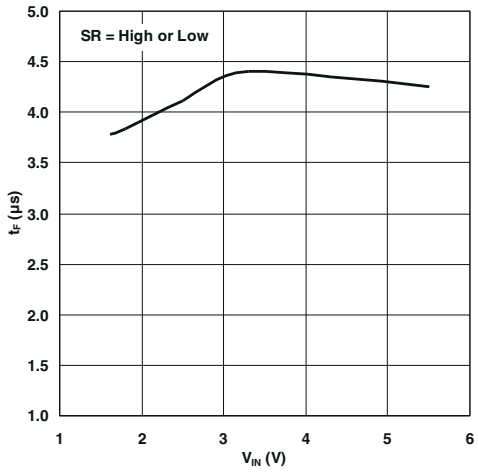


图 5-8. Fall Time vs Input Voltage

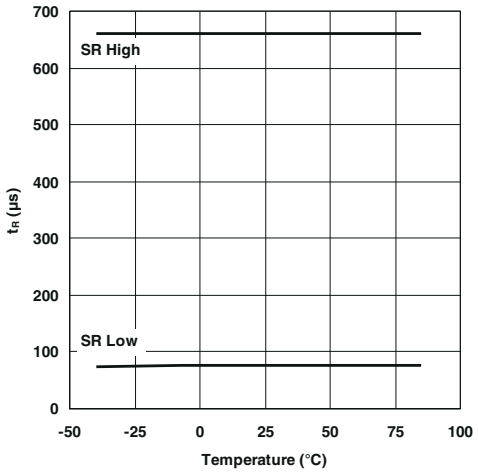


图 5-9. Rise Time vs Temperature

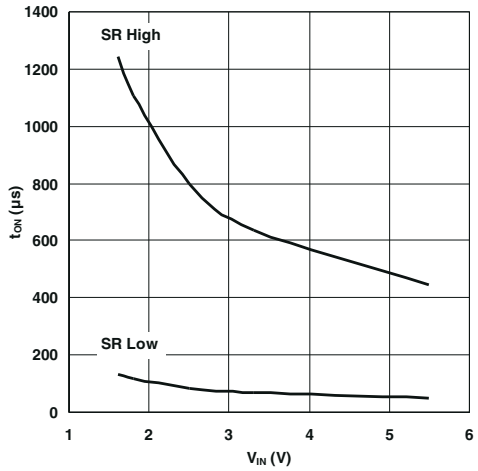


图 5-10. On Time vs Input Voltage

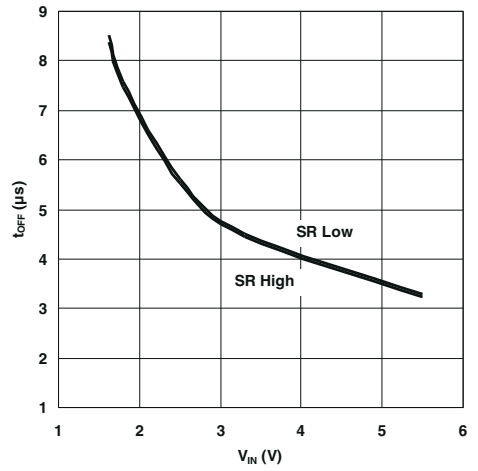


图 5-11. Off Time vs Input Voltage

5.8 Typical Switching Characteristics (continued)

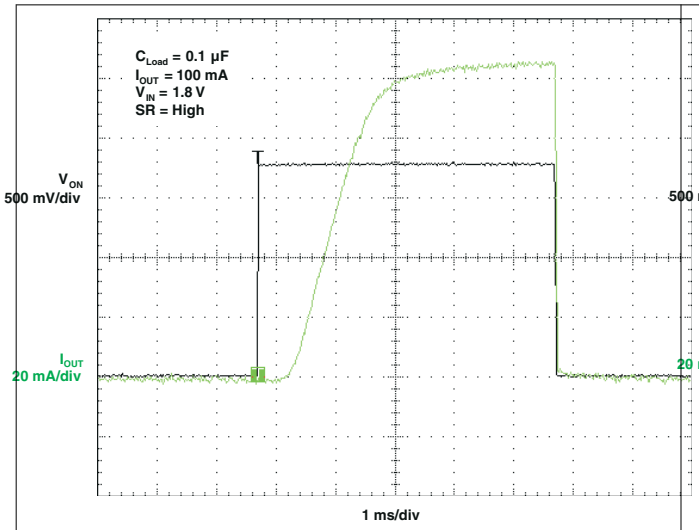


图 5-12. t_{ON} Response

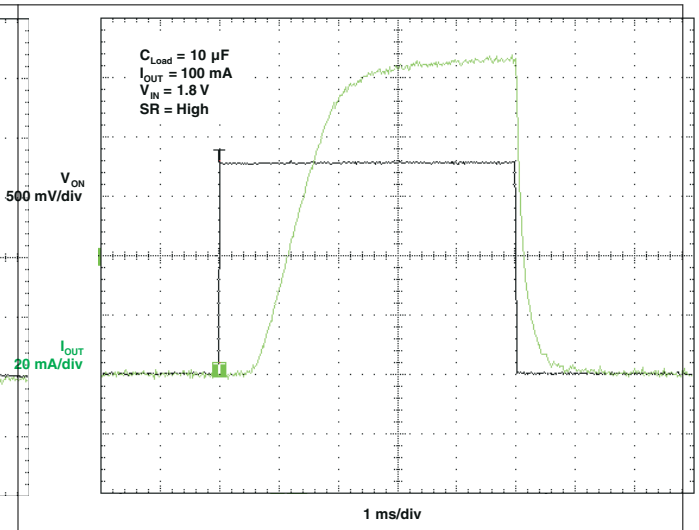


图 5-13. t_{ON} Response

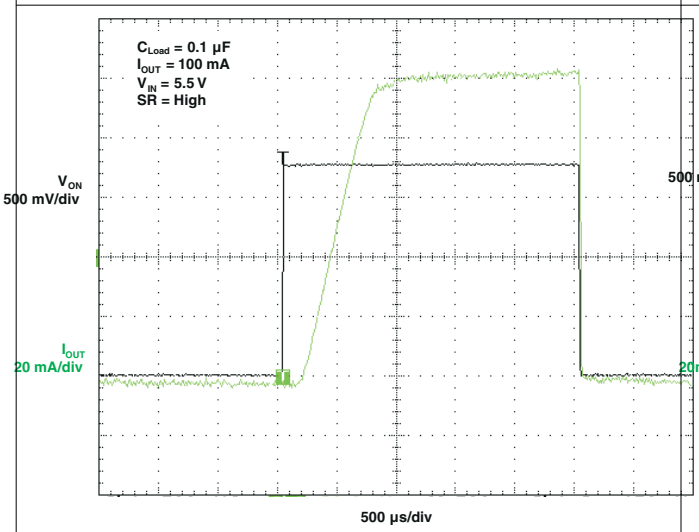


图 5-14. t_{ON} Response

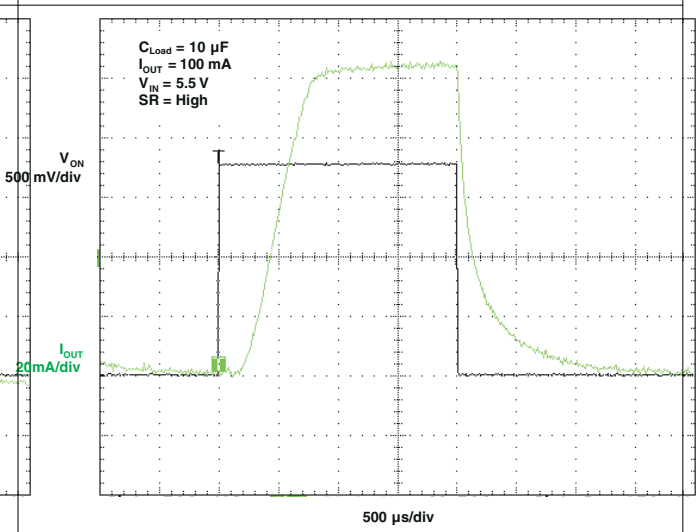


图 5-15. t_{ON} Response

5.8 Typical Switching Characteristics (continued)

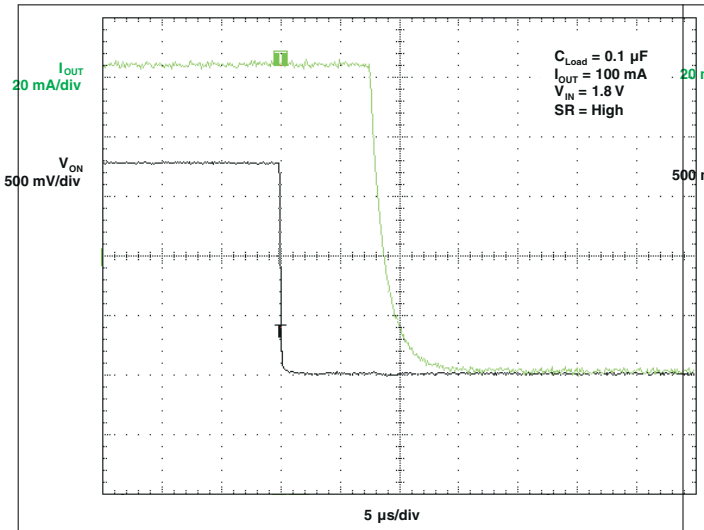


图 5-16. t_{OFF} Response

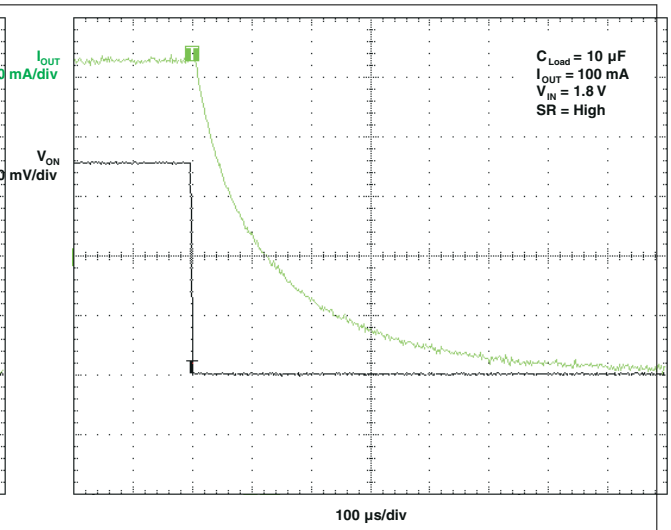


图 5-17. t_{OFF} Response

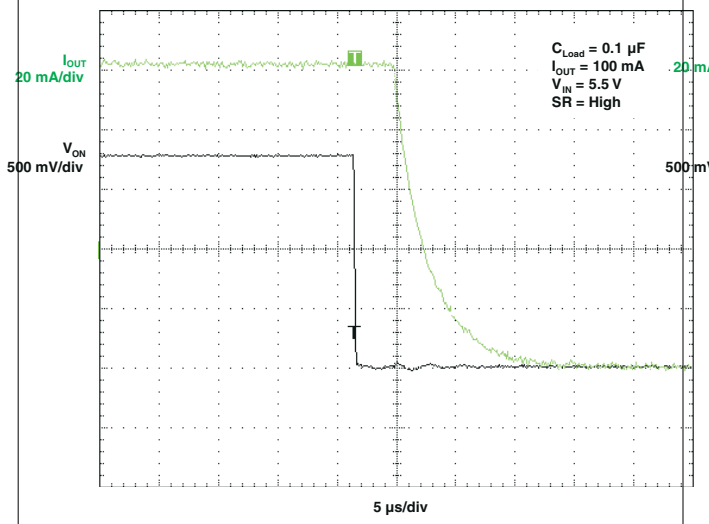


图 5-18. t_{OFF} Response

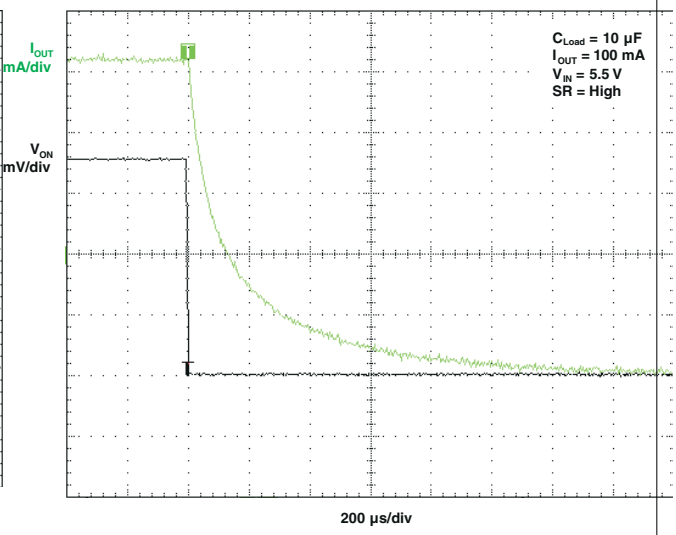


图 5-19. t_{OFF} Response

5.8 Typical Switching Characteristics (continued)

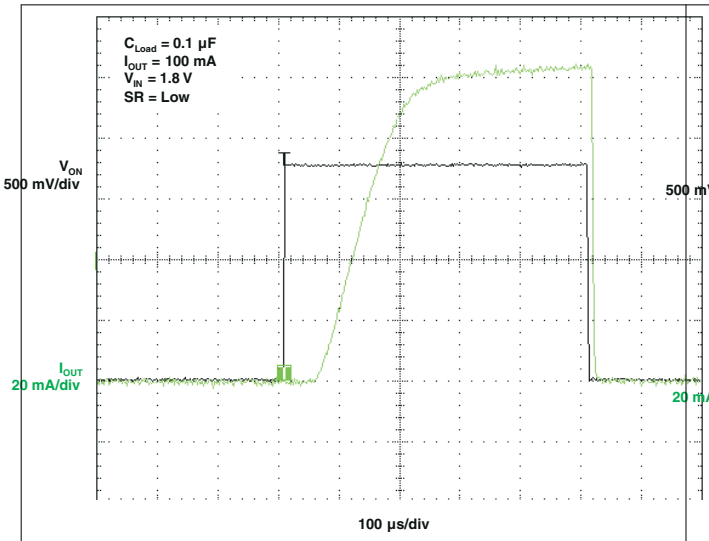


图 5-20. t_{ON} Response

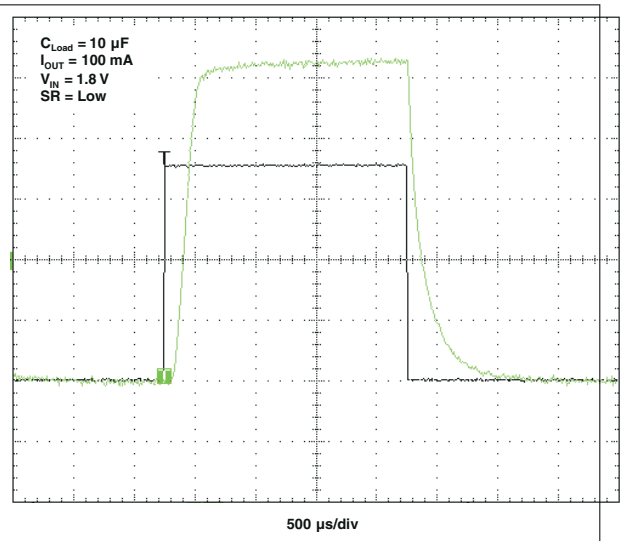


图 5-21. t_{ON} Response

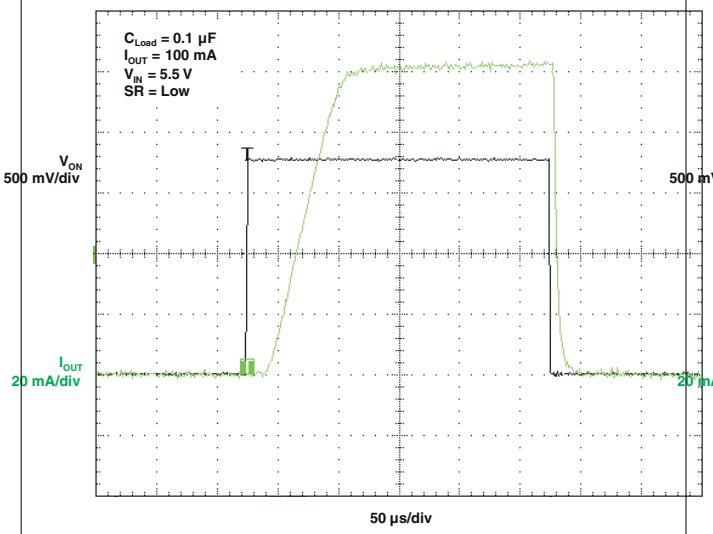


图 5-22. t_{ON} Response

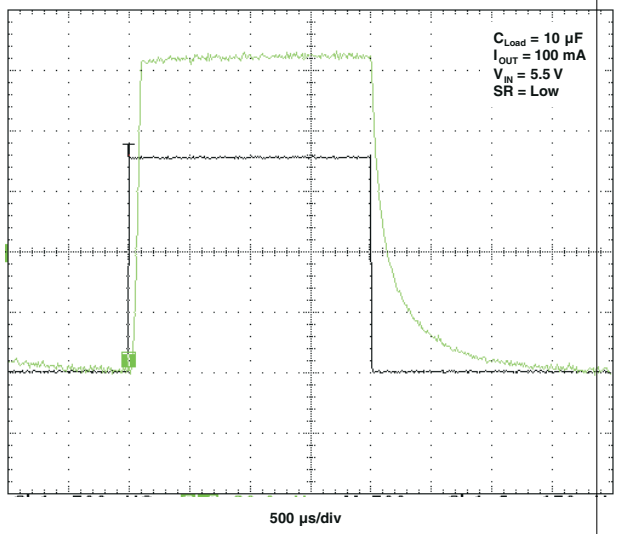


图 5-23. t_{ON} Response

5.8 Typical Switching Characteristics (continued)

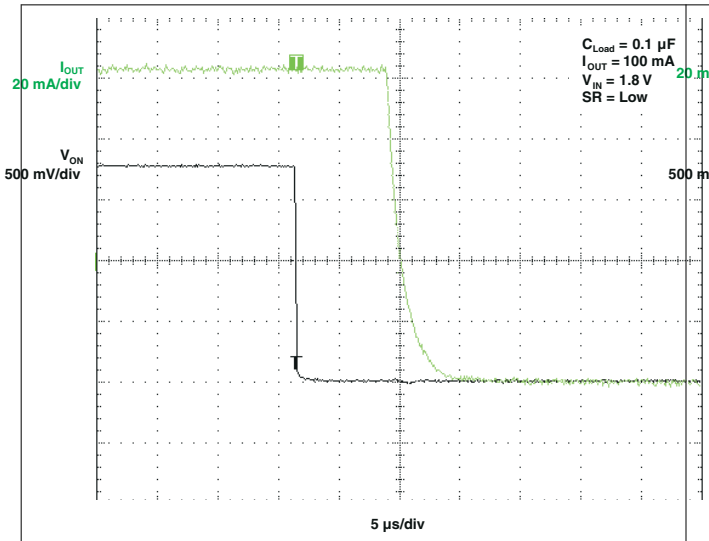


图 5-24. t_{OFF} Response

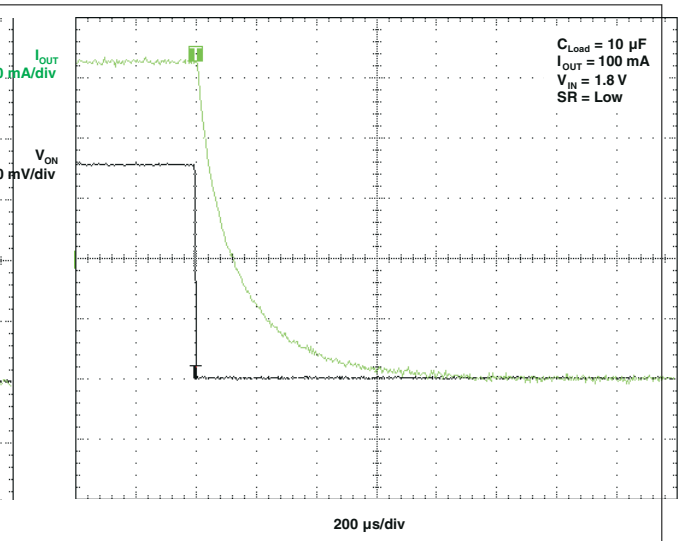


图 5-25. t_{OFF} Response

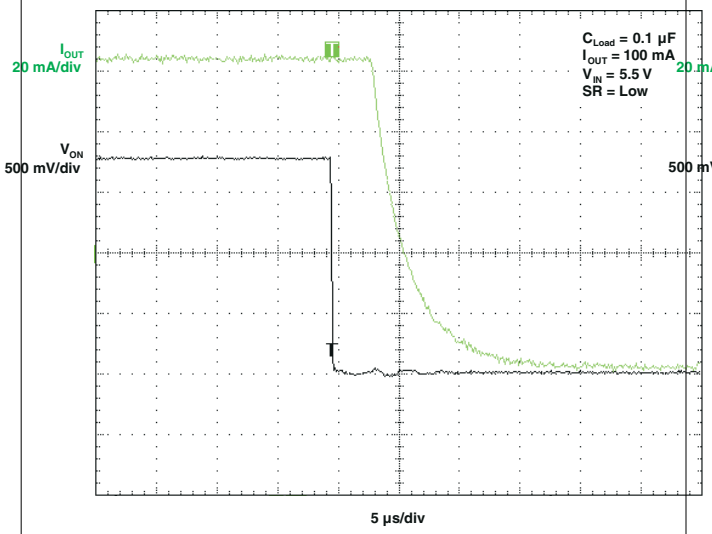


图 5-26. t_{OFF} Response

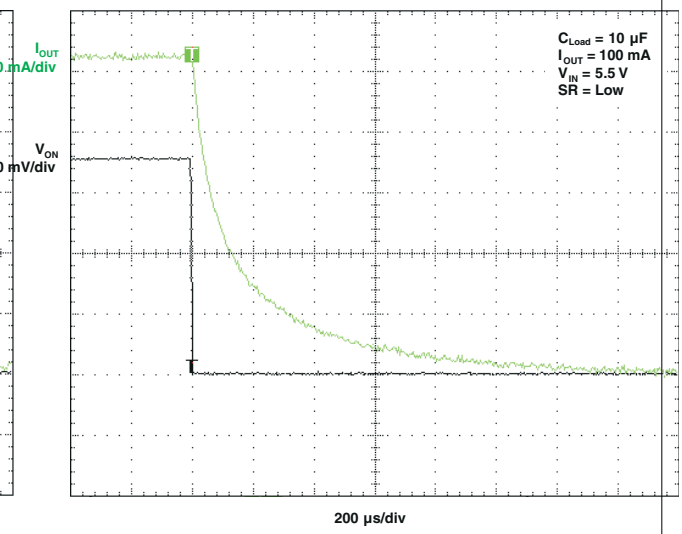
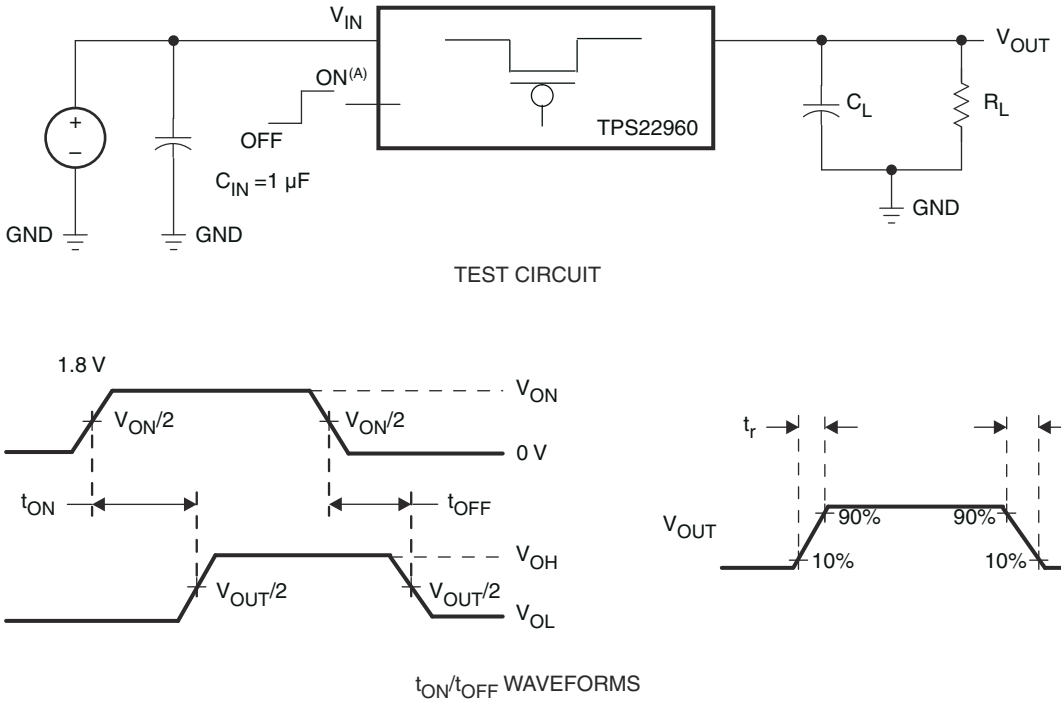


图 5-27. t_{OFF} Response

6 Parameter Measurement Information



A. t_{rise} and t_{fall} of the control signal is 100ns.

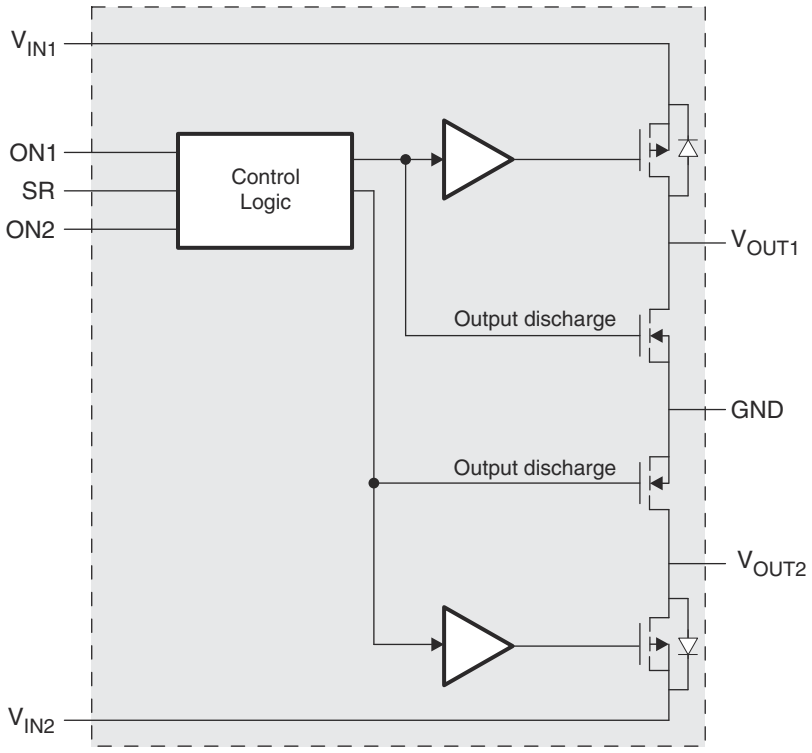
图 6-1. Test Circuit and t_{ON}/t_{OFF} Waveforms

7 Detailed Description

7.1 Overview

The TPS22960 is a dual-channel load switch. The two channels can be independently controlled using the ONx pins. Each channel has an 85-Ω quick discharge resistance from V_{OUTX} to GND when disabled. A single control pin (SR) is used to set the slew rate for both channels..

7.2 Functional Block Diagram



7.3 Feature Description

This section will discuss the features of the TPS22960 which have been summarized in 表 7-1.

表 7-1. Feature Summary

DEVICE	r_{ON} AT 3.3 V (TYP)	SLEW RATE AT 3.3 V (TYP)	QUICK OUTPUT DISCHARGE(1)	MAX OUTPUT CURRENT	ENABLE
TPS22960	435 mΩ	75 μs with SR = low 660 μs with SR = high	Yes	500 mA	Active High

(1) This feature discharges the output of the switch to ground through an 85-Ω resistor, preventing the output from floating.

7.3.1 Output Slew Rate (SR) Control

The slew rate (rise time) of the device is internally controlled in order to avoid inrush current, and it can be slowed down if needed using the SR pin. At 3.3 V, TPS22960 features a 75-μs rise time with the SR pin tied to ground, and a 660-μs rise time with the SR pin tied high. Both channels will have the same slew rate set by the SR pin.

7.3.2 Quick Output Discharge (QOD)

Each channel of the TPS22960 includes an independent QOD feature. When the channel is disabled, a discharge resistor is connected between VOUTx and GND. This resistor has a typical value of 85 Ω and prevents the output from floating while the switch is disabled.

7.4 Device Functional Modes

表 7-2. Configurable Logic Function Table

ONx	V_{INx} TO V_{OUTx}	V_{OUTx} TO GND
L	OFF	ON
H	ON	OFF

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

8.1.1 ON/OFF Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state, as long as there is no fault. ON is active HI and has a low threshold, making it capable of interfacing with low voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, or 3.3-V GPIOs.

8.1.2 Input Capacitor

To limit voltage drop or voltage transients, sufficient capacitance needs to be placed on the input side of the load switch (from V_{IN} to GND). In most cases, a 1-µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. However, when switching heavy capacitive loads, higher values of C_{IN} may be needed to prevent the system supply voltage from dropping.

8.1.3 Output Capacitor

The integral body diode in the PMOS switch will allow reverse current flow if V_{OUT} exceeds V_{IN}. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} if the system supply is removed. In the case where the system supply could be removed and reverse current is a concern, a C_{IN} greater than C_L is recommended.

8.2 Typical Application

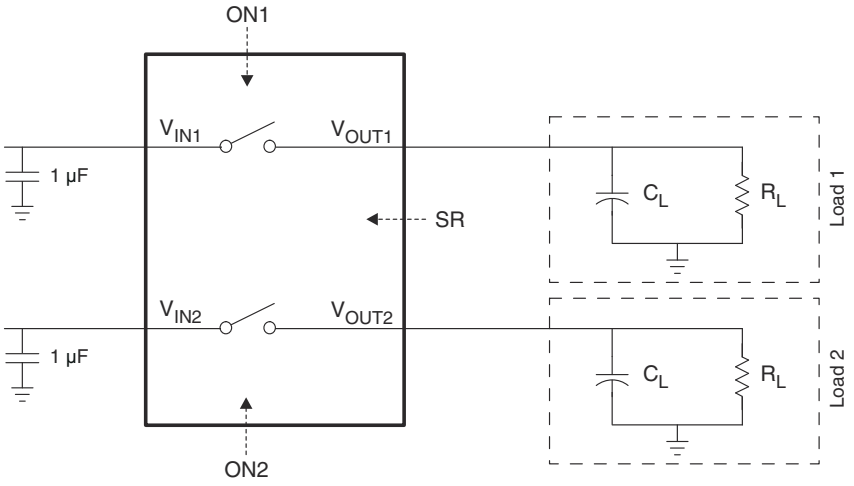


图 8-1. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use input parameters in 表 8-1.

表 8-1. Design Parameters

PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
C_L	22 µF
Maximum acceptable inrush current	200 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (in this example, 3.3 V). This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

$$\text{Inrush Current} = C \times dV / dt \quad (1)$$

Where:

C = output capacitance

dV = output voltage

dt = rise time

The TPS22960 offers selectable rise time control for V_{OUT}. This feature allows the user to control the inrush current during turnon. 方程式 1 can be used to find the required rise time to limit the inrush current to the design requirements

$$200\ \text{mA} = 22\ \mu\text{F} \times (3.3\ \text{V} \times 80\%) / dt \quad (2)$$

dt = 290 µs (4)

To ensure an inrush current of less than 200 mA, SR must be set high for a rise time greater than 290 µs. The following application curves show the different inrush for each SR setting in this design example.

8.2.3 Application Curves

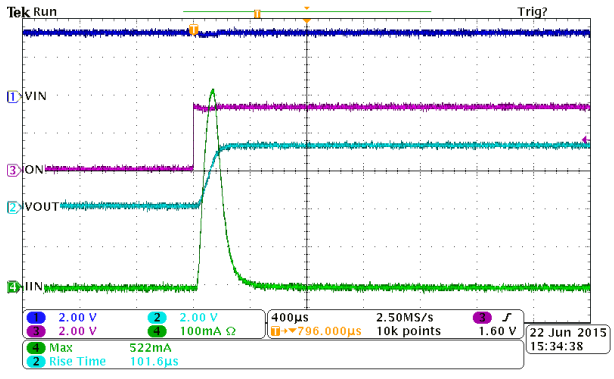


图 8-2. Inrush Current with SR = Low

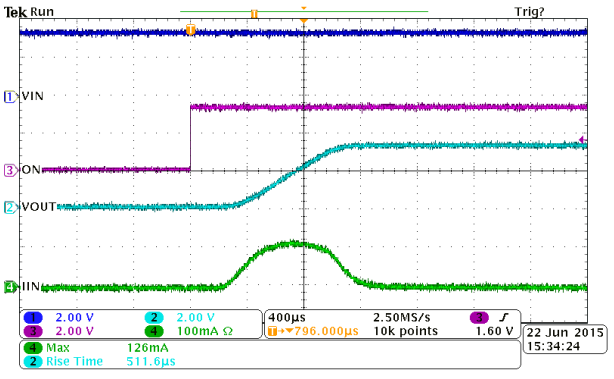


图 8-3. Inrush Current with SR = High

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage range of 1.62 V to 5.5 V. The power supply should be well-regulated and placed as close to the device terminals as possible. It must be able to withstand all transient

and load current steps. In most situations, using an input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input

The requirements for larger input capacitance can be mitigated by selecting the slower slew rate +SR=high. This will cause the load switch to turn on more slowly and limit the inrush current.

8.4 Layout

8.4.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for VI_N, V_{OUT}, and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

8.4.2 Layout Example

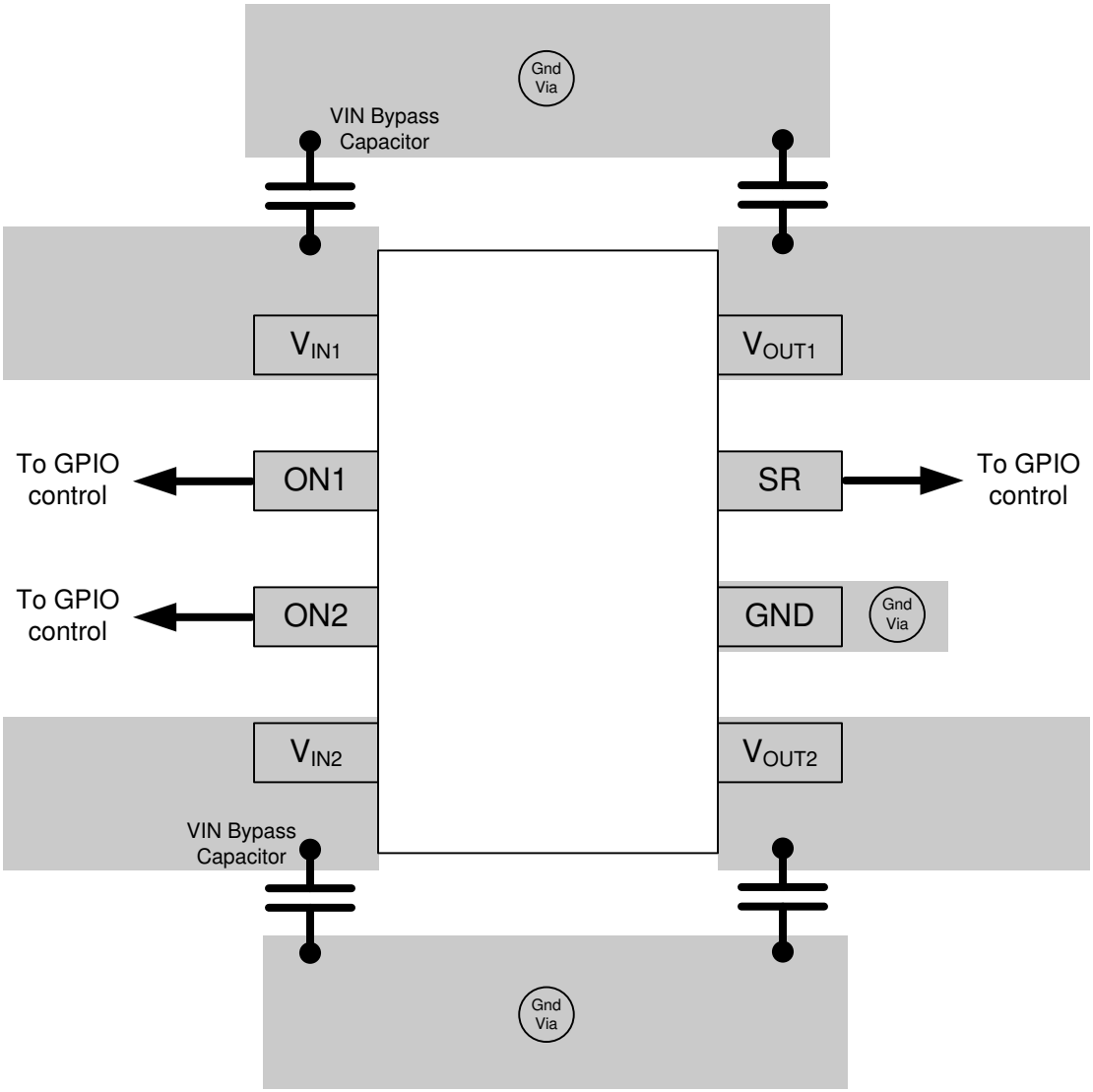


图 8-4. DCN Package Layout

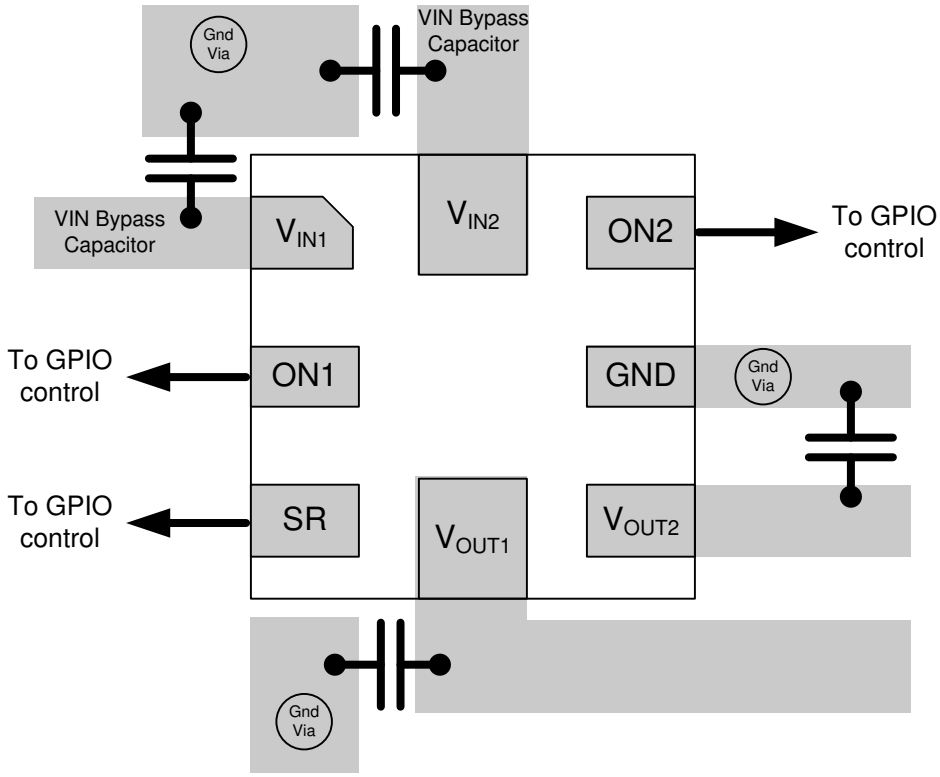


图 8-5. RSE Package Layout

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.3 Trademarks

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (February 2016) to Revision E (April 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Changed maximum $I_{IN(OFF)}$ at VIN=1.8V from 0.9μA : to 1.2μA in the *Electrical Characteristics* section	4

Changes from Revision C (July 2015) to Revision D (February 2016)	Page
• 更改了 *节 8.1*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22960DCNR	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFRO, NFRR)
TPS22960DCNR.A	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFRO, NFRR)
TPS22960DCNR.B	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFRO, NFRR)
TPS22960DCNRG4	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFRR
TPS22960DCNRG4.A	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFRR
TPS22960DCNRG4.B	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFRR
TPS22960RSER	Active	Production	UQFN (RSE) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	72
TPS22960RSER.A	Active	Production	UQFN (RSE) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	72
TPS22960RSER.B	Active	Production	UQFN (RSE) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	72
TPS22960RSET	Active	Production	UQFN (RSE) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	72
TPS22960RSET.A	Active	Production	UQFN (RSE) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	72
TPS22960RSET.B	Active	Production	UQFN (RSE) | 8	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	72

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

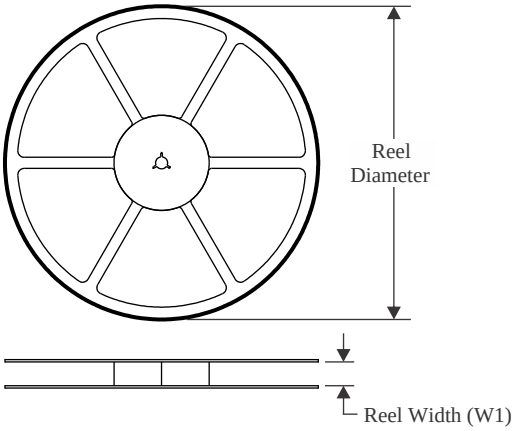
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

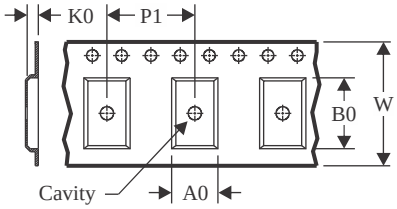
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

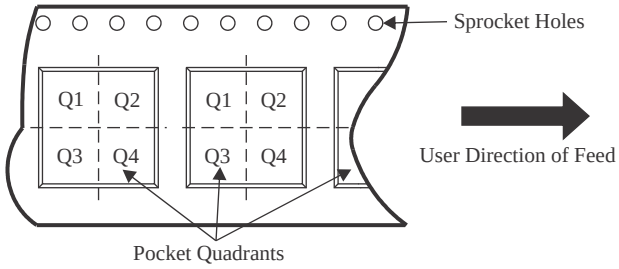


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

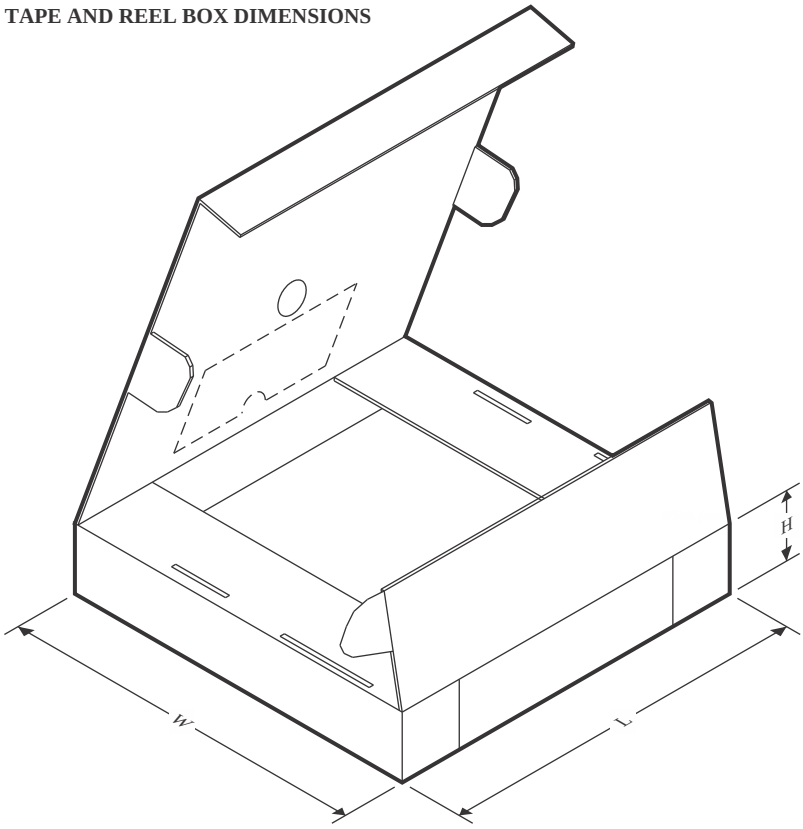
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22960DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS22960DCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22960DCNRG4	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS22960RSER	UQFN	RSE	8	3000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
TPS22960RSET	UQFN	RSE	8	250	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

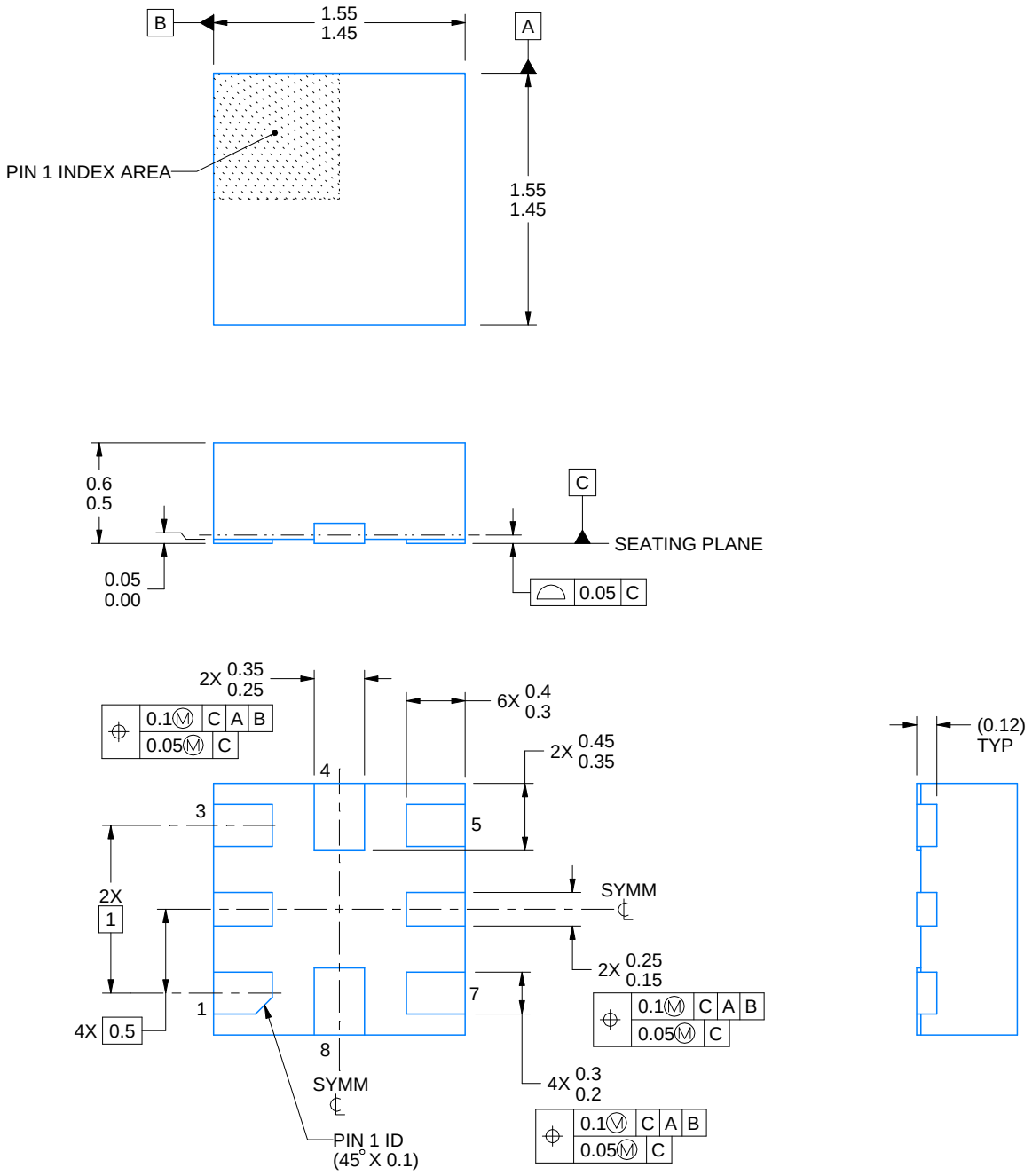
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22960DCNR	SOT-23	DCN	8	3000	183.0	183.0	20.0
TPS22960DCNR	SOT-23	DCN	8	3000	203.0	203.0	35.0
TPS22960DCNRG4	SOT-23	DCN	8	3000	183.0	183.0	20.0
TPS22960RSER	UQFN	RSE	8	3000	183.0	183.0	20.0
TPS22960RSET	UQFN	RSE	8	250	183.0	183.0	20.0

RSE0008A

PACKAGE OUTLINE

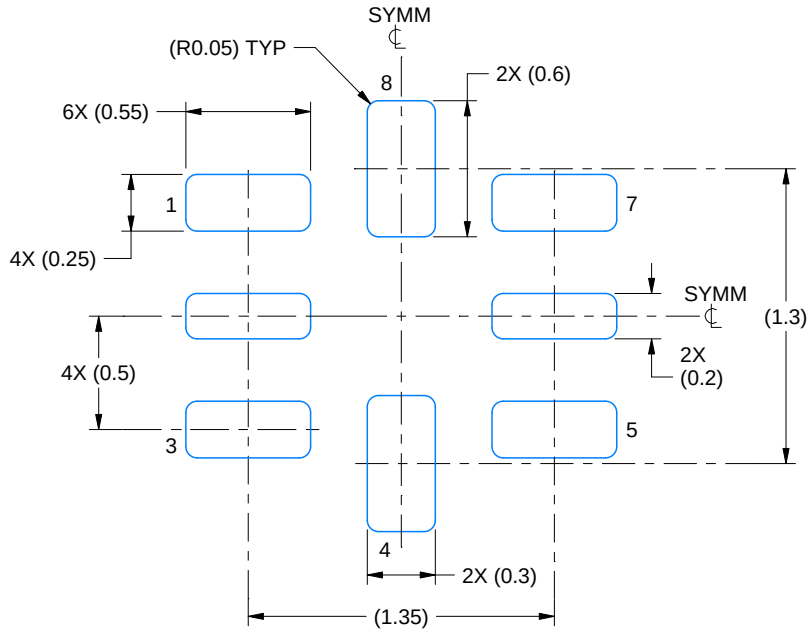
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

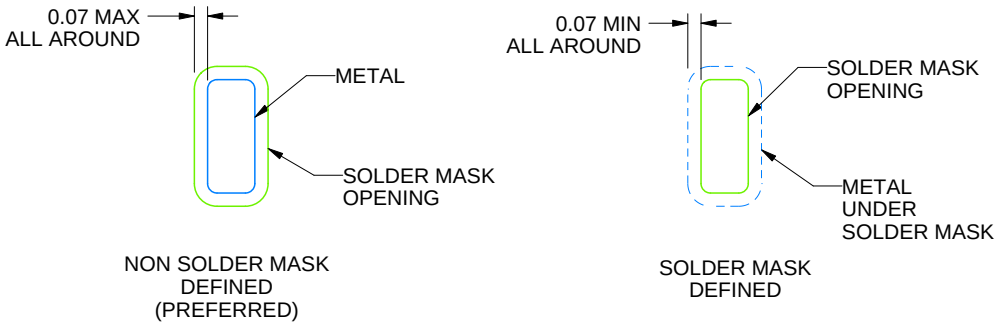


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

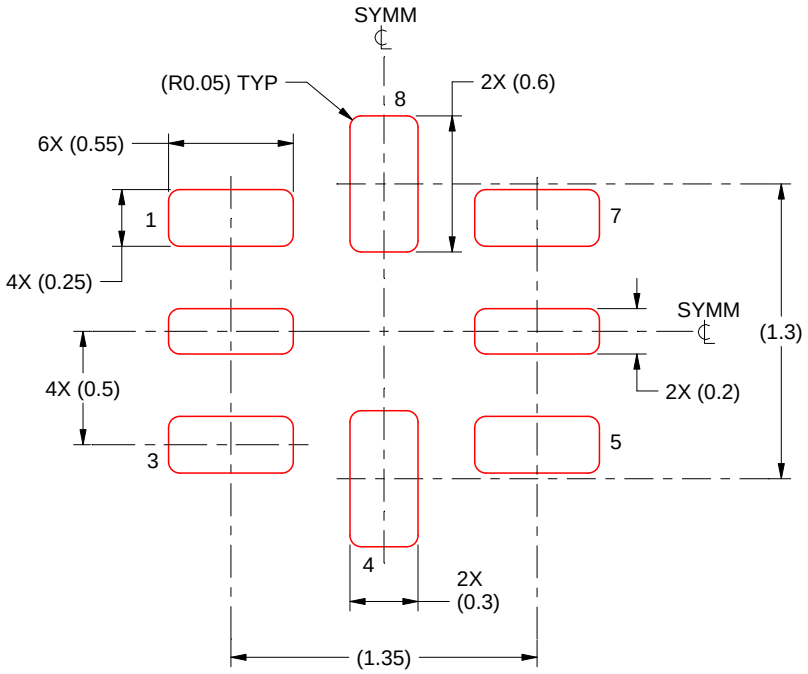


SOLDER MASK DETAILS
NOT TO SCALE

4220323/B 03/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



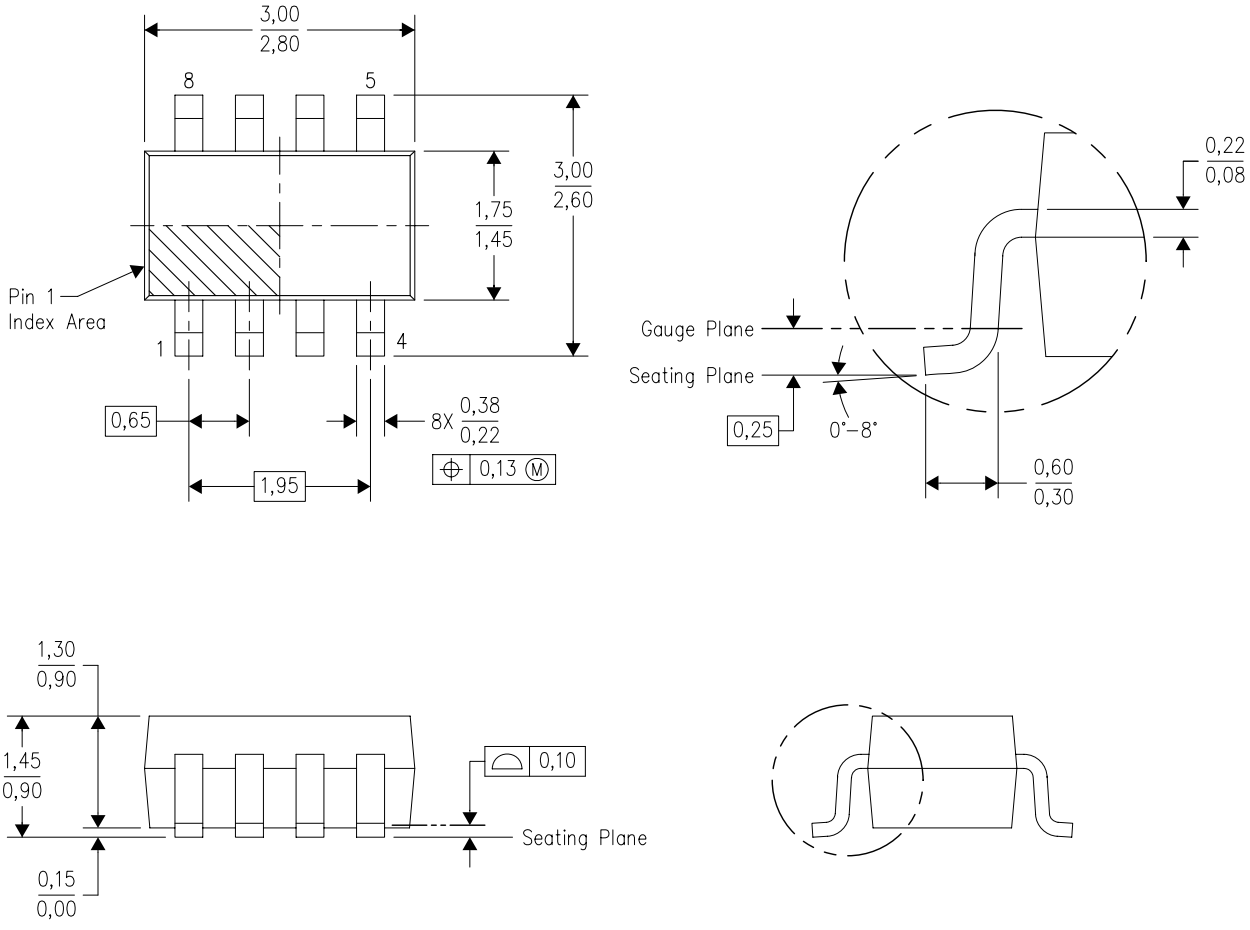
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220323/B 03/2018

NOTES: (continued)

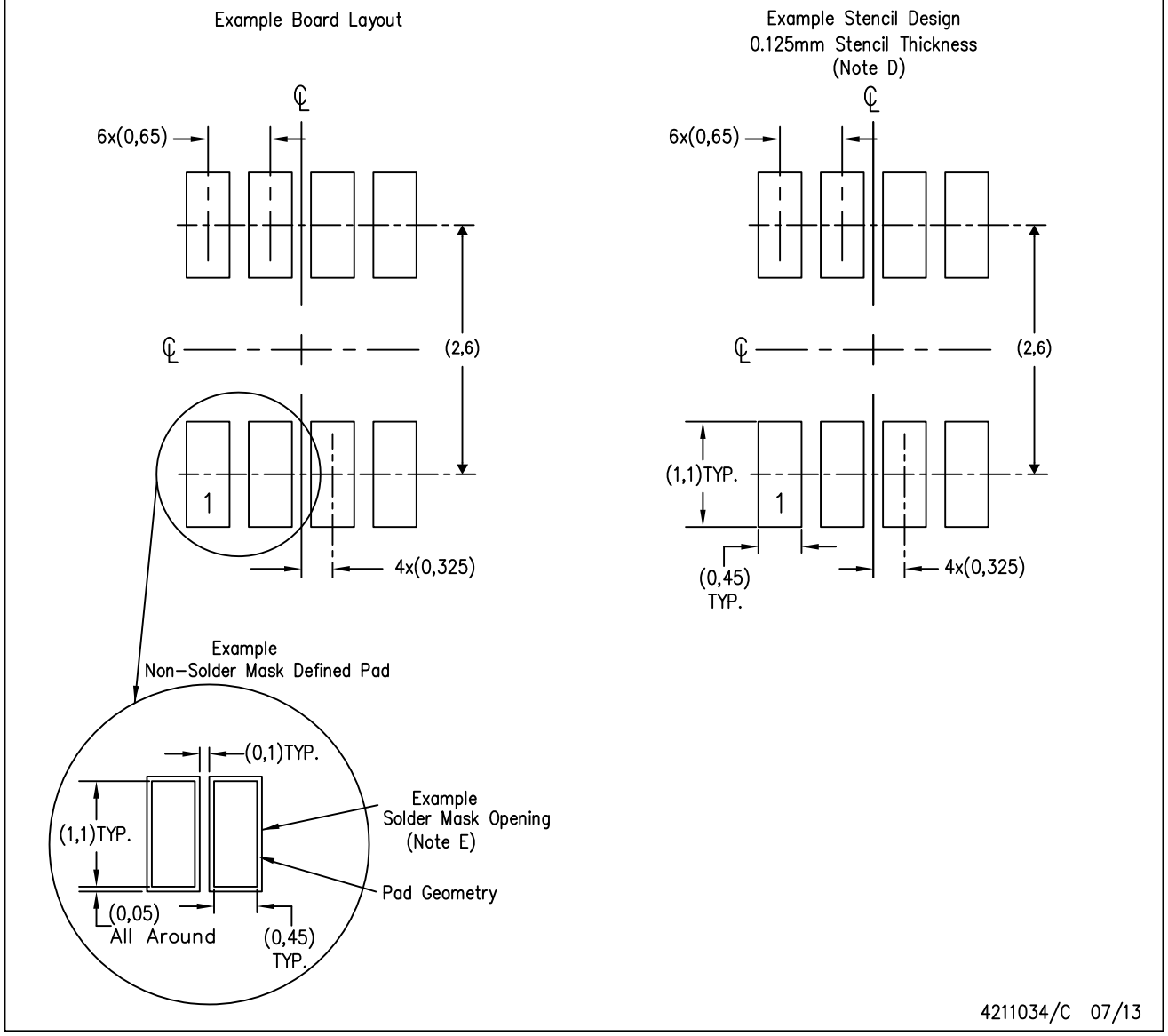
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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最后更新日期：2025 年 10 月