# TPS383x Nano Power Voltage Supervisor With Selectable Reset Delay

## 1 Features

- Supply current: 220 nA (typical)
- Precision supply voltage supervision range: 1.8 V, 2.5 V, 3.0 V, and 3.3 V
- Power-on reset generator with selectable delay time: 10 ms or 200 ms
- Push and pull $\overline{\text{RESET}}$ output (TPS3836), Push and pull RESET output (TPS3837), or open-drain $\overline{\text{RESET}}$ output (TPS3838)
- Manual reset
- 5-pin SOT23 and 2-mm × 2-mm, 6-pin SON packages
- Temperature range: –40°C to 85°C

## 2 Applications

- Applications using low-power DSPs, microcontrollers, or microprocessors
- Portable- and battery-powered equipment
- Intelligent instruments
- Wireless communication systems
- Notebook computers
- Applications using the MSP430™
- For automotive systems, see TPS383x-Q1

## 3 Description

The TPS3836, TPS3837, and TPS3838 device families of supervisory circuits provide circuit initialization and timing supervision, primarily for digital signal processors (DSP) and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage $V_{DD}$ becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors $V_{DD}$ and keeps the $\overline{\text{RESET}}$ output active as long as $V_{DD}$ remains below the threshold voltage of $V_{IT}$. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time starts after $V_{DD}$ rises above the threshold voltage $V_{IT}$.

When CT is connected to GND, a fixed delay time of typically 10 ms is asserted. When connected to $V_{DD}$, the delay time is typically 200 ms. When the supply voltage drops below the threshold voltage $V_{IT}$, the output becomes active (low) again. All the devices of this family have a fixed-sense threshold voltage ($V_{IT}$) set by an internal voltage divider.

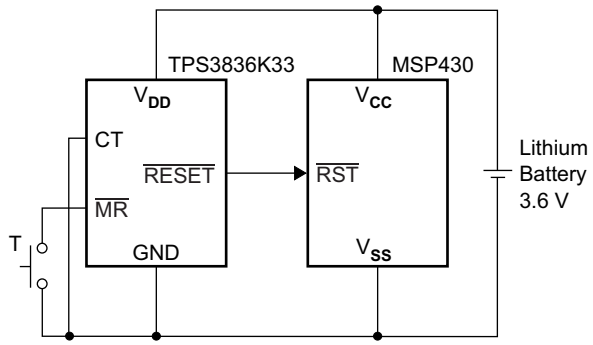
The TPS3836 has an active-low, push-pull $\overline{\text{RESET}}$ output. The TPS3837 has an active-high, push-pull RESET, and the TPS3838 integrates an active-low, open-drain $\overline{\text{RESET}}$ output. The product spectrum is designed for supply voltages of 1.8 V, 2.5 V, 3.0 V, and 3.3 V. The circuits are available in either a SOT23-5 or a 2-mm × 2-mm SON-6 package. The TPS3836, TPS3837, and TPS3838 families are characterized for operation over a temperature range of –40°C to 85°C.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS383x | WSON (6) | 2.00 mm × 2.00 mm |
| | SOT (5) | 2.90 mm × 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Application Circuit**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

**Changes from Revision E (October 2010) to Revision F** **Page**

- Changed format to meet latest data sheet standards; changed data sheet title, added *Device Information* table, *Pin Configurations and Functions*, *Parameter Measurement Information*, *Detailed Description*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Receiving Notification of Documentation Updates*, and *Support Resources* sections. Moved existing sections into the new format ... 1
- Changed 2x2 WSON to 2-mm × 2-mm WSON in fifth Features bullet ... 1
- Changed link to automotive data sheet ... 1
- Added full acronym name for DSP to first sentence of *Description* section ... 1
- Changed 2x2 WSON to 2-mm × 2-mm WSON in last paragraph of *Description* section ... 1
- Changed *Ordering Information* table to *Device Comparison Table* ... 3
- Deleted soldering temperature parameter from *Absolute Maximum Ratings* table ... 4
- Moved storage temperature range to *Absolute Maximum Ratings* table ... 4
- Changed *Handling Ratings* table to *ESD Ratings* ... 4
- Added *Thermal Information* table ... 5
- Moved propagation (delay) time maximum values to the TYP column ... 6
- Changed propagation times for the high-to-low-level output and low-to-high-level output from: 0.1 µs to: 0.3 µs ... 6


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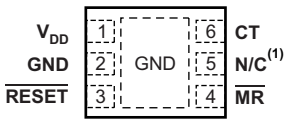
## 5 Device Comparison Table(1)

| PRODUCT | NOMINAL SUPPLY VOLTAGE | THRESHOLD VOLTAGE ($V_{IT}$)(1) |
|---|---|---|
| TPS383xE18 | 1.8 V | 1.71 V |
| TPS383xJ25 | 2.5 V | 2.25 V |
| TPS383xH30 | 3.0 V | 2.79 V |
| TPS383xL30 | 3.0 V | 2.64 V |
| TPS383xK33 | 3.3 V | 2.93 V |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(1) Custom threshold voltages are available. Minimum order quantities apply. Contact factory for details and availability.

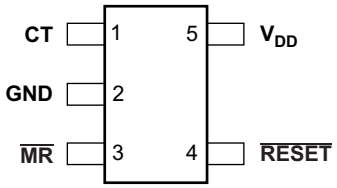
## 6 Pin Configuration and Functions

**TPS3838 DRV Package**
**6-Pin WSON**
**(Top View)**

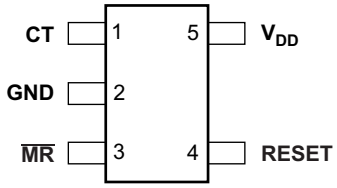



(1) N/C: Not Connected

**TPS3836 and TPS3838 DBV Package**
**5-Pin SOT**
**(Top View)**




**TPS3837 DBV Package**
**5-Pin SOT**
**(Top View)**




**Pin Functions**

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| | WSON | SOT (TPS3836, TPS3838) | SOT (TPS3837) | | |
| CT | 6 | 1 | 1 | — | Capacitor Time Delay Pin. Connect this pin to GND to set reset delay time to 10 ms. Connect this pin to $V_{DD}$ to set reset delay time to 200 ms. |
| GND | 2 | 2 | 2 | — | Ground |
| $\overline{MR}$ | 4 | 3 | 3 | I | Manual Reset. When $\overline{MR}$ activates to logic low, $\overline{RESET}$/RESET activates. When $\overline{MR}$ is inactive, $\overline{RESET}$/RESET depends only on the voltage at $V_{DD}$. If $\overline{MR}$ is unused, connect to $V_{DD}$ to minimize current consumption. |
| N/C | 5 | — | — | — | No Connect |
| $\overline{RESET}$ | 3 | 4 | — | O | Active-Low Output Reset. When $V_{DD}$ falls below $V_{IT}$ or when $\overline{MR}$ activates to logic low, the $\overline{RESET}$ pin activates to logic low. When $V_{DD}$ rises above $V_{IT}$ plus $V_{HYS}$ and $\overline{MR}$ deactivates to logic high, $\overline{RESET}$ deactivates to logic high after reset delay time $t_D$. |
| RESET | — | — | 4 | O | Active-High Output Reset. When $V_{DD}$ falls below $V_{IT}$ or when $\overline{MR}$ activates to logic low, the RESET pin activates to logic high. When $V_{DD}$ rises above $V_{IT}$ plus $V_{HYS}$ and $\overline{MR}$ deactivates to logic high, RESET deactivates to logic low after reset delay time $t_D$. |

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**Pin Functions (continued)**

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| | WSON | SOT (TPS3836, TPS3838) | SOT (TPS3837) | | |
| $V_{DD}$ | 1 | 5 | 5 | I | Input Supply Voltage. This device monitors the voltage at the $V_{DD}$ pin. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ (2) | | 7 | V |
| | All other pins(2) (3) | –0.3 | 7 | V |
| Maximum low output current, $I_{OL}$ | | | 5 | mA |
| Maximum high output current, $I_{OH}$ | | | –5 | mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{DD}$) | | | ±10 | mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{DD}$) | | | ±10 | mA |
| Continuous total power dissipation | | See the Thermal Information table | | |
| Operating temperature, $T_A$ | | –40 | 85 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) If RESET or $\overline{\text{RESET}}$ are pulled above $V_{DD}$, the internal ESD structure presents an effective 1.5-kΩ resistor between these pins, causing leakage current to flow into the RESET or $\overline{\text{RESET}}$ pin.

## 7.2 Dissipation Ratings

| PACKAGE | $T_A$ < +25°C POWER RATING | DERATING FACTOR ABOVE $T_A$ = +25°C | $T_A$ = +70°C POWER RATING | $T_A$ = +85°C POWER RATING |
|---|---|---|---|---|
| DBV | 437 mW | 3.5 mW/°C | 280 mW | 227 mW |
| DRV Low-K(1) | 715 mW | 7.1 mW/°C | 395 mW | 285 mW |
| DRV High-K(2) | 1540 mW | 15.4 mW/°C | 845 mW | 615 mW |

(1) The JEDEC low-K (1s) board used to derive this data was a 3in x 3in, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in x 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on the top and bottom of the board.

## 7.3 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | 4000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.4 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | | 1.6 | 6 | V |
| Voltage | CT, $\overline{\text{MR}}$, RESET, and $\overline{\text{RESET}}$ pins | 0 | $V_{DD}$ + 0.3 | V |
| High-level input voltage, $V_{IH}$ | | 0.7 × $V_{DD}$ | | V |


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## Recommended Operating Conditions (continued)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Low-level input voltage, $V_{IL}$ | | | 0.3 × $V_{DD}$ | V |
| Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$ | | | 100 | ns/V |
| Operating temperature, $T_A$ | | –40 | 85 | °C |
| Pullup resistor value | $\overline{RESET}$ pin (TPS3838 only) | $\frac{V_{Pullup}}{50\ \mu A}$ | | Ω |

## 7.5 Thermal Information

| THERMAL METRIC[1] | | TPS383x | | UNIT |
|---|---|---|---|---|
| | | DRV (WSON) | DBV (SOT) | |
| | | 6 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 84.7 | 153.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 85.2 | 108.1 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.5 | 33.5 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.9 | 10.9 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 48.2 | 33.1 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 30.0 | n/a | |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

## 7.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $\overline{RESET}$ (TPS3836) | $V_{DD}$ = 3.3 V, $I_{OH}$ = –2 mA | 0.8 × $V_{DD}$ | | | V |
| | | | $V_{DD}$ = 6 V, $I_{OH}$ = –3 mA | | | | |
| | | RESET (TPS3837) | $V_{DD}$ = 1.8 V, $I_{OH}$ = –1 mA | | | | |
| | | | $V_{DD}$ = 3.3 V, $I_{OL}$ = –2 mA | | | | |
| $V_{OL}$ | Low-level output voltage | $\overline{RESET}$ (TPS3836, TPS3838) | $V_{DD}$ = 1.8 V, $I_{OL}$ = 1 mA | | | 0.4 | V |
| | | | $V_{DD}$ = 3.3 V, $I_{OL}$ = 2 mA | | | | |
| | | RESET (TPS3837) | $V_{DD}$ = 3.3 V, $I_{OL}$ = 2 mA | | | | |
| | | | $V_{DD}$ = 6 V, $I_{OL}$ = 3 mA | | | | |
| | Power-up reset voltage[1] | TPS3836, TPS3838 | $V_{DD}$ ≥ 1.1 V, $I_{OL}$ = 50 µA | | | 0.2 | V |
| | | TPS3837 | $V_{DD}$ ≥ 1.1 V, $I_{OL}$ = –50 µA | 0.8 × $V_{DD}$ | | | V |
| $V_{IT}$ | Negative-going input threshold voltage[2] | TPS383xE18 | $T_A$ = –40°C to 85°C | 1.66 | 1.71 | 1.74 | V |
| | | TPS383xJ25 | | 2.18 | 2.25 | 2.29 | |
| | | TPS383xH30 | | 2.70 | 2.79 | 2.85 | |
| | | TPS383xL30 | | 2.56 | 2.64 | 2.69 | |
| | | TPS383xK33 | | 2.84 | 2.93 | 2.99 | |
| $V_{HYS}$ | Hysteresis at $V_{DD}$ input | | 1.7 V < $V_{IT}$ < 2.5 V | | 30 | | mV |
| | | | 2.5 V < $V_{IT}$ < 3.5 V | | 40 | | |
| | | | 3.5 V < $V_{IT}$ < 5 V | | 50 | | |
| $I_{IH}$ | High-level input current | $\overline{MR}$ [3] | $\overline{MR}$ = 0.7 × $V_{DD}$, $V_{DD}$ = 6 V | –40 | –60 | –100 | µA |
| | | CT | CT = $V_{DD}$ = 6 V | –25 | | 25 | nA |

(1) The lowest voltage at which the $\overline{RESET}$ output becomes active. $t_R$, $V_{DD}$ ≥ 15 µs/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminal.
(3) If manual reset is unused, $\overline{MR}$ should be connected to $V_{DD}$ to minimize current consumption.

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## Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{IL}$ | Low-level input current | $\overline{MR}$ (3) | $\overline{MR}$ = 0 V, $V_{DD}$ = 6 V | –130 | –200 | –340 | µA |
| | | CT | CT = 0 V, $V_{DD}$ = 6 V | –25 | | 25 | nA |
| $I_{OH}$ | High-level output current | TPS3838 | $V_{DD} = V_{IT} + 0.2$ V, $V_{OH} = V_{DD}$ | | | 25 | nA |
| $I_{DD}$ | Supply current | | $V_{DD} > V_{IT}$, $V_{DD} < 3$ V | | 220 | 400 | nA |
| | | | $V_{DD} > V_{IT}$, $V_{DD} > 3$ V | | 250 | 450 | |
| | | | $V_{DD} < V_{IT}$ | | 10 | 15 | µA |
| | Internal pullup resistor at $\overline{MR}$ | | | | 30 | | kΩ |
| $C_I$ | Input capacitance at $\overline{MR}$ and CT | | $V_I$ = 0 V to $V_{DD}$ | | 5 | | pF |

## 7.7 Timing Requirements

At $T_A$ = 25°C, $R_L$ = 1 MΩ, and $C_L$ = 50 pF, unless otherwise noted.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_W$ | Pulse duration | At $V_{DD}$ | $V_{IH} = V_{IT} + 0.2$ V, $V_{IL} = V_{IT} – 0.2$ V | | 6 | | µs |
| | | At $\overline{MR}$ | $V_{DD} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$ | | 1 | | |

## 7.8 Switching Characteristics

At $T_A$ = 25°C, $R_L$ = 1 MΩ, and $C_L$ = 50 pF, unless otherwise noted.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_D$ | Delay time | | $V_{DD} \geq V_{IT} + 0.2$ V, $\overline{MR} = 0.7 \times V_{DD}$, CT = GND, (see *Timing Diagram*) | 5 | 10 | 15 | ms |
| | | | $V_{DD} \geq V_{IT} + 0.2$ V, $\overline{MR} = 0.7 \times V_{DD}$, CT = $V_{DD}$, (see *Timing Diagram*) | 100 | 200 | 300 | |
| $t_{PHL}$ | Propagation (delay) time, high-to-low-level output | $V_{DD}$ to $\overline{RESET}$ delay (TPS3836, TPS3838) | $V_{IL} = V_{IT} – 0.2$ V, $V_{IH} = V_{IT} + 0.2$ V | | 10 | | µs |
| | | | $V_{IL}$ = 1.6 V | | 50 | | |
| $t_{PLH}$ | Propagation (delay) time, low-to-high-level output | $V_{DD}$ to RESET delay (TPS3837) | $V_{IL} = V_{IT} – 0.2$ V, $V_{IH} = V_{IT} + 0.2$ V | | 10 | | µs |
| | | | $V_{IL}$ = 1.6 V | | 50 | | |
| $t_{PHL}$ | Propagation (delay) time, high-to-low-level output | $\overline{MR}$ to $\overline{RESET}$ delay (TPS3836, TPS3838) | $V_{DD} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IL} = 0.7 \times V_{DD}$ | | 0.3 | | µs |
| $t_{PLH}$ | Propagation (delay) time, low-to-high-level output | $\overline{MR}$ to RESET delay (TPS3837) | $V_{DD} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IL} = 0.7 \times V_{DD}$ | | 0.3 | | µs |


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## 7.9 Typical Characteristics

Test conditions are $T_J$ = 25°C unless otherwise noted.

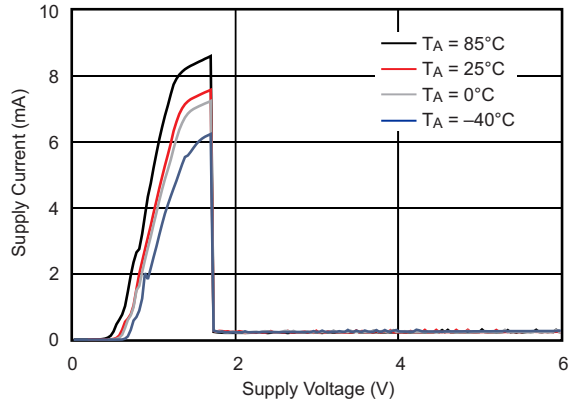



**Figure 1. Supply Current vs Supply Voltage**

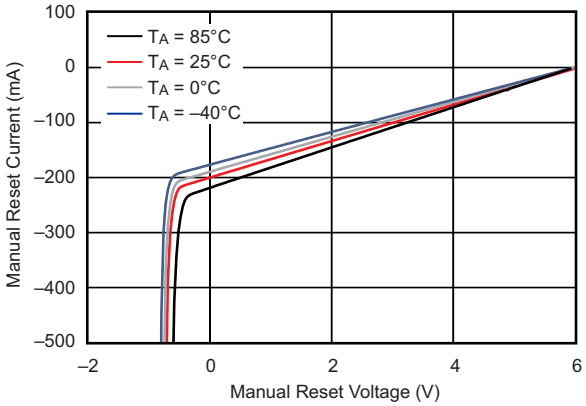



**Figure 2. Manual Reset Current vs Manual Reset Voltage**

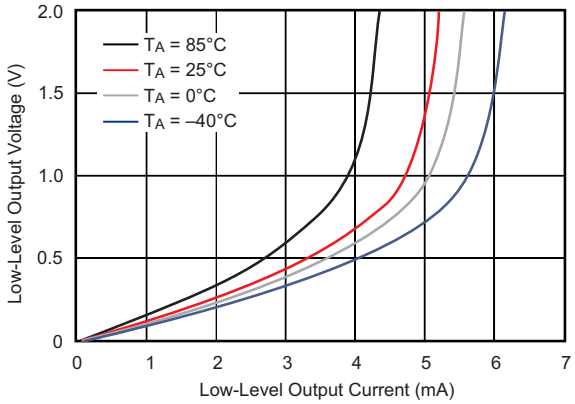



**Figure 3. Low-Level Output Voltage vs Low-Level Output Current**

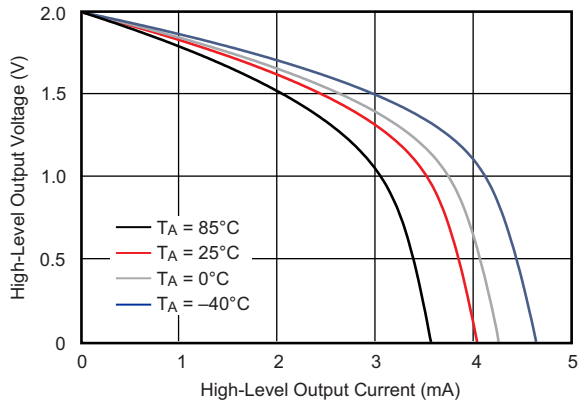



**Figure 4. High-Level Output Voltage vs High-Level Output Current**

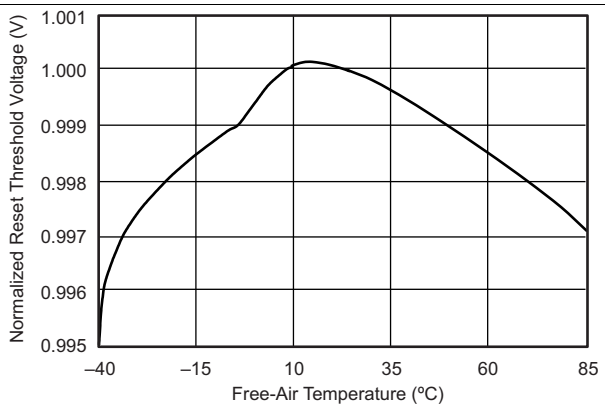



**Figure 5. Normalized Reset Threshold Voltage vs Free-Air Temperature**

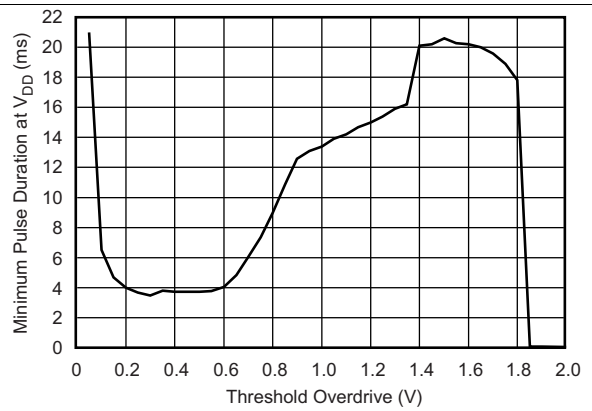



**Figure 6. Minimum Pulse Duration at $V_{DD}$ vs $V_{DD}$ Threshold Overdrive**

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# 8 Parameter Measurement Information

## 8.1 Timing Diagram

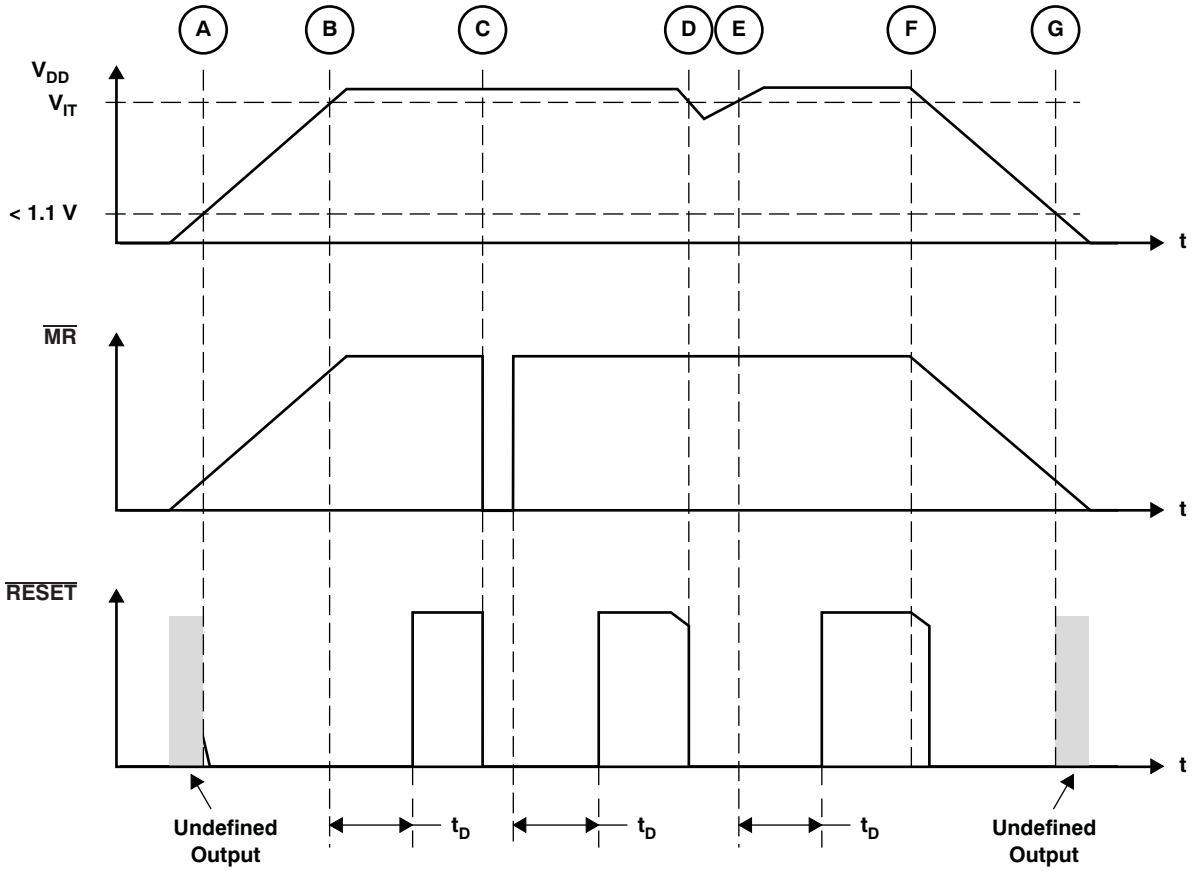



**Figure 7. Timing Diagram**

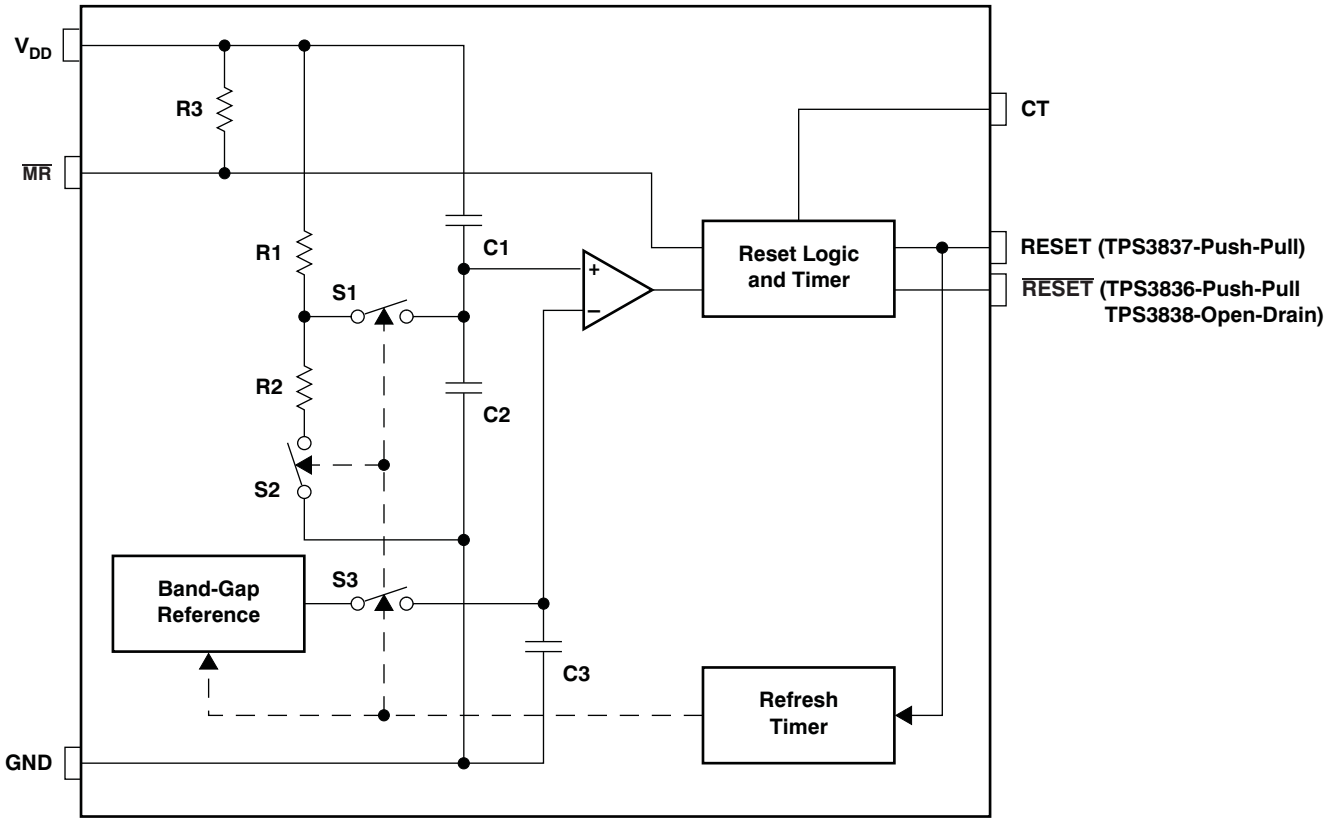

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# 9 Detailed Description

## 9.1 Overview

The TPS3836, TPS3837, and TPS3838 devices are a family of nano power voltage supervisors with manual reset and selectable reset delay.

## 9.2 Functional Block Diagram




## 9.3 Feature Description

### 9.3.1 Input Voltage ($V_{DD}$)

The $V_{DD}$ pin monitors the input voltage with an internal comparator and when the voltage at $V_{DD}$ falls below $V_{IT}$, the reset output is asserted to active state after the propagation delay time: $t_{PHL}$ for TPS3836 and TPS3838, $t_{PLH}$ for TPS3837. When $V_{DD}$ rises above $V_{IT}$ plus $V_{HYS}$ and $\overline{MR}$ is logic high, the reset output deasserts to an inactive state after the reset delay time, $t_D$. Note that the $V_{DD}$ and $\overline{MR}$ pins have different propagation delays with the same label.

### 9.3.2 Manual Reset ($\overline{MR}$)

Manual reset is an active-low logic input that when $\overline{MR}$ is logic low, the reset output asserts to the active state after the propagation delay: $t_{PHL}$ for TPS3836 and TPS3838, $T_{PLH}$ for TPS3837. Once $\overline{MR}$ is logic high and $V_{DD}$ is above $V_{IT}$, the reset output deasserts to an inactive state after the reset delay time, $t_D$. As previously noted, the $V_{DD}$ and $\overline{MR}$ pins have different propagation delays with the same label.

### 9.3.3 Selectable Reset Delay (CT)

The reset delay, $t_D$, can be configured to 10 ms by connecting CT to GND or 200 ms by connecting CT to $V_{DD}$.

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## Feature Description (continued)

### 9.3.4 Reset Output ($\overline{\text{RESET}}$ / RESET)

TPS3836 is a push-pull, active-low $\overline{\text{RESET}}$ output. The $\overline{\text{RESET}}$ output is logic high when inactive and logic low when active. This device does not require a pullup resistor.

TPS3837 is a push-pull, active-high RESET output. The RESET output is logic low when inactive and logic high when active. This device does not require a pullup resistor.

TPS3838 is an open-drain, active-low $\overline{\text{RESET}}$ output. The $\overline{\text{RESET}}$ output is logic high when inactive and logic low when active. This device does require a pullup resistor. Refer to *Recommended Operating Conditions* to determine the recommended value of the pullup resistor.

**NOTE**

The reset output is active when $V_{DD}$ is below $V_{IT}$ or $\overline{\text{MR}}$ is logic low. The reset output is inactive when $V_{DD}$ is above $V_{IT}$ plus $V_{HYS}$ and $\overline{\text{MR}}$ is logic high.

## 9.4 Device Functional Modes

Table 1 summarized the various functional modes of the device. Logic high is represented at "H" and logic low is represented by "L". True is represented as "1" and false is represented as "0".

**Table 1. Function Table**

| $\overline{\text{MR}}$ | $V_{DD} > V_{IT}$ | $\overline{\text{RESET}}$ (1) | RESET (2) |
|---|---|---|---|
| L | 0 | L | H |
| L | 1 | L | H |
| H | 0 | L | H |
| H | 1 | H | L |

(1) TPS3836 and TPS3838.
(2) TPS3837 only.


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# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The following section describes a typical application for this device. This is to serve as an example only as different applications have different requirements.

## 10.2 Typical Application

In this application, TPS3836K33 monitors a 3.6-V Lithium-ion battery and sends a reset signal to a MCU when the battery reaches undervoltage.

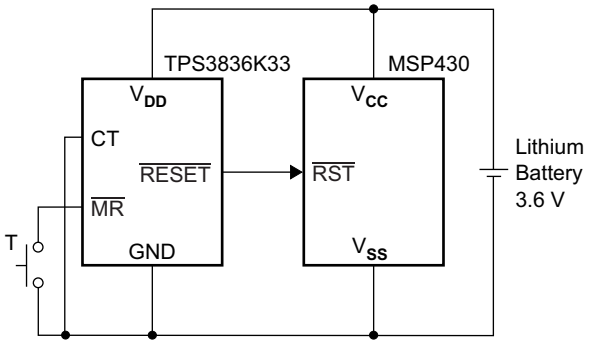



**Figure 8. Typical Application Circuit**

### 10.2.1 Design Requirements

This application monitors the 3.6-V battery and triggers a undervoltage fault to the MCU when the battery voltage falls below 3 V. The application does not release the undervoltage fault until the battery voltage is above approximately 3 V for longer than 200 ms typical. The application must not consume more than 1 µA.

### 10.2.2 Detailed Design Procedure

The TPS3836K33 is the correct device variant to choose since the undervoltage threshold for this variant is 2.93 V typical. This meets the undervoltage fault requirement of the application. To achieve releasing the undervoltage fault condition after the battery is above 3 V for 200 ms, connect CT to $V_{DD}$ to select the 200-ms reset delay option. Choosing TPS3836 push-pull variant save a pullup resistor since no pullup resistor is required for the push-pull variant. These family of devices have 450-nA maximum Iq, which meets the current consumption requirement.

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## Typical Application (continued)

### 10.2.3 Application Curves

This section shows the voltage monitoring functionality. Figure 9 shows when $V_{DD}$ drops below 2.93 V, the $\overline{\text{RESET}}$ output asserts to active low. Figure 10 shows that when the $V_{DD}$ rises above 2.93 V + 40 mV = approximately 2.97 V for 200 ms, the $\overline{\text{RESET}}$ output deasserts to inactive logic high.

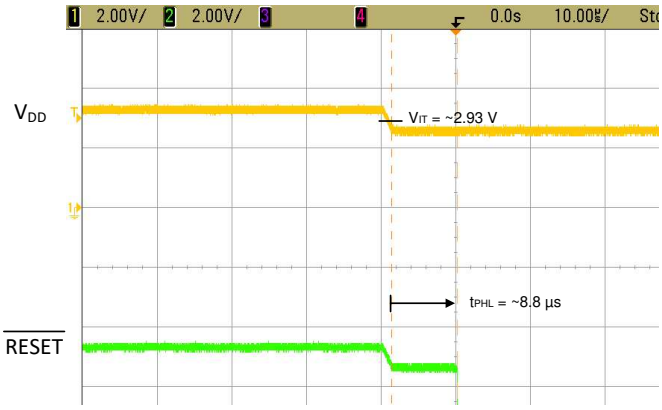



**Figure 9. $V_{DD}$ Falling Below $V_{IT}$ Triggers a $\overline{\text{RESET}}$ Assertion After $t_{PHL}$**

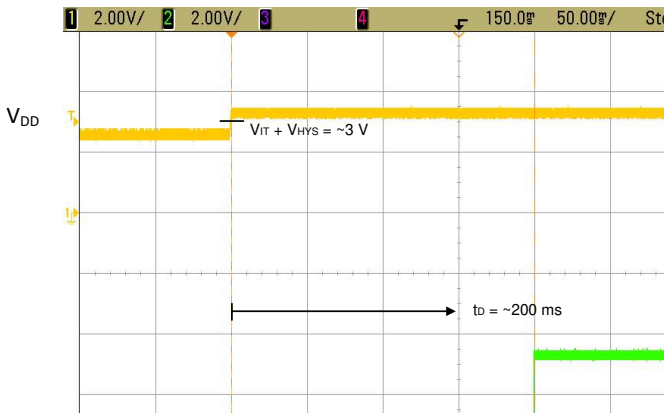



**Figure 10. $V_{DD}$ Rising Above $V_{IT}$ + $V_{HYS}$ for $t_D$ Releases $\overline{\text{RESET}}$ to Inactive**


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# 11 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.6 V and 6 V. TI recommends an input supply capacitor between the $V_{DD}$ pin and GND pin. This device has a 7-V absolute maximum rating on the $V_{DD}$ pin. Take extra precautions if the voltage supply providing power to $V_{DD}$ is susceptible to any large voltage transient that can exceed 7 V.

# 12 Layout

## 12.1 Layout Guidelines

Make sure that the connection to the $V_{DD}$ pin is low impedance. Good analog design practice recommends placing a minimum 0.1-µF ceramic capacitor as near as possible to the $V_{DD}$ pin to GND. If using the TPS3838 variant, be sure to follow the *Recommended Operating Conditions* to determine the pullup resistor value. Larger transients and faster slew rates on $V_{DD}$ should use larger input capacitors. If not using $\overline{MR}$, tie to $V_{DD}$ to reduce current consumption.

## 12.2 Layout Example

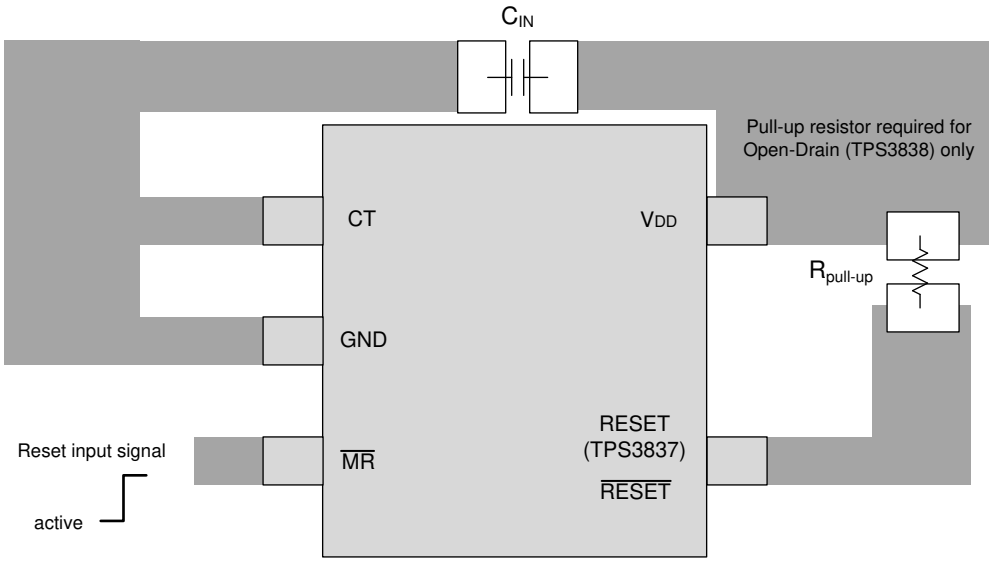



**Figure 11. TPS3836, TPS3837, and TPS3838 Typical Layout**

# 13 Device and Documentation Support

## 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPS3836 | Click here | Click here | Click here | Click here | Click here |
| TPS3837 | Click here | Click here | Click here | Click here | Click here |
| TPS3838 | Click here | Click here | Click here | Click here | Click here |

## 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 13.4 Trademarks

MSP430, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS3836E18DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDNI |
| TPS3836E18DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDNI |
| TPS3836E18DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDNI |
| TPS3836E18DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDNI |
| TPS3836H30DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHRI |
| TPS3836H30DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHRI |
| TPS3836H30DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHRI |
| TPS3836H30DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PHRI |
| TPS3836J25DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDSI |
| TPS3836J25DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDSI |
| TPS3836J25DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDSI |
| TPS3836J25DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDSI |
| TPS3836K33DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDTI |
| TPS3836K33DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDTI |
| TPS3836K33DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDTI |
| TPS3836K33DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDTI |
| TPS3836L30DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCAI |
| TPS3836L30DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCAI |
| TPS3836L30DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCAI |
| TPS3836L30DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCAI |
| TPS3837E18DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDOI |
| TPS3837E18DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDOI |
| TPS3837J25DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDRI |
| TPS3837J25DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDRI |
| TPS3837J25DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDRI |
| TPS3837J25DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDRI |
| TPS3837K33DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDUI |
| TPS3837K33DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDUI |
| TPS3837K33DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDUI |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS3837K33DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDUI |
| TPS3837K33DBVTG4 | NRND | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | - | Call TI | Call TI | -40 to 85 | |
| TPS3837L30DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCBI |
| TPS3837L30DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCBI |
| TPS3837L30DBVT | Obsolete | Production | SOT-23 (DBV) \| 5 | - | - | Call TI | Call TI | -40 to 85 | PCBI |
| TPS3838E18DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDQI |
| TPS3838E18DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDQI |
| TPS3838E18DBVR.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDQI |
| TPS3838E18DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDQI |
| TPS3838E18DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDQI |
| TPS3838E18DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDQI |
| TPS3838E18DBVT.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDQI |
| TPS3838J25DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDPI |
| TPS3838J25DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDPI |
| TPS3838J25DBVR.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDPI |
| TPS3838J25DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDPI |
| TPS3838J25DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDPI |
| TPS3838J25DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDPI |
| TPS3838J25DBVT.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDPI |
| TPS3838K33DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDVI |
| TPS3838K33DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDVI |
| TPS3838K33DBVR.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDVI |
| TPS3838K33DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDVI |
| TPS3838K33DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDVI |
| TPS3838K33DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDVI |
| TPS3838K33DBVT.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PDVI |
| TPS3838K33DRVR | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | CCS |
| TPS3838K33DRVR.A | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | CCS |
| TPS3838K33DRVR.B | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | CCS |
| TPS3838K33DRVT | Active | Production | WSON (DRV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | CCS |
| TPS3838K33DRVT.A | Active | Production | WSON (DRV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | CCS |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS3838K33DRVT.B | Active | Production | WSON (DRV) \| 6 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | CCS |
| TPS3838L30DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCCI |
| TPS3838L30DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCCI |
| TPS3838L30DBVR.B | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCCI |
| TPS3838L30DBVT | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCCI |
| TPS3838L30DBVT.A | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCCI |
| TPS3838L30DBVT.B | Active | Production | SOT-23 (DBV) \| 5 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PCCI |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS3836, TPS3838 :**

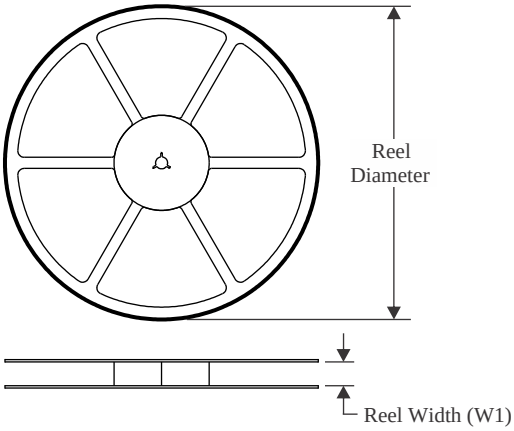
- Automotive : TPS3836-Q1, TPS3838-Q1
- Enhanced Product : TPS3836-EP

NOTE: Qualified Version Definitions:

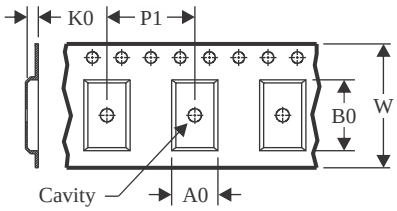
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

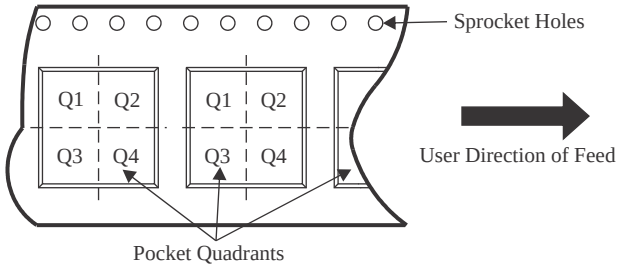



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

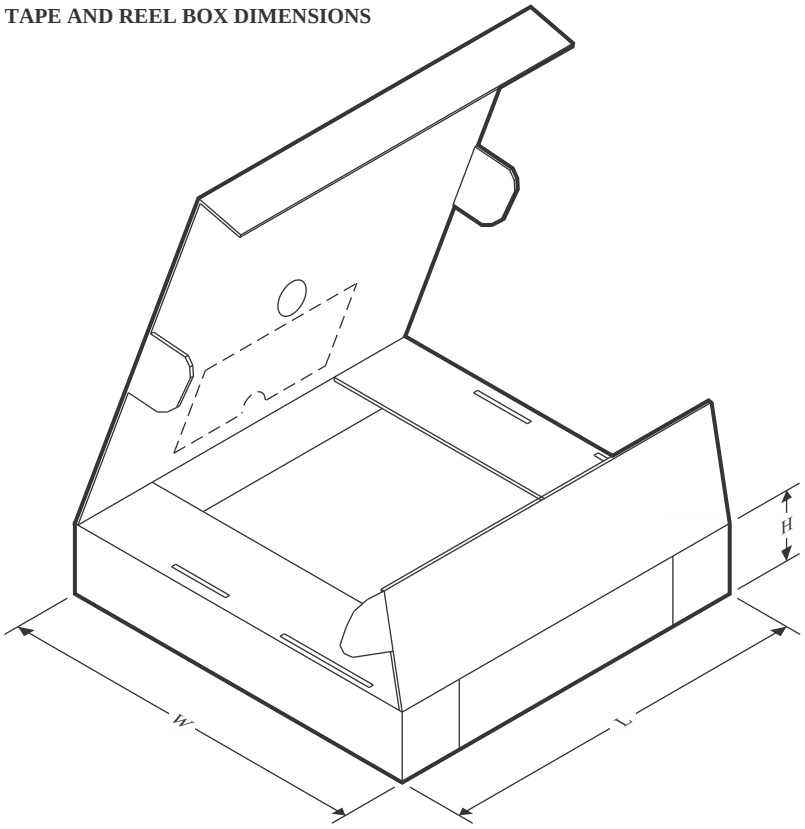



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3836E18DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3836E18DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3836H30DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3836H30DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3836J25DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3836J25DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3836K33DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3836K33DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3836L30DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3836L30DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3837E18DBVT | SOT-23 | DBV | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3837J25DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3837J25DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3837K33DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3837K33DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3837L30DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3838E18DBVR | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3838E18DBVT | SOT-23 | DBV | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3838J25DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3838J25DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3838J25DBVT | SOT-23 | DBV | 5 | 250 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3838J25DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3838K33DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3838K33DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3838K33DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TPS3838K33DRVR | WSON | DRV | 6 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS3838K33DRVT | WSON | DRV | 6 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS3838L30DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3838L30DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3838L30DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3838L30DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS3836E18DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3836E18DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS3836H30DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3836H30DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS3836J25DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3836J25DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS3836K33DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3836K33DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS3836L30DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3836L30DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS3837E18DBVT | SOT-23 | DBV | 5 | 250 | 200.0 | 183.0 | 25.0 |
| TPS3837J25DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3837J25DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS3837K33DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3837K33DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS3837L30DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3838E18DBVR | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS3838E18DBVT | SOT-23 | DBV | 5 | 250 | 200.0 | 183.0 | 25.0 |

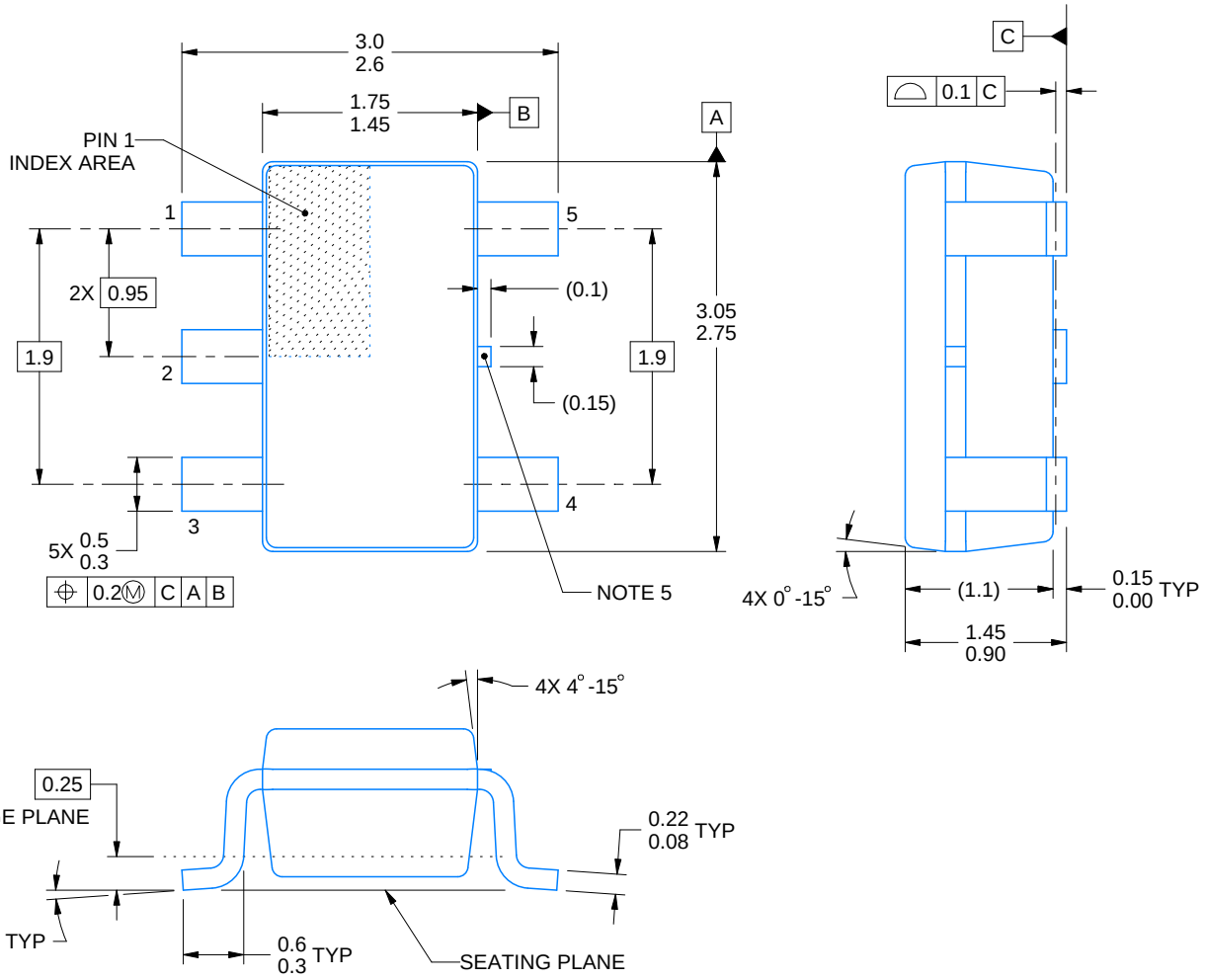
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS3838J25DBVR | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS3838J25DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3838J25DBVT | SOT-23 | DBV | 5 | 250 | 203.0 | 203.0 | 35.0 |
| TPS3838J25DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS3838K33DBVR | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS3838K33DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3838K33DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| TPS3838K33DRVR | WSON | DRV | 6 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS3838K33DRVT | WSON | DRV | 6 | 250 | 200.0 | 183.0 | 25.0 |
| TPS3838L30DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS3838L30DBVR | SOT-23 | DBV | 5 | 3000 | 200.0 | 183.0 | 25.0 |
| TPS3838L30DBVT | SOT-23 | DBV | 5 | 250 | 200.0 | 183.0 | 25.0 |
| TPS3838L30DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

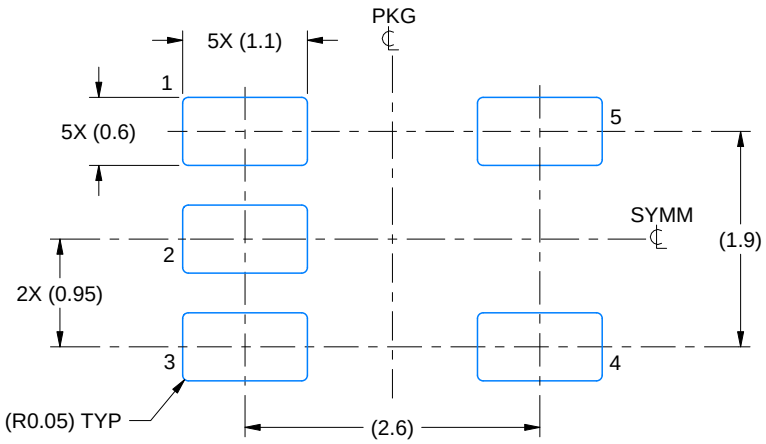
SMALL OUTLINE TRANSISTOR



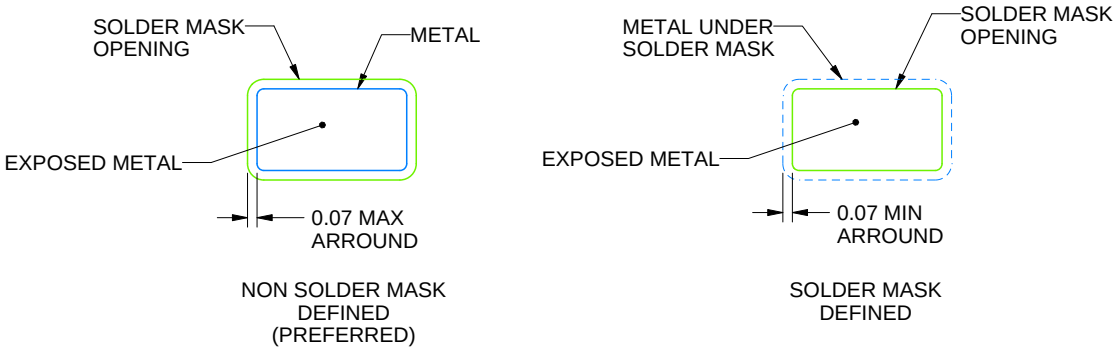

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

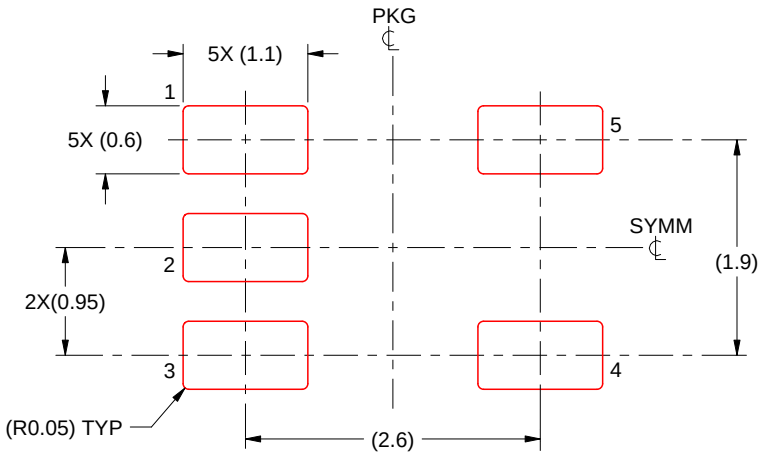



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

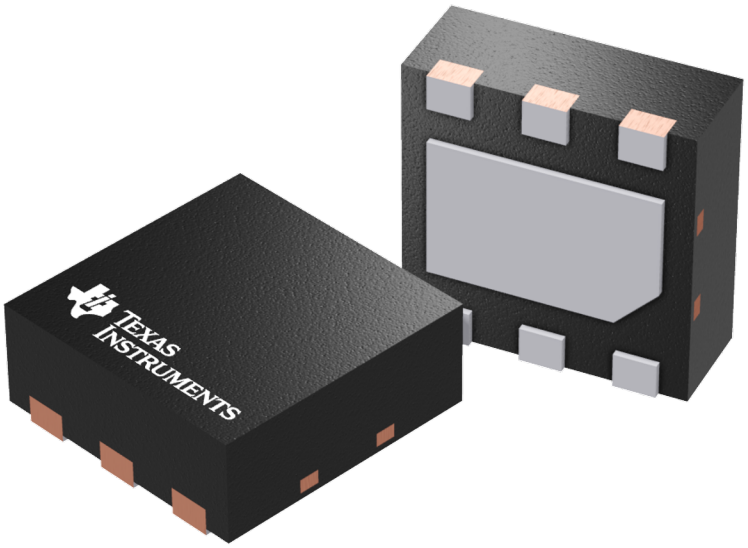
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



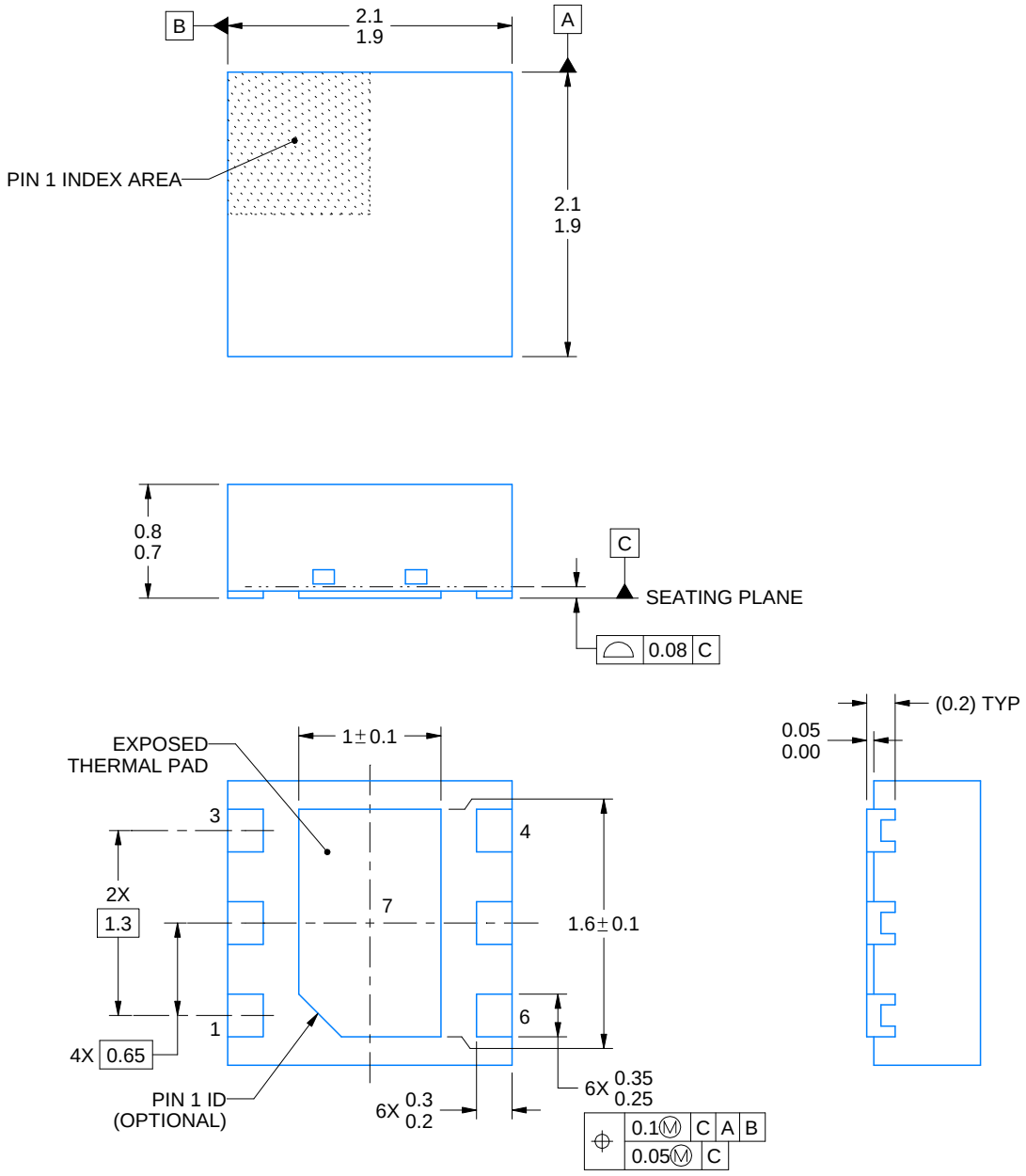

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# DRV0006D

# PACKAGE OUTLINE

## WSON - 0.8 mm max height

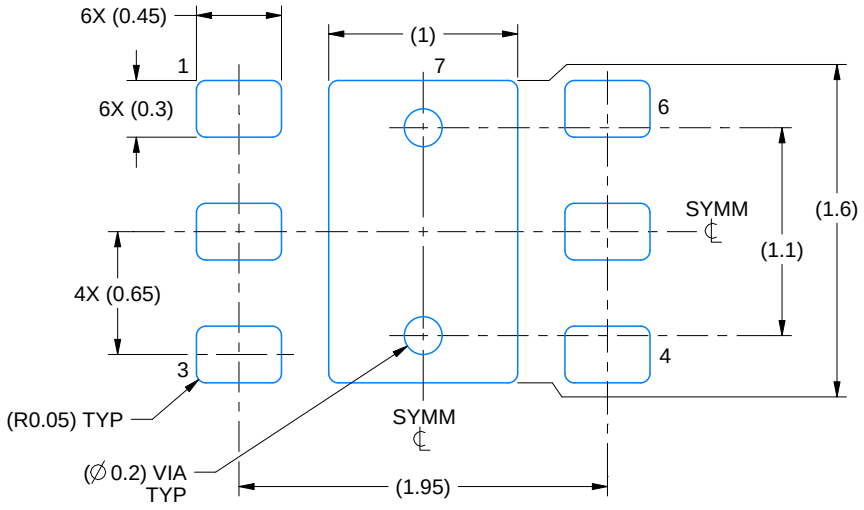
PLASTIC SMALL OUTLINE - NO LEAD



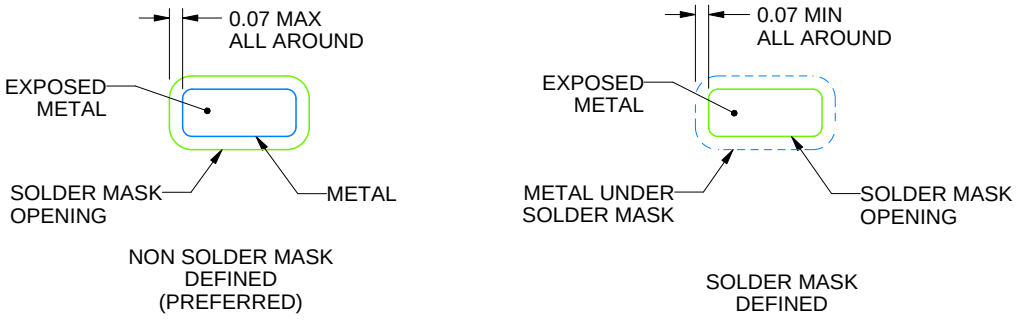

4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

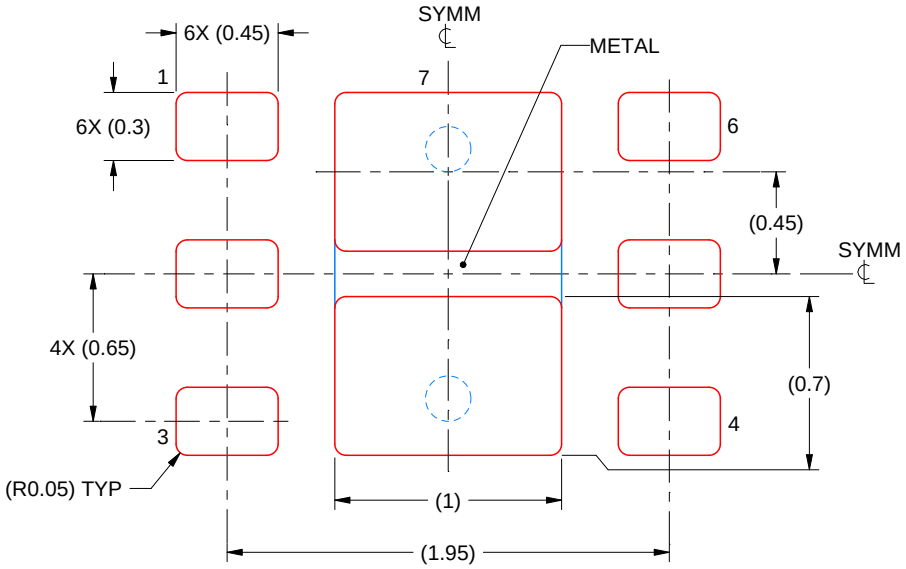



SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



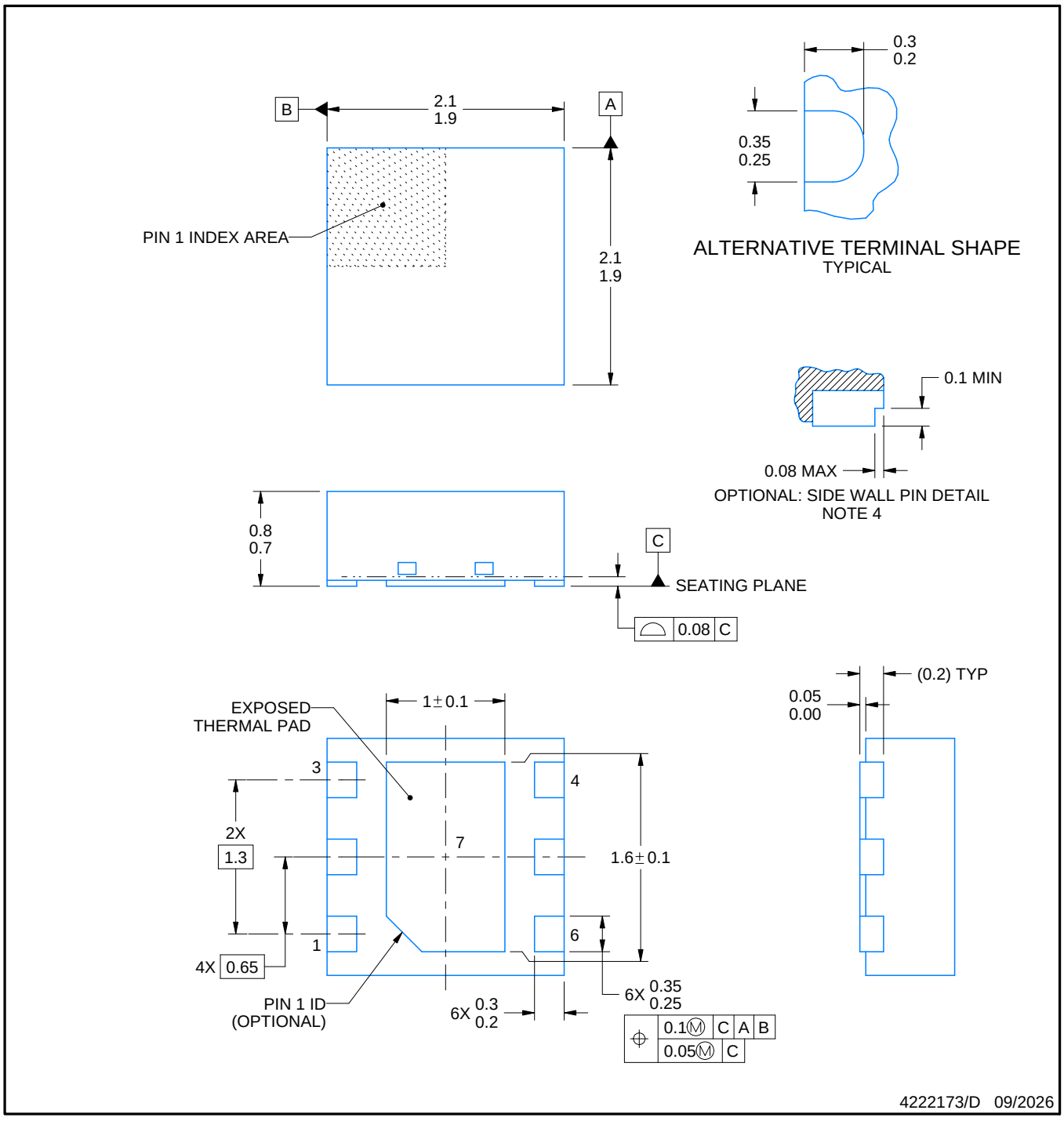

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

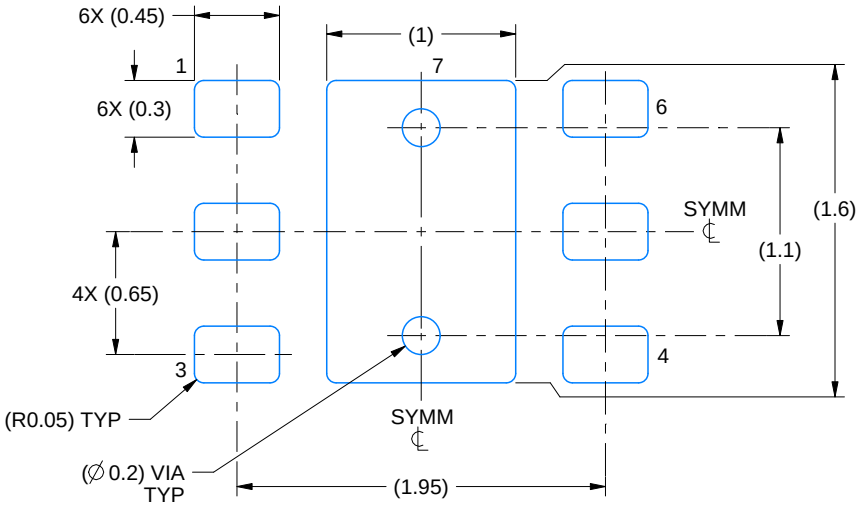
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

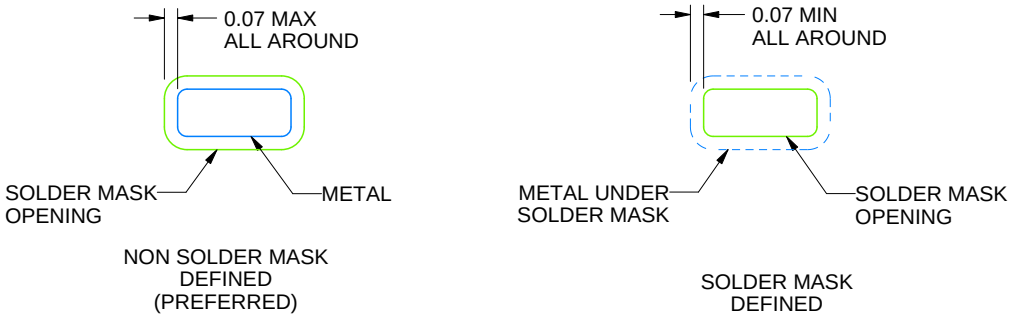



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.




LAND PATTERN EXAMPLE
SCALE:25X

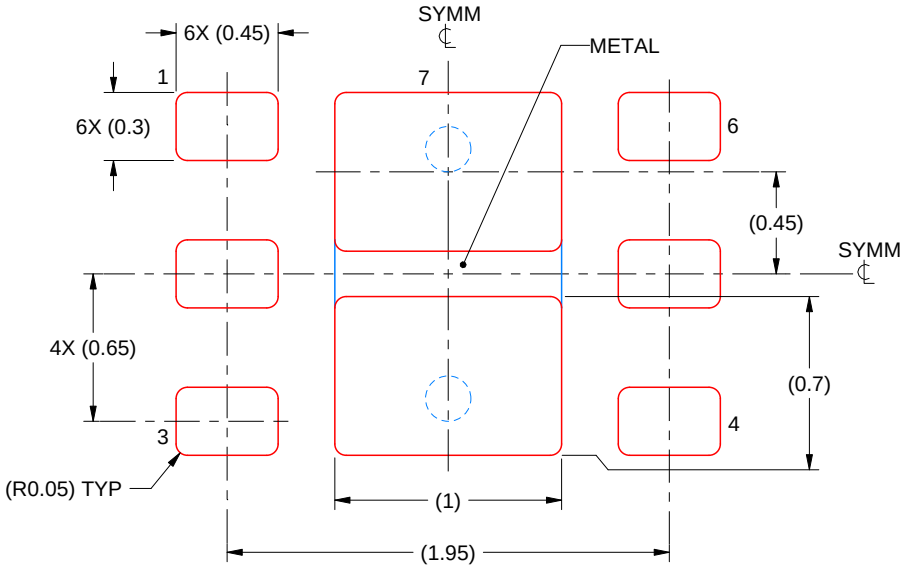



SOLDER MASK DETAILS

4222173/D 09/2026

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/D 09/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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