LOW PIN COUNT, LOW V_{IN} (3.0 V TO 5.5 V) SYNCHRONOUS BUCK DC-TO-DC CONTROLLER WITH EXTERNAL REFERENCE INPUT

FEATURES

- **3.0-V to 5.5-V Input**
- **External Reference required: 0.5 V to 1.5 V**
- **Output Voltage from REFIN to 90% of VIN**
- **High-Side Drive for N-Channel FET**
- **Supports Pre-Biased Outputs**
- **Adaptive Anti-Cross Conduction Gate Drive**
- **Fixed switching frequency (600 kHz) Voltage Mode Control**
- **Three Selectable Short Circuit Protection Levels**
- **Hiccup Restart from Faults**
- **Active Low Enable**
- **Thermal Shutdown Protection at 145°C**
- **10-Pin, 3-mm x 3-mm SON (DRC)**

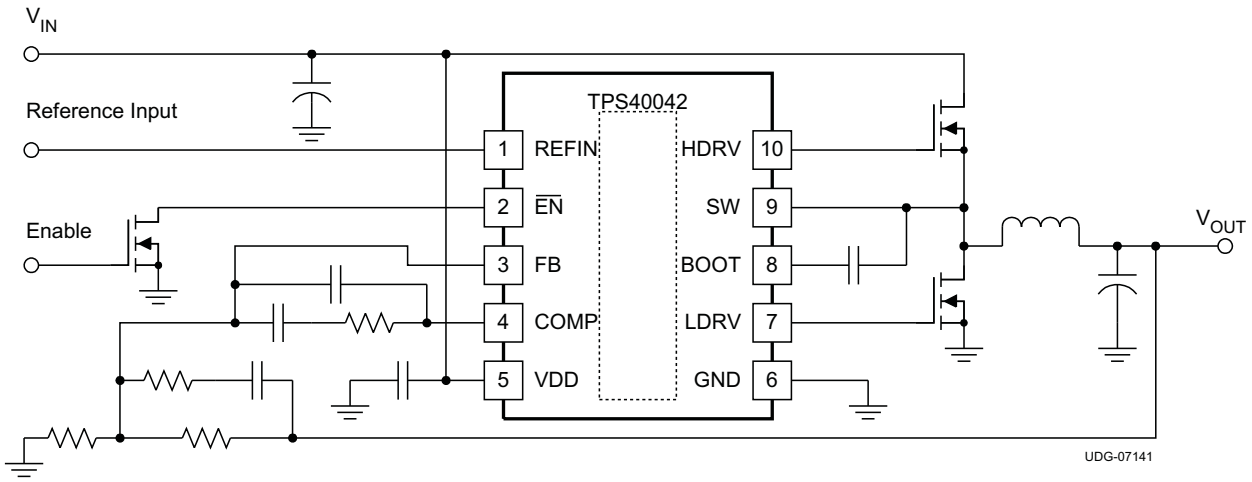
APPLICATIONS

- **DDR Memory**
- **Point of Load**
- **Telecommunications**
- **DC to DC Modules**

CONTENTS

DESCRIPTION

The TPS40042 DC/DC controller is designed to operate with an input source between a 3.0 V and 5.5 V. To reduce the number of external components, a number of operating parameters are fixed internally. The operating frequency for example, is internally set at 600 kHz. (Continued)



DESCRIPTION (CONT.)

One of three short circuit threshold levels may be selected by the addition of an external resistor from the COMP pin to circuit ground (no resistor is the default setting). During power on, and before the internal soft start commands the output voltage to rise, the TPS40042 enters a calibration cycle, measures the current out of the COMP pin, and selects an internal SCP threshold voltage. At the end of the 1.5-ms calibration time, the output voltage is allowed to enter soft-start. During operation, the selected SCP threshold voltage is compared to the upper MOSFET's voltage drop during its ON time to determine whether there is an overload condition. If the voltage across the MOSFET exceeds the threshold voltage, the TPS40042 counts seven continuous pulses before shutting completely OFF for seven soft start charge/discharge cycles, after which, the TPS40042 attempts to restart the output.

During startup, both the high-side MOSFET switch and the synchronous rectifier are held in the OFF state until the internal soft start commands an output voltage higher than the voltage currently at the output. This may happen when the output is pre-biased at some voltage greater than zero and less than the desired regulation voltage. When the internal soft start first commands the output to rise, the pulse width of the synchronous rectifier is slowly increased from zero to the full 1-D conduction time by a number of discrete steps. In this way, inductor current is not allowed to reverse quickly, and ensures a monotonic startup of the output whether the output starts from zero or from a pre-bias level. If power is applied to the device while the $\overline{EN}$ (enable low) pin is allowed to float high, the TPS40042 remains OFF. Only when the $\overline{EN}$ pin is pulled down towards ground is the controller allowed to start.

ORDERING INFORMATION

OPERATING FREQUENCY	PACKAGE	TAPE AND REEL QTY.	PART NUMBER
600 kHz	Plastic 10-pin SON (DRC)	250	TPS40042DRCT
600 kHz	Plastic 10-pin SON (DRC)	3000	TPS40042DRCR

DEVICE RATINGS

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted, all voltages are with respect to GND.)

PARAMETER		VALUE	UNIT
VDD		6.5	V
SW		-3 to 10.5	
SW	transient (< 50 ns)	-5	
BOOT		SW+6.5	
HDRV		SW to SW+6.5	
$\overline{EN}$, FB, LDRV ,REFIN		-0.3 to 6.5	
COMP		-0.3 to 3	
	Operating junction temperature	-40 to 150	°C
	Storage junction temperature	-55 to 150	

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
V_{VDD}	Input voltage to VDD pin	3.0		5.5	V
V_{REFIN}	Voltage applied to REFIN pin during regulation	0.5		1.5	V
T_J	Junction temperature	-40		125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

PARAMETER	MIN	TYP	MAX	UNIT
Human body model		2500		V
CDM		1500		V

PACKAGE DISSIPATION RATINGS(1)

THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 85°C POWER RATING
48°C/W	2W	0.8W

(1) For more information on the DRC package and the test method, refer to TI technical brief, literature number SZZA017.

ELECTRICAL CHARACTERISTICS

T_J = -40 °C to 85°C V_{VDD} = 5 V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VDD}	Input voltage range (1)		3.0		5.5	V
IDD_{sd}	Shutdown	$V_{\overline{EN}} = V_{VDD}$		100	180	µA
IDDq	Quiescent	V_{FB} = 0.8 V		1.0	2.0	mA
IDDs	Switching current	No load at HDRV/LDRV		3.0		
$UVLO_{ON}$	Minimum turn-on voltage		1.90	2.05	2.2	V
$UVLO_{HYS}$	Hysteresis		80	130	200	mV
OSCILLATOR/ RAMP GENERATOR						
f_{PWM}	PWM frequency	3.0 V < V_{VDD} < 5.5 V	500	600	700	kHz
f_{PWM}	PWM frequency	V_{VDD} = 5.0 V, 0°C < T_J < 70°C	540	600	660	kHz
V_{RAMP}	Ramp amplitude PP	$V_{PEAK} - V_{VALLEY}$	0.75	0.87	1.0	V
V_{VALLEY}	Ramp valley voltage			0.4		V
PWM						
MAXDUTY	Maximum duty cycle,	V_{FB} = 0 V, 3.0 V < V_{VDD} < 5.5 V	88%	95%		
MINDUTY	Minimum duty cycle				0%	
MIN pulse width (2)	Minimum controllable pulse width	Minimum width control range before jumping to zero.		90	150	ns
ERROR AMPLIFIER						
V_{OS}	FB to REFIN offset voltage	0.5 V < V_{REFIN} < 1.5 V	-5	0	5	mV
I_{FB}	FB, REFIN input bias current			-30	-125	nA
V_{OH}	High level output voltage	I_{OH} = 0.5 mA, V_{FB} = 0 V, V_{VDD} = 5.5 V	2.0	2.5		V
V_{OL}	Low level output voltage	I_{OL} = 0.5 mA, V_{FB} = V_{VDD}		80	150	mV
I_{OH}	Output source current	V_{COMP} = 0.7 V, V_{FB} = GND	1	6		mA
I_{OL}	Output sink current	V_{COMP} = 0.7 V, V_{FB} = V_{VDD}	2	8		
G_{BW} (2)	Gain bandwidth		5	10		MHz
A_{OL}	Open loop gain		55	85		dB
SHORT CIRCUIT PROTECTION						
$_{TH1}$	Low short circuit threshold voltage	Resistor COMP to GND = 2.4 kΩ, T_J = 25°C	80	105	130	mV
V_{TH2}	Medium short circuit threshold voltage	Default: No resistor COMP to GND, T_J = 25°C	140	175	210	
V_{TH3}	High short circuit threshold voltage	Resistor COMP to GND = 12 kΩ, T_J = 25°C	250	310	370	
$V_{TH(tc)}$ (2)	Threshold temperature coefficient			3100		ppm
$t_{ON(oc)}$ (2)	Minimum HDRV pulse time in over current			190		ns
$t_{SWOCblank}$ (2)	SW leading edge blanking pulse in over current detection			100		
t_{HICCUP}	Hiccup time between restarts			40		ms

(1) V_{VDD} operation to 2.25 V is possible with some degradation in specifications. Under this condition, the V_{REFIN} range is limited to 0.5 V to 0.7 V.

(2) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_J = -40 °C to 85°C V_{VDD} = 5 V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START/ENABLE						
t_{CAL} (3)	Calibration time before softstart begins		1.0	1.6	2.5	ms
t_{SS} (3)	Soft start time (4)	FB rise time from 0 V to V_{REFIN} = 1.5 V	4.5	6.0	7.5	
t_{REG}	Time to voltage regulation	Sum of t_{CAL} plus t_{SS} ; V_{REFIN} = 1.5 V	5.5	7.6	10	
V_{EN}	Enable threshold	$\overline{EN}$ voltage w.r.t. V_{VDD}	-0.8	-1.2	-1.6	V
V_{ENHYS}	Enable hysteresis			50		mV
BOOTSTRAP						
$R_{BOOT3V3}$	Bootstrap switch resistances	V_{BOOT} to V_{VDD}, V_{VDD} = 3.3 V		50		Ω
R_{BOOT5V}		V_{BOOT} to V_{VDD}, V_{VDD} = 5 V		30		
OUTPUT DRIVER						
$R_{HDHI3V3}$	HDRV pull-up resistance	V_{BOOT} - V_{SW} = 3.3 V, I_{SRCE} = 100 mA		3.0	5.5	Ω
$R_{HDLO3V3}$	HDRV pull-down resistance	V_{BOOT} - V_{SW} = 3.3 V, I_{SINK} = 100 mA		1.5	3	
$R_{LDHI3V3}$	LDRV pull-up resistance	V_{VDD} = 3.3 V, I_{SOURCE} = 100 mA		3.0	5.5	
$R_{LDLO3V3}$	LDRV pull-down resistance	V_{VDD} = 3.3 V, I_{SINK} = 100 mA		1.0	2.0	
t_{RISE} (5)	LDRV, HDRV rise time	C_{LOAD} = 1 nF		15	35	ns
t_{FALL} (5)	LDRV, HDRV fall time	C_{LOAD} = 1 nF		10	25	
T_{DEAD} HL	Adaptive timing HDRV to LDRV	No load	15	30	45	
T_{DEAD} LH	Adaptive timing LDRV to HDRV	No load	5	15	35	
SWITCH NODE						
I_{LEAK}	Leakage current	$V_{\overline{EN}}$ = V_{VDD}	-2			µA
THERMAL SHUTDOWN						
t_{SD} (5)	Shutdown temperature			145		°C
	Hysteresis			15		

(3) t_{CAL} and t_{SS} track with temperature and input voltage
(4) Soft start time is a function of V_{REFIN}. See Applications section for further detail.
(5) Ensured by design. Not production tested.

TYPICAL CHARACTERISTICS

Quiescent Current (Non-Switching)

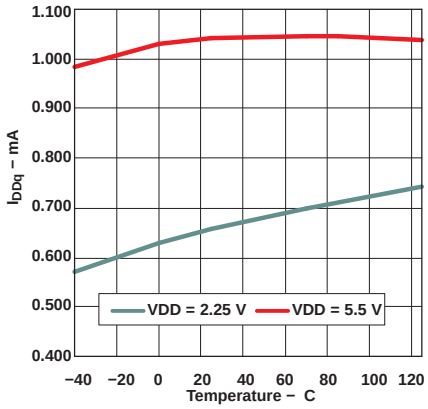


Figure 1.

Shutdown Current

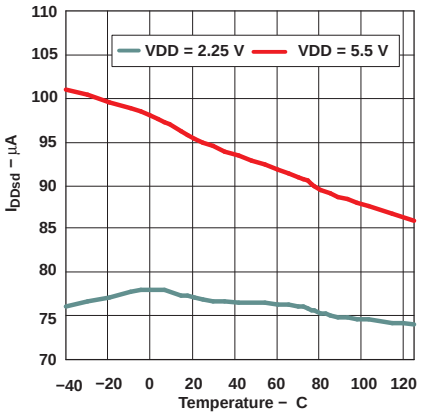


Figure 2.

UVLO Threshold

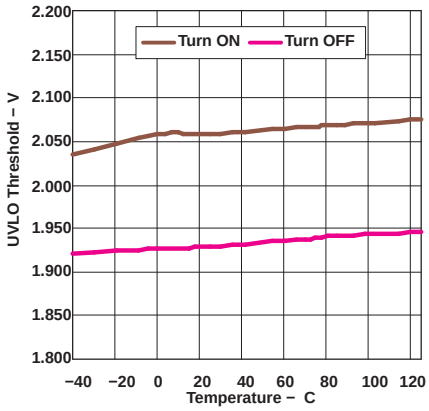


Figure 3.

$\overline{EN}$ Threshold

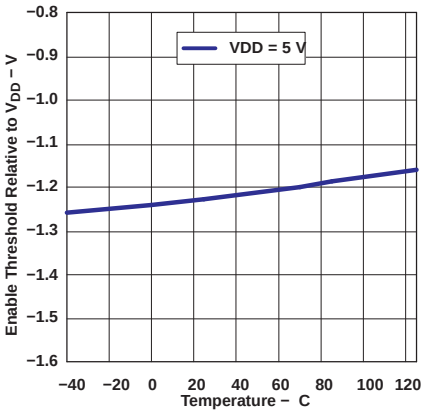


Figure 4.

Oscillator Frequency

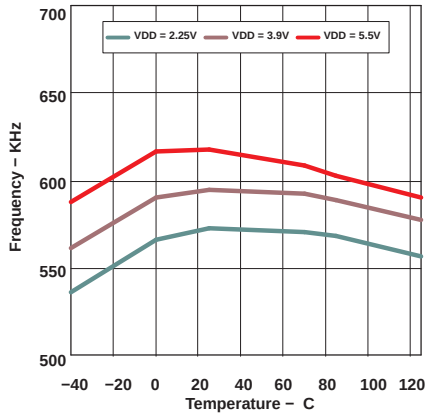


Figure 5.

Soft Start Time; V_{REFIN} = 1.5 V

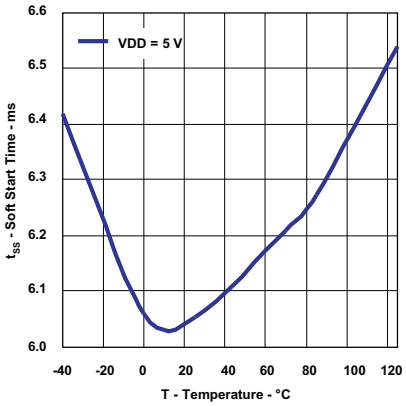


Figure 6.

TYPICAL CHARACTERISTICS (continued)

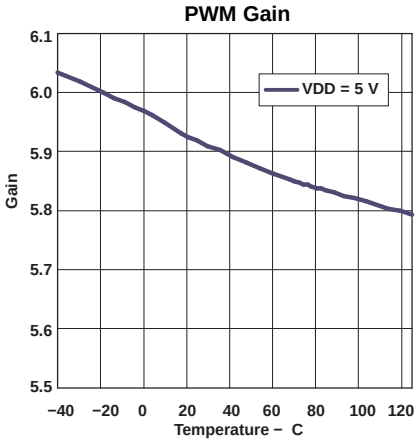


Figure 7.

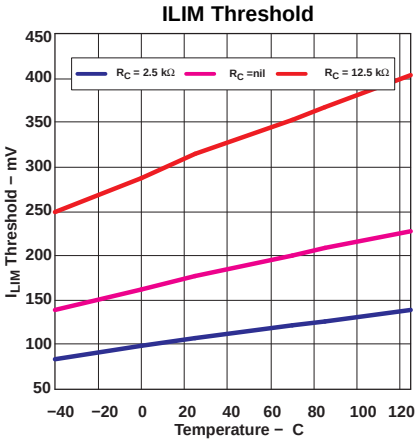


Figure 8.

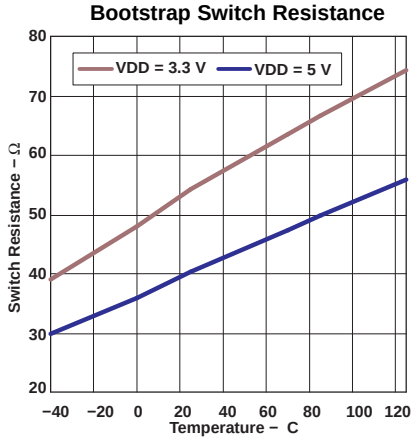


Figure 9.

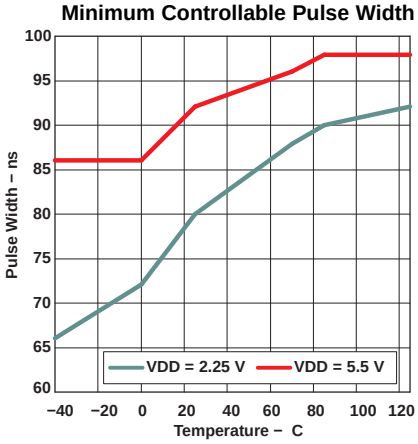


Figure 10.

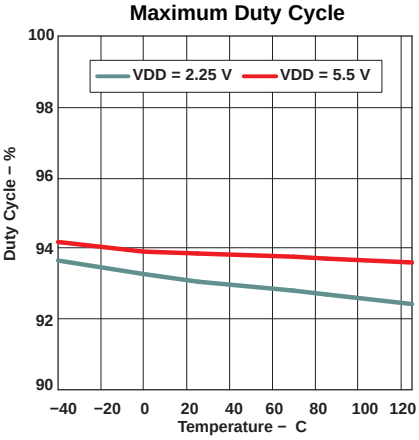


Figure 11.

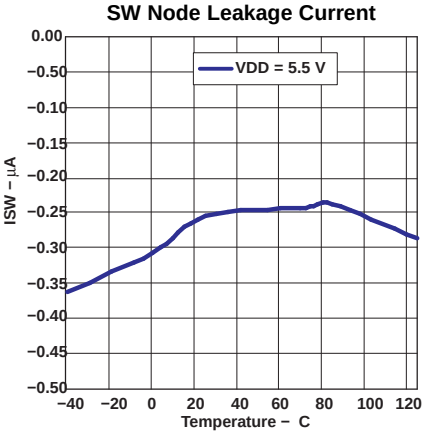


Figure 12.

DEVICE INFORMATION

TERMINAL CONFIGURATION

The package is an 10-pin SON (DRC) package.

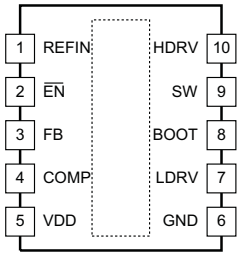


Figure 13. DRC Package Terminal Configuration (Top View)

Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BOOT	8	I	Input (bootstrapped) supply to the high-side gate driver for PWM enabling the gate of the high side FET to be driven above the input supply rail. Connect a ceramic capacitor from this pin to SW. This capacitor is charged from the VDD pin voltage through an internal switch. The switch is turned ON during the off time of the converter. To slow down the turn on of the external MOSFET, a small resistor (1 Ω to 3 Ω) may be placed in series with the bootstrap capacitor. See Applications Section to calculate the appropriate value.
COMP	4	O	Output of the error amplifier and connection node for loop feedback components. The voltage at this pin determines the duty cycle for the PWM. Optionally, a resistor from this pin to ground is used to determine the voltage threshold used for short circuit protection. (See Application Section) • Low threshold R = 2.4 kΩ, ±10% • Mid threshold R = not installed • High threshold R = 12 kΩ, ±10%
$\overline{EN}$	2	I	Active low enable input allows ON/OFF operation of the controller. If power is applied to the TPS40042 while the $\overline{EN}$ pin is allowed to float high, the TPS40042 remains disabled (both external switches are held OFF). Only when the $\overline{EN}$ pin is pulled to 1.2 V below VDD is the TPS40042 allowed to start. An internal 100-kΩ resistor is connected between VDD and $\overline{EN}$ to provide pull up. Connect this pin to GND to bypass the enable function.
FB	3	I	Inverting input of the error amplifier. In closed loop operation, the voltage at this pin is at the same potential as the REFIN pin. A series resistor divider from the converter output to ground, with the center connection tied to this pin, determines the value of the regulated output voltage. This pin is also a connection node for loop feedback components.
GND	6		Electrical ground connection for the device.
HDRV	10	O	This is the gate drive output for the high side N-channel MOSFET switch for PWM. It is referenced to SW and is bootstrapped for enhancement of the high-side switch.
LDRV	7	O	Gate drive output for the low-side synchronous rectifier (SR) N-channel MOSFET.
REFIN	1	I	Non-inverting imput to the error amplifier. A precision voltage must be applied to this pin before the TPS40042 is enabled. Since this input is connected directly to the non-inverting pin of the error amplifier, the quality of the voltage at this pin has a direct impact on the quality of the output voltage.
SW	9	O	Connection to the switched node of the converter and the power return for the upper gate driver. There should be a high current return path from the source of the upper MOSFET to this pin. It is also used by the adaptive gate drive circuits to minimize the dead time between upper and lower MOSFET conduction.
VDD	5	I	Power input to the device. This pin should be locally bypassed to GND with a low ESR ceramic capacitor of 1 μF or greater.
	PPAD		Thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane. See Application Section for PC board layout information.

Block Diagram

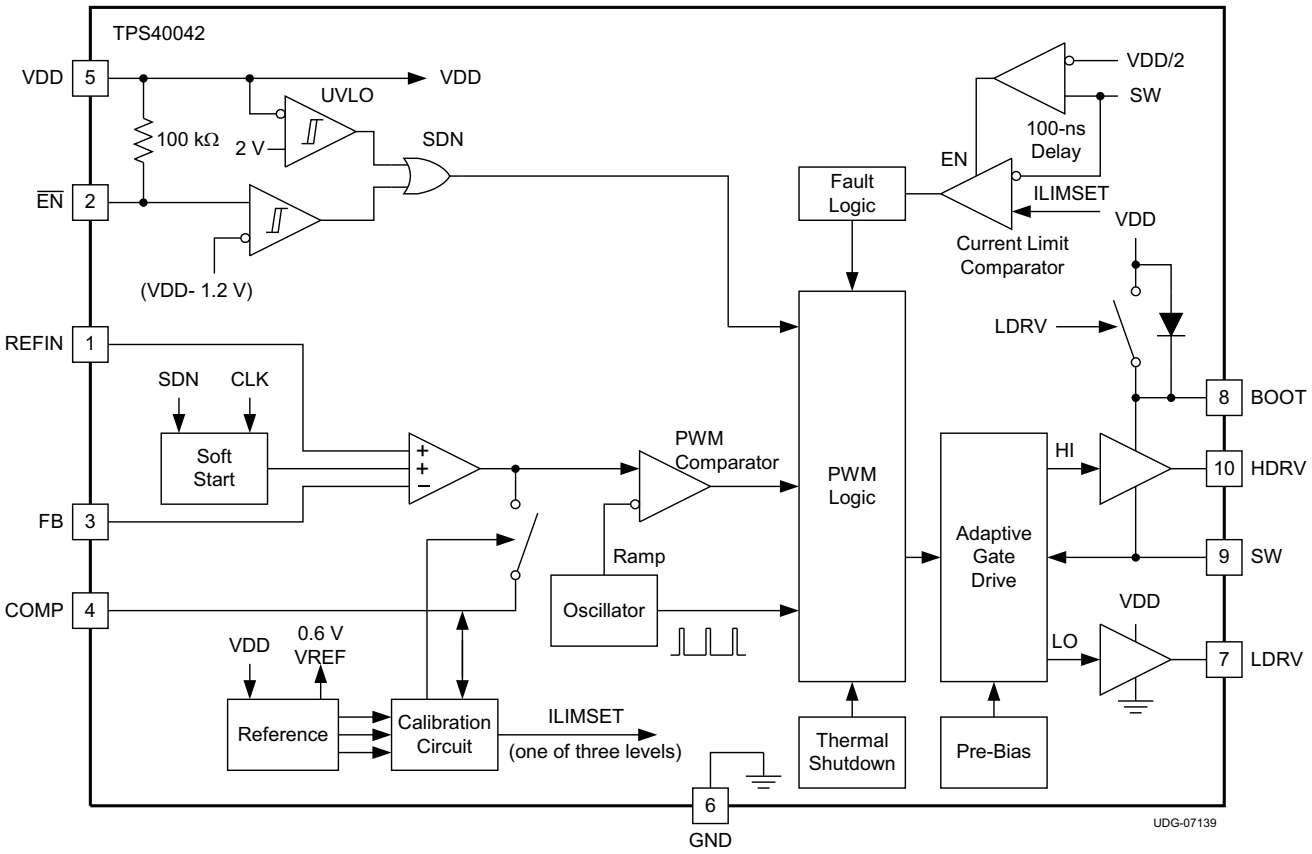


Figure 14. Functional Block Diagram

APPLICATION INFORMATION

Functional Description

The TPS40042 is a fixed frequency voltage mode synchronous buck controller. In operation, the Synchronous Rectifier (SR) is allowed to conduct current in both directions, allowing a converter to operate in continuous cnduction (CCM) mode, even under no load conditions, simplifying feedback loop compensation requirements. During startup, internal circuitry modulates the switching of the synchronous rectifier to prevent discharging of the output if a pre-biased condition exists.

Voltage Reference Input

An external voltage reference input is required. During operation, the voltage must be between 0.5v and 1.5v.

REFIN may be used in either of two ways:

- As a reference input. In this case, REFIN must be stable before the TPS40042 is enabled. the internal soft-start controls the rate of rise of the output voltage during startup. The time to reach output voltage regulation is dependent on the voltage on the REFIN pin.
- As a tracking input. If REFIN is held to zero until soft-start has completed (7.6-ms), then REFIN will control the output voltage during startup and regulation.

Voltage Error Amplifier

The error amplifier has a bandwidth of greater than 5 MHz, and open loop gain of at least 55 dB. The output voltage swing is limited to just above and below the oscillator ramp levels to improve transient response.

Loop Compensation

Voltage mode buck type converters are typically compensated using Type III networks. Please refer to the Design Example for detailed methodology in designing feedback loops for voltage mode converters.

DESIGN HINT: When designing the compensation for the feedback loop, remember that a low impedance compensation network combined with a long network time constant can cause the short circuit threshold setting to not be as expected. The time constant and impedance of the network connected from COMP to FB should be as shown in Equation 1 to guarantee no interaction with the short circuit threshold setting.

$$\frac{0.4\,V}{R_{FB}} \times e^{\left(-\frac{t}{R_{FB} \times C_{FB}}\right)} < 10\,\mu A \quad (1)$$

where

- t is 1 ms, the sampling time of the short circuit threshold setting circuit
- R_{FB} and C_{FB} are the values of the feedback components. e.g. R3 and C4 of the Design Example.

Oscillator

The oscillator frequency is internally fixed. The TPS40042 operating frequencies is nominally 600 kHz.

UVLO

When the input voltage is below the UVLO threshold, the TPS40042 turns off the internal oscillator and holds all gate drive outputs in the low (OFF) state. When the input rises above the UVLO threshold, and the $\overline{EN}$ pin is below the turn ON threshold, the start-up sequence is allowed to begin.

Enable and Start-Up Sequence

The $\overline{EN}$ pin of the TPS40042 is internally pulled to VDD. When power is applied to VDD, the $\overline{EN}$ pin is allowed to float high, and the TPS40042 remains OFF. Only when the $\overline{EN}$ pin is externally pulled below the threshold voltage of (V_{VDD} - 1.2 V) is the TPS40042 allowed to start. When enabled, the TPS40042 enters a calibration cycle where the short circuit current threshold is determined. The TPS40042 monitors the current out of the COMP pin and selects a threshold based on the sensed value of the current. See *Selecting the Short Circuit Current Limit Threshold* section for for details. When this calibration time is completed, the soft-start cycle is allowed to begin. See Figure 15 below.

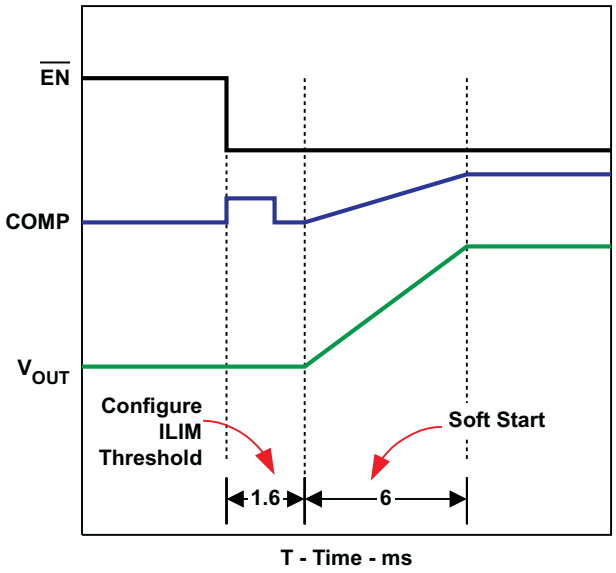


Figure 15. Startup with V_{REFIN} =1.5 V

DESIGN HINT: If the enable function is not used, the $\overline{EN}$ pin should be connected to ground (GND).

DESIGN HINT: When designing the feedback loop compensation, ensure the capacitors used are not so large that they distort the COMP pin calibration waveform.

Soft Start

At the end of a calibration cycle, the TPS40042 slowly increases the voltage to the non-inverting input of the error amplifier. In this way, the output voltage slowly ramps up until the voltage on the non-inverting input to the error amplifier reaches the external (V_{REFIN}) reference voltage. At that time, the voltage at the non-inverting input to the error amplifier remains at the applied reference voltage.

During the soft-start interval, pulse-by-pulse current limiting is active. If seven consecutive current limit pulses are detected, overcurrent is declared and a timeout period equivalent to seven calibration/soft-start cycles goes into effect. See *Output Short Circuit Protection* section for details.

Since the rate of rise of the output voltage is constant with different REFIN voltage levels, the actual soft start time is directly proportional to the value of the external reference voltage. The rate of rise at the non-inverting input of the error amplifier is 0.25 V/ms. The rate of rise measured at the output terminals of the DC/DC converter will be increased by the output voltage-to-reference voltage ratio.

$$t_{SS} = \left(\frac{V_{REFIN}}{1.5\,V} \right) \times 6.0\,ms \quad (2)$$

For example, if a 1-V external reference is applied for a 1.5-V output DC/DC converter, the soft-start time-to-output voltage regulation is 4 ms.

Pre-Bias Startup

The TPS40042 supports pre-biased output voltage applications. In cases where the output voltage is held up by external means while the TPS40042 is off, full synchronous rectification is disabled during the initial phase of soft starting the output voltage. When the first PWM pulses are detected during soft start, the controller slowly initiates synshronous rectification by starting the synchronous rectifier with a narrow on time. It then increments that on time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This approach prevents the sinking of current from a pre-biased output, and ensures the output voltage startup and ramp to regulation is smooth and controlled.

NOTE:

If the output is pre-biased, PWM pulses start when the internal soft-start voltage rises above the error amplifier input (FB pin).

Figure 16 below depicts the waveform of the HDRV and LDRV output signals at the beginning PWM pulses. When HDRV turns off, diode rectification is enabled. Before the next PWM cycle starts, LDRV is turned on for a short pulse. With every clock cycle, the leading edge of LDRV is modulated, increasing the on time of the synchronous rectifier. Eventually, the leading edge of LDRV coincides with the falling edge of HDRV to achieve full synchronous rectification. During normal operation of the converter, the TPS40042 operates in full two quadrant source/sink mode.

Figure 17 shows the startup waveform of a 1.2-V output converter under three different pre-biased output conditions. The lowest trace is when there is no pre-bias on the output. The center and top most traces indicate converter startup with 0.5-V and 1.0-V pre-bias conditions.

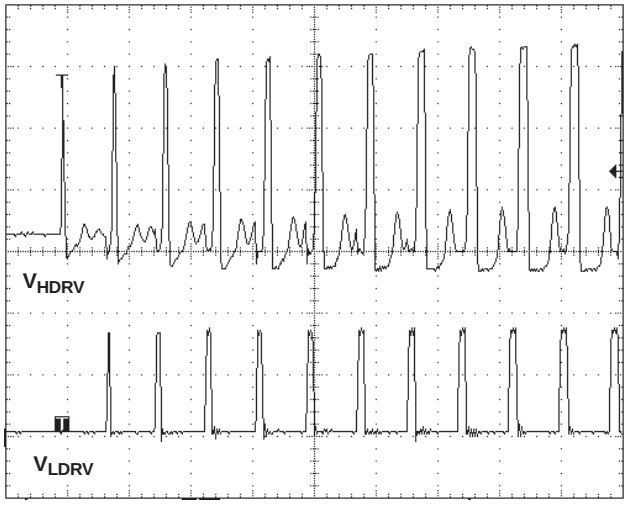


Figure 16. MOSFET Drivers at Beginning of Soft Start

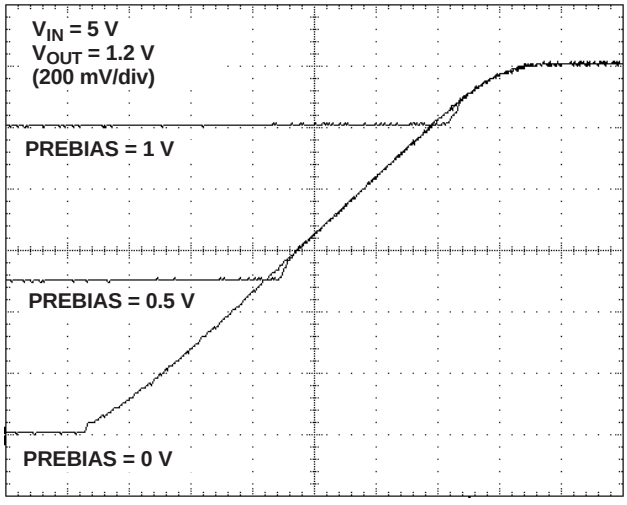


Figure 17. Startup Waveforms; VREFIN = 0.6 V

The recommended output voltage pre-bias range is less than or equal to 90% of the final regulation voltage. A pre-biased output voltage of 90% to 100% of final regulation could lead to the sinking of current from the pre-bias source. If the pre-biased voltage is greater than the designed converter output regulation voltage, then upon the completion of the soft-start interval, the TPS40042 turns ON the Synchronous Rectifier, therby drawing current from the output to bring the output voltage into regulation. Note that this may cause some undershoot of the output voltage before entering regulation.

Output Short Circuit Protection

To minimize circuit losses, the TPS40042 uses the $R_{DS(on)}$ of the upper MOSFET switch as the current sensing element. The current limit comparator, initially blanked during the first portion of each switching cycle, senses the voltage across the high-side MOSFET when it is fully ON. This voltage is compared to an internally selected short circuit current (SCC) limit threshold voltage. If the comparator senses a voltage drop across the high-side MOSFET greater than the SCC limit threshold, it outputs an OC pulse. This terminates the current PWM pulse

preventing further current ramp-up, and sets the fault counter to count up one count on the next clock cycle. Similarly, if no OC pulse is detected, the fault counter decrements by one count. If seven OC pulses are summed, a fault condition is declared and the upper switch of the PWM output of the chip is immediately disabled (turned OFF) and remains that way until the fault time-out period has elapsed. Both HDRV and LDRV drivers are kept OFF during the fault time-out.

The fault time-out period is determined by cycling through seven internal soft-start time periods. At the end of the fault time-out period, startup is attempted again.

The main purpose is for hard fault protection of the power switches. The internal SCC voltage has a positive temperature coefficient designed to improve the short circuit threshold tolerance variation with temperature. However, given the tolerance of the voltage thresholds and the $R_{DS(on)}$ range for a MOSFET, it is possible to apply a load that thermally damages the external MOSFETs.

Selecting the Short Circuit Current Limit Threshold

The TPS40042 uses one of three user selectable voltage thresholds. During the calibration interval at power on or enable (Figure 15), the TPS40042 monitors the current out of the COMP pin and selects a threshold based on the sensed value. If the current is zero; that is, no resistor is connected between COMP and GND, then the threshold voltage level is 180 mV. If a 2.4-kΩ resistor is connected between COMP and GND, then the threshold voltage level is 105 mV. If a 12-kΩ resistor is connected between COMP and GND, then the threshold voltage is 310 mV.

Once calibration is complete, the selected SCP threshold level is latched into place and remains constant. In addition, the sensing circuits on COMP pin during calibration are disconnected from the COMP pin, and soft start is allowed to begin.

Synchronous Rectification and Gate Drive

In a buck converter, when the upper switch MOSFET turns off, current is flowing in the inductor to the load. This current cannot be stopped immediately without using infinite voltage. To give this current a path to flow and maintain voltage levels at a safe level, a rectifier or catch device is used. This device can be either a diode, or it can be a controlled active device. The TPS40042 provides a signal to drive an N-channel MOSFET as a synchronous rectifier (SR). This control signal is carefully coordinated with the drive signal for the main switch so that there is minimum dead time from the time that the SR turns OFF and the upper switch MOSFET turns ON, and minimum delay from when the upper switch MOSFET turns OFF and the SR turns ON.

NOTE:

The longer the time spent in diode conduction during the rectifier conduction period, the lower the converter efficiency.

The drivers for the external HDRV and LDRV MOSFETs are capable of driving a gate to source voltage of approximately 5 V. At VDD = 5 V, the drivers are capable of driving MOSFETs appropriate for a 15-A converter. The LDRV driver switches between VDD and ground, while HDRV driver is referenced to SW and switches between BOOT and SW. The drivers have non-overlapping timing that is governed by an adaptive delay circuit that minimizes body diode conduction in the synchronous rectifier.

Gate Drive Resistors

The TPS40042's adaptive gate delay circuitry monitors the HDRV-to-SW and LDRV-to-GND voltages to determine the state of the external MOSFET switches. Any voltage drop across an external series gate drive resistor is sensed as reduced gate voltage during turn-off and may interfere with the MOSFET timing.

DESIGN HINT: A resistor should never be placed in series with the synchronous rectifiers gate and the gate trace should be kept as short as practical in the layout.

Total Gate Charge

The internal voltage sensing of the external MOSFET gate voltages used by the TPS40042 to control the dead-times between turn-off and turn-on can be sensitive to large MOSFET gate charges, especially when different gate charges are used for the high-side and low-side MOSFETs. Increased gate charge increases MOSFET switching times and decreases the dead-time between the MOSFETs switching.

DESIGN HINT:	MOSFETs with no more than 40 nC of total gate charge should be selected. The upper switch MOSFET's gate charge should be no less than 60% of the synchronous rectifier's gate charge to minimize the turn-on/turn-off delay mismatch between the high-side and low-side MOSFET.

Synchronous Rectifier dV/dt Turn-On

As the upper switch MOSFET turns on, the switch node voltage rises from close to ground to VIN in a very short period of time (typically 10 ns to 30 ns) resulting in very high voltage spikes on the switch node. The construction of a MOSFET creates parasitic capacitances between its terminals, particularly the gate-to-drain and gate-to-source, creating a capacitive divider between the drain and source of the MOSFET with the gate at its mid-point. If the gate-to-drain charge (Q_{GD}) is larger than the gate-to-source charge (Q_{GS}), the capacitive divider places proportionally more charge on the gate of the MOSFET as the switch node voltage rises than is shunted to GND. In extreme cases, this can cause the synchronous rectifier gate voltage to rise above the turn on threshold voltage of the MOSFET and causes cross-conduction. This is called dV/dt turn-on. It increases power dissipation in both the high-side and the low-side MOSFET, reducing efficiency.

DESIGN HINT:	Select a synchronous rectifier MOSFET with a Q_{GD} to Q_{GS} ratio of less than one and provide a wide, low resistance, low inductance loop in the synchronous rectifier gate drive circuit. (See Layout Consideration)

DESIGN HINT:	A resistor in series with the boost capacitor slows the turn on of the high-side MOSFET, and reduces the dV/dt of the switch node. See Boost Capacitor Series Resistor section.

Bootstrap for N-Channel MOSFET Drive

The PWM duty cycle is limited to a maximum of 95%, allowing the bootstrap capacitor to charge during every cycle. During each PWM OFF period, the voltage on VDD charges the bootstrap capacitor. When the PWM switch is next commanded to turn ON, the voltage used to drive the MOSFET is derived from the voltage on this capacitor. Since this is a charge transfer circuit, the value of the bootstrap capacitor must be sized such that the energy stored in the capacitor on a per cycle basis is greater then the gate charge requirement of the MOSFET being used. See the Design Example section for details.

Bootstrap Capacitor Series Resistor

Since resistors should not be placed in series with the high-side gate, it may be necessary to place a small 1-Ω to 3-Ω resistor in series with the bootstrap capacitor to control the turn-on of the main switching MOSFET and reduce the dV/dt rate of rise of the switch node voltage. A resistor placed between the BOOT pin and the bootstrap capacitor increases the series resistance during the turn-on of the high-side MOSFET, and has no effect during the high-side MOSFET's turn-off period. This prevents the TPS40042 from sensing the upper switch MOSFET's turn-off too early and reducing the upper switch MOSFET turn-off to the SR MOSFET turn-on delay timing too far.

DESIGN HINT:	To reduce EMI, place a small 1-Ω to 3-Ω resistor in series with the boost capacitor to control the turn-on of the main switching FET.

External Schottky Diode for Low Input Voltage

The TPS40042 uses an internal P-channel MOSFET switch between VDD and BOOT to charge the bootstrap capacitor during synchronous rectifier conduction time. At low input voltages, a MOSFET can not be turned on

hard enough to rapidly replenish the charge required to turn on an (high gate charge) external high-side MOSFET. For this situation, an external Schottky diode between the VDD and BOOT pins may be added. While the diode carries very small average current (Q_G x F_{SW}) it may be required to carry several hundred mA of peak surge current. The diode should be rated for at least 500 mA of surge current. For higher input voltage applications, if a resistor is used in series with the boost capacitor, connect the diode to the junction of the resistor and capacitor to remove the added resistance from the capacitor's charge path.

DESIGN HINT:	For low input voltages, and a high gate charge upper switch MOSFET, a small Schottky diode should be placed from VDD to BOOT. Do not use a resistor in series with the boost capacitor.

VDD Bypass and Filtering

To prevent switching noise from being injected into the TPS40042 control circuitry, a ceramic capacitor (1 µF minimum) must be placed as close to the VDD pin and GND pad as possible.

VDD Filter Resistor

To further limit the noise on VDD, a small 1-Ω to 2-Ω resistor may be placed between the input voltage and the VDD pin to create a small filter to VDD. The resistor should connect near the drain of the upper switch MOSFET to prevent trace IR drops from increasing the sensed voltage drop. The resistor itself should be placed close to Pin 5.

The current through the resistor includes the device's no-load switching current of 2 mA plus gate switching current. The voltage drop induced across this resistor reduces the VDD-to-SW voltage sensed by the over current protection circuitry within the device. This results with the apparent voltage drop across the upper switch MOSFET being increased, thereby decreasing the current at which protection will occur. To minimize this effect, the resistor value should be selected to yield less than a 25-mV drop.

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown level, the PWM and the oscillator are turned off and HDRV and LDRV are driven off. When the junction cools to the required level, the PWM soft starts as during a normal power-up cycle.

Package Power Dissipation

The power dissipation in a controller is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Qg, of the external MOSFETs, and the operating frequency of the converter. The total power dissipation is:

$$P_T = V_{DD} \times \left(Iq + f_{SW} \times \left(Q_{SW} + Q_{SR} \right) \right) \quad (3)$$

where

- I_Q is the quiescent operating current (neglecting drivers)
- $Qg_{SW}$is the total gate charges of the upper switch MOSFET
- Qg_{SR} is the total gate charges of the synchronous rectifier MOSFET

The maximum power capability of the PowerPad™ package is dependent on the layout as well as air flow. The thermal impedance from junction-to-air assuming 2-oz. copper trace and thermal pad with solder and no air flow is detailed in Reference [5].

PCB Layout Guidelines

A synchronous BUCK power stage has two primary current loops, the input current loop that carries high ac discontinuous current and an output current loop that carries high dc continuous current. The output current loop carries low ac inductor ripple current.

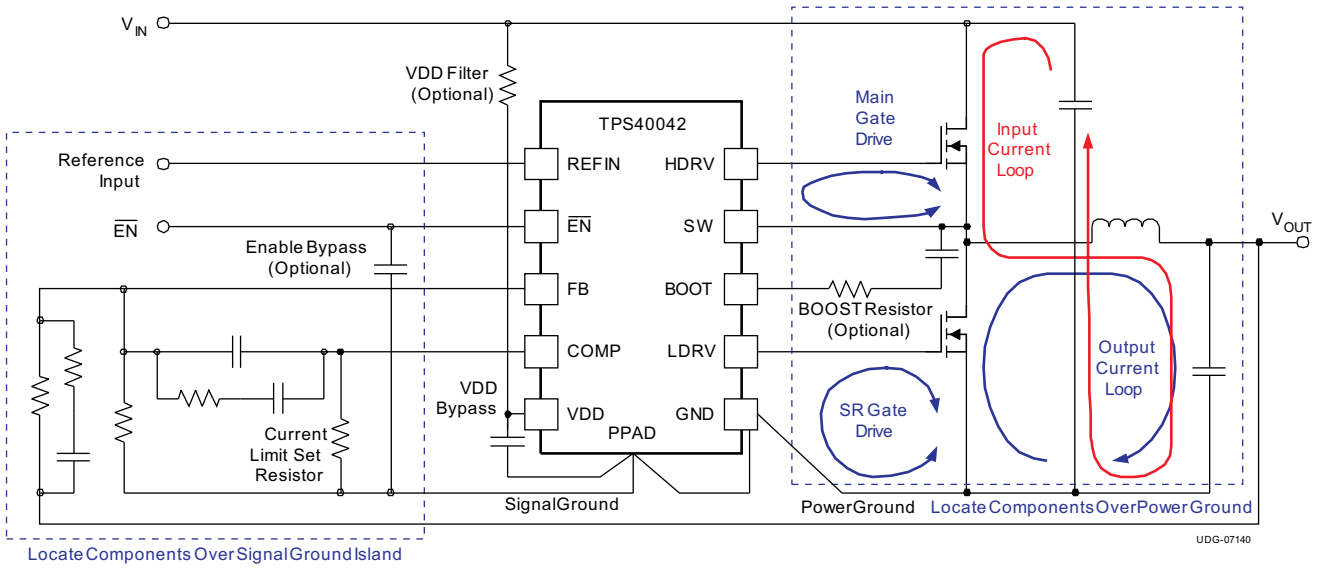


Figure 18. Synchronous BUCK Power Stage

Power Component Routing

As shown in Figure 18, the input current loop contains the input capacitors, the switching MOSFET, the inductor, the output capacitors, and the ground path back to the input capacitors. To keep this loop as small as possible, it is good practice to place some ceramic capacitance directly between the drain of the main switching MOSFET and the source of the synchronous rectifier (SR) through a power ground plane directly under the MOSFETs.

The output current loop includes the filter inductor, the output capacitors, and the ground return between the output capacitors and the source of the synchronous rectifier MOSFET. As with the input current loop, the ground return between the output capacitor ground and the source of the SR source should be routed under the inductor and MOSFETs to minimize the power loop area.

Device to Power Stage Interface

The TPS40042 uses a very fast break-before-make anti-cross conduction circuit to minimize power loss. Adding external impedance in series with the gates of the switching MOSFETs adversely affects the converter's operation and must be avoided. The loop impedance (HDRV-to-gate plus source-to-SW and LDRV-to-SR gate plus SR source-to-GND) should be kept to less than 20 nH to avoid possible cross-conduction. The HDRV and LDRV connections should widen to 20 mils as soon as possible out from the device pin.

The return for the main switching MOSFET gate drive is the SW pin of the TPS40042. The SW pin should be routed to the source of the main switching FET with at least a 20-mils wide trace as close to the HDRV trace as possible to minimize loop impedance.

The return for the SR MOSFET gate drive is the TPS40042 GND pad. The GND pad should be connected directly to the source of the SR with at least a 20-mil wide trace directly under the LDRV trace. Use a minimum of 2 parallel vias to connect the GND pad to the source of the SR if multiple layers are used.

A small, less than 3-Ω resistor may be added in series with the BOOT pin to slow the turn-on of the upper switch MOSFET, thereby reducing the rising edge slew-rate of the switch node. In turn, this reduces EMI, increases upper MOSFET OFF to SR ON dead time, and minimizes induced dV/dt turn-on of the SR when the upper switch MOSFET turns on. It is recommended customers make provisions on their boards for this resistor and not use resistors in series with MOSFET gate leads.

VDD Filtering

A ceramic capacitor, 1 μF minimum, must be placed as close to the VDD pin and GND pad as possible with a 15-mil wide (or greater) trace. If used, a small series connected resistor (1 Ω to 2 Ω) may be placed less than 100 mils from the TPS40042 between the supply input voltage and the VDD pin to further reduce switching noise on the VDD pin.

NOTE:

The voltage drop across this resistor affects the level at which the over-current circuit operates by filtering the sensed VDD voltage.

Device Connections

If a current limit resistor is used (COMP to GND), it must be placed within 100 mils of the COMP pin to limit noise injection into the PWM comparator. Compensation components (feedback divider, and associated error amplifier components) should be placed over a signal ground island connected to the power ground at the GND pad through a 10-mil wide trace. If multiple layers are used, connect to GND through a single via on an internal layer opposite the connection to the source of the synchronous rectifier.

PowerPAD™ Layout

The PowerPAD™ package provides low thermal impedance for heat removal from the device. The PowerPAD™ derives its name and low thermal impedance from the large bonding pad on the bottom of the device. The circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depend on the size of the PowerPAD™ package. See PCB Layout Guidelines for further information.

Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) works well when 1-oz copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter plus 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. Refer to PowerPAD™ Thermally Enhanced Package[2] for more information on the PowerPAD™ package.

DESIGN EXAMPLES

Example 1. A 5-V to 1.8-V DC-to-DC Converter Using a TPS40042

The following example illustrates the design process and component selection for a 5-V to 0.9-V DDR termination synchronous buck converter. The design goal parameters are given in the table below. A list of symbol definitions is found at the end of this section.

Design Goal Parameters

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		4.5		5.5	V
$V_{INripple}$	Input ripple	I_{OUT} = 6 A			75	mV
V_{OUT}	Output voltage	I_{OUT} = 0 A, V_{IN} = 5 V		0.9		V
	Line regulation	V_{IN} = 4.5 A to 5.5 V		0.5%		
	Load regulation	I_{OUT} = 0 A to 6 A		0.5%		
V_{RIPPLE}	Output ripple	I_{OUT} = 6 A			36	mV
V_{TRANS}	Transient deviation	I_{OUT} = -2 A to 2 A, I_{OUT} = 2 A to -2 A		40		
I_{OUT}	Output current	V_{IN} = 4.5 V to 5.5 V	-6		6	A
F_{SW}	Switching frequency			600		kHz
	Size				1	In^2

For this example, the schematic shown in Figure 19 is used.

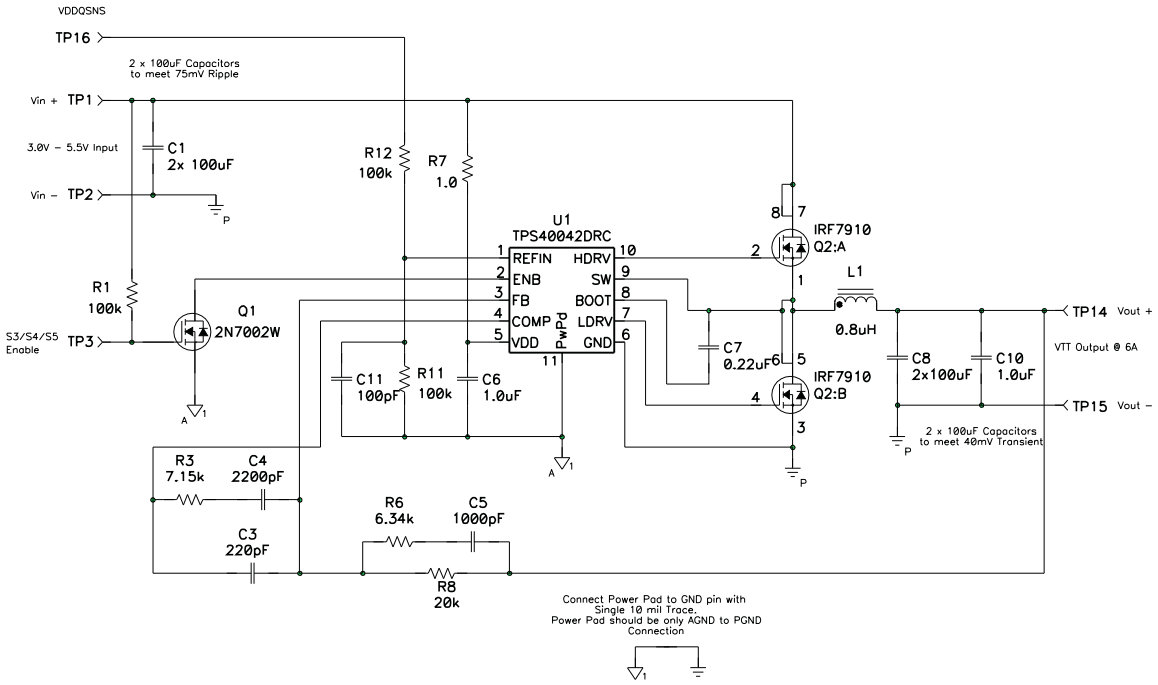


Figure 19. TPS40042 Sample Schematic

Inductor Selection

The inductor is typically sized for 30% peak-to-peak ripple current (I_{RIPPLE}) Given this target ripple current, the required inductor size is calculated by:

$$L = \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{F_{SW}} \quad (4)$$

Solving with $V_{IN(max)}$ = 5.5 V, an inductor value of 0.69 µH is obtained. A standard value of 0.8 µH is selected, resulting in 1.56-A peak-peak ripple. The RMS current through the inductor is approximated by the equation:

$$I_{L(rms)} = \sqrt{\left(I_{L(avg)}\right)^2 + \frac{1}{12}\left(I_{RIPPLE}\right)^2} = \sqrt{\left(I_{OUT}\right)^2 + \frac{1}{12}\left(I_{RIPPLE}\right)^2} \quad (5)$$

Using Equation 5, the maximum RMS current in the inductor is about 6 A.

Output Capacitor Selection (C8 & C9)

The selection of the output capacitor is typically driven by the output load transient response requirement. Equation 6 and Equation 7 estimate the output capacitance required for a given output voltage transient deviation.

$$C_{OUT(min)} = \frac{I_{TRAN(max)}^2 \times L}{\left(V_{IN(min)} - V_{OUT}\right) \times V_{TRAN} \times 2} \text{ when } V_{IN(min)} < 2 \times V_{OUT} \quad (6)$$

$$C_{OUT(min)} = \frac{I_{TRAN(max)}^2 \times L}{V_{OUT} \times V_{TRAN} \times 2} \text{ when } V_{IN(min)} > 2 \times V_{OUT} \quad (7)$$

For this example, Equation 7 is used in calculating the minimum output capacitance.

Based on a 4-A load transient with a maximum 40-mV deviation, a minimum of 177-µF output of capacitance is required.

The output ripple is divided into two components. The first is the ripple voltage generated by inductor ripple current flowing through the output capacitor's capacitance, and the second is the voltage generated by the ripple current flowing in the output capacitor's ESR. The maximum allowable ESR is then determined by the maximum ripple voltage and is approximated by:

$$ESR_{MAX} = \frac{V_{RIPPLE(total)} - V_{RIPPLE(cap)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(total)} - \left(\frac{I_{RIPPLE}}{C_{OUT} \times F_{SW}}\right)}{I_{RIPPLE}} \quad (8)$$

Based on 177 µF of capacitance, 1.56-A ripple current, 600-kHz switching frequency and a design goal of 36-mV ripple voltage, we calculate a maximum ESR of 13.6 mΩ. Two 1206, 100-µF, 6.3-V, X5R ceramic capacitors are selected to provide significantly less than 13.6 mΩ of ESR.

Peak Current Rating of Inductor

With output capacitance known, it is now possible to calculate the charging current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is approximated by:

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{T_{SS}} \quad (9)$$

Using the TPS40042's soft-start time of 5-ms, C_{OUT} = 200 µF and V_{OUT} = 0.9 V, I_{CHARGE} is found to be 40 mA. The peak current rating of the inductor is now found by:

$$L_{L(peak)} = I_{OUT(max)} + \frac{1}{2}\left(I_{RIPPLE}\right) + I_{CHARGE} \quad (10)$$

The inductor requirements are summarized in the table below.

Inductor Requirements

PARAMETER	SYMBOL	VALUE	UNITS
Inductance	L	0.8	µH
RMS current (thermal rating)	$I_{L(rms)}$	6.0	A
Peak current (saturation rating)	$I_{L(peak)}$	7.08	

A PG0083.801, 0.8 µH is selected for its small size, low DCR and high current handling capability.

Input Capacitor Selection (C1 & C2)

The input voltage ripple is divided between capacitance and ESR. For this design, $V_{RIPPLE(CAP)}$ = 50 mV and $V_{RIPPLE(ESR)}$ = 25 mV. The minimum capacitance and maximum ESR are estimated by:

$$C_{IN(min)} = \frac{I_{LOAD} \times V_{OUT}}{V_{RIPPLE(cap)} \times V_{IN} \times F_{SW}} \tag{11}$$

$$ESR_{MAX} = \frac{V_{RIPPLE(ESR)}}{I_{LOAD} + \frac{1}{2}\left(I_{RIPPLE}\right)} \tag{12}$$

For this design, C_{IN} > 60 µF and ESR < 3.5 mΩ. The RMS current in the input capacitors is estimated by:

$$I_{RMS(cin)} = I_{IN(rms)} - I_{IN(avg)} = \sqrt{\left[\left(I_{OUT}\right)^2 + \frac{1}{12}\left(I_{RIPPLE}\right)^2\right] \times \frac{V_{OUT}}{V_{IN}}} - \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \tag{13}$$

With $V_{IN} = V_{IN(max)}$, the input capacitors must support a ripple current of 1.56 A_{RMS}. Two 1206, 100-µF, X5R ceramic capacitors with about 2-mΩ ESR and a 2-A RMS current rating are selected. It is important to check the dc bias voltage derating curves to ensure the capacitors provide sufficient capacitance at the working voltage.

MOSFET Switch Selection (Q1 & Q2)

The switching losses for the upper switch MOSFET are estimated by:

$$P_{G1SW} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times \left(T_{RISE} + T_{FALL}\right) \times F_{SW} = V_{IN} \times I_{OUT} \times \frac{Q_{GS2\_Q1} + Q_{GD\_Q1}}{\frac{V_{DD} - V_{TH}}{R_{DRIVE}}} \times F_{SW} \tag{14}$$

For this design, switching losses are higher at low input voltage due to the lower gate drive current. Designing for 1 W of total losses in both MOSFETS and 20% of the total MOSFET losses in switching losses, we can estimate our maximum gate-to-drain charge for the design at:

$$Q_{GS2\_Q1} + Q_{GD\_Q1} < \frac{P_{G1SW}}{V_{IN} \times I_{OUT}} \times \frac{V_{DD} - V_t}{R_{DRIVE}} \times \frac{1}{F_{SW}} \tag{15}$$

For a low-gate threshold MOSFET, and the TPS40042's 5 Ω and 3 Ω drive resistances, we estimate a maximum Q_{GS2}+Q_{GD} of 10.8 nC.

The conduction losses in the upper switch MOSFET are estimated by the RMS current through the MOSFET times its $R_{DS(on)}$:

$$P_{CON\_Q1} = D \times \left[\left(I_{OUT}\right)^2 + \frac{1}{12}\left(I_{RIPPLE}\right)^2\right] \times R_{DS(on)} = \frac{V_{OUT}}{V_{IN}} \times {I_{L(rms)}}^2 \times R_{DS(on\_Q1)} \tag{16}$$

Estimating about 30% of total MOSFET losses to be high-side conduction losses, the maximum $R_{DS(on)}$ of the high-side MOSFET can be estimated by:

$$R_{DS(on\_Q1)} = \frac{P_{CON\_Q1}}{{I_{L(rms)}}^2 \times \frac{V_{OUT}}{V_{IN}}} \tag{17}$$

For this design, with I_{L_RMS} = 6 A_{RMS} and 4.5 V to 0.9 V, $R_{DS(on\_Q1)}$ is < 39 mΩ for the upper switch MOSFET.

Estimating 50% of total MOSFET losses are in the SR as conduction losses, repeat equation 14. Then calculate the maximum $R_{DS(on)}$ of the SR by the equation:

$$R_{DS(on\_Q2)} = \frac{P_{CON\_Q2}}{I_{L(rms)}^{2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (18)$$

For this design I_{L_RMS} = 6 A at 5.5 V to 0.9 V $R_{DS(on\_Q2)}$ < 15.9 mΩ. The table below summarizes the MOSFET requirements.

MOSFET Requirements

PARAMETER	SYMBOL	VALUE	UNITS
High-side FET $R_{DS(on)}$	$R_{DS(on\_Q1)}$	39	mΩ
High-side FET turn-on charge	Q_{GS2_Q1} +Q_{GD_Q1}	10.8	nC
Low-side FET $R_{DS(on)}$	$R_{DS(on\_Q2)}$	15.9	mΩ

IRF7910 has an $R_{DSON(max)}$ of **15 mΩ** at 4.5-V gate drive,Q_{GD} of 6.2 nC, and Q_{GS2} of 2 nC.

Bootstrap Capacitor (C7)

To ensure proper charging of the upper switch MOSFET gate, limit the ripple voltage on the bootstrap capacitor to < 5% of the minimum gate drive voltage of 3.0 V.

$$C_{BOOST} = \frac{20 \times Q_{GS\_Q1}}{V_{IN(min)}} \quad (19)$$

Based on the IRF7910 MOSFET with a maximum total gate charge of 26 nC, calculate a minimum of 116 nF of capacitance. The next higher standard value of 220 nF is selected.

VDD Bypass Capacitor (C6)

Select a 1.0-µF ceramic bypass capacitor for VDD.

VDD Filter Resistor (R7)

An optional resistor in series with VDD helps filter switching noise from the device. Driving the two IRF7910 MOSFETs, with a typical total Q_G of 17 nC each, we calculate a maximum I_{DD} current of 22 mA. The result of equation 19, leads to selecting a 1-Ω resistor, and limits the voltage drop across this resistor to less than 25 mV.

$$R_{VDD} < \frac{V_{RVDD(max)}}{I_{DD}} = \frac{25\ mV}{2\ mA + \left(Q_{G\_Q1} + Q_{G\_Q2}\right)F_{SW}} \quad (20)$$

Short Circuit Protection (R2)

The TPS40042 use the forward drop across the upper switch MOSFET during the ON time to measure the inductor current. The voltage drop across the high-side MOSFET is given by:

$$V_{CS} = I_{L(peak)} \times R_{DS(on\_Q1)} \quad (21)$$

When V_{IN} = 4.5 V to 5.5 V, I_{L_PEAK} = 7.2A. Using the IRF7910 MOSFET, we calculate the peak voltage drop to be 108 mV. The TPS40042's internal 3100-ppm temperature coefficient helps compensate for the MOSFET's $R_{DS(on)}$ temperature coefficient. For this design, select the short circuit protection voltage threshold of 180 mV by selecting R2 = OPEN.

REFIN Divider Resistors

In DDR2 applications, VTT=1/2 VDDQ. A 2:1 resistor divider with R11=R12 =100-kΩ provides V_{REFIN}. If a buffer is to be used to provide VTT_REF, the output of the buffer should be tied to V_{REFIN} on the TPS40042 to minimize offset from VTT_REF to VTT.

REFIN Bypass Capacitor

A capacitor from VTT_REF to GND removes VDDQ noise from the REFIN input. The capacitor is selected by Equation 22.

$$C11 = \left(\frac{\left(\left(\frac{1}{R11} \right) + \left(\frac{1}{R12} \right) \right)}{2\pi \times BW_{REFIN}} \right) \tag{22}$$

For a bandwidth of BW_{REFIN} = 30 kHz, C11 calculates to 106 pF, a 100-pF ceramic capacitor is used.

Feedback Loop Design

To design feedback circuit, a small signal average modeling technique is employed. Further information on this technique may be found in the references.

Modeling the Power Stage

The peak-to-peak ramp voltage given in the Electrical Specification table allows the modulator gain to be calculated as:

$$A_{MOD} = \frac{V_{IN}}{V_{RAMP(p-p)}} \tag{23}$$

For this design, a modulator gain of 7.3 (17.3 dB) is calculated.

The LC filter applies a double pole at the resonance frequency:

$$F_{RES} = \frac{1}{2 \times \pi \times \sqrt{L \times C}} \tag{24}$$

For this design, the resonance frequency is about 11.3 kHz. Below this frequency, the power stage has the dc gain of 17.3 dB and above this frequency the power stage gain drops off at -40 dB per decade. The ESR zero is approximated by:

$$F_{ESR} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{ESR}} \tag{25}$$

For C_{OUT} = 2 x 100 µF and R_{ESR} = 2.5 mΩ F_{ESR} = 318 kHz. This is greater than 1/5th the switching frequency and outside the scope of the error amplifier design. The gain of the power stage would change to -20 dB per decade above F_{ESR}. The straight line approximation the power stage gain is approximated in Figure 20.

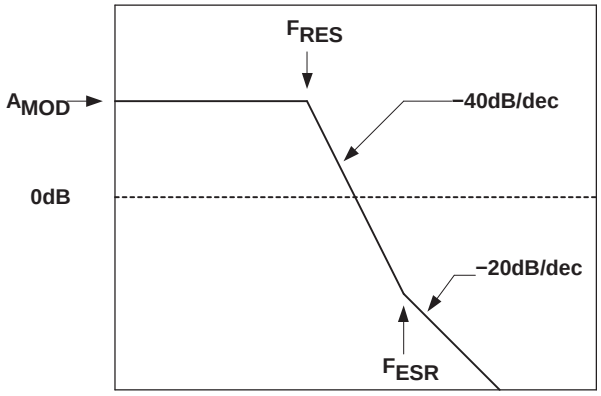


Figure 20. Power Stage Frequency Response Straight Line Approximation

Feedback Divider

Select R8 be between 10 kΩ and 100 kΩ. For this design, select 20 kΩ. While no feedback divider is needed for the VTT tracking output ($V_{OUT} = V_{REFIN}$) , R8 is necessary to provide input impedance to the error amplifier.

Error Amplifier Pole-Zero Selection

Place two zeros at about 80% of the resonance frequency to keep the actual resonance frequency above the two zeros over the L and C tolerance. For F_{RES} = 11.3 kHz, F_{Z1} = 9.0 kHz and F_{Z2} = 7 kHz. Selecting the cross-over frequency (F_{CO}) of the control loop between 3 times the LC filter resonance and 1/5th the switching frequency. For most applications 1/10th the switching frequency provides a good balance between ease of design and fast transient response.

If $F_{ESR} < F_{CO}$; F_{P1} = (1/2) F_{CO} and F_{P2} = 2x F_{CO}.

If $F_{ESR} > 2x\ F_{CO}$; $F_{P1} = F_{CO}$ and F_{P2} = 4x F_{CO}.

For this design with F_{SW} = 600 kHz, F_{RES} = 11.3 kHz and F_{ESR} = 318 kHz.

F_{CO} = 60 kHz and since $F_{ESR} > 2x\ F_{CO}$, $F_{P1} = F_{CO}$ and F_{P2} = 4x F_{CO}.

Since $F_{CO} < F_{ESR}$ the power stage gain at the desired cross-over can be approximated by:

$$A_{PS(fcc)} = A_{MOD} - 40 \times LOG\left(\frac{F_{CO}}{F_{RES}}\right) \quad (26)$$

$A_{PS}(F_{CO})$ = -11.7 dB, so the error amplifier gain between the two poles should be $10^{(11.7/20)}$ = 3.84.

If the error amplifier gain is greater than 0 dB at F_{SW}, the converter can achieve a stable bi-modal operation with duty cycles alternating between two stable values, and the output regulated with a output ripple component at (1/2) F_{SW}. To prevent this effect, check F_{P2} by the equation:

$$F_{P2(max)} = \frac{F_{SW}}{A_{MID(band)}} \quad (27)$$

Since $F_{P2} > F_{P2(max)}$, it is possible for this control loop to obtain bi-modal operation. To prevent this bi-modal operation, reduce F_{CO} and re-calculate $A_{PC}(F_{CO})$, F_{P1}, and $F_{P2(max)}$.

Now, F_{CO} = 40 kHz, $A_{MID\text{-}BAND}$ = 1.48, F_{P1} = 25 kHz and F_{P2} = 100 kHz.

The table below summarizes the error amplifier compensation network design criteria.

Error Amplifier Compensation Network

PARAMETER	SYMBOL	VALUE	UNITS
First zero frequency	F_{Z1}	9	kHz
Second zero frequency	F_{Z2}	9	
First pole frequency	F_{P1}	25	
Second pole frequency	F_{P2}	100	
Mid-band gain	$A_{MID\text{-}BAND}$	1.48	V/V

Feedback Components (R3, R6, C3, C4, C5)

Approximate C5 with the formula:

$$C5 = \frac{1}{2 \times \pi \times R8 \times F_{Z2}} \quad (28)$$

C5 = 1000 pF (closest standard capacitor value greater than the calculated 884 pF) and approximate R6 with the formula:

$$R6 = \frac{1}{2 \times \pi \times C5 \times F_{P1}} \quad (29)$$

R6 = 6.34 kΩ (closest standard resistor value to calculated 6.37 kΩ) Calculate R3 by the formula:

$$R3 = \frac{A_{MID(band)} \times (R6 \times R8)}{R6 + R8} \quad (30)$$

With A_{MID_BAND} = 1.48, R6 = 6.34 kΩ and R8 = 20 kΩ, R3 = 7.15 kΩ (closest standard resistor value to calculated 7.12 kΩ) Calculate C3 and C4 by the equations:

$$C4 = \frac{1}{2 \times \pi \times R3 \times F_{Z1}} \quad (31)$$

$$C3 = \frac{1}{2 \times \pi \times R3 \times F_{P2}} \quad (32)$$

For R3 = 7.15 kΩ, C3 = 220 pF (closest standard value to 222 pF) C4 = 2200 pF (closest standard value to 2473 pF)

Error Amplifier straight line approximation transfer function looks like Figure 21.

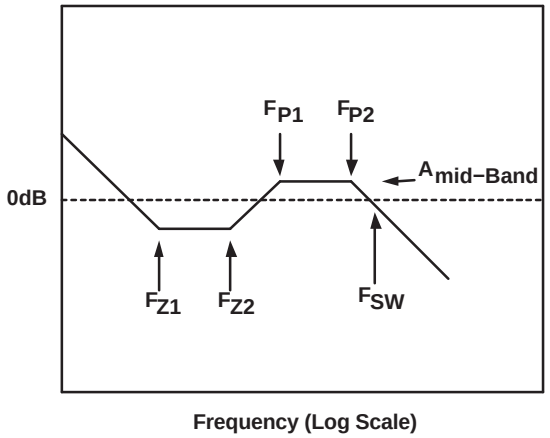


Figure 21. Error Amplifier Frequency Response Straight Line Approximation

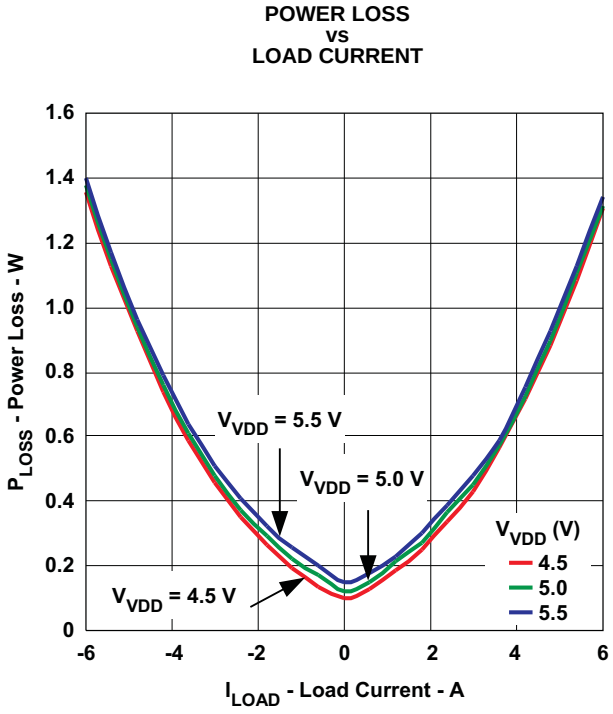


Figure 22.

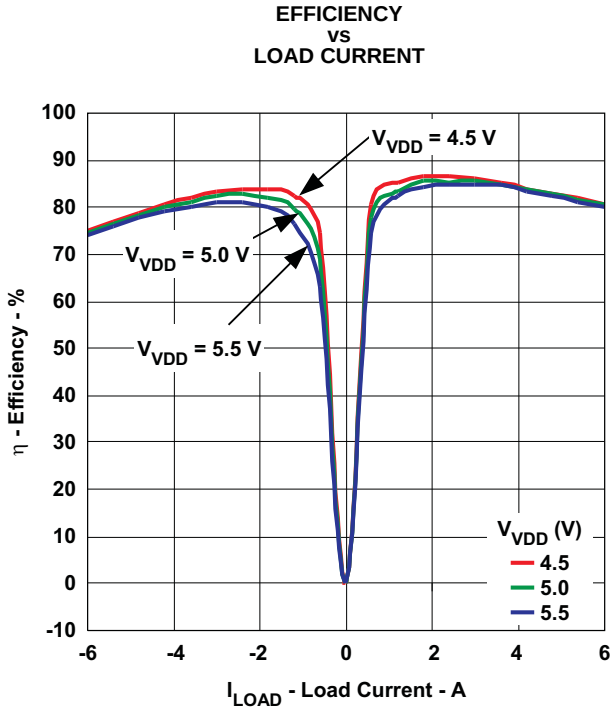


Figure 23.

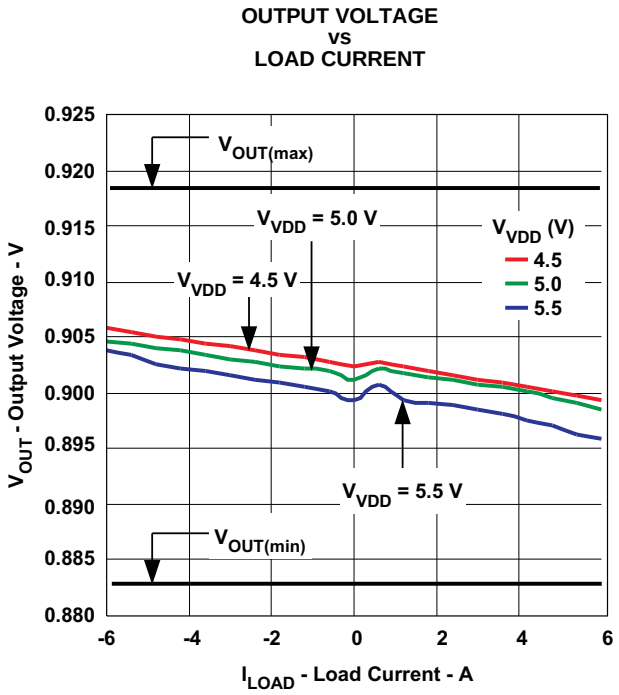

OUTPUT VOLTAGE
vs
LOAD CURRENT
0.925
0.920
0.915
0.910
0.905
0.900
0.895
0.890
0.885
0.880
VOUT(max)
VVDD = 5.0 V
VVDD = 4.5 V
VVDD = 5.5 V
VOUT(min)
VVDD (V)
4.5
5.0
5.5
VOUT - Output Voltage - V
-6
-4
-2
0
2
4
6
ILOAD - Load Current - A

Figure 24.

List of Materials

REF	QTY	DESCRIPTION	MFR	PART NUMBER
C1	2	Capacitor, ceramic, 6.3 V, X5R, 20%, 100 µF, 1210	TDK	C325X5R0J107M
C3	1	Capacitor, ceramic, 50 V, X7R, 20%, 220pF, 0402	TDK	C1005C01H221M
C4	1	Capacitor, ceramic, 50 V, X7R, 20%, 2200 pF, 0402	TDK	C1005X7R1H222M
C5	1	Capacitor, ceramic, 50 V, X7R, 20%, 1000 pF, 0402	TDK	C1005X7R1H102M
C6	1	Capacitor, ceramic, 6.3 V, X5R, 20%, 1.0 µF, 0402	TDK	C1005X7R0J105M
C7	1	Capacitor, ceramic, 6.3 V, X5R, 20%, 0.22 µF, 0402	TDK	C1005X7R0J224M
C8	2	Capacitor, ceramic, 6.3 V, X5R, 20%, 100 µF, 1210	TDK	C3225X5R0J107M
C10	1	Capacitor, ceramic, 6.3 V, X5R, 20%, 1.0 µF, 0402	TDK	C1005X7R0J105M
C11	1	Capacitor, ceramic, 50 V, X7R, 20%, 100pF, 0402	TDK	C1005C01H101M
L1	1	Inductor, SMT, 0.8 µH, 12 A, 6.6 mΩ, ED1514, 0.268 x 0.268	Pulse	PG0083.801
Q2	1	MOSFET, dual N-channel, 20 V, 6.6 A, 29 mΩ, 1.0 µH, SO8	IR	IRF7910
R3	1	Resistor, chip, 1/16 W, 1%, 7.15 kΩ, 0402	Std	Std
R6	1	Resistor, chip, k 1/1 W, 1%, 6.34 kΩ, 0402	Std	Std
R7	1	Resistor, chip, k, 1/16 W, 1%, 1.0 Ω, 0402	Std	Std
R8	1	Resistor, chip, k 1/16 W, 1%, 20 kΩ, 0402	Std	Std
R11	1	Resistor, chip, 100 kΩ, 1/16 W, 1%, 100 kΩ, 0402	Std	Std
R12	1	Resistor, chip, 100 kΩ, 1/16 W, 1%, 100 kΩ, 0402	Std	Std
U1	1	Device, Low Voltage DC to DC Synchronous Buck Controller, TPS40042DRC, SON-10P	TPS40042DRC	TI
Active High Enable Circuit				
R1	1	Resistor, chip, 100 kΩ, 1/16 W, 1%, 100 kΩ, 0402	Std	Std
Q1	1	Mosfet, N-channel, VDS 60 V, RDS 2 Ω, ID 115 mA, 2N7002W, SOT-323 (SC-70)	Diodes Inc	2N7002W-7

Definition of Symbols

SYMBOL	DESCRIPTION
$V_{IN(max)}$	Maximum operating input voltage
$V_{IN(min)}$	Minimum operating input voltage
$V_{INRIPPLE}$	Peak-to-peak ac ripple voltage on V_{IN}
V_{OUT}	Target output voltage
$V_{OUTRIPPLE}$	Peak-to-peak ac ripple voltage on V_{OUT}
$I_{OUT(max)}$	Maximum operating load current
I_{RIPPLE}	Peak-to-peak ripple current through the output filter inductor
I_{L_PEAK}	Peak ripple current through the output filter inductor
I_{L_RMS}	Root mean squared current through the output filter inductor
I_{RMS_CIN}	Root mean squared current in input capacitor
F_{SW}	Switching frequency
F_{CO}	Desired control loop cross-over frequency
A_{MOD}	Low frequency gain of the pulse width modulator
$V_{CONTROL}$	PWM control voltage (error amplifier output voltage - V_{COMP})
F_{RES}	L-C filter resonant frequency
F_{ESR}	Output capacitors' ESR zero frequency
F_{P1}	First pole frequency in error amplifier compensation
F_{P2}	Second pole frequency in error amplifier compensation
F_{Z1}	First zero frequency in error amplifier compensation
F_{Z2}	Second pole frequency in error amplifier compensation
Q_{G1_Q1}	Total gate charge of upper switch MOSFET
Q_{G2_Q2}	Total gate charge of synchronous rectifier MOSFET
$R_{DS(on\_Q1)}$	"ON" drain-to-source resistance of upper switch MOSFET
$R_{DS(on\_Q2)}$	"ON" drain-to-source resistance of synchronous rectifier MOSEFT
P_{CON_Q1}	Conduction losses in upper switch MOSFET
P_{SW_Q1}	Switching losses in upper switch MOSFET
P_{CON_Q2}	Conduction losses in synchronous rectifier MOSFET
Q_{GD_Q1}	Gate-to-drain charge of upper switch MOSFET
Q_{GS2_Q1}	Post threshold gate-to-source charge of the upper switch MOSFET. (Estimate from Q_G vs. V_{GS} if not provided in MOSFET data sheet)
V_{FB}	Internal reference voltage as measured on FB pin.
V_{RAMP_slope}	Slope of internal PWM ramp
$A_{PS(Fco)}$	V_{COMP} to V_{OUT} gain at desired loop cross-over frequency. (dB)
$A_{MID\text{-}BAND}$	V_{OUT} to V_{COMP} gain at desired loop cross-over frequency (V/V)
BW_{REFIN}	Desired frequency bandwidth of the REFIN input.

ADDITIONAL REFERENCES

Related Parts

The following parts have characteristics similar to the TPS40042 and may be of interest.

Related Parts

DEVICE	DESCRIPTION
TPS40007/9	Low Voltage Synchronous Buck Controller with Predictive Gate Drive®
TPS40021	Full Featured Low Voltage Synchronous Buck Controller with Predictive Gate Drive®
TPS40040/1	Low Voltage Synchronous Buck Controller

References

These references may be found on the web at www.power.ti.com under Technical Documents. Many design tools and links to additional references, including design software, may also be found at www.power.ti.com

1. *Under The Hood Of Low Voltage DC/DC Converters*, SEM1500 Topic 5, 2002 Seminar Series
2. *Understanding Buck Power Stages in Switchmode Power Supplies*, SLVA057, March 1999
3. *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, SEM 1400, 2001 Seminar Series
4. *Designing Stable Control Loops*, SEM 1400, 2001 Seminar Series
5. Additional PowerPAD™ information may be found in Applications Briefs SLMA002 and SLMA004
6. QFN/SON PCB Attachment, Texas Instruments Literature Number SLUA271, June 2002

Package Outline and Recommended PCB Footprint

The following pages outline the mechanical dimensions of the DRC package and provide recommendations for PCB layout footpring.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS40042DRCR	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0042
TPS40042DRCR.A	Active	Production	VSON (DRC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0042
TPS40042DRCT	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0042
TPS40042DRCT.A	Active	Production	VSON (DRC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	0042

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

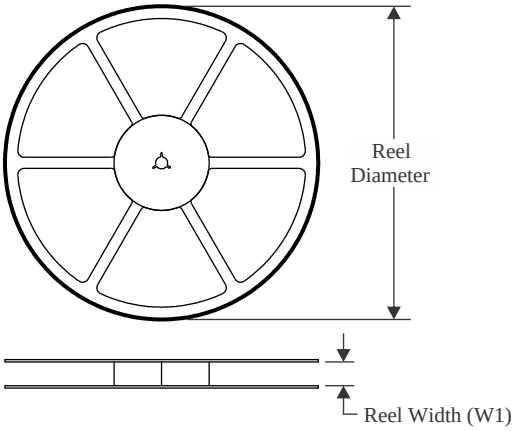
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

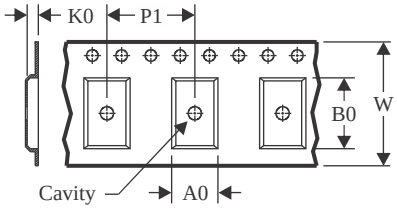
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

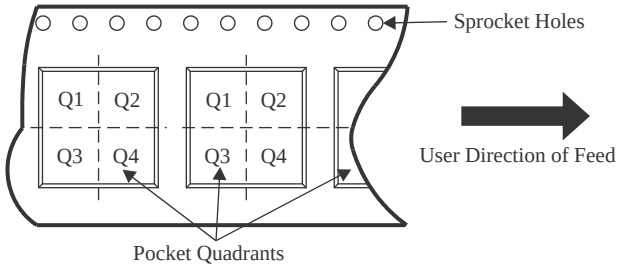


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

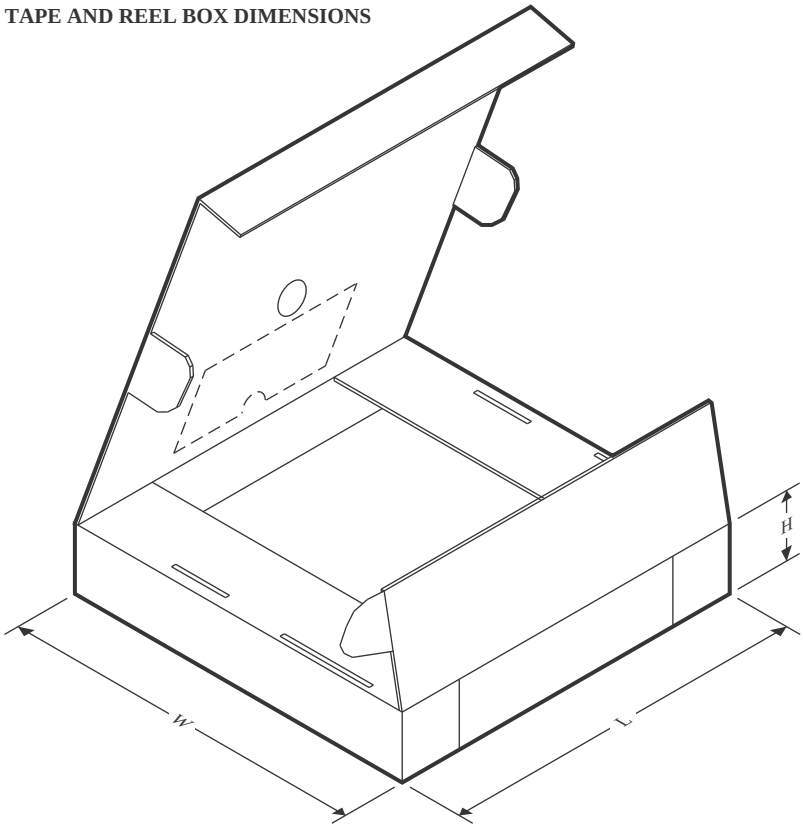
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40042DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS40042DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40042DRCR	VSON	DRC	10	3000	353.0	353.0	32.0
TPS40042DRCT	VSON	DRC	10	250	213.0	191.0	35.0

GENERIC PACKAGE VIEW

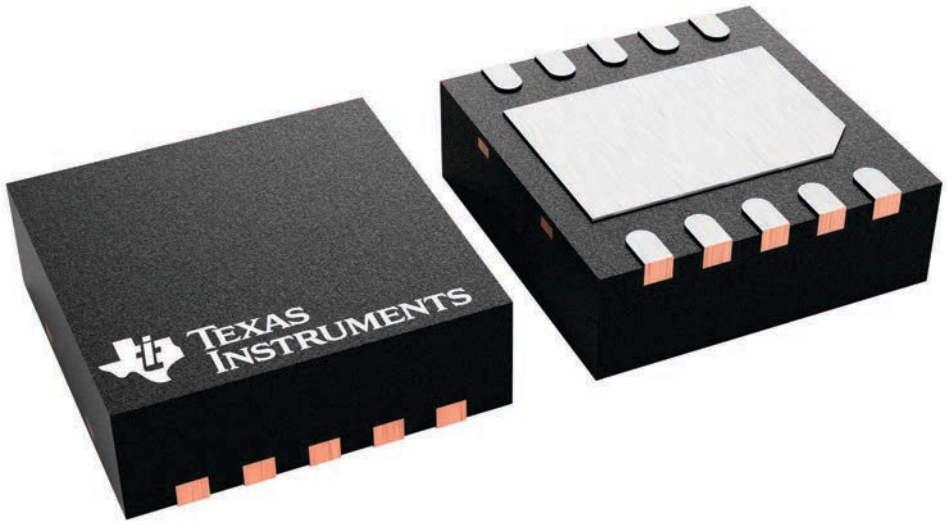
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



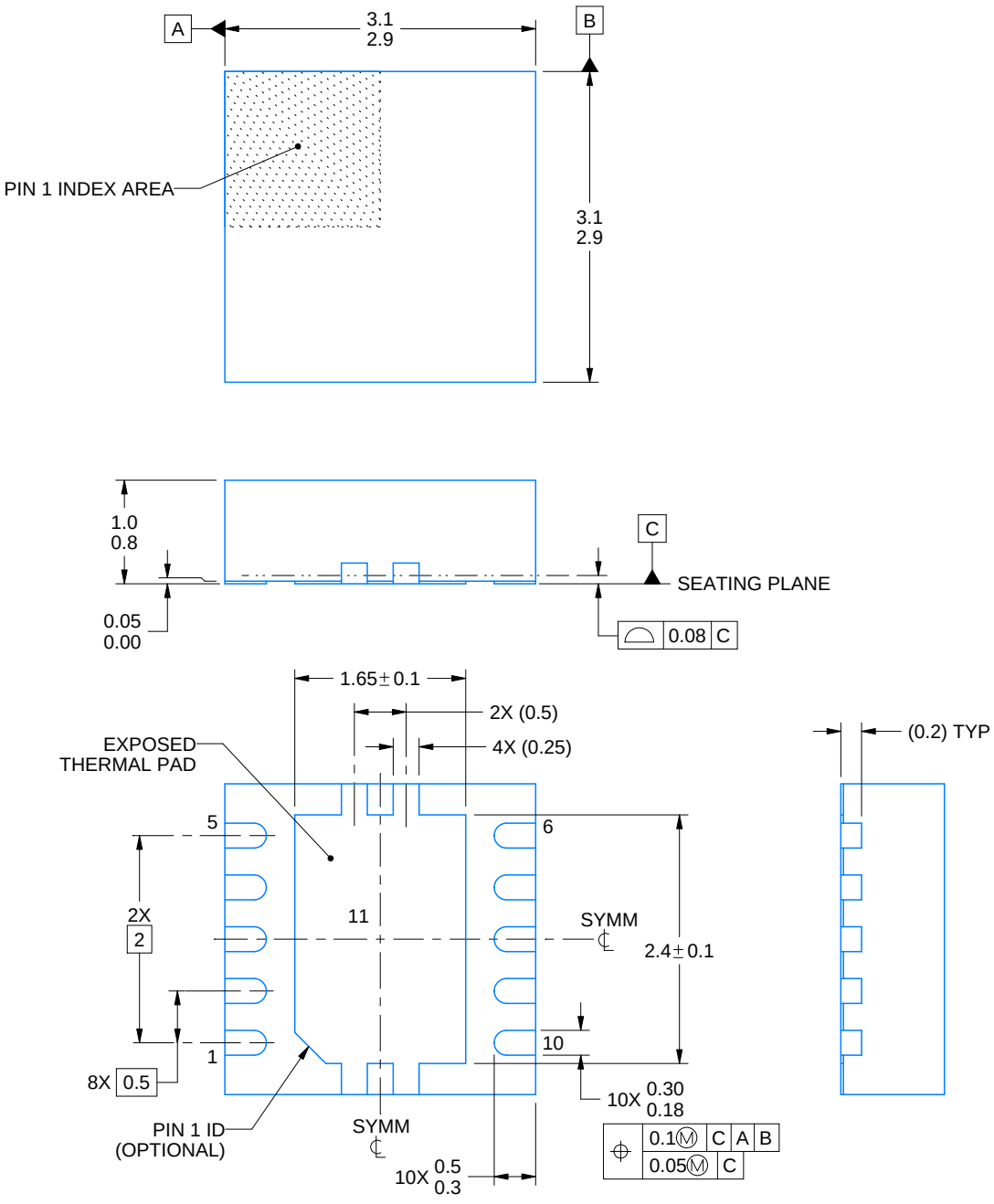
4226193/A

DRC0010J

PACKAGE OUTLINE

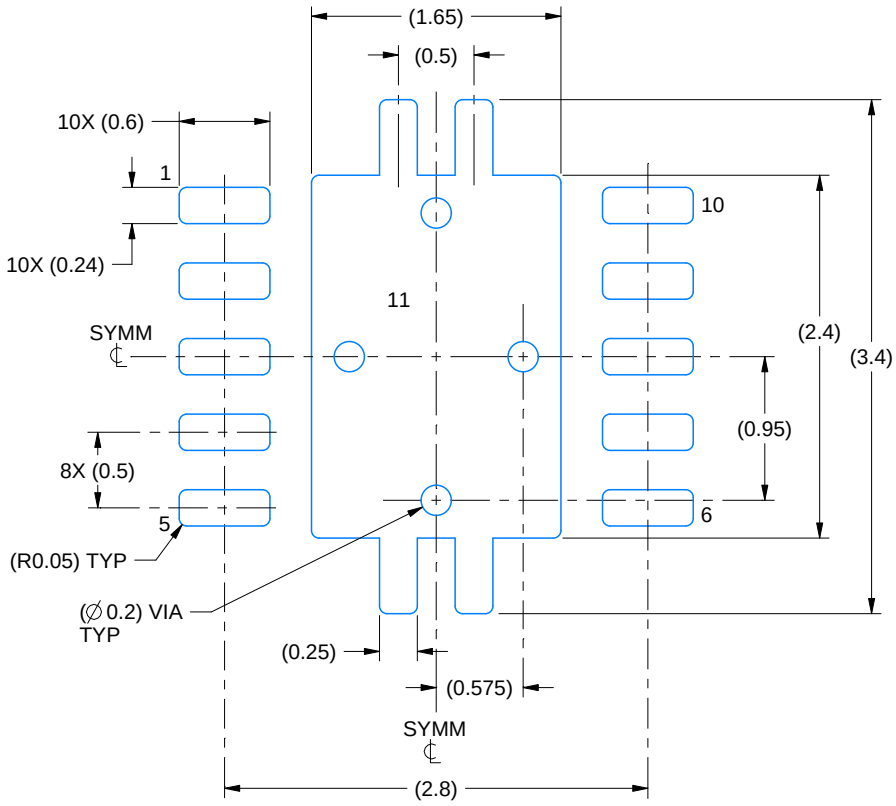
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

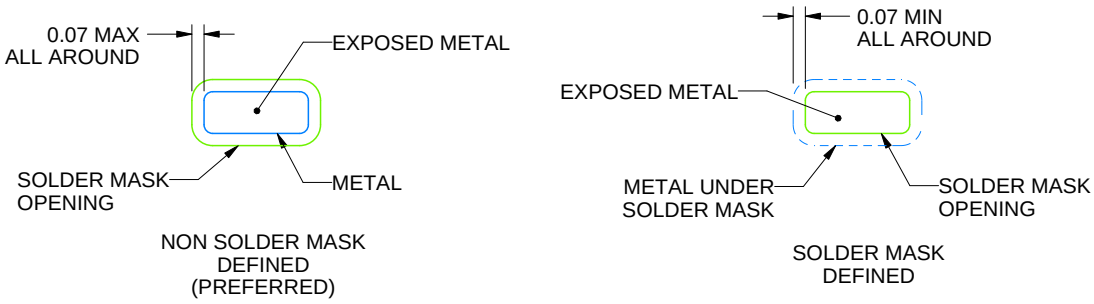


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

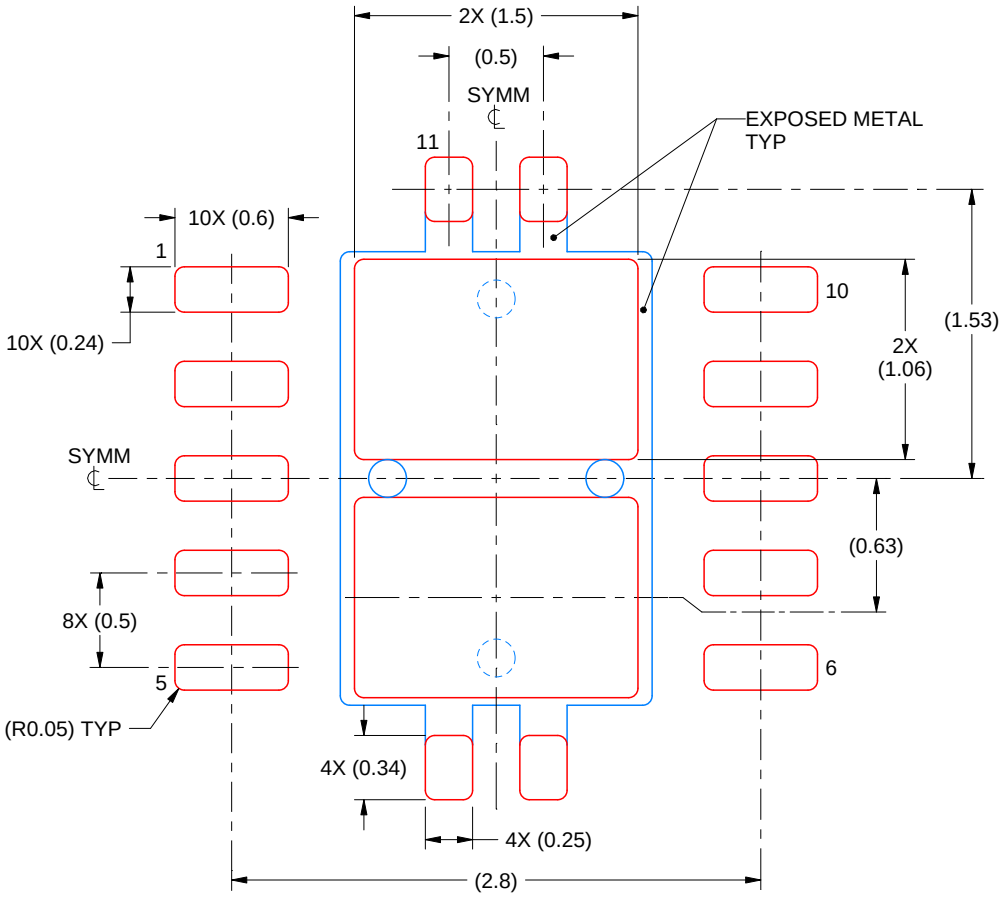
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025