3 V 至 20 V PMBUS 同步降压控制器

查询样品: TPS40400

特性

- 输入工作电压范围：**3 V** 至 **20 V**
- 支持 **PMBus** 功能的模拟控制器
- 参考电压 **600 mV ± 1%**
- 远程电压感测放大器
- 内部 **6 V** 稳压器与 **6 V** 栅极驱动器
- 可编程过流保护
- 电感器电阻或串行电阻适用于电流感测
- 可编程开关频率：**200 kHz** 至 **2 MHz**
- 电源良好指示器
- 热关断
- 可编程软启动
- 内部引导二极管
- 预偏置输出安全
- **24** 引脚 **QFN** 封装

应用范围

- 智能电源系统
- 电源模块
- 通信设备
- 计算机设备

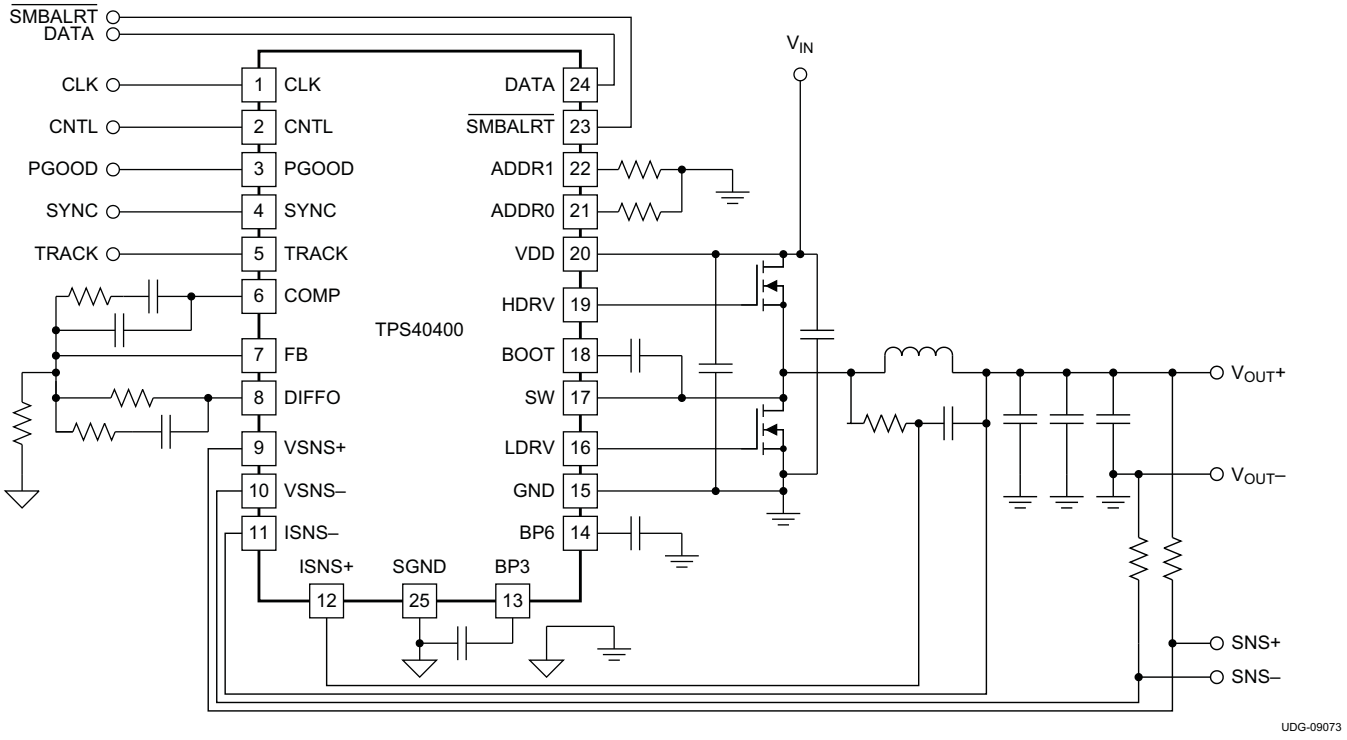
说明

TPS40400是一款成本优化的灵活同步降压控制器, 采用 3.0 V 至 20 V 额定电源供电。该控制器是一款模拟 PWM 控制器，可通过 PMBus 接口进行编程和监控。该器件的高灵活特性包括可编程软启动时间、可编程短路限制以及可编程欠压锁定 (UVLO) 等。 该控制器是一款模拟 PWM 控制器，可通过 PMBus 接口进行编程和监控。 该器件的高灵活特性包括可编程软启动时间、可编程短路限制以及可编程欠压锁定 (UVLO) 等。

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
SwitcherPro is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

版权 © 2011, Texas Instruments Incorporated



版权 © 2011, Texas Instruments Incorporated

说明（继续）

自适应反交叉传导方案可用于避免功率 FET 出现直通电流。 栅极驱动电压为 6 V，可改进功率 FET，减少损失。 通过感应电感器上或与电感器串联电阻器上的压降，可检测短路情况。 PMBus 可编程阈值与该电压相比较，可检测过流。 在达到过流阈值时，则可采用逐脉冲电流限制方案将电流降至可接受的水平。 如果过流情况持续超过转换器的 7 个时钟周期，则宣布故障条件，转换器将关闭并进入短中断重启模式或锁存。 该行为可通过 PMBus 接口选择。 其它 PMBus 接口特性还包括可编程工作频率、软起动时间、过压及欠压阈值、对有关事件的响应，以及包括边缘效应和状态监测在内的输出电压改变等。

ORDERING INFORMATION(1)(2)

PACKAGE	PINS	TAPE AND REEL QTY.	ORDERABLE NUMBER
Plastic QFN (RHL)	24	250	TPS40400RHLT
		3000	TPS40400RHLR

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

		VALUE		
		MIN	MAX	UNIT
Input voltage range	VDD	–0.3	22	V
	SW	–5	27	
	BOOT	–0.3	30	
	BOOT-SW, HDRV-SW (Differential from BOOT or HDRV to SW)	–0.3	7	
	VSNS+, TRACK, SYNC, FB	–0.3	7	
	DATA, CLK, CNTL	–0.3	3.6	
	ISNS+, ISNS–	–0.3	15	
	VSNS–	–0.3	0.3	
Output voltage range	HDRV	–0.3	30	V
	BP3	–0.3	3.8	
	BP6, COMP, PGOOD, DIFFO, LDRV	–0.3	7	
	$\overline{\text{SMBALRT}}$, ADDR0	–0.3	3.6	
T_J Operating junction temperature range		–40	150	°C
T_{STG} Storage temperature range		–55	150	°C

PACKAGE DISSIPATION RATINGS(1)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT (°C/W)	AIRFLOW	T_A = 25°C POWER RATING (W)	T_A = 85°C POWER RATING (W)
24-Pin Plastic QFN (RHL)	31.1	Natural Convection	3.21	1.29
	25.2	200 LFM	3.96	1.58
	23	400 LFM	4.36	1.74

(1) Ratings based on JEDEC High Thermal Conductivity (High K) Board. For more information on the test method, see TI Technical Brief SZZA017.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
VDD	Input operating voltage	3.0		20	V
T_J	Operating junction temperature	–40		125	°C

Copyright © 2011, Texas Instruments Incorporated

ELECTROSTATIC DISCHARGE PROTECTION

	MIN	TYP	MAX	UNIT
Human Body Model (HBM)		2500		V
Charged Device Model (CDM)		1500		V

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for –40°C ≤ T_J ≤ 125°C, V_{DD}= 12 Vdc, FREQUENCY_SWITCH = 600 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VDD}	Input voltage range		3		20	V
I_{VDD}	Input operating current	Switching, no driver load		6	15	mA
VOLTAGE REFERENCE						
V_{FB}	Feedback pin voltage default settings	-40ºC ≤ T_J ≤ 125ºC	594	600	606	mV
$V_{FB(max)}$	Feedback pin voltage maximum adjustment			750		mV
$V_{FB(min)}$	Feedback pin voltage minimum adjustment			450		mV
$V_{FB(inc)}$	Feedback pin voltage adjustment resolution			2.34		mV
$V_{FB(NL)}$	Maximum nonlinearity error over adjustment range				10	mV
BP6 REGULATOR						
V_{BP6}	6-V regulator output voltage		6.2	6.5	6.8	V
V_{DO6}	Regulator dropout voltage, (V_{VDD} – V_{BP6})	V_{VDD} = 6 V, I_{BP6} = 50 mA			300	mV
I_{BP6}	Regulator current limit		100			mA
BP3 REGULATOR						
V_{BP3}	3.3-V regulator output voltage		3.1	3.3	3.5	V
V_{DO3}	Regulator dropout voltage, (V_{VDD} – V_{BP3})	V_{VDD} = 3V, I_{BP3} = 5 mA		100	200	mV
OSCILLATOR						
f_{SW}	Switching frequency	Factory default setting	480	600	720	kHz
	Nominal frequency range		200		2000	
	Accuracy	3 V ≤ V_{VDD} ≤ 20 V, 200 kHz ≤ f_{SW} ≤ 2 MHz	–20%		20%	
V_{IH}	SYNC high-level input voltage		2.0			V
V_{IL}	SYNC low-level input voltage				0.4	
I_{SYNC}	SYNC pin leakage current	V_{SYNC} = 6 V			100	nA
		V_{SYNC} = 0 V			100	
t_{SRISE}	Maximum SYNC rise time(1)		100			ns
t_{SYNC}	Minimum SYNC pulse width		100			ns
V_{RMP}	Ramp amplitude(1)	FREQUENCY_SWITCH = 200 kHz	V_{VDD}/6.6	V_{VDD}/6.5	V_{VDD}/6.3	V
		FREQUENCY_SWITCH = 600 kHz	V_{VDD}/7.0	V_{VDD}/6.8	V_{VDD}/6.6	
		FREQUENCY_SWITCH = 2000 kHz	V_{VDD}/10	V_{VDD}/9.6	V_{VDD}/9.2	
V_{VLY}	Valley voltage(1)			0.9		
f_{SYNC}	SYNC range % of nominal oscillator frequency	200 kHz ≤ f_{SW} ≤ 2 MHz	85%		150%	
PULSE WIDTH MODULATOR (PWM)						
D_{MAX}	Maximum duty cycle(1) (2)	FREQUENCY_SWITCH = 600 kHz	90%			
		FREQUENCY_SWITCH = 1.2 MHz	85%			
		FREQUENCY_SWITCH = 2 MHz	75%			
$t_{OFF(min)}$	Minimum OFF time			170	225	ns
$t_{ON(min)}$	Minimum controllable pulse(1)	T_J = 25°C, f_{SW} = 600 kHz			75	ns

(1) Ensured by design. Not production tested.
(2) Operation at 3 V reduces maximum duty cycle by approximately 5%.

Copyright © 2011, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these specifications apply for –40°C ≤ T_J ≤ 125°C, V_{DD}= 12 Vdc, FREQUENCY_SWITCH = 600 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT-START						
t_{SS}	Soft-start time (3)	Factory default setting	2.7	3.1	3.5	ms
	Accuracy	600 µs ≤ t_{SS} ≤ 9 ms	–15%		15%	
ERROR AMPLIFIER						
GBWP	Gain bandwidth product(4)		15	20		MHz
A_{OL}	DC gain(4)		60			dB
I_{IBFB}	Input bias current: FB (out of pin)		0		100	nA
I_{IBT}	Input bias current: TRACK (out of pin)		0		250	nA
I_{EAOP}	Output source current	V_{FB} = 0 V, V_{COMP} ≥ 2 V	1			mA
I_{EAOM}	Output sink current	V_{FB} = 2 V, V_{COMP} ≤ 0.3 V	1			
V_{COMPH}	Error amplifier high output voltage	V_{FB} = 0 V	3.8			V
V_{COMPL}	Error amplifier low output voltage	V_{FB} = 2 V			50	mV
$V_{TRACK(ofst)}$	TRACK pin offset voltage		–5		+5	mV
CURRENT SENSE AMPLIFIER						
I_{ISNS+}	ISNS+ bias current				200	nA
$I_{ISNS–}$	ISNS– bias current				100	µA
V_{ICM}	Input common mode range		0.45		15	V
AO_{CM}	Common mode gain				–80	dB
V_{LIN}	Input linear range, VISNS+ - VISNS-(5)		–45		110	mV
CURRENT LIMIT PROTECTION						
t_{OFF}	Off time between restart attempts			6 × t_{SS}		ms
V_{ILIMTH}	V_{CS+} – $V_{CS–}$ voltage that trips OC fault function	Factory default settings(5), T_J = 25°C	27	30	33	mV
	Threshold accuracy	3 V ≤ V_{VDD} ≤ 20 V, 30 mV ≤ V_{ILIMTH} ≤ 110 mV, T_J = 25°C	–10%		10%	
		3V ≤ V_{VDD} ≤ 20 V, V_{ILIMTH} ≤ 30 mV, T_J = 25°C	–3		3	mV
	Comparator offset	V_{ILIMTH} = 30 mV, T_J = 25°C	–3		3	mV
	Temperature coefficient(4)			4000		ppm/°C
t_{DLYOC}	Overcurrent delay	3-mV overdrive, T_J = 25°C		155		ns
V_{ILIMW}	V_{CS+} – $V_{CS–}$ voltage that sets warning status	Factory default settings, T_J = 25°C	12	15	18	mV
	Threshold accuracy	3 V ≤ V_{VDD} ≤ 20V, 1.9 mV ≤ V_{ILIMTH} ≤ 120 mV, T_J = 25°C	–10%		10%	
		3V ≤ V_{VDD} ≤ 20 V, V_{ILIMTH} < 30 mV, T_J = 25°C	–3		3	mV
	Comparator offset	V_{ILIMTH} = 20 mV, T_J = 25°C	–3		3	mV
	Temperature coefficient(4)			4000		ppm/°C
t_{DLYOCW}	Overcurrent warning delay(4)	3-mV overdrive		250		ns

(3) See applications section for more information regarding soft-start time setting.
(4) Ensured by design. Not production tested.
(5) The entire current ripple waveform must reside inside the linear range for current reading results to be accurate. DC current level must be zero or greater for accurate results. Current sense does not support applications that sink current. Transient voltages (such as ripple) are permitted to go below 0 V, but must be within the specified linear range.

Copyright © 2011, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these specifications apply for –40°C ≤ T_J ≤ 125°C, V_{DD}= 12 Vdc, FREQUENCY_SWITCH = 600 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVERS						
R_{HDHI}	High-side driver pull up resistance	(V_{BOOT} – V_{SW}) = 6.4 V, I_{HDRV} = –100 , T_J = 25°C		1.25	2.5	Ω
R_{HDLO}	High-side driver pull down resistance	(V_{BOOT} – V_{SW}) = 6.4 V, I_{HDRV} = 100 mA, T_J = 25°C		1.3	2.6	Ω
R_{LDHI}	Low-side driver pull up resistance	T_J = 25°C		1.25	2.5	Ω
R_{LDLO}	Low-side driver pull down resistance	T_J = 25°C		0.8	1.5	Ω
t_{HRISE}	High-side driver rise time (6)	C_{LOAD} = 2.2 nF		6	12.1	ns
t_{HFALL}	High-side driver fall time (6)			6.3	12.6	ns
t_{LRISE}	Low-side driver rise time (6)			6	12.1	ns
t_{LFALL}	Low-side driver fall time (6)			4	8	ns
t_{DT}	Anti-cross conduction time	MFR_SPECIFIC_00 bit 0 = 0, (short dead time.)	20		50	ns
I_{SW}	SW pin leakage current (out of pin)	V_{SW} = 0 V			1	µA
BOOTSTRAP						
V_{BOOT}	Internal diode voltage drop	I_{BOOT} = 5 mA		0.7	1	V
$I_{BOOT(lk)}$	BOOT diode leakage current(6)	(V_{BOOT} – V_{SW}) = 6 V		1		µA
UVLO						
$V_{UVLO(on)}$	VDD UVLO turn on threshold(7)	Factory default settings (minimum)	2.475	2.750	3.025	V
	Accuracy(7)	2.25 V ≤ V_{VDD} ≤ 20 V, 2.75 V ≤ VIN_ON ≤ 18 V	–10%		10%	V
$V_{UVLO(off)}$	VDD UVLO turn off threshold(7)	Factory default settings (minimum)	2.25	2.5	2.75	V
	Accuracy(7)	2.25 V < V_{VDD} < 20 V, 2.75 V < VIN_OFF < 17.6 V	–10%		10%	V
REMOTE VOLTAGE SENSE AMPLIFIER						
V_{IOFST}	Input offset voltage		–10		10	mV
R_{GAIN}	Gain setting resistor(6)		48	60	72	kΩ
V_{DIFFO}	Output voltage at DIFFO pin	V_{VDD} > 6.5 V	0		6	V
		V_{VDD} = 5 V	0		4.5	V
		V_{VDD} = 3 V	0		2.5	V
K_{DIFF}	Differential gain of amplifier		0.995	1.000	1.005	V/V
V_{AGBWP}	Closed loop bandwidth(6)		2			MHz
I_{VAOP}	Output source current	V_{SNS+} = V_{DIFFO} = 5 V, $V_{SNS–}$ = 0 V	1			mA
I_{VAOM}	Output sink current	V_{SNS+} = 0 V, $V_{SNS–}$ = 4.5 V, V_{DIFFO} = 5 V	1			mA
POWERGOOD						
V_{PGON}	FB pin voltage upper limit for power good on	Factory default settings		648		mV
	FB pin voltage lower limit for power good on			552		mV
	Accuracy	540 mV < V_{PGON} < 660 mV	–5%		5%	
V_{PGOFF}	FB pin voltage upper limit for power good off	Factory default settings		660		mV
	FB pin voltage lower limit for power good off			540		mV
	Accuracy	528 mV < V_{PGOFF} < 672 mV	–5%		5%	
R_{PGD}	Pull down resistance of PGD pin	V_{FB} = 0, I_{PGOOD} = 5 mA			50	Ω
I_{PGDLK}	Leakage current	Factory default settings , 550 mV < V_{FB} < 650 mV, V_{PGOOD} = 5 V	3		15	µA
t_{PGD}	Delay filter from FB(6)			5		µs

(6) Ensured by design. Not production tested.
(7) Although specifications appear to overlap, hysteresis is assured for UVLO turn on and turn off thresholds.

Copyright © 2011, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these specifications apply for –40°C ≤ T_J ≤ 125°C, V_{DD}= 12 Vdc, FREQUENCY_SWITCH = 600 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE MARGINING						
MRG_{SLP}	VFB slope during margin voltage transition (8)	Factory default settings	250	214	188	V/s
	Accuracy	3 V < V_{VDD} < 20 V, 600 µs < t_{SS} < 9 ms	–15%		15%	
V_{FBMH}	FB pin voltage after margin high command	Factory default settings	650	660	670	mV
V_{FBML}	FB pin voltage after margin low command	Factory default settings	532	540	548	mV
$V_{FBM(max)}$	Maximum FB pin voltage with Margin	–40°C < T_J < 125°C	742	750	758	mV
$V_{FBM(min)}$	Minimum FB pin voltage with Margin	–40°C < T_J < 125°C	445	450	455	mV
$V_{FB(inc)}$	Resolution of FB steps with margin			2.34		mV
OVERVOLTAGE AND UNDERVOLTAGE DETECTION						
V_{OV}	FB pin overvoltage threshold (OV flag)	Factory default settings	638	672	705	mV
	Accuracy	3 V < V_{VDD} < 20 V, 648 mV < V_{OV} < 690 mV	–5%		5%	
V_{UV}	FB pin undervoltage threshold (UV flag)	Factory default settings	502	528	554	mV
	Accuracy	3 V < V_{VDD} < 20 V, 510 mV < V_{OV} < 552 mV	–5%		5%	
PMBus INTERFACE						
V_{IH}	High-level input voltage, CLK, DATA, CNTL		2.1			V
V_{IL}	Low-level input voltage, CLK, DATA, CNTL				0.8	V
I_{IH}	High-level input current, CLK, DATA, CNTL		–10		10	µA
	CNTL		–12		10	
I_{IL}	Low-level input current, CLK, DATA, CNTL		–10		10	µA
	CNTL		–12		10	
V_{OL}	Low-level output voltage, DATA, $\overline{SMBALRT}$	3.0 V ≤ V_{VDD} ≤ 20 V, I_{OUT} = 2 mA			0.4	V
I_{OH}	High-level open drain leakage current, DATA, $\overline{SMBALRT}$	V_{OUT} = 3.6 V	0		10	µA
C_O (8)	Pin capacitance, CLK, DATA			0.7		pF
f_{PMB}	PMBus operating frequency range	Slave mode	10		400	kHz
t_{BUF}	Bus free time between START and STOP(8)		4.7			µs
$t_{HD:STA}$	Hold time after repeated START(8)		4.0			µs
$t_{SU:STA}$	Repeated START setup time(8)		4.7			µs
$t_{SU:STO}$	STOP setup time(8)		4.0			µs
$t_{HD:DAT}$	Data hold time(8)	Receive mode	0			ns
		Transmit mode	300			
$t_{SU:DAT}$	Data setup time(8)		250			ns
$t_{TIMEOUT}$	Error signal/detect(8)		25		35	µs
$t_{LOW:MEXT}$	Cumulative clock low master extend time(8)				50	µs
$t_{LOW:SEXT}$	Cumulative clock low slave extend time(8)				25	µs
t_{LOW}	Clock low time(8)		4.7			µs
t_{HIGH}	Clock high time(8)		4.0			µs
t_{FALL}	CLK/DATA fall time(8)				300	ns
t_{RISE}	CLK/DATA rise time(8)				1000	ns
PMBus ADDRESSING						
I_{ADD}	ADDX pin current		8.23	9.75	11.21	µA
$V_{ADD(L)}$	Address pin illegal low voltage threshold				0.055	V

(8) Ensured by design. Not production tested.

Copyright © 2011, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

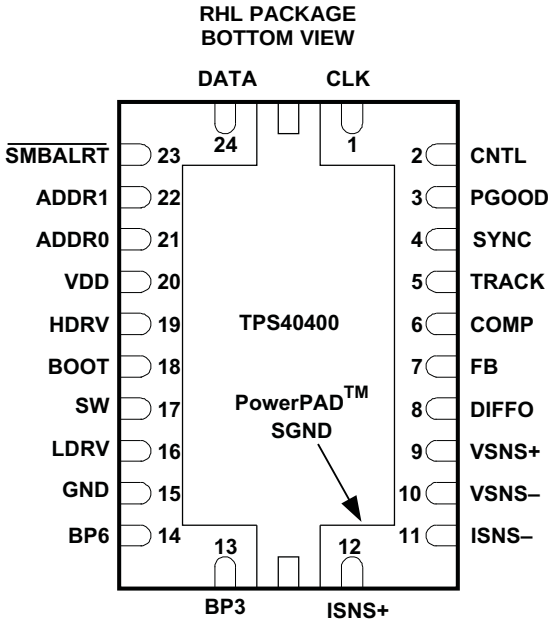
Unless otherwise stated, these specifications apply for –40°C ≤ T_J ≤ 125°C, V_{DD}= 12 Vdc, FREQUENCY_SWITCH = 600 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MEASUREMENT SYSTEM						
t_{IDLY}	Read delay time (9)		153	192	231	µs
I_{RES}	Current measurement resolution (LSB) (10) (11)			122		µV
I_{RNG}	Current measurement range(11) (12)		–45		110	mV
I_{ACC}	Gain accuracy(13)		–3%		3%	
I_{OFST}	Offset		–3		3	mV
$V_{OUT(res)}$	VOUT measurement resolution (LSB)			15.625		mV
$V_{OUT(rng)}$	VOUT voltage measurement range		0		14	V
$V_{OUT(gain)}$	Gain accuracy(13)(14)		–2		2	LSB
$V_{OUT(gain_adj)}$	Gain adjustment range through PMBus		–10%		10%	
$V_{OUT(ofst)}$	Offset(13)(14)		–3%		3%	
$V_{OUT(ofst_adj)}$	Gain adjustment range through PMBus		–125		124	mV
$V_{IN(res)}$	V_{IN} measurement resolution			32.5		mV
$V_{IN(rng)}$	V_{IN} voltage measurement range		3.0		20	V
$V_{IN(gain)}$	Gain accuracy(13)(14)		–2%		2%	
$V_{IN(gain_adj)}$	Gain adjustment range through PMBus		–10%		10%	
$V_{IN(offst)}$	Offset(13)(14)		–5.5	–2	1.4	LSB
$V_{IN(offst_adj)}$	Offset adjustment range through PMBus		–2		1.968	V
THERMAL SHUTDOWN						
T_{JSD}	Junction OT shutdown temperature(14)		135	145	155	°C
T_{JSDH}	Shutdown hysteresis(14)		25	30	35	°C
T_{JWRN}	Junction OT warning threshold(14)		120	130	140	°C
T_{JWRNH}	Junction OT warning temperature hysteresis(14)		15	20	25	°C

(9) All read backs are an average of 16 consecutive measurements – not a rolling average. Time is a delay between parameter updates.
(10) Constrained by the resolution of READ_IOUT command. This presents as the greater of 122 µV/ IOUT_CAL_GAIN or 62.5 mA, the resolution of the READ_IOUT command
(11) Voltage is converted to current by dividing by IOUT_CAL_GAIN, the effective value of the resistance used to sense current in the application. Maximum amount that can be reported via PMBus is 64A.
(12) Current reading is only supported to 0 average. Voltage transients to –45mV are taken into account when computing this average.
(13) PMBus commands provide for calibration of each device on an individual basis for improved overall system accuracy.
(14) Ensured by design. Not production tested.

Copyright © 2011, Texas Instruments Incorporated

DEVICE INFORMATION



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
ADDR0	21	I	Low-order address pin for PMBus address configuration. One of eight resistor values must be connected from this pin to SGND to select the low-order octal digit in the PMBus address.
ADDR1	22	I	High-order address pin for PMBus address configuration. One of eight resistor values must be connected from this pin to SGND to select the high-order octal digit in the PMBus address.
BOOT	18	I	Gate drive voltage for the high-side N-channel MOSFET. A capacitor 100 nF typical must be connected between this pin and SW.
BP3	13	O	Bypass pin for the internal regulator that supplies power to the internal controls of the device. Normal regulation voltage is 3.3 V. Connect a 100 nF or larger capacitor from this pin to GND.
BP6	14	O	Bypass pin for the internal regulator that supplies power to the gate drivers. Normal regulation voltage is 6.5 V. Connect a 1-µF or larger capacitor from this pin to GND.
CLK	1	I	Clock input for the PMBus interface
CNTL	2	I	Logic level input that controls the startup and shutdown of the converter, Exact functionality is determined by PMBus options.
COMP	6	O	Output of the error amplifier. Used for control loop compensation.
DATA	24	I/O	Data I/O for the PMBus interface
DIFFO	8	O	Output of the unity gain remote voltage sense amplifier. Typically connected to the voltage divider on FB
FB	7	I	Inverting input to the error amplifier. A voltage divider is connected here to sense the output voltage.
GND	15	–	Common connection for the device. This pin should connect to the thermal pad under the device package and to the power stage ground, preferably close to the source of the Low-side or rectifier FET. Connections should be arranged so that no power level current slow across the pad connected to the thermal pad on the underside of the device.
HDRV	19	O	Gate drive signal to the high-side FET
ISNS–	11	I	Inverting input to the current sense amplifier
ISNS+	12	I	Non-inverting input to the current sense amplifier
LDRV	16	O	Output used to drive the gate of the low-side or rectifier FET.
PGOOD	3	O	Power good output. This is an open drain output that pulls low when any fault condition exists within the device or when the device is not operating within a user selectable operating range of the nominal output voltage of the converter.

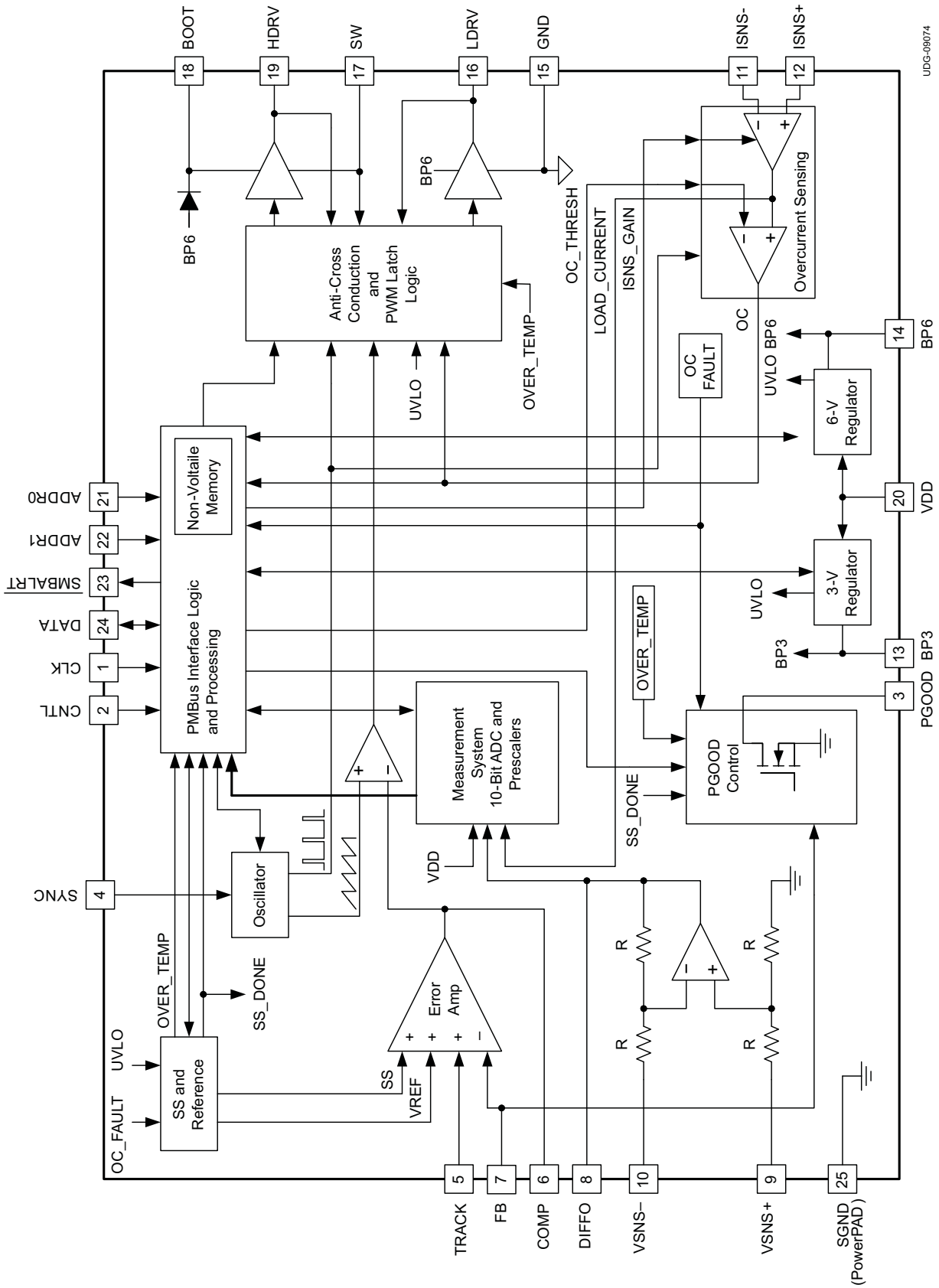
Copyright © 2011, Texas Instruments Incorporated

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SGND	PAD	-	Signal ground for the controller. Connect the ground of signal level circuits to this pin. Connections should be arranged so that power level currents do not flow in the pad attached to the thermal plane or in the SGND portion of the circuit.
$\overline{\text{SMBALRT}}$	23	O	Output used to signal that PMBus host that the controller needs attention.
SW	17	I	This is the common connection for the flying high-side FET driver and also serve as a sense line for the adaptive anti-cross-conduction circuitry
SYNC	4	I	Logic level input to the oscillator inside the controller. The oscillator resets on the rising edge of a pulse train applied to this pin and begin a new switching cycle.
TRACK	5	I	Analog input to the non inverting side of the control loop error amplifier. The error amplifier has three inputs (voltage reference, TRACK and soft-start ramp) to it's "+" side, and the lowest voltage applied to these three inputs dominate and control the output voltage of the whole converter. This pin is to allow the user to configure a voltage divider that allows the controller output follow an external reference voltage during startup.
VDD	20	I	Input power connection for the device. 3.0 V to 20 V required.
VSNS+	9	I	Non-inverting input to the unity gain remote voltage sense amplifier.
VSNS–	10	I	Inverting input to the unity gain remote voltage sense amplifier.

Copyright © 2011, Texas Instruments Incorporated

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

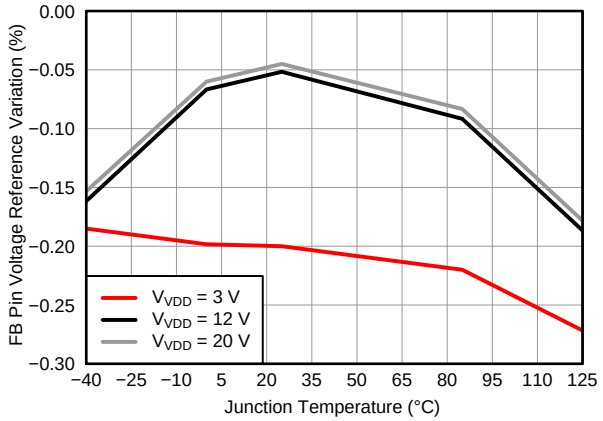


Figure 1. FB Pin Voltage Reference Variation vs. Junction Temperature

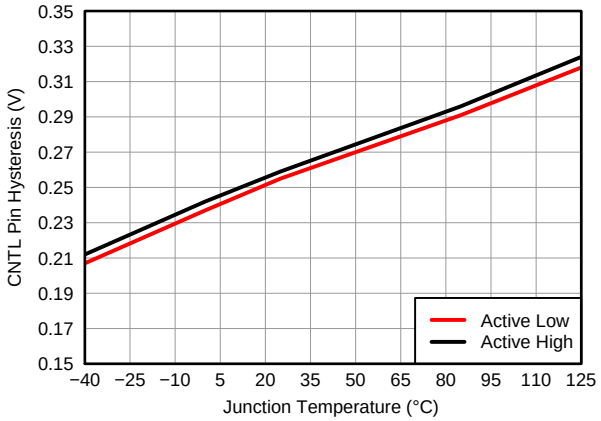


Figure 2. CRTL Pin Hysteresis vs. Junction Temperature

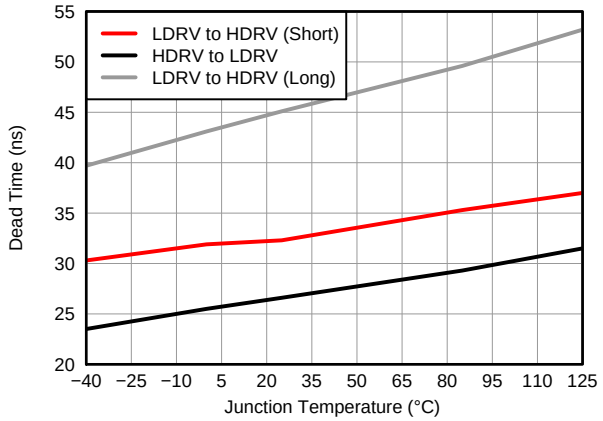


Figure 3. Dead Time vs. Junction Temperature

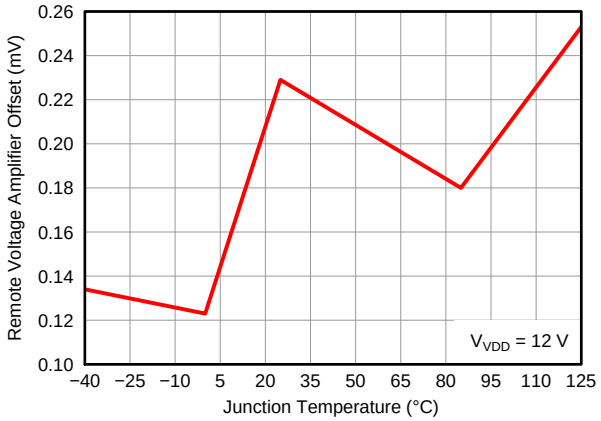


Figure 4. Remote Voltage Amplifier Offset vs. Junction Temperature

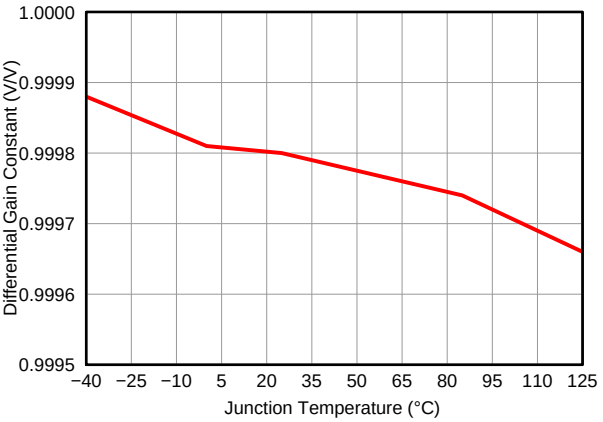


Figure 5. Remote Voltage Amplifier Gain vs. Junction Temperature

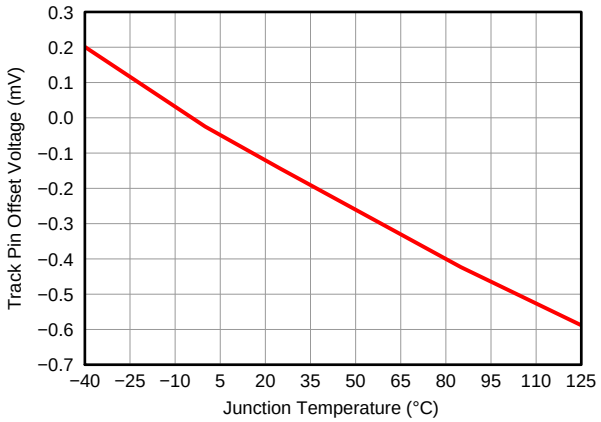


Figure 6. TRACK Pin Offset Voltage vs. Junction Temperature

Copyright © 2011, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

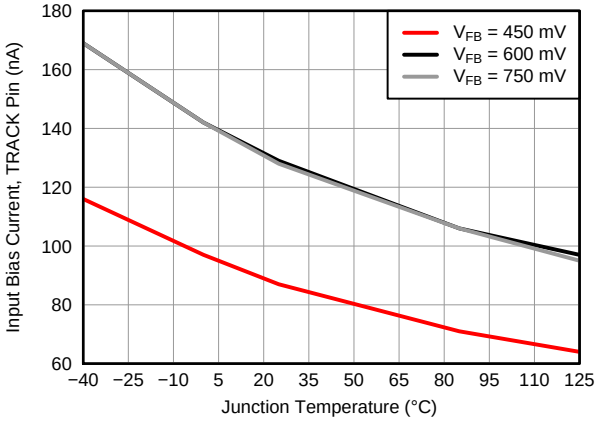


Figure 7. TRACK Pin Input Bias Current vs. Junction Temperature

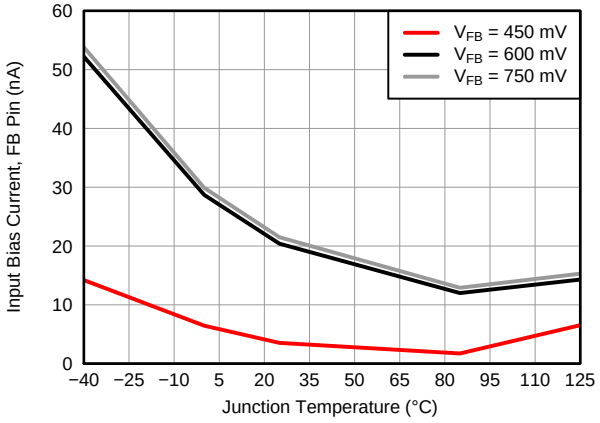


Figure 8. FB pin Input Bias Current vs. Junction Temperature

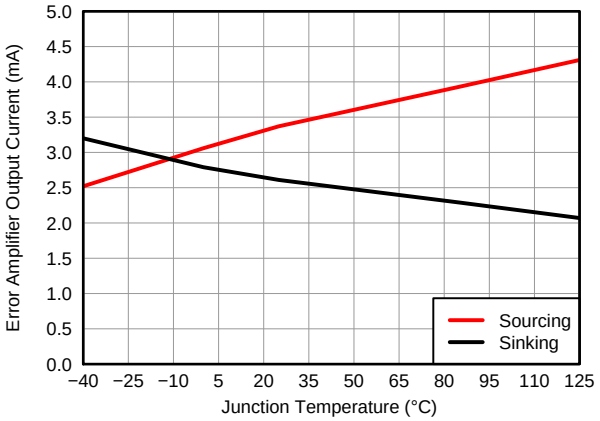


Figure 9. Error Amplifier Output Current vs. Junction Temperature

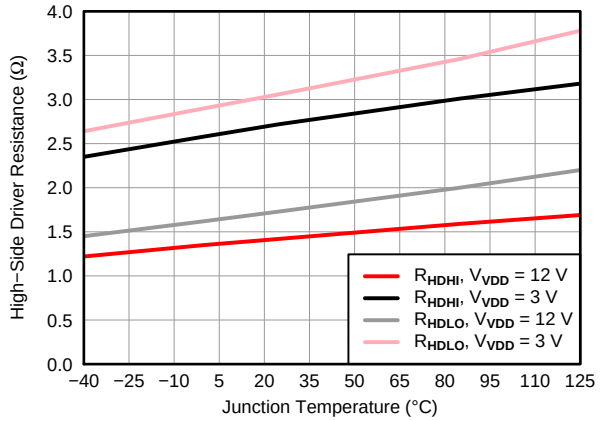


Figure 10. High-Side Driver Resistance vs. Junction Temperature

MINIMUM ON-TIME
vs
JUNCTION TEMPERATURE

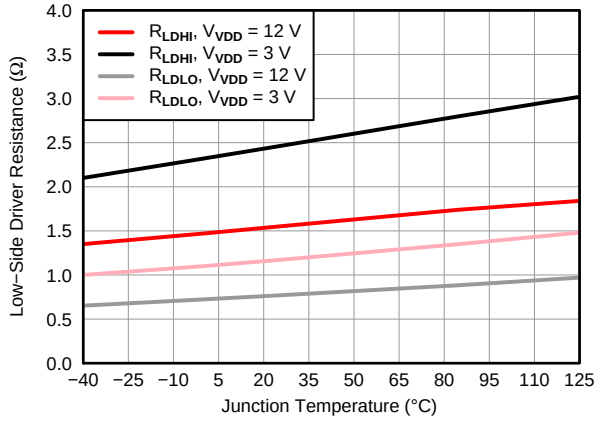


Figure 11. Low-Side Driver Resistance vs. Junction Temperature

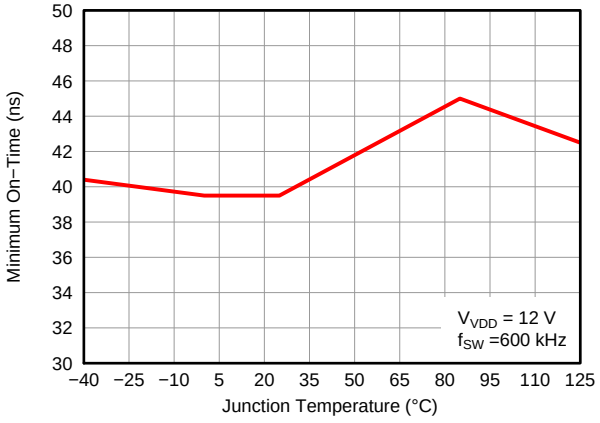


Figure 12. Minimum On-Time vs. Junction Temperature

Copyright © 2011, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

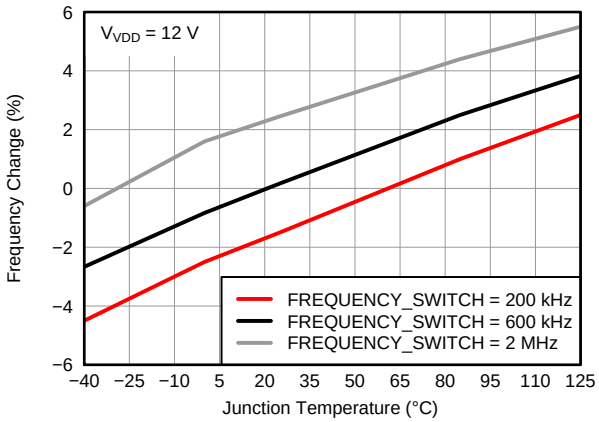


Figure 13. Switching Frequency Change vs. Junction Temperature

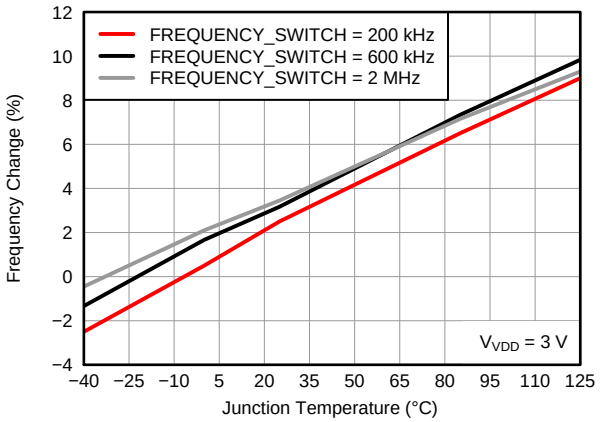


Figure 14. Switching Frequency Change vs. Junction Temperature

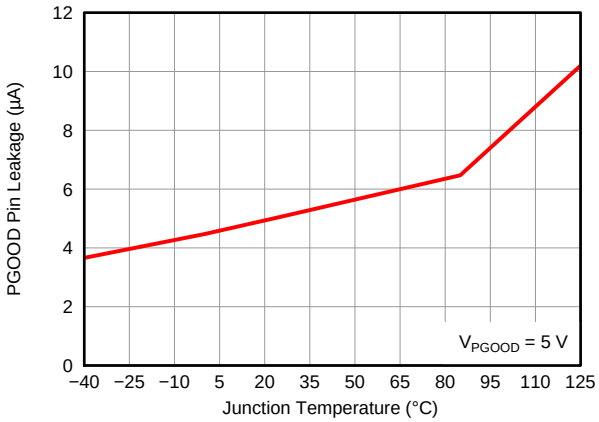


Figure 15. PGOOD Pin Current Leakage vs. Junction Temperature

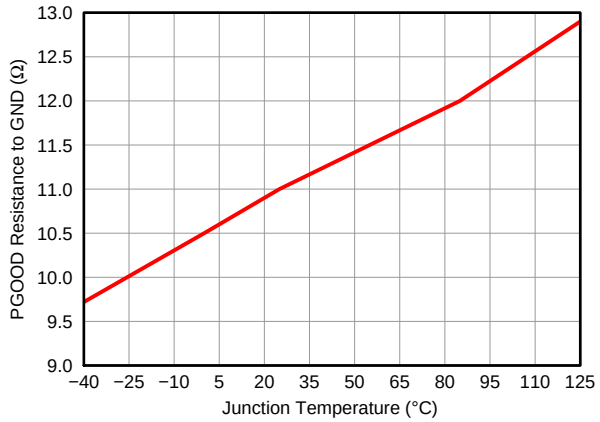


Figure 16. PGOOD Resistance to GND vs. Junction Temperature

Copyright © 2011, Texas Instruments Incorporated

APPLICATION INFORMATION

PMBus

General Description

Timing and electrical characteristics of the PMBus can be found in the PMB Power Management Protocol Specification, Part 1, revision 1.1 available at http://pmbus.org. The TPS40400 supports both the 100 kHz and 400 kHz bus timing requirements. The TPS40400 does not stretch pulses on the PMBus when communicating with the master device.

Communication over the TPS40400 device PMBus interface can either support the Packet Error Checking (PEC) scheme or not. If the master supplies CLK pulses for the PEC byte, it is used. If the CLK pulses are not present before a STOP, the PEC is not used.

The TPS40400 supports a subset of the commands in the PMBus 1.1 specification. Most all of the controller parameters can be programmed using the PMBus and stored as defaults for later use. All commands that require data input or output use the literal format. The exponent of the data words is fixed at a reasonable value for the command and altering the exponent is not supported. Direct format data input or output is not supported by the TPS40400. See the SUPPORTED COMMANDS section for specific details.

The TPS40400 also supports the SMBALERT response protocol. The SMBALERT response protocol is a mechanism by which a slave (the TPS40400) can alert the bus master that it wants to talk. The master processes this event and simultaneously accesses all slaves on the bus (that support the protocol) through the alert response address. Only the slave that caused the alert acknowledges this request. The host performs a modified receive byte operation to get the slave's address. At this point, the master can use the PMBus status commands to query the slave that caused the alert. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

The TPS40400 contains non-volatile memory that is used to store configuration settings and scale factors. The settings programmed into the device are not automatically saved into this non-volatile memory though. The STORE_DEFAULT_ALL command must be used to commit the current settings to non-volatile memory as device defaults. The settings that are capable of being stored in non-volatile memory are noted in their detailed descriptions.

Setting up the Controller – Hardware Connections

The TPS 40400 is an analog controller, meaning that it uses traditional analog circuitry to control the output of the converter. Many of the operating parameters are set using the PMBus interface. This section describes how to set the controller parameters in an application.

Output voltage. The output voltage is set in a very similar to the way to a traditional analog controller using a voltage divider from the output to the feedback (FB) pin. The output voltage must be divided down to the nominal reference voltage of 600mV. Figure 17 shows the typical connections for the controller. The voltage at the load can be sensed using the unity gain differential voltage sense amplifier. This provides better load regulation for output voltages lower than 5V nominal (see electrical specifications for the maximum output voltage of the differential sense amplifier). For output voltages above this level, connect the output voltage directly to the junction of R1 and C1, leave DIFFO open do not connect the VSNS inputs to the output voltage. In this case, it is also recommended to connect VSNS+ to BP3 and VSNS- to GND. If desired the differential amplifier may also be used elsewhere in the overall system as a voltage buffer provided the electrical specifications are not exceeded

Copyright © 2011, Texas Instruments Incorporated

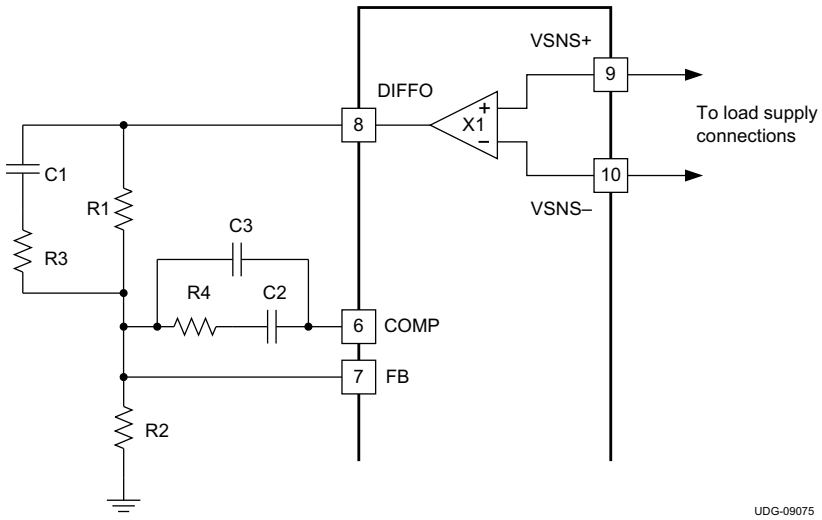


Figure 17. Setting the Output Voltage

The components in Figure 17 that determine the nominal output voltage are R1 and R2. R1 is normally chosen to make the feedback compensation values (R3, R4, C1, C2 andC3) come close to readily available standard values. R2 is then calculated in Equation 1.

$$R2 = V_{FB} \times \left(\frac{R1}{(V_{OUT} - V_{FB})} \right) \quad (1)$$

where

- V_{FB} is the feedback voltage
- V_{OUT} is the desired output voltage
- R1 and R2 are in the same units

The feedback voltage can be changed ±25% from the nominal 600mV using PMBus commands. This allows the output voltage to vary by the same percentage. *See the PMBus Functionality and Additional Setup section for further details.* Once the output voltage is set and the values of R1 and R2 are known, the VOUT_SCALE LOOP parameter can be calculated. This parameter is required for the PMBus interface to function properly when making output voltage adjustments.

Voltage feed forward. The TPS40400 has input voltage feed forward that maintains a constant power stage gain as input voltage varies and provides for very good response to input voltage transient disturbances. The simple constant power stage gain of the controller greatly simplifies feedback loop design because loop characteristics remains constant as the input voltage changes, unlike a buck converter without voltage feed forward. For modeling purposes, the gain from the COMP pin to the average voltage at the input of the L-C filter is 6V/V.

Output current limit and warning. The TPS40400 uses a differential current sense scheme to sense the output current. The sense element can be either the series resistance of the power stage filter inductor or a separate current sense resistor. When using the inductor series resistance as in Figure 18, a filter must be used to remove the large AC component of voltage across the inductor and leave only the component of the voltage that appears across the resistance of the inductor. The values of R5 and C4 for the ideal case can be found by Equation 2. The time constant of the R-C filter should be equal to or greater than the time constant of the inductor itself. If the time constants are equal, the voltage appearing across C4 is be the current in the inductor multiplied the inductor resistance. The inductor ripple current is reflected in the voltage across C4 perfectly in this case and there is no reason to have a shorter R-C time constant. The time constant of the R-C filter can be made longer than the inductor time constant because this is a voltage mode controller and the current sensing is done for overcurrent detection and output current reporting only. Extending the R-C filter time constant beyond the inductor time constant lowers the AC ripple component of voltage present at the ISNS pins of the TPS40400 but leaves the correct DC current information intact. This also delays slightly the response to an overcurrent event, but reduces noise in the system leading to cleaner overcurrent performance and current reporting data over the PMBus

Copyright © 2011, Texas Instruments Incorporated

$$R5 \times C4 \geq \left(\frac{L}{R_{ESR}} \right)$$

where (from Figure 18)

- R5 and R_{ESR} are in Ω
- C4 is in F (suggest 100 nF, 10^{-7}F)
- L is in H (2)

The maximum voltage that the TPS40400 is designed to accept across the ISNS pins is 110 mV. Because most all inductors have a copper conductor and because copper has a fairly large temperature coefficient of resistance, the resistance of the inductor and the current through the inductor should make a DC voltage less than 110 mV when the inductor is at the maximum temperature for the converter. This also applies for the external resistor in Figure 19. The full load output current multiplied by the sense resistor value, must be less that 110 mV at the maximum converter operating temperature.

There is also a constraint on the negative (reverse current) voltage that can be applied to the ISNS pins of the TPS40400. The voltage differential from ISNS+ to ISNS- should not be less than –45 mV. If this condition is not met, inaccurate results from the READ_IOUT command is the result. This is intended to be a ripple voltage limitation. The net current through the inductor must flow towards the load from the input voltage. Current sinking, while possible for the controller to accommodate, is not supported for overcurrent detection or for the READ_IOUT command.

In all cases, C4 should be placed as close to the ISNS pins as possible to help avoid problems with noise.

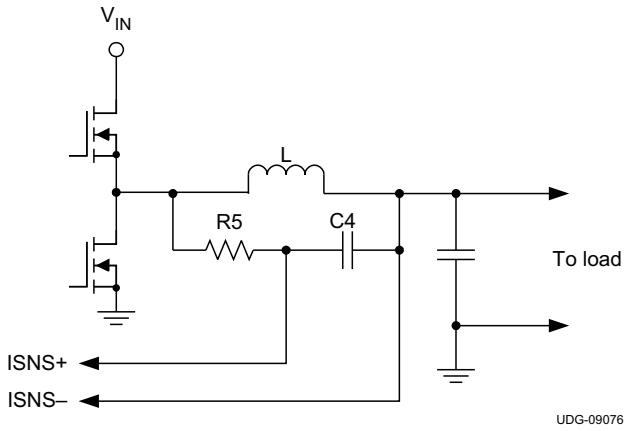


Figure 18. Current Sensing Using Inductor Resistance

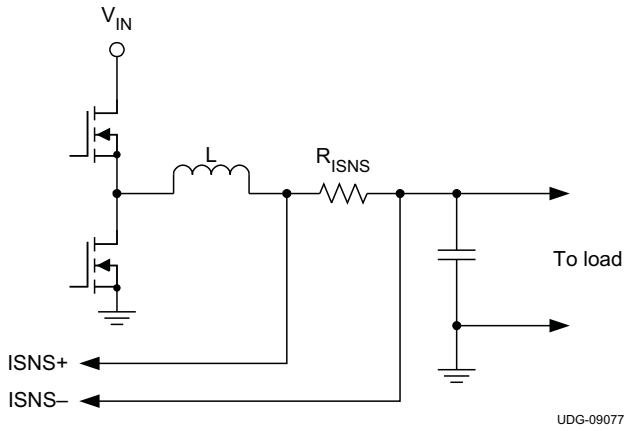


Figure 19. Current Sensing Using Sense Resistor

Once the current sensing method is chosen, the TPS40400 needs to be told what the resistance of the current sense element is. This allows the proper calculation of thresholds for the overcurrent fault and warning, as well as more accurate reporting of the actual output current. The IOUT_CAL_GAIN command is used to set the value of the sense element resistence of the device. IOUT_OC_WARN_LIMIT and IOUT_OC_FAULT_LIMIT set the levels for the overcurrent warning and fault levels respectively. (*See the PMBus Functionality and Additional Setup section for more details*.)

Linear regulators. The TPS40400 has two on board linear regulators primarily intended to provide suitable power for the internal circuitry of the device. These pins, BP3 and BP6 must be properly bypassed to function properly. BP3 needs a minimum of 100nF connected to GND and BP6 should have approximately 1µF connected to GND.

It is permissible to use the external regulator to power other circuits if desired, but care must be taken to ensure that the loads placed on the regulators do not adversely affect operation of the controller. The main consideration is to avoid loads with heavy transient currents that can affect the regulator outputs. Transient voltages on these outputs could result in noisy or erratic operation of the TPS40400.

.

Copyright © 2011, Texas Instruments Incorporated

Current limits must also be observed. Shorting the BP3 pin to GND damages the BP3 regulator. The BP3 regulator input comes from the BP6 regulator output. The current limit circuit on the BP6 regulator is 100 mA so the total current drawn from both regulators must be less than that. This total current includes the TPS40400 operating current I_{VDD} plus the gate drive current required to drive the power FETs. The total available current from two regulators is found in Equation 3 and Equation 4:

$$I_{LIN} = I_{BP6} - (I_{VDD} + I_{GATE}) \quad (3)$$

$$I_{GATE} = f_{SW} \times (Q_{gHIGH} + Q_{gLOW}) \quad (4)$$

where

- I_{LIN} is the total current that can be drawn from BP3 and BP6 in aggregate
- I_{BP6} is the current limit of the BP6 regulator – 100 mA minimum
- I_{VDD} is the quiescent current of the TPS40400 – 15 mA maximum
- I_{GATE} is the gate drive current required by the power FETs
- f_{SW} is the switching frequency
- Q_{gHIGH} is the total gate charge required by the high-side FET
- Q_{gLOW} is the total gate charge required by the low-side FET

PMBus address. The PMBus specification requires that each device connected to the PMBus have a unique address on the bus. The TPS40400 has 64 possible addresses (0 through 63 in decimal) that can be assigned by connecting resistors from the ADDR0 and ADDR1 pins to SGND. The address is set in the form of two octal (0-7) digits, one digit for each pin. ADDR1 is the high-order digit and ADDR0 is the low-order digit.

The E96 series resistors suggested for each digit value are shown in Table 1.

Table 1. E96 Series Resistors

DIGIT	RESISTANCE (kΩ)
0	10
1	15.4
2	23.7
3	36.5
4	54.9
5	84.5
6	130
7	200

The TPS40400 also detects values that are out of range on the ADDR0 and ADDR1 pins. If either pin is detected as having an out of range resistance connected to it, the TPS40400 continues to respond to PMBus commands, but at address 127, which is outside of the possible programmed addresses. It is possible but not recommended to use the device in this condition, especially if other TPS40400 devices are present on the bus or if another device could possibly occupy the 127 address.

PMBus connections. The TPS40400 supports both the 100 kHz and 400 kHz bus speeds. Connection for the PMBus interface should follow the High Power DC specifications given in section 3.1.3 in the SMBus specification V2.0 for the 400-kHz bus speed or the Low Power DC specifications in section 3.1.2. The complete SMBus specification is available from the SMBus web site, smbus.org.

PMBus Functionality and Additional Setup

Data format. There are three data formats supported in PMBus form commands that require representation of a literal number as their argument (commands that set thresholds, voltages or report such). A compatible device needs to only support one of these formats. The TPS40400 supports the *Linear* data format only for these commands. In this format, the data argument consists of two parts, a mantissa and an exponent. The number represented by this argument can be expressed as shown in Equation 5.

$$Value = Mantissa \times 2^{exponent} \quad (5)$$

Copyright © 2011, Texas Instruments Incorporated

Output voltage adjustment. The nominal output voltage of the converter can be adjusted using the VOUT_TRIM command. See the VOUT_TRIM command description for the format of this command as used in the TPS40400. The adjustment range is ±25% from the nominal output voltage. The VOUT_TRIM command is typically used to trim the final output voltage of the converter without relying on high precision resistors being used in Figure 17. The resolution of the adjustment is 7 bits, with a resulting minimum step size of approximately 0.4%. Note that the output margining is accomplished using this same 7 bit structure so the total combined deviation from the nominal output for margining and VOUT_TRIM is still limited to ±25%. Exceeding this range causes errors.

In order for the PMBus output voltage adjustments to function correctly, the VOUT_SCALE_LOOP parameter must be set properly. VOUT_SCALE_LOOP is a PMBus command (*see Supported PMBus Commands*) that tells the controller what the ratio of the voltage divider that sets the nominal output voltage is. The data for this command is the ratio of the divider that is used to set the output voltage. From Figure 17, VOUT_SCALE_LOOP parameter can be calculated using Equation 6.

$$VOUT_SCALE_LOOP = \frac{V_{FB}}{V_{OUT(nom)}} \tag{6}$$

The resolution of the VOUT_SCALE_LOOP command is 0.00195, or slightly under 0.2% due to the data format of the command (the linear data mode exponent is fixed at -9 for this command). This granularity affects the accuracy of adjustments to the output voltage made using the PMBus (VOUT_TRIM, VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW) as well as setting the over and under voltage fault and warning levels. These commands use the VOUT_SCALE_LOOP parameter to calculate what the reference voltage needs to be for the requested output voltage or the thresholds referenced to the FB pin need to be for the requested warning and fault levels.

Once the VOUT_SCALE_LOOP parameter has been properly set, the commands that adjust the output voltage functions properly. There are three possible states that the TPS4040 can be in when considering what the actual output voltage is:

- No output margin
- Margin high
- Margin low

These output states are set using the OPERATION command. The FB pin reference voltage is calculated as follows in each of these states.

No margin voltage:

$$V_{FB} = \left((VOUT_TRIM \times VOUT_SCALE_LOOP) + 0.6\right) \tag{7}$$

Margin high voltage state:

$$V_{FB} = \left((VOUT_MARGIN_HIGH + VOUT_TRIM) \times VOUT_SCALE_LOOP\right) \tag{8}$$

Copyright © 2011, Texas Instruments Incorporated

Margin low state:

$$V_{FB} = \left((VOUT_MARGIN_LOW + VOUT_TRIM) \times VOUT_SCALE_LOOP \right)$$

where

- V_{FB} is the FB pin voltage
- VOUT_TRIM is the offset voltage in volts to be applied to the output voltage
- VOUT_SCALE_LOOP is the output voltage divider scale parameter
- VOUT_MARGIN_HIGH is the requested margin high voltage
- VOUT_MARGIN_LOW is the requested margin low voltage (9)

For these conditions, the output voltage is shown in Equation 10.

$$V_{OUT} = V_{FB} \times \left(\frac{(R2 + R1)}{R2} \right)$$

where

- V_{FB} is the pin voltage calculated in Equation 7
- R2 and R1 are in consistent units from Figure 17
- VOUT is the output voltage (10)

NOTE

The sum of the margin and trim voltages cannot be more that ±25% from the nominal output voltage. The FB pin voltage can deviate no more that this from the nominal 600 mV.

When using the margin commands, the transition rate between any two of the three states (margin high, no margin and margin low) is determined by the soft start time (set by TON_RISE and the output voltage information available to the controller using the VOUT_SCALE_LOOP command. The result is that the transition rate between margin states is the same volts per second as the soft start ramp – assuming that the user has input the correct value for VOUT_SCALE_LOOP.

Overcurrent thresholds. PMBus provides for adjustable overcurrent in the TPS40400. To function properly, the TPS40400 must be given the current sensing element resistance value. This is accomplished by issuing the IOUT_CAL_GAIN command with the argument set to the resistance of the sense element (see the IOUT_CAL_GAIN command description). The resolution of this command is 30.5 µΩ and the range is 0 to 15.6 mΩ.

Another command, IOUT_CAL_OFFSET (see the command description) can be used to trim out offset errors in the READ_IOUT command results, overcurrent warning and fault level thresholds. The resolution of this command is 62.5 mA Offsets cannot be trimmed closer than half of this amount. The range for this command is -4 A to 3.937 A. Calibrating offsets to a level greater than this is not possible.

Once these two parameters have been set the IOUT_OC_WARN_LIMIT and IOUT_OC_FAULT_LIMIT limit commands can be used to set the overcurrent warning and fault thresholds for the converter. There are two resolution limiting factors in setting the overcurrent thresholds. The first is the resolution available in the IOUT_OC_WARN_LIMIT and IOUT_OC_FAULT_LIMIT commands. The resolution available here is 500 mA. This is the absolute minimum adjustment that can be made to these thresholds. The other potential limit is the resolution of the overcurrent DAC and can result in lower resolution. The overcurrent detection is done using a DAC to set the threshold and a comparator to sense when the actual current level is above that threshold. The resolution of the DAC is 1.875 mV. The resistance of the current sense element and this resolution determine the minimum adjustment that can be made to the overcurrent warning and fault thresholds. That minimum adjustment is given in Equation 11.

$$I_{\Delta OC} = \frac{1.875\,mV}{R_{ISNS}}$$

where

- $I_{\Delta OC}$ is the minimum change that can be made in the overcurrent warning or fault threshold

Copyright © 2011, Texas Instruments Incorporated

- R_{ISNS} is the resistance of the current sensing element, either the inductor DC resistance or the resistance of the current sense resistor used (11)

Combining these two resolution limits shows that for current sense elements with a resistance below 3.75 mΩ, the overcurrent resolution is given by Equation 11. For current sense element resistances above 3.75 mΩ, the overcurrent warning and fault resolution is 500 mA.

The TPS40400 has built in temperature correction for the temperature coefficient of resistance for copper wound inductors used as current sense elements. As the temperature of a copper wound inductor increases, its resistance increases, resulting in a higher DC component of voltage across it for a given current. This leads to a decrease in the current that would actually trip the overcurrent thresholds. The voltages that the TPS40400 uses to represent the overcurrent thresholds is automatically adjusted higher as the die temperature of the TPS40400 increases. The temperature coefficient for the increase of the thresholds is chosen close to the temperature coefficient of copper at 4000 ppm/°C. The change in overcurrent threshold voltage from one temperature to another is given in Equation 12.

$$V_{OC2} - V_{OC1} = (T2 - T1) \times (1 + TC_{CU}) \times V_{OC1}$$

where

- V_{OC1} and V_{OC2} are the overcurrent threshold voltages
- T1 and T2 are the corresponding temperatures in °C
- T_{CCU} is the temperature coefficient, 0.004 (12)

The change in overcurrent threshold voltages given in Equation 12 maintains the actual overcurrent trip points near constant only if the die temperature of the TPS40400 and the copper temperature of the inductor are closely coupled. If the inductor copper temperature rises higher than the TPS40400 die temperature, the overcurrent thresholds appears to decrease and vice versa.

Temperature compensation applied to the overcurrent thresholds must be considered. The threshold voltage must not be or become greater (with the internal temperature compensation) than 110 mV referred to the voltage at the ISNS pins. For instance, if a 10 mΩ resistance inductor was used as the current sense element, a current of 10 A would cause a 100mV DC level at the current sense pins. At first this looks just fine and within the bounds of the 110 mV limit of the controller. However, the temperature compensation of the threshold inside the device raises the effective threshold as the TPS40100 die temperature increases. For 100°C increase in die temperature, for example, the effective threshold crossed at the ISNS pins to trip an overcurrent is approximately 140 mV at the ISNS pins. The TPS40400 cannot respond this high and the result is a failure of the overcurrent mechanism to respond at higher die temperatures. For a given maximum temperature defined by the characteristics of the particular application, the maximum overcurrent setting that should be made for the TPS40400 is calculated in Equation 13.

$$I_{MAX} = \frac{V_{ISNS(max)}}{R_{ISNS} \times \left((T_{MAX} - 25) \times (TC_{CU} + 1)\right)}$$

where

- I_{MAX} is the maximum overcurrent threshold setting permissible (using the IOUT_OC_FAULT_LIMIT command) in A
- $V_{ISNS(max)}$ is the maximum allowable voltage differential at the ISNS pins, 120 mV R_{ISNS} is the resistance of the current sensing element – either inductor or current sense resistor
- T_{MAX} is the maximum junction temperature expected for the TPS40400 in °C
- TC_{CU} is the temperature coefficient of resistance for copper, 0.004 (13)

Equation 13 is illustrated in Figure 20. This figure shows the variation of the internal overcurrent threshold as the die temperature increases. In this example, the designated maximum die temperature is 125°C. For the overcurrent threshold to be valid at this temperature (110 mV or below), the maximum overcurrent threshold that should be set using the IOUT_OC_FAULT or IOUT_OC_WARN commands should correspond to no more than 75.7 mV. The current level that achieves this is what is calculated in Equation 13. If the maximum expected die temperature is less than 125°C, then the maximum 25°C overcurrent threshold increases accordingly.

Copyright © 2011, Texas Instruments Incorporated

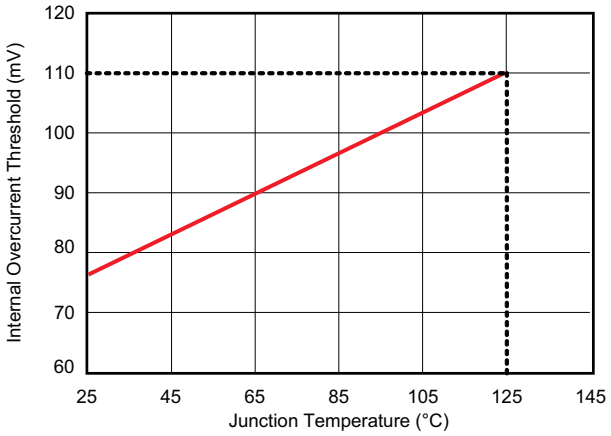


Figure 20. Internal Overcurrent Threshold Variation

Reading the output current. The average output current for the converter is readable using the READ_IOUT command. The results of this command support only positive or current sourced from the converter. If the converter is sinking current the result of this command is a reading of 0 A. Another consideration is the amount of ripple voltage applied to the ISNS pins when the DC voltage level is low – i.e., low or no output current. Because the TPS40400 averages out the ripple voltage when reporting the output current using the READ_IOUT command. Excessive negative ripple voltage ($V_{ISNS+} - V_{ISNS-} < 0$) at the ISNS pins causes an error in the reported output current. To ensure accurate readings the differential voltage at these pins should not be allowed to exceed –45 mV.

Soft-start time. The TPS40400 supports several soft-start times from 600 µs to 9 ms selected by the TON_RISE PMBus command. See the command description for full details on the levels and implementation. When selecting the soft-start time, care must be taken to ensure that the charging current for the output capacitors is considered. In some applications (e.g., those with large amounts of output capacitance) this current can lead to problems with nuisance tripping of the overcurrent protection circuitry. To ensure that this does not happen, the output capacitor charging current should be included when considering where to set the overcurrent threshold. The output capacitor charging current can be found using Equation 14:

$$I_{CAP} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}} \quad (14)$$

where

- I_{CAP} is the startup charging current of the output capacitance in A
- V_{OUT} is the output voltage of the converter in V
- C_{OUT} is the total output capacitance in F
- t_{SS} is the selected soft-start time in seconds

With the charging current calculated, the overcurrent threshold can then be calibrated to the sum of the maximum load current and the output capacitor charging current plus some margin. The amount of margin required depends on the individual application, but 25% is a suggested starting point. More or less may be required.

Power good. The TPS40400 has user selectable power good thresholds. These thresholds determine at what voltage the PGOOD pin is allowed to go high and the associated PMBus flags are cleared. There are three possible settings that can be had. See the POWER_GOOD_ON and POWER_GOOD_OFF command descriptions for complete details. Note that these commands establish symmetrical values above and below the nominal voltage. Values entered for each threshold should be the voltages corresponding to the threshold below the nominal output voltage. For instance, if the nominal output voltage is 3.3 V, and the desired power good on thresholds are ±5%, the POWER_GOOD_ON command is issued with 2.85 V as the desired threshold. The POWER_GOOD_OFF command must be set to a lower value (higher percentage) than the POWER_GOOD_ON command as well. The VOUT_SCALE_LOOP command must be set to approximately 0.1818 for these examples to work correctly.

Copyright © 2011, Texas Instruments Incorporated

The FB pin is used to sense the output voltage for the purposes of power good detection. Because of this there is the inherent filtering action provided by the compensation network connected from COMP to FB. As the output voltage rises or falls below the nominal value, the error amplifier attempts to force FB to match its reference voltage. When the error amplifier is no longer able to do this, the FB pin begins to drift and trip the power good threshold. For this reason the network from COMP to FB should have no purely resistive path.

Power good de-asserts during all startups, after any fault condition is detected or whenever the device is turned off or in a disabled state (OPERATION command or CNTL pin put the device into a disabled or off state). The PGOOD pin acts like a diode to GND when the device has no power applied to the VDD pin.

Undervoltage lockout. The TPS40400 provides flexible user adjustment of the undervoltage lockout threshold and the hysteresis. Two PMBus commands VIN_ON and VIN_OFF allow the user to set these input voltage turn on and turn off thresholds independently, with a 500-mV resolution from a minimum of 2.5-V turn off to a maximum 18-V turn on. See the command descriptions for more details.

Output overvoltage and undervoltage thresholds. The TPS40400 has output overvoltage protection and undervoltage protection capability. The comparators that look at the overvoltage conditions and undervoltage conditions use the FB pin as the output sensing point so the filtering effect of the compensation network connected from COMP to FB has an effect on the speed of detection. As the output voltage rises or falls below the nominal value, the error amplifier attempts to force FB to match its reference voltage. When the error amplifier is no longer able to do this, the FB pin begins to drift and trip the overvoltage threshold or the undervoltage threshold. For this reason the network from COMP to FB should have no purely resistive path.

The VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT commands are used to set the output overvoltage and undervoltage thresholds. There are four possible thresholds that can be set with the undervoltage and overvoltage commands. See the command descriptions for complete details.

Programmable fault responses. For the various fault conditions, the TPS40400 allows the user to select the fault response. The faults that have programmable responses with the TPS40400 are overcurrent (see the IOUT_OC_FAULT_RESPONSE command description), overtemperature, (see the OT_FAULT_RESPONSE command description), output overvoltage, (see the VOUT_OV_FAULT_RESPONSE command description) and output undervoltage, (see the VOUT_UV_FAULT_RESPONSE command description). These commands program the TPS40400 response to the corresponding fault condition. Possible responses include ignoring the fault, latching off and requiring a reset (either VDD power cycle or a toggling of the CNTL pin and/or OPERATION command status) for the converter to restart. See the individual fault response command descriptions for details on what is available for the specific command.

User data and adjustable anti-cross conduction delay. The TPS 40400 provides a command, MFR_SPECIFIC_00, which can be used as a scratchpad to store 14 bits of arbitrary data. These bits can represent anything that the user desires and can be stored in EEPROM for non-volatility. Bit 0 of this command is used to select between two dead time settings for the controller. The particular setting required for a given application depends upon several things, including total FET gate charge, FET gate resistance, PCB layout quality, temperature, etc. It is not possible to give a hard and fast rule as to when to use which setting, but generally, for FETs above 25 nC gate charge, the longer dead time setting should be looked at. The shorter dead time setting allows higher efficiency in applications where the FETs are generally small and switch very quickly, while may lead to minimum amounts of cross conduction in applications with larger, slower switching FETs. Conversely, using the longer dead time setting with smaller, faster switching FETs leads to excessive body diode conduction in the low-side FET, leading to a drop in converter efficiency. Bit 1 of this command permanently locks certain parameters from being changed when set to 1. Use with caution. For more detail, see the MFR_SPECIFIC_00 command description.

Copyright © 2011, Texas Instruments Incorporated

SUPPORTED COMMANDS

The TPS40400 supports the following commands from the PMBus 1.1 specification.

OPERATION (01h)

The OPERATION command is used to turn the device output on or off in conjunction with the input from the CONTROL pin. It is also used to set the output voltage to the upper or lower MARGIN voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CONTROL pin instructs the device to change to another mode.

Command	OPERATION							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r	r/w	r/w	r/w	r/w	r	r
Function	ON	X	Margin				X	X
Default Value	0	0	0	0	0	0	X	X

On

This bit is an enable command to the converter.

- 0: output switching is disabled. Both drivers placed in an off or low state.
- 1: output switching is enabled. The device is allowed to begin power conversion assuming no fault conditions exist.

Margin

If Margin Low is enabled, load the value from the VOUT_MARGIN_LOW command. If Margin High is enabled, load the value from the VOUT_MARGIN_HIGH command. (See PMBus specification for more information)

- 00XX: Margin Off
- 0101: Margin Low (Ignore Fault)
- 0110: Margin Low (Act on Fault)
- 1001: Margin High (Ignore Fault)
- 1010: Margin High (Act on Fault)

Note that the reference voltage used for overvoltage, undervoltage detection and power good are derived from the actual reference voltage in effect at the time. Setting a margin to test for one of these fault conditions does not work. Testing for these conditions must be done by forcing the FB pin to a voltage that would trip these fault conditions based on the current reference voltage and the percentage difference from this level set by the threshold setting commands.

ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of CNTL pin input and serial bus commands needed to turn the unit on and off. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Command	ON_OFF_CONFIG							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r
Function	X	X	X	pu	cmd	cpr	pol	cpa
Default Value	X	X	X	1	0	1	1	1

pu

The pu bit sets the default to either operate any time power is present or for the on/off to be controlled by CNTL pin and PMBus OPERATION command. This bit is used in conjunction with the 'cp', 'cmd', and 'on' bits to determine start up.

Copyright © 2011, Texas Instruments Incorporated

Bit Value	ACTION
0	Device powers up any time power is present regardless of state of the CNTL pin.
1	Device does not power up until commanded by the CNTL pin and OPERATION command as programmed in bits [2:0] of the ON_OFF_CONFIG register.

cmd

The cmd bit controls how the device responds to the OPERATION command.

Bit Value	ACTION
0	Device ignores the “on” bit in the OPERATION command.
1	Device responds to the “on” bit in the OPERATION command.

cpr

The cpr bit sets the CNTL pin response. This bit is used in conjunction with the 'cmd', 'pu', and 'on' bits to determine start up.

Bit Value	ACTION
0	Device ignores the CNTL pin. On/off is controlled only by the OPERATION command.
1	Device requires the CNTL pin to be asserted to start the unit.

pol

The pol bit controls the polarity of the CONTROL pin. For a change to become effective, the contents of the ON_OFF_CONFIG register must be stored to non-volatile memory using either the SOR_DEFAULT_ALL or STORE_DEFAULT_CODE commands and the device power cycled. Simply writing a new value to this bit does not change the polarity of the CNTL pin.

Bit Value	ACTION
0	CNTL pin is active low.
1	CNTL pin is active high.

cpa

The cpa bit sets the CNTL pin action when turning the controller off. This bit is read internally and cannot be modified by the user.

Bit Value	ACTION
1	Turn off the output and stop transferring energy to the output as fast as possible.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its $\overline{\text{SMBALERT}}$ signal output if the device is asserting the $\overline{\text{SMBALERT}}$ signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit is immediately reset and the host notified by the usual means.

Copyright © 2011, Texas Instruments Incorporated

WRITE_PROTECT (10h)

The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to the device configuration or operation. All supported command parameters may have their parameters read, regardless of the WRITE_PROTECT settings. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Command	WRITE_PROTECT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	X	X	X	X	X
Function	bit7	bit6	bit5	X	X	X	X	X
Default Value	0	0	0	X	X	X	X	X

bit5

Bit Value	ACTION
0	Enable all writes as permitted in bit6 or bit7
1	Disable all writes except the WRITE_PROTECT, OPERATION and ON_OFF_CONFIG. (bit6 and bit7 must be 0 to be valid data)

bit6

Bit Value	ACTION
0	Enable all writes as permitted in bit5 or bit7
1	Disable all writes except for the WRITE_PROTECT and OPERATION commands. (bit5 and bit7 must be 0 to be valid data)

bit7

Bit Value	ACTION
0	Enable all writes as permitted in bit5 or bit6
1	Disable all writes except for the WRITE_PROTECT command. (bit5 and bit6 must be 0 to be valid data)

In any case, only one of the three bits may be set at any one time. Attempting to set more than one bit results in an alert being generated and the cml bit is STATUS_WORD being set.

STORE_DEFAULT_ALL (11h)

The STORE_DEFAULT_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up.

It is permissible to use this command while the device is switching. Note however that the device continues to switch but ignores all fault conditions until the internal store process has completed.

EEPROM programming faults cause the device to NACK and set the 'cml' bit in the STATUS_BYTE and the 'oth' bit in the STATUS_CML registers.

RESTORE_DEFAULT_ALL (12h)

The RESTORE_DEFAULT_ALL command restores all of the storable register settings from EEPROM memory.

This command should not be used while the device is actively switching. If this is done, the device stops switching the output drivers and the output voltage drops. Depending on loading conditions, the output voltage could reach an undervoltage level and trigger an undervoltage fault response if programmed to do so. The command can be used while the device is switching, but it is not recommended as it results in a restart that could disrupt power sequencing requirements in more complex systems. It is strongly recommended that the device be stopped before issuing this command.

Copyright © 2011, Texas Instruments Incorporated

STORE_DEFAULT_CODE (13h)

The STORE_DEFAULT_CODE command instructs the PMBus core to store the contents of the programming register whose Command Code matches the value in the data byte into memory as the new default value.

Command	STORE_DEFAULT_CODE							
Bit Position	7	6	5	4	3	2	1	0
Access	w	w	w	w	w	w	w	w
Function	Command code							

EEPROM programming faults cause the device to NACK and set the ‘cml’ bit in the STATUS_BYTE and the ‘oth’ bit in the STATUS_CML registers. It is permissible to use this command while the device is switching. Note however that the device continues to switch but ignores all fault conditions until the internal store process has completed.

It is permitted to use the STORE_DEFAULT_CODE command while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable, undesirable or even catastrophic results. It is recommended to turn off the device output before issuing this command.

RESTORE_DEFAULT_CODE (14h)

The RESTORE_DEFAULT_CODE command instructs the PMBus core to overwrite the programming register whose Command Code matches the value in the data byte, with the default value.

Command	STORE_DEFAULT_CODE							
Bit Position	7	6	5	4	3	2	1	0
Access	w	w	w	w	w	w	w	w
Function	Command code							

The RESTORE_DEFAULT_CODE command should not be used while the device is switching because the device stops switching and restarts. During the restart, the low-side driver turns on for an extended time period and could damage loads that are sensitive to the power rail sinking current. If this is of no concern then the command may be used while the device is switching.

NOTE

A VIN_UV fault may be triggered when RESTORE_DEFAULT_ALL or RESTORE_DEFAULT_CODE command is set. The firmware workaround is accomplished by verifying that, upon completion of a RESTORE_DEFAULT_ALL or RESTORE_DEFAULT_CODE command, the sole source asserting SMB_ALERT is STATUS_BYTE[3] (VIN_UV). If so, issue a CLEAR_FAULTS command. Any other source asserting SMB_ALERT under these circumstances (i.e. completion of RESTORE_DEFAULT_ALL or RESTORE_DEFAULT_CODE) would indicate an actual fault condition.

VOUT_MODE (20h)

Description: The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit mode and 5-bit exponent parameter, as shown below. The 3-bit mode sets whether the device uses the Linear or Direct modes for output voltage related commands. The 5-bit parameter sets the exponent value for the linear data mode. The mode and exponent parameters are set and do not permit the user to change the values.

Command	VOUT_MODE							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Mode			Exponent				
Default Value	0	0	0	1	0	1	1	0

Copyright © 2011, Texas Instruments Incorporated

Mode:

Value fixed at 000, linear mode.

Exponent

Value fixed at 11011, Exponent for Linear mode values is –10.

VOUT_TRIM (22h)

The VOUT_TRIM command is used to apply a fixed offset voltage to the output voltage command value. It is most typically use by the end user to trim the output voltage at the time the PMBus device is assembled into the end user system. It is vital that the VOUT_SCALE_LOOP comand is set correctly in order to obtaining correct results. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal).

$$V_{OUT(offst)} = VOUT_TRIM \times 2^{-10} \tag{15}$$

The maximum value of $V_{OUT(offst)}$ is ±25% of nominal VOUT. Nominal V_{OUT} is set by external resistors and the 600 mV error amplifier reference. The valid range in 2s complement for this command is –4000h to 3FFF. The high order two bits of the high byte must both be either 0 or 1. They cannot have different values. If a value outside of the ±25% is given with this command, the TPS40400 sets the output voltage to the upper or lower limit depending on the direction of the setting, assert SMBALRT, set the CML bit in STATUS_BYTE and the invalid data bit STATUS_CML.

Command	VOUT_TRIM															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_MARGIN_HIGH (25h)

The VOUT_MARGIN_HIGH command sets the target voltage which the output changes to when the OPERATION command is set to "Margin High". The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal). The actual output voltage commanded by a margin high command can be found by:

$$V_{OUT(MH)} = (VOUT_MARGIN_HIGH + VOUT_TRIM) \times 2^{-10} \tag{16}$$

The maximum margin range is ±25% of nominal VOUT. Nominal VOUT is set by external resistors and a 600 mV error amplifier reference and does not include the offset generated by VOUT_TRIM. It is critical that the correct value be programmed into VOUT_SCALE_LOOP for the correct margin value to be calculated. Error checking is not performed when the VOUT_MARGIN_HIGH command is issued. The error checking is done when the OPERATION command is issued calling for a margin high state. At that time, values outside the ±25% range is treated as invalid data and causes the set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The output voltage is then set to to the upper or lower limit depending on the direction of the setting. The device state can be restored to power up defaults by issuing either the RESTORE_DEFAULT_ALL or RESTORE_DEFAULT_CODE commands.

Copyright © 2011, Texas Instruments Incorporated

Command	VOUT_MARGIN_HIGH															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	1	0	1	0	1	0	0	0	1	1	1

The default value of VOUT_MARGIN_HIGH is 0x547 or 1351. This corresponds to a default margin high voltage of 1.32 V with the default VOUT_SCALE_LOOP value of 0.5 and external resistor selection to give 1.2 V nominal output voltage.

VOUT_MARGIN_LOW (26h)

The VOUT_MARGIN_LOW command sets the target voltage which the output changes to when the OPERATION command is set to "Margin Low". The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal). The actual output voltage commanded by a margin high command can be found by:

$$V_{OUT(ML)} = (VOUT_MARGIN_LOW + VOUT_TRIM) \times 2^{-10} \quad (17)$$

The maximum margin range is ±25% of nominal VOUT. Nominal VOUT is set by external resistors and a 600 mV error amplifier reference and does not include the offset generated by VOUT_TRIM. It is critical that the correct value be programmed into VOUT_SCALE_LOOP for the correct margin value to be calculated. Error checking is not performed when the VOUT_MARGIN_LOW command is issued. The error checking is done when the OPERATION command is issued calling for a margin high state. At that time, values outside the ±25% range is treated as invalid data and causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The output voltage is then set to the upper or lower limit depending on the direction of the setting. The device state can be restored to power up defaults by issuing either the RESTORE_DEFAULT_ALL or RESTORE_DEFAULT_CODE commands.

Command	VOUT_MARGIN_LOW															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	1

The default value of VOUT_MARGIN_LOW is 0x451 or 1105. This corresponds to a default margin high voltage of 1.08 V with the default VOUT_SCALE_LOOP value of 0.5 and external resistor selection to give 1.2 V nominal output voltage.

VOUT_SCALE_LOOP (29h)

VOUT_SCALE_LOOP is equal to the feedback resistor ratio. The nominal output voltage is set by a resistor divider and the internal 600mV reference voltage. The default value of VOUT_SCALE_LOOP is 0.5 meaning that the reference voltage is one half of the output voltage. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The correct setting for the VOUT_SCALE_LOOP parameter is shown in Equation 18.

$$VOUT_SCALE_LOOP = \frac{V_{FB}}{V_{OUT(nom)}} \quad (18)$$

It is important that this parameter is set correctly because it has an effect on several other parameters. Any parameter that operates on or reports output voltage depends on the correct setting of this parameter for correct results to be obtained.

Copyright © 2011, Texas Instruments Incorporated

Command	VOUT_SCALE_LOOP															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent						Mantissa									
Default Value	1	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0

Exponent

Value fixed at –9 (dec).

Mantissa

Default value is 256 (dec). When combined with the exponent, the overall value of VOUT_SCALE_LOOP is 0.5 (dec). The maximum value for the mantissa is 512 for a VOUT_SCALE_LOOP value of 1.

FREQUENCY_SWITCH (33h)

The FREQUENCY_SWITCH command sets the switching frequency. Smarty Jones only supports frequencies from 200 kHz to 2 MHz. Values written within the supported frequency range is rounded up to the nearest supported increment. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

There are 14 distinct supported frequencies:

- 200 kHz
- 300 kHz
- 400 kHz
- 500 kHz
- **600 kHz (default)**
- 700 kHz
- 800 kHz
- 900 kHz
- 1.0 MHz
- 1.2 MHz
- 1.4 MHz
- 1.6 MHz
- 1.8 MHz
- 1.9 MHz

The data word that accompanies this command is divided into a fixed 5-bit exponent and an 11-bit mantissa. The 5 most significant bits of the mantissa are fixed, while the lower six bits may be altered.

Command	FREQUENCY_SWITCH															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1	1

Exponent

Fixed at 5(dec)

Mantissa

The upper five bits are fixed at 0.
The lower six bits are writeable with a default value of 19 (dec).

Copyright © 2011, Texas Instruments Incorporated

VIN_ON (35h)

The VIN_ON command sets the value of the input voltage at which the unit should start operation assuming all other required startup conditions are met. Values are mapped to the nearest supported increment. Values outside the supported range are treated as invalid data and cause the device set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The value of VIN_ON remains unchanged on an out-of-range write attempt. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

SUPPORTED VIN_ON VALUES			
2.75(1)	6.50	10.50	14.50
3.00	7.00	11.00	15.00
3.50	7.50	11.50	15.50
4.00	8.00	12.00	16.00
4.50	8.50	12.50	16.50
5.00	9.00	13.00	17.00
5.50	9.50	13.50	17.50
6.00	10.00	14.00	18.00

(1) Default setting

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected, SMBALERT being asserted along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5-bit exponent and an 11-bit mantissa. The four most significant bits of the mantissa are fixed, while the lower 7 bits may be altered.

Command	VIN_ON															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1	1

Exponent

–2 (dec), fixed.

Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 11 (dec).

Copyright © 2011, Texas Instruments Incorporated

VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage at which the unit should stop operation. Values are mapped to the nearest supported increment. Values outside the supported range is treated as invalid data and causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers. The value of VIN_ON remains unchanged during an out-of-range write attempt. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

SUPPORTED VIN_OFF VALUES			
2.50(1)	6.50	10.50	14.50
3.00	7.00	11.00	15.00
3.50	7.50	11.50	15.50
4.00	8.00	12.00	16.00
4.50	8.50	12.50	16.50
5.00	9.00	13.00	17.00
5.50	9.50	13.50	17.50
6.00	10.00	14.00	

(1) Default setting

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON resultx in the new value being rejected, SMBALERT being asserted along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5 bit exponent and an 11 bit mantissa. The 4 most significant bits of the mantissa are fixed, while the lower 7 bits may be altered.

Command	VIN_OFF															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1	0

Exponent

–2 (dec), fixed.

Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 10 (dec)

IOUT_CAL_GAIN (38h)

The IOUT_CAL_GAIN is the ratio of the voltage at the current sense element to the sensed current. The units are Ohms (Ω). The effective current sense element can be the DC resistance of the inductor or a separate current sense resistor. The default setting is 3 mΩ, and the resolution is 30.5 μΩ. The range is 0 to 15.6 mΩ. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Command	IOUT_CAL_GAIN															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	0	0	0	1	0	0	0	0	1	1	0	0	0	1	0

Copyright © 2011, Texas Instruments Incorporated

Exponent

–15 (dec), fixed.

Mantissa

The upper four bits are fixed at 0.
The lower seven bits are programmable with a default value of 98 (dec)

IOUT_CAL_OFFSET (39h)

The IOUT_CAL_OFFSET is used to compensate for offset errors in the READ_IOUT results and the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT thresholds. The units are amps. The default setting is 0 amps. The resolution of the argument for this command is 62.5 mA and the range is +3937.5mA to -4000 mA. Values written outside of this range alias into the supported range. For example, 1110 0100 0000 0001 has an expected value of –63.0625 amps, but results in 1110 0111 1111 0001 which is –0.9375 A. This occurs because the read-only bits are fixed. The Exponent is always –4 and the 5 msb bits of the Mantissa are always equal to the sign bit. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Command	IOUT_CAL_OFFSET															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Exponent

–4 (dec), fixed.

Mantissa

MSB is programmable with sign, next 4 bits are sign extend only.
Lower six bits are programmable with a default value of 0 (dec)

VOUT_OV_FAULT_LIMIT (40h)

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage that causes an output overvoltage fault. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The effective value of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal) so the effective overvoltage trip point requested is:

$$V_{OUT(OV_req)} = VOUT_OV_FAULT_LIMIT \times 2^{-10} \quad (19)$$

The VOUT_OV_FAULT_LIMIT has two data bytes formatted as 2's complement binary integer. The actual values for the VOUT_ OV_FAULT_LIMIT trip point are set to fixed percentages of nominal V_{OUT}. There are four fixed percentages of the nominal V_{OUT} that are supported for overvoltage trip points.

- 108%
- 110%
- **112% (default)**
- 115%

For example, for a 1.2V nominal output, VOUT_OV_FAULT_LIMIT can be set to 1.296 V, 1.32 V, 1.344 V or 1.38 V. Values within the supported range is set to the nearest fixed percentage. It is critical that the correct value be programmed into VOUT_SCALE_LOOP for the correct overvoltage fault trip point to be calculated. Values outside the supported range results in the corresponding extreme value to be selected. No error conditions are reported

Copyright © 2011, Texas Instruments Incorporated

Command	VOUT_OV_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0

VOUT_OV_FAULT_RESPONSE (41h)

Description: The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to a VOUT_OV_FAULT_LIMIT fault. The device also:

- Sets the VOUT_OV bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT OV fault bit in the STATUS_VOUT register, and
- Notifies the host via $\overline{\text{SMBALRT}}$ pin

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

A one-byte unsigned binary data argument is used with this command:

Command	VOUT_OV_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/W	r/w	r/w	r/w	r/w	r	r	r
Function	RSP[1]	RSP[0]	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	0	0	0	0	0	1	0	0

RSP[1:0]

Output voltage overvoltage response

00: The device continues operation without interruption.

01: The device continues operation for four switching cycles. If the fault is still present, the device shuts down and responds according to RS[2:0].

10: The device shuts down and responds according to RS[2:0].

11: The device shuts down and attempts to restart.

RS[2:0]

Output voltage overvoltage retry setting

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted.

Copyright © 2011, Texas Instruments Incorporated

VOUT_UV_FAULT_LIMIT (44h)

The VOUT_UV_FAULT_LIMIT command sets the value of the output voltage that causes an output undervoltage fault. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The effective value of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal) so the effective overvoltage trip point requested is:

$$V_{OUT(UV_req)} = VOUT_UV_FAULT_LIMIT \times 2^{-10} \quad (20)$$

The VOUT_UV_FAULT_LIMIT has two data bytes formatted as two's complement binary integer. The actual values for VOUT_ UV_FAULT_LIMIT trip point are set to fixed percentages of nominal VOUT. There are four fixed percentages of V_{OUT} that are supported for overvoltage trip points.

- 92%
- 90%
- **88% (default)**
- 85%

For example, for a 1.2 V nominal output, VOUT_UV_FAULT_LIMIT can be set to 1.104 V, 1.08 V, 1.056 V or 1.02 V. Values within the supported range are set to the nearest fixed percentage. It is critical that the correct value be programmed into VOUT_SCALE_LOOP for the correct overvoltage fault trip point to be calculated. Values outside the supported range results in the corresponding extreme value to be selected. No error conditions are reported.

The VOUT_UV_FAULT_LIMIT command has two bytes formatted as a two's compliment binary integer:

Command	VOUT_UV_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	1	0	0	1	0	0	0	1	1	1	1

VOUT_UV_FAULT_RESPONSE (45h)

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to a VOUT_UV_FAULT_LIMIT fault. The device also:

- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT UV Fault bit in the STATUS_VOUT register, and
- Notifies the host via $\overline{\text{SMBALRT}}$ pin

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

A one-byte unsigned binary data word is used with this command:

Command	VOUT_UV_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r	r	r
Function	RSP[1]	RSP[0]	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	0	0	0	0	0	1	0	0

RSP[1:0]

Output voltage undervoltage response

00: The device continues operation without interruption.

Copyright © 2011, Texas Instruments Incorporated

01: The device continues operation for four switching cycles. If the fault is still present, the device shuts down and responds according to RS[2:0].

10: The device shuts down and responds according to RS[2:0].

11: The device shuts down and attempts to restart.

RS[2:0]

Output voltage undervoltage retry setting

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted.

IOUT_OC_FAULT_LIMIT (46h)

The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current fault condition. The IOUT_OC_FAULT_LIMIT should be set to equal to or greater than the IOUT_OC_WARN_LIMIT. Writing a value to IOUT_OC_FAULT_LIMIT less than IOUT_OC_WARN_LIMIT causea the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the SMBALRT signal. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The IOUT_OC_FAULT_LIMIT takes a two-byte data word formatted as follows:

Command	IOUT_OC_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	1	0	0	0	0	0	0	1	0	1	0	0

Exponent

–1 (dec), fixed.

Mantissa

The upper five bits are fixed at 0.
The lower six bits are programmable with a default value of 20 (dec)

The actual output current for a give mantissa and exponent is shown in Equation 21.

$$I_{OUT(oc)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \quad (21)$$

The default output fault current setting is 10 A. Values of $I_{OUT(oc)}$ can range between 0 A and 35 A in 500-mA increments.

IOUT_OC_FAULT_RESPONSE (47h)

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an IOUT_OC_FAULT_LIMIT fault. The device also:

- Sets the IOUT_OC bit in the STATUS_BYTE
- Sets the IOUT/POUT bit in the STATUS_WORD
- Sets the IOUT OC Fault bit in the STATUS_IOUT register, and
- Notifies the host as described in section 10.2.2 of the PMBus Specification.

Copyright © 2011, Texas Instruments Incorporated

The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Command	IOUT_OC_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r	r	r
Function	RSP[1]	RSP[0]	RS[2]	RS[1]	RS[0]	X	X	X
Default Value	0	0	0	0	0	1	0	0

RSP[1:0]

00: The device continues operation without interruption

01: This is unsupported and causes a data error.

10: The device continues operation for four switching cycles. If the fault is still present, the device shuts down and responds according to RS[2:0].

11: The device shuts down and attempts to restart.

RS[2:0]

000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

111: A one value for the Retry Setting means that the unit goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted.

IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning. When this current level is exceeded the device:

- Sets the OTHER bit in the STATUS_BYTE
- Sets the OCW bit in the STATUS_WORD
- Sets the IOUT overcurrent Warning (OCW) bit in the STATUS_IOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALRT}}$

The IOUT_OC_WARN_LIMIT threshold should always be set to less than or equal to the IOUT_OC_FAULT_LIMIT. Writing a value to IOUT_OC_WARN_LIMIT greater than IOUT_OC_FAULT_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the $\overline{\text{SMBALRT}}$ signal. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The IOUT_OC_WARN_LIMIT takes a two byte data word formatted as follows:

Command	IOUT_OC_WARN_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1

Copyright © 2011, Texas Instruments Incorporated

Exponent

–1 (dec), fixed

Mantissa

The upper five bits are fixed at 0.
Lower six bits are programmable with a default value of 15 (dec)

The actual output warning current level for a give mantissa and exponent is:

$$I_{OUT(oc)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \quad (22)$$

The default output fault current setting is 10A. Values of $I_{OUT(oc)}$ can range from 0A to 35A in 500mA increments. The default output warning current setting is 7.5A.

OT_FAULT_RESPONSE (50h)

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an output over temperature fault. The temperature sensed is the die temperature of the TPS40400 only. No other temperature sensors are provided. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands. The OT_FAULT_LIMIT parameter is not programmable and is therefore not supported in the PMBus command set. When an over temperature fault condition is sensed, the device:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the OT FAULT bit in the STATUS_TEMPERATURE register, and
- Notifies the host by asserting the $\overline{\text{SMBALRT}}$ signal

A one-byte unsigned binary data word is used with this command:

Command	OT_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r/w	r	r	r	r	r	r
Function	X	OTF_RS	X	X	X	X	X	X
Default Value	1	1	0	0	0	0	0	0

OTF_RS

Over temperature fault retry setting

0: A zero value for the Retry setting indicates that the unit does not attempt to restart.

1: A one value for the Retry setting indicates that the unit goes through a normal startup (soft-start) when the die temperature falls below the hysteresis band limit. (See the *Electrical Characteristics* table).

POWER_GOOD_ON (5Eh)

The POWER_GOOD_ON command sets the value of the output voltage at which the PGOOD output pin (open drain) is asserted high. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands. The actual implementation is a window comparator with symmetrical thresholds above and below the nominal. This command sets both the upper and lower power good threshold at the same time. The parameter passed with this command is always the lower threshold (less than the nominal output) and is mapped to the closest supported percentages of the nominal output voltage inTable 2.

Copyright © 2011, Texas Instruments Incorporated

Table 2. Supported POWER_GOOD_ON Levels

THRESHOLD	
Low	**High**
95%	105%
92%	108%
90%	110%

For example, with a 1.2 V nominal output voltage, the POWER_GOOD_ON command can set the lower threshold to 1.14 V, 1.104 V or 1.08 V. Doing this automatically sets the upper thresholds to 1.26 V, 1.296 V and 1.32 V respectively.

The effective value of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal) so the effective lower power good turn on threshold requested is:

$$V_{OUT(PGOOD_ON)} = POWER_GOOD_ON \times 2^{-10} \quad (23)$$

The nominal output voltage is set by external resistors and a 600-mV error amplifier reference. It is critical that the correct value be programmed into VOUT_SCALE_LOOP in order to correctly select the desired POWER_GOOD_ON threshold.

Normally, the POWER_GOOD_ON threshold is set higher than the POWER_GOOD_OFF threshold. If the POWER_GOOD_ON threshold is set to a value equal to or less than the POWER_GOOD_OFF threshold, the device:

- Sets the CML bit in the STATUS_BYTE
- Sets the Invalid data bit in STATUS_CML
- Notifies the host via $\overline{\text{SMBALRT}}$ pin

It is the user's responsibility to ensure that the chosen POWER_GOOD_ON and POWER_GOOD_OFF thresholds are reasonable with respect to each other. For values written outside the supported ranges are ACK'ed but causes the $\overline{\text{SMBALRT}}$ line to assert and the CML bit to be set in the STATUS_WORD. The invalid data bit is also set in the STATUS_CML results. The actual POWER_GOOD_ON threshold is set to the nearest supported extreme value. For instance, with VOUT_SCALE_LOOP set to 0.5 for a typical 1.2-V output supply, setting POWER_GOOD_ON to 0.5 results in the threshold being set to the 90% value.

The POWER_GOOD_ON command has two data bytes formatted as two's complement binary integer:

Command	**POWER_GOOD_ON**															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	1	0	0	0	1	1	0	1	0	1	0

The default value sets the power good turn on threshold to 1.1035V which maps to the 92% low threshold and 108% high threshold.

POWER_GOOD_OFF (5Fh)

The POWER_GOOD_OFF command sets the value of the output voltage at which the PGOOD output pin (open drain output) is de-asserted low. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands. The actual implementation is a window comparator with symmetrical thresholds above and below the nominal. This command sets both the upper and lower power good threshold at the same time. The parameter passed with this command is always the lower threshold (less than the nominal output) and is mapped to the closest supported percentages of the nominal output voltage below:

Copyright © 2011, Texas Instruments Incorporated

Supported POWER_GOOD_OFF Levels	
Low Threshold	**High Threshold**
92%	108%
90%(1)	110%
88%	112%

(1) Default value

For example, with a 1.2 V nominal output voltage, the POWER_GOOD_OFF command can set the lower threshold to 1.104 V, 1.0 8V or 1.056 V. Doing this automatically sets the upper thresholds to 1.296 V, 1.32 V and 1.344 V respectively.

The effective value of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –10 (decimal) so the effective lower power good turn on threshold requested are:

$$V_{OUT(PGOOD_OFF)} = POWER_GOOD_OFF \times 2^{-10} \quad (24)$$

The nominal output voltage is set by external resistors and a 600 mV error amplifier reference. It is critical that the correct value be programmed into VOUT_SCALE_LOOP for the correct POWER_GOOD_ON threshold to be selected.

Normally, the POWER_GOOD_ON threshold is set higher than the POWER_GOOD_OFF threshold. If the POWER_GOOD_ON threshold is set to a value equal to or less than the POWER_GOOD_OFF threshold, the device:

- Sets the CML bit in the STATUS_BYTE
- Sets the Invalid data bit in STATUS_CML
- Notifies the host via $\overline{\text{SMBALRT}}$ pin

It is the user's responsibility to make sure that chsen POWER_GOOD_ON and POWER_GOOD_OFF thresholds are reasonable with respect to each other. For values written outside the supported ranges are ACK'ed but cause the $\overline{\text{SMBALRT}}$ line to assert and the CML bit to be set in the STATUS_WORD. The invalid data bit is also set in the STATUS_CML results. The actual POWER_GOOD_OFF threshold is set to the nearest supported extreme value. For instance, with VOUT_SCALE_LOOP set to 0.5 for a typical 1.2-V output supply, setting POWER_GOOD_OFF to 0.5 results in the threshold being set to the 88% value.

The POWER_GOOD_OFF command has two data bytes formatted as two's complement binary integer:

Command	**POWER_GOOD_OFF**															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	1	0	0	0	1	0	1	0	0	1	0

The default value sets the power good turn off threshold to 1.08 V which maps to the 90% low threshold and 108% high threshold.

TON_RISE (61h)

The TON_RISE command sets the time in ms, from when the output starts to rise until the voltage has entered the regulation band. There are several discreet settings that this command supports. Commanding a value other than one of these values results in the nearest supported value being selected.

The supported TON_RISE times over PMBus are as follows. Note that the actual soft-start time is longer than the entered value. Typically the nominal value seen in operation is approximately 15% longer that the time entered.

- 600 µs
- 900 µs
- 1.2 ms
- 1.8 ms

Copyright © 2011, Texas Instruments Incorporated

- **2.7 ms (default value)**
- 4.2 ms
- 6.0 ms
- 9.0 ms

A value of 0 ms instructs the unit to bring its output voltage to the programmed regulation value as quickly as possible. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

The TON_RISE command is formatted as a linear mode two's complement binary integer.

Command	TON_RISE															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	1

Exponent

–4 (dec), fixed.

Mantissa

The upper two bits are fixed at 0.
The lower five bits are programmable with a default value of 43 (dec)

STATUS_BYTE (78h)

The STATUS_BYTE command returns one byte of information with a summary of the most critical device faults. For TPS40400, 4 fault bits is flagged in this particular command: output over-voltage, output over-current, over-temperature, and output under-voltage. The STATUS_BYTE reports communication faults in the CML bit. Other communication faults set the NONE OF THE ABOVE bit.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	X	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMPERATURE	CML	NONE OF THE ABOVE
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OFF:

The device is not providing power to the output, regardless of the reason. In TPS40400, this flag means that the converter is not enabled.

VOUT_OV:

An output overvoltage fault has occurred.

IOUT_OC:

An output over current fault has occurred.

VIN_UV:

An input undervoltage fault has occurred.

TEMPERATURE:

A temperature fault or warning has occurred.

Copyright © 2011, Texas Instruments Incorporated

CML:

A **C**ommunications, **M**emory or **L**ogic fault has occurred.

NONE OF THE ABOVE:

A fault or warning not listed in bit1 through bits 1-7 has occurred, for example an undervoltage condition or an over current warning condition

STATUS_WORD (78h)

The STATUS_WORD command returns two bytes of information with a summary of the device's fault/warning conditions. The low byte is identical to the STATUS_BYTE above. The additional byte reports the warning conditions for output overvoltage and overcurrent, as well as the power good status of the converter.

Command	STATUS_WORD (low byte)							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	X	OFF	VOUT_OV	IOUT_OC	VIN_UV	TEMPERATURE	CML	NONE OF THE ABOVE
Default Value	0	x	0	0	0	0	0	0

A "1" in any of the low byte (STATUS_BYTE) bit positions indicates that:

OFF:

The device is not providing power to the output, regardless of the reason. In TPS40400, this flag means that the converter is not enabled.

VOUT_OV:

An output overvoltage fault has occurred.

IOUT_OC:

An output over current fault has occurred.

VIN_UV:

An input undervoltage fault has occurred.

TEMPERATURE:

A temperature fault or warning has occurred.

CML:

A **C**ommunications, **M**emory or **L**ogic fault has occurred.

NONE OF THE ABOVE:

A fault or warning not listed in bits 1-7 has occurred

Command	STATUS_WORD (high byte)							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	VOUT	IOUT/POUT	X	X	$\overline{\text{POWER_GOOD}}$	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of the high byte bit positions indicates that:

VOUT:

An output voltage fault or warning has occurred

Copyright © 2011, Texas Instruments Incorporated

IOUT/POUT:

An output current warning or fault has occurred. The PMBus specification states that this also applies to output power. TPS40400 does not support output power warnings or faults.

$\overline{\text{POWER_GOOD}}$:

The power good signal is negated.

STATUS_VOUT (7Ah)

The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults. The only bits of this register supported by TPS40400 are VOUT_OV Fault and VOUT_UV Fault.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	VOUT OV Fault	X	X	VOUT UV Fault	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

VOUT OV Fault:

The device has seen the output voltage rise above the VOUT_OV_FAULT_LIMIT threshold.

VOUT UV Fault:

The device has seen the output voltage fall below the VOUT_UV_FAULT_LIMIT threshold.

STATUS_IOUT (7Bh)

The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults. The only bits of this register supported by TPS40400 are IOUT_OC Fault and IOUT_OC Warning.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	IOUT_OV Fault	X	IOUT OC Warning	X	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

IOUT_OV Fault:

The device has seen the output current rise above the level set by IOUT_OC_FAULT_LIMIT.

VOUT_UV Fault:

The device has seen the output current rise relating to the level set by IOUT_OC_WARN_LIMIT.

Copyright © 2011, Texas Instruments Incorporated

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns one byte of information relating to the status of the converter temperature related faults. The only bits of this register supported by TPS40400 are OT Fault and OT Warning.

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	OT Fault	OT Warning	X	X	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

OT Fault:

The device die temperature has exceeded the preset fault threshold.

OT Warning:

The device die temperature has exceeded the preset warning threshold.

STATUS_CML (7Eh)

The STATUS_CML command returns one byte of information relating to the status of the converter's communication related faults. The bits of this register supported by TPS40400 are:

Invalid/Unsuppported Command, Invalid/Unsupported Data, Packet Error Check Failed and Other Communication Fault.

Command	STATUS_CML							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Invalid/Unsuppported Command	Invalid/Unsupported Data	Packet Error Check Failed	X	X	X	Other Communication Fault	X
Default Value	0	0	0	0	0	0	0	0

A "1" in any of these bit positions indicates that:

Invalid/Unsupported Command:

An invalid or unsupported command has been received.

Invalild/Unsupported Data

Invalid or unsupported data has been received

Packet Error Check Failed

A packet has failed the CRC error check.

Other Communication Fault

Some other communication fault or error has occurred

Copyright © 2011, Texas Instruments Incorporated

READ_VIN (88h)

The READ_VIN commands returns two bytes of data in the linear data format that represent the input voltage applied to the VDD pin of the controller. The data format is as follows:

Command	READ_VIN															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0

The input voltage is scaled before it reaches the internal analog to digital converter so that resolution of the input voltage read back is 31.25mV. The input voltage can be found using Equation 25.

$$V_{IN} = \text{Mantissa} \times 2^{\text{Exponent}} \times (1 + \text{READ_VIN_CAL_GAIN}) + \text{READ_VIN_CAL_OFFSET} \quad (25)$$

Exponent

Fixed at –5.

Mantissa

The lower 10 bits are the result of the ADC conversion of the input voltage. The 11th bit is fixed at 0 because only positive numbers are considered valid.

READ_VIN_CAL_GAIN comes from the MFR_SPECIFIC_06 command

READ_VIN_CAL_OFFSET comes from the MFR_SPECIFIC_07 command

READ_VOUT (8Bh)

The READ_VOUT commands returns two bytes of data in the linear data format that represent the output voltage of the controller. The output voltage is sensed at the ISNS- pin so voltage drop to the load is not accounted for. The data format is as follows:

Command	READ_VOUT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The setting of the VOUT_MODE affects the results of this command as well. In the TPS40400, VOUT_MODE is set to linear mode with an exponent of –10 and cannot be altered. The output voltage can be found by:

$$V_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \times (1 + \text{READ_VOUT_CAL_GAIN}) + \text{READ_VOUT_CAL_OFFSET} \quad (26)$$

Exponent

Fixed at -10 by VOUT_MODE

Mantissa

Bits 13 (bit 5 in high order byte) through 4 are the result of the ADC conversion of the ouput voltage. The effective LSB using this scheme is 15.625 mV.

READ_VOUT_CAL_GAIN is derived from the MFR_SPECIFIC_05 command

READ_VOUT_CAL_OFFSET is derived from the MFR_SPECIFIC_04 command

Copyright © 2011, Texas Instruments Incorporated

READ_IOUT (8Ch)

The READ_IOUT commands returns two bytes of data in the linear data format that represent the output current of the controller. The output current is sensed at the ISNS+ and ISNS– pins. The data format is as follows:

Command	READ_IOUT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

The output current is scaled before it reaches the internal analog to digital converter so that resolution of the output current read is 62.5 mA, though resolution may be less depending on the setting of IOUT_CAL_GAIN. The maximum value that can be reported is 64 A. It is mandatory that the IOUT_CAL_GAIN and IOUT_CAL_OFFSET parameters are sset correctly in order to obtain accurate results. The output current can be found by using Equation 27.

$$I_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \tag{27}$$

Exponent

Fixed at -4.

Mantissa

The lower 10 bits are the result of the ADC conversion of the input voltage. The 11th bit is fixed at 0 because only positive numbers are considered valid.

PMBUS_REVISION (98h)

The PMBUS_REVISION command returns a single, unsigned binary byte that indicates that the TPS40400 is compliant with the 1.1 revision of the PMBus specification.

Command	PMBUS_REVISION							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Default Value	0	0	0	1	0	0	0	1

MFR_VIN_MIN (A0h)

The MFR_VIN_MIN command returns a two-byte linear formatted result that indicates the minimum voltage from which the TPS40400 is able to convert power. The data is formatted as follows:

Command	MFR_VIN_MIN															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0

The minimum input voltage can be found using Equation 28.

$$V_{IN} = \text{Mantissa} \times 2^{\text{Exponent}} \tag{28}$$

This equates to 3 V when evaluated with the default values. The TPS40400 begins to convert power at a minimum input of 2.75-V.

Copyright © 2011, Texas Instruments Incorporated

Exponent

Fixed at –2.

Mantissa

Fixed at 12.

MFR_VIN_MAX (A1h)

The MFR_VIN_MAX returns a two-byte linear formatted result that represents the maximum voltage that the TPS40400 is specified to operate at. The data is formatted as follows:

Command	MFR_VIN_MAX															
Format																
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	1	0	1	0	0	0	0

The maximum input voltage can be found from:

$$V_{IN(min)} = Mantissa \times 2^{Exponent} \quad (29)$$

This equals 20 V when evaluated with the default values.

Exponent

Fixed at –2.

Mantissa

Fixed at 80.

MFR_VOUT_MIN (A4h)

This command returns a two byte result that represents the minimum output voltage the TPS40400 supports.

Command	MFR_VOUT_MIN															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Mantissa															
Default Value	0	0	0	0	0	0	1	0	0	1	1	0	0	1	1	0

The setting of the VOUT_MODE affects the results of this command as well. In the TPS40400, VOUT_MODE is set to linear mode with an exponent of -10 and cannot be altered. The minimum nominal output voltage can be found by:

$$V_{OUT(max)} = Mantissa \times 2^{Exponent} \quad (30)$$

This equals to 600 mV using the pre-set values. Using VOUT_TRIM, it is possible to adjust this voltage down to approximately 450 mV.

Exponent

Fixed at –10.

Mantissa

Fixed at 614.

Copyright © 2011, Texas Instruments Incorporated

MFR_VOUT_MAX (A5h)

The command returns a two-byte result that represents the maximum output voltage that the TPS40400 supports.

Command	MFR_VOUT_MAX															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Mantissa															
Default Value	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

The setting of the VOUT_MODE affects the results of this command as well. In the TPS40400, VOUT_MODE is set to linear mode with an exponent of –10 and cannot be altered. The maximum nominal output voltage can be found by:

$$V_{OUT(max)} = \text{Mantissa} \times 2^{\text{Exponent}} \quad (31)$$

This evaluates to 12 V using the pre-set values.

Exponent

Fixed at –10.

Mantissa

Fixed at 12288

MFR_SPECIFIC_00 (D0h)

The MFR_SPECIFIC_00 command is used for storing arbitrary user data and for selecting a dead time or anti-cross conduction time for the TPS40400. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

This command take a two byte unsigned binary argument as follows.

Command	MFR_SPECIFIC_00															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	USER_DATA								USER_DATA						WPE	DTC
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Dead Time Control setting (DTC)

- 0: Fast. Dead time = ~25 ns
- 1: Slow. Dead time = ~ 50 ns

WPE

Write protect extension. Writing a 1 to this bit position permanently locks the following parameters:

- IOUT_CAL_GAIN
- IOUT_CAL_OFFSET
- FREQUENCY_SWITCH
- IOUT_OC_FAULT_LIMIT
- MFR_SPECIFIC_00

Copyright © 2011, Texas Instruments Incorporated

NOTE

Subsequent to setting the WPE bit, either a STORE_DEFAULT_ALL or STORE_DEFAULT_CODE (for MFR_SPECIFIC_00) PMBus command must be issued in order to prevent the WPE bit from being cleared when the device is subjected to a reset-restart operation.

MFR_SPECIFIC_01 (D1h)

This command is used for trimming internal components of the TPS40400 and is not recommended for general use.

MFR_SPECIFIC_02 (D2h)

This command is used for trimming internal components of the TPS40400 and is not recommended for general use.

MFR_SPECIFIC_03 (D3h)

This command is used for trimming internal components of the TPS40400 and is not recommended for general use.

MFR_SPECIFIC_04 (D4h)

This command applies an offset to the READ_VOUT command results to calibrate out offset errors in the on board measurement system. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Command	MFR_SPECIFIC_04															
Format	Linear, two's compliment binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r(1)	r(1)	r(1)	r(1)	r(1)	r(1)	r(1)	r(1)	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Bits are sign extension only and are not otherwise programmable.

Default value: 0

$$READ_VOUT_CAL_OFFSET = Mantissa \times 2^{Exponent} \quad (32)$$

- Exponent is fixed at 2^{-10} by VOUT_MODE
- LSB value is 975 µV
- Range -125 mV to 124 mV

MFR_SPECIFIC_05 (D5h)

This command applies a gain correction to the READ_VOUT command results to calibrate out gain errors in the on board measurement system. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Command	MFR_SPECIFIC_05															
Format	Linear, two's compliment binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r(1)	r(1)	r(1)	r(1)	r(1)	r(1)	r(1)	r(1)	r(1)	r(1)	r(1)	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0

(1) Bits are sign extension only and are not otherwise programmable.

Copyright © 2011, Texas Instruments Incorporated

Default value: 0

$$READ_VOUT_CAL_GAIN = Mantissa \times 2^{Exponent}$$

- Exponent is fixed at -8
- LSB value is 0.4%
- Range -0.125 to 0.121 (33)

MFR_SPECIFIC_06 (D6h)

This command applies an offset to the READ_VIN command results to calibrate out offset errors in the on board measurement system. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Command	MFR_SPECIFIC_06															
Format	Linear, two's compliment binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r(1)	r(1)	r(1)	r(1)	r(1)	r/w	r(1)	r(1)	r(1)	r(1)	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0

(1) Bits are sign extension only and are not otherwise programmable.

Default value: 0

$$READ_VIN_CAL_OFFSET = Mantissa \times 2^{Exponent}$$

- Exponent is fixed at -5
- LSB value is 32vmV
- Range -2vV to 1.968vV (34)

MFR_SPECIFIC_07 (D7h)

This command applies a gain correction to the READ_VIN command results to calibrate out gain errors in the on board measurement system. The contents of this register can be stored to non-volatile memory using the STORE_DEFAULT_ALL or STORE_DEFAULT_CODE commands.

Command	MFR_SPECIFIC_07															
Format	Linear, two's compliment binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r(1)	r(1)	r(1)	r(1)	r(1)	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) Bits are sign extension only and are not otherwise programmable.

Default value: 0

$$READ_VIN_CAL_GAIN = Mantissa \times 2^{Exponent}$$

- Exponent is fixed at -8
- LSB value is 0.4%
- Range -0.125V to 10.121 (35)

Copyright © 2011, Texas Instruments Incorporated

MFR_SPECIFIC_44 (FCh)

This command returns a two byte unsigned binary 12-bit device identifier code and 4-bit revision code in the following format.

Command	MFR_SPECIFIC_44															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Identifier Code												Revision Code			
Default Value	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1

This command is oriented toward providing similar information to the DEVICE_ID command but for devices that do not support block read and write functions.

Identifier Code

Fixed at 1 (dec)

Revision Code

Starts at 0 and increments as revisions progress.

Copyright © 2011, Texas Instruments Incorporated

DESIGN EXAMPLES

Design Example 1: 12-V Input, 1.2-V Output, 20-A (max) Output Current

Design Parameters

The following example illustrates the design process and component selection for a synchronous buck converter using the TPS40400 controller. The design goal parameters are listed in Table 3.

Table 3. Design Electrical Parameters

PARAMETER		NOTES AND CONDITIONS	MIN	NOM	MAX	UNITS
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		8	12	14	V
I_{IN}	Input current	V_{IN} = 8 V, I_{OUT} = 20 A		3.6		A
	No load input current	V_{IN} = 12 V, I_{OUT} = 0 A		60		mA
$V_{IN(start)}$	V_{IN} start voltage			7		V
$V_{IN(stop)}$	V_{IN} stop voltage			5		V
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage	V_{IN} = 12 V, I_{OUT} = 20 A	1.08	1.2	1.32	V
	Line regulation	8 ≤ V_{IN} ≤ 14 V, I_{OUT} = 20 A			0.5%	
	Load regulation	V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 20 A			0.5%	
Vout_ripple	Output ripple voltage	V_{IN} = 12 V, I_{OUT} = 20 A			50	mV_{P-P}
Iout	Output current	8 ≤ V_{IN} ≤ 14	0		20	A
I_{OCP}	Output over current inception point	V_{IN} = 12 V	21	25	29	A
SS	Soft-start time	(default)		2.8		ms
	Transient response					
ΔI	Load step	10 A ≤ I_{OUT} ≤ 20 A		10		A
	Load slew rate			1		A/μS
	Overshoot			120		mV
	Settling time			20		μs
SYSTEM CHARACTERISTICS						
f_{SW}	Switching frequency			300		kHz
η_{PK}	Peak efficiency	V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 20 A		90%		
η	Full load efficiency	V_{IN} = 12 V, I_{OUT} = 20 A		85%		
T_{OPER}	Operating temperature range	8 ≤ V_{IN} ≤ 14 V, 0 A ≤ I_{OUT} ≤ 20 A	–40		60	°C

Design Procedure

The following design example is for an output of 1.2 V at 20-A maximum, with an input range of 8 V to 14 V.

Selecting a Switching Frequency

This design example is calculated for a switching frequency of 300 kHz to improve efficiency. The switching frequency can be changed with the Fusion GUI, but some components may need to be revised at other switching frequencies.

Output Inductor, L_{OUT}

The output inductor value is determined by the peak-to-peak ripple at high line, and in this case a value of 30% of output current maximum is used.

$$L_{OUT} = \frac{V_{IN(max)} - V_{OUT}}{0.3 \times I_{OUT}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} = \frac{14 - 1.2}{0.3 \times 20} \times \frac{1}{300\,kHz} = 610\,nH \quad (36)$$

Copyright © 2011, Texas Instruments Incorporated

For this design a 750-nH inductor from Pulse (PG0077.801) was selected. The actual ripple current should now be recalculated using the actual inductance value.

$$I_{RIPPLE} = di = dt \times \frac{V_L}{L} = 3.05\,\mu \times \frac{1.2}{0.75\,\mu} = 4.88\,A_{P-P} \tag{37}$$

With this ripple current, the inductor RMS and peak current values can be calculated.

The RMS value of a zero-average triangular wave is given by Equation 38.

$$I_{RMS} = \sqrt{(I_{DC})^2 + (I_{AC})^2} = \sqrt{(20)^2 + \left(\frac{4.88}{\sqrt{12}}\right)^2} = 20.05\,A_{RMS} \tag{38}$$

At maximum load and maximum line, the peak inductor current is given by Equation 39.

$$I_{PEAK} = I_{DC} + \frac{I_{P-P}}{2} = 20 + \frac{4.88}{2} = 22.44\,A_{PEAK} \tag{39}$$

The DCR of the selected inductor (from the data sheet) is 1.2 mΩ. Inductor conduction losses are described in Equation 40.

$$P = I^2 \times R = (I_{RMS})^2 \times DCR = (20.05)^2 \times 1.2\,m\Omega = 0.482\,W \tag{40}$$

Output Capacitance, C_{OUT}

The selection of the output capacitor is typically affected by the output transient response requirement. Equation 41 and Equation 42 can be used to over-estimate the voltage deviation to account for delays in the loop bandwidth and can be used to determine the required output capacitance. The estimate of C_{OUT} based on overshoot is shown in Equation 41.

$$V_{OVERSHOOT} < \frac{\Delta I_{OUT}}{C_{OUT}} \times \Delta t = \frac{\Delta I_{OUT}}{C_{OUT}} \times \frac{\Delta I_{OUT} \times L_O}{V_{OUT}} = \frac{(\Delta I_{OUT})^2 \times L_O}{V_{OUT} \times C_{OUT}} \tag{41}$$

The estimate of C_{OUT} based on undershoot is shown in Equation 42.

$$V_{UNDERSHOOT} < \frac{\Delta I_{OUT}}{C_{OUT}} \times \Delta t = \frac{\Delta I_{OUT}}{C_{OUT}} \times \frac{\Delta I_{OUT} \times L_O}{(V_{IN} - V_{OUT})} = \frac{(\Delta I_{OUT})^2 \times L_O}{(V_{IN} - V_{OUT}) \times C_{OUT}} \tag{42}$$

When $V_{IN(min)} > 2 \times V_{OUT}$, use the overshoot equation ($V_{Overshoot}$) to calculate minimum output capacitance. When $V_{IN(min)} < 2 \times V_{OUT}$ use the undershoot equation ($V_{Undershoot}$). In this design example, $V_{IN(min)}$ is much larger than $2 \times V_{OUT}$ so Equation 43 is used to determine the required minimum output capacitance.

$$C_{OUT} = \frac{(\Delta I_{OUT})^2 \times L_{OUT}}{V_{OUT} \times V_{OVERSHOOT}} = \frac{(10)^2 \times 750\,nH}{1.2 \times 120\,mV} = 520\,\mu F \tag{43}$$

The Resistive Component of Output Ripple

With a minimum capacitance, the maximum allowable ESR is determined by the maximum ripple voltage and is approximated by Equation 44.

$$ESR_{MAX} = \frac{V_{SPEC} - V_{RIPPLE(cap)}}{I_{RIPPLE}} = \frac{V_{SPEC} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}} = \frac{50\,mV - \left(\frac{4.88}{8 \times 521\,\mu F \times 300\,kHz}\right)}{4.88} = 9.45\,m\Omega \tag{44}$$

The factor of 8 in the equation above results from the calculation of capacitor voltage resulting from a triangular current. For this design, a 680-µF, 45-mΩ ESR, 5-nH ESL tantalum and two, 47-µF, 3-mΩ ESR, 0.9-nH ESL ceramic capacitors were selected for a total capacitance of 780 µF.

Copyright © 2011, Texas Instruments Incorporated

Peak Current Rating of the Inductor

With the output capacitance known, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is shown in Equation 45 and the resulting peak inductor current is shown in Equation 46 .

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{t_{SS}} = \frac{1.2 \times (680\,\mu + 2 \times 47\,\mu)}{3.1\,m} = 0.3\,A \quad (45)$$

$$I_{L1(peak)} = I_{OUT(max)} + \left(\frac{I_{RIPPLE}}{2}\right) + I_{CHARGE} = 20 + \left(\frac{4.88}{2}\right) + 0.3 = 23.04\,A \quad (46)$$

Input Capacitance, C_{IN}

The input capacitor is selected to limit the input ripple voltage to 20% or less of V_{IN}. The ripple voltage is due to the current flowing in the input capacitor's ESR as well as capacitance charging and discharging. To simplify the calculations, an infinitely large series input inductance is assumed. With an infinite inductor, the input capacitor current is calculated to be 5.6 Arms.

For reasons of availability, consider the capacitor EEVFC1E331P, which is an electrolytic, 330-µF, 25-V capacitor with 150-mΩ of ESR and 100-nH ESL. This capacitor has an rms current rating of 670 mA. With the calculated rms value of the capacitor current of 5.6 Arms, this implies that needs to be additional capacitance with a much lower ESR across the input bus in order to divert most of the AC current to this low ESR capacitor.

Another readily available capacitor is selected. A 22-µF, ceramic, 25-V, 10-mΩ ESR, 0.9-nH ESL device, two in parallel. With these capacitors in parallel, the ripple in the electrolytic is well within its rating with a value of 329 mA_{rms}.

Switching MOSFETs, Q_{HS} and Q_{LS}

The high-side and low-side FETs, Q_{HS} and Q_{LS}, are selected based on several factors including:

- Vds, the drain to source voltage rating. This design requires a 25-V device
- Vgs, the gate to source voltage rating. For the TPS40400 this voltage is 6.5 V
- Conduction losses, based on $I^2 \times R_{DS(on)}$
- Gate charge, must be low enough to be driven by the PWM controller

These devices are selected:

LOCATION	PART NUMBER	VOLTAGE RATING (V)	$R_{DS(on)}$ (mΩ)	GATE CHARGE Q_G(nC)	QTY
High-side	CSD16404Q5A	25	4.1	8	1
Low-side	CSD16325Q5	25	1.7	25	2

Since the selected FETs are very fast, the controller is programmed to have the shorter dead-time of 25 ns.

General Component Selection

Refer to the schematic in Figure 21 for device reference designators and connections for the TPS40400 Design Example 1.

Copyright © 2011, Texas Instruments Incorporated

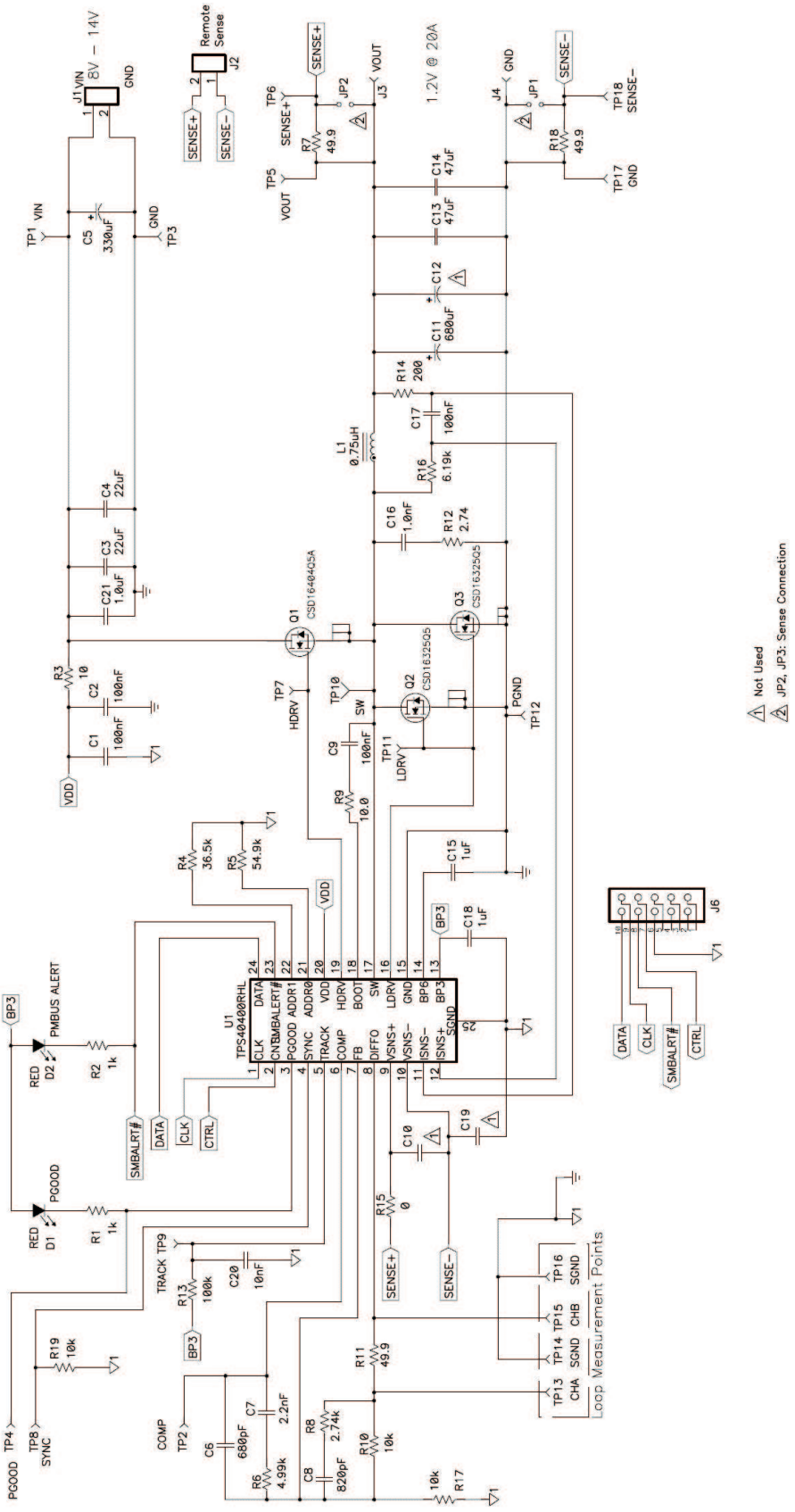


Figure 21. Schematic

Device Addressing, R_{ADDR0} and R_{ADDR1}

The PMBus address for the device must be read from the ADDR0 and ADDR1 pins. Each pin has an internal fixed current source and the resulting developed voltage is read and converted to the desired device address. The external resistors R_{ADDR0} and R_{ADDR1} from the address pins to ground set eight possible states for a total of 64 possible addresses. The address states are determined by voltages on the address pins per Table 4.

Table 4. Address Configuration

DIGIT	RESISTANCE (kΩ)
0	10
1	15.4
2	23.7
3	36.5
4	54.9
5	84.5
6	130
7	200

For this design, the address of 34 octal, or 28 decimal is selected arbitrarily. In order to achieve this address, the ADDR0 resistor R5 would be 54.9 kΩ and the ADDR1 resistor R4 would be 36.5 kΩ.

Current Sense FIter, R16 and C17

Current sensing for the TPS40400 is typically done by sensing the voltage drop across the output inductor's (L1) DC resistance. In order to do this, the large AC switching voltage forced across L1 must be filtered out so that the measured voltage is only the DC drop. This is done by placing an R-C filter directly across the output choke (high-frequency filter) L1. The R-C combination is chosen such that it provides enough filtering for the application and the time constant is chosen to match that of the output inductor and its ESR, which is shown in Equation 47.

$$\tau = \frac{L1}{DCR} \tag{47}$$

Usually a capacitor value is chosen between 10 nF and 1 µF for this location. A value of 100 nF is arbitrarily chosen, which yields Equation 48.

$$R16 = \frac{L1}{DCR} \times \frac{1}{C} = \frac{750\,nH}{1.2\,m\Omega \times 100\,nF} = 6.25\,k\Omega \tag{48}$$

Choose a standard value of 6.19 kΩ.

The capacitor C17 should be placed as close to the ISNS+ and ISNS– pins as possible to provide good bypass filtering. R16 should be placed close to the inductor to prevent traces with the switch node voltage from being propagated across the PCB and getting close to sensitive pins of the TPS40400.

Voltage Decoupling Capacitors, C_{BP3}, C_{BP6}, and C_{VDD}

Three pins on the TPS40400 have DC bias voltages. It is necessary to add small decoupling capacitors to these pins. Table 5 shows the recommended minimum values.

Table 5. Voltage Decoupling Capacitor Values

DEVICE LOCATION	RECOMMENDED MINIMUM VALUE	FUNCTION	SELECTED VALUE
C_{BP3}, (C18)	0.1-µF low ESR	V_{CC} for internal controls of the device	1-µF ceramic
C_{BP6}, (C15)	1-µF low ESR	V_{CC} for gate drivers	1-µF ceramic
C_{VDD}, (C1) and (C2)	0.1-µF low ESR	V_{CC} for input power to the device	2 x 100 nF, with additional series 10-Ω filter resistor R3 to filter out switching noise from the power FETs

Copyright © 2011, Texas Instruments Incorporated

Bootstrap Capacitor, C9

Selection of the bootstrap capacitor is based on the total gate charge of the high-side FET and the allowable ripple on the BOOT pin. A ripple of 0.2 V is chosen as maximum for this design. This yields a value described in Equation 49.

$$C_{BOOT} = C9 \geq \frac{Q_{GHS}}{V_{BOOT(ripple)}} \times \frac{8\,nC}{0.2\,V} = 40\,nF \tag{49}$$

Choose a standard value of 100 nF. Additionally, a series resistor R9 is added in order to reducing the turn-on speed of the high-side FET, Q1.

Snubber R12 and C16

For this design, the snubber function is designed based on an allowable snubber power dissipation. A target value of between 0.25% and 0.5% of the rated output power (P_{OUT}) is used as the starting point for the calculation of the snubber values. Once the snubber values are determined and real hardware is obtained, the snubber values can be adjusted to achieve better results.

$$\frac{Energy}{seconds} = \frac{E}{cycle} \times f_{SW} = 2(events) \times \frac{1}{2} \times C \times V^2 \times 300\,kHz \tag{50}$$

$$C = \frac{60\,mW}{V^2 \times 300\,kHz} = \frac{60\,mW}{196 \times 300\,kHz} = 1.02\,nF \tag{51}$$

$$R = \frac{\frac{Shortest\ Pulse\ Width}{10}}{5 \times C} = \frac{28.6\,n}{5 \times C} = \frac{28.6\,n}{5 \times 1\,n} = 5.72\,\Omega \tag{52}$$

Loop Compensaton Components

Using the Texas Instruments SwitcherPro™ design tool and the resulting plant (system) bode plot, a crossover frequency of 20 kHz is selected with 45° of phase margin. The resulting compensation components are listed in Table 6.

Table 6. Deisgn Example 1 Component Summary

COMPONENT LOCATION	VALUE
R6	4.99 kΩ
R8	2.74 kΩ
C6	680 pF
C7	2.2 nF
C8	820 pF

Output Voltage Set Point, R_{BIAS}

The output voltage can be set by choosing and calculating R1 and R_{BIAS} . The V_{OUT} set point is shown in Equation 53.

$$R_{BIAS} = \frac{V_{REF} \times R1}{V_{OUT} - V_{REF}} \tag{53}$$

In this design R1 was chosen to be 10 kΩ. R_{BIAS} is calculated to be 10 kΩ.

Copyright © 2011, Texas Instruments Incorporated

Remote Sensing

Remote sensing can be accomplished with the differential amplifier as shown in Figure 22. Resistors RS1 and RS2 (R7 and R18 in the schematic above) are used if the sense connections fail or get damaged. The values of RS1 and RS2 are bound by an upper value such that the voltage drop across them does not introduce appreciable voltage regulation error from the bias current, and a lower value such that the voltage drop in the load wires which appears across these resistors does not dissipate appreciable power. Values between 10 Ω to 50 Ω are usually chosen.

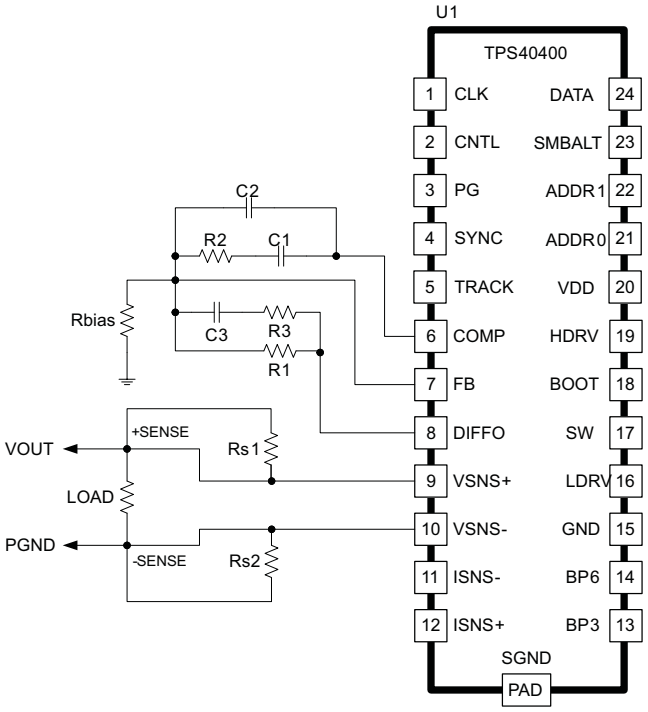


Figure 22. Remote Sense Schematic

Copyright © 2011, Texas Instruments Incorporated

Typical Performance Characteristics

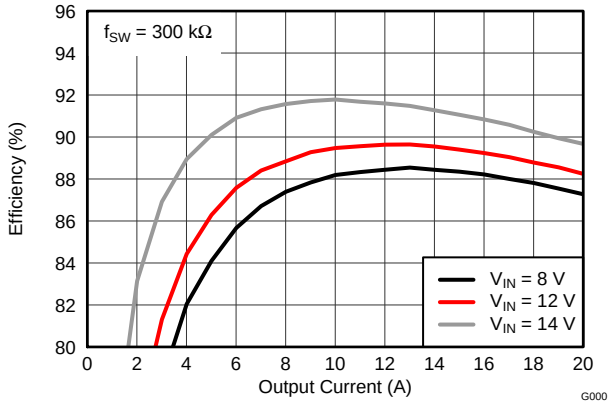


Figure 23. Efficiency

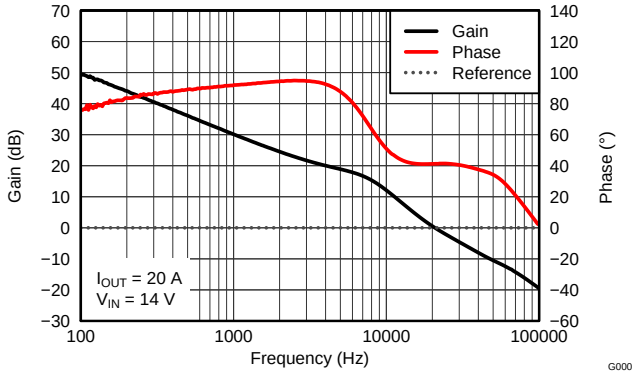


Figure 24. Plant (System) Bode

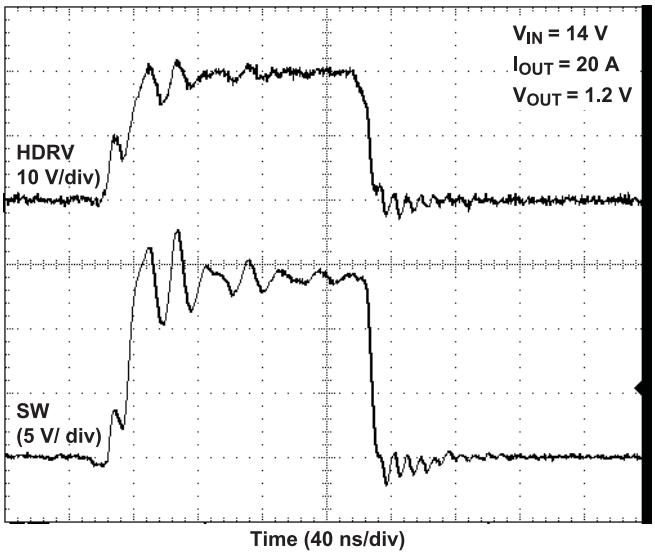


Figure 25. Switching Waveform

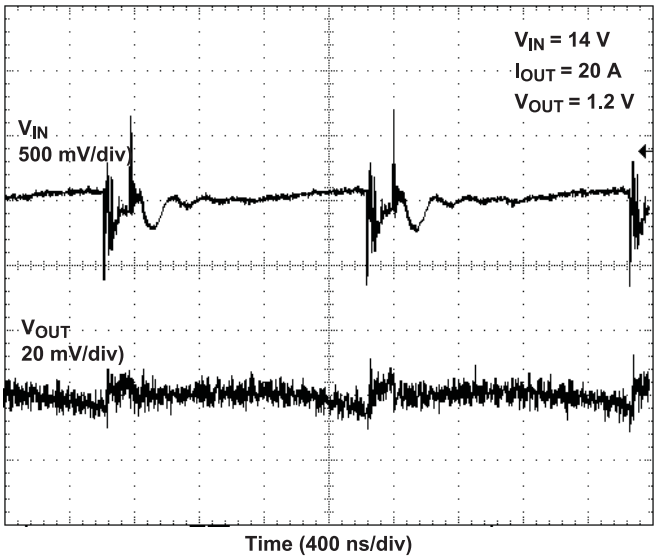


Figure 26. Ripple Waveform

Copyright © 2011, Texas Instruments Incorporated

Design Example 1 List of Materials

Table 7 lists of materials for Design Example 1.

Table 7. List of Materials

REFERENCE DESIGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
C1, C2, C9, C17	4	100 nF	Ceramic, 25 V, X7R, 10%	0603	Std	Std
C11	1	680 µF	Tantalum, 6.3 V, 10%	7343 (D)	TPSE687K006R0045	AVX
C13, C14	2	47 µF	Ceramic, 6.3 V, X7R, 10%	1210	Std	Std
C15, C18	2	1 µF	Ceramic, 16 V, X7R, 10%	0805	Std	Std
C16	1	1.0 nF	Ceramic, 25 V, X7R, 10%	0603	Std	Std
C20	1	10 nF	Ceramic, 50 V, X7R, 10%	0603	Std	Std
C21	1	1.0 µF	Ceramic, 25 V, X7R, 10%	1206	Std	Std
C3, C4	2	22 µF	Ceramic, 25 V, X7R, 10%	1210	Std	Std
C5	1	330 µF	Aluminum, 25 V, 150 mΩ, FC series	10 mm x 12 mm	EEVFC1E331P	Panasonic
C6	1	680 pF	Ceramic, 50 V, X7R, 10%	0603	Std	Std
C7	1	2.2 nF	Ceramic, 50 V, X7R, 10%	0603	Std	Std
C8	1	820 pF	Ceramic, 50 V, X7R, 10%	0603	Std	Std
D1, D2	2	RED	LED, Red, 20-mA, 6-mcd	0603	LTST-C190CKT	Lite On
J1, J2	2	D120/2DS	Terminal block, 2-pin, 15-A, 5.1mm	0.40 inch x 0.35 inch	ED120/2DS	On Shore Technology
J3, J4	2	L35	Type L - copper single conductor, one-hole mount	0.813 inch x 0.375 inch	L35	Thomas and Betts
J6	1	86479-3	Male right angle 2 x 5-pin, 100mil spacing	0.607 inch x 0.484 inch	86479-3	AMP
JP1, JP2	2	PEC02SAAN	Header, 2-pin, 100 mil Spacing	0.100 inch x 2	PEC02SAAN	Sullins
L1	1	0.75 µH	Inductor, SMT, 0.75 µH, 1.2 mΩ, 31A	0.512 x 0.571 inch	PG0077.801	Pulse
Q1	1	CSD16404Q5A	MOSFET, N-channel, 25 V, 20 A, 4.1 mΩ	QFN5X6mm	CSD16404Q5A	TI
Q2, Q3	2	CSD16325Q5	MOSFET, N-channel, 25 V, 33 A, 1.7 mΩ	QFN-8 POWER	CSD16325Q5	TI
R1, R2	2	1 kΩ	Resistor, 1/16-W, 5%	0603	Std	Std
R10, R17, R19	3	10 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
R12	1	2.74 kΩ	Resistor, 1/8W, 1%	1206	Std	Std
R13	1	100 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
R14	1	200 Ω	Resistor, 1/16W, 1%	0603	Std	Std
R15	1	0 Ω	Resistor, 1/16W, 1%	0603	Std	Std
R16	1	6.19 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
R3, R9	2	10 Ω	Resistor, 1/16W, 1%	0603	Std	Std
R4	1	36.5 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
R5	1	54.9 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
R6	1	4.99 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
R7, R11, R18	3	49.9 Ω	Resistor, 1/16W, 1%	0603	Std	Std
R8	1	2.74 kΩ	Resistor, 1/16W, 1%	0603	Std	Std
U1	1	TPS40400RHL	3.0 V to 20 V PMBus synchronous buck controller	QFN-24	TPS40400RHL	TI

Copyright © 2011, Texas Instruments Incorporated

Internal Configuration

Internal configuration of the TPS40400 is handled via the PMBus (pins CLK and DATA) and the Fusion Digital Power Designer (GUI interface). An example of the configuration window that is used to make internal configuration changes to the TSP40400 is shown below in Figure 27.

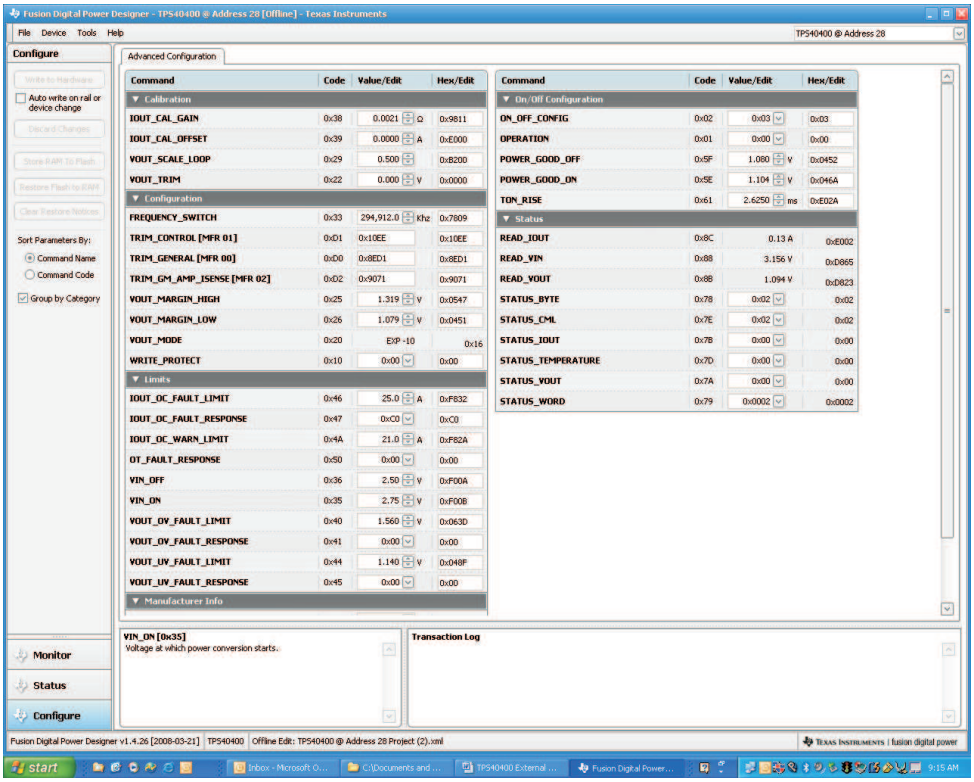


Figure 27. Advanced Configuration Window

Figure 27 shows are the user changeable parameters of the TPS40400 and these consist of the following sections.

- Calibration
- Configuration
- Limits
- On/Off Configuration

The status section is read only, and consists of data read from the TPS40400 such as V_{OUT}, I_{OUT}, V_{IN}, and status words. A full description of each command and status word is available in the SUPPORTED COMMANDS section of the TPS40400 datasheet.

Copyright © 2011, Texas Instruments Incorporated

Configuration changes can be implemented by changing the value in the **Value/Edit** box of each parameter. Most boxes allow direct parameter changes such as voltage or current, but some boxes such as **IOUT_OC_FAULT_RESPONSE** provide a pop-up configuration window as shown in Figure 28, and others provide a pull-down menu. Select the appropriate radio buttons to make the desired changes.

To implement the changes to the device, click on the [Write to Hardware] button. This stores the changes to the device in volatile memory, so these changes are lost when input power is cycled. To permanently make changes and commit those changes to non-volatile memory, click on the [Store RAM to Flash] button.

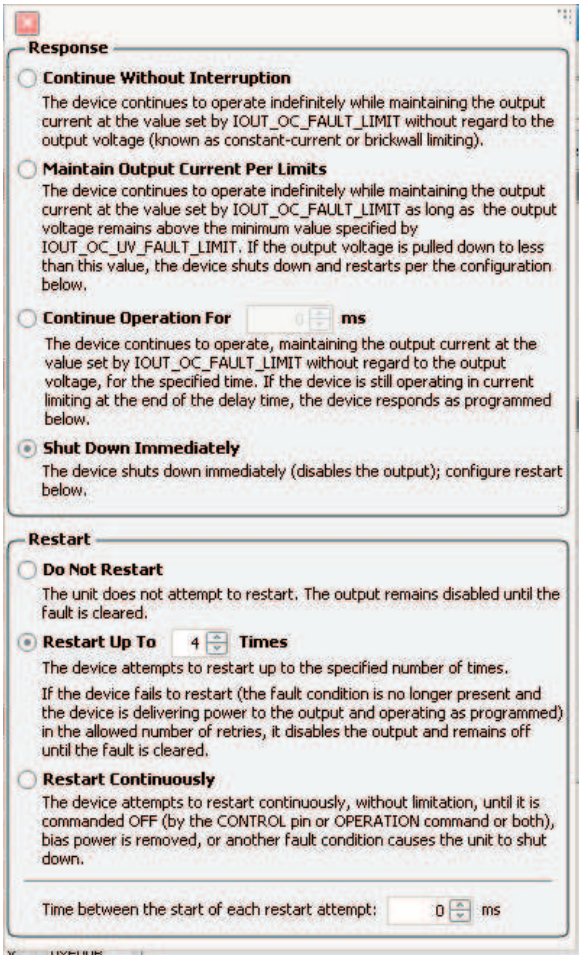


Figure 28. IOUT_OC_FAULT_RESPONE Configuration Window

Copyright © 2011, Texas Instruments Incorporated

Design Example 2: 12-V Input, 5-V Output, 5-A (max) Output Current

Design Example 2 Parameters

The following example illustrates the design process and component selection for a synchronous buck converter using the TPS40400 controller. The design goal parameters are listed in Table 8.

Table 8. Design Example 2 Electrical Parameters

PARAMETER		NOTES AND CONDITIONS	MIN	NOM	MAX	UNITS
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		8	12	14	V
I_{IN}	Input current	V_{IN} = 8 V, I_{OUT} = 5 A		3.5		A
	No load input current	V_{IN} = 12 V, I_{OUT} = 0 A		60		mA
$V_{IN(start)}$	V_{IN} start voltage			7		V
$V_{IN(stop)}$	V_{IN} stop voltage			6		V
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage	V_{IN} = 12 V, I_{OUT} = 5 A	4.75	5.00	5.25	V
	Line regulation	8 ≤ V_{IN} ≤,14 V, I_{OUT} = 5 A			0.5%	
	Load regulation	V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 5 A			0.5%	
Vout_ripple	Output ripple voltage	V_{IN} = 12 V, I_{OUT} = 5 A			50	mV_{P-P}
Iout	Output current	8 ≤ V_{IN} ≤ 14	0		5	A
I_{OCP}	Output over current inception point	V_{IN} = 12 V	6.7	8.0	9.3	A
SS	Soft-start time	(default)		5		ms
	Transient response					
ΔI	Load step	2 A ≤ I_{OUT} ≤ 5 A		3		A
	Load slew rate			1		A/µS
	Overshoot			500		mV
	Settling time			50		µs
SYSTEM CHARACTERISTICS						
f_{SW}	Switching frequency			300		kHz
η_{PK}	Peak efficiency	V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 5 A		90%		
η	Full load efficiency	V_{IN} = 12 V, I_{OUT} = 5 A		85%		
T_{OPER}	Operating temperature range	8 ≤ V_{IN} ≤ 14 V, 0 A ≤ I_{OUT} ≤ 5 A	–40		60	°C

Copyright © 2011, Texas Instruments Incorporated

General Component Selection

Refer to the schematic below for device reference designators and connections.

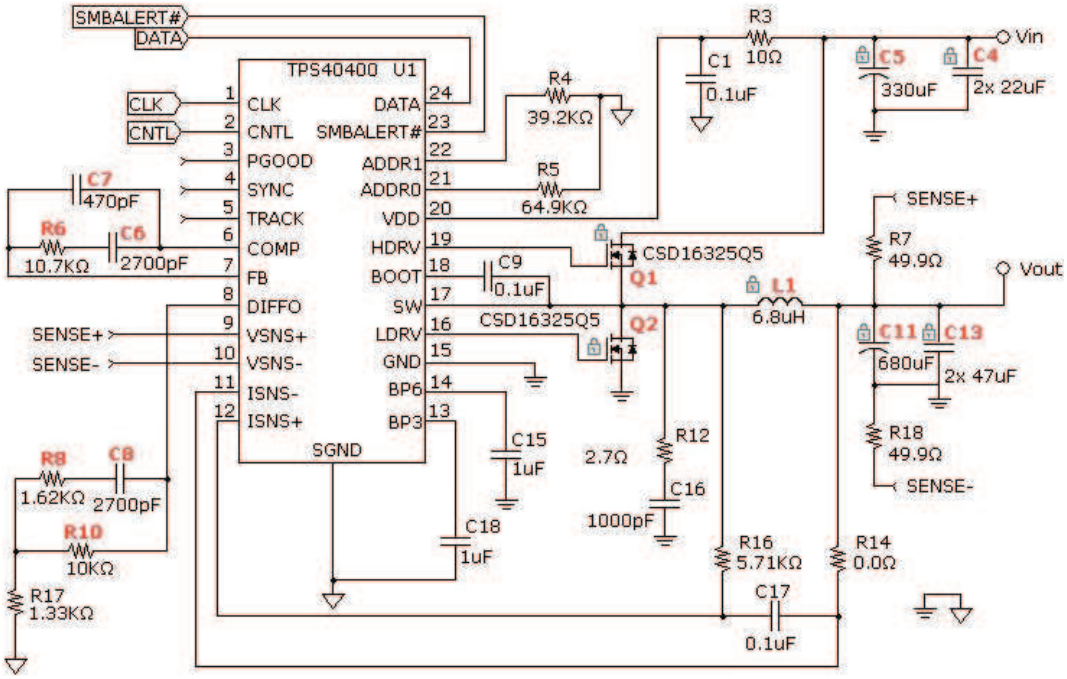


Figure 29. Design Example 2 Schematic

Copyright © 2011, Texas Instruments Incorporated

Design Example 2 List of Materials

Table 9 lists of materials for Design Example 2.

Table 9. Design Example 2 List of Materials

REFERENCE DESIGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
C1, C2, C9, C17	4	0.1 µF	Ceramic, X7R, 25 V, 20%	0603	Standard	Standard
C3, C4	2	22 µF	Ceramic, X7R, 25 V, 10%	1210	Standard	Standard
C5	1	330 µF	Aluminum, 25 V, 20%	10x12mm	EEVFC1E331P	Panasonic
C6	1	2700 pF	Ceramic, X7R, 10 V, 20%	0603	Standard	Standard
C7	1	470 pF	Ceramic, X7R, 10 V, 20%	0603	Standard	Standard
C8	1	2700 pF	Ceramic, X7R, 10 V, 20%	0603	Standard	Standard
C11	1	680 µF	Tantalum, 6.3 V, 20%	7343 (D)	TPSE6870060045	Standard
C13, C14	2	47 µF	Ceramic, X7R, 6.3 V, 20%	1210	GRM32ER60J476M	Standard
C15, C18	2	1 µF	Ceramic, X7R, 16 V, 20%	0603	Standard	Standard
C16	1	1000 pF	Ceramic, X7R, 25 V, 20%	0603	Standard	Standard
L1	1	6.8 µH	Inductor, 6.8 µH, 12 mΩ		PF0553.682NL	Pulse
Q1	1	CSD16325Q5	Transistor, N-channel FET, 25 V, 100 A, 10 Ω	QFN 5x6	CSD16325Q5	TI
Q2	1	CSD16325Q5	Transistor, N-channel, 25 V, 100 A, 10 Ω	QFN 5x6	CSD16325Q5	TI
R3	1	10 Ω	Resistor, 1/16W, 5%	0603	Standard	Standard
R4	1	39.2 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
R5	1	64.9 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
R6	1	10.7 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
R7, R18	2	49.9 Ω	Resistor, 1/16W, 1%	0603	Standard	Standard
R8	1	1.62 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
R10	1	10 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
R12	1	2.7 Ω	Resistor, 1/16W, 5%	0603	Standard	Standard
R14	1	0.0 Ω	Resistor, 1/16W, 1%	0603	Standard	Standard
R16	1	5.71 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
R17	1	1.33 kΩ	Resistor, 1/16W, 1%	0603	Standard	Standard
U1	1	TPS40400	3.0V-20V PMBus synchronous buck controller	24-pin QFN	TPS40400RHL	Texas Instruments

Copyright © 2011, Texas Instruments Incorporated

Design Characterization

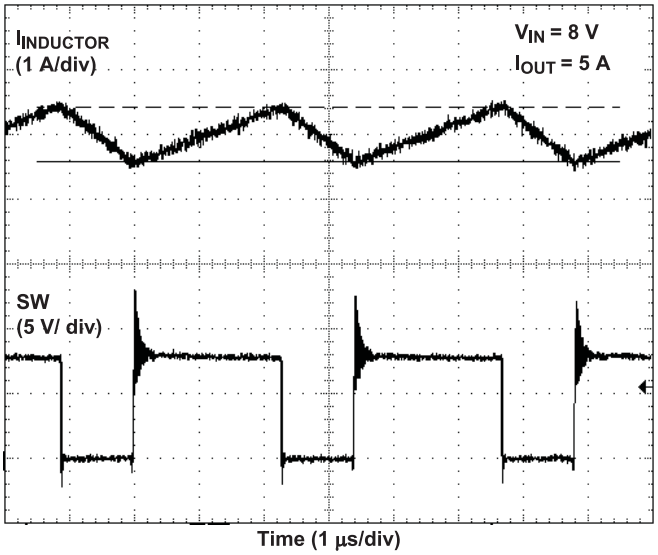


Figure 30. Switching Voltage and Inductor Current Waveform

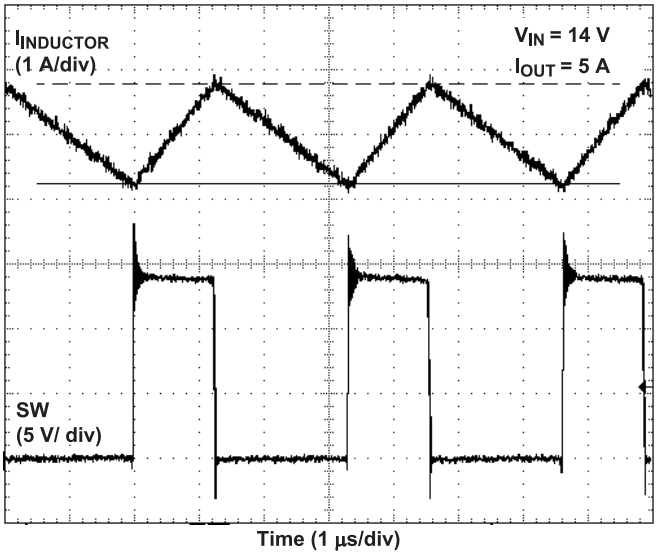


Figure 31. Switching Voltage and Inductor Current Waveform

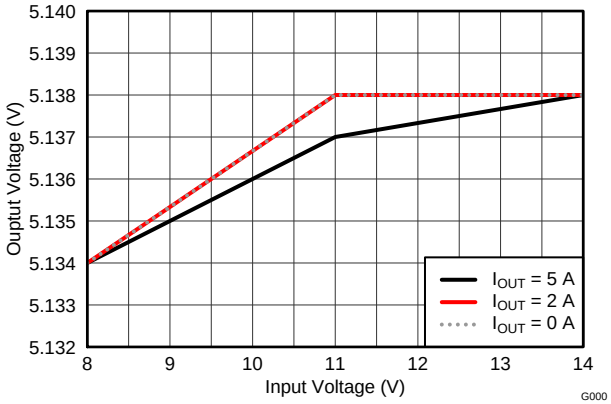


Figure 32. Design Example 2 Line Regulation

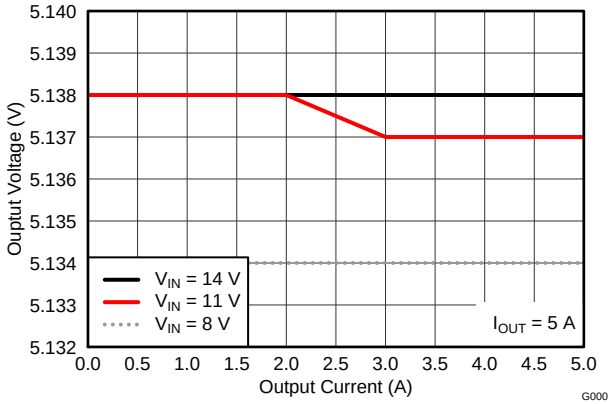


Figure 33. Design Example 2 Load Regulation

Copyright © 2011, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision A (JULY 2011) to Revision B	Page
• Changed corrected default values in ON_OFF_CONFIG table.	24
• Added Design Example 1	52
• Added Design Example 2	63

Copyright © 2011, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS40400RHLR	Active	Production	VQFN (RHL) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	40400
TPS40400RHLR.A	Active	Production	VQFN (RHL) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	40400
TPS40400RHLT	Active	Production	VQFN (RHL) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	40400
TPS40400RHLT.A	Active	Production	VQFN (RHL) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	40400
TPS40400RHLTG4	Active	Production	VQFN (RHL) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	40400
TPS40400RHLTG4.A	Active	Production	VQFN (RHL) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	40400

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

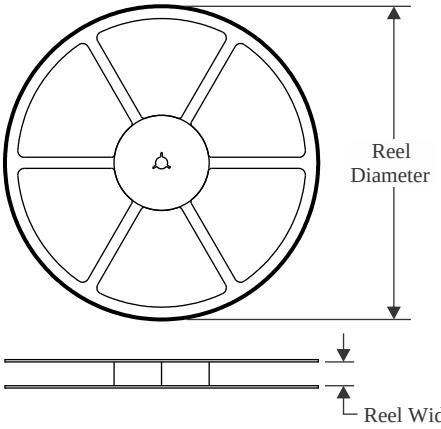
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

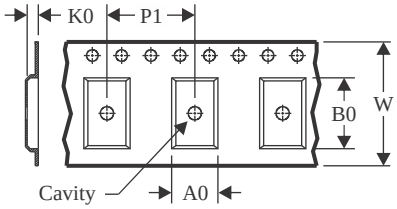
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

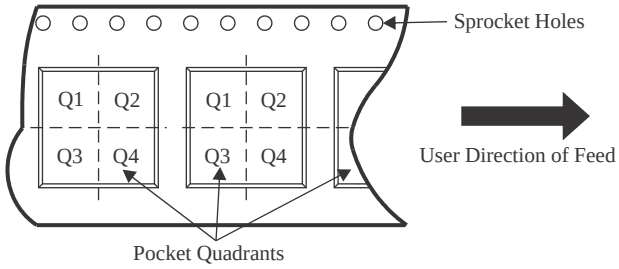


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

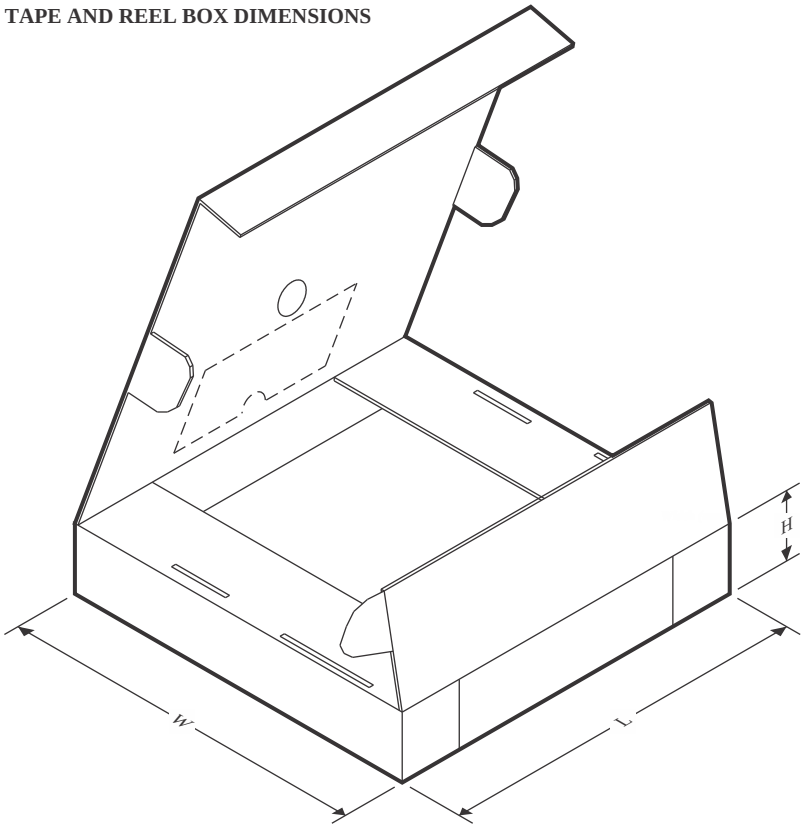
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

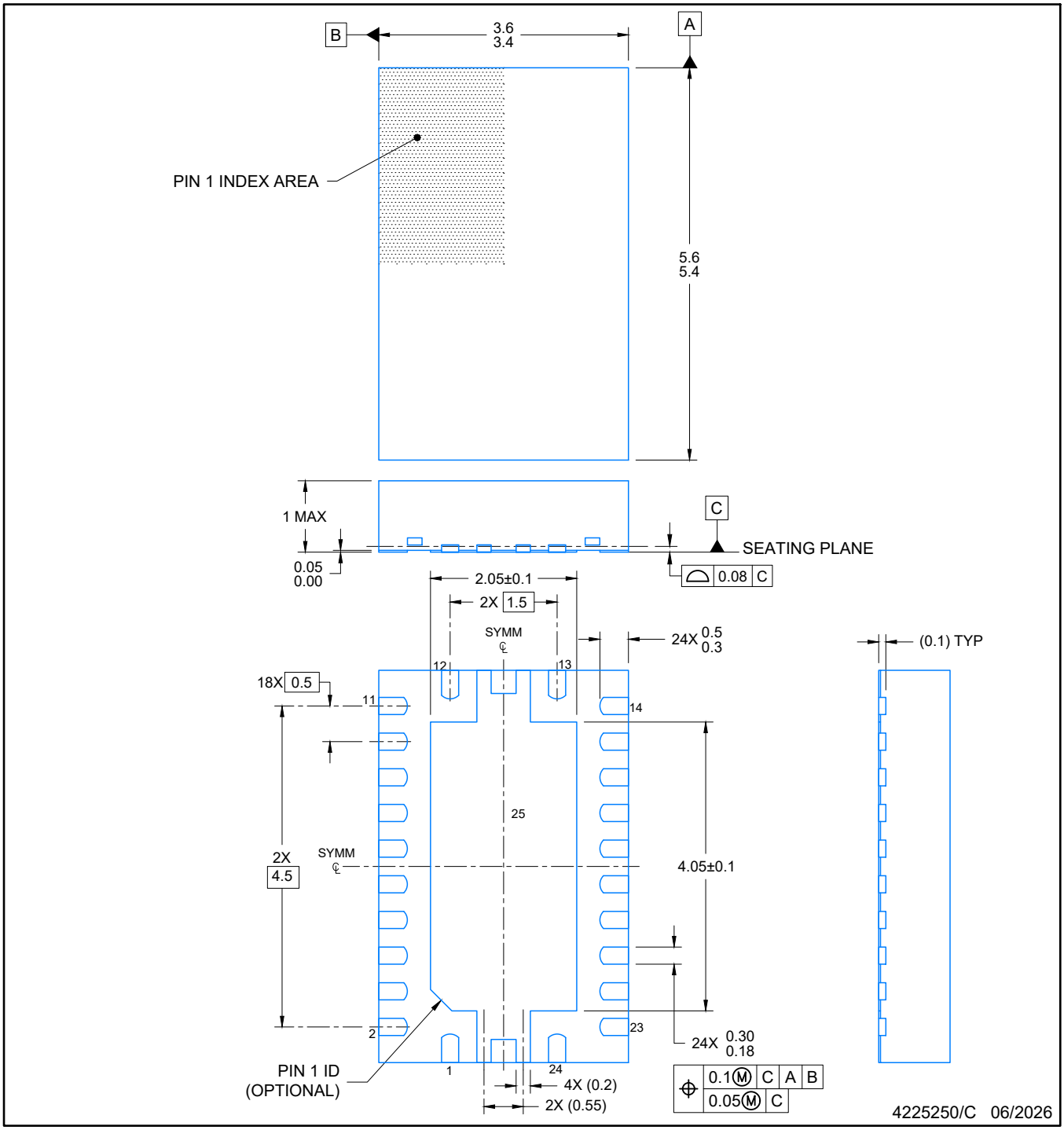
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40400RHLR	VQFN	RHL	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
TPS40400RHLT	VQFN	RHL	24	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
TPS40400RHLTG4	VQFN	RHL	24	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



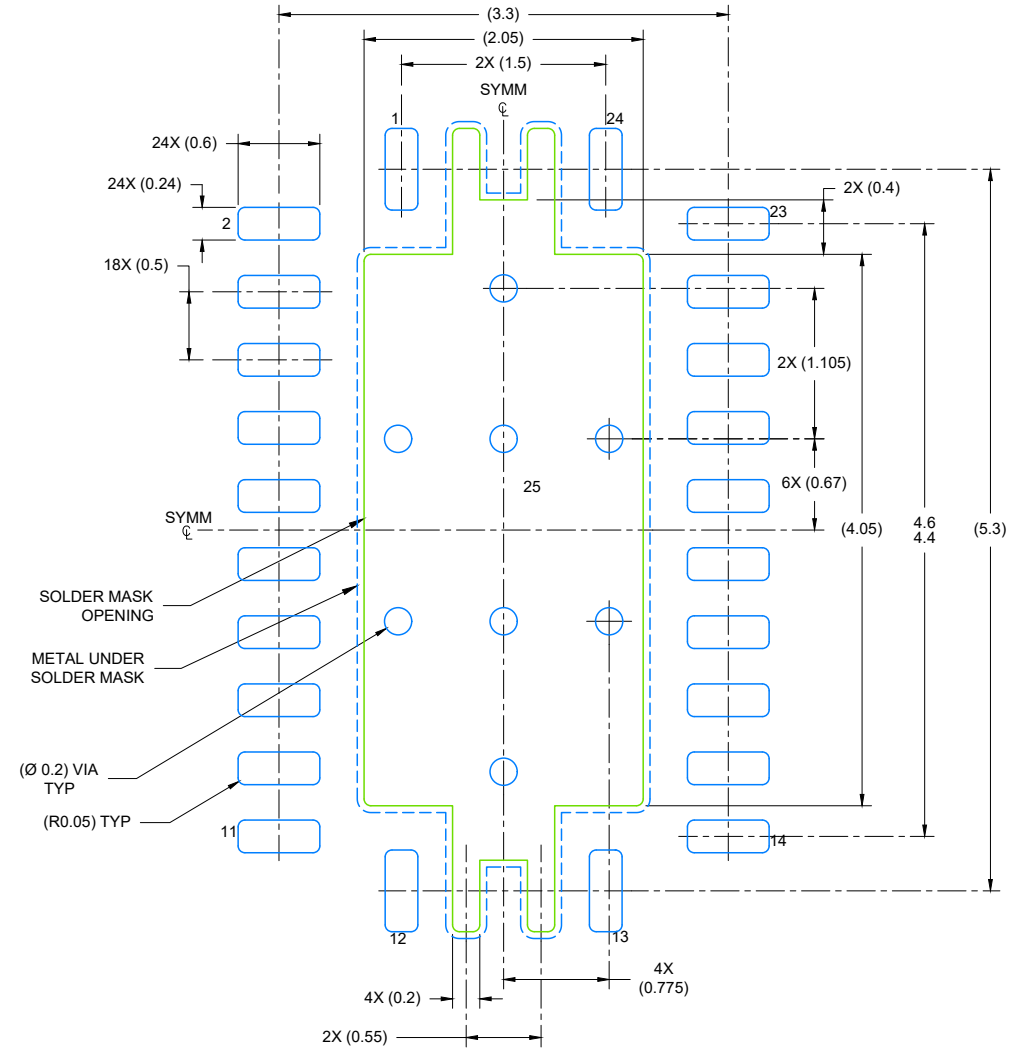
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40400RHLR	VQFN	RHL	24	3000	353.0	353.0	32.0
TPS40400RHLT	VQFN	RHL	24	250	213.0	191.0	35.0
TPS40400RHLTG4	VQFN	RHL	24	250	213.0	191.0	35.0

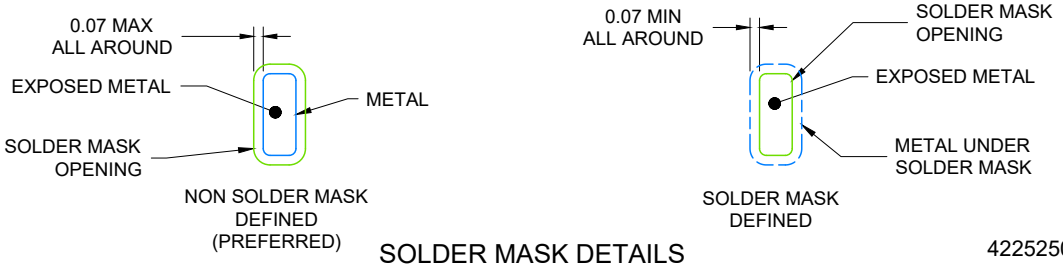


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

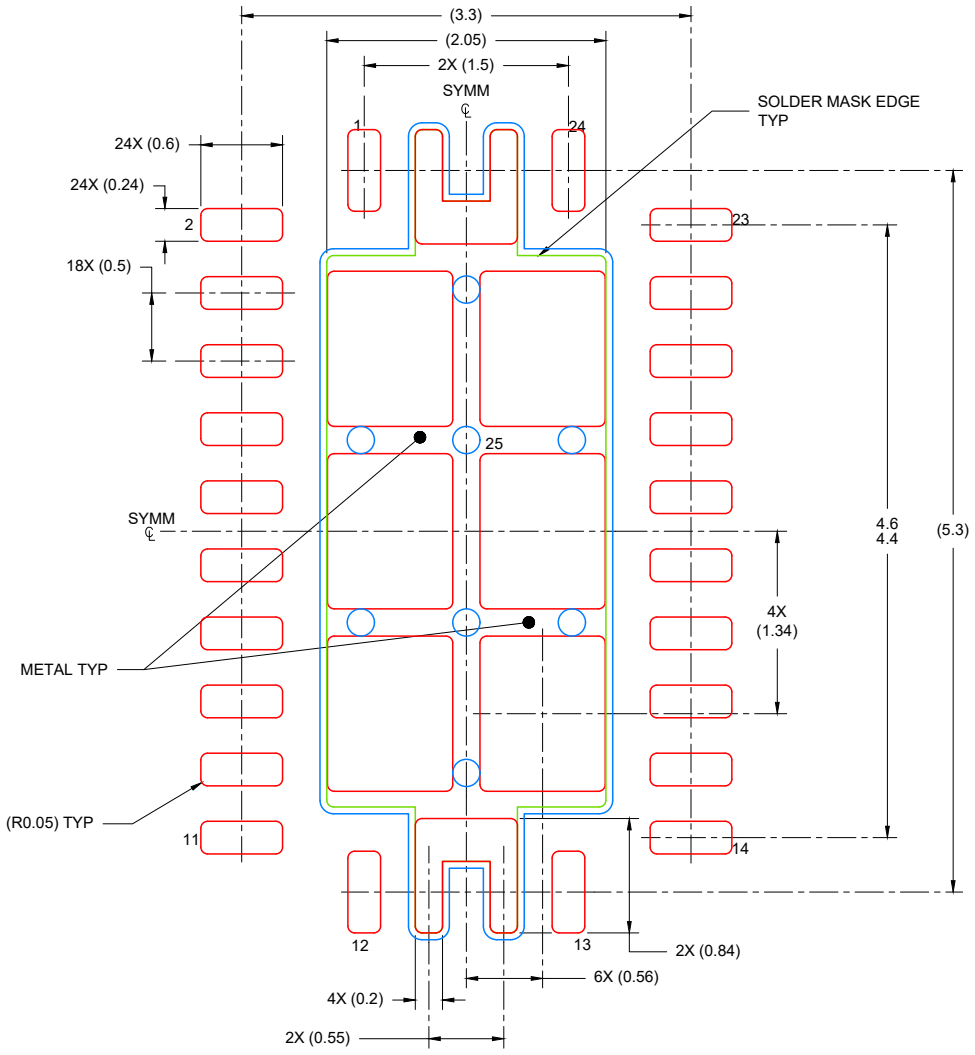


SOLDER MASK DETAILS

4225250/C 06/2026

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 18X

4225250/C 06/2026

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月