具有轻载效率优化的单相脉宽调制 (PWM) 控制器

特性

- **1.5V** 至 **19V** 转换电压范围
- **4.5V** 至 **14V** 电源电压范围
- 电压模式控制
- 针对效率优化的轻负载跳跃模式
- 高精度 **0.5%** 内部 **0.8V** 基准
- **0.8V** 至 **0.7 ×** V_{IN} 的可调输出电压
- 内部软启动
- 支持预偏置启动
- 支持软启动
- 从 **250kHz** 至 **1MHz** 的可编程开关频率
- 过流保护
- 针对过流的电感器直流电阻 **(DCR)** 感测
- 针对零电流检测的 $R_{DS(on)}$ 感测
- 过压和欠压保护
- 开漏电源正常输出
- 内部自举开关
- 由 **VCCDR** 供电的集成高电流驱动器
- 小型 **3 mm x 3 mm** 的 **16** 引脚四方扁平无引线 **(QFN)** 封装

应用范围

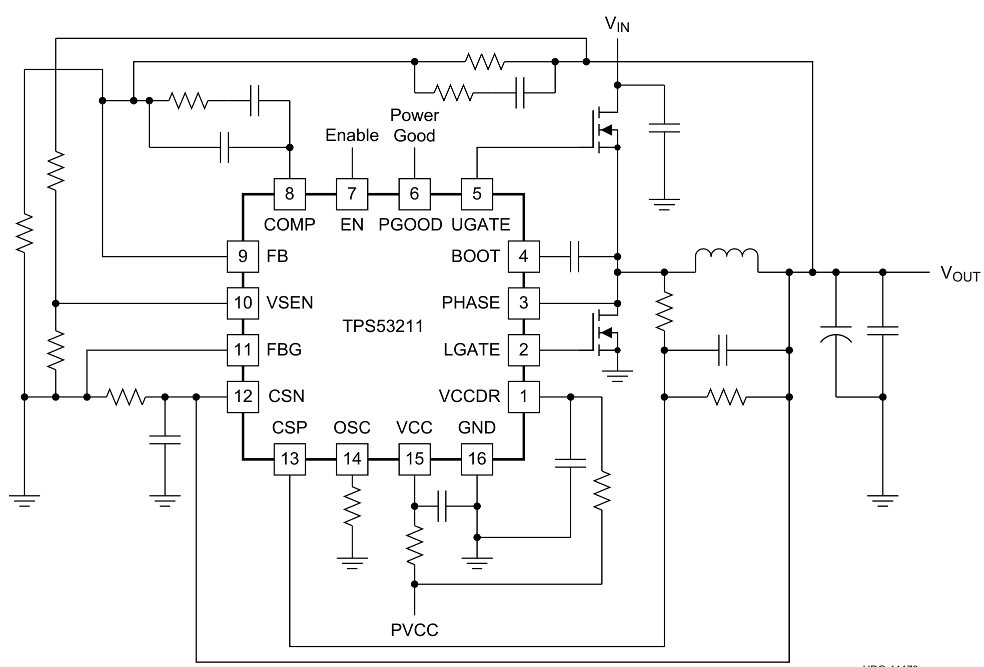
- 服务器和台式机子系统电源
- **DDR** 内存和端接电源
- 分布式电源
- 通用直流**/**直流转换器

描述

TPS53211 是一款具有集成高电流驱动器的单相位 PWM 控制器。 它用于 1.5V 到最高 19V 的转换电压。

TPS53211 特有一个跳跃模式解决方案，此解决方案在无需增加输出电压纹波的情况下可优化轻负载条件下的效率。 此器件提供预偏置启动，软停止，集成自举开关，电源正常功能，EN / 输入欠压闭锁 (UVLO) 保护。 它支持高达 19 V 的转换电压，以及 0.8V 至 0.7V × V_{IN} 的输出电压可调范围。

TPS53211 采用 3mm × 3mm，16 引脚，QFN 封装（符合绿色环保 RoHs 标准且无铅），并且可在 -40° C 到 85°C 的温度范围内额定运行。



English Data Sheet: SLUSAA9

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

TA	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ECO PLAN
–40°C to 85°C	Plastic QFN (RGT)	TPS53211RGTR	16	Tape and Reel	3000	Green (RoHS and no Pb/Br)
		TPS53211RGTT		Mini Reel	250	

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNITS
Input voltage range(2)	VCC, EN		–0.3	15	V
	VCCDR		–0.3	7.7	
	BOOT	dc	–0.3	36	
	BOOT to PHASE	dc	–0.3	7.7	
		transient < 200 ns	–5	7.7	
	PHASE	dc	–3	26	
		transient < 200 ns	–5	30	
	FB, VSEN, OSC		–0.3	3.6	
	CSP, CSN	V_{VCC} > 7.5 V	–0.7	6	
		V_{VCC} ≤ 7.5 V	–0.7	VCC-1.5	
Output voltage range(3)	UGATE		–0.3	36	V
	UGATE to PHASE, LGATE	dc	–0.3	7.7	
		transient < 200 ns	–5	7.7	
	COMP		–0.3	3.6	
	PGOOD		–0.3	15	
Ground pins	GND		–0.3	0.3	V
	FBG		–0.3	0.3	
Electrostatic discharge	Human Body Model (HBM)			1500	V
	Charged Device Model (CDM)			500	
Storage junction temperature			–55	150	°C
Operating junction temperature			–40	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the SW terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS53211 QFN 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	51.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	85.4	
θ_{JB}	Junction-to-board thermal resistance	20.1	
ψ_{JT}	Junction-to-top characterization parameter	1.3	
ψ_{JB}	Junction-to-board characterization parameter	19.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNITS
Input voltage range	VCC		4.5		14	V
	EN		–0.1		V_{VCC}+0.1	
	VCCDR		4.5		7	
	BOOT	dc	–0.1		34	
	BOOT to PHASE	dc	–0.1		7	
		transient < 200ns	–3		7	
	PHASE	dc	–1		24	
		transient < 200ns	–3		28	
	FB, VSEN, OSC		–0.1		3.3	
	CSP, CSN	V_{VCC} > 7.5 V	–0.1		5.5	
		V_{VCC} ≤ 7.5 V	–0.1		V_{VCC}–2	
Output voltage range	UGATE		–0.1		34	V
	UGATE to PHASE, LGATE	dc	–0.1		7	
		transient < 200 ns	–3		7	
	COMP		–0.1		3.3	
	PGOOD		–0.1		12	
Ground pins	GND		–0.1		0.1	
	FBG		–0.1		0.1	
Junction temperature range, T_J			–40		125	°C
Operating free-air temperature, T_A			–40		85	°C

ELECTRICAL CHARACTERISTICS(1)

over operating free-air temperature range, VCC = 12V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VCC}	VCC supply voltage	Nominal input voltage range	4.5		12	V
V_{POR}	VCC POR threshold	Ramp up; EN ='HI'	4.1	4.25	4.4	V
V_{PORHYS}	VCC POR hysteresis	VCCDR POR hysteresis		200		mV
I_{CC_STBY}	Standby current	EN pin is low. V_{VCC}= 12 V			60	µA
R_{Boot}	Rds(on) of the boot strap switch			10		Ω
DRIVER SUPPLY						
V_{CCDR}	VCCDR Supply voltage	Nominal input voltage range	4.5		7.0	V
V_{PORDR}	VCCDR POR threshold	Ramp up; EN ='HI'	3.15	3.32	3.50	V
$V_{PORHYSDR}$	VCCDR POR hysteresis	VCCDR POR hysteresis		220		mV
I_{CCDR_STBY}	Standby current	EN pin is low. V_{VCC} = 12 V			100	µA
REFERENCE						
V_{VREF}	VREF	Internal precision reference voltage		0.8		V
TOL_{VREF}	VREF tolerance	Close loop trim. 0°C ≤ T_J ≤ 70°C	–0.5%		0.5%	
ERROR AMPLIFIER						
UGBW(2)	Unity gain bandwidth		14			MHz
AOL(2)	Open loop gain		80			dB
$I_{FB(int)}$	FB Input leakage current	Sourced from FB pin		10		nA
$I_{EA(max)}$	Output sinking and sourcing current			2.5		mA
SR(2)	Slew rate			5		V/µs
ENABLE						
V_{ENH}	EN logic high		2.2			V
V_{ENL}	EN logic low				600	mV
I_{EN}	EN pin current				12	µA
SOFT START						
t_{SS_delay}	Delay after EN asserting	EN = 'HI' to "switching enabled"		$1024/f_{SW}$		ms
$t_{PGDELAY}$	PGOOD startup delay time	PG delay after soft-start begins		$1560/f_{SW}$		ms
RAMP						
	Ramp amplitude	4.5V < V_{VCC} < 12 V		2		V
PWM						
$t_{MIN(on)}$(2)	Minimum ON time		40			ns
D_{MAX}(2)	Maximum duty cycle	f_{SW} = 1 MHz	70%			
SWITCHING FREQUENCY						
$f_{SW(typ)}$	Typical switching frequency	R_{OSC} = 61.9 kΩ	360	400	440	kHz
$f_{SW(min)}$	Minumum switching frequency	R_{OSC} = 250 kΩ		250		kHz
$f_{SW(max)}$	Maximum switching frequency	R_{OSC} = 14 kΩ		1		MHz
$f_{SW(tol)}$	Switching frequency tolerance	R_{OSC} > 12.4 kΩ	–20%		20%	
OVERCURRENT						
V_{OC_TH}	CSP-CSN threshold for DCR sensing	T_A = 25°C	17	20	23	mV

(1) See PS pin description for levels.
(2) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS[1] (continued)

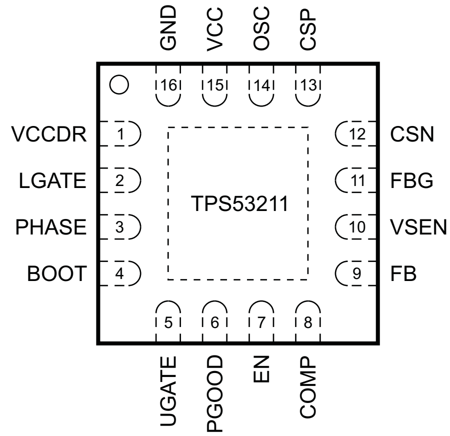
over operating free-air temperature range, VCC = 12V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVERS						
R_{HDHI} [3]	High-side driver sourcing resistance	(V_{BOOT} – V_{PH}) forced to 5 V, high state		1		Ω
R_{HDLO}	High-side driver sinking resistance	(V_{BOOT} – V_{PH}) forced to 5 V, low state		0.5		Ω
R_{LDHI}	Low-side driver sourcing resistance	(V_{CCDR}– GND) = 5 V, high state		0.7		Ω
R_{LDLO}	Low-side driver sinking resistance	V_{CCDR}– GND = 5 V, low state		0.33		Ω
POWER GOOD						
V_{PGDL}	PG lower threshold	Measured at VSEN w/r/t VREF		87%	89%	
V_{PGDU}	PG upper threshold	Measured at VSEN w//rt VREF	110%	113%	116%	
V_{PGHYS}	PG hysteresis	Measured at VSEN w/r/t VREF		3.5%		
$t_{OVPGDLY}$	PG delay time at OVP	Time from VSEN out of +12.5% of VREF to PG low		2.3		µs
$t_{UVPGDLY}$	PG delay time at UVP	Time from VSEN out of –12.5% of VREF to PG low		2.3		µs
$V_{INMINPG}$	Minimum V_{CC} voltage for valid PG at startup.	Measured at V_{VCC} with 1 mA (or 2 mA) sink current on PG pin at startup.		1		V
V_{PGPD}	PG pull-down voltage	Pull down voltage with 4 mA sink current		0.2	0.4	V
I_{PGLK}	PG leakage current	Hi-Z leakage current, apply 6.5 V in off state	7.8	12	16.2	µA
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
V_{OVth}	OVP threshold	Measured at the VSEN wrt. VREF.	110%	113%	116%	
V_{UVth}	UVP threshold	Measured at the VSEN wrt. VREF.		87%	89%	
t_{OVPDLY}	OVP delay time	Time from VSEN out of +12.5% of VREF to OVP fault		2.3		µs
t_{UVPDLY} [3]	UVP delay time	Time from VSEN out of –12.5% of VREF to UVP fault		80		µs
THERMAL SHUTDOWN						
THSD [3]	Thermal shutdown	Latch off controller, attempt soft-stop	130	140	150	°C
$THSD_{HYS}$ [3]	Thermal shutdown hysteresis	Controller starts again after temperature has dropped		40		°C

(3) Ensured by design. Not production tested.

DEVICE INFORMATION

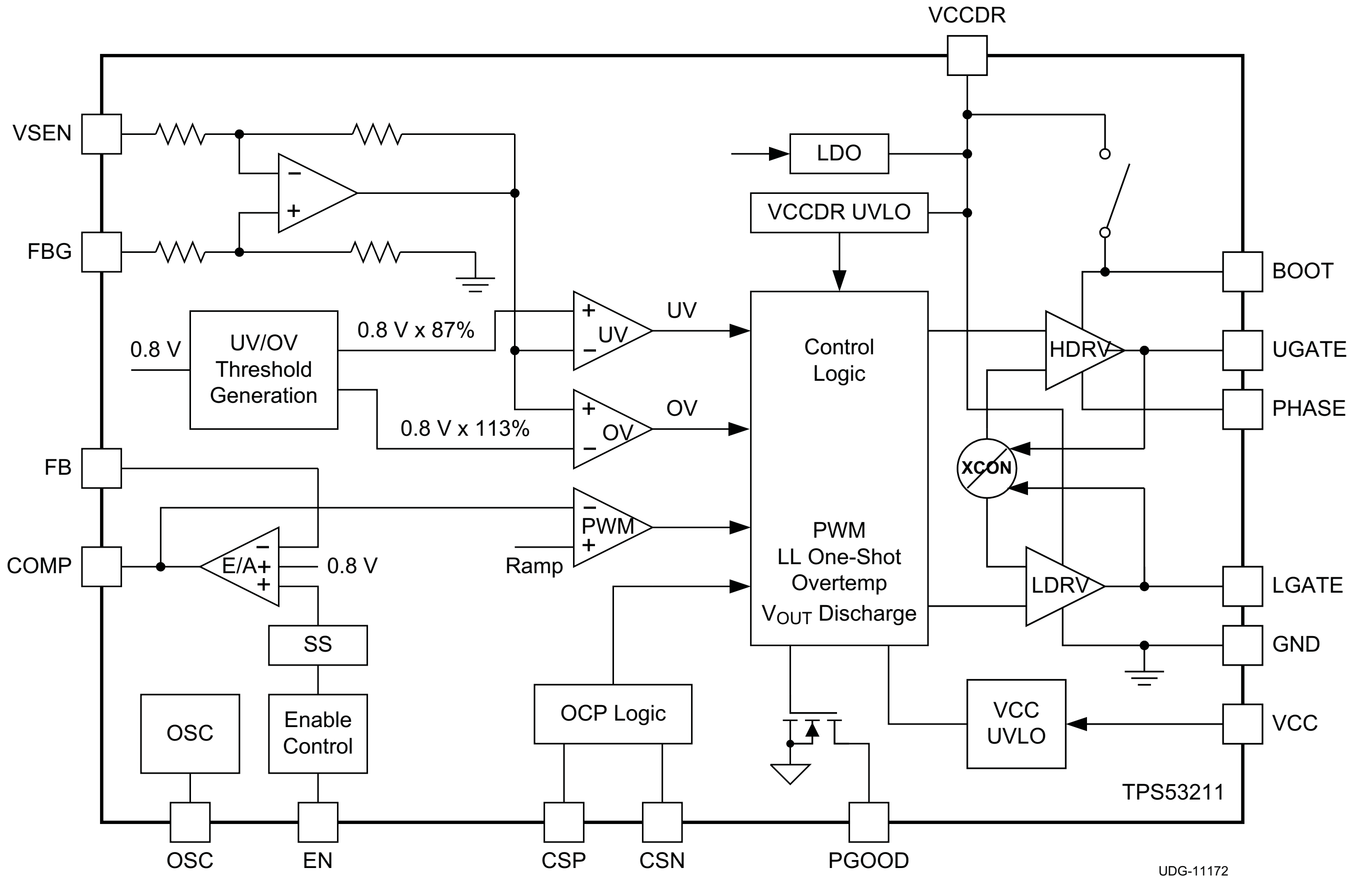
TPS53211
16 PINS
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	4	I	Supply input for high-side drive (boot strap pin). Connect capacitor from this pin to SW pin
COMP	8	O	Error amplifier compensation terminal. Type III compensation method is generally recommended for stability.
CSN	12	I	Current sense negative input.
CSP	13	I	Current sense positive input
EN	7	I	Enable.
FB	9	I	Voltage feedback. Use for OVP, UVP and PGD determination.
FBG	11	G	Feedback ground for output voltage sense.
GND	16	G	Logic ground and low-side gate drive return.
PHASE	3	O	Output inductor connection to integrated power devices.
LGATE	2	O	Low-side gate drive output.
OSC	14	O	Frequency programming input.
PGOOD	6	O	Power good output flag. Open drain output. Pull up to an external rail via a resistor.
UGATE	5	O	High-side gate drive output.
VCC	15	I	Supply input for analog control circuitry.
VCCDR	1	I/O	Bias voltage for integrated drivers.
VSEN	10	I	Output voltage sense

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

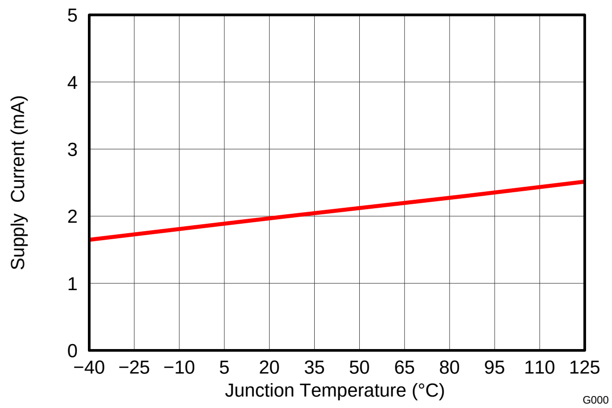


Figure 1. VCC Current vs. Junction Temperature

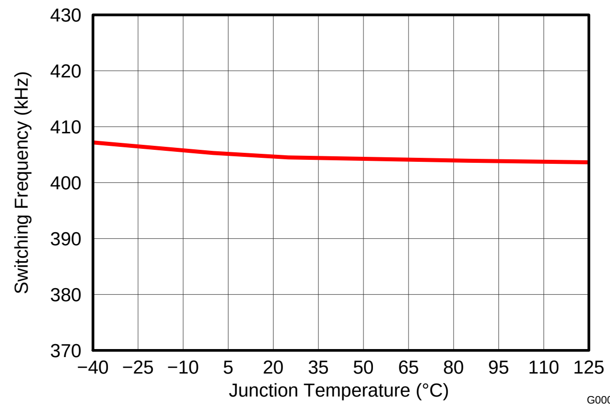


Figure 2. Switching Frequency vs. Junction Temperature

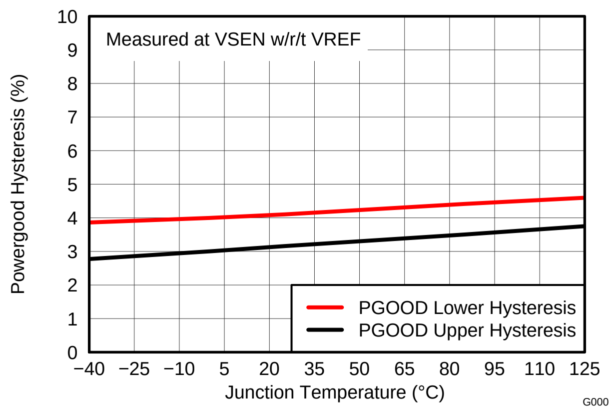


Figure 3. Power Good Hysteresis vs. Junction Temperature

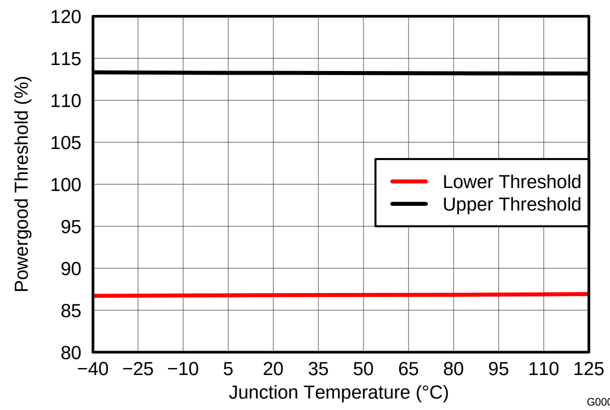


Figure 4. Power Good Threshold vs. Junction Temperature

DETAILED DESCRIPTION

Introduction

The TPS53211 is a single-channel synchronous buck controller with integrated high-current drivers. The TPS53211 is used for 1.5 V up to 19 V conversion voltage, and provides output voltage from 0.8 V to 0.7 V_{IN}. It operates with programmable switching frequency ranging from 250 kHz to 1 MHz.

This device employs a skip mode solution that optimizes the efficiency at light-load condition without compromising the output voltage ripple. The device provides pre-bias startup, integrated bootstrap switch, power good function, EN/Input UVLO protection. The TPS53211 is available in the 3 mm by 3mm 16-pin QFN package and is specified from –40°C to 85°C.

Switching Frequency Setting

The clock frequency is programmed by the value of the resistor connected from the OSC pin to ground. The switching frequency is programmable from 250 kHz to 1 MHz. The relation between the frequency and the OSC resistance is given by Equation 1.

$$f_{SW} = 200 + \frac{10^6}{\left(R_{OSC} \times 78.5\right) + 150} \tag{1}$$

where

- R_{OSC} is the resistor connected from the OSC pin to ground in kΩ
- f_{SW} is the desired switching frequency in kHz

Soft-Start Function

The soft-start function reduces the inrush current during the start-up. A slow rising reference voltage is generated by the soft-start circuitry and sent to the input of the error amplifier. When the soft-start ramp voltage is less than 800 mV, the error amplifier uses this ramp voltage as the reference. When the ramp voltage reaches 800 mV, a fixed 800 mV reference voltage is utilized for the error amplifier. The soft-start function is implemented only when VCC and VCCDR are above the respective UVLO thresholds and the EN pin is released.

When the soft-start begins, the device initially waits for 1024 clock cycles and then starts to ramp up the reference. After the reference voltage begins to rise, the PGOOD signal goes high after a 1560 clock-cycle delay.

UVLO Function

The TPS53211 provides UVLO protection for the input supply (VCC) and driver supply (VCCDR). If the supply voltage is lower than UVLO threshold voltage minus the hysteresis, the device shuts off. When the voltage rises above the threshold voltage, the device restarts. The typical UVLO rising threshold is 4.25 V for VCC and 3.32 V for VCCDR. Hysteresis of 200 mV for VCC and 220 mV for VCCDR are also provided to prevent glitch.

Overcurrent Protection

The TPS53211 continuously monitors the current flowing through the inductor. The inductor DCR current sense is implemented by comparing and monitoring the difference between the CSP and CSN pins. DCR current sensing requires time constant matching between the inductor and the sensing network:

$$\frac{L}{DCR} = R \times C \tag{2}$$

TPS53211 has two level OC thresholds: 20 mV and 30 mV for the voltage between the CSP and CSN pins.

If the voltage between the CSP and CSN pins exceeds the 20 mV current limit threshold, an OC counter starts to increment to count the occurrence of the overcurrent events. The converter shuts down immediately when the OC counter reaches four (4). The OC counter resets if the detected current is lower than the OC threshold after an OC event. Normal operation can only be restored by cycling the VCC voltage.

If the voltage between the CSP and CSN pins is higher than 30 mV, the device latches off immediately. Normal operation can be restored only by cycling the VCC voltage.

The TPS53211 has thermal compensation to adjust the OCP threshold in order to reduce the influence of inductor DCR variation due to temperature change. The OCP level has a change rate of 0.35%/°C.

Overvoltage and Undervoltage Protection

The TPS53211 monitors the VSEN pin voltage to detect the overvoltage and undervoltage conditions. A resistor divider with the same ratio as on the FB input is recommended for the VSEN input. The overvoltage and undervoltage thresholds are set to ±13% of V_{OUT}.

When the VSEN voltage is greater than 113% of the reference, the overvoltage protection is activated. The high-side MOSFET turns off and the low-side MOSFET turns on. Normal operation can be restored only by cycling the VCC pin voltage.

When the VSEN voltage is lower than 87% of the reference voltage, the undervoltage protection is triggered and the PGOOD signal goes low. After 80 µs, the controller is latched off with both the upper and lower MOSFETs turned off.

After both the undervoltage and overvoltage events, the device is latched off. Normal operation can be restored only by cycling the VCC pin voltage.

Power Good

The TPS53211 monitors the output voltage through the VSEN. During start up, the power good signal delay after the reference begins to rise is 1560 clock cycles. After this delay, if the output voltage is within ±9.5% of the target value, PGOOD signal goes high.

At steady state, if the VSEN voltage is within 113% and 87% of the reference voltage, the power good signal remains high. If VSEN voltage is outside of this limit, PGOOD pin is pulled low by the internal open drain output. The PGOOD output is an open drain and requires an external pull-up resistor.

Over-Temperature Protection

The TPS53211 continuously monitors the die temperature. If the die temperature exceeds the threshold value (140˚C typical), the device shuts off. When the device temperature lowers to 40˚C below the over-temperature threshold, it restarts and return to normal operation.

APPLICATION INFORMATION

The following example illustrates the design process and component selection for a single output synchronous buck converter using TPS53211. The schematic of a design example is shown in Figure 5. The specifications of the converter are listed in Table 1.

Table 1. Specification of the Single Output Synchronous Buck Converter

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		10.8	12	13.2	V
V_{OUT}	Output voltage			1.05		V
V_{RIPPLE}	Output ripple	I_{OUT} = 20 A		1% of V_{OUT}		V
I_{OUT}	Output current			20		A
f_{SW}	Switching frequency			400		kHz

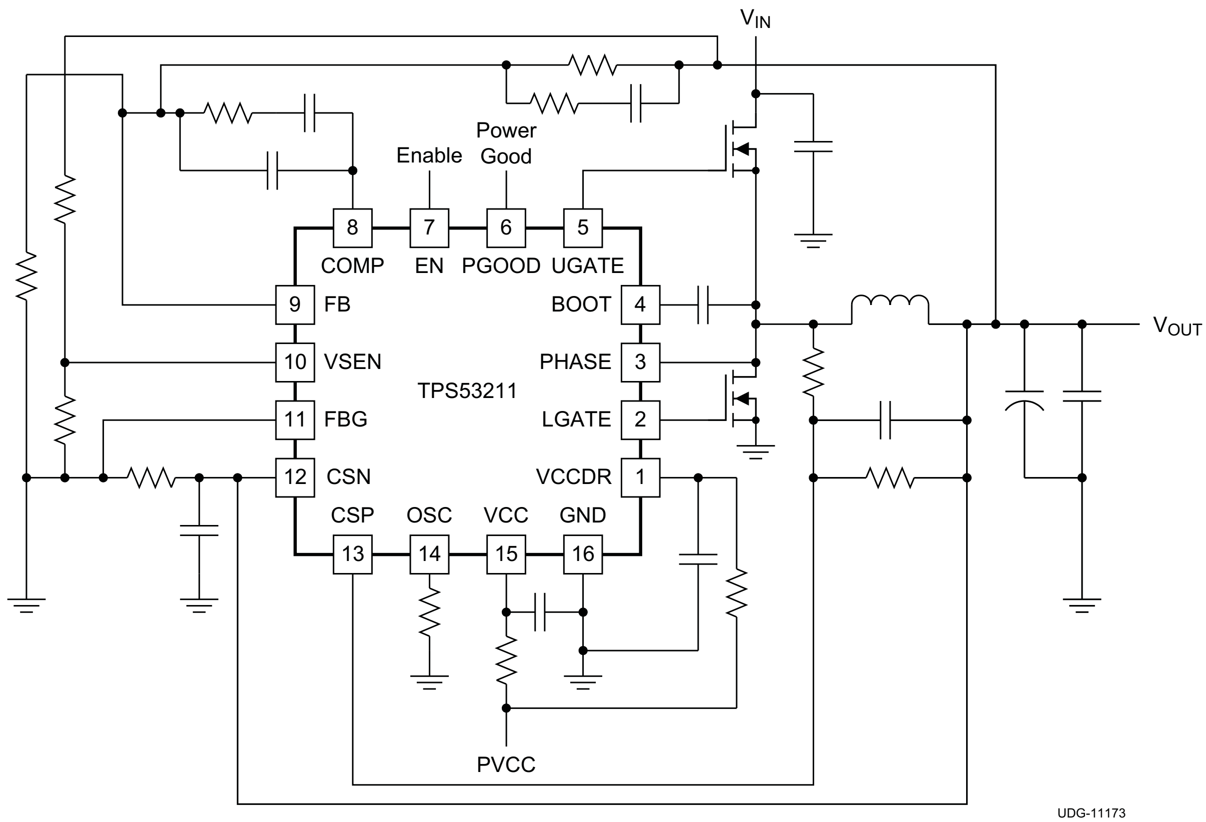


Figure 5. Typical 12-V Input Application Circuit

Output Inductor Selection

Determine an inductance value that yields a ripple current of approximately 20% to 40% of maximum output current. The inductor ripple current is determined by Equation 3:

$$I_{L(ripple)} = \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \tag{3}$$

The inductor requires a low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

Output Capacitor Selection

The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has three components:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} \quad (4)$$

$$V_{RIPPLE(C)} = \frac{I_{L(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (5)$$

$$V_{RIPPLE(ESR)} = I_{L(ripple)} \times ESR \quad (6)$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L} \quad (7)$$

When a ceramic output capacitor is chosen, the ESL component is usually negligible. In the case when multiple output capacitors are used, the total ESR and ESL should be the equivalent of the all output capacitors in parallel.

When operating in DCM, the output ripple is dominated by the component determined by capacitance. It also varies with load current and can be expressed as shown in Equation 8.

$$V_{RIPPLE(DCM)} = \frac{\left(\alpha \times I_{L(ripple)} - I_{OUT}\right)^2}{2 \times f_{SW} \times C_{OUT} \times I_{L(ripple)}}$$

where

- α is the DCM On-Time coefficient and can be expressed as $\alpha = \frac{t_{ON(dcm)}}{t_{ON(ccm)}}$ (8)

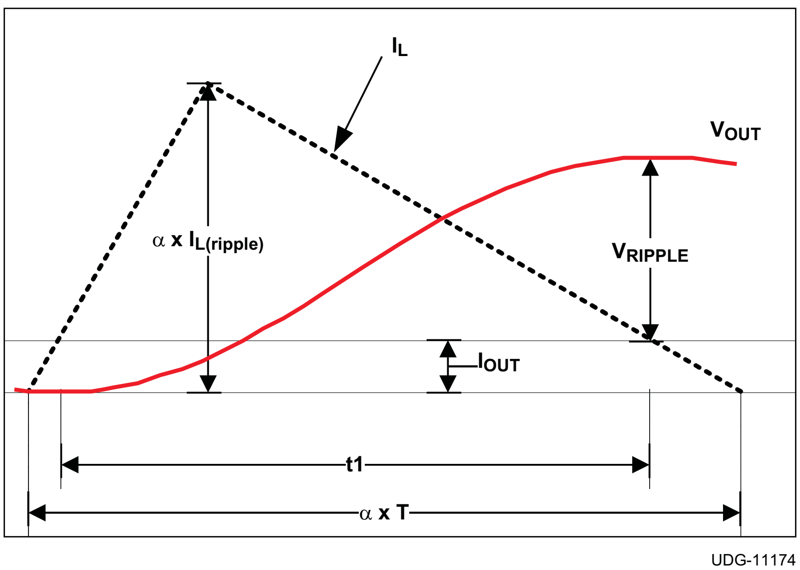


Figure 6. DCM V_{OUT} Ripple Calculation

Input Capacitor Selection

The selection of input capacitor should be determined by the ripple current requirement. The ripple current generated by the converter needs to be absorbed by the input capacitors as well as the input source. The RMS ripple current from the converter can be expressed as:

$$I_{IN(ripple)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where

- D is the duty cycle and can be expressed as $D = \frac{V_{OUT}}{V_{IN}}$ (9)

To minimize the ripple current drawn from the input source, sufficient input decoupling capacitors should be placed close to the device. The ceramic capacitor is recommended due to the inherent low ESR and low ESL. The input voltage ripple can be calculated as below when the total input capacitance is determined:

$$V_{IN(ripple)} = \frac{I_{OUT} \times D}{f_{SW} \times C_{IN}} \quad (10)$$

Output Voltage Setting Resistors Selection

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 7. R1 is connected between FB pin and the output, and R2 is connected between the FB pin and FBG. The recommended value for R1 is between 1 kΩ and 5 kΩ. Determine R2 using Equation 11.

$$R1 = \left(\frac{0.8}{(V_{OUT} - 0.8)} \right) \times R1 \quad (11)$$

Compensation Design

The TPS53211 employs voltage mode control. To effectively compensation the power stage and ensures fast transient response, Type III compensation is typically used.

The control to output transfer function can be described in Equation 12.

$$G_{CO} = 4 \times \frac{1 + s \times C_{OUT} \times ESR}{1 + s \times \left(\frac{L}{DCR + R_{LOAD}} + C_{OUT} \times (ESR + DCR) \right) + s^2 \times L \times C_{OUT}} \quad (12)$$

The output LC filter introduces a double pole, calculated in Equation 13.

$$f_{DP} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}} \quad (13)$$

The ESR zero of can be calculated calculated in Equation 14

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \quad (14)$$

Figure 7 shows the configuration of Type III compensation and typical pole and zero locations. Equation 15 through Equation 17 describe the compensator transfer function and poles and zeros of the Type III network.

$$G_{EA} = \frac{(1 + s \times C_1 \times (R_1 + R_3))(1 + s \times R_4 \times C_2)}{(s \times R_1 \times (C_2 + C_3)) \times (1 + s \times C_1 \times R_3) \times \left(1 + s \times R_4 \frac{C_2 \times C_3}{C_2 + C_3}\right)} \quad (15)$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R_4 \times C_2} \quad (16)$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R_1 + R_3) \times C_1} \cong \frac{1}{2 \times \pi \times R_1 \times C_1} \quad (17)$$

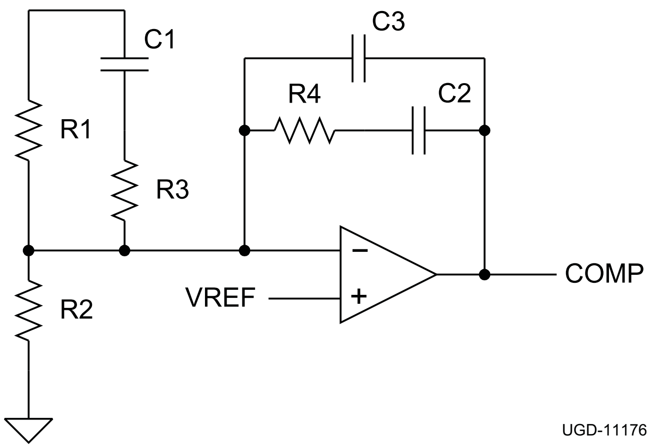


Figure 7. Type III Compensation Network Configuration

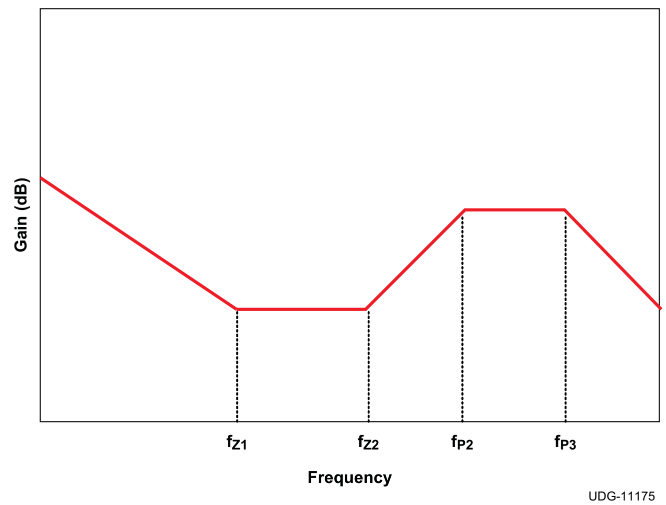


Figure 8. Type III Compensation Network Waveform

$$f_{P1} = 0 \quad (18)$$

$$f_{P2} = \frac{1}{2 \times \pi \times R_3 \times C_1} \quad (19)$$

$$f_{P3} = \frac{1}{2 \times \pi \times R_4 \times \left(\frac{C_2 \times C_3}{C_2 + C_3}\right)} \cong \frac{1}{2 \times \pi \times R_4 \times C_3} \quad (20)$$

The two zeros can be placed near the double pole frequency to cancel the response from the double pole. One pole can be used to cancel ESR zero, and the other non-zero pole can be placed at half switching frequency to attenuate the high frequency noise and switching ripple. Suitable values can be selected to achieve a compromise between high phase margin and fast response. A phase margin higher than 45° is required for stable operation.

Changes from Original (September 2011) to Revision A **Page**

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS53211RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	53211
TPS53211RGTR.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	53211
TPS53211RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	53211
TPS53211RGTT.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	53211

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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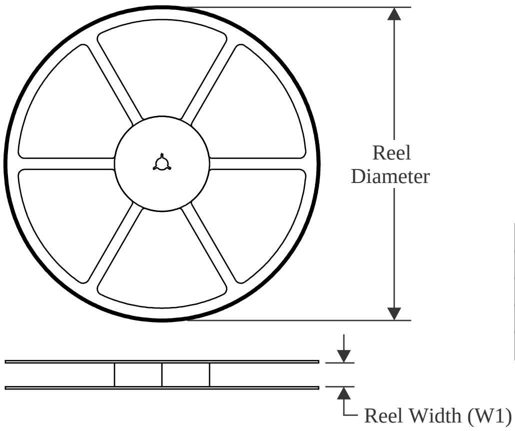
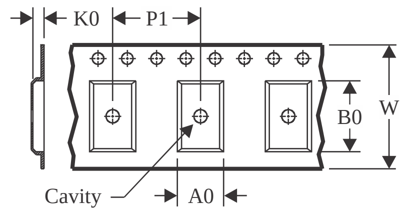
TAPE AND REEL INFORMATION

REEL DIMENSIONS

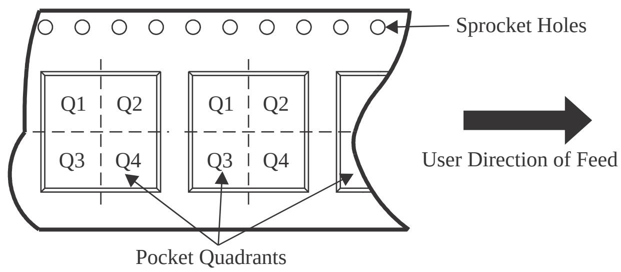


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

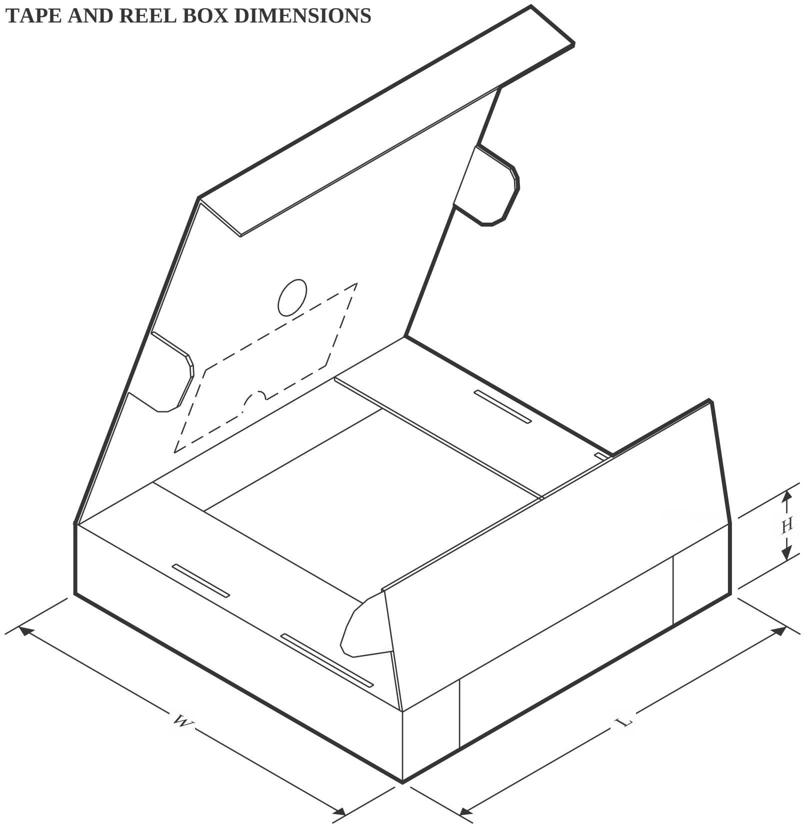
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

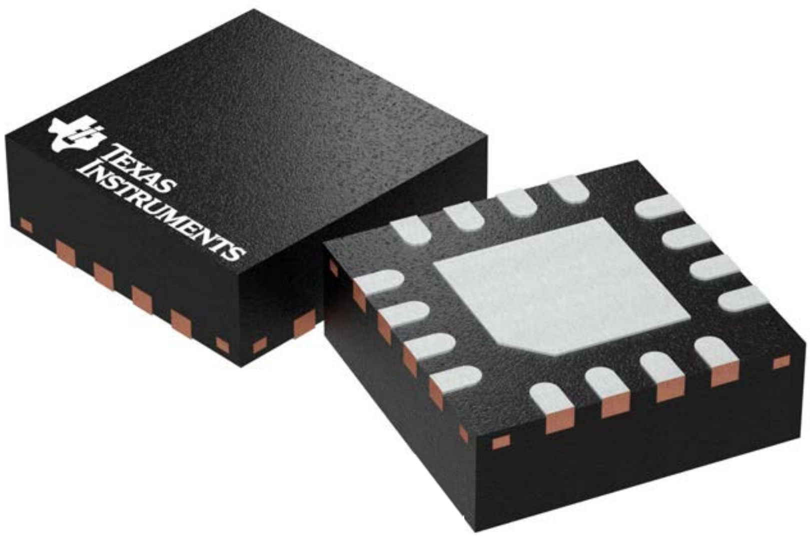
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53211RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS53211RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

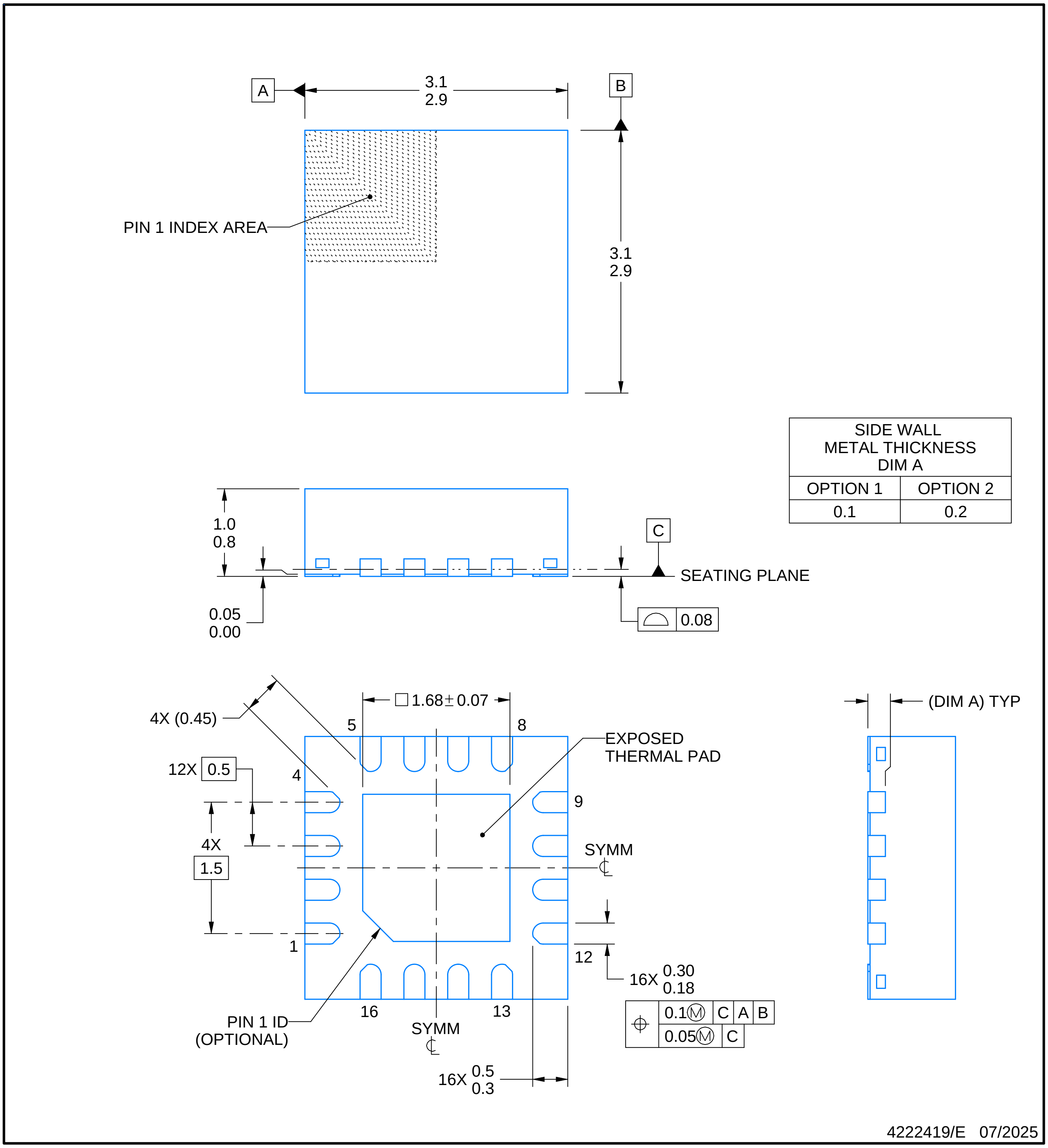


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53211RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
TPS53211RGTT	VQFN	RGT	16	250	210.0	185.0	35.0



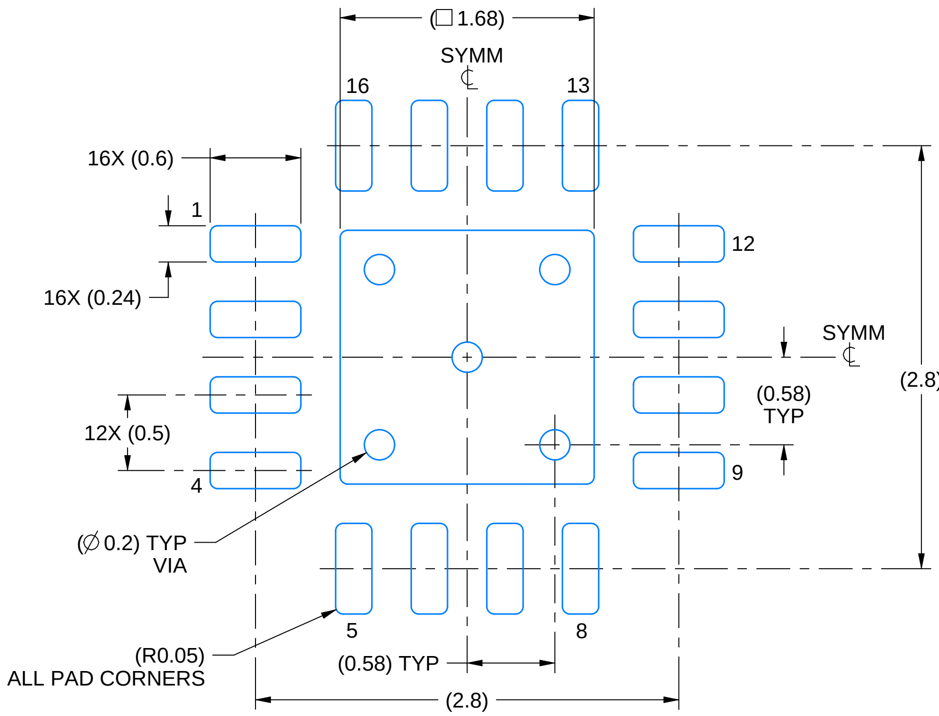
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



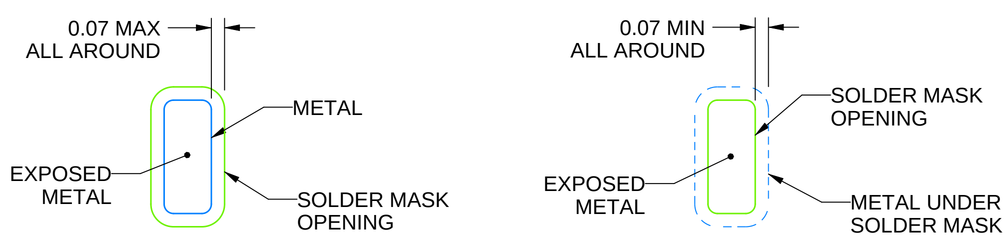
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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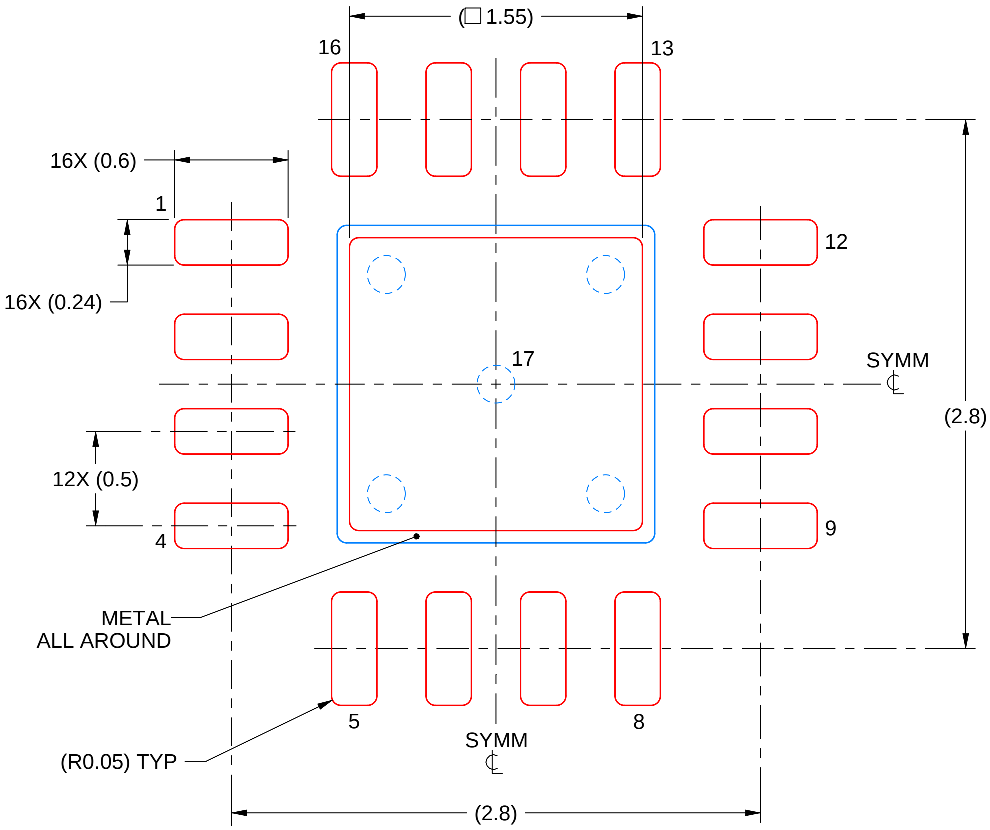
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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