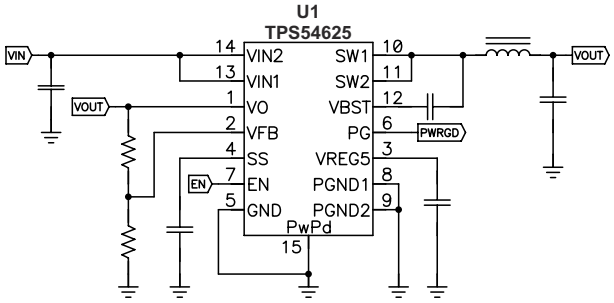
4.5V 至 18V 输入、6.5A 同步降压转换器

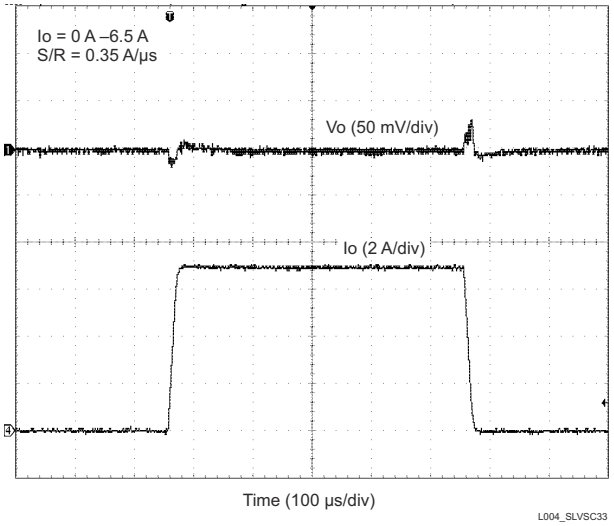
1 特性

- D-CAP2™ 模式支持快速瞬态响应
- 低输出纹波且支持陶瓷输出电容器
- 宽 V_{IN} 输入电压范围：4.5V 至 18V
- 输出电压范围：0.76V 至 5.5V
- 高效率集成型 FET
  针对较低占空比应用进行了优化
  - 36mΩ（高侧）与 28mΩ（低侧）
- 高效率，关断时流耗少于 10μA
- 高初始带隙基准精度
- 可调软启动
- 预偏置软启动
- 650kHz 开关频率 (f_{SW})
- 逐周期限流
- 电源正常输出

2 应用范围

- 低电压系统的广泛应用
  - 数字电视电源
  - 高清蓝光光盘™播放器
  - 网络互联家庭终端设备
  - 数字机顶盒 (STB)





3 说明

TPS54625 是一款自适应接通时间 D-CAP2™ 模式同步降压转换器。TPS54625 可帮助系统设计人员用成本有效、低组件数量、低待机电流解决方案来完成不同终端设备的电源总线调节器集。

TPS54625 的主控制环路采用 D-CAP2™ 模式控制，无需外部补偿元件便可实现超快的瞬态响应。TPS54625 的专有电路还使该器件可采用诸如高分子有机半导体固体电容器 (POSCAP) 或高分子聚合物电容器 (SP-CAP) 等低等效串联电阻 (ESR) 输出电容器以及超低 ESR 陶瓷电容器。该器件的工作电压介于 4.5V 至 18V 的 VIN 输入之间。输出电压可在 0.76V 与 5.5V 之间进行编程。该器件还特有一个可调软启动时间和一个电源正常功能。TPS54625 采用 14 引脚散热薄型小外形尺寸 (HTSSOP) 封装，设计工作温度介于 -40°C 到 85°C 之间。

4 ORDERING INFORMATION(1)

T_A	PACKAGE(2) (3)	ORDERABLE PART NUMBER	PIN	TRANSPORT MEDIA, QUANTITY
–45°C to 85°C	PowerPAD™ (HTSSOP) – PWP	TPS54625PWP	14	Tube
		TPS54625PWPR		Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) All package options have Cu NIPDAU lead/ball finish.

5 最大绝对额定值

在自然通风温度范围内（除非另有说明）(1)

			值	单位
V_I	输入电压范围	VIN1、VIN2 EN	-0.3 至 20	V
		VBST	-0.3 至 26	V
		VBST（10ns 瞬态值）	-0.3 至 28	V
		VBST（与 SW1、SW2 间的关系）	-0.3 至 6.5	V
		VFB、VO、SS、PG	-0.3 至 6.5	V
		SW1, SW2	-2 至 20	V
		SW1、SW2（10ns 瞬态值）	-3 至 22	V
V_O	输出电压范围	VREG5	-0.3 至 6.5	V
		PGND1、PGND2	-0.3 至 0.3	V
V_{diff}	从 GND 到 POWERPAD 的电压		-0.2 至 0.2	V
静电放电 (ESD) 额定值	静电放电	人体放电模型 (HBM)	2	kV
		充电器件模型 (CDM)	500	V
T_J	工作结温		-40 至 150	°C
T_{stg}	存储温度		-55 至 150	°C

(1) 超出*最大绝对额定值*下列出的值的应力可能会对器件造成永久损坏。这些仅为在应力额定值下的工作情况，对于额定值下的器件的功能性操作以及在超出*推荐的运行条件*下标明的任何其它条件下的操作，在此并未说明。长时间处于最大绝对额定情况下会影响设备的可靠性。

6 THERMAL INFORMATION

THERMAL METRIC(1)		TPS54625 PWP (14 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	40.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	28.7	
θ_{JB}	Junction-to-board thermal resistance	24.2	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	23.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.4	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	18	V
V_I	Input voltage range	VBST	–0.1	24	V
		VBST(10 ns transient)	–0.1	27	
		VBST (vs SW)	–0.1	6.0	
		SS, PG	–0.1	5.7	
		EN	–0.1	18	
		VO, VFB	–0.1	5.5	
		SW1, SW2	–1.8	18	
		SW1, SW2 (10 ns transient)	–3	21	
		PGND1, PGND2	–0.1	0.1	
V_O	Output voltage range	VREG5	–0.1	5.7	V
I_O	Output Current range	I_{VREG5}	0	5	mA
R_{EN}	Power Good Resistor		25	150	kΩ
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	150	°C

8 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating - non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5 V, V_{VFB} = 0.8 V		950	1400	μA
I_{VINSDN}	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V		3.6	10	μA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	1.6			V
V_{ENL}	EN low-level input voltage	EN			0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	200	400	800	kΩ
VFB VOLTAGE AND DISCHARGE RESISTANCE						
V_{VFBTH}	VFB threshold voltage	T_A = 25°C, V_O = 1.05 V, continuous mode	757	765	773	mV
		T_A = 0℃ to 85℃, V_O = 1.05 V, continuous mode (1)	753		777	
		T_A = –40°C to 85°C, V_O = 1.05 V, continuous mode(1)	751		779	
I_{VFB}	VFB input current	VFB = 0.8 V, T_A = 25°C		0	±0.15	μA
R_{Dischg}	V_O discharge resistance	V_{EN} = 0 V, V_O = 0.5 V, T_A = 25°C		100	150	Ω
VREG5 OUTPUT						
V_{VREG5}	VREG5 output voltage	T_A = 25°C, 6.0 V < V_{IN} < 18 V, 0 < I_{VREG5} < 5 mA	5.2	5.5	5.7	V
I_{VREG5}	Output current	V_{IN} = 6 V, V_{VREG5} = 4 V, T_A = 25°C	20			mA
MOSFET						
R_{dsonh}	High side switch resistance	T_A = 25°C, V_{BST} - $V_{SW1,2}$ = 5.5 V		36		mΩ
R_{dsonl}	Low side switch resistance	T_A = 25°C		28		mΩ

8 ELECTRICAL CHARACTERISTICS (continued)

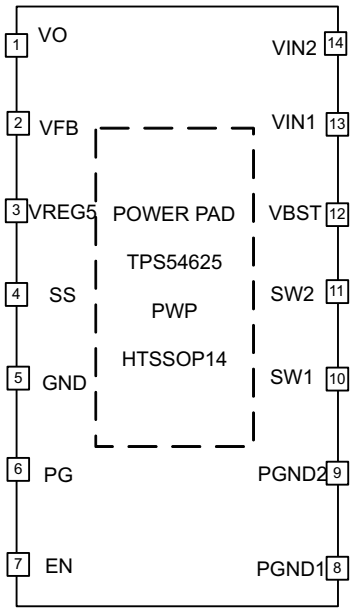
over operating free-air temperature range, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{ocl}	Current limit	L_{OUT} = 1.5 µH(1)	7.2	8.2	9.5	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature (1)		165		°C
		Hysteresis (1)		35		
ON-TIME TIMER CONTROL						
T_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		150		ns
$T_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{VFB} = 0.7 V		260	310	ns
SOFT START						
I_{SSC}	SS charge current	V_{SS} = 1 V	4.2	6.0	7.8	µA
I_{SSD}	SS discharge current	V_{SS} = 0.5 V	1.5	3.3		mA
POWER GOOD						
V_{THPG}	PG threshold	V_{VFB} rising (good)	85%	90%	95%	
		V_{VFB} falling (fault)		85%		
I_{PG}	PG sink current	V_{PG} = 0.5 V	2.5	5		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	120%	125%	130%	
T_{OVPDEL}	Output OVP prop delay			10		µs
V_{UVP}	Output UVP trip threshold	UVP detect	60%	65%	70%	
		Hysteresis		10%		
T_{UVPDEL}	Output UVP delay			0.25		ms
T_{UVPEN}	Output UVP enable delay	Relative to soft-start time		X 1.7		
UVLO						
V_{UVLO}	UVLO threshold	Wake up VREG5 voltage	3.45	3.75	4.05	V
		Hysteresis VREG5 voltage	0.13	0.32	0.48	

(1) Not production tested.

9 DEVICE INFORMATION

PWP PACKAGE
(TOP VIEW)



Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
VO	1	Connect to output of converter. This pin is used for output discharge function.
VFB	2	Converter feedback input. Connect with feedback resistor divider.
VREG5	3	5.5V power supply output. An external capacitor (typical 1uF) should be connected to GND. VREG5 is not active when EN is low.
SS	4	Soft start control. An external capacitor should be connected to GND.
GND	5	Signal ground pin.
PG	6	Open drain power good output
EN	7	Enable control input. EN is active high and must be pulled up to enable the device.
PGND1, PGND2	8, 9	Ground returns for low-side MOSFET. Also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1,SW2	10, 11	Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparator.
VBST	12	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to respective SW1, SW2 terminals. An internal PN diode is connected between VREG5 and VBST pin.
VIN1, VIN2	13, 14	Power Input and connected to high side NFET drain. Supply Input for 5V internal linear regulator for the control circuitry
PowerPAD™	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND

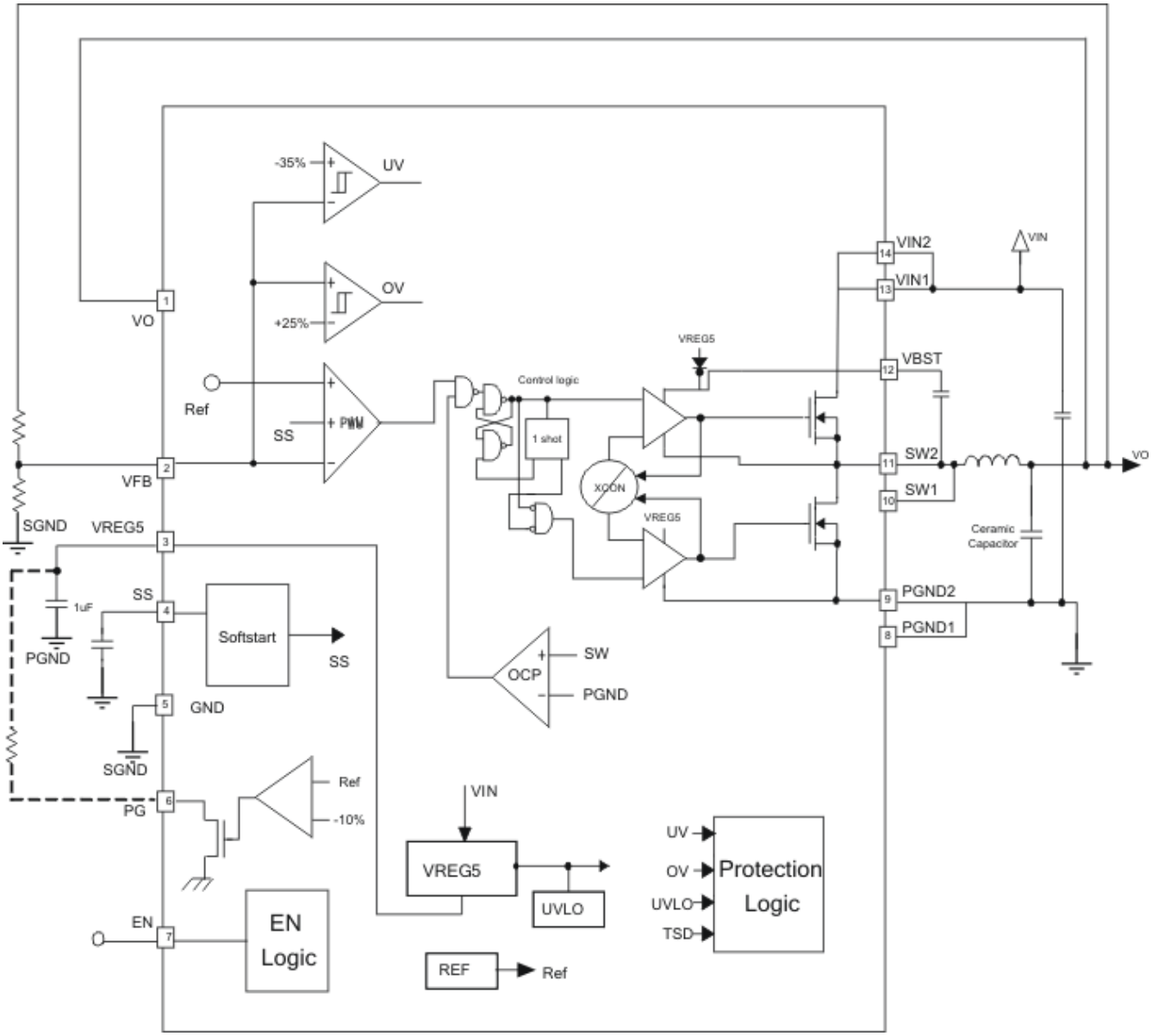


图 9-1. FUNCTIONAL BLOCK DIAGRAM (HTSSOP)

10 OVERVIEW

The TPS54625 is a 6.5A synchronous step-down (buck) converter with two integrated N-channel MOSFETs, using Forced Continuous Conduction Mode (FCCM) at light load for small output voltage ripple. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

11 DETAILED DESCRIPTION

11.1 PWM Operation

The main control loop of the TPS54625 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

11.2 PWM Frequency and Adaptive On-Time Control

TPS54625 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54625 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. The actual frequency may vary from 650kHz depending on the off time, which is ended when the feed back portion of the output voltage falls to the V_{FB} threshold voltage.

11.3 Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6-μA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in 方程式 1. VFB voltage is 0.765 V and SS pin source current is 6 μA.

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF} \times 1.1}{I_{SS}(\mu A)} = \frac{C_{SS}(nF) \times 0.765 \times 1.1}{6} \quad (1)$$

TPS54625 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage V_{FB}), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation .

11.4 Power Good

TPS54625 has power-good open drain output. The power-good function is activated after soft start has finished. The power good function becomes active after 1.7 times soft-start time. When the output voltage becomes within –10% of the target value, internal comparators detect power good state and the power good signal becomes high. Rpg resistor value, which is connected between PG and VREG5, is required from 25 kΩ to 150 kΩ. If the feedback voltage goes under 15% of the target value, the power good signal becomes low.

11.5 Output Discharge Control

TPS54625 discharges the output when EN is low, or the controller is turned off by the protection functions (UVP, UVLO and thermal shutdown). The device discharges the output using an internal 100-Ω MOSFET which is connected to VO and GND. The internal low-side MOSFET is not turned on for the output discharge operation to avoid the possibility of causing negative voltage at the output.

11.6 Current Protection

The output over-current protection(OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current Iout. The TPS54625 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current is higher than the over-current threshold. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall.

11.7 Over/Under Voltage Protection

TPS54625 detects over and under voltage conditions by monitoring the feedback voltage (VFB). This function is enabled after approximately 1.7 x times the softstart time.

When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and the circuit latches and both the high-side MOSFET driver and the low-side MOSFET driver turn off.

When the feedback voltage becomes lower than 65% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250us, the device latches off both internal top and bottom MOSFET.

11.8 UVLO Protection

Under voltage lock out protection (UVLO) monitors the voltage of $V_{REG5.pin}$. When the VREG5 voltage is lower than UVLO threshold voltage, The TPS54625 is shut off. This protection is non-latching.

11.9 Thermal Shutdown

Thermal protection is self-activating. If the junction temperature exceeds the threshold value (typically 165°C), the TPS54625 is shut off. This is non-latch protection.

12 TYPICAL CHARACTERISTICS

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

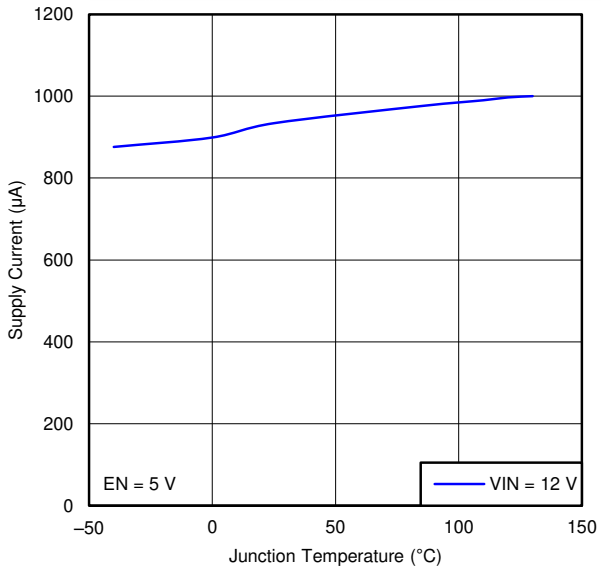


图 12-1. V_{IN} CURRENT vs JUNCTION TEMPERATURE

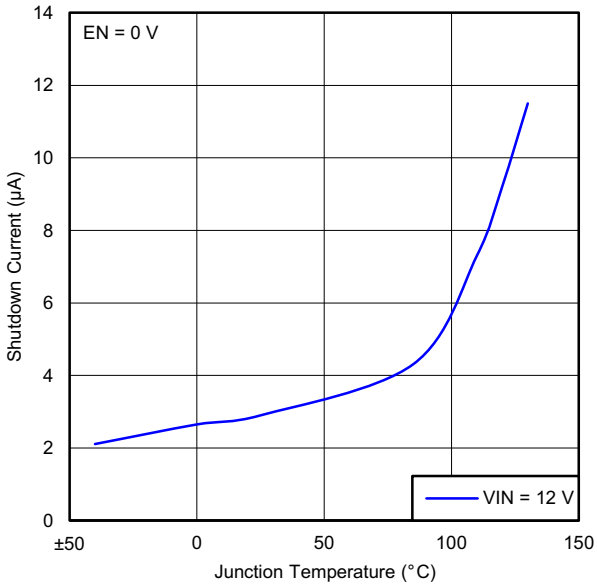


图 12-2. V_{IN} SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

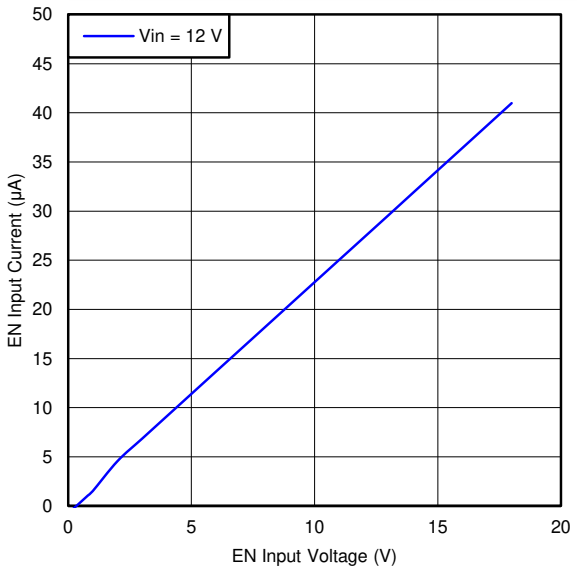


图 12-3. EN CURRENT vs EN VOLTAGE

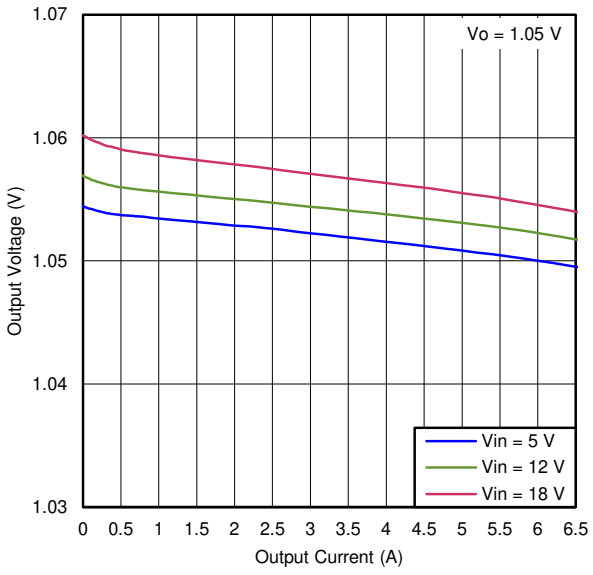


图 12-4. 1.05-V OUTPUT VOLTAGE vs OUTPUT CURRENT

12 TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

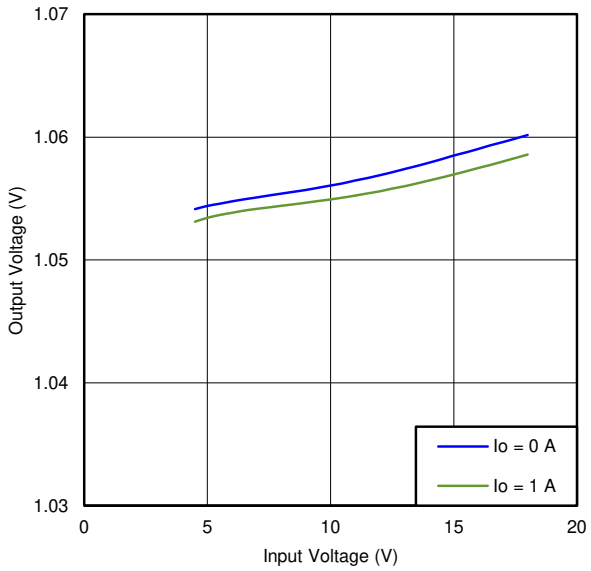


图 12-5. 1.05-V OUTPUT VOLTAGE vs INPUT VOLTAGE

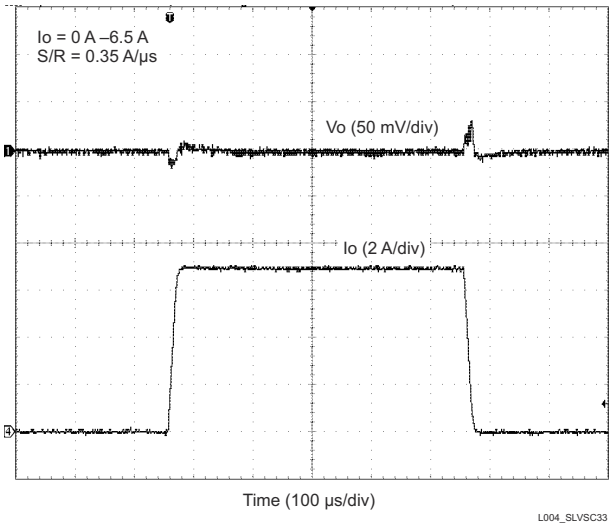


图 12-6. 1.05-V, 0-mA to 6.5-A LOAD TRANSIENT RESPONSE

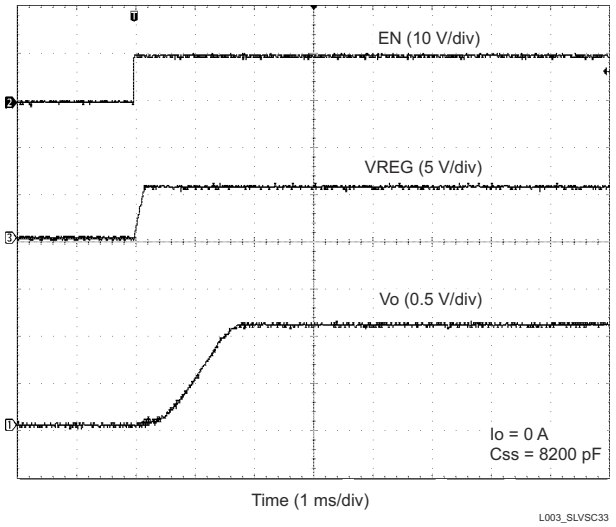


图 12-7. START-UP WAVE FORM

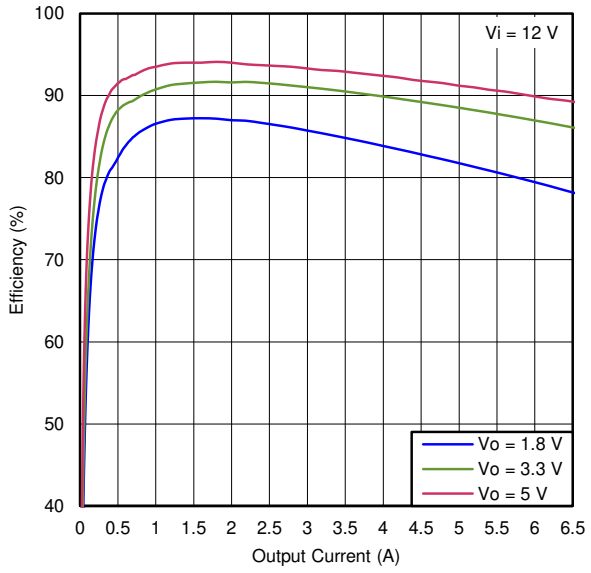


图 12-8. EFFICIENCY vs OUTPUT CURRENT (12 V)

12 TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

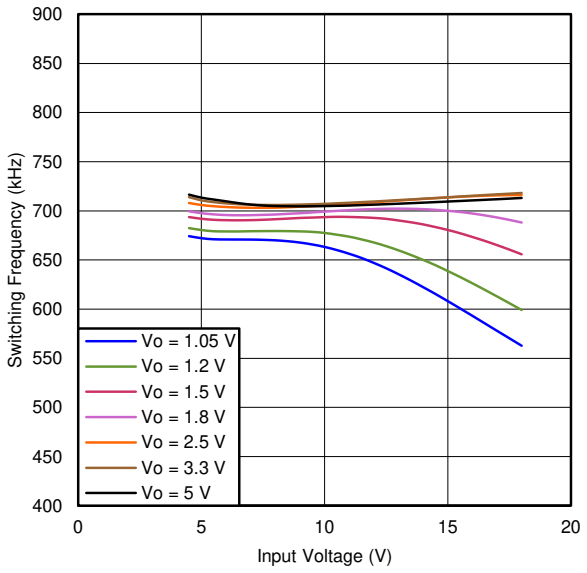


图 12-9. SWITCHING FREQUENCY vs INPUT VOLTAGE (I_O = 1 A)

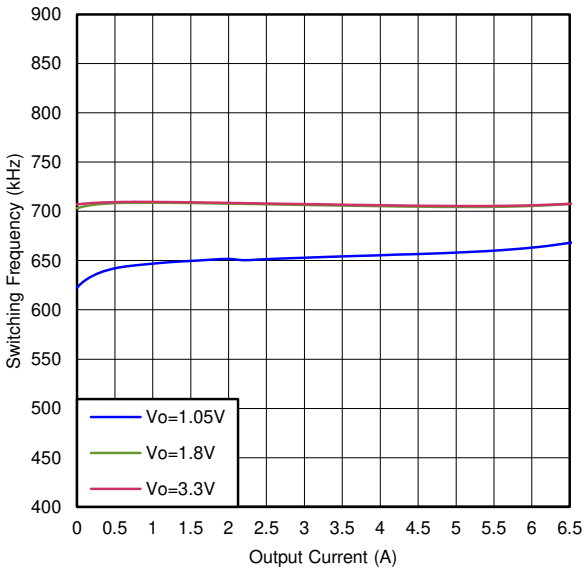


图 12-10. SWITCHING FREQUENCY vs OUTPUT CURRENT

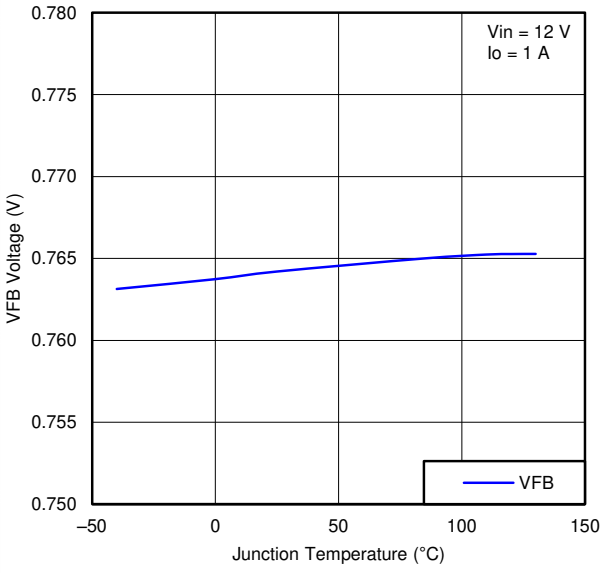


图 12-11. VFB VOLTAGE vs JUNCTION TEMPERATURE

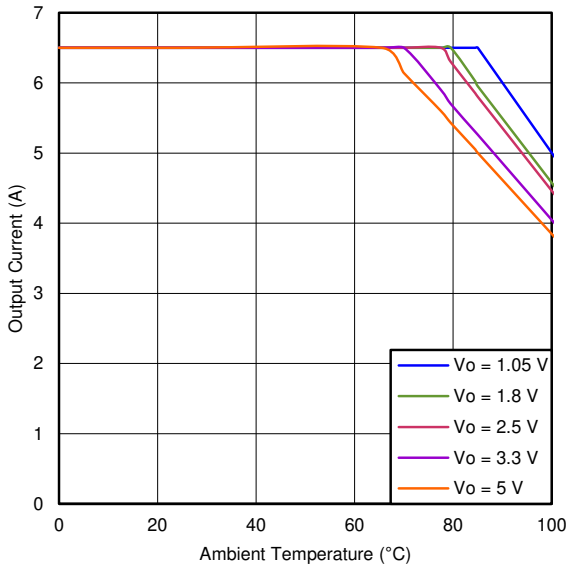


图 12-12. OUTPUT CURRENT vs AMBIENT TEMPERATURE

12 TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

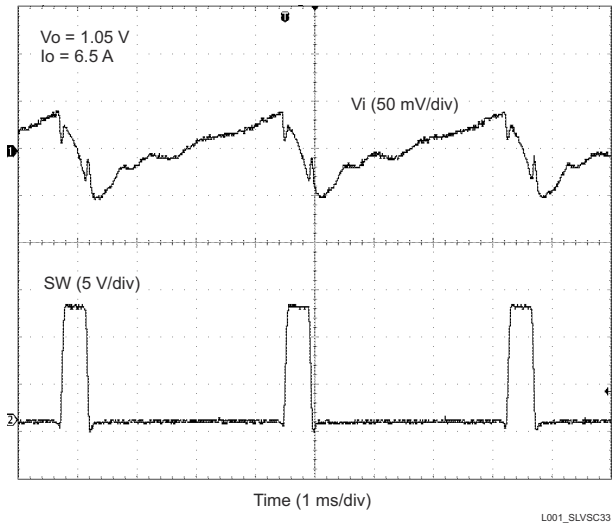


图 12-13. VOLTAGE RIPPLE AT INPUT (I_O = 6.5 A)

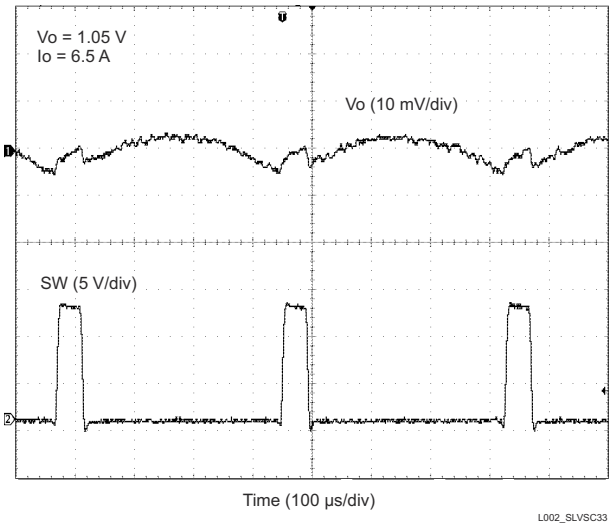


图 12-14. VOLTAGE RIPPLE AT OUTPUT (I_O = 6.5 A)

13 DESIGN GUIDE

13.1 Step By Step Design Procedure

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

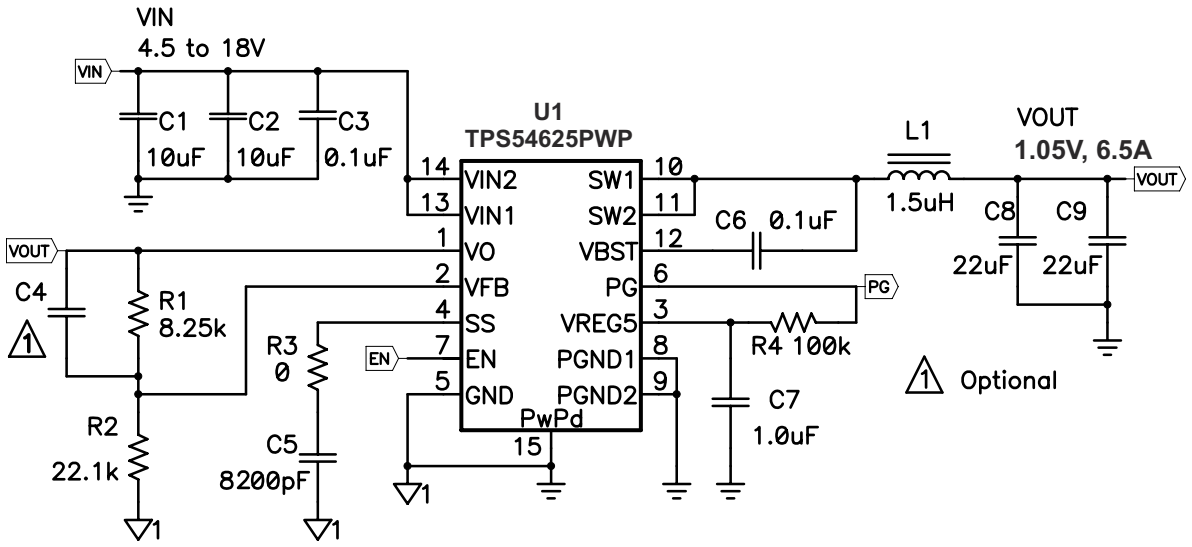


图 13-1. Schematic

13.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using 方程式 2 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.765 \bullet \left(1 + \frac{R1}{R2}\right) \tag{2}$$

13.3 Output Filter Selection

The output filter used with the TPS54625 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}} \tag{3}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54625. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of 方程式 3 is located below the high frequency zero but close enough that the phase boost provided be the high

frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 13-1

表 13-1. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)	L1 (µH)	C8 + C9 (µF)
1	6.81	22.1	5 - 220	1.0 - 1.5 - 4.7	22 - 68
1.05	8.25	22.1	5 - 220	1.0 - 1.5 - 4.7	22 - 68
1.2	12.7	22.1	5 - 100	1.0 - 1.5 - 4.7	22 - 68
1.5	21.5	22.1	5 - 68	1.0 - 1.5 - 4.7	22 - 68
1.8	30.1	22.1	5 - 22	1.2 - 1.5 – 4.7	22 - 68
2.5	49.9	22.1	5 - 22	1.5 - 2.2 – 4.7	22 - 68
3.3	73.2	22.1	5 - 22	1.8 - 2.2 – 4.7	22 - 68
5	124	22.1	5 - 22	2.5 - 3.3 – 4.7	22 - 68

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1.

Since the DC gain is dependent on the output voltage, the required inductor value will increase as the output voltage increases. For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 方程式 4, 方程式 5 and 方程式 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{SW}.

Use 650 kHz for f_{SW} and also use 1.5µH for Lo. Make sure the chosen inductor is rated for the peak current of 方程式 5 and the RMS current of 方程式 6.

$$Ilp\text{-}p = \frac{V_{OUT}}{V_{IN\,(max)}} \bullet \frac{V_{IN\,(max)} - V_{OUT}}{L_O \bullet f_{SW}} \tag{4}$$

$$I_{lpeak} = I_O + \frac{Ilp\text{-}p}{2} \tag{5}$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} Ilp\text{-}p^2} \tag{6}$$

For this design example, the calculated peak current is 7.01 A and the calculated RMS current is 6.51 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54625 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22µF to 68µF. Use 方程式 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{\sqrt{12} \bullet V_{IN} \bullet L_O \bullet f_{SW}} \tag{7}$$

For this design two TDK C3216X5R0J226M 22µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4A.

13.4 Input Capacitor Selection

The TPS54625 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 μF is recommended for the decoupling capacitor. An additional 0.1 μF capacitor from pin 14 to ground is recommended to improve the EMI performance. The capacitor voltage rating needs to be greater than the maximum input voltage.

13.5 Bootstrap Capacitor Selection

A 0.1 μF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

13.6 VREG5 Capacitor Selection

A 1.0 μF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

14 THERMAL INFORMATION

This PowerPad™ package incorporates an exposed thermal pad that is designed to be directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD™ Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in the following illustration.

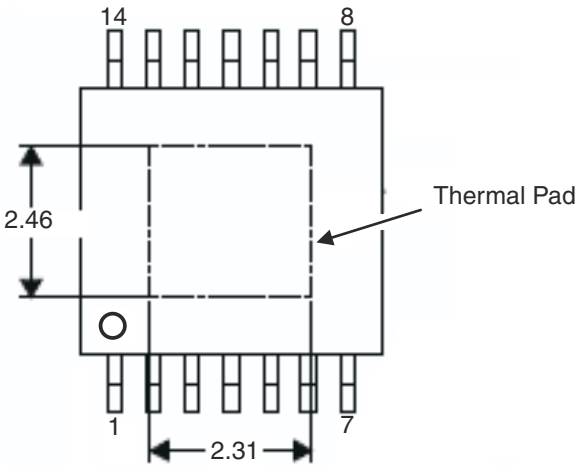


图 14-1. Thermal Pad Dimensions

15 LAYOUT CONSIDERATIONS

1. A top side area should be filled with ground as much as possible due to relatively higher current output device.
2. The ground area under the device thermal pad should be large as possible and directly connect to the thermal pad. Also 2nd, 3rd and 4th PCB layer should be connected to ground directly from the thermal pad.
3. Keep the input switching current loop as small as possible.
4. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
5. Keep analog and non-switching components away from switching components.
6. Make a single point connection from the signal ground to power ground.
7. Do not allow switching current to flow under the device.
8. Keep the pattern lines for VIN and PGND broad.
9. Exposed pad of device must be connected to PGND with solder.
10. VREG5 capacitor should be placed near the device, and connected PGND.
11. Output capacitor should be connected to a broad pattern of the PGND.
12. Voltage feedback loop should be as short as possible, and preferably with ground shield.
13. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
14. Providing sufficient via is preferable for VIN, SW and PGND connection.
15. PCB pattern for VIN, SW, and PGND should be as broad as possible.
16. VIN Capacitor should be placed as near as possible to the device.

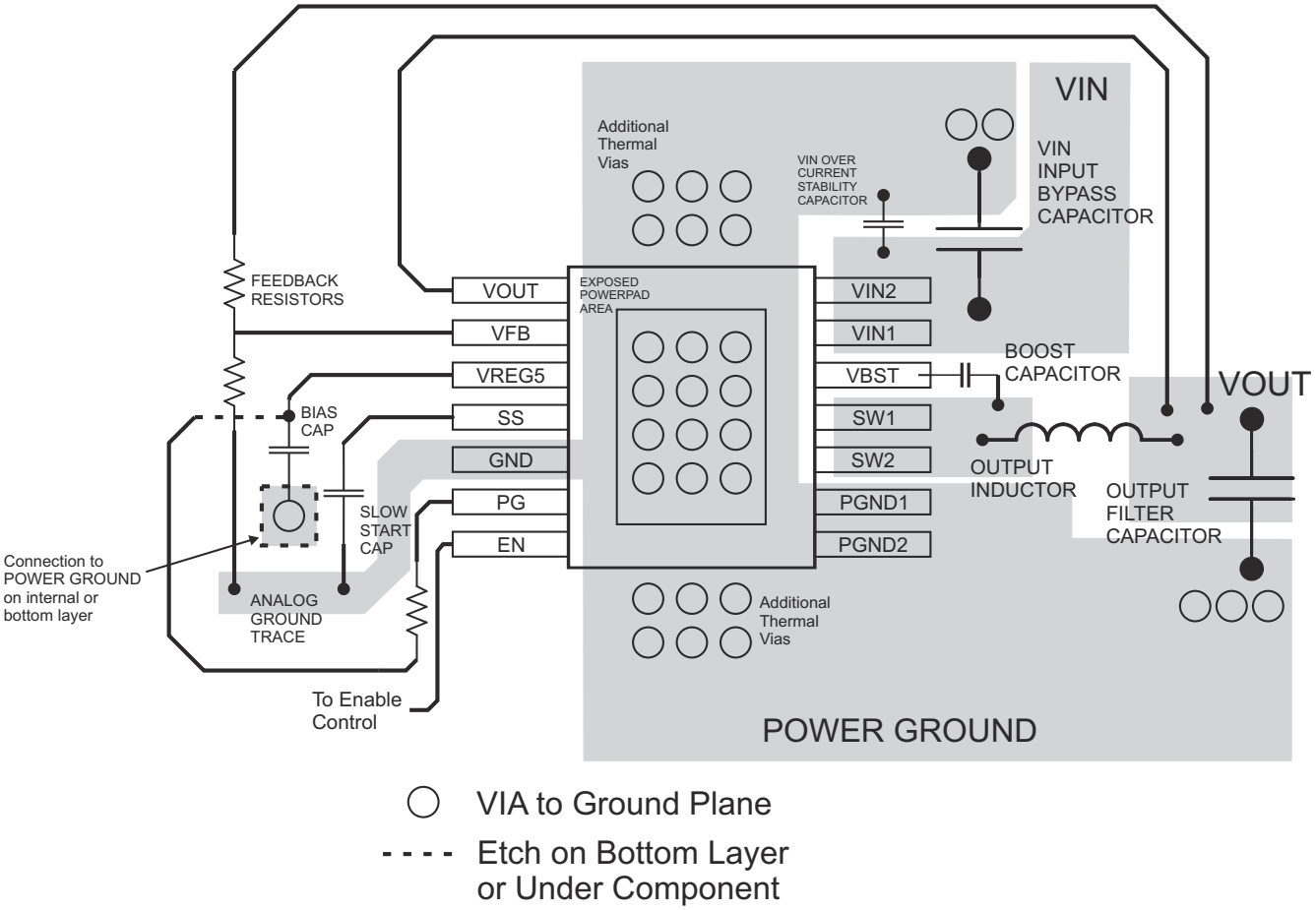


图 15-1. PCB Layout

16 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (August 2013) to Revision A (October 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated the light load mode to Forced Continuous Conduction Mode (FCCM)	7

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54625PWP	Active	Production	HTSSOP (PWP) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54625
TPS54625PWP.A	Active	Production	HTSSOP (PWP) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54625
TPS54625PWPR	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54625
TPS54625PWPR.A	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54625

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

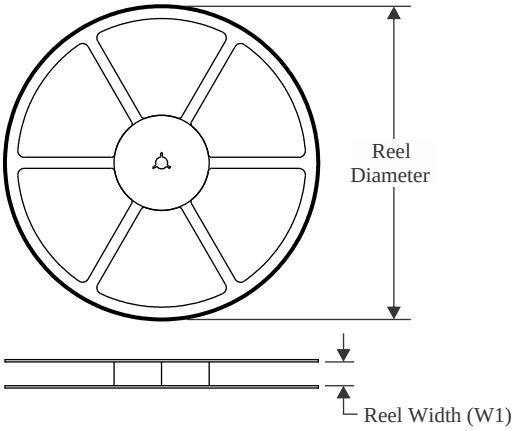
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

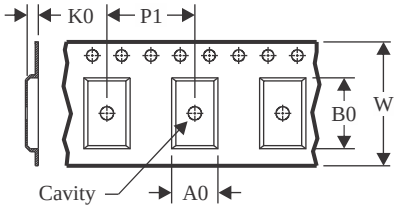
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

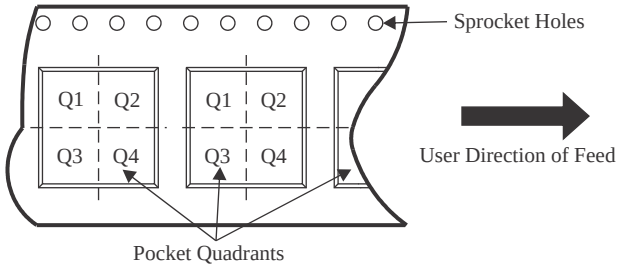


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

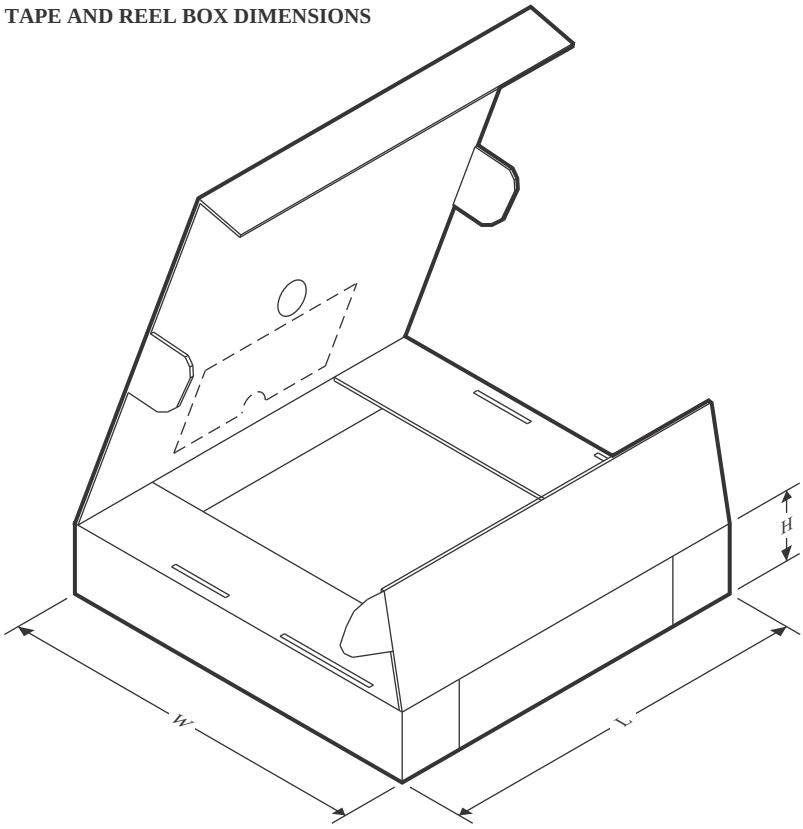
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54625PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

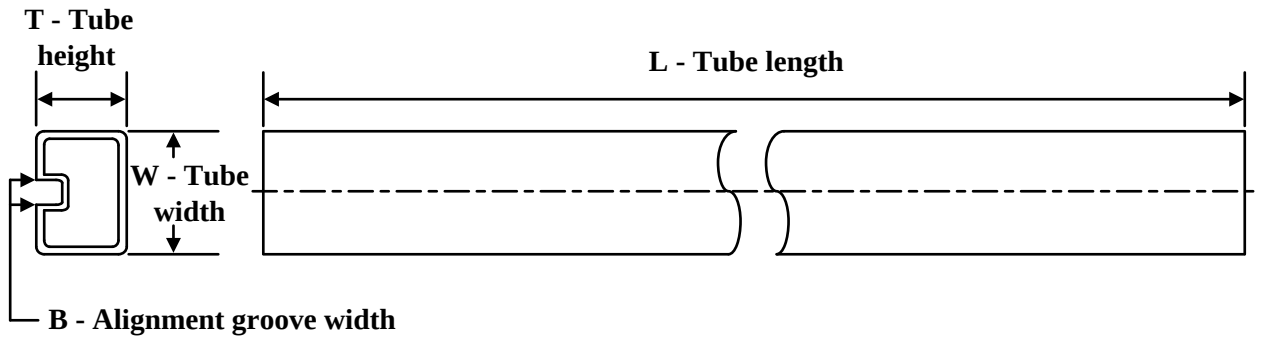
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54625PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54625PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
TPS54625PWP.A	PWP	HTSSOP	14	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

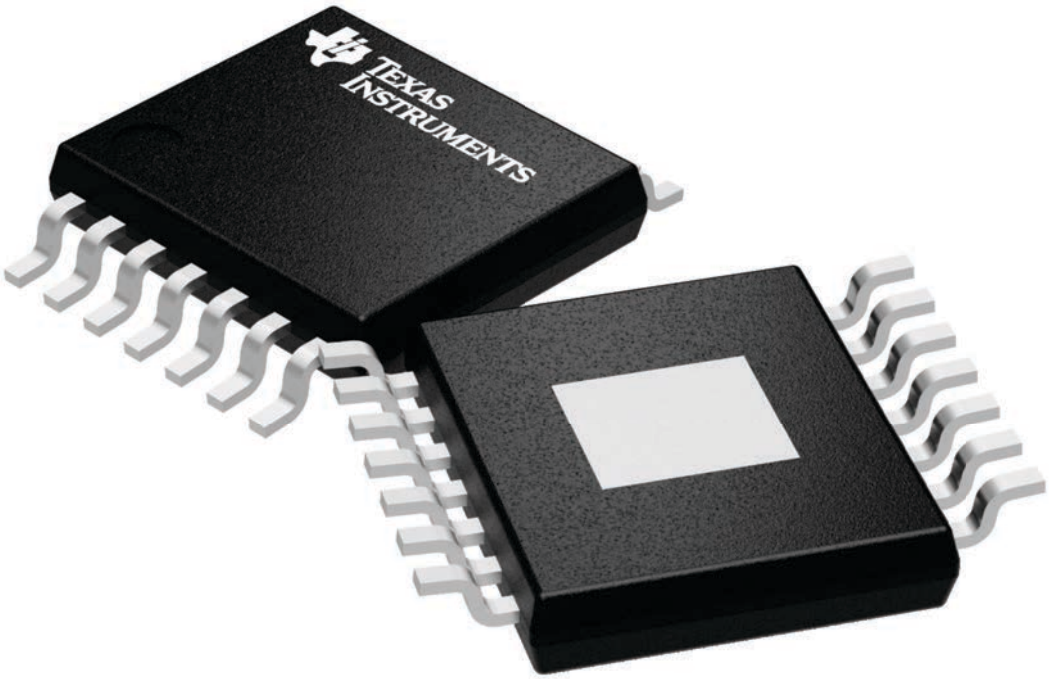
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



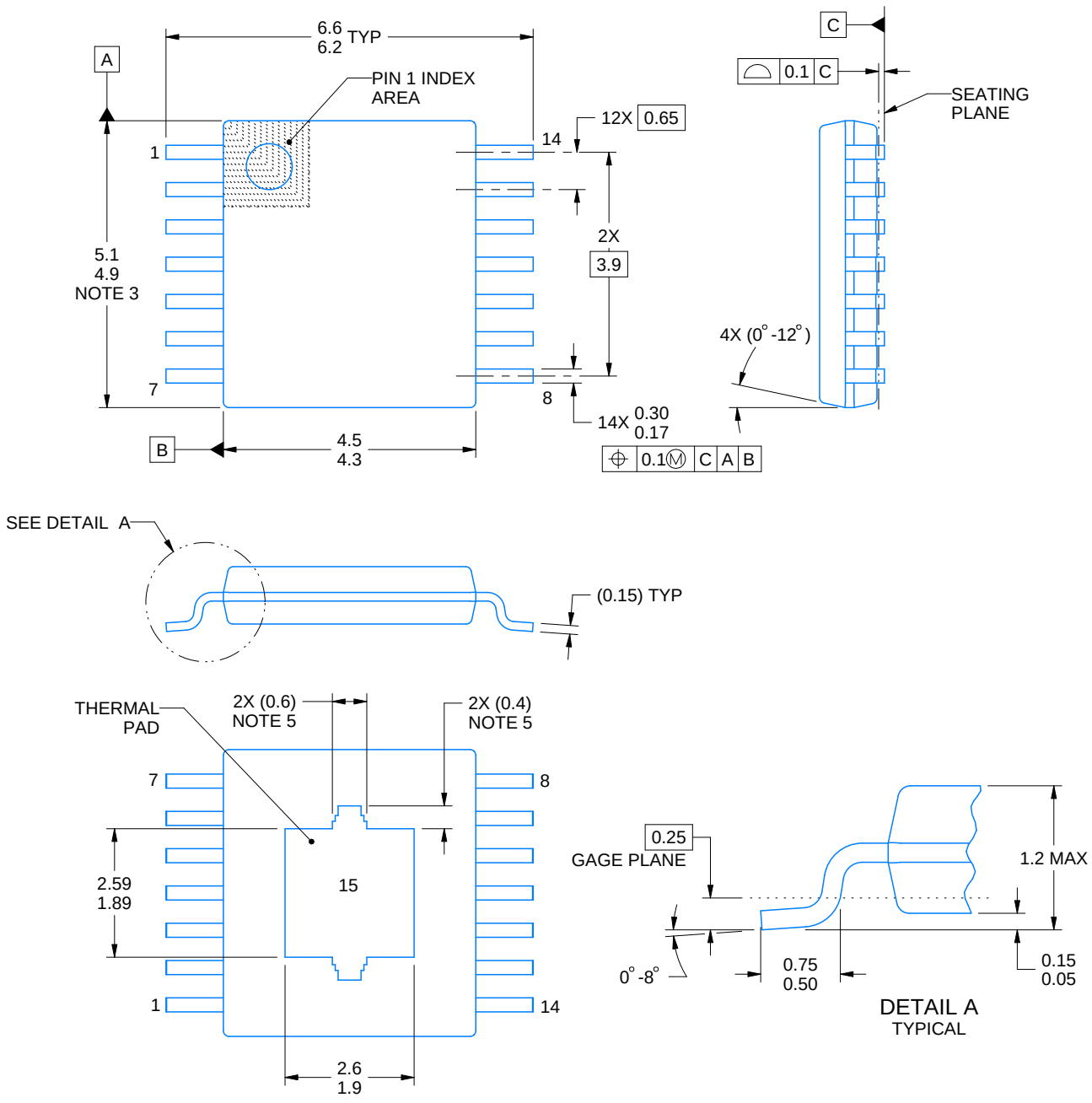
4224995/A

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

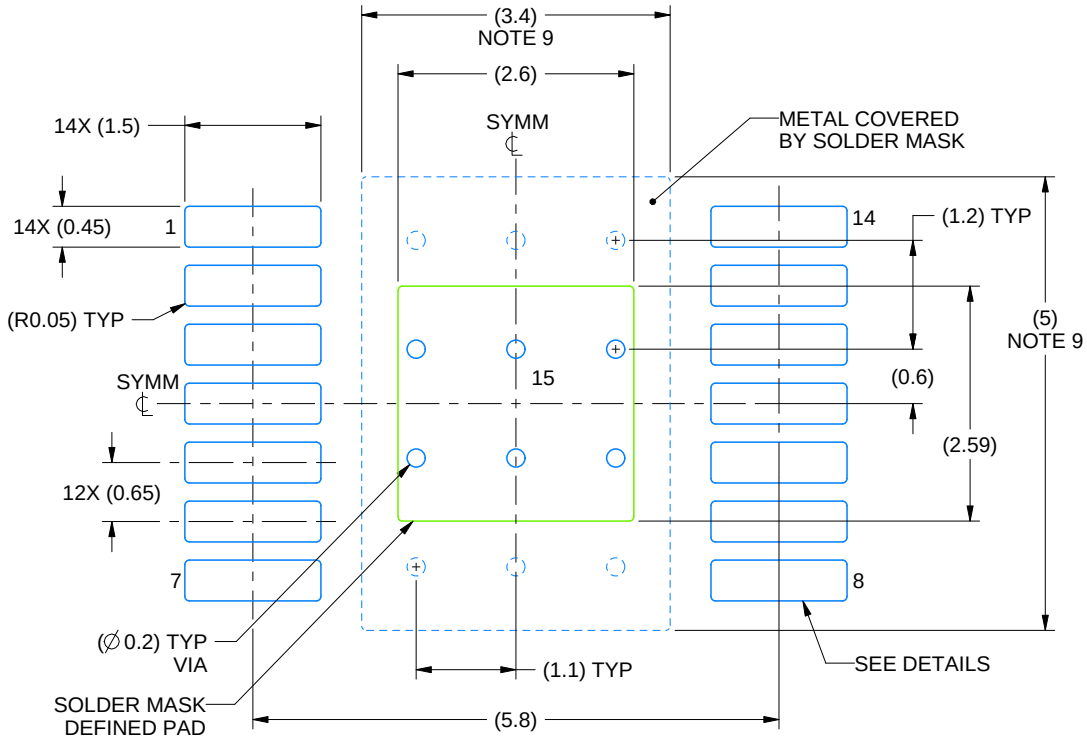
SMALL OUTLINE PACKAGE



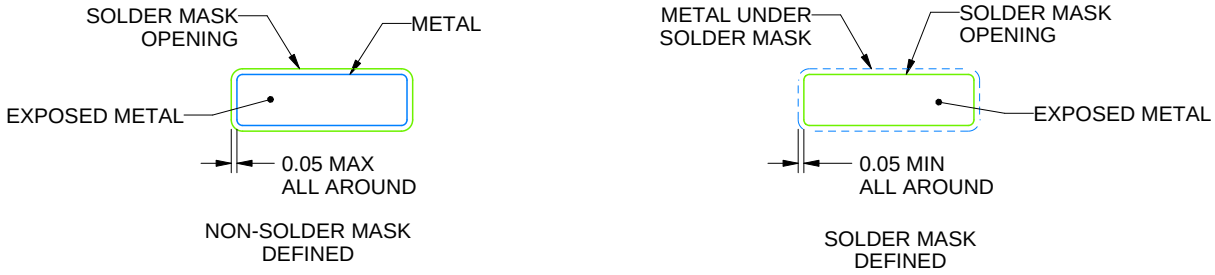
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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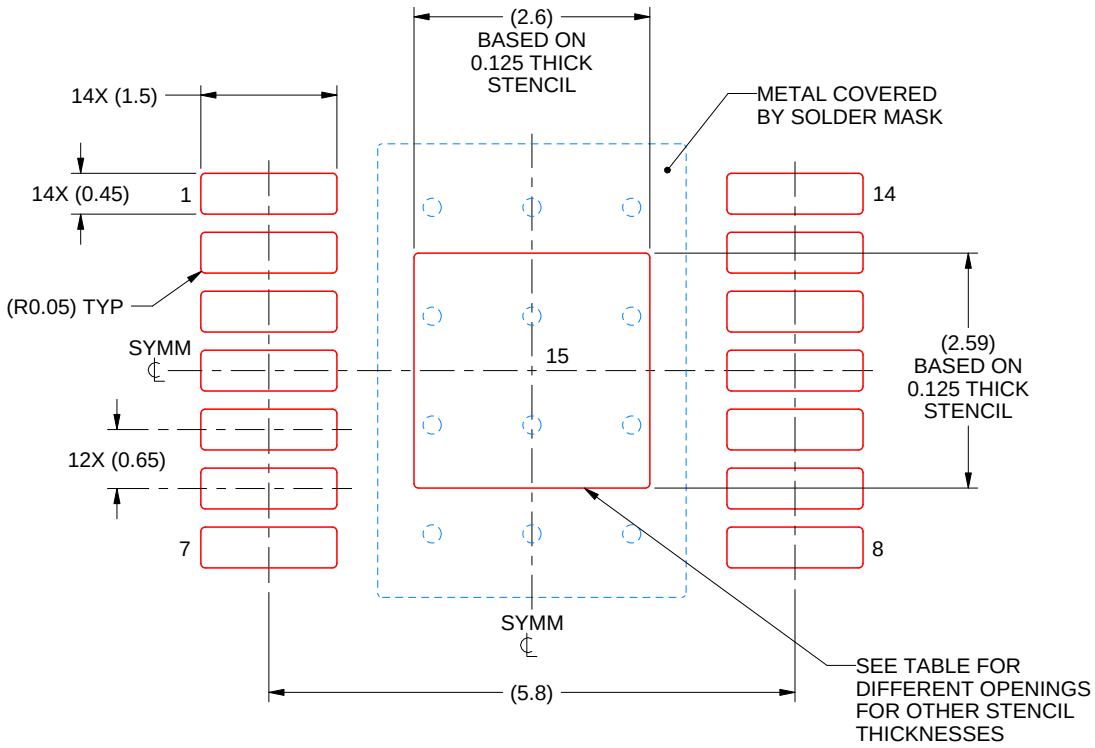
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

4229706/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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最后更新日期：2025 年 10 月