具有 ECO-Mode™ 的 4.5V 至 18V 输入，6.5A 同步降压 SWIFT™ 转换器

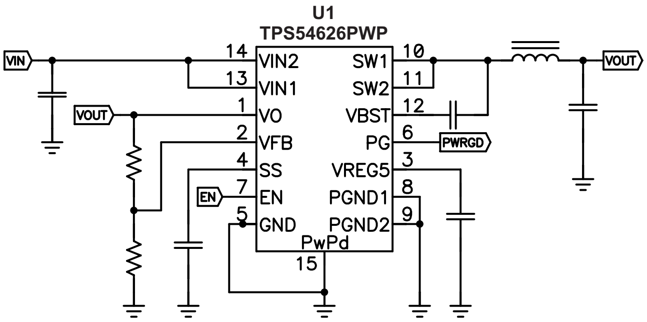
查询样品: TPS54626

特性

- **D-CAP2™** 模式支持快速瞬态响应
- 低输出纹波，支持陶瓷输出电容器
- 宽 **VIN** 输入电压范围：**4.5V** 至 **18V**
- 输出电压范围：**0.76V** 至 **5.5V**
- 高效率集成型场效应晶体管 **(FET)** 针对更低占空比应用进行了优化 — **36mΩ**（高侧）与 **28 mΩ**（低侧）
- 关断时的高效率，流耗不足 **10μA**
- 高初始带隙基准精度
- 可调软启动
- 预偏置软启动
- **650kHz** 开关频率 **(f_{SW})**
- 逐周期限流
- 电源正常输出
- 自动跳跃 **Eco-mode™** 为了在轻负载下实现高效率

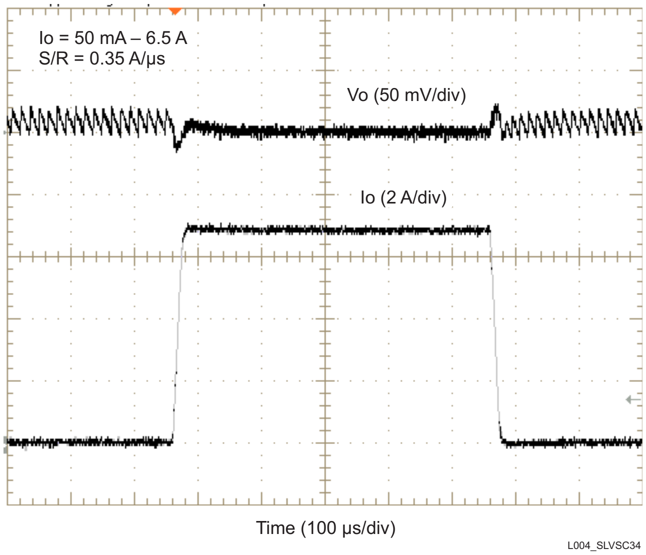
应用范围

- 低电压系统的广泛应用
  - 数字电视电源
  - 高清 **Blu-ray Disc™** 播放器
  - 网络家庭终端设备
  - 数字机顶盒 **(STB)**



说明

TPS54626 是一款自适应接通时间 D-CAP2™ 模式同步降压转换器。 TPS54626 可帮助系统设计人员用成本有效、低组件数量、低待机电流解决方案来完成不同终端设备的电源总线调节器集。 TPS54626 的主控制环路采用 D-CAP2™ 模式控制，此模式无需外部补偿组件便可实现极快的瞬态响应。 自适应接通时间支持高负载条件下脉宽调制 (PWM) 模式与轻负载下减频运行之间的无缝操作，以实现高效率。 TPS54626 的专有电路还可使该器件能够适应诸如高分子聚合物电容器 (SP-CAP) 等低等效串联电阻 (ESR) 输出电容器以及超低 ESR 陶瓷电容器。 该器件在 4.5V 至 18V 的 VIN 输入电源电压范围内运行。 输出电压可在 0.76V 与 5.5V 之间设定。该器件还特有一个可调软启动时间和一个电源正常功能。 TPS54626 采用 14 引脚散热薄型小外形尺寸 (HTSSOP) 封装，设计工作温度介于 -40°至 85° 之间。



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English Data Sheet: SLVSC34

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2) (3)	ORDERABLE PART NUMBER	PIN	TRANSPORT MEDIA
–45°C to 85°C	PWP	TPS54626PWP	14	Tube
		TPS54626PWPR		Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) All package options have Cu NIPDAU lead/ball finish.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

			VALUE		UNIT
			MIN	MAX	
V_I	Input voltage range	VIN1, VIN2, EN	–0.3	20	V
		VBST	–0.3	26	V
		VBST (10 ns transient)	–0.3	28	V
		VBST (vs Sw1, SW2)	–0.3	6.5	V
		VFB, VO, SS, PG	–0.3	6.5	V
		SW1, SW2	–2	20	V
		SW1, SW2 (10 ns transient)	–3	22	V
V_O	Output voltage range	VREG5	–0.3	6.5	V
		PGND1, PGND2	–0.3	0.3	V
V_{diff}	Voltage from GND to POWERPAD		–0.2	0.2	V
ESD rating	Electrostatic discharge	Human Body Model (HBM)		2	kV
		Charged Device Model (CDM)		500	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54626	UNITS
		PWP (14 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	40.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	28.7	
θ_{JB}	Junction-to-board thermal resistance	24.2	
ψ_{JT}	Junction-to-top characterization parameter	0.8	
ψ_{JB}	Junction-to-board characterization parameter	23.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	18	V
V_I	Input voltage range	VBST	–0.1	24	V
		VBST (10 ns transient)	–0.1	27	
		VBST (vs SW)	–0.1	6.0	
		SS, PG	–0.1	5.7	
		EN	–0.1	18	
		VO, VFB	–0.1	5.5	
		SW1, SW2	–1.8	18	
		SW1, SW2 (10 ns transient)	–3	21	
		PGND1, PGND2	–0.1	0.1	
V_O	Output voltage range	VREG5	–0.1	5.7	V
I_O	Output Current range	I_{VREG5}	0	5	mA
R_{PG}	Power Good resistor		25	150	kΩ
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	150	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating - non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5 V, V_{VFB} = 0.8 V		950	1400	μA
I_{VINSDN}	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V		3.6	10	μA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	En	1.6			V
V_{ENL}	EN low-level input voltage	EN			0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	200	400	800	kΩ
VFB VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	VFB threshold voltage	VFB voltage light load mode, T_A = 25°C, V_O = 1.05 V, I_O = 10mA		772		mV
		T_A = 25°C, V_O = 1.05 V, continuous mode	757	765	773	
		T_A = 0°C to 85°C, V_O = 1.05 V, continuous mode(1)	753		777	
		T_A = –40°C to 85°C, V_O = 1.05 V, continuous mode(1)	751		779	
I_{VFB}	VFB input current	V_{VFB} = 0.8 V, T_A = 25°C		0	±0.15	μA
R_{Dischg}	V_O discharge resistance	V_{EN} = 0 V, V_O = 0.5 V, T_A = 25°C		100	150	Ω
VREG5 OUTPUT						
V_{VREG5}	VREG5 output voltage	T_A = 25°C, 6 V < V_{IN} < 18 V, 0 < I_{VREG5} < 5 mA	5.2	5.5	5.7	V
I_{VREG5}	Output current	V_{IN} = 6 V, V_{VREG5} = 4 V, T_A = 25°C	20			mA
MOSFET						
R_{dsonh}	High side switch resistance	T_A = 25°C, VBST-SW1,2 = 5.5V		36		mΩ
R_{dsonl}	Low side switch resistance	T_A = 25°C		28		mΩ

(1) Not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

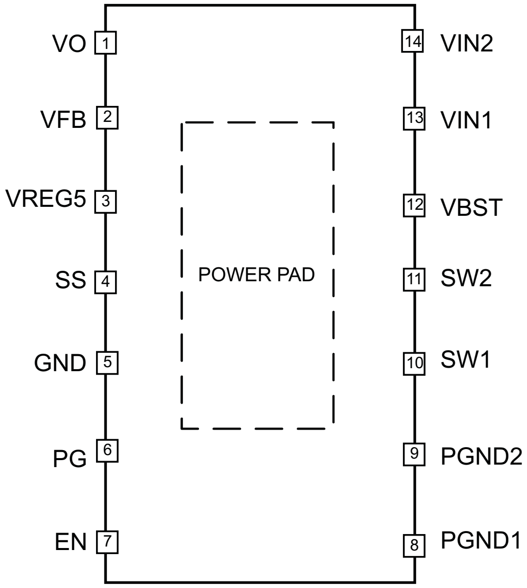
over operating free-air temperature range, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{ocl}	Current limit	L = 1.5 μH (2),	7.2	8.2	9.5	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature (2)		165		°C
		Hysteresis (2)		35		
ON-TIME TIMER CONTROL						
T_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		150		ns
$T_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.7 V		260	310	ns
SOFT START						
I_{SSC}	SS charge current	V_{SS} = 1.0 V	4.2	6.0	7.8	μA
I_{SSD}	SS discharge current	V_{SS} = 0.5 V	1.5	3.3		mA
POWER GOOD						
V_{THPG}	PG threshold	V_{VFB} rising (good)	85%	90%	95%	
		V_{VFB} falling (fault)		85%		
I_{PG}	PG sink current	V_{PG} = 0.5 V	2.5	5		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	120%	125%	130%	
T_{OVPDEL}	Output OVP prop delay			10		μs
V_{UVP}	Output UVP trip threshold	UVP detect	60%	65%	70%	
		Hysteresis		10%		
T_{UVPDEL}	Output UVP delay			0.25		ms
T_{UVPEN}	Output UVP enable delay	Relative to soft-start time		X 1.7		
UVLO						
V_{UVLO}	UVLO threshold	Wake up VREG5 voltage	3.45	3.75	4.05	V
		Hysteresis VREG5 voltage	0.13	0.32	0.48	

(2) Not production tested.

DEVICE INFORMATION

PWP PACKAGE
(TOP VIEW)



PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NUMBER	
VO	1	Connect to output of converter. This pin is used for output discharge function.
VFB	2	Converter feedback input. Connect with feedback resistor divider.
VREG5	3	5.5V power supply output. A Capacitor (typical 1µF) should be connected to GND. VREG5 is not active when EN is low.
SS	4	Soft start control. An external capacitor should be connected to GND.
GND	5	Signal ground pin.
PG	6	Open drain power good output
EN	7	Enable control input. EN is active high and must be pulled up to enable the device.
PGND1, PGND2	8, 9	Ground returns for low-side MOSFET. Also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1, SW2	10,11	Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparator.
VBST	12	Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to respective SW1,SW2 terminals. An internal PN diode is connected between VREG5 and VBST pin.
VIN1,VIN2	13,14	Power Input and connected to high side NFET drain.
		Supply Input for 5V internal linear regulator for the control circuitry
PowerPAD™	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND

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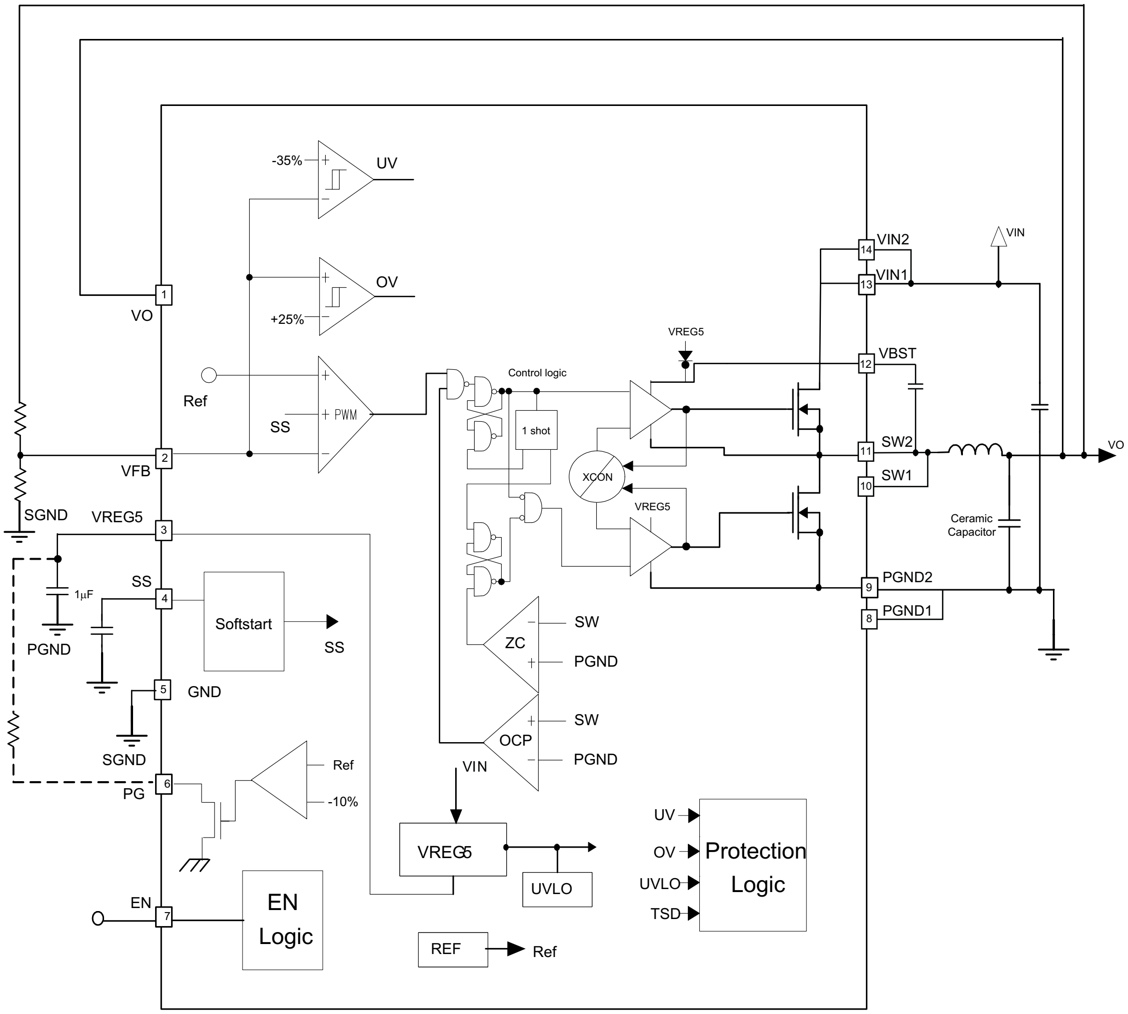
FUNCTIONAL BLOCK DIAGRAM (HTSSOP)



OVERVIEW

The TPS54626 is a 6.5-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs and auto-skip Eco-mode™ to improve light lode efficiency. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

DETAILED DESCRIPTION

PWM Operation

The main control loop of the TPS54626 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable with virtually no ripple at the output.

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At the beginning of each cycle, the high-side MOSFET is turned on. The MOSFET is turned off after the internal one-shot timer expires. The one-shot timer is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

PWM Frequency and Adaptive On-Time Control

TPS54626 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54626 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. Therefore, when duty ratio is VOUT/VIN, the frequency is constant.

Auto-Skip Eco-Mode™ Control

The TPS54626 is designed with Auto-Skip mode to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as is was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{1}$$

Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6 µA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 2. VFB voltage is 0.765 V and SS pin source current is 6 µA.

$$t_{SS}(\text{ms}) = \frac{C_{SS}(\text{nF}) \text{ x } V_{REF} \times 1.1}{I_{SS}(\mu\text{A})} = \frac{C_{SS}(\text{nF}) \text{ x } 0.765 \times 1.1}{6} \tag{2}$$

TPS54626 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage V_{FB}), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

Power Good

The TPS54626 has power good open drain output. The power-good function is activated after soft start has finished. The power good function becomes active after 1.7 times soft-start time. When the output voltage becomes within –10% of the target value, internal comparators detect power good state and the power good signal becomes high. Rpg resistor value, which is connected between PG and VREG5, is required from 25kΩ to 150kΩ. If the feedback voltage goes under 15% of the target value, the power good signal becomes low.

Output Discharge Control

TPS54626 discharges the output when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO and thermal shutdown). The device discharges the output using an internal 100-Ω MOSFET which is connected from VO to PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

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Current Protection

The output over-current protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current Iout. If the measured voltage is above the voltage proportional to the current limit, then the device constantly monitors the low side FET switch voltage, which is proportional to the switch current, during the low-side on-time.

The converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and new switching cycle begins. IN subsequent switching cycles, the on-time is set to fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current is higher than the over-current threshold. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output under-voltage protection circuit to be activated. This protection itself is non-latching.

Over/Under Voltage Protection

TPS54626 detects over and under voltage conditions by monitoring the feedback voltage (VFB). This function is enabled after approximately 1.7 x times the softstart time.

When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and the circuit latches and both the high-side MOSFET driver and the low-side MOSFET driver turn off.

When the feedback voltage becomes lower than 65% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250us, the device latches off both internal top and bottom MOSFET.

UVLO Protection

Under voltage lock out protection (UVLO) monitors the voltage of the V_{REG5} pin. When the V_{REG5} voltage is lower than UVLO threshold voltage, the TPS54626 is shut off. This is protection is non-latching.

Thermal Shutdown

Thermal protection is self-activating. If the junction temperature exceeds the threshold value (typically 165°C), the TPS54626 is shut off. This protection is non-latching.

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TYPICAL CHARACTERISTICS

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

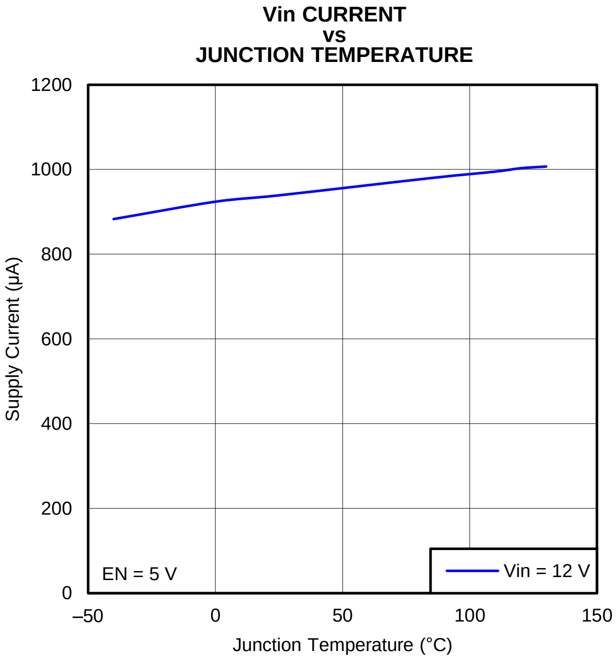

Figure 1.

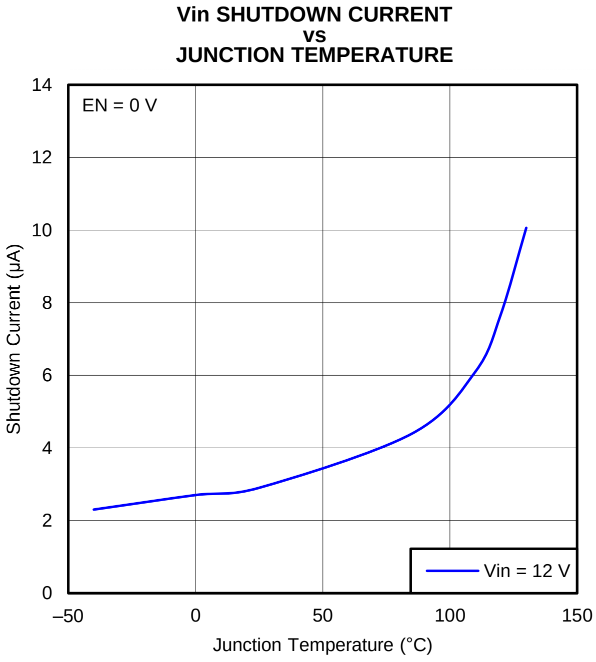

Figure 2.

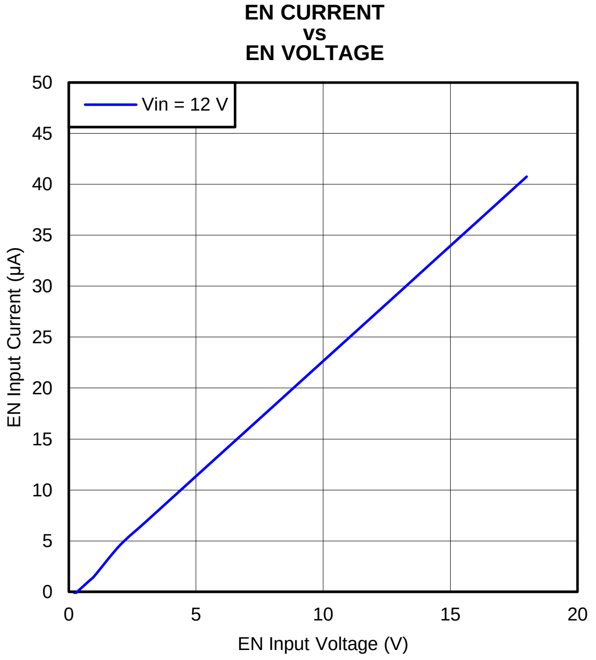

Figure 3.

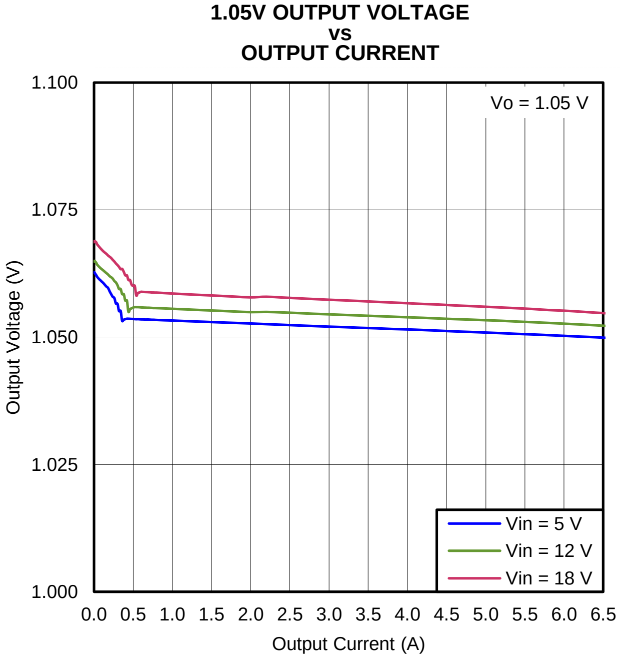

Figure 4.

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TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

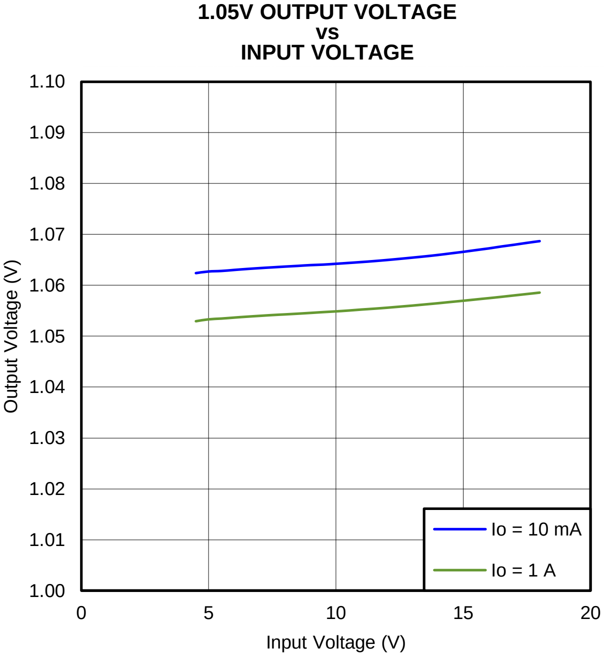
1.05V OUTPUT VOLTAGE vs INPUT VOLTAGE

Figure 5.

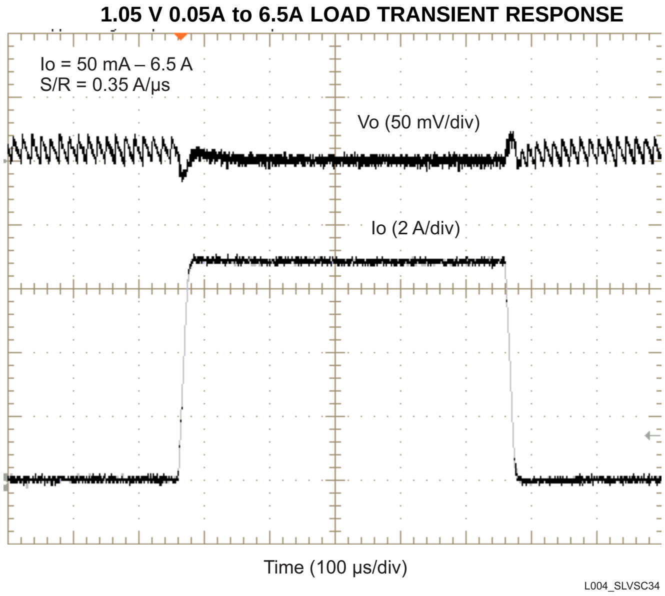
1.05 V 0.05A to 6.5A LOAD TRANSIENT RESPONSE

Figure 6.

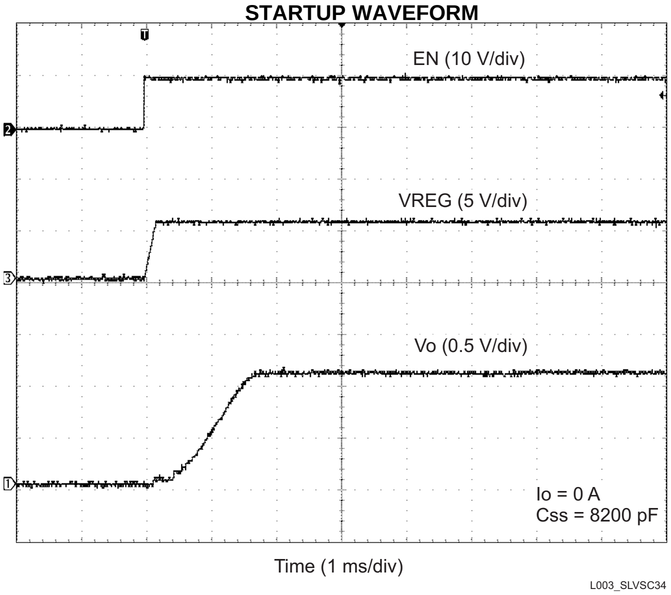
STARTUP WAVEFORM

Figure 7.

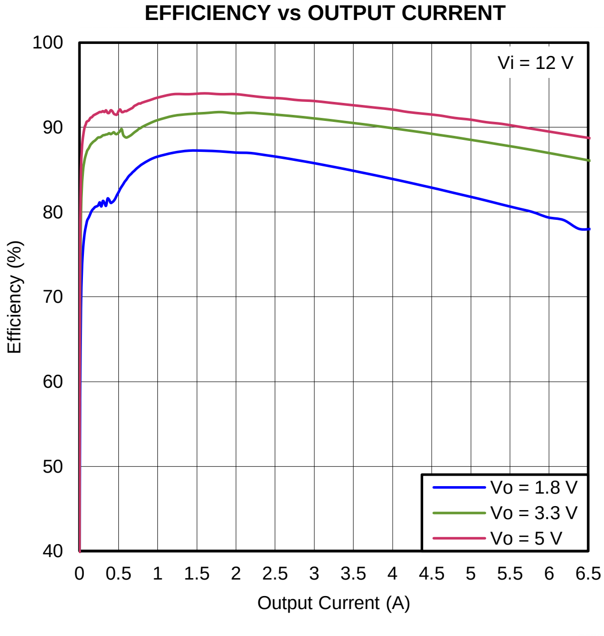
EFFICIENCY vs OUTPUT CURRENT

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

LIGHT LOAD EFFICIENCY vs OUTPUT CURRENT

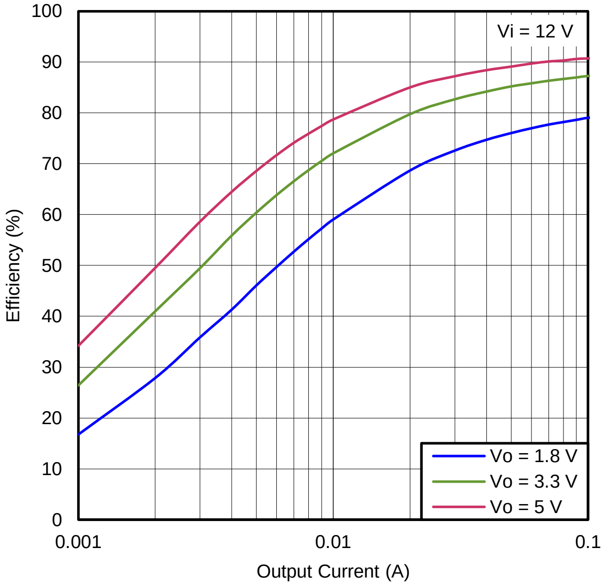

Figure 9.

SWITCHING FREQUENCY vs INPUT VOLTAGE (IO=1A)

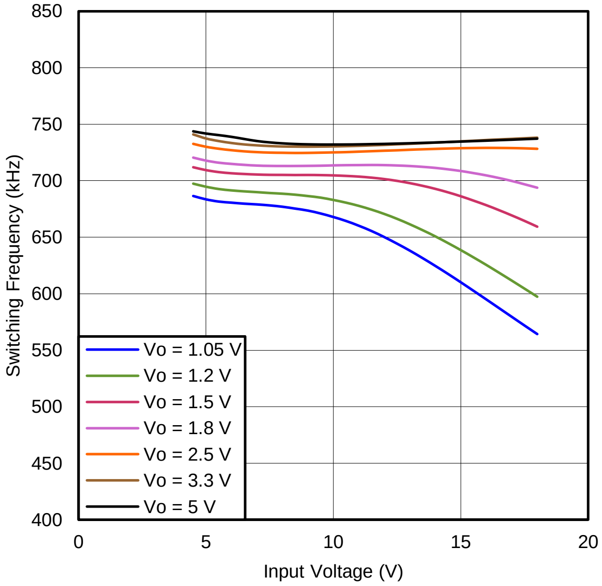

Figure 10.

SWITCHING FREQUENCY vs OUTPUT CURRENT

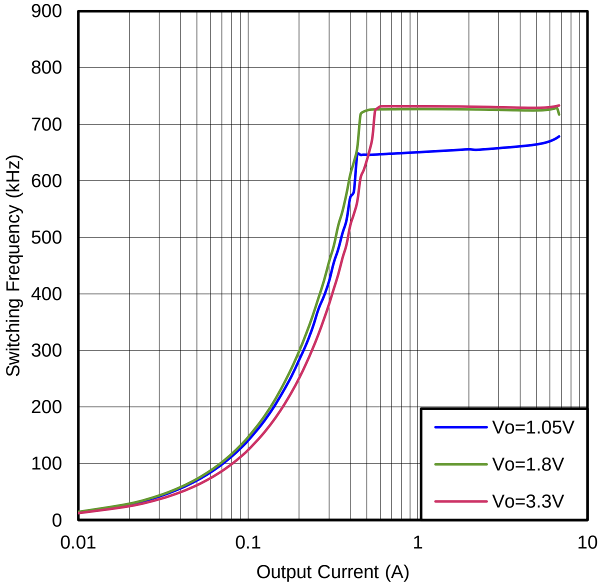

Figure 11.

VFB VOLTAGE vs JUNCTION TEMPERATURE

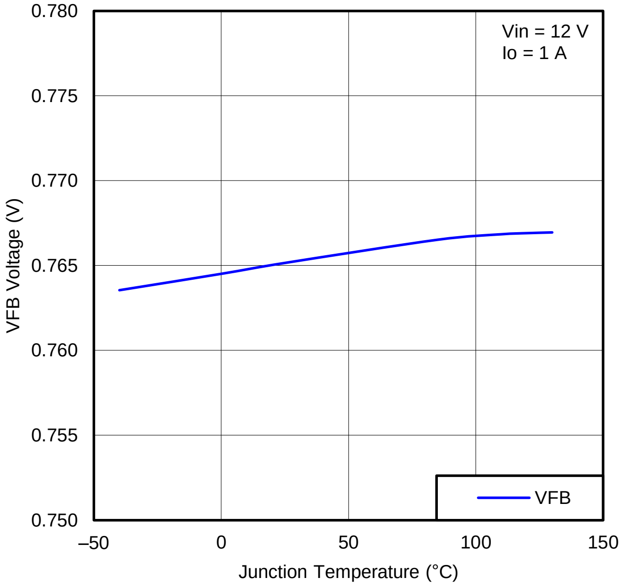

Figure 12.

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TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, T_A = 25 °C (unless otherwise noted)

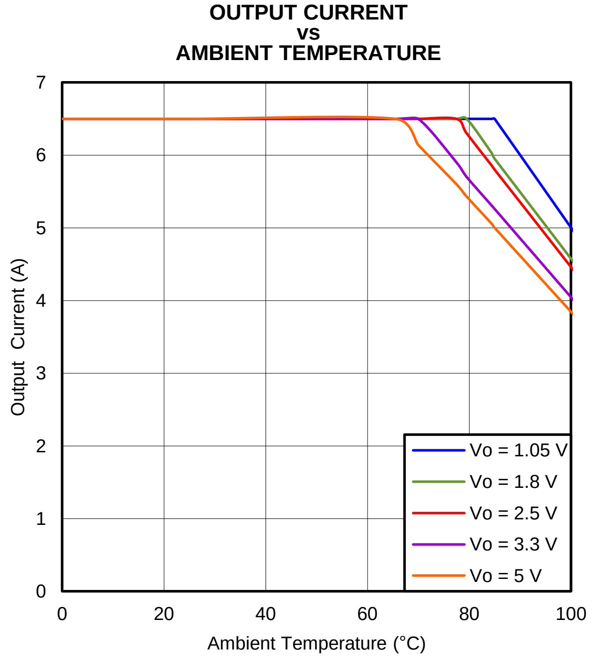

Figure 13.

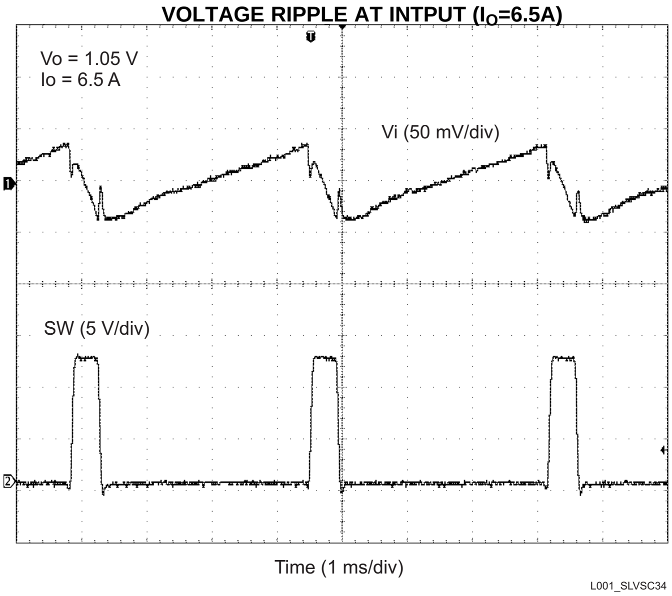

Figure 14.

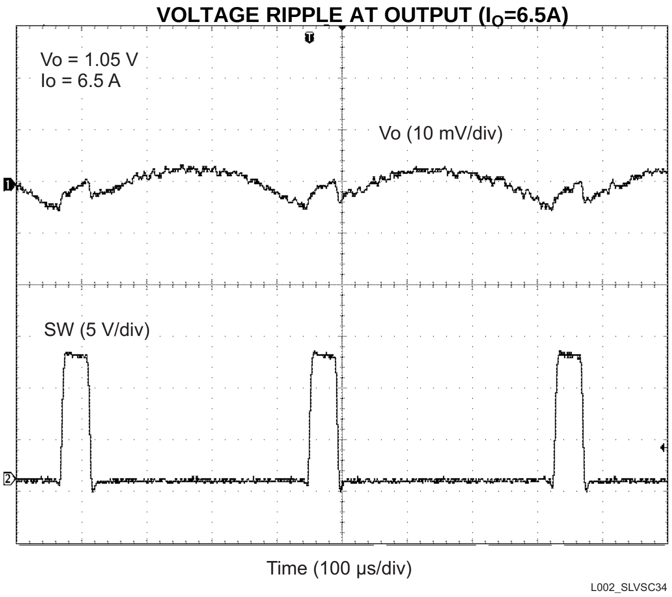

Figure 15.

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DESIGN GUIDE

Step By Step Design Procedure

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

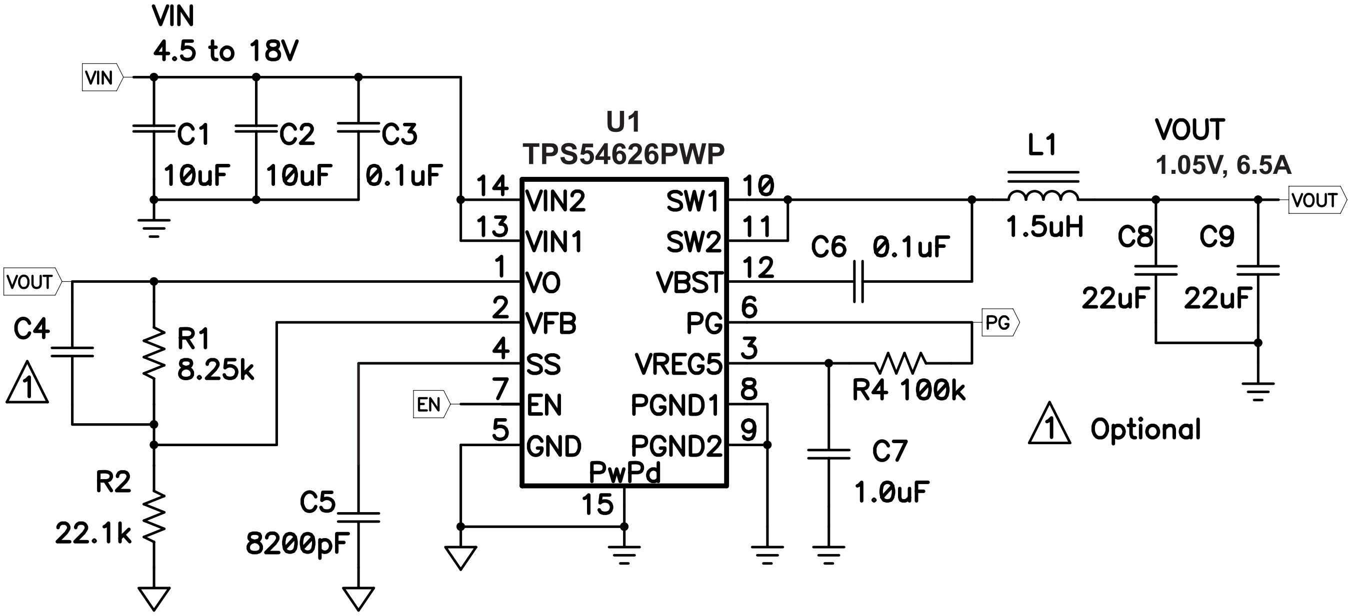

Figure 16. Schematic

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 3 to calculate V_{OUT}

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.765 \bullet \left(1 + \frac{R1}{R2}\right) \tag{3}$$

Output Filter Selection

The output filter used with the TPS54626 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{4}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54626. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 4 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1

Table 1. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)[1]	L1 (µH)	C8 + C9 (µF)
1	6.81	22.1	5 - 220	1.0 - 1.5 - 4.7	22 - 68
1.05	8.25	22.1	5 - 220	1.0 - 1.5 - 4.7	22 - 68
1.2	12.7	22.1	5 - 100	1.0 - 1.5 - 4.7	22 - 68
1.5	21.5	22.1	5 - 68	1.0 - 1.5 - 4.7	22 - 68
1.8	30.1	22.1	5 - 22	1.2 - 1.5 - 4.7	22 - 68
2.5	49.9	22.1	5 - 22	1.5 - 2.2 – 4.7	22 - 68
3.3	73.2	22.1	5 - 22	1.8 - 2.2 – 4.7	22 - 68
5	124	22.1	5 - 22	2.5 - 3.3 – 4.7	22 - 68

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 5, Equation 6 and Equation 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{SW}.

Use 650 kHz for f_{SW}. and also use 1.5µH for LO Make sure the chosen inductor is rated for the peak current of Equation 6 and the RMS current of Equation 7.

$$Ilp-p = \frac{V_{OUT}}{V_{IN\,(max)}} \bullet \frac{V_{IN\,(max)} - V_{OUT}}{L_O \bullet f_{SW}} \tag{5}$$

$$I_{lpeak} = I_O + \frac{Ilp-p}{2} \tag{6}$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} Ilp-p^2} \tag{7}$$

For this design example, the calculated peak current is 7.01 A and the calculated RMS current is 6.51 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54626 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22µF to 68µF. Use Equation 8 to determine the required RMS current rating for the output capacitor

$$I_{CO(RMS)} = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{\sqrt{12} \bullet V_{IN} \bullet L_O \bullet f_{SW}} \tag{8}$$

For this design two TDK C3216X5R0J226M 22µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.284 A and each output capacitor is rated for 4 A.

Input Capacitor Selection

The TPS54626 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 uF. is recommended for the decoupling capacitor. An additional 0.1 µF capacitor from pin 14 to ground is recommended to improve the stability of the over-current limit function. The capacitor voltage rating needs to be greater than the maximum input voltage.

Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

VREG5 Capacitor Selection

A 1-µF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

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THERMAL INFORMATION

This PowerPad™ package incorporates an exposed thermal pad that is designed to be directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD™ Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD™ Made Easy*, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in the following illustration.

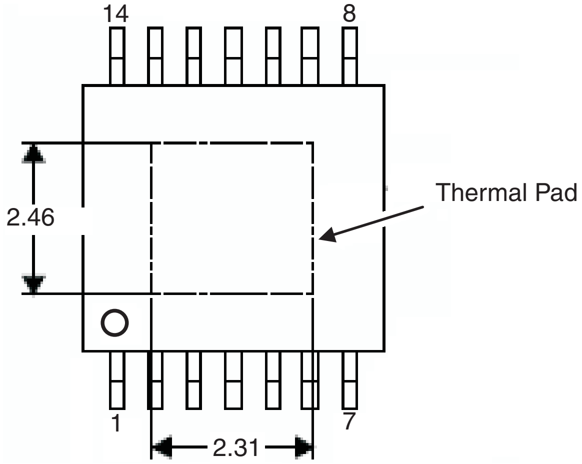

Figure 17. Thermal Pad Dimensions

LAYOUT CONSIDERATIONS

1. A top side area should be filled with ground as much as possible due to relatively higher current output device.
2. The ground area under the device thermal pad should be large as possible and directly connect to the thermal pad. Also 2nd, 3rd and 4th PCB layer should be connected to ground directly from the thermal pad.
3. Keep the input switching current loop as small as possible.
4. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
5. Keep analog and non-switching components away from switching components.
6. Make a single point connection from the signal ground to power ground.
7. Do not allow switching current to flow under the device.
8. Keep the pattern lines for VIN and PGND broad.
9. Exposed pad of device must be connected to PGND with solder.
10. VREG5 capacitor should be placed near the device, and connected PGND.
11. Output capacitor should be connected to a broad pattern of the PGND.
12. Voltage feedback loop should be as short as possible, and preferably with ground shield.
13. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
14. Providing sufficient via is preferable for VIN, SW and PGND connection.
15. PCB pattern for VIN, SW, and PGND should be as broad as possible.
16. VIN Capacitor should be placed as near as possible to the device.

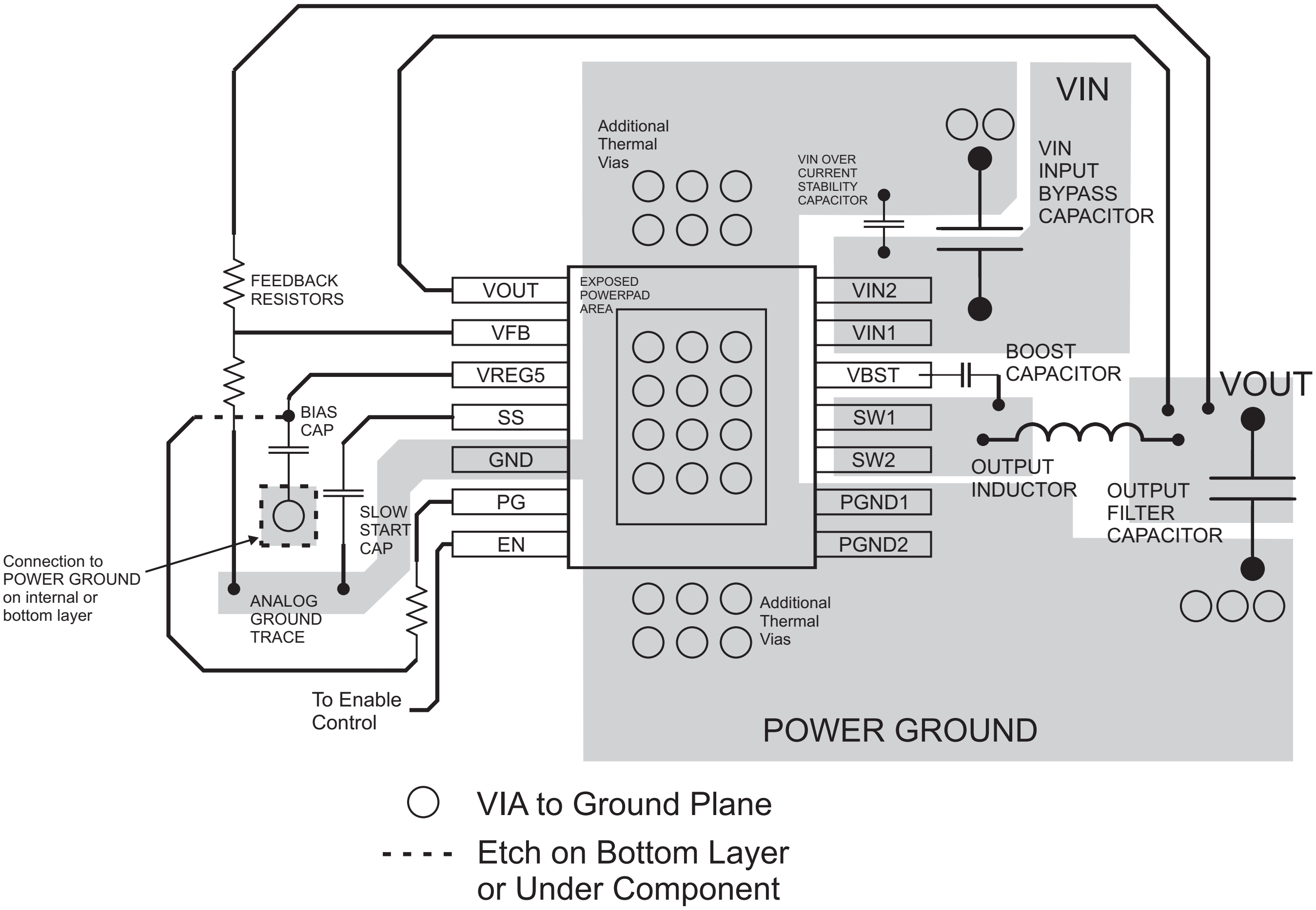

Figure 18. PCB Layout for PWP Package

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54626PWP	Active	Production	HTSSOP (PWP) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54626
TPS54626PWP.A	Active	Production	HTSSOP (PWP) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54626
TPS54626PWPR	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54626
TPS54626PWPR.A	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54626
TPS54626PWPRG4	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54626
TPS54626PWPRG4.A	Active	Production	HTSSOP (PWP) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS54626

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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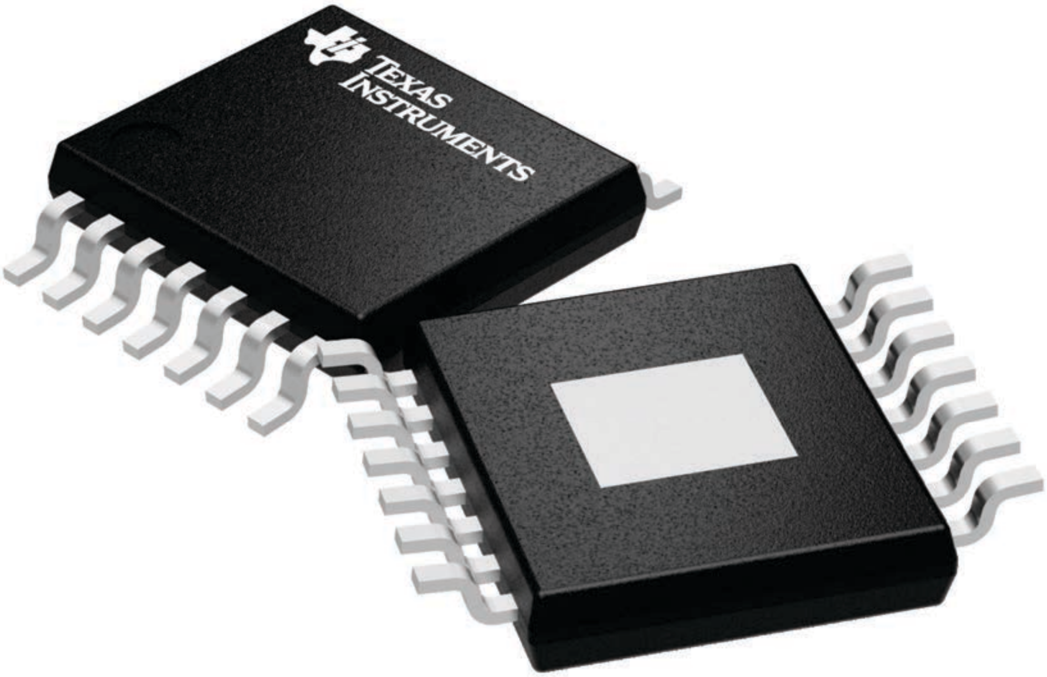
PWP 14

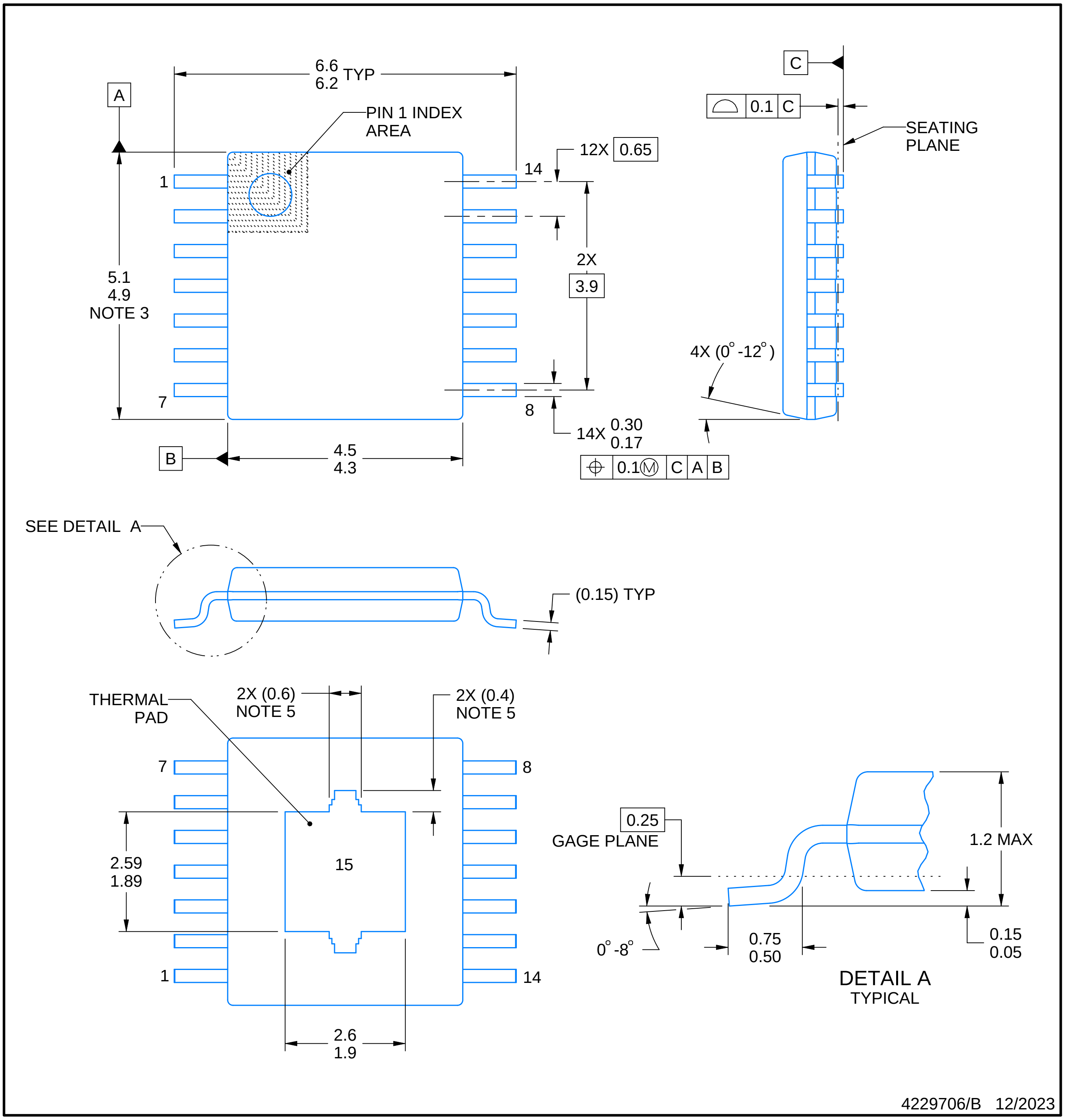
PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



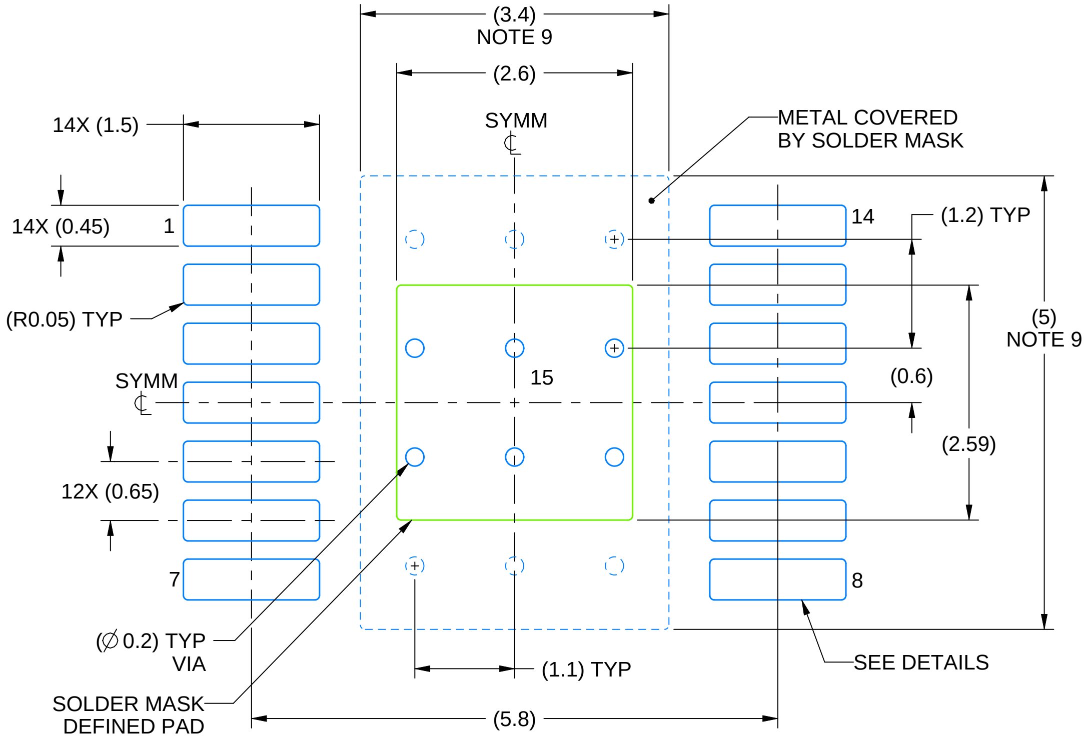


4229706/B 12/2023

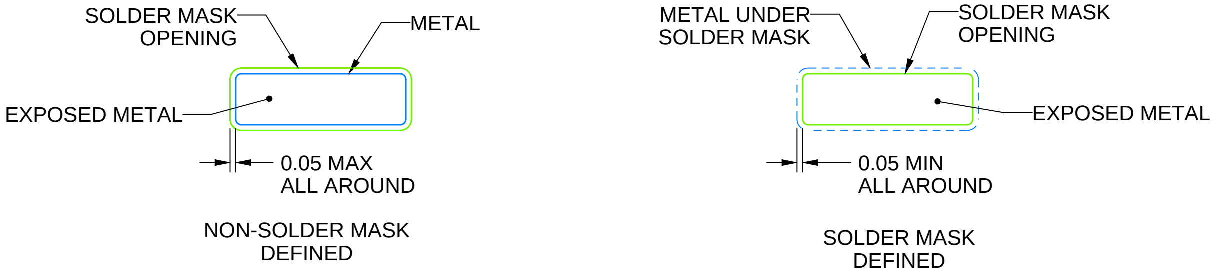
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



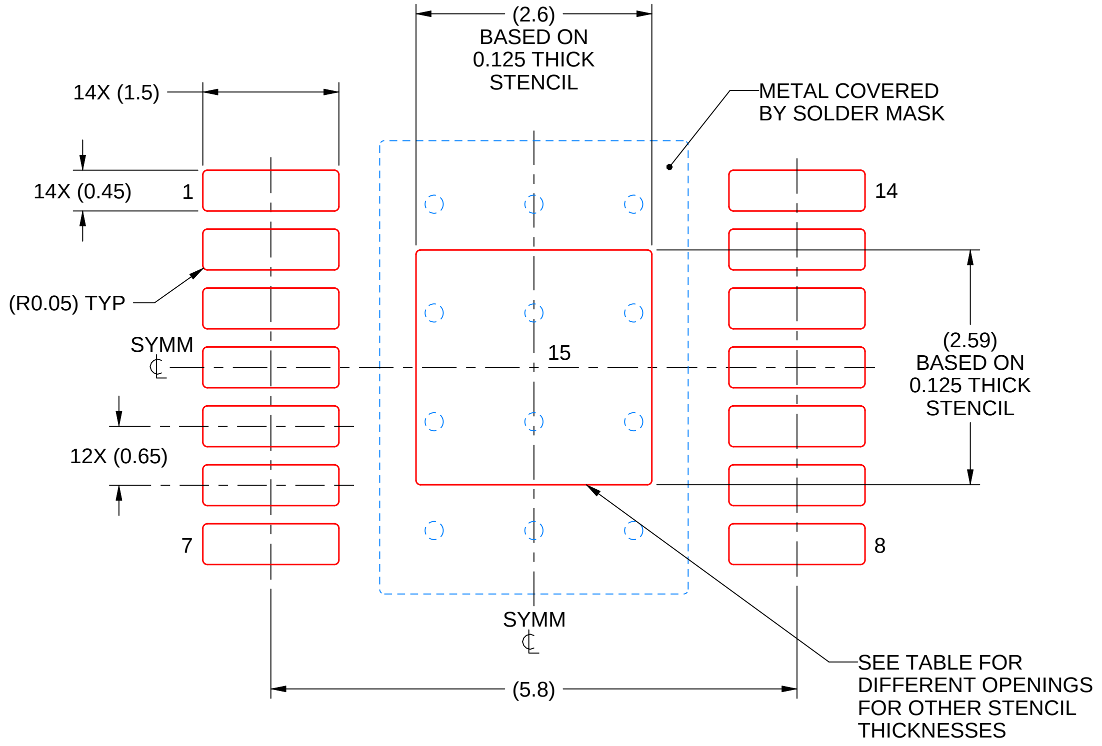
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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