TPS61170 1.2-A High-Voltage Boost Converter in 2-mm x 2-mm^2 QFN Package

1 Features

- 3-V to 18-V Input Voltage Range
- High Output Voltage: Up to 38 V
- 1.2-A Integrated Switch
- 1.2-MHz Fixed Switching Frequency
- 12 V at 300 mA and 24 V at 150 mA From 5-V Input (Typical)
- Up to 93% Efficiency
- *On-The-Fly* Output Voltage Reprogramming
- Skip-Switching Cycle for Output Regulation at Light Load
- Built-in Soft Start
- 6-Pin, 2-mm × 2-mm QFN Package

2 Applications

- 5-V to 12-V and 24-V, 12-V to 24-V Boost Converter
- Buck Boost Regulation Using SEPIC Topology
- ADSL Modems

3 Description

The TPS61170 is a monolithic, high-voltage switching regulator with integrated 1.2-A, 40-V power MOSFET. The device can be configured in several standard switching-regulator topologies, including boost and SEPIC. The device has a wide input-voltage range to support applications with input voltage from multicell batteries or regulated 5-V, 12-V power rails.

The TPS61170 operates at a 1.2-MHz switching frequency, allowing the use of low-profile inductors and low-value ceramic input and output capacitors. External loop compensation components give the user flexibility to optimize loop compensation and transient response. The device has built-in protection features, such as pulse-by-pulse overcurrent limit, soft start, and thermal shutdown.

The FB pin regulates to a reference voltage of 1.229 V. The reference voltage can be lowered using a 1-wire digital interface (Easyscale™ protocol) through the CTRL pin. Alternatively, a pulse width-modulation (PWM) signal can be applied to the CTRL pin. The duty cycle of the signal reduces the feedback reference voltage proportionally.

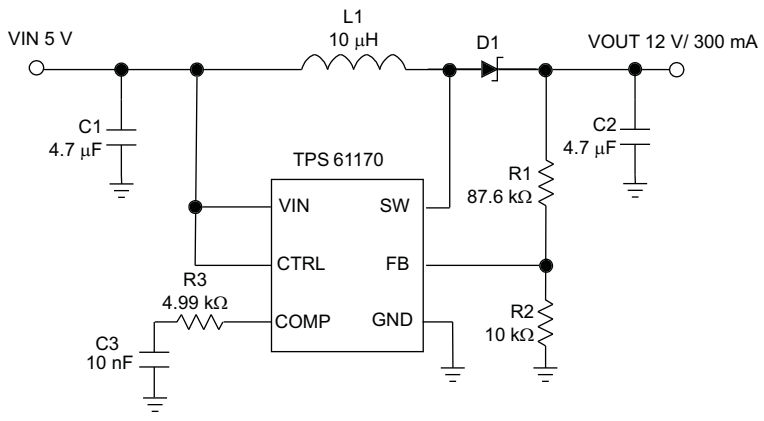
The TPS61170 is available in a 6-pin 2-mm × 2-mm QFN package, allowing a compact power-supply solution.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61170	VSON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application Schematic



L1: TOKO#A915_Y-100M
C1: Murata GRM188R61A475K
C2: Murata GRM21BR61E475K
D1: ONsemi MBR0540T1
*R3, C3: Compensation RC network

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5 Revision History

Changes from Revision C (April 2011) to Revision D **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

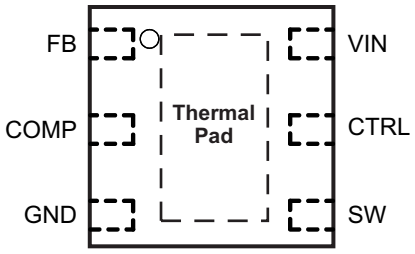
Changes from Revision B (November 2009) to Revision C **Page**

- Changed C1 part number in Figure 18, Figure 19, and Figure 20 from "GRM188RA475K " to "GRM21BR61E475K" 21

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6 Pin Configuration and Functions

QFN Package
6 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	2	O	Output of the transconductance error amplifier. Connect an external RC network to this pin to compensate the regulator.
CTRL	5	I	Control pin of the boost regulator. CTRL is a multifunctional pin which can be used to enable the device and control the feedback voltage with a PWM signal or for digital communications.
FB	1	I	Feedback pin for current. Connect to the center tap of a resistor divider to program the output voltage.
GND	3	O	Ground
SW	4	I	This is the switching node of the IC. Connect SW to the switched side of the inductor.
Thermal Pad			The thermal pad should be soldered to the analog ground plane to avoid thermal issue. If possible, use thermal vias to connect to ground plane for ideal power dissipation.
VIN	6	I	The input supply pin for the IC. Connect VIN to a supply voltage from 3 V to 18 V.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_I	Supply Voltages on VIN (2)	–0.3	20	V
	Voltages on CTRL (2)	–0.3	20	V
	Voltage on FB and COMP (2)	–0.3	3	V
	Voltage on SW (2)	–0.3	40	V
T_J	Operating Junction Temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

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7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_I	Input voltage range, VIN	3		18	V
V_O	Output voltage range	VIN		38	V
L	Inductor(1)	10		22	µH
C_I	Input capacitor	1			µF
C_O	Output capacitor(1)	1		10	µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) These values are recommended values that have been successfully tested in several applications. Other values may be acceptable in other applications but should be fully tested by the user.

7.4 Thermal Information

THERMAL METRIC(1)		TPS61170 DRV 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.0	
ψ_{JT}	Junction-to-top characterization parameter	1.7	
ψ_{JB}	Junction-to-board characterization parameter	36.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

VIN = 3.6 V, CTRL = VIN, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range, VIN		3.0		18	V
I_Q	Operating quiescent current into VIN	Device PWM switching no load			2.3	mA
I_{SD}	Shutdown current	CRTL=GND, VIN = 4.2 V			1	µA
UVLO	Under-voltage lockout threshold	VIN falling		2.2	2.5	V
V_{hys}	Under-voltage lockout Hysteresis			70		mV
ENABLE AND REFERENCE CONTROL						
$V_{(CTRLh)}$	CTRL logic high voltage	VIN = 3 V to 18 V	1.2			V
$V_{(CTRL)}$	CTRL logic low voltage	VIN = 3 V to 18 V			0.4	V
$R_{(CTRL)}$	CTRL pulldown resistor		400	800	1600	kΩ
t_{off}	CTRL pulse width to shutdown	CTRL high to low	2.5			ms
t_{es_det}	Easy Scale detection time(1)	CTRL pin low	260			µs
t_{es_delay}	Easy Scale detection delay		100			µs
t_{es_win}	Easy Scale detection window time		1			ms
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		1.204	1.229	1.254	V
$V_{(REF_PWM)}$	Voltage feedback regulation voltage under reprogram	V_{FB} = 492 mV	477	492	507	mV
I_{FB}	Voltage feedback input bias current	V_{FB} = 1.229 V			200	nA
f_S	Oscillator frequency		1.0	1.2	1.5	MHz
D_{max}	Maximum duty cycle	V_{FB} = 100 mV	90%	93%		
t_{min_on}	Minimum on pulse width			40		ns
I_{sink}	Comp pin sink current			100		µA
I_{source}	Comp pin source current			100		µA
G_{ea}	Error amplifier transconductance		240	320	400	µmho
R_{ea}	Error amplifier output resistance	5 pF connected to COMP		6		MΩ
f_{ea}	Error amplifier crossover frequency	5 pF connected to COMP		500		kHz
POWER SWITCH						
$R_{DS(on)}$	N-channel MOSFET on-resistance	VIN = 3.6 V		0.3	0.6	Ω
		VIN = 3.0 V			0.7	
I_{LN_NFET}	N-channel leakage current	V_{SW} = 35 V, T_A = 25°C			1	µA
OC and SS						
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	0.96	1.2	1.44	A
I_{LIM_Start}	Start up current limit	D = D_{max}		0.7		A
t_{Half_LIM}	Time step for half current limit			5		ms
t_{REF}	Vref filter time constant			180		µs
t_{step}	V_{REF} ramp up time			213		µs

(1) EasyScale communication is allowed immediately after the CTRL pin has been low for more than t_{es_det}. To select EasyScale mode, the CTRL pin must be low for more than t_{es_det} the end of t_{es_win}.

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Electrical Characteristics (continued)

VIN = 3.6 V, CTRL = VIN, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EasyScale TIMING						
t_{start}	Start time of program stream		2			µs
t_{EOS}	End time of program stream		2		360	µs
t_{H_LB}	High time low bit	Logic 0	2		180	µs
t_{L_LB}	Low time low bit	Logic 0	2 × t_{H_LB}		360	µs
t_{H_HB}	High time high bit	Logic 1	2 × t_{L_HB}		360	µs
t_{L_HB}	Low time high bit	Logic 1	2		180	µs
V_{ACKNL}	Acknowledge output voltage low	Open drain, R_{pullup} =15 kΩ to Vin			0.4	V
$t_{valACKN}$	Acknowledge valid time	See (2)			2	µs
t_{ACKN}	Duration of acknowledge condition	See (2)			512	µs
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

(2) Acknowledge condition active 0, this condition will only be applied if the RFA bit is set. Open drain output, line needs to be pulled high by the host with resistor load.

7.6 Typical Characteristics

Table 1. Table Of Graphs

Circuit of Figure 1, L = TOKO A915_Y-100M, D1 = ONsemi MBR0540T1, unless otherwise noted.		FIGURE
Efficiency	VIN = 5 V; VOUT = 12 V, 18 V, 24 V, 30 V	Figure 1
Efficiency	VIN = 5 V, 8.5 V, 12 V; VOUT = 24 V	Figure 2
Output voltage accuracy	I_{LOAD}= 100 mA	Figure 3
Switch current limit	T_A = 25°C	Figure 4
Switch current limit		Figure 5
Error amplifier transconductance		Figure 6
EasyScale step		Figure 7
PWM switching operation	VIN = 5 V; VOUT = 12 V; I_{LOAD}= 250 mA	Figure 14
Load transient response	VIN = 5 V; VOUT = 12 V; I_{LOAD}= 50 mA to 150 mA	Figure 15
Start-up	VIN = 5 V; VOUT = 12 V; I_{LOAD}= 250 mA	Figure 16
Skip-cycle switching	VIN = 9 V ; VOUT = 12 V, I_{LOAD}= 100 µA	Figure 17

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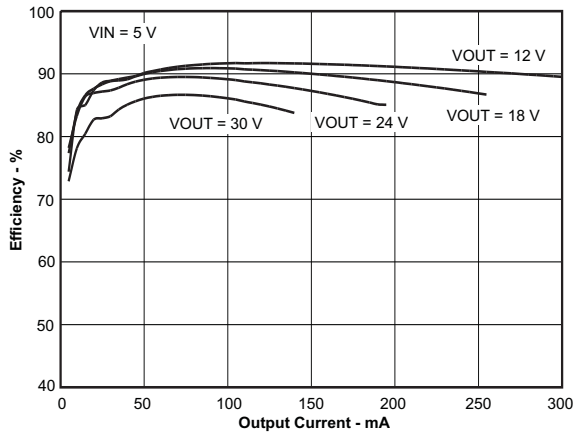


Figure 1. Efficiency vs Output Current

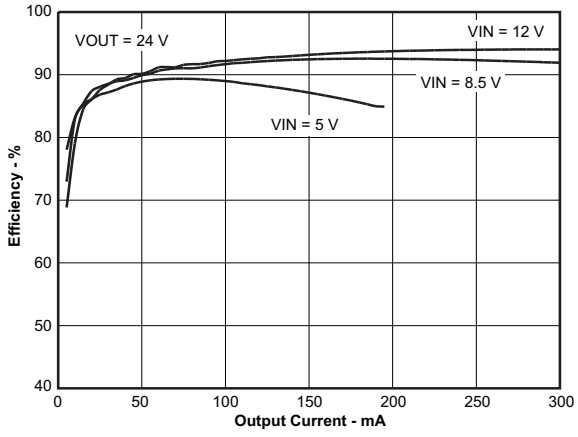


Figure 2. Efficiency vs Output Current

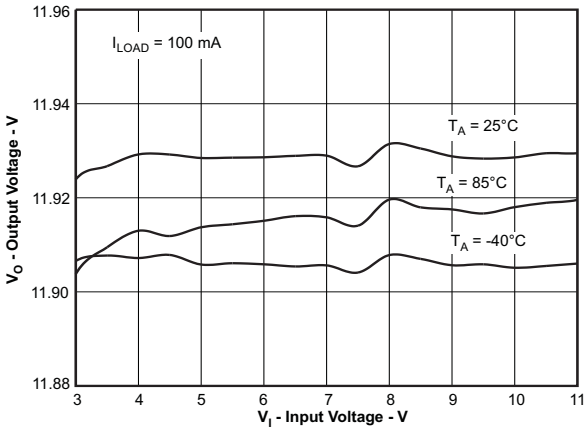


Figure 3. Output Voltage vs Input Voltage

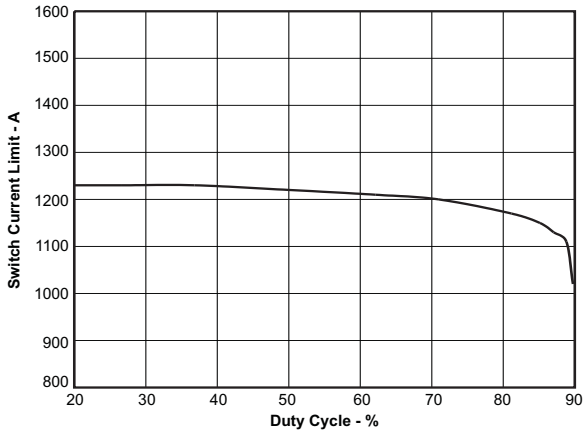


Figure 4. Switch Current Limit vs Duty Cycle

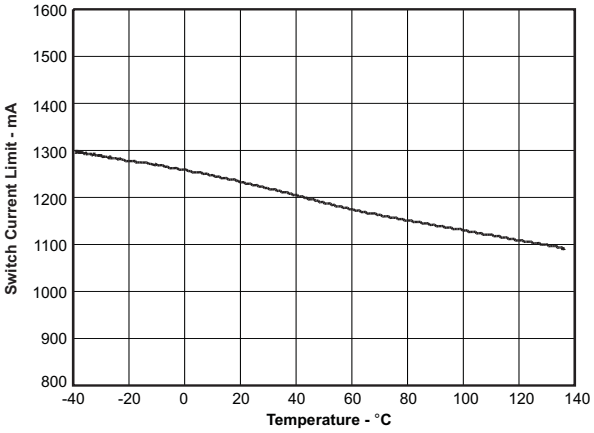


Figure 5. Switch Current Limit vs Temperature

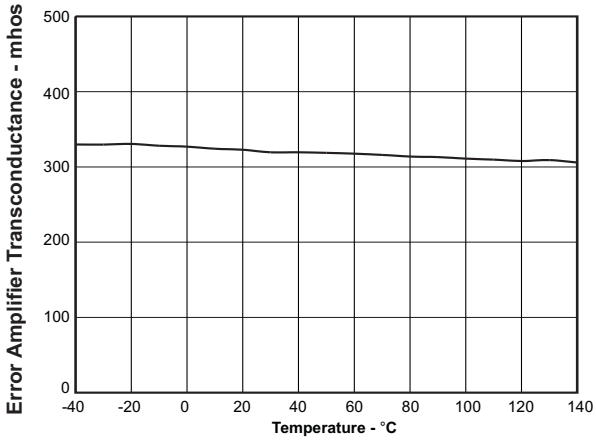


Figure 6. Error Amplifier Transconductance vs Temperature

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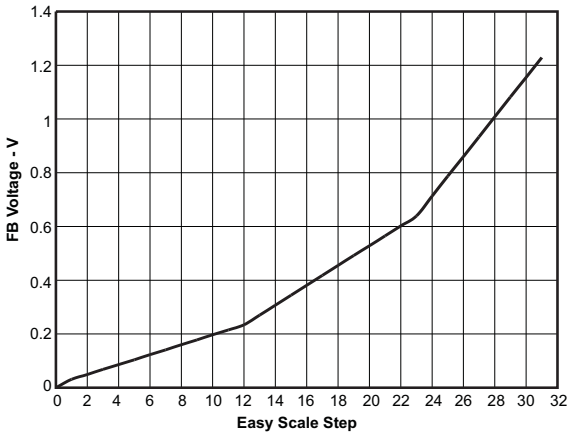


Figure 7. FB Voltage vs EasyScale Step

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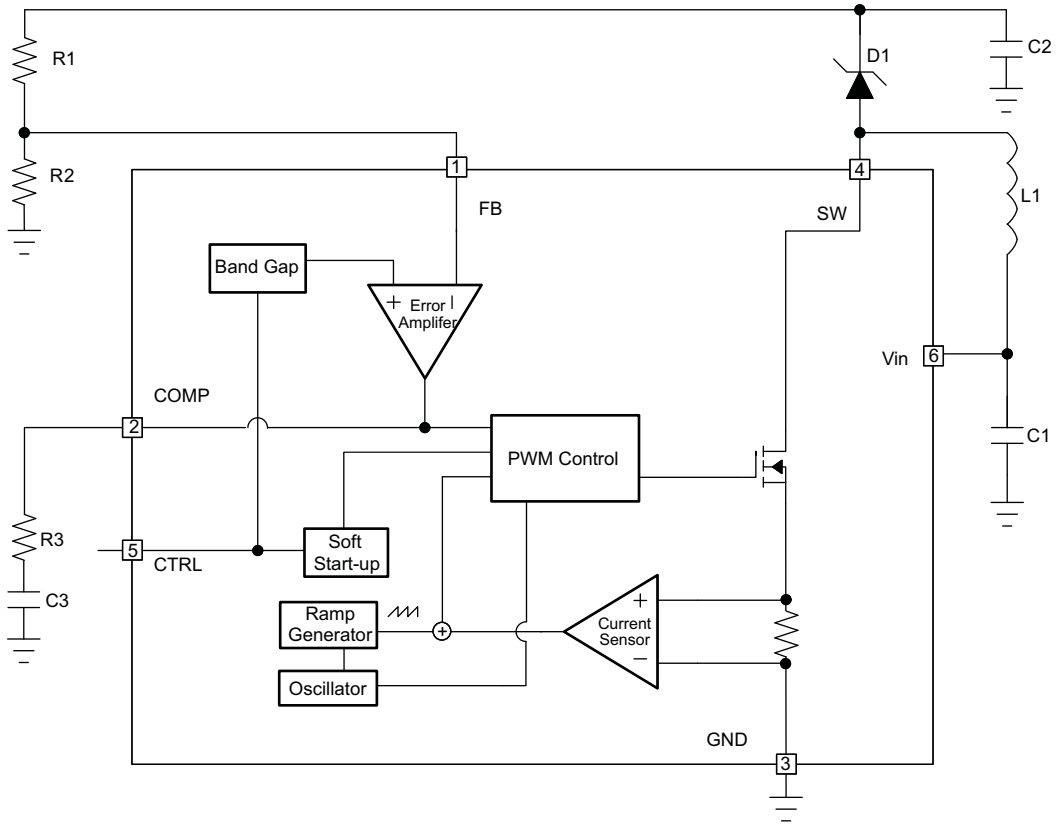
8 Detailed Description

8.1 Overview

The TPS61170 integrates a 40-V low side FET for providing output voltages up to 38 V. The device regulates the output with current mode PWM (pulse width modulation) control. The switching frequency of the PWM is fixed at 1.2 MHz (typical). The PWM control circuitry turns on the switch at the beginning of each switching cycle. The input voltage is applied across the inductor and stores the energy as the inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current rises to the threshold set by the error amplifier output, the power switch turns off and the external Schottky diode is forward biased. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats each switching cycle. As shown in the block diagram, the duty cycle of the converter is determined by the PWM control comparator which compares the error amplifier output and the current signal.

A ramp signal from the oscillator is added to the current ramp. This *slope* compensation ramp is necessary to avoid subharmonic oscillations that are intrinsic to current mode control at duty cycles higher than 50%. The feedback loop regulates the FB pin to a reference voltage through an error amplifier. The output of the error amplifier must be connected to the COMP pin. An external RC compensation network must be connected to the COMP pin to optimize the feedback loop for stability and transient response.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Soft Start-Up

Soft-start circuitry is integrated into the IC to avoid a high inrush current during start-up. After the device is enabled by a logic high signal on the CTRL pin, the FB pin reference voltage ramps up in 32 steps, with each step taking 213 µs. This ensures that the output voltage rises slowly to reduce inrush current. Additionally, for the first 5 msec after the COMP voltage ramps, the current limit of the PWM switch is set to half of the normal current limit specification or below 700 mA (typical). See the start-up waveform for a typical example, Figure 16.

8.3.2 Overcurrent Protection

TPS61170 has a cycle-by-cycle overcurrent limit feature that turns off the power switch once the inductor current reaches the overcurrent limit. The PWM circuitry resets itself at the beginning of the next switch cycle. During an over-current event, this results in a decrease of output voltage that is directly proportional to load current. The current limit threshold as well as input voltage, output voltage, switching frequency and inductor value determine the maximum available output current. Larger inductance values typically increase the current output capability because of the reduced current ripple. See *Maximum Output Current* for the output current calculation.

8.3.3 Undervoltage Lockout (UVLO)

An undervoltage lockout prevents mis-operation of the device at input voltages below 2.2 V (typical). When the input voltage is below the undervoltage threshold, the device remains off and the internal switch FET is turned off. The undervoltage lockout threshold is set below minimum operating voltage of 3V to avoid any transient VIN dip triggering the UVLO and causing the device to reset. For the input voltages between UVLO threshold and 3 V, the device attempts operation, but the specifications are not ensured.

8.3.4 Thermal Shutdown

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The IC restarts when the junction temperature drops by 15°C.

8.3.5 Enable and Shutdown

The TPS61170 enters shutdown when the CTRL voltage is less than 0.4 V for more than 2.5 ms. In shutdown, the input supply current for the device is less than 1 µA (maximum). The CTRL pin has an internal 800-kΩ (typical) pulldown resistor to disable the device when the pin is left unconnected.

8.4 Device Functional Modes

8.4.1 Feedback Reference Program Mode Selection

The CTRL pin is used for changing the FB pin reference voltage *on-the-fly*. There are two methods to program the reference voltage, PWM signal and 1-wire interface (EasyScale). The programming mode is selected each time the device is enabled. The default mode is to use the duty cycle of the PWM signal on the CTRL pin to modulate the reference voltage. To enter the 1-wire interface mode, the following digital pattern on the CTRL pin must be recognized by the IC every time the IC starts from the shutdown mode.

1. Pull CTRL pin high to enable the TPS61170 and to start the 1 wire mode detection window.
2. After the EasyScale detection delay (t_{es_delay}, 100 µsec) expires, drive CTRL low for more than the EasyScale detection time (t_{es_detect}, 260 µsec).
3. The CTRL pin has to be low for more than EasyScale detection time before the EasyScale detection window (t_{es_win}, 1msec) expires. EasyScale detection window starts from the first CTRL pin low to high transition.

The IC immediately enters the 1-wire mode once the previous three conditions are met. The EasyScale communication can start before the detection window expires. Once the mode is programmed, it can not be changed without another start up. In other words, the IC must be shutdown by pulling the CTRL low for 2.5 ms and restarted in order to exit EasyScale Mode. See Figure 8 for a graphical explanation.

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Device Functional Modes (continued)

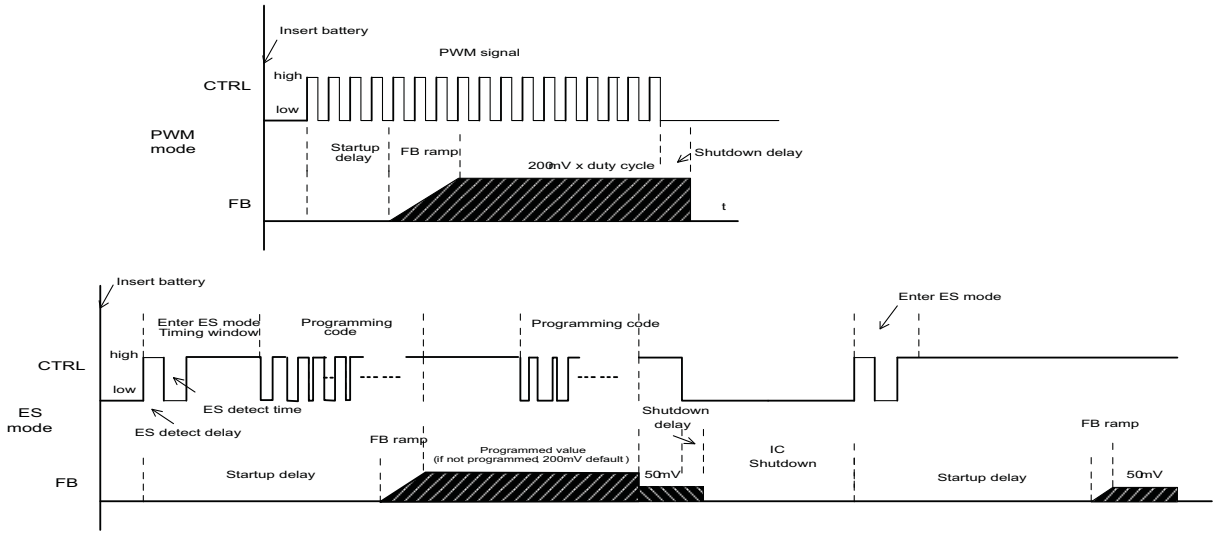


Figure 8. Mode Detection of Feedback Reference Program

8.4.2 PWM Program Mode

When the CTRL pin is constantly high, the FB voltage is regulated to 1.229V typically. However, the CTRL pin allows a PWM signal to lower this regulation voltage. The relationship between the duty cycle and FB voltage is given in Equation 1:

$$V_{FB} = \text{Duty} \times 1.229\ \text{V} \quad (1)$$

where

- Duty = duty cycle of the PWM signal
- 1.229 V = internal reference voltage

As shown in Figure 9, the IC chops up the internal 1.229 V reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. The regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM mode in the range of 5 kHz to 100 kHz. The requirement of minimum frequency comes from the EasyScale detection delay and detection time specification for the mode selection. The device can mistakenly enter 1 wire mode if the PWM signal frequency is less than 5 kHz. Because there is an internal fixed ON-time error of 40 nS, the FB voltage absolute value will be different than expected when the PWM frequency is above 100 kHz. For example, the additional duty cycle of 3.2% due to the ON-time error increases the FB voltage when using an 800 kHz PWM signal. A compromise between PWM frequency and FB voltage accuracy extends the frequency range. Adding an external RC filter to the pin serves no purpose.

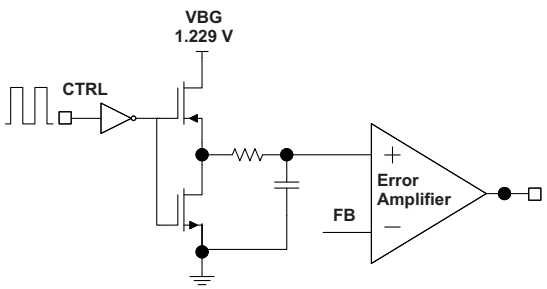


Figure 9. Block Diagram of Programmable FB Voltage Using PWM Signal

Device Functional Modes (continued)

8.4.3 1-Wire Program Mode

The CTRL pin features a simple digital interface to control the feedback reference voltage. The 1-wire mode can save the processor power and battery life as it does not require a PWM signal all the time, and the processor can enter idle mode if available.

The TPS61170 adopts the EasyScale protocol, which can program the FB voltage to any of the 32 steps with single command. See Table 2 for the FB pin voltage steps. The programmed reference voltage is stored in an internal register. The default value is full scale when the device is first enabled (V_{FB} = 1.229 V). A power reset clears the register value and reset it to default.

8.5 Programming

8.5.1 EasyScale

EasyScale is a simple but very flexible one pin interface to configure the FB voltage. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor. Figure 10 and Table 2 give an overview of the protocol. The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 72 hex. The data byte consists of five bits for information, two address bits, and the RFA bit. The RFA bit set to high indicates the *Request for Acknowledge* condition. The Acknowledge condition is only applied if the protocol was received correctly. The advantage of EasyScale compared with other on pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7 kBit/sec and up to 160 kBit/sec.

Table 2. Selectable FB Voltage

	FB VOLTAGE (mV)	D4	D3	D2	D1	D0
0	0.000	0	0	0	0	0
1	0.031	0	0	0	0	1
2	0.049	0	0	0	1	0
3	0.068	0	0	0	1	1
4	0.086	0	0	1	0	0
5	0.104	0	0	1	0	1
6	0.123	0	0	1	1	0
7	0.141	0	0	1	1	1
8	0.160	0	1	0	0	0
9	0.178	0	1	0	0	1
10	0.197	0	1	0	1	0
11	0.215	0	1	0	1	1
12	0.234	0	1	1	0	0
13	0.270	0	1	1	0	1
14	0.307	0	1	1	1	0
15	0.344	0	1	1	1	1
16	0.381	1	0	0	0	0
17	0.418	1	0	0	0	1
18	0.455	1	0	0	1	0
19	0.492	1	0	0	1	1
20	0.528	1	0	1	0	0
21	0.565	1	0	1	0	1
22	0.602	1	0	1	1	0
23	0.639	1	0	1	1	1
24	0.713	1	1	0	0	0
25	0.787	1	1	0	0	1

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Table 2. Selectable FB Voltage (continued)

	FB VOLTAGE (mV)	D4	D3	D2	D1	D0
26	0.860	1	1	0	1	0
27	0.934	1	1	0	1	1
28	1.008	1	1	1	0	0
29	1.082	1	1	1	0	1
30	1.155	1	1	1	1	0
31	1.229	1	1	1	1	1

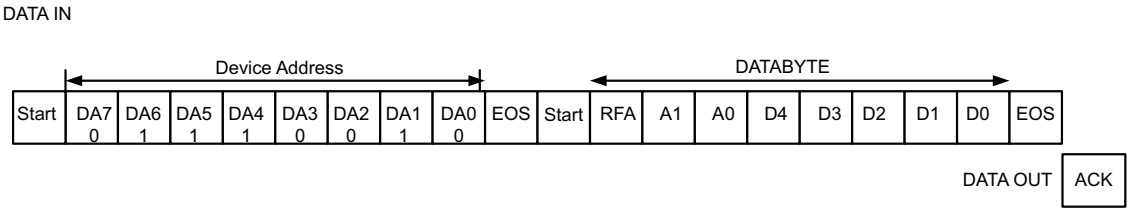


Figure 10. EasyScale Protocol Overview

Table 3. EasyScale Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte 72 hex	7	DA7	IN	0 MSB device address
	6	DA6		1
	5	DA5		1
	4	DA4		1
	3	DA3		0
	2	DA2		0
	1	DA1		1
	0	DA0		0 LSB device address
Data byte	7 (MSB)	RFA	IN	Request for acknowledge. If high, acknowledge is applied by device
	6	A1		0 Address bit 1
	5	A0		0 Address bit 0
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0
		ACK	OUT	Acknowledge condition active 0, this condition will only be applied in case RFA bit is set. Open-drain output, Line must be pulled high by the host with a pullup resistor. This feature can only be used if the master has an open-drain output stage. In case of a push pull output stage Acknowledge condition may not be requested!

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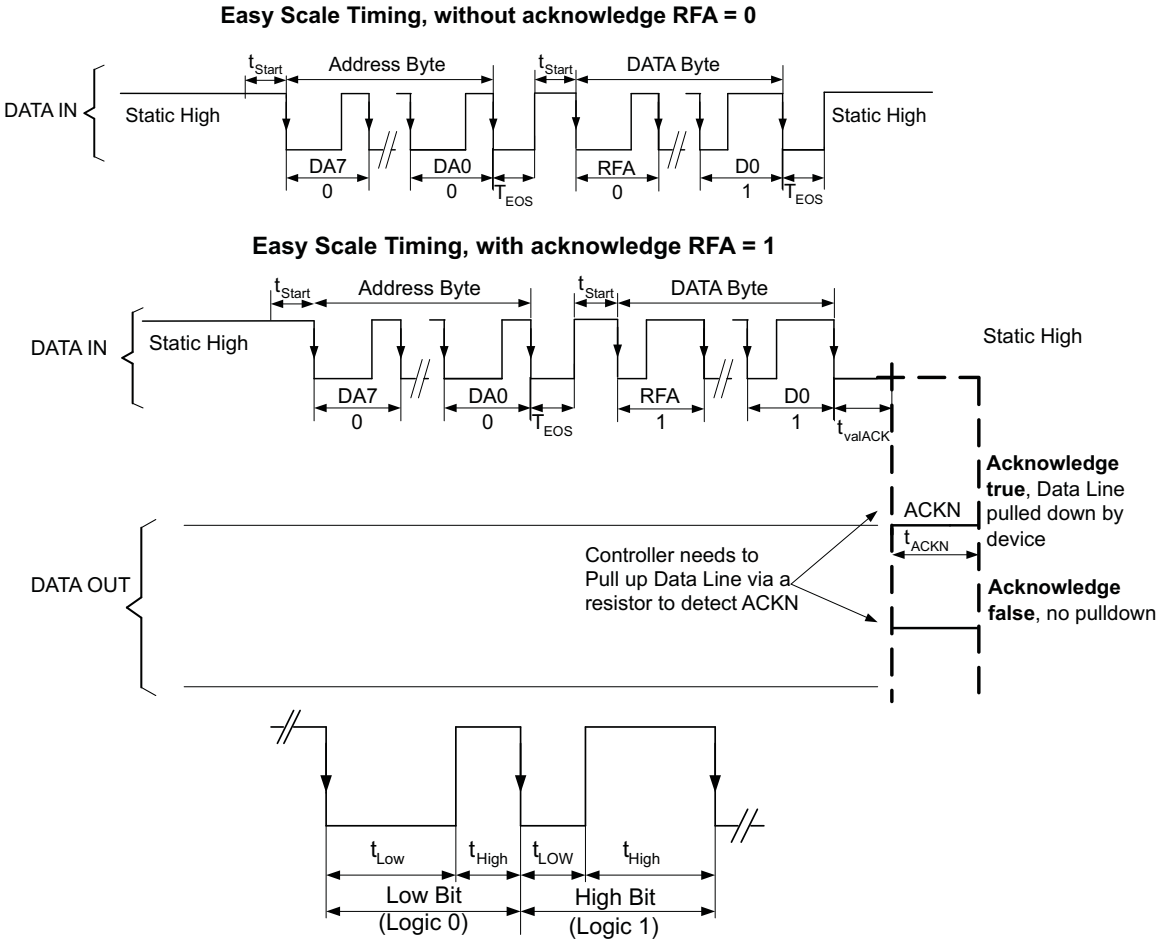


Figure 11. EasyScale— Bit Coding

All bits are transmitted MSB first and LSB last. Figure 11 shows the protocol without acknowledge request (Bit RFA = 0), Figure 11 with acknowledge (Bit RFA = 1) request. Prior to both bytes, device address byte and data byte, a start condition must be applied. For this, the CTRL pin must be pulled high for at least t_{start} (2 µs) before the bit transmission starts with the falling edge. If the CTRL pin is already at high level, no start condition is needed prior to the device address byte. The transmission of each byte is closed with an End of Stream condition for at least t_{EOS} (2 µs).

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between t_{LOW} and t_{HIGH}. It can be simplified to:

High Bit: $t_{HIGH} > t_{LOW}$, but with t_{HIGH} at least 2x t_{LOW}, see Figure 11.

Low Bit: $t_{HIGH} < t_{LOW}$, but with t_{LOW} at least 2x t_{HIGH}, see Figure 11.

The bit detection starts with a falling edge on the CTRL pin and ends with the next falling edge. Depending on the relation between t_{HIGH} and t_{LOW}, the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by a set RFA bit.
- The transmitted device address matches with the device address of the device.
- 16 bits is received correctly.

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If the device turns on the internal ACKN-MOSFET and pulls the CTRL pin low for the time t_{ACKN}, which is 512 µs maximum then the Acknowledge condition is valid after an internal delay time t_{valACK}. This means that the internal ACKN-MOSFET is turned on after t_{valACK}, when the last falling edge of the protocol was detected. The master controller keeps the line low in this period. The master device can detect the acknowledge condition with its input by releasing the CTRL pin after t_{valACK} and read back a logic 0. The CTRL pin can be used again after the acknowledge condition ends.

Note that the acknowledge condition may only be requested if the master device has an open-drain output. For the push-pull output stage, the use a series resistor in the CRTL line to limit the current to 500 µA is recommended for such cases as:

- an accidentally requested acknowledge, or
- to protect the internal ACKN-MOSFET.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6170 is designed for output voltages up to 38 V with a switch peak current limit of 0.96-A minimum. The device, which operates in peak current mode PWM control, is externally compensated for maximum flexibility and stability. The switching frequency is fixed at 1.2 MHz, and the input voltage range is 3.0 to 18 V. The following section provides a step-by-step design approach for configuring the TPS61170 as a voltage regulating boost converter.

9.2 Typical Application

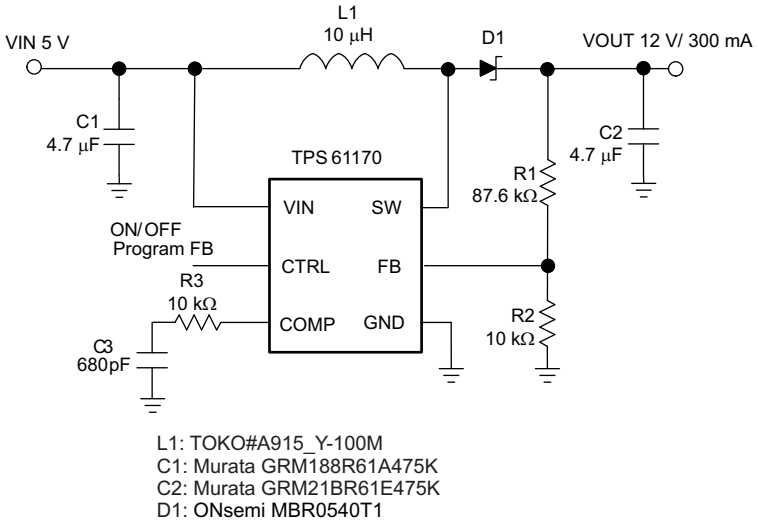


Figure 12. 5-V to 12-V DCDC Power Conversion With Programmable Feedback Reference Voltage

9.2.1 Design Requirements

Table 4. TPS61170 12-V Output Design Requirements

PARAMETERS	VALUES
Input Voltage	5.0V ± 20%
Output Voltage	12V
Output Current	300mA

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9.2.2 Detailed Design Procedure

9.2.2.1 Program Output Voltage

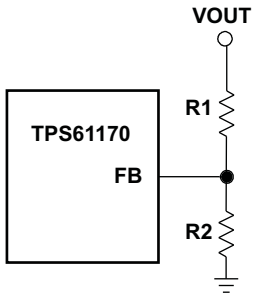


Figure 13. Program Output Voltage

To program the output voltage, select the values of R1 and R2 (see Figure 13) according to Equation 2.

$$Vout = 1.229\ V \times \left(\frac{R1}{R2} + 1\right) \qquad R1 = R2 \times \left(\frac{Vout}{1.229\ V} - 1\right) \tag{2}$$

Considering the leakage current through the resistor divider and noise decoupling to FB pin, an optimum value for R2 is around 10k. The output voltage tolerance depends on the accuracy of the reference voltage and the tolerance of R1 and R2.

9.2.2.2 Maximum Output Current

The overcurrent limit in a boost converter limits the maximum input current, and thus the maximum input power for a given input voltage. The maximum output power is less than the maximum input power due to power conversion losses. Therefore, the current-limit setting, input voltage, output voltage and efficiency can all affect the maximum output current. The current limit clamps the peak inductor current; therefore, the ripple must be subtracted to derive the maximum DC current. The ripple current is a function of the switching frequency, inductor value and duty cycle. The following equations take into account of all the above factors for maximum output current calculation.

$$I_P = \frac{1}{\left[L \times F_s \times \left(\frac{1}{V_{out} + V_f - V_{in}} + \frac{1}{V_{in}}\right)\right]} \tag{3}$$

where:

- I_P = inductor peak to peak ripple current
- L = inductor value
- V_f = Schottky diode forward voltage
- F_s = switching frequency
- V_{out} = output voltage

$$I_{out_max} = \frac{V_{in} \times (I_{lim} - I_P/2) \times \eta}{V_{out}} \tag{4}$$

where:

- I_{out_max} = Maximum output current of the boost converter
- I_{lim} = overcurrent limit
- η = efficiency

For instance, when V_{in} is 5 V, V_{out} is 12 V, the inductor is 10 µH, the Schottky forward voltage is 0.2 V; and then the maximum output current is 300 mA in a typical operation.

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9.2.2.3 Switch Duty Cycle

The maximum switch duty cycle (D) of the TPS61170 is 90% (min). The duty cycle of a boost converter under continuous conduction mode (CCM) is given by:

$$D = \frac{Vout - Vin}{Vout} \quad (5)$$

For a 5 V to 12 V application, the duty cycle is 58.3%, and for a 5 V to 24 V application, the duty cycle is 79.2%. The duty cycle must be lower than the maximum specification of 90% in the application; otherwise, the output voltage cannot be regulated.

Once the PWM switch is turned on, the TPS61170 has minimum ON pulse width. This sets the limit of the minimum duty cycle. When operating at low duty cycles, the TPS61170 enters pulse-skipping mode. In this mode, the device turns the power switch off for several switching cycles to prevent the output voltage from rising above regulation. This operation typically occurs in light load condition when the PWM operates in discontinuous mode. See the Figure 17.

9.2.2.4 Inductor Selection

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications: inductor value, DC resistance (DCR) and saturation current. Considering inductor value alone is not enough.

The inductance value of the inductor determines its ripple current. It is recommended that the peak-to-peak ripple current given by Equation 3 be set to 30–40% of the DC current. Inductance values shown in *Recommended Operating Conditions* are recommended for most applications. Inductor DC current can be calculated as

$$I_{in_DC} = \frac{Vout \times Iout}{Vin \times \eta} \quad (6)$$

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous PWM where the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. In general, inductors with large inductance and low DCR values provide much more output current and higher conversion efficiency. Inductors with smaller inductance values can give better load transient response. For these reasons, a 10 µH to 22 µH inductance value range is recommended. Table 5 lists some recommended inductors for the TPS61170.

TPS61170 has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is lower than 10 µH, the slope compensation may not be adequate, and the loop can become unstable. Therefore, customers need to verify operation in their application if the inductor is different from the recommended values.

Table 5. Recommended Inductors for TPS61170

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (L × W × H mm)	VENDOR
A915_Y-100M	10	90	1.3	5.2 × 5.2 × 3.0	TOKO
VLCF5020T-100M1R1-1	10	237	1.1	5 × 5×2.0	TDK
CDRH4D22/HP	10	144	1.2	5 × 5 × 2.4	Sumida
LQH43PN100MR0	10	247	0.84	4.5 × 3.2 × 2.0	Murata

9.2.2.5 Schottky Diode Selection

The high switching frequency of the TPS61170 demands a high-speed rectifying switch for optimum efficiency. Ensure that the average and peak current rating of the diode exceeds the average output current and peak inductor current. In addition, the reverse breakdown voltage of the diode must exceed the switch FET rating voltage of 40 V. So, the ONSemi MBR0540 is recommended for TPS61170. However, Schottky diodes with lower rated voltages can be used for lower output voltages to save the solution size and cost. For example, a converter providing a 12-V output with 20-V diode is a good choice.

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9.2.2.6 Compensation Capacitor Selection

The TPS61170 has an external compensation, COMP pin, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external resistor R3 and ceramic capacitor C3 are connected to COMP pin to provide a pole and a zero. This pole and zero, along with the inherent pole of a current mode control boost converter, determine the close loop frequency response. This is important to a converter stability and transient response.

The following equations summarize the poles, zeros and DC gain of a TPS61170 boost converter with ceramic output capacitor (C2), as shown in the block diagram. They include the dominant pole (f_{P1}), the output pole (f_{P2}) of a boost converter, the right-half-plane zero (f_{RHPZ}) of a boost converter, the zero (f_Z) generated by R3 and C3, and the DC gain (A).

$$f_{P1} = \frac{1}{2\pi \times 6\ M\Omega \times C3} \quad (7)$$

$$f_{P2} = \frac{2}{2\pi \times Rout \times C2} \quad (8)$$

$$f_{RHPZ} = \frac{Rout}{2\pi \times L} \times \left(\frac{Vin}{Vout}\right)^2 \quad (9)$$

$$f_Z = \frac{1}{2\pi \times R3 \times C3} \quad (10)$$

$$A = \frac{1.229}{Vout} \times Gea \times 6\ M\Omega \times \frac{Vin}{Vout \times Rsense} \times Rout \times \frac{1}{2} \quad (11)$$

where Rout is the load resistance, Gea is the error amplifier transconductance located in *Electrical Characteristics*, Rsense (100mΩ typical) is a sense resistor in the current control loop. These equations helps generate a simple bode plot for TPS61170 loop analysis.

Increasing R3 or reducing C3 increases the close loop bandwidth which improves the transient response. Adjusting R3 and C3 in opposite directions increase the phase, and help loop stability. For many of the applications, the recommended value of 10k and 680pF makes an ideal compromise between transient response and loop stability. To optimize the compensation, use C3 in the range of 100pF to 10nF, and R3 of 10k. See the TI application report SLVA319 for thorough analysis and description of the boost converter small signal model and compensation design.

9.2.2.7 Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability. The ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated using Equation 12.

$$C_{out} = \frac{\left(V_{out} - V_{in}\right) I_{out}}{V_{out} \times Fs \times V_{ripple}} \quad (12)$$

Where, V_{ripple} = peak-to-peak output ripple. The additional output ripple component caused by ESR is calculated using:

$$V_{ripple_ESR} = I_{out} \times R_{ESR} \quad (13)$$

Due to its low ESR, Vripple_ESR can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging and AC signal. For example, larger form factor capacitors (in 1206 size) have a resonant frequencies in the range of the switching frequency. So, the effective capacitance is significantly lower. The DC bias can also significantly reduce capacitance. Ceramic capacitors can lose as much as 50% of its capacitance at its rated voltage. Therefore, choose a ceramic capacitor with a voltage rating at least 1.5X its expected dc bias voltage.

The capacitor in the range of 1 µF to 4.7 µF is recommended for input side. The output typically requires a capacitor in the range of 1 µF to 10 µF. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

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The popular vendors for high value ceramic capacitors are:

TDK (http://www.component.tdk.com/components.php)

Murata (http://www.murata.com/cap/index.html)

9.2.3 Application Curves

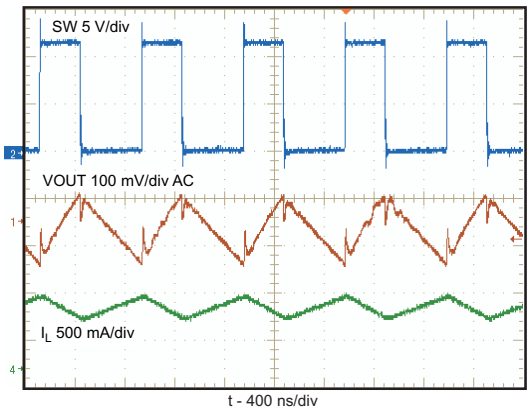


Figure 14. PWM Switching Operation

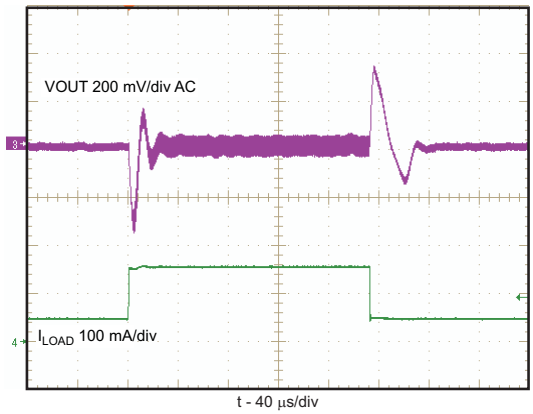


Figure 15. Load Transient Response

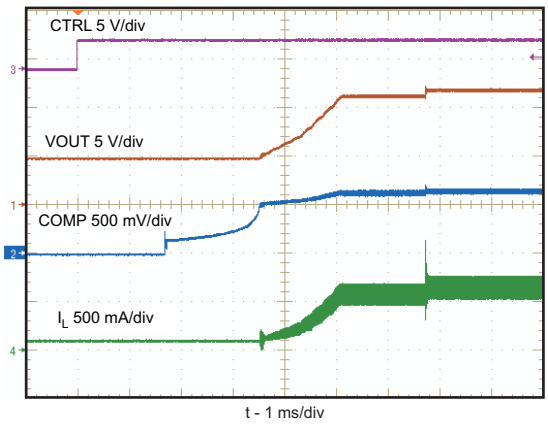


Figure 16. Start-Up

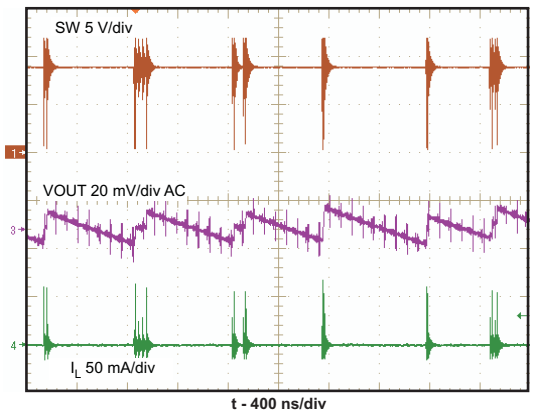
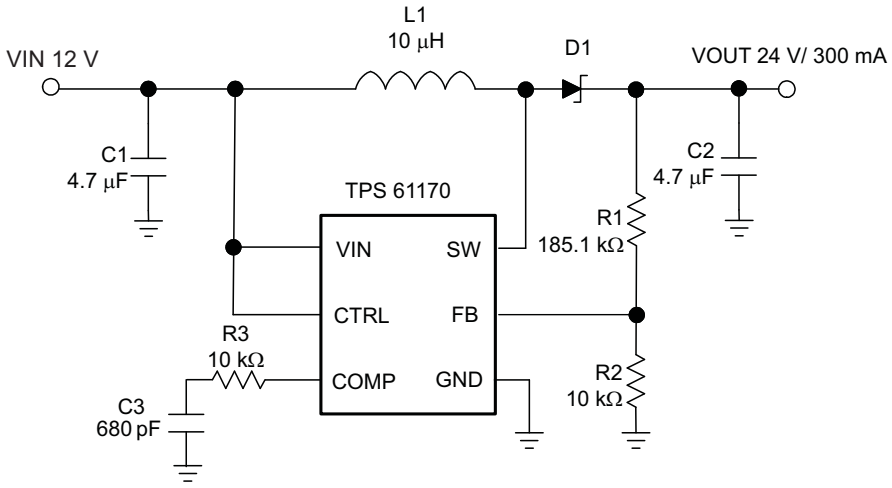


Figure 17. Skip-Cycle Switching

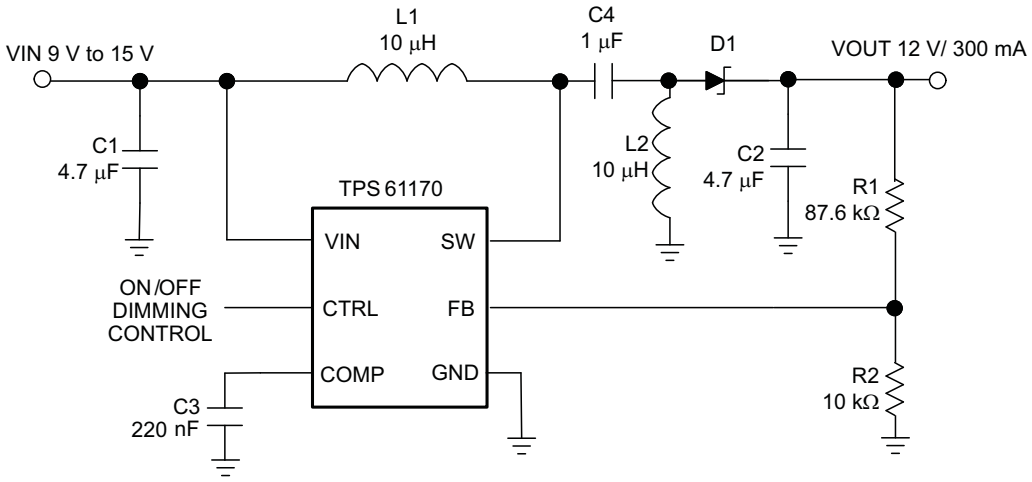
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9.3 System Examples



L1: TOKO#A915_Y-100M
C1: Murata GRM21BR61E475K
C2: Murata GRM32ER71H475K
D1: ONsemi MBR0540T1

Figure 18. 12-V to 24-V DCDC Power Conversion



L1: TOKO#A915_Y-100M
C1: Murata GRM21BR61E475K
C2: Murata GRM21BR61E475K
D1: ONsemi MBR0540T1
*L1, L2 can be replaced by 1:1 transformer

Figure 19. 12-V SEPIC (Buck-Boost) Converter

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System Examples (continued)

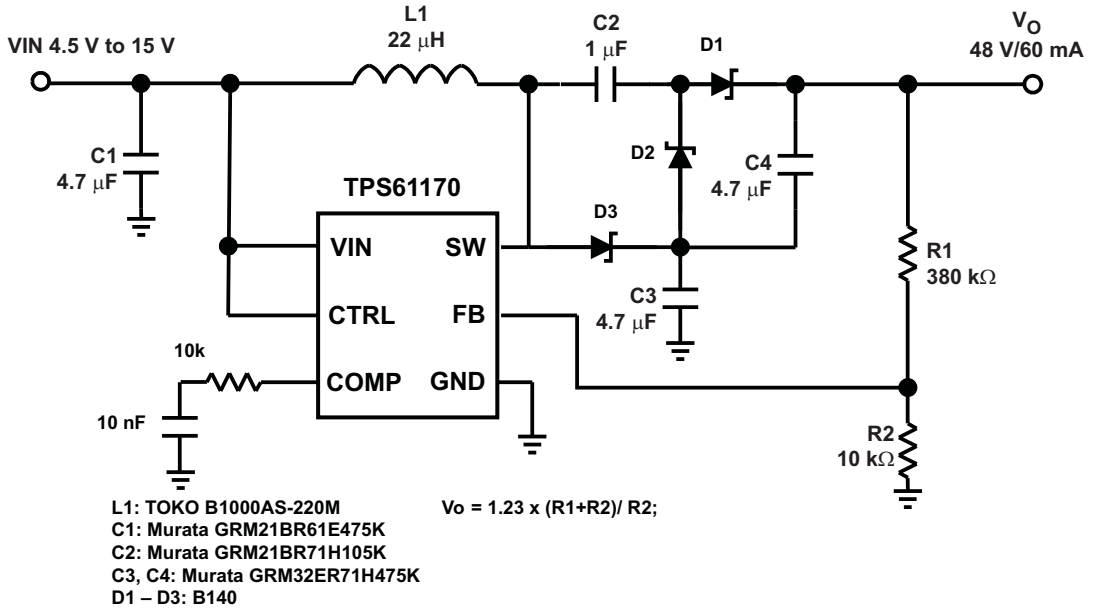


Figure 20. 48-V Phantom Power Application Circuit

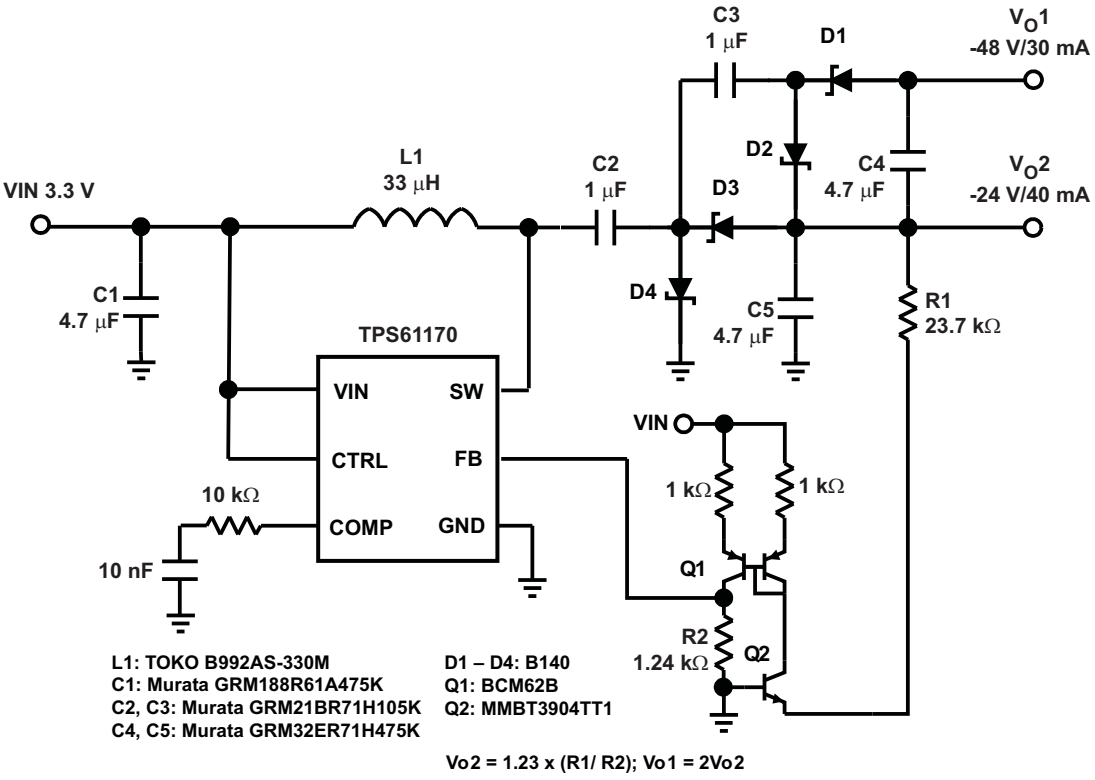


Figure 21. –24-V / –48-V Buck-Boost Converter From 3.3-V Input

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System Examples (continued)

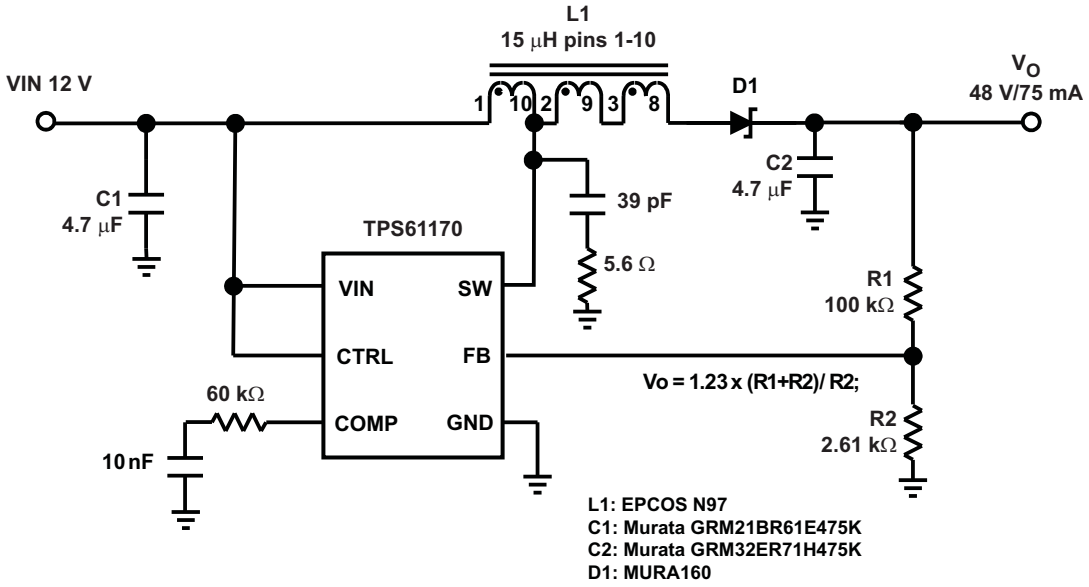


Figure 22. 12-V to 48-V Flyback Topology

10 Power Supply Recommendations

The TPS61170 is designed to operate from an input voltage supply range from 3.0 V to 18 V. The power supply to the TPS61170 needs to have a current rating according to the supply voltage, output voltage, and output current of the TPS61170 device.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, especially those switching at high frequencies and/or providing high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To maximize efficiency, switch rise and fall times should be as short as possible. To reduce radiation of high frequency switching noise and harmonics, proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling. The high current path including the switch, Schottky diode, and output capacitor, contains nanosecond rise and fall times and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce the IC supply ripple. Figure 23 shows a sample layout

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11.2 Layout Example

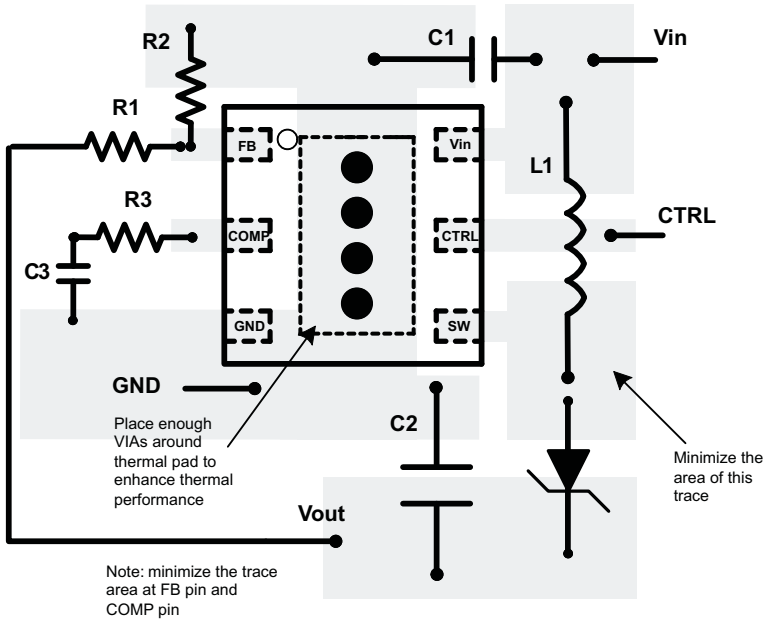


Figure 23. PCB Layout Recommendation

11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation of the TPS61170. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 14:

$$P_{D(max)} = \frac{125^{\circ}C - T_A}{R_{\theta JA}} \quad (14)$$

where, T_A is the maximum ambient temperature for the application. $R_{\theta JA}$ is the thermal resistance junction-to-ambient given in the *Thermal Information* table.

The TPS61170 comes in a thermally enhanced QFN package. This package includes a thermal pad that improves the thermal capabilities of the package. The $R_{\theta JA}$ of the QFN package greatly depends on the PCB layout and thermal pad connection. The thermal pad must be soldered to the analog ground on the PCB. Using thermal vias underneath the thermal pad as illustrated in the layout example. Also see the *QFN/SON PCB Attachment* application report (SLUA271).

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- QFN/SON PCB Attachment Application Report, SLUA271
- Ultralow Power 100-mA Low-Dropout Linear Regulator, SLVS319

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61170DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BZS
TPS61170DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BZS
TPS61170DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZS
TPS61170DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BZS
TPS61170DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BZS
TPS61170DRVTG4	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS61170 :

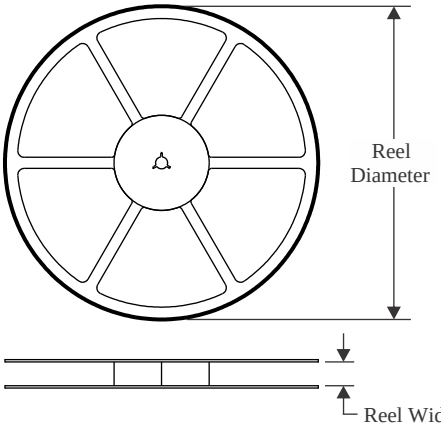
- Automotive : TPS61170-Q1

NOTE: Qualified Version Definitions:

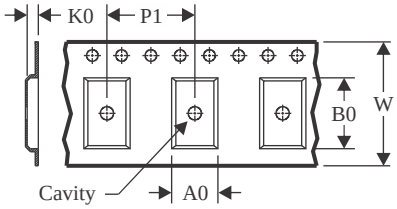
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

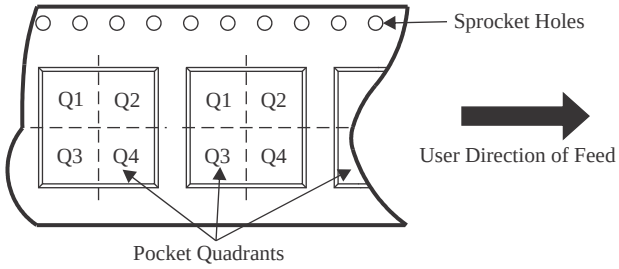


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

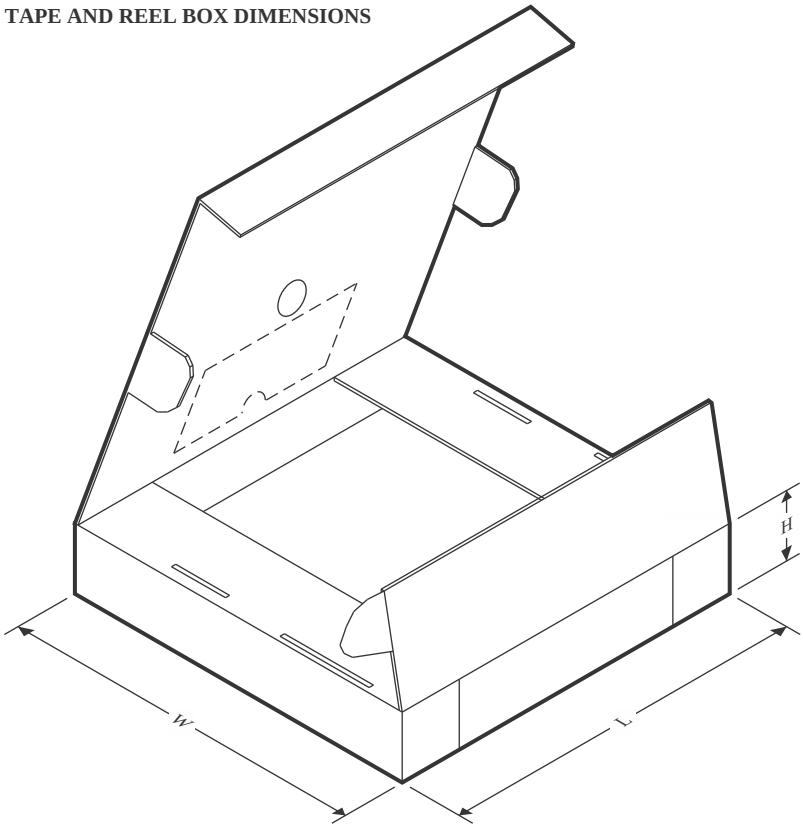
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61170DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61170DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61170DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61170DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61170DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

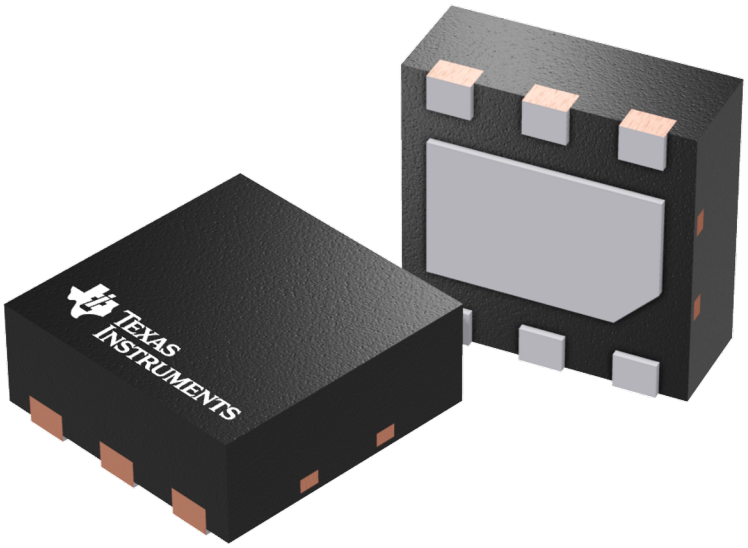


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61170DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS61170DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS61170DRVR	WSON	DRV	6	3000	213.0	191.0	35.0
TPS61170DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS61170DRVT	WSON	DRV	6	250	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



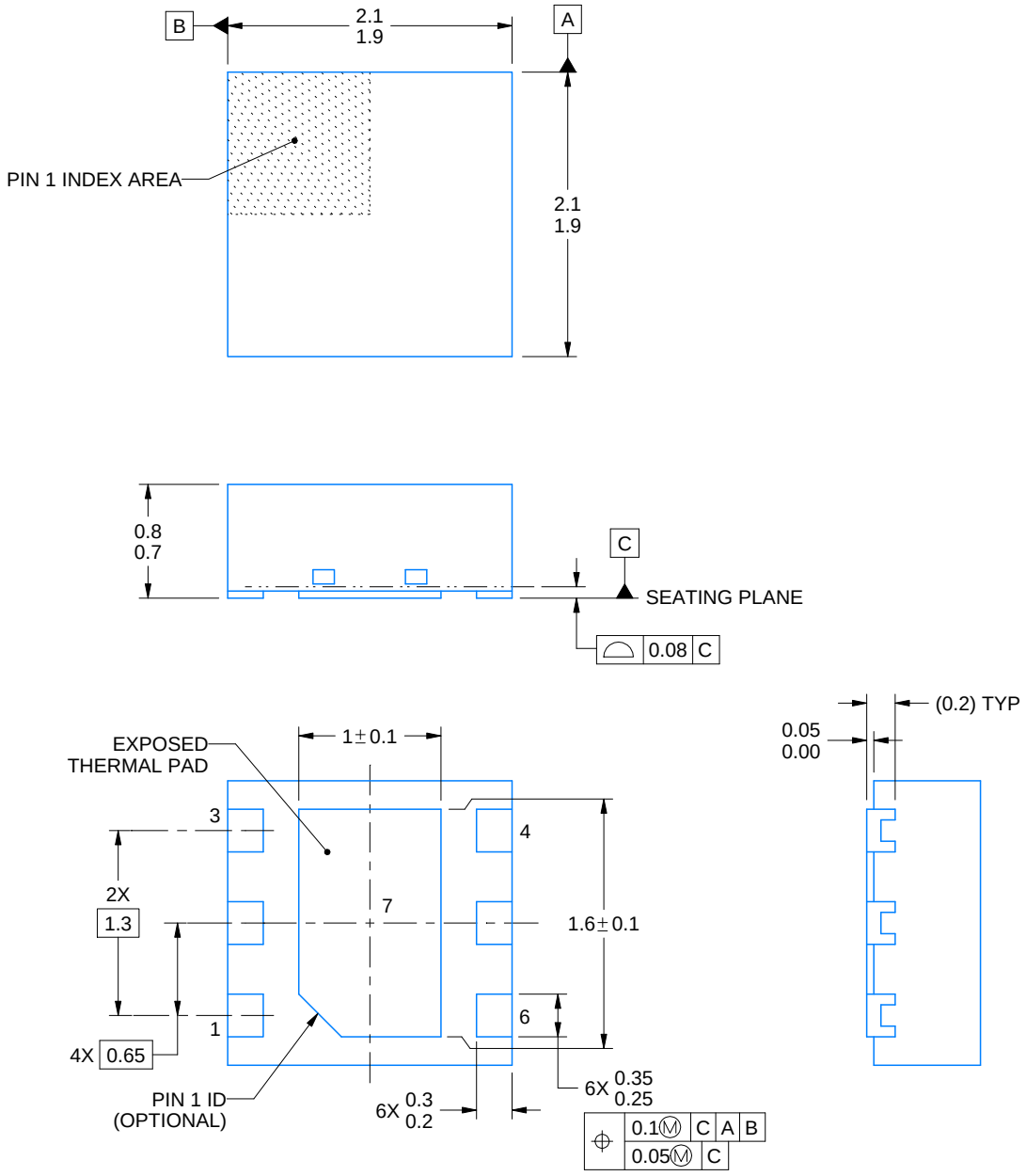
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

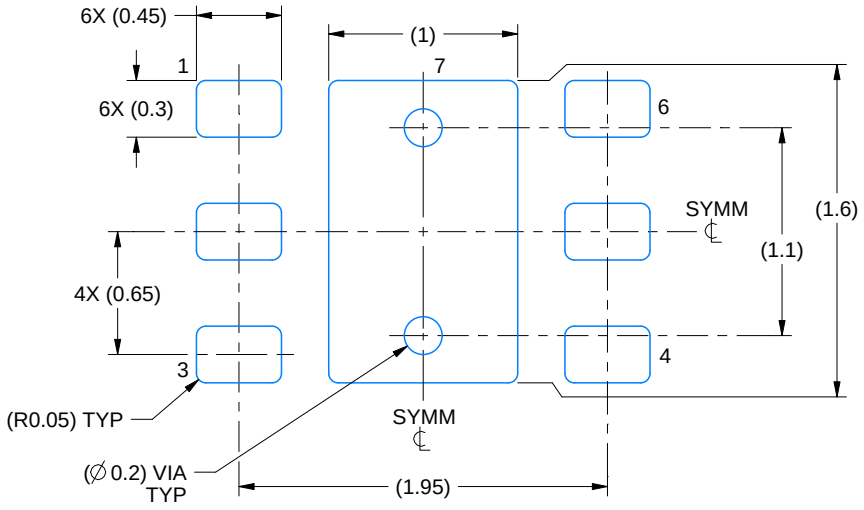
PLASTIC SMALL OUTLINE - NO LEAD



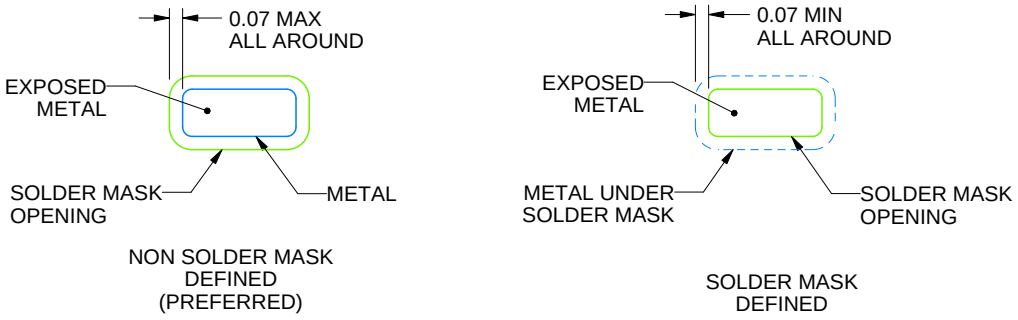
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

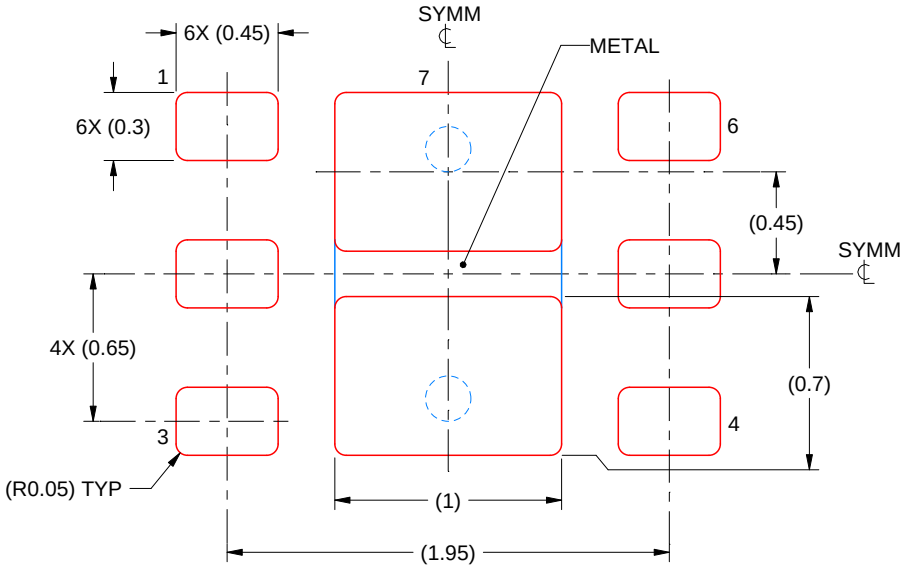


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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