500-mA, 6-MHz SYNCHRONOUS STEP-DOWN CONVERTER IN CHIP SCALE PACKAGING

FEATURES

- 89% Efficiency at 6MHz Operation
- Output Current Up to 500mA
- Wide V_{IN} Range From 2.3V to 5.5V
- 6MHz Regulated Frequency Operation
- *Best in Class* Load and Line Transient
- ±1.5% Total DC Voltage Accuracy
- Automatic PFM/PWM Mode Switching
- 30μA Quiescent Current
- 35ns Minimum On-Time
- Internal Soft Start, <200-μs Start-Up Time
- Current Overload and Thermal Shutdown Protection
- Three Surface-Mount External Components Required (One MLCC Inductor, Two Ceramic Capacitors)
- Complete Sub 1-mm Component Profile Solution
- Total Solution Size <13 mm^2
- Available in a 6-Pin NanoFree™ (CSP) Packaging

APPLICATIONS

- Cell Phones, Smart-Phones
- PDAs, Pocket PCs
- WLAN and Bluetooth™ Applications
- DVB-H Tuner Applications
- Portable Hard Disk Drives
- DC/DC Micro Modules

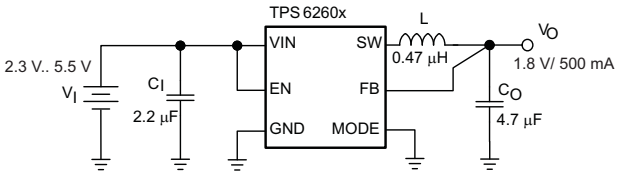

Figure 1. Smallest Solution Size Application (Fixed Output Voltage)

DESCRIPTION

The TPS6260x device is a high-frequency synchronous step-down dc-dc converter optimized for battery-powered portable applications. Intended for low-power applications, the TPS6260x supports up to 500mA load current, and allows the use of low cost chip inductor and capacitors.

With a wide input voltage range of 2.3V to 5.5V, the device supports applications powered by Li-Ion batteries with extended voltage range. Different fixed voltage output versions are available from 1V to 2.5V.

The TPS6260x operates at a regulated 6-MHz switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

The PFM mode extends the battery life by reducing the quiescent current to 30μA (typ) during light load and standby operation. For noise-sensitive applications, the device can be forced into fixed frequency PWM mode by pulling the MODE pin high. In the shutdown mode, the current consumption is reduced to less than 1μA.

The TPS6260x is available in an 6-pin chip-scale package (CSP).

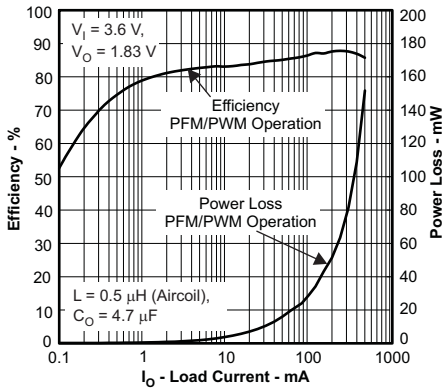

Figure 2. Efficiency vs Load Current

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PART NUMBER	OUTPUT VOLTAGE	PACKAGE	ORDERING(2)(3)	PACKAGE MARKING CHIP CODE
-40°C to 85°C	TPS62600	1.83V	YFF-6	TPS62600YFF	G9
	TPS62601	1.8V		TPS62601YFF	GA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The YFF package is available in tape and reel. Add a R suffix (TPS62600YFFR) to order quantities of 3000 parts. Add a T suffix (TPS62600YFFT) to order quantities of 250 parts.
(3) Internal tap points are available to facilitate output voltages in 25mV increments.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_I	Voltage at VIN, SW(2)	-0.3 V to 7 V
	Voltage at FB(2)	-0.3 V to 3.6 V
	Voltage at EN, MODE (2)	-0.3 V to V_I + 0.3 V
	Power dissipation	Internally limited
T_A	Operating temperature range(3)	-40°C to 85°C
T_J (max)	Maximum operating junction temperature	150°C
T_{stg}	Storage temperature range	-65°C to 150°C
ESD rating (4)	Human body model	2 kV
	Charge device model	1 kV
	Machine model	200 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$.
(4) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$(2)	$R_{\theta JB}$(2)	POWER RATING $T_A \le 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$
YFF-6	125°C/W	53°C/W	800mW	8mW/°C

(1) Maximum power dissipation is a function of T_J(max), θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_J(max)-T_A] / \theta_{JA}$.
(2) This thermal data is measured with high-K board (4 layers board according to JESD51-7 JEDEC standard).

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ELECTRICAL CHARACTERISTICS

V_I = 3.6V, V_O = 1.83V, EN = 1.8 V, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_I	Input voltage range			2.3		5.5	V
I_Q	Operating quiescent current		I_O = 0mA. PFM mode enabled, device not switching		30	45	µA
			I_O = 0mA, L = 0.47µH (Aircoil) Forced PWM operation		6.5		mA
$I_{(SD)}$	Shutdown current		EN = GND		0.2	1	µA
UVLO	Undervoltage lockout threshold				2.05	2.1	V
ENABLE, MODE							
V_{IH}	High-level input voltage			1			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input connected to GND or VIN		0.01	1	µA
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on resistance		$V_I = V_{(GS)}$ = 3.6V		310		mΩ
			$V_I = V_{(GS)}$ = 2.5V		380		mΩ
I_{lkg}	P-channel leakage current, PMOS		$V_{(DS)}$ = 5.5V, -40°C ≤ T_J ≤ 85°C			1	µA
$r_{DS(on)}$	N-channel MOSFET on resistance		$V_I = V_{(GS)}$ = 3.6V		250		mΩ
			$V_I = V_{(GS)}$ = 2.5V		320		mΩ
I_{lkg}	N-channel leakage current, NMOS		$V_{(DS)}$ = 5.5V, -40°C ≤ T_J ≤ 85°C			2	µA
	P-MOS current limit		2.3V ≤ V_I ≤ 5.5V. Open loop	900	1000	1100	mA
	Input current limit under short-circuit conditions		V_O = 0 , L = 0.47µH		30		mA
	Thermal shutdown				140		°C
	Thermal shutdown hysteresis				10		°C
OSCILLATOR							
f_{SW}	Oscillator frequency	TPS62600 TPS62601	I_O = 0mA, L = 0.47µH. Forced PWM operation	5.4	6	6.6	MHz
OUTPUT							
$V_{(OUT)}$	Regulated DC output voltage	TPS62600 TPS62601	2.5V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 500mA PFM/PWM operation	0.985×V_{NOM}	V_{NOM}	1.025×V_{NOM}	V
			2.5V ≤ V_I ≤ 5.5V, 0 mA ≤ I_O ≤ 500mA PWM operation	0.985×V_{NOM}	V_{NOM}	1.015×V_{NOM}	V
	Line regulation		V_I = V_O + 0.5V (min 2.3V) to 5.5V, I_O = 200mA		0.25		%/V
	Load regulation		I_O = 0mA to 500mA		-0.0003		%/mA
	Feedback input resistance				460		kΩ
$t_{on(MIN)}$	Minimum on-time (P-channel MOSFET)				35		ns
ΔV_O	Power-save mode ripple voltage	TPS62600 TPS62601	I_O = 1mA		0.015×V_{NOM}		V_{PP}
	Start-up time		I_O = 0mA, Time from active EN to V_O		180		µs

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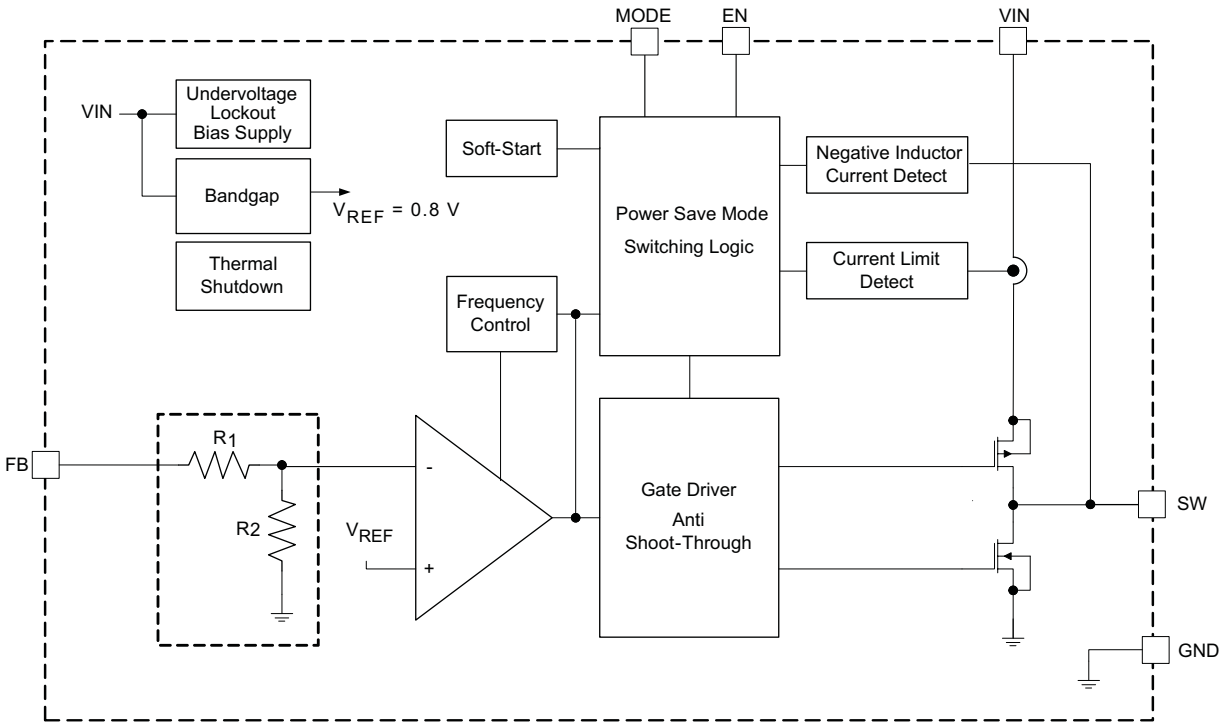
PIN ASSIGNMENTS



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
FB	C1	I	Output feedback sense input. Connect FB to the converter's output.
VIN	A2	I	Power supply input.
SW	B1	I/O	This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs.
EN	B2	I	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin to V_I enables the device. This pin must not be left floating and must be terminated.
MODE	A1	I	This is the mode selection pin of the device. This pin must not be left floating and must be terminated.
			MODE = LOW: The device is operating in fixed frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents.
			MODE = HIGH: Low-noise mode enabled, fixed frequency PWM operation forced.
GND	C2	–	Ground pin.

FUNCTIONAL BLOCK DIAGRAM



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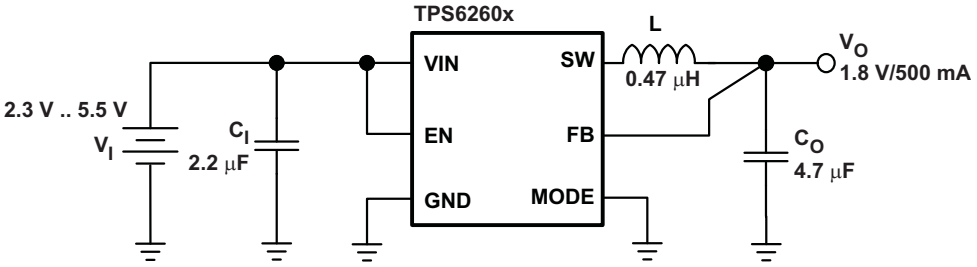
PARAMETER MEASUREMENT INFORMATION



List of components:

- L = MURATA LQM21PN1R0NGR
- C_I = MURATA GRM155R60J225ME15 (2.2µF, 6.3V, 0402, X5R)
- C_O = MURATA GRM155R60G475ME47 (4.7µF, 4V, 0402, X5R)

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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Load current	3, 4, 5
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	Load transient response		9, 10, 11, 12 13, 14, 15, 16
V_O	DC output voltage	vs Load current	17
I_Q	No load quiescent current	vs Input voltage	18
f_s	Switching frequency	vs Temperature	19
$r_{DS(on)}$	P-channel MOSFET $r_{DS(on)}$	vs Input voltage	20
	N-channel MOSFET $r_{DS(on)}$	vs Input voltage	21
	PWM operation		22
	Power-save mode operation		23
	Start-up		24

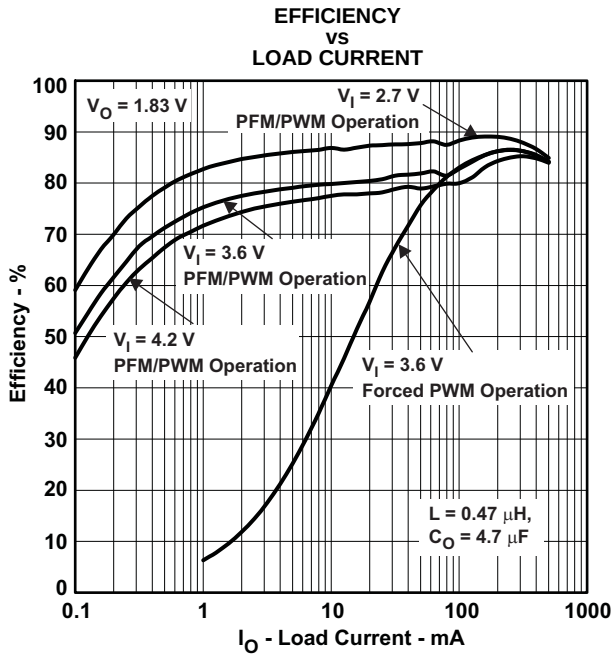

Figure 3.

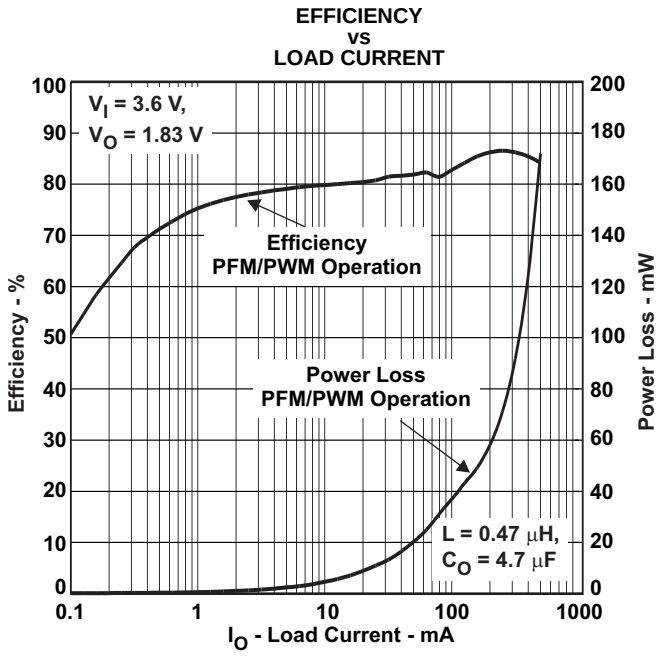

Figure 4.

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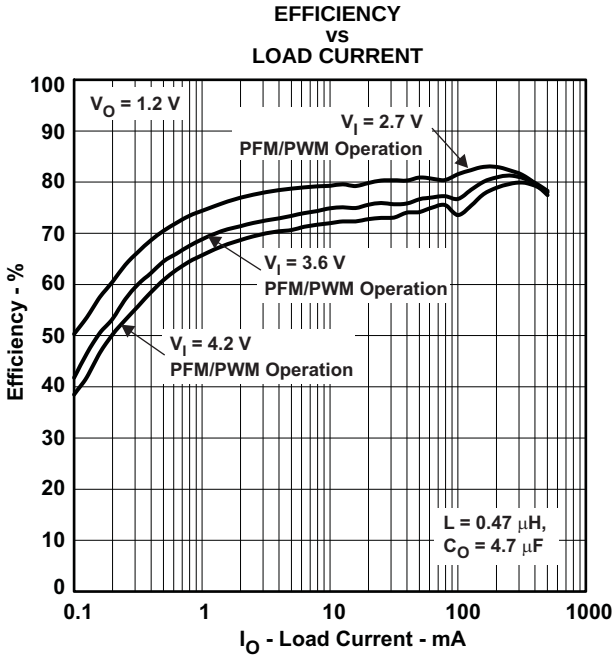

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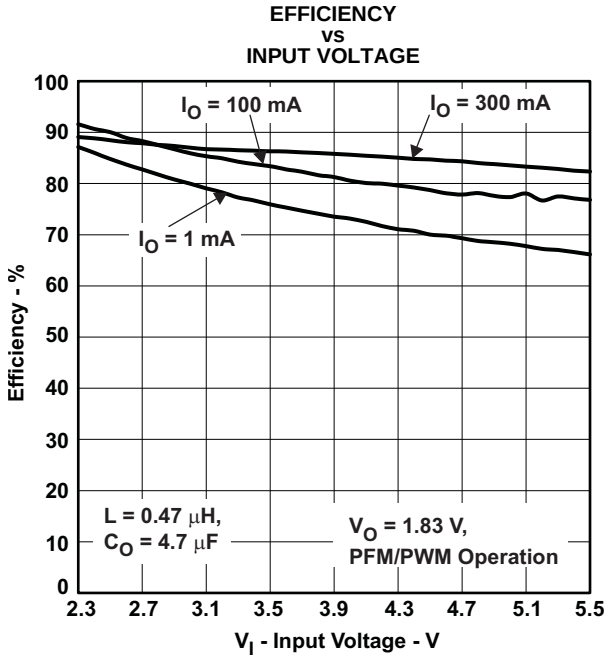

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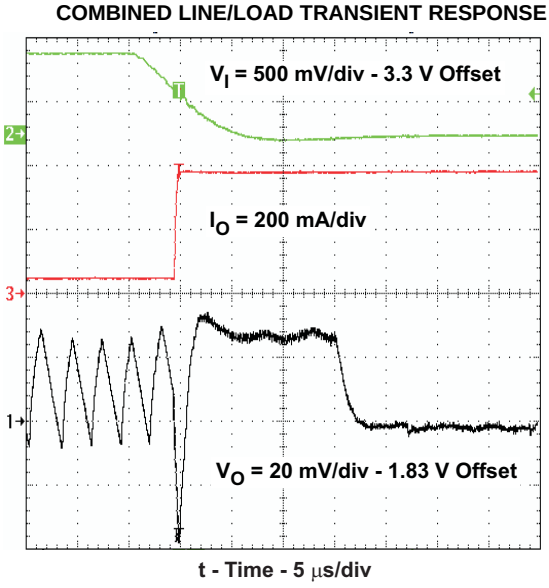

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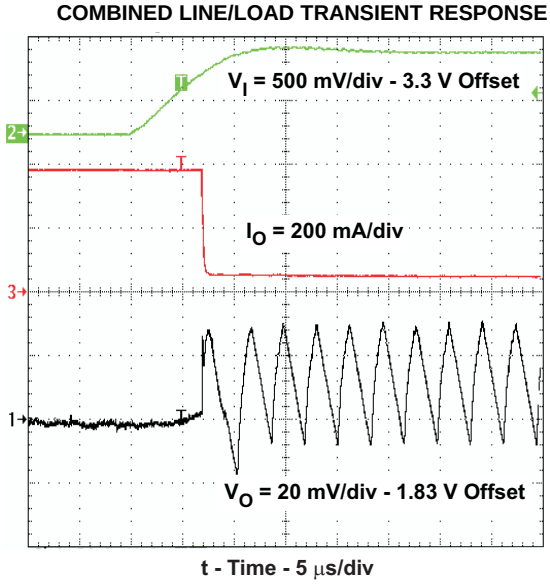

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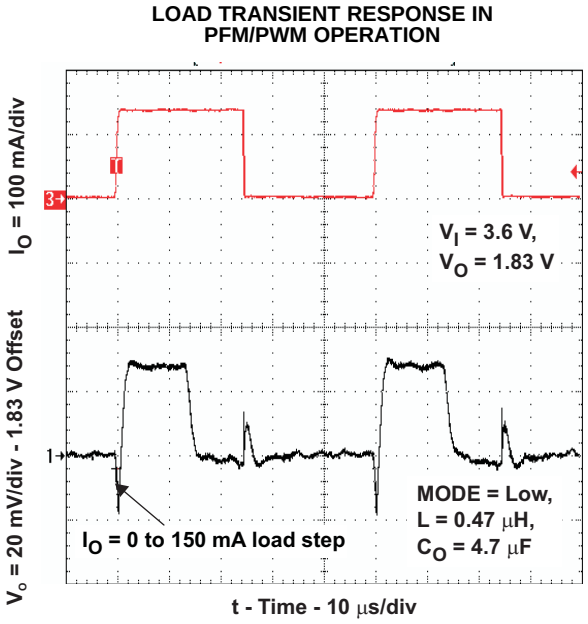

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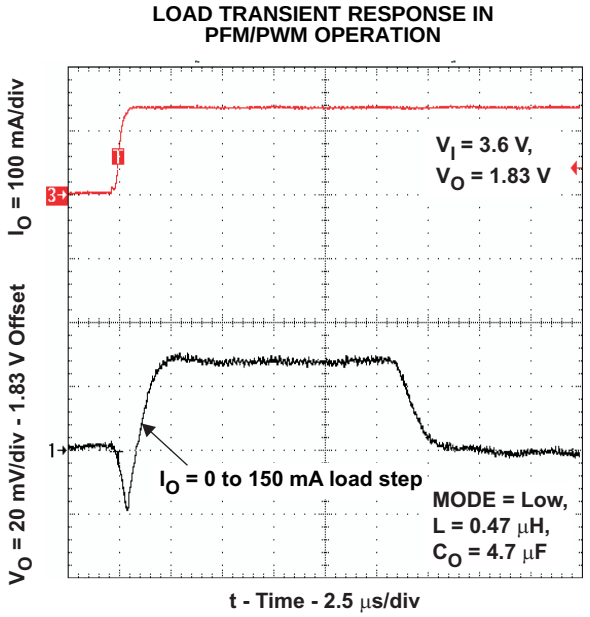

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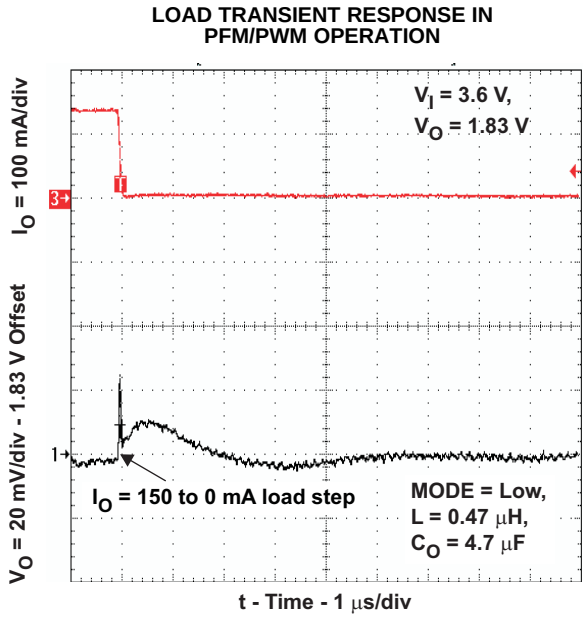

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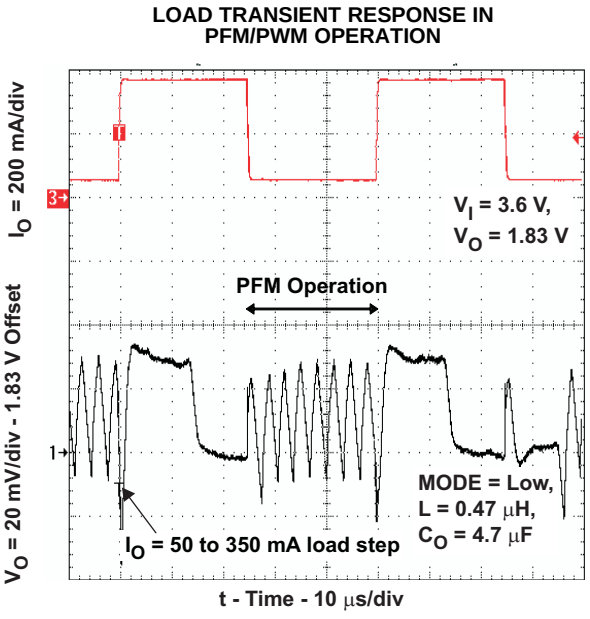

Figure 12.

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LOAD TRANSIENT RESPONSE IN
PFM/PWM OPERATION

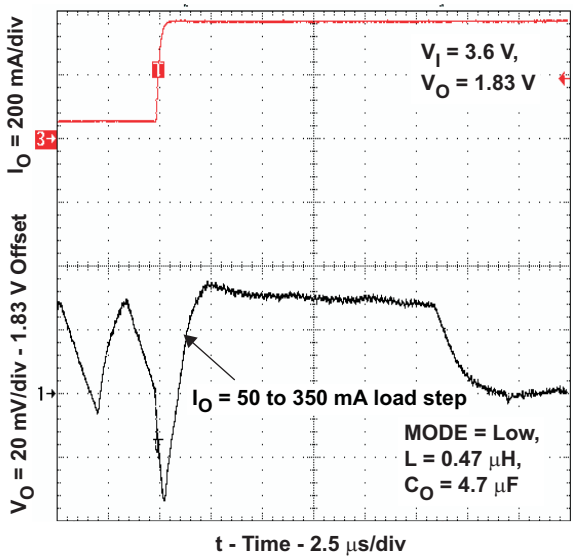

Figure 13.

LOAD TRANSIENT RESPONSE IN
PFM/PWM OPERATION

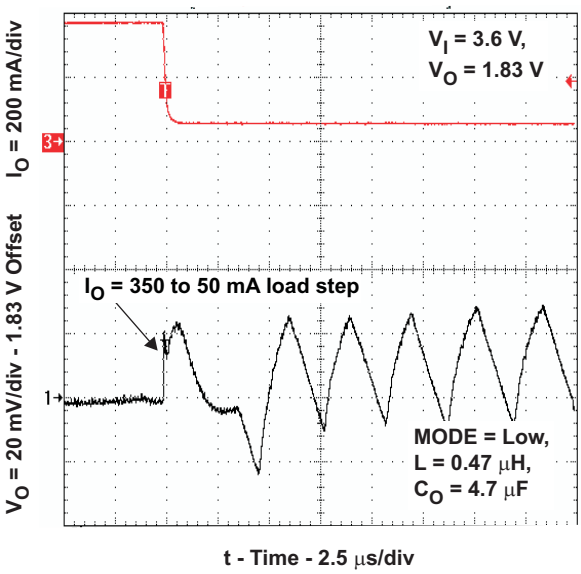

Figure 14.

LOAD TRANSIENT RESPONSE IN
PFM/PWM OPERATION

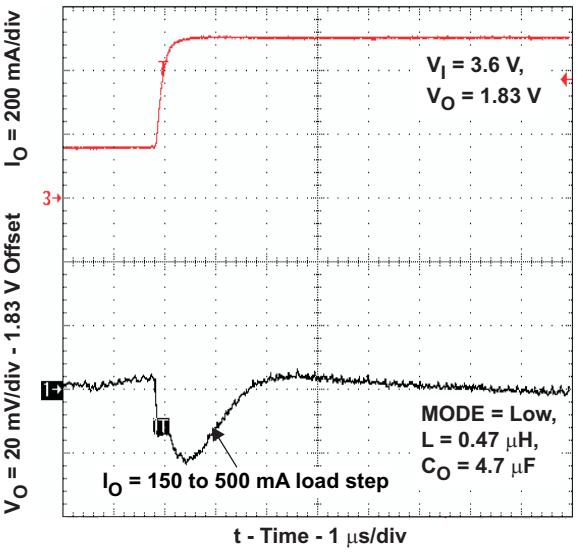

Figure 15.

LOAD TRANSIENT RESPONSE IN
PFM/PWM OPERATION

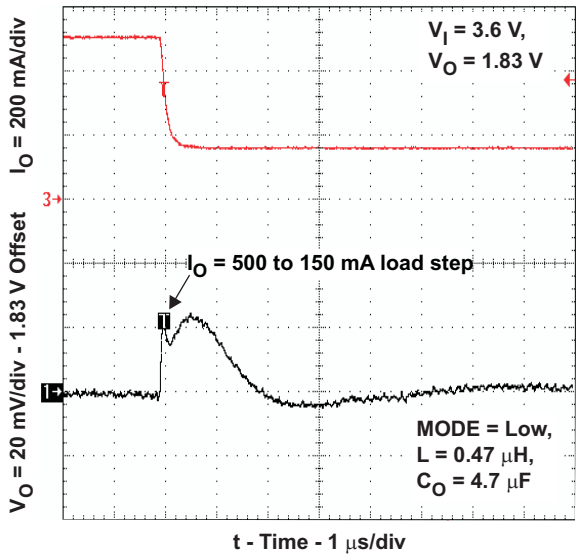

Figure 16.

OUTPUT VOLTAGE
vs
LOAD CURRENT

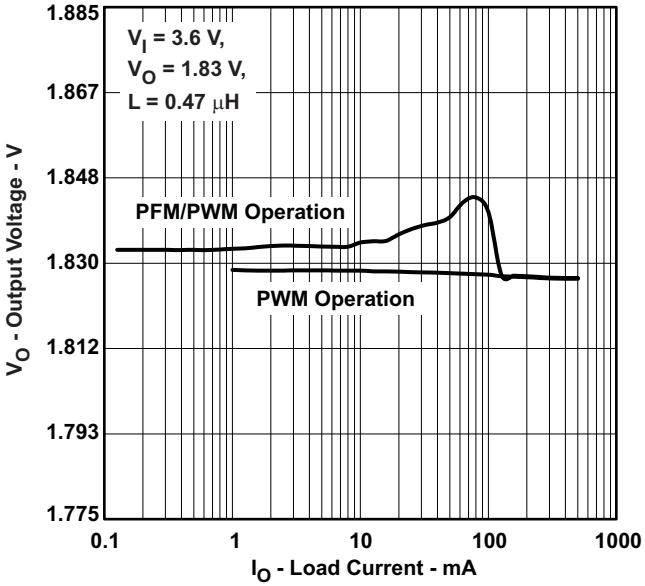

Figure 17.

QUIESCENT CURRENT
vs
INPUT VOLTAGE

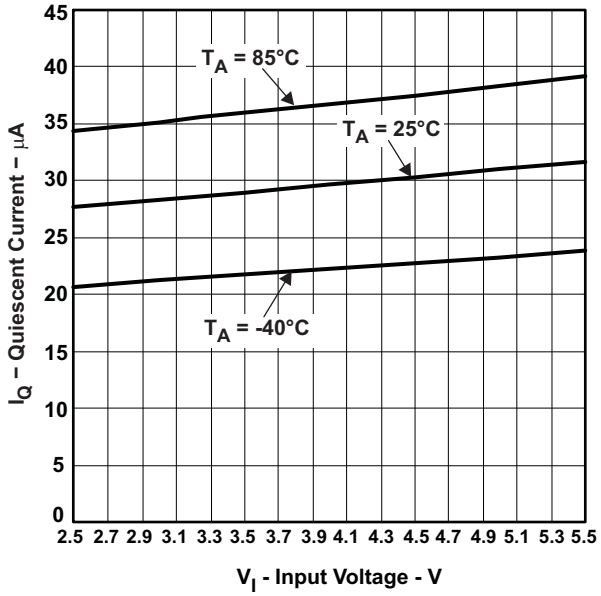

Figure 18.

SWITCHING FREQUENCY
vs
INPUT VOLTAGE

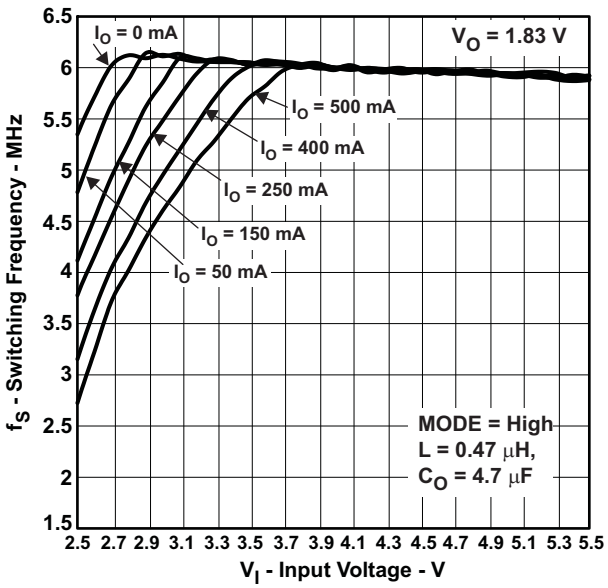

Figure 19.

P-CHANNEL $r_{DS(ON)}$
vs
INPUT VOLTAGE

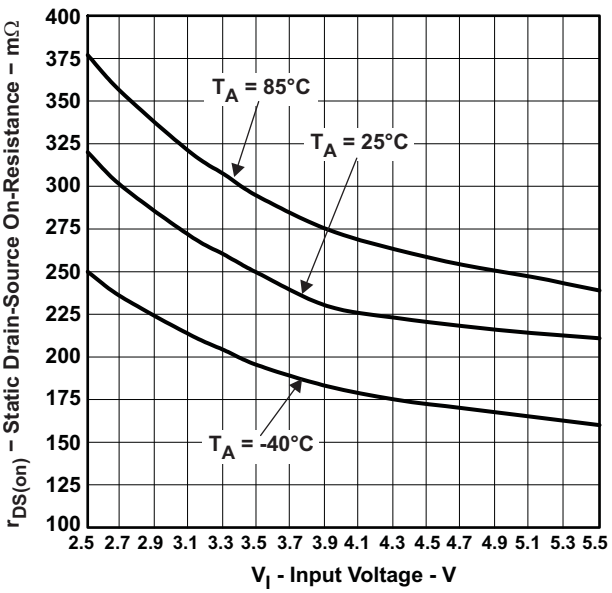

Figure 20.

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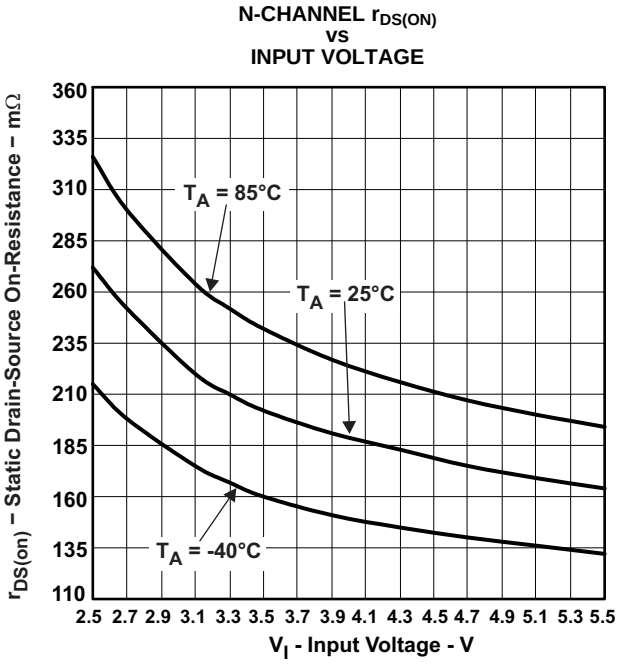

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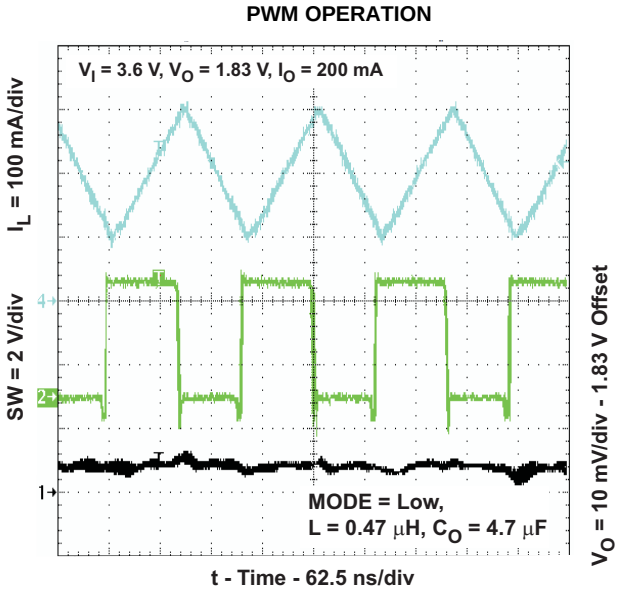

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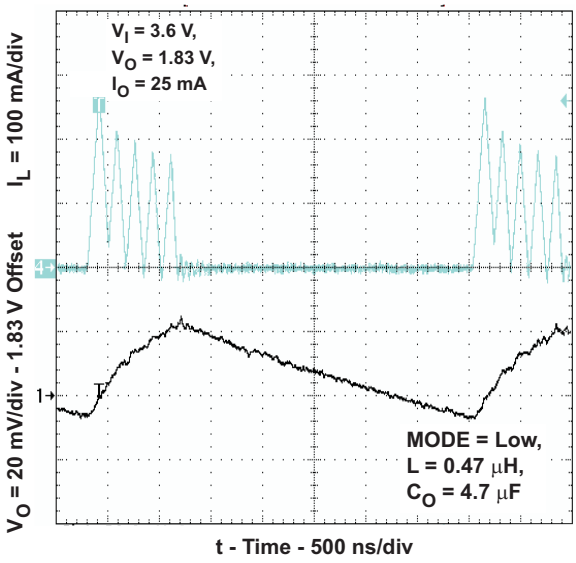

Figure 23.

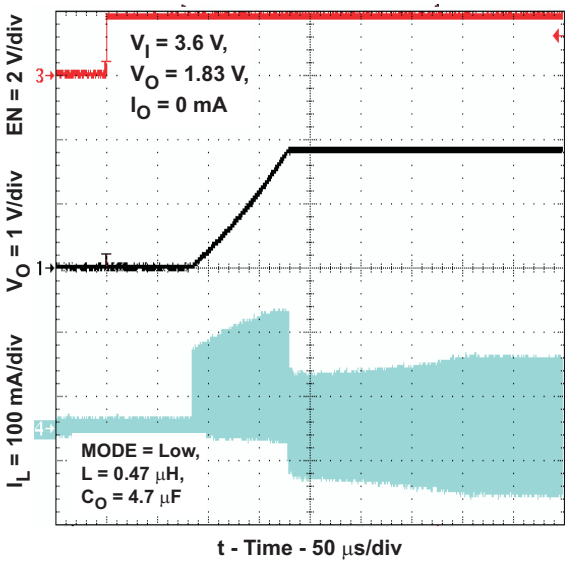

Figure 24.

DETAILED DESCRIPTION

OPERATION

The TPS6260x is a synchronous step-down converter typically operates at a regulated 6-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS6260x converter operates in power-save mode with pulse frequency modulation (PFM).

The converter uses a unique frequency locked ring oscillating modulator to achieve *best-in-class* load and line response and allows the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the P-channel MOSFET switch is turned on and the inductor current ramps up rising the output voltage until the main comparator trips, then the control logic turns off the switch.

One key advantage of the non-linear architecture is that there is no traditional feed-back loop. The loop response to change in V_O is essentially instantaneous, which explains the transient response. The absence of a traditional, high-gain compensated linear loop means that the TPS6260x is inherently stable over a range of L and C_O.

The device integrates two current limits, one in the P-channel MOSFET and another one in the N-channel MOSFET. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on. When the current in the N-channel MOSFET is above the N-MOS current limit threshold, the N-channel MOSFET remains on until the current drops below its current limit.

The current limit in the N-channel MOSFET is important for small duty-cycle operation when the current in the inductor does not decrease because of the P-channel MOSFET current limit delay, or because of start-up conditions where the output voltage is low.

SWITCHING FREQUENCY

The magnitude of the internal ramp, which is generated from the duty cycle, reduces for duty cycles either set of 50%. Thus, there is less overdrive on the main comparator inputs which tends to slow the conversion down. The intrinsic maximum operating frequency of the converter is about 10MHz to 12MHz, which is controlled to circa. 6MHz by a frequency locked loop.

When high or low duty cycles are encountered, the loop runs out of range and the conversion frequency falls below 6MHz. The tendency is for the converter to operate more towards a "constant inductor peak current" rather than a "constant frequency". In addition to this behavior which is observed at high duty cycles, it is also noted at low duty cycles.

When the converter is required to operate towards the 6MHz nominal at extreme duty cycles, the application can be assisted by decreasing the ratio of inductance (L) to the output capacitor's equivalent serial inductance (ESL). This increases the *ESL step* seen at the main comparator's feed-back input thus decreasing its propagation delay, hence increasing the switching frequency.

POWER-SAVE MODE

With decreasing load current, the device automatically switches into pulse skipping operation in which the power stage operates intermittently based on load demand. By running cycles periodically, the switching losses are minimized, and the device runs with a minimum quiescent current and maintaining high efficiency. The converter positions the dc output voltage approximately 0.5% above the nominal output voltage under light load conditions. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

When in power-save mode, the converter resumes its operation when the output voltage trips below the nominal voltage. It ramps up the output voltage with a minimum of three pulses and goes into power-save mode when the inductor current has returned to a zero steady state. As a consequence of the dynamic voltage positioning in the power-save mode, the average output voltage is slightly higher than its nominal value in PWM mode. For a load transient from light load to heavy load, the logic returns the regulated output voltage to nominal after 64 continuous cycles.

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The output current at which the PFM/PWM transition occurs is approximated by Equation 1:

$$I_{PFM/PWM} = \frac{V_O}{V_I} \times \frac{V_I - V_O}{2 \times L \times f_{SW}} \quad (1)$$

- $I_{PFM/PWM}$: output current at which PFM/PWM transition occurs
- f_{SW} : switching frequency (6-MHz typical)
- L : inductor value

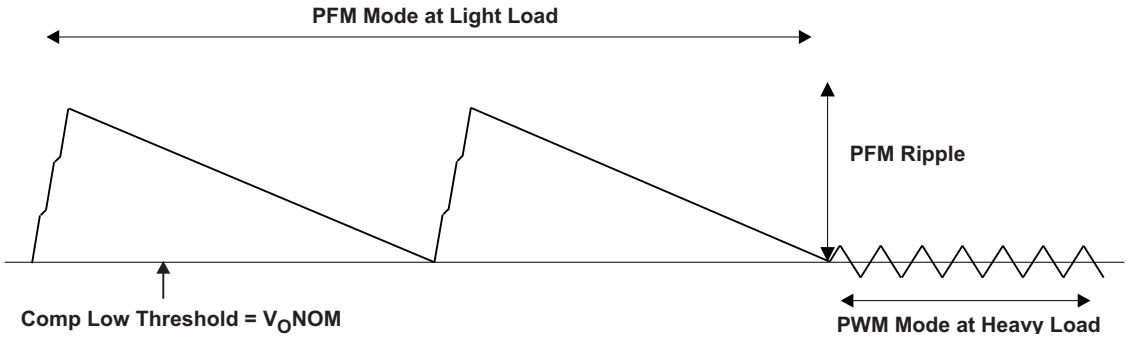

Figure 25. Operation in PFM Mode and Transfer to PWM Mode

MODE SELECTION

The MODE pin allows to select the operating mode of the device. Connecting this pin to GND enables the automatic PWM and power-save mode operation. The converter operates in fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter operates with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

ENABLE

The device starts operation when EN is set high and starts up with the soft start as previously described.

Pulling the EN pin low forces the device into shutdown, with a shutdown quiescent current of typically 0.1µA. In this mode, the P and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off. For proper operation, the EN pin must be terminated and must not be left floating.

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SOFT START

The TPS6260x has an internal soft-start circuit that limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the converter. The soft-start system progressively increases the on-time from a minimum pulse-width of 30ns as a function of the output voltage. This mode of operation continues for c.a. 180µs after enable. Should the output voltage not have reached its target value by this time, such as in the case of heavy load, the soft-start transitions to a second mode of operation.

The converter then operates in a current limit mode, specifically the P-MOS current limit is set to half the nominal limit, and the N-channel MOSET remains on until the inductor current has reset. After a further 100 µs, the device ramps up to the full current limit operation if the output voltage has risen above 0.7V (approximately). Therefore, the start-up time mainly depends on the output capacitor and load current.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The TPS6260x device have a UVLO threshold set to 2.05V (typical). Fully functional operation is permitted down to 2.1V input voltage.

SHORT-CIRCUIT PROTECTION

As soon as the output voltage falls below 0.7V (approximately), the converter current limit is reduced to half of the nominal value. Because the short-circuit protection is enabled during start-up, the device does not deliver more than half of its nominal current limit until the output voltage exceeds 0.7V (approximately). This needs to be considered when a load acting as a current sink is connected to the output of the converter.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds typically 140°C, the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs are turned off. The device continues its operation when the junction temperature again falls below typically 130°C.

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APPLICATION INFORMATION

INDUCTOR SELECTION

The TPS6260x series of step-down converters have been designed to operate with an effective inductance value in the range of 0.3µH to 1.3µH and with output capacitors in the range of 4.7µF to 10µF. The internal compensation is optimized to operate with an output filter of L = 0.47µH and C_O = 4.7µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For more details, see the *CHECKING LOOP STABILITY* section.

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher V_I or V_O.

$$\Delta I_L = \frac{V_O}{V_I} \times \frac{V_I - V_O}{L \times f_{SW}} \qquad \Delta I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2} \tag{2}$$

with: f_{SW} = switching frequency (6 MHz typical)

L = inductor value

ΔI_L = peak-to-peak inductor ripple current

$I_{L(MAX)}$ = maximum inductor current

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6260x converters.

Table 1. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS
MURATA	LQM21P_J0	2.0 x 1.2 x 1.0 max. height
	LQM21P_C0	2.0 x 1.2 x 0.55 max. height
HITACHI METALS	HSLI-201210AG-R47	2.0 x 1.2 x 1.0 max. height
	HSLI-201210SW-R85	2.0 x 1.2 x 1.0 max. height
	JSLI-201610AG-R70	2.0 x 1.6 x 1.0 max. height
TOKO	MDT2012-CX1R0-R	2.0 x 1.2 x 1.0 max. height

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OUTPUT CAPACITOR SELECTION

The advanced fast-response voltage mode control scheme of the TPS6260x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage step caused by the output capacitor ESL and the ripple current flowing through the output capacitor impedance.

At light loads, the device operates in power-save mode and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds and propagation delays. The typical output voltage ripple is 1.5% of the nominal output voltage V_O.

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. For most applications, a 2.2-µF capacitor is sufficient.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_I and the power source lead to reduce ringing than can occur between the inductance of the power source leads and C_I.

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_O immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_O. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_O to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_O can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

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LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. High-speed operation of the TPS6260x devices demand careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability and switching frequency issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.

The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. In order to get an optimum *ESL step*, the output voltage feedback point (FB) should be taken in the output capacitor path, approximately 1mm away for it. The feed-back line should be routed away from noisy components and traces (e.g. SW line).

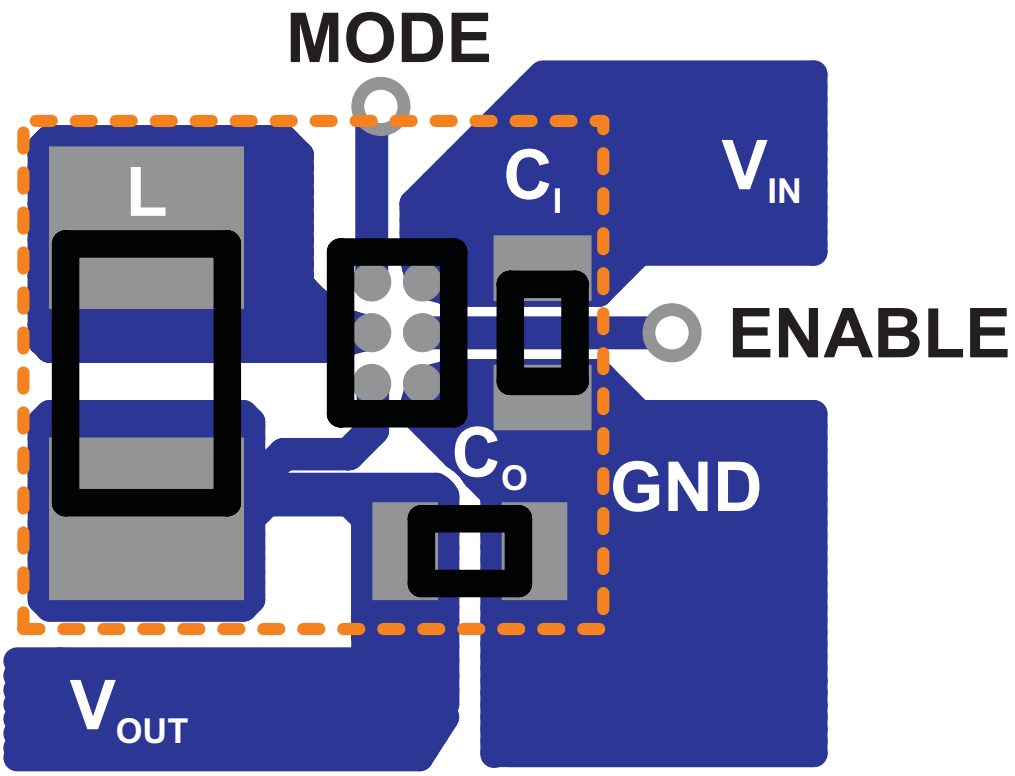


Figure 26. Suggested Layout (Top)

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component

Three basic approaches for enhancing thermal performance are listed below:

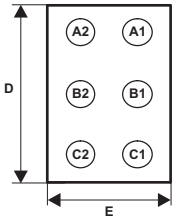
- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS6260x devices is 125°C. The thermal resistance of the 6-pin CSP package (YFF-6) is $R_{\theta JA}$ = 125°C/W. Regulator operation is specified to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 320 mW.

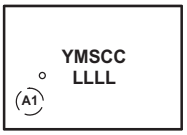
$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{125°C - 85°C}{125°C/W} = 320mW \quad (3)$$

PACKAGE SUMMARY

CHIP SCALE PACKAGE (BOTTOM VIEW)



CHIP SCALE PACKAGE (TOP VIEW)



Code:

- YM — Year Month date Code
- S — Assembly site code
- CC— Chip code
- LLLL — Lot trace code

CHIP SCALE PACKAGE DIMENSIONS

The TPS6260x device is available in an 6-bump chip scale package (YFF, NanoFree™). The package dimensions are given as:

- D = 1.290 ±0.05 mm
- E = 0.916 ±0.05 mm

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62601YFFT	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GA
TPS62601YFFT.B	Active	Production	DSBGA (YFF) | 6	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	GA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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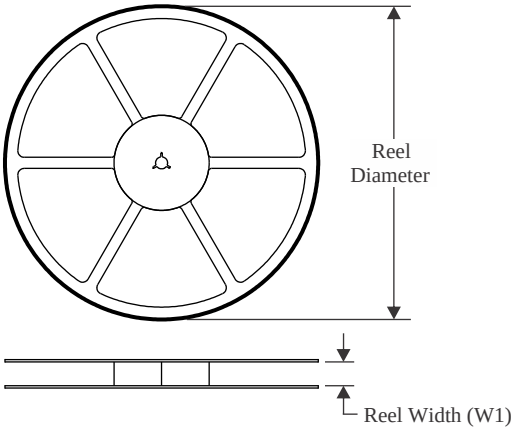
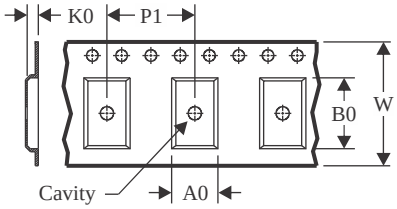
TAPE AND REEL INFORMATION

REEL DIMENSIONS

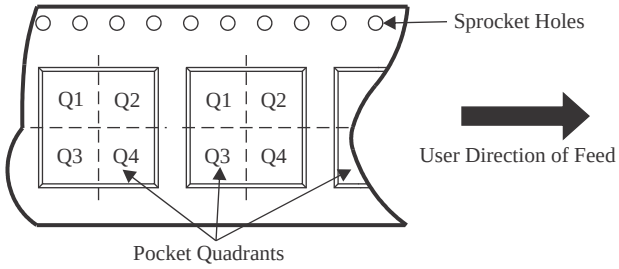


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

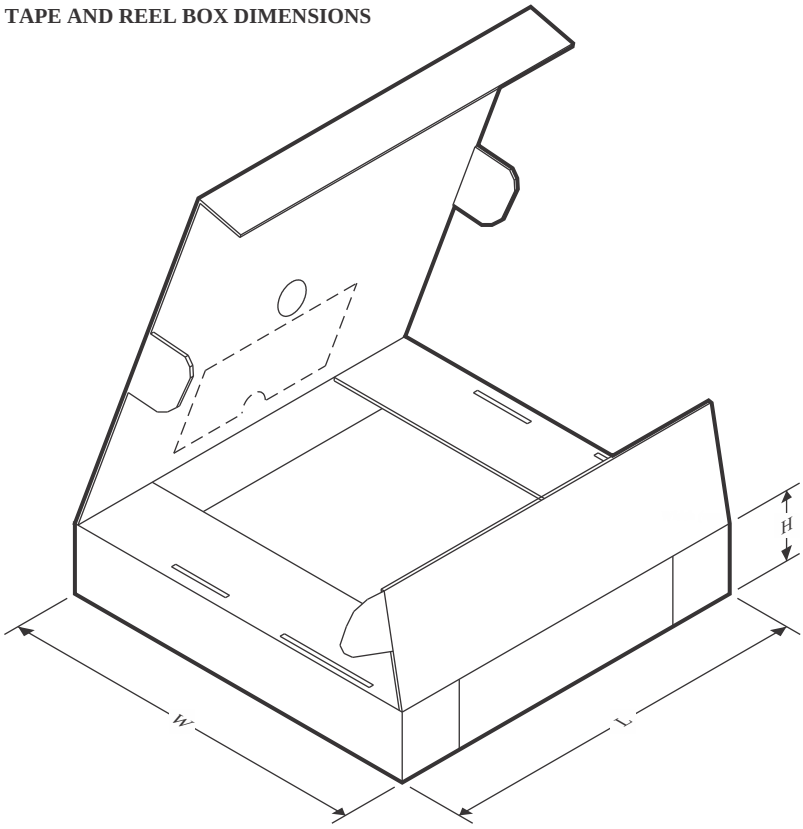
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62601YFFT	DSBGA	YFF	6	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

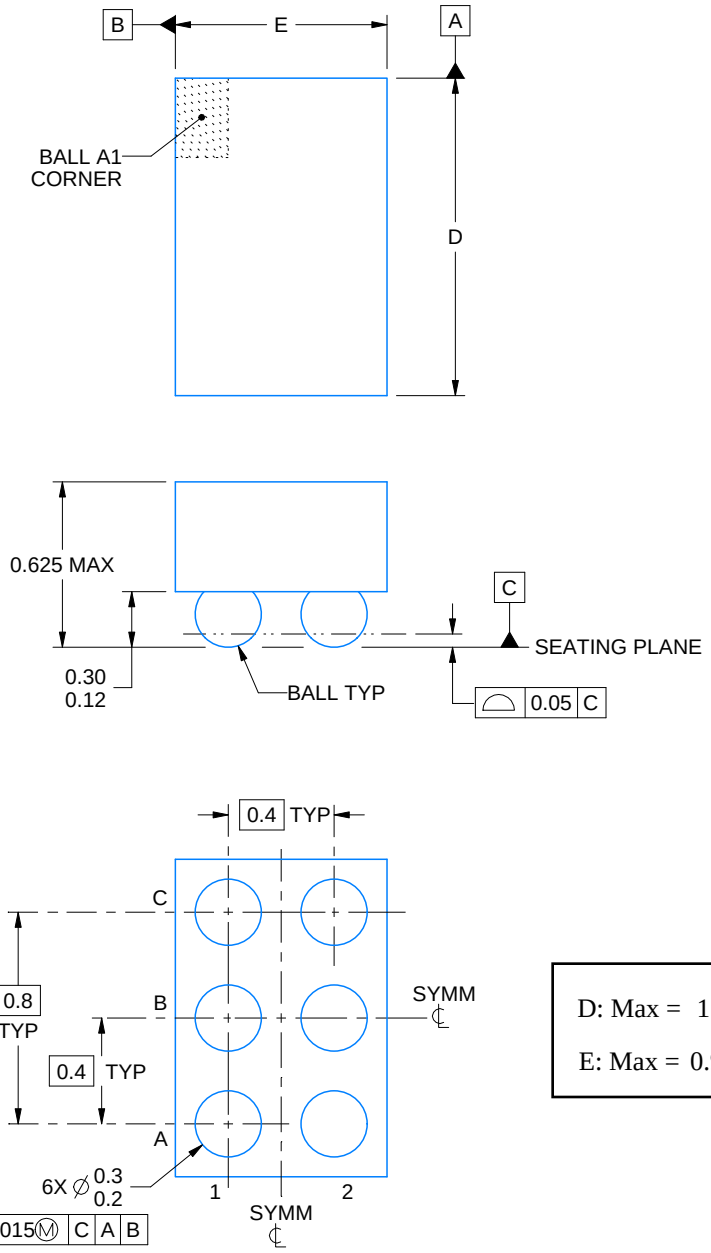
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62601YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



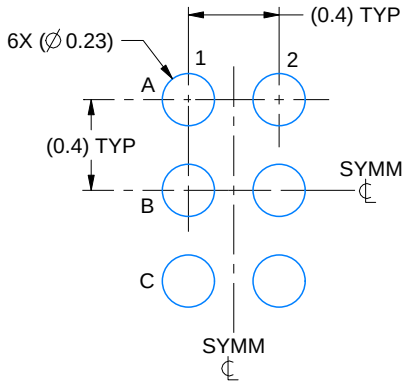
D: Max = 1.33 mm, Min = 1.27 mm

E: Max = 0.956 mm, Min =0.896 mm

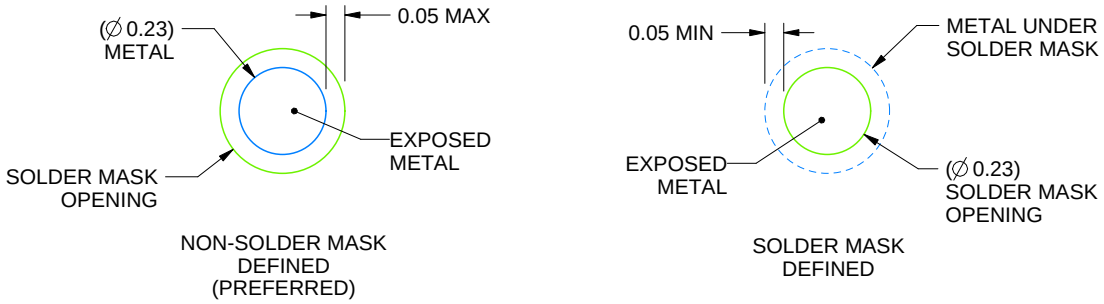
4223785/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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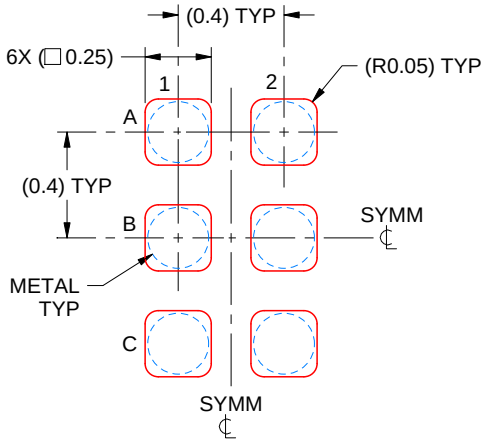
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:35X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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