TEXAS INSTRUMENTS
TPS628301, TPS628302, TPS628303, TPS628304
ZHCSNO6B – FEBRUARY 2023 – REVISED MARCH 2024

TPS62830x 采用小型 WQFN 和 SOT583 封装、具有 1% 输出精度的 2.25V 至 5.5V 输入、1A/2A/3A/4A 降压转换器

1 特性

- 2.25V 至 5.5V 输入电压范围
- 0.5V 至 4.5V 可调节输出电压
- 1% FB 电压精度（T_J 为 –40°C 至 125°C）
- 优化的 EMI 性能
- 有助于符合 CISPR 11/32 标准
  - 集成片上噪声滤波电容器
  - 可根据 CISPR 进行测量
- 出色的瞬态响应
- 7μA 运行静态电流
- 2.0MHz 开关频率
- 35mΩ 和 18mΩ 内部功率 MOSFET
- DCS-Control 拓扑
- MODE 引脚，用于选择导通模式
- 支持 1.2V GPIO
- 100% 占空比，可实现超低压降
- 有源输出放电
- 电源正常状态输出
- 热关断保护
- 断续或闭锁 OCP/OVP
- 提供 SIMPLIS 模型
- 使用 TPS62830x 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 固态硬盘
- 便携式电子产品
- 模拟安防摄像头和 IP 网络摄像头
- 工业 PC
- 工厂自动化和控制
- ASIC、SoC 和 MCU 电源
- 通用负载点

3 说明

TPS62830x 是一个具有低静态电流且易于使用的同步降压直流/直流转换器系列。TPS62830x 基于 DCS-Control 拓扑，可提供快速瞬态响应和较小的输出电容。由于具有内部基准，该系列器件可在 -40°C 至 125°C 的结温范围内，以 1% 的高反馈电压精度将输出电压调节到 0.5V 以下。该系列器件提供两种封装，各封装器件之间引脚对引脚兼容。

TPS62830x 具有一个 MODE 引脚，用于控制器件的工作模式。省电模式可在极轻负载下保持高效率，从而延长系统电池的运行时间。强制 PWM 模式会维持连续导通模式，从而确保超低的输出电压纹波和准固定开关频率。该器件具有电源正常信号和受控良好的内部软启动电路。TPS62830x 能够以 100% 模式运行。在故障保护方面，TPS62830x 加入了断续短路保护以及热关断功能。一个器件选项具有针对短路和过压事件的闭锁保护。该系列提供两种封装：8 引脚 1.0mm × 2.0mm QFN 封装，提供超高功率密度设计；8 引脚 1.6mm × 2.1mm SOT583 封装，提供易于组装的设计。

封装信息

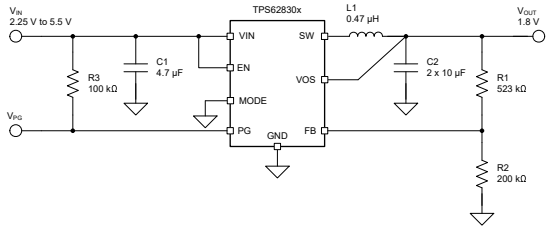
器件型号	封装(1)	封装尺寸(2)
TPS62830x	RZE（WQFN，8）	1mm x 2mm
	DRL（SOT583，8）	2.1mm x 1.6mm

(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）

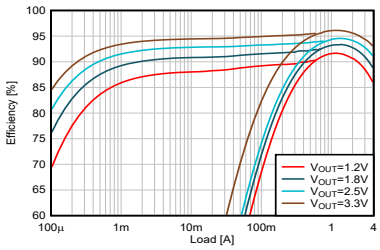
器件信息

器件型号(1)	输出电流	OCP 模式	软启动时间
TPS62830xA	1A、2A、3A、4A	断续	300μs
TPS62830xB	3A	闭锁	300μs
TPS62830xK	1A、2A、3A、4A	断续	880μs

(1) 请参阅*器件选项*表。



典型应用原理图



V_{IN} = 5V 时的效率

Table of Contents

4 Device Options

PART NUMBER	OUTPUT CURRENT	SOFT START, t_{SS}	OCP MODE	PACKAGE	OUTPUT VOLTAGE
TPS628301ARZER	1A	300µs	Hiccup	WQFN-HR	Adjustable(2)
TPS628302ARZER	2A				
TPS628303ARZER	3A				
TPS628304ARZER	4A				
TPS628301KRZER	1A	880µs			
TPS628302KRZER	2A				
TPS628303KRZER	3A				
TPS628304KRZER	4A				
TPS628301ADRLR	1A	300µs		SOT583	
TPS628302ADRLR	2A				
TPS628303ADRLR	3A				
TPS628304ADRLR	4A				
TPS628303BDRLR	3A		OCP/OVP Latch-off(1)		

(1) For other output current versions with OCP/OVP Latch-off, please contact Marketing for availability.
(2) For fixed output voltage versions, please contact Marketing for availability.

5 Pin Configuration and Functions

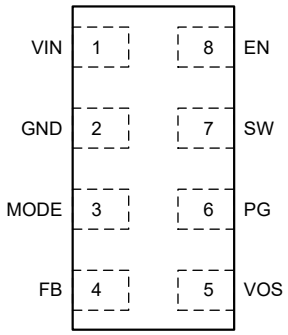


图 5-1. RZE Package 8-Pin WQFN Top View

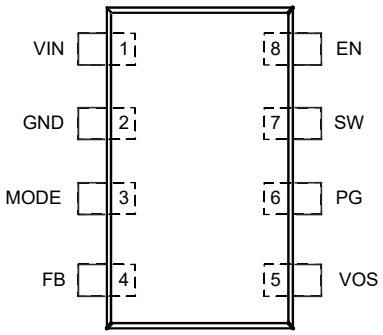


图 5-2. DRL Package 8-Pin SOT Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VIN	1	PWR	Input voltage pin. Connect the input capacitor as close as possible between V_{IN} and GND.
GND	2		Ground pin.
MODE	3	I	The device runs in PSM/PWM mode when this pin is pulled low and in forced-PWM mode when pulled high. This event can also be done when the device is in-operation. Do not leave this pin floating.
FB	4	I	Feedback pin. Connect the resistive output voltage divider to this pin.
VOS	5	I	Output voltage sense pin. This pin must be connected directly after the inductor.
PG	6	O	Power good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave this pin floating.
SW	7	PWR	Switch pin of the power stage
EN	8	I	Device enable pin. To enable the device, this pin must be pulled high. Pulling this pin low disables the device. Do not leave this pin unconnected.

(1) I = input, O = output, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage (2)	V_{IN}, EN, MODE, FB, PG	–0.3	6	V
Voltage (2)	SW (DC)	–0.3	V_{IN} + 0.3	V
Voltage (2)	SW (AC , < 10 ns) (3)	–2.5	10	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.
(3) While switching

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	± 2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.25		5.5	V
V_{OUT}	Output voltage range	0.5		4.5	V
C_{IN}	Effective input capacitance (1)	3			µF
L	Nominal output inductor	0.24	0.47	1.0	µH
C_{OUT}	Effective output capacitance (1)	12		200	µF
I_{OUT}	Output current range; TPS628301			1	A
I_{OUT}	Output current range; TPS628302			2	A
I_{OUT}	Output current range; TPS628303			3	A
I_{OUT}	Output current range; TPS628304 (2)			4	A
I_{PG}	Power-good input current capability			1	mA
T_J	Operating junction temperature	–40		125	°C

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer´s DC bias curves for the effective capacitance vs DC voltage applied.
(2) Lifetime is reduced when operating continuously at I_{OUT} = 4 A and the junction temperature > 105°C.

6.4 Thermal Information Discrete

THERMAL METRIC(1)		TPS62830xRZE		TPS62830xDRL		UNIT
		8 pin-WQFN		8 pin-SOT583		
		JEDEC	EVM	JEDEC	EVM	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.7	77.6	110.9	80	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90.9	n/a(2)	41.4	n/a(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.7	n/a(2)	22.2	n/a(2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.7	2.8	0.8	1.3	°C/W

6.4 Thermal Information Discrete（续）

THERMAL METRIC(1)		TPS62830xRZE		TPS62830xDRL		UNIT
		8 pin-WQFN		8 pin-SOT583		
		JEDEC	EVM	JEDEC	EVM	
ψ_{JB}	Junction-to-board characterization parameter	30.7	44.7	22.1	28.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.
(2) Not applicable to an EVM.

6.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 2.25 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating quiescent current	EN = V_{IN}, I_{OUT} = 0 mA, V_{OUT} = 1.8 V, MODE = GND, device not switching		7	17	µA
I_{SD}	V_{IN} shutdown supply current	EN = low, T_J = –40°C to 85°C		100	700	nA
$V_{UVLO(+)}$	Rising UVLO threshold voltage (V_{IN})		2.05	2.15	2.25	V
$V_{UVLO(hys)}$	UVLO hysteresis (V_{IN})		90	120		mV
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	T_J rising		150		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC PINs						
$V_{EN(+)}$	High-level input voltage (EN)		0.8			V
$V_{EN(-)}$	Low-level input voltage (EN)				0.35	V
$V_{MODE(+)}$	High-level input voltage (MODE)		0.8			V
$V_{MODE(-)}$	Low-level input voltage (MODE)				0.35	V
$I_{EN(LKG)}$	EN Input leakage current	V_{EN} = HIGH		10	100	nA
$I_{MODE(LKG)}$	MODE Input leakage current	V_{MODE} = HIGH		10	100	nA
STARTUP						
t_{SS}	Internal fixed soft-start time	From V_{OUT} = 0 to V_{OUT} = 95%	180	300	440	µs
t_{SS}	Internal fixed soft-start time	From V_{OUT}= 0 to V_{OUT}= 95%; only TPS62830x***K*** versions	530	880	1300	µs
$t_{d(EN)}$	Enable delay time	From EN HIGH to device starts switching		120	220	µs
REFERENCE VOLTAGE						
V_{FB}	Feedback voltage accuracy	PWM mode	495	500	505	mV
V_{FB}	Feedback voltage accuracy	PWM mode	–1		+1	%
V_{FB}	Feedback voltage accuracy	PFM mode, $C_{OUT,eff}$ ⩾ 15 µF, L = 0.47 µH	–1		+2	%
$I_{FB(LKG)}$	FB input leakage current, adjustable version	V_{FB} = 0.5 V		10	70	nA
$I_{VOS(LKG)}$	VOS input leakage current	V_{EN} = low		100	500	nA
POWER GOOD						
$V_{PG,UV(+)}$	Rising power-good threshold voltage (output undervoltage)	Power Good low, V_{FB} rising	94	96	98	%
$V_{PG,UV(-)}$	Falling power-good threshold voltage (output undervoltage)	Power Good high, V_{FB} falling	90	92	94	%
$V_{PG,OV(+)}$	Rising power-good threshold voltage (output overvoltage)	Power Good high, V_{FB} rising	108	110	112	%
$V_{PG,OV(-)}$	Falling power-good threshold voltage (output overvoltage)	Power Good low, V_{FB} falling	102.5	105	107	%
$t_{d(PG)}$	Power good delay at start-up	Low-to-high transition on the PG pin at start up		128		µs
$t_{d(PG)}$	Power good deglitch delay during operation	High-to-low or low-to-high transition on the PG pin	30	45	60	µs
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	V_{PG} = 5.0 V		10	100	nA

6.5 Electrical Characteristics（续）

T_J = –40°C to +125°C, V_{IN} = 2.25 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PG,OL}$	PG pin low-level output voltage	I_{PG} = 1 mA			0.4	V
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	$V_{IN} \geqslant$ 5 V		35	57	mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	$V_{IN} \geqslant$ 5 V		18	29	mΩ
f_{SW}	Switching frequency, PWM mode	I_{OUT} = 1 A, V_{OUT} = 1.8 V		2.0		MHz
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	TPS628301	1.8	2.1	2.6	A
$I_{HS(OC)}$	High-side peak current limit	TPS628302	2.7	3.3	3.9	A
$I_{HS(OC)}$	High-side peak current limit	TPS628303	4.0	4.6	5.4	A
$I_{HS(OC)}$	High-side peak current limit	TPS628304	5.0	5.9	7.0	A
$I_{LS(NOC)}$	Low-side negative current limit	Sinking current limit on LS FET		–1.8		A
OUTPUT DISCHARGE						
I_{DIS}	Output discharge current on SW pin	V_{IN} > 2 V, V_{SW} = 0.4 V, EN = LOW	75	400		mA
OUTPUT OVP						
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	V_{FB} rising; devices with OVP feature only	108	110	112	%
$t_{d(OVP)}$	OVP delay	Devices with OVP feature only		35		µs

6.6 Typical Characteristics

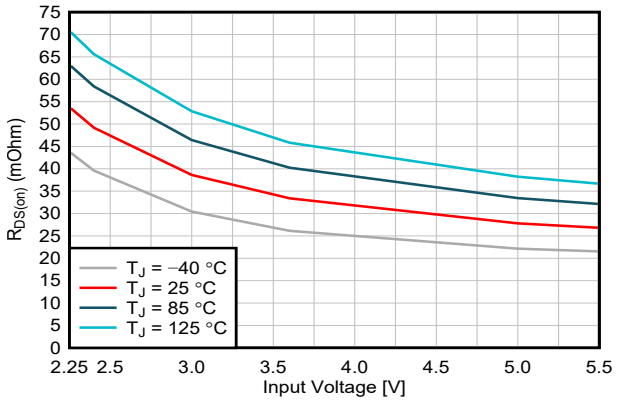


图 6-1. High-Side FET On-Resistance

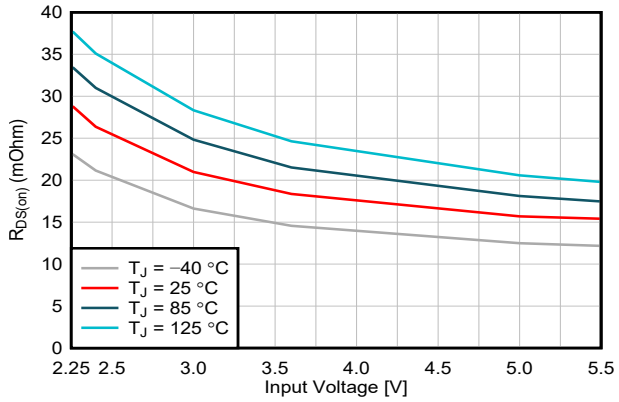


图 6-2. Low-Side FET On-Resistance

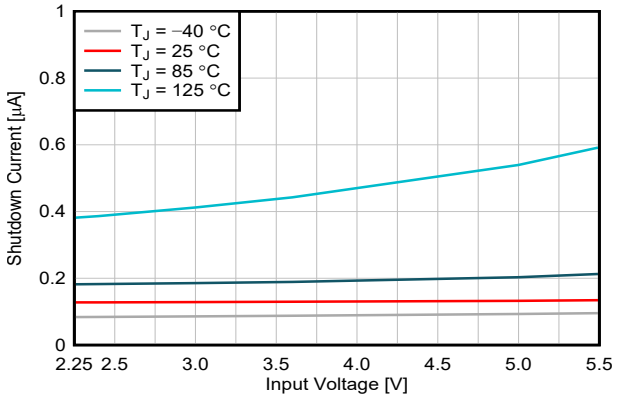


图 6-3. Shutdown Current

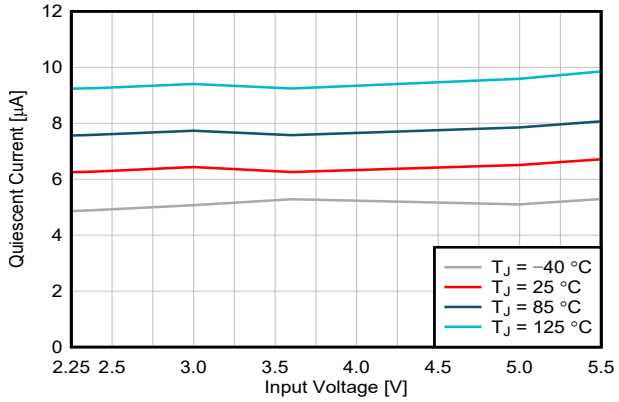


图 6-4. Quiescent Current

7 Detailed Description

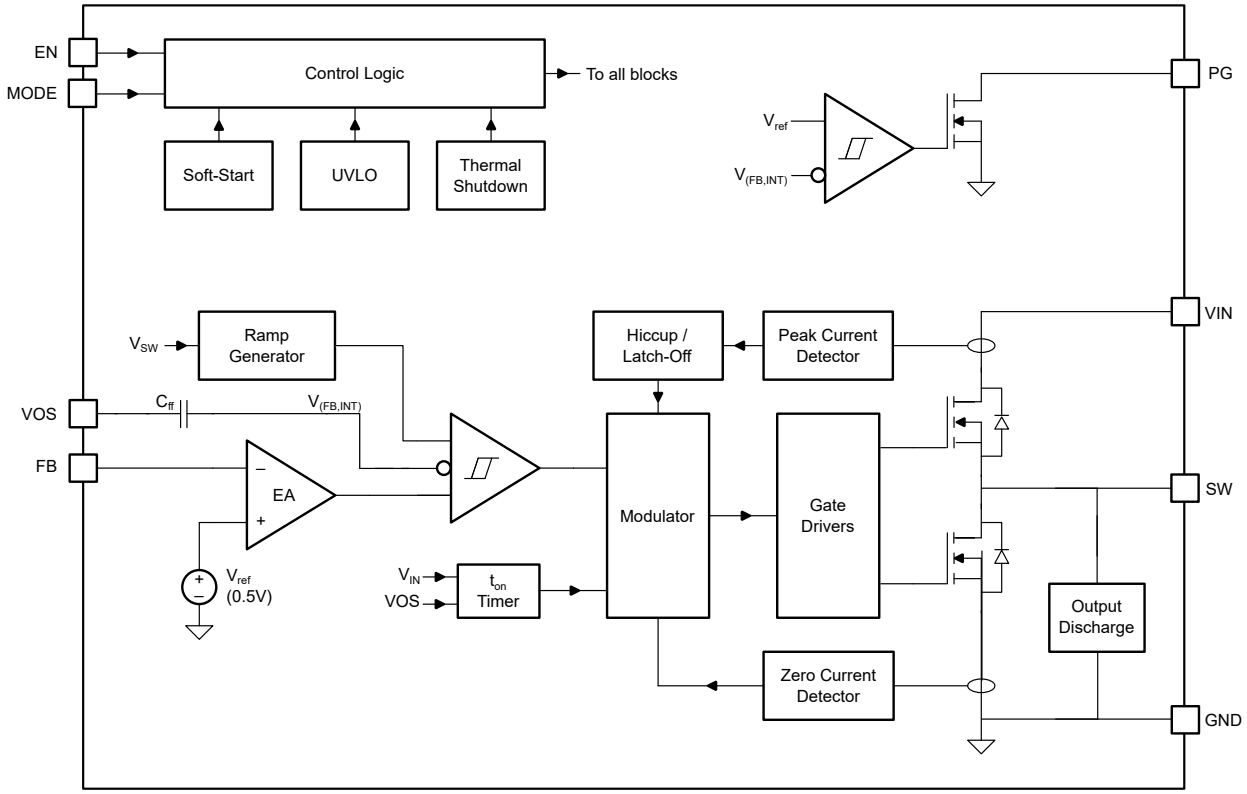
7.1 Overview

The TPS62830x is a family of low-voltage step-down converters available in 1-, 2-, 3- and 4-A versions. These devices use a DCS-Control scheme which transitions seamlessly from pulse-width modulation (PWM) at medium and high output currents to pulsed-frequency modulation (PFM) at low output currents. During PWM operation, the devices switch at 2 MHz; during PFM operation, the switching frequency varies with the load current and reduces as the load current decreases. For applications that require the lowest possible output voltage ripple or a constant switching frequency, a high logic level on the MODE pin forces the devices to use PWM under all load conditions (at the expense of lower efficiency at low output currents). An external resistor-divider sets the output voltage anywhere from 0.5 V to 4.5 V and the nominal switching frequency is 2 MHz with a controlled variation over the input voltage range.

Device variants are available that support both hiccup and latch-off protection behavior.

The TPS62830x devices offer two significant advantages compared to previous devices in this series: Transient performance has improved significantly by usage of a fast comparator in both PFM and PWM modes, and EMI is reduced by an on-chip decoupling capacitor and an optimized gate driver.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pulse Width Modulation (PWM) Operation

If the MODE pin is LOW and at load currents larger than half the inductor ripple current, the device operates in pulse width modulation in continuous conduction mode (CCM) as shown in 图 7-1. The PWM operation is based on an adaptive constant on-time control with stabilized switching frequency. To achieve a stable switching frequency in a steady state condition, the on-time is calculated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 500ns \quad (1)$$

If the MODE pin is HIGH, the converter maintains a forced-PWM operation for all load currents.

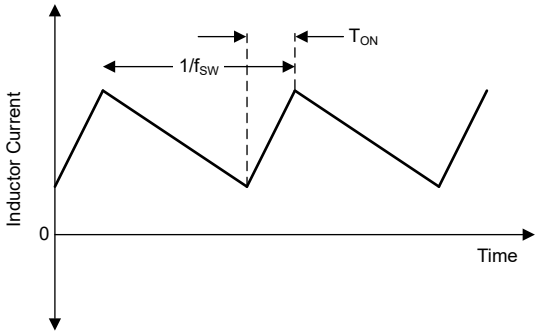


图 7-1. Continuous Conduction Mode (PWM-CCM) Current Waveform

7.3.2 Power Save Mode (PSM) Operation

To maintain high efficiency at light loads, the device enters power save mode (PSM) at the boundary to discontinuous conduction mode (DCM). This event happens when the output current becomes smaller than half of the ripple current of the inductor. The device operates with a fixed on-time, and the switching frequency decreases proportional to the load current as shown in 图 7-2. Calculate as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{T_{ON}^2 \times \frac{V_{IN}}{V_{OUT}}\left[\frac{V_{IN} - V_{OUT}}{L}\right]} \quad (2)$$

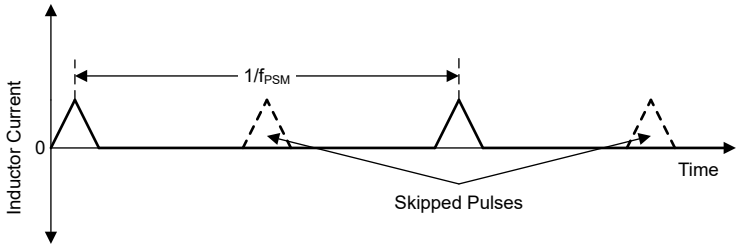


图 7-2. Discontinuous Conduction Mode (PSM-DCM) Current Waveform

In PSM, the output voltage rises slightly above the nominal target, which can be minimized using larger output capacitance. At duty cycles larger than 90%, the device does not enter PSM and maintains output regulation in PWM mode.

7.3.3 Start-Up and Soft Start

When the EN voltage goes High, the device starts loading the default values into the device registers. This action typically is done within 120 μs. After that, the internal soft-start circuitry controls the output voltage during start-up. This control avoids excessive inrush current and makes sure of a controlled output voltage ramp. This control also prevents unwanted voltage drops from high-impedance power sources or batteries. Finally, the PG signal has a delay up to 180 μs at start-up. 图 7-3 shows a start-up sequence, where the EN pin is pulled up to VIN.

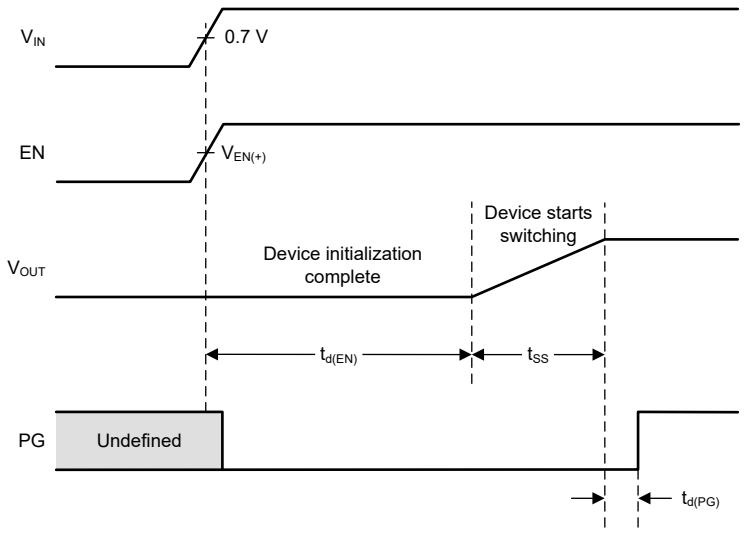


图 7-3. Start-Up Timing When EN is Pulled Up to VIN

图 7-4 shows a start-up sequence, where an external signal is connected to the EN pin.

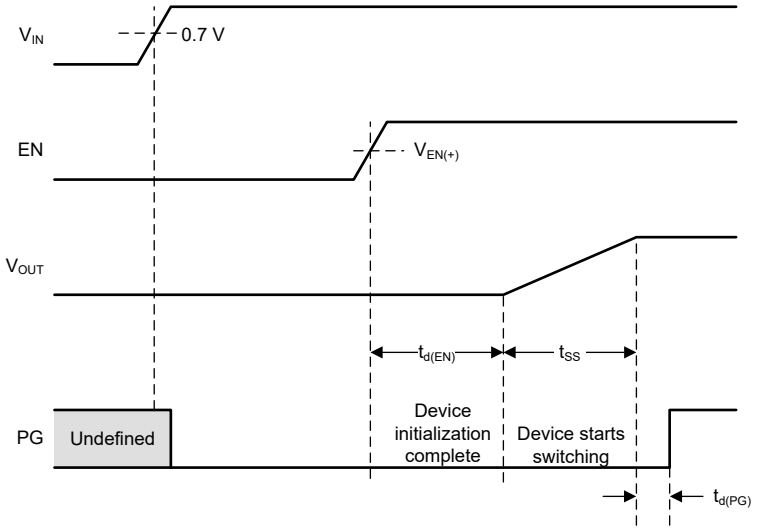


图 7-4. Start-Up Timing When an External Signal is Connected to the EN Pin

The TPS62830x can start into a prebiased output if enabled for the first time. For a new prebiased operation, a power cycle is needed to disable the active output discharge. 图 7-5 shows a start-up into a prebiased output voltage.

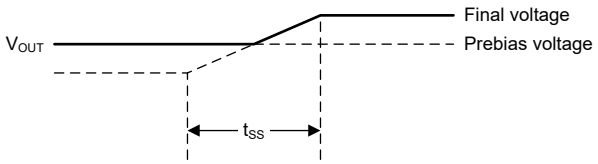


图 7-5. Start-Up into a Prebiased Output

7.3.4 Switch Cycle-by-Cycle Current Limit

All the devices in the family have a cycle-by-cycle current limit function. When the device detects that the current in the high-side FET exceeds the high-side current limit, either due to a heavy load or a short-circuit condition, the device immediately turns off the high-side FET and turns on the low-side FET. The high-side FET turns on again at the start of the next switching cycle. Note that because of the propagation delay in the current limit comparator (typically 60 ns), the current flowing in the high-side FET when the device detects a current limit condition can be slightly higher than the current limit specified in the device Electrical Characteristics.

Devices with an 'A' and 'K' suffix in their part number respond to repeated current limit events with hiccup behavior (see *Device Options*).

Devices with a 'B' suffix in their part number respond to repeated current limit events with latch-up behavior (see *Device Options*).

7.3.5 Short-Circuit Protection

In devices with hiccup protection, when a current limit event occurs for 32 consecutive switching cycles (about 16 µs), the device turns off the high-side FET for about 9.6 ms, during which time the inductor current decays through the low-side FET body diode. After 9.6 ms has expired, the device automatically starts switching again, beginning with a soft-start condition. The device alternates between bursts of switching cycles and 9.6-ms pauses for as long as the overload condition on the output exists.

In devices with latch-off protection, When a current limit event occurs for 32 consecutive switching cycles (about 16 µs), the device stops switching and latches off the high-side and low-side FETs. To recover normal operation after a latched short-circuit event, you must cycle V_{IN} or EN.

In devices with latch-off protection, there is also an OVP protection circuit that uses the PG window comparator. An OVP event is detected when the FB voltage is approximately 110% × (0.5V) for a period longer than the deglitch time of 35 µs. In this case, the converter de-asserts the PG signal and performs the overvoltage protection function. The converter latches off both high-side and low-side FET and remains in this state. To recover normal operation after a latched short-circuit event, you must cycle V_{IN} or EN.

7.3.6 Undervoltage Lockout

The undervoltage lockout (UVLO) function prevents misoperation of the device if the input voltage drops below the UVLO threshold.

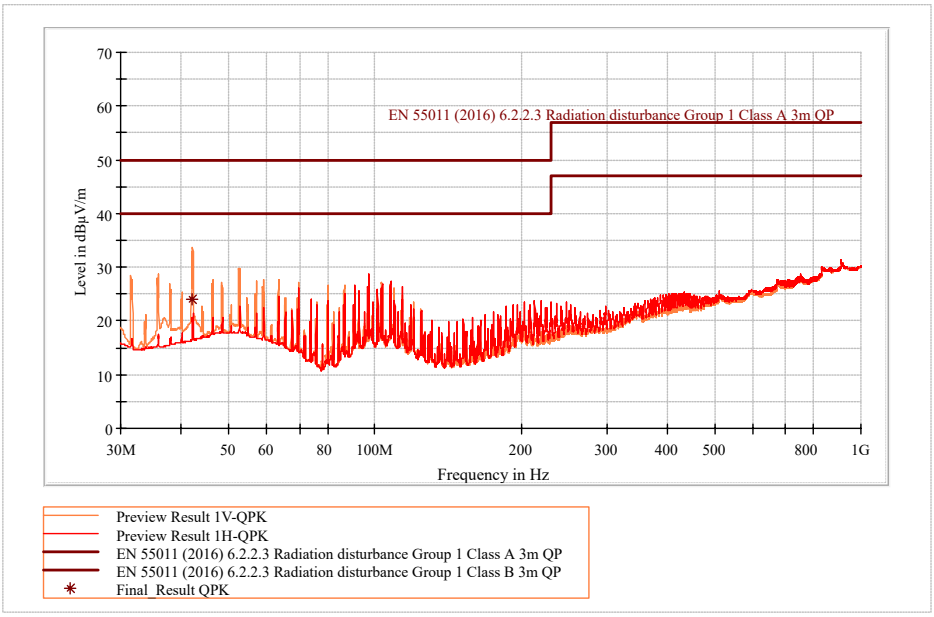
7.3.7 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 150°C (typical), the device goes in thermal shutdown with a hysteresis of typically 20°C. After T_J has decreased enough, the device resumes normal operation.

7.3.8 Optimized EMI Performance

TPS62830x devices incorporate advanced techniques to minimize Electromagnetic Interference (EMI) and makes complying with stringent EMI standards simple. By integrating capacitors directly onto the silicon, parasitic elements are reduced and loop area is minimized, effectively reducing high-frequency noise emissions primarily above 450 MHz. The on-chip capacitors ensure low-inductance paths for high-frequency AC switching current and damping voltage ringing.

Additionally to the on-chip capacitors, the gate driver has been improved with advanced slew rate control mechanisms and by smoothing the supply voltage. The switch node voltage is controlled in a way to reduce sharp edges and minimize voltage overshoot, consequently diminishing EMI.



The above plot is measured on the EVM with the TPS628304ARZER and standard BOM. There is no notable difference on EMI performance between available packages.

I_{OUT} = 4 A V_{IN} = 5.5 V V_{OUT} = 1.8 V

图 7-6. Radiated EMI Performance (CISPR11 Radiated Emission Test with Class A and Class B Limits)

7.4 Device Functional Modes

7.4.1 Enable, Disable, and Output Discharge

The device starts operation when Enable (EN) is set High. The input threshold levels are typically 0.8 V for rising and 0.35 V for falling signals. Do not leave EN floating. Shutdown is forced if EN is pulled Low with a shutdown current of typically 100 nA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off and the output voltage is actively discharged through the SW pin by a current sink. Therefore VIN must remain present for the discharge to function.

7.4.2 Minimum Duty Cycle and 100% Mode Operation

There is no limitation for small duty cycles because, even at very low duty cycles, the switching frequency is reduced as needed to always make sure of a proper regulation.

If the output voltage (V_{OUT}) comes close to the input voltage (V_{IN}), the device enters 100% mode. While the high-side switch is constantly turned on, the low-side switch is switched off. This action is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The difference between V_{IN} and V_{OUT} is determined by the voltage drop across the high-side FET and the DC resistance of the inductor. The minimum V_{IN} that is needed to maintain a specific V_{OUT} value is estimated as:

$$V_{IN,min} = V_{OUT} + I_{OUT,MAX} \times \left(R_{DS(on)} + R_L\right) \quad (3)$$

where

- $V_{IN,min}$ = Minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ = Maximum output current
- $R_{DS(on)}$ = High-side FET ON-resistance
- R_L = Inductor ohmic resistance (DCR)

7.4.3 Power Good

The TPS62830x has a built-in power-good (PG) function. The PG pin goes high impedance when the output voltage has reached the nominal value. Otherwise, including when disabled, in UVLO or in thermal shutdown, PG is Low (see 表 7-1). The PG function is formed with a window comparator, which has an upper and lower voltage threshold. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 5.5 V.

表 7-1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, V_{FB} ≥ 0.48 V	√	
	EN = High, V_{FB} ≤ 0.56 V		√
	EN = High, V_{FB} ≤ 0.525 V	√	
	EN = High, V_{FB} ≥ 0.55 V		√
Shutdown	EN = Low		√
Thermal shutdown	$T_J > T_{JSD}$		√
UVLO	$0.7\ V < V_{IN} < V_{UVLO}$		√
Power supply removal	$V_{IN} < 0.7$ V	√	

The PG signal can be used for sequencing of multiple rails by connecting the PG signal to the EN pin of other converters. Leave the PG pin unconnected when not used. The PG rising edge and falling edge has a 40 µs blanking time, as shown in 图 7-7. At start-up, the delay of PG signal is typically 125 µs after soft start is finished.

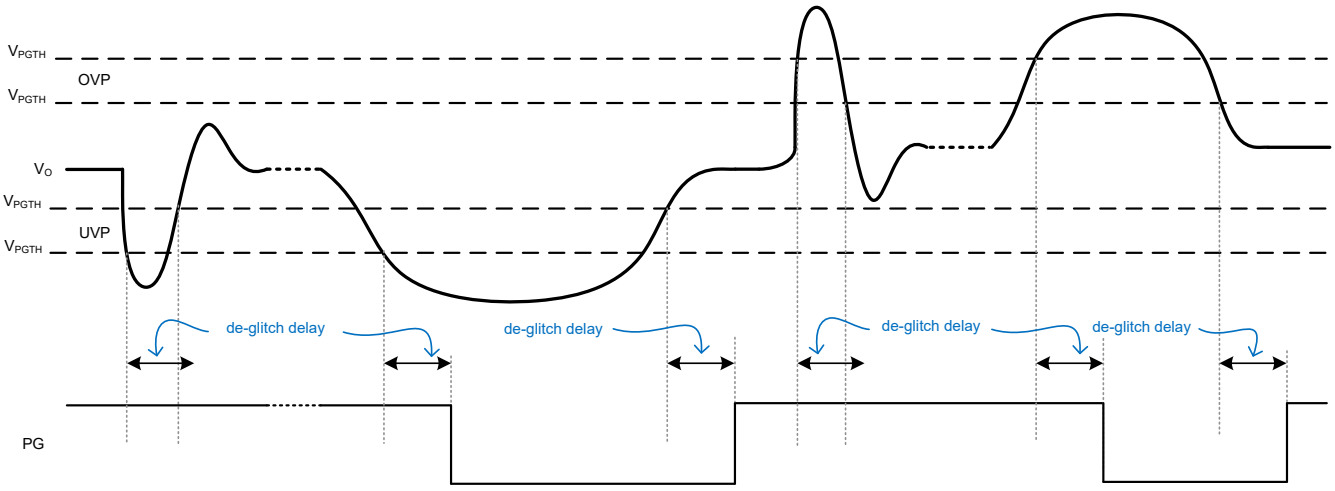


图 7-7. Power-Good Behavior

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

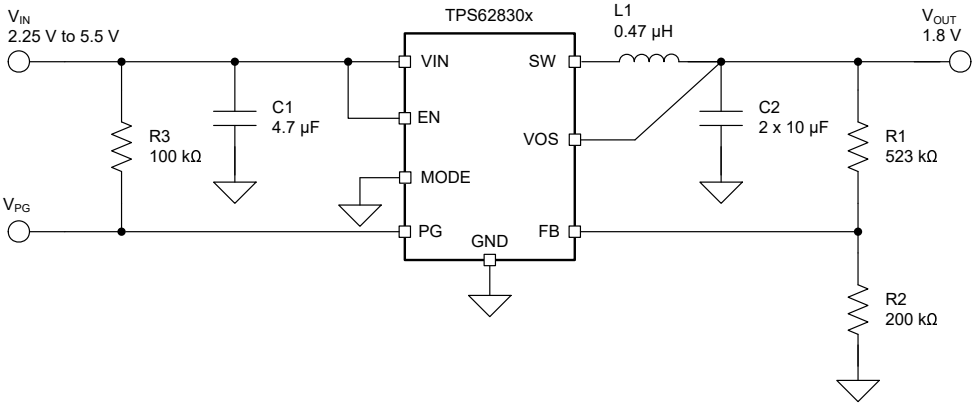


图 8-1. Typical Application of TPS62830x (Optimized for Design Size)

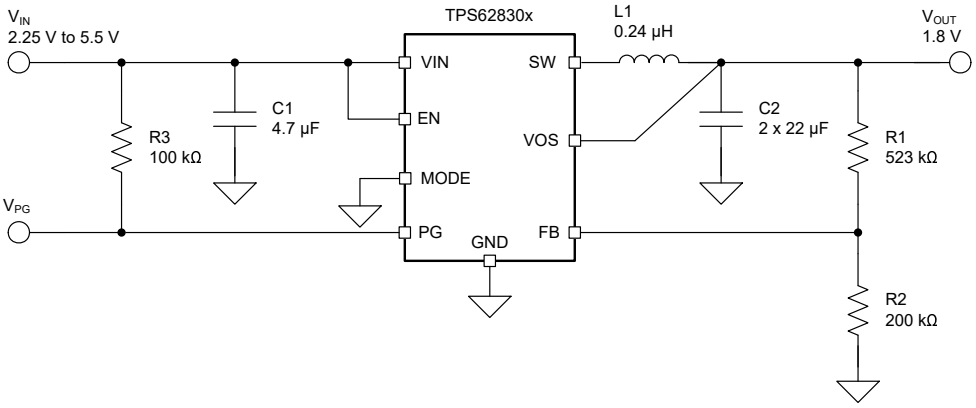


图 8-2. Typical Application of TPS62830x (Optimized for Transient Response)

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.25 V to 5.5 V
Output voltage	1.8 V
Output ripple voltage	< 15 mV

表 8-2 lists the components used for the example.

表 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	4.7 µF, Ceramic capacitor, 6.3 V, X7R, size 0603, JMK107BB7475KA-T	Taiyo Yuden
C2	2 × 10 µF, Ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106KA73D	Murata
L1	0.47 µH, Power inductor, XGL4015-471ME	Coilcraft
R1	Depending on the output voltage, 1%, size 0402	Std
R2	200 kΩ, Chip resistor, 1/16 W, 1%, size 0402	Std
R3	100 kΩ, Chip resistor, 1/16 W, 1%, size 0402	Std

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62830x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to 方程式 4:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.5\,V} - 1\right) \quad (4)$$

R2 can be any value between 200 kΩ and 600 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity.

8.2.2.3 Inductor Selection

The main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 方程式 5 and 方程式 6 are given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2} \quad (5)$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (6)$$

where:

- $I_{OUT,MAX}$ = Maximum output current
- ΔI_L = Inductor current ripple
- f_{SW} = Switching frequency
- L = Inductor value

TI recommends to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size must also be taken into account when selecting an appropriate inductor. Finally, for better transient response performance, TI recommends a smaller inductance value. 表 8-3 lists recommended inductors.

表 8-3. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING [A]	DIMENSIONS [mm]	MAX. DC RESISTANCE [mΩ]	MFR PART NUMBER(1)
0.47	4.4	4.0 × 4.0 × 1.6	7.5	XGL4015-471ME, Coilcraft
	4.8	2.0 × 1.6 × 1.0	22	HTEN20161T-R47MDR, Cyntec
	4.8	2.0 × 1.6 × 1.0	22	CIGT201610EHR47MNE, Samsung
	5.1	2.0 × 1.6 × 1.0	34	TFM201610ALM-R47MTAA, TDK
0.24	4.8	2.0 × 1.25 × 0.8	17	LSCNE2012HKTR24MD, Taiyo Yuden
	4.7	2.0 × 1.6 × 1.0	19	CIGT201610LHR24MNE, Samsung
	4.7	2.0 × 1.6 × 1.0	20	DFE201610E-R24M, MuRata
	3.6	2.0 × 1.6 × 0.8	23	CIGT201608LMR24MNE, Samsung

(1) See the *Third-party Products Disclaimer*.

8.2.2.4 Output Capacitor Selection

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, 表 8-5 outlines possible inductor and capacitor value combinations for most applications. Cells with the (✓) mark represent combinations that are proven for stability by simulation and lab test. additionally, cells with the (+) mark represent combinations that are proven for stability by simulation only. Check further combinations for each individual application.

The DCS-Control scheme of the TPS62830x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. To keep low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple. Considering the DC-bias derating the capacitance, the recommended minimum effective output capacitance is 12 µF when using a 0.47-µH or larger inductor. When using a 0.24-µH or lower inductor, the recommended minimum effective output capacitance is 22 µF. 表 8-6 lists recommended capacitors.

表 8-4. Matrix of Output Capacitor and Inductor Combinations (TPS628301 and TPS628302)

V_{OUT} [V]	NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)		
		2 × 10 or 22	2 × 22 or 47	100
$0.5 \leqslant V_{OUT} \leqslant 1.8$	0.47	✓ (1)	✓	+
	1.0	+	+	
$1.8 < V_{OUT}$	0.47		✓ (1)	+
	1.0	+	+	

表 8-5. Matrix of Output Capacitor and Inductor Combinations (TPS628303 and TPS628304)

V_{OUT} [V]	NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)		
		2 × 10 or 22	2 × 22 or 47	100
$0.5 \leqslant V_{OUT} \leqslant 1.8$	0.47	✓ (1)	✓	+
	0.24	+	✓	+
$1.8 < V_{OUT}$	0.47		✓ (1)	+
	0.24		✓	+

(1) This LC combination is the standard value and recommended for most applications.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.

表 8-6. List of Recommended Capacitors

NOMINAL CAPACITANCE [µF]	VOLTAGE RATING [V]	DIMENSIONS [mm]	MFR PART NUMBER(1)
10	6.3	2.0 × 1.5 × 1.25	MSASJ21GAB7106MTNA01, Taiyo Yuden
10	10	2.0 × 1.25 × 1.25	C2012X7R1A106K125AC, TDK
10	10	1.6 × 0.8 × 0.8	GRM188Z71A106KA73#, MuRata
10	10	1.6 × 0.8 × 0.8	C1608X5R1A106K080AC, TDK
22	10	2.0 × 1.25 × 1.25	GRM21BZ71A226ME15#, MuRata
22	10	1.6 × 0.8 × 0.8	C1608X5R1A226M080AC, TDK

8.2.2.5 Input Capacitor Selection

The input capacitor is the low-impedance energy source for the converter, which helps provide stable operation. Because the buck converter has a pulsating input current, a low ESR ceramic input capacitor is required for best input voltage filtering to minimize input voltage spikes. Place the capacitor between VIN and GND pins and as close as possible to those pins.

For most applications, a minimum effective input capacitance of 3 µF is sufficient, though a larger value reduces input current ripple and is recommended. When operating from a high impedance source, TI recommends a larger input buffer capacitor ⩾10 µF to avoid voltage drops during start-up and load transients. Additionally, small de-coupling capacitors can also be used in case of noise at the input if the device. The input capacitor can be increased without any limit for better input voltage filtering.

表 8-7 shows a list of recommended capacitors.

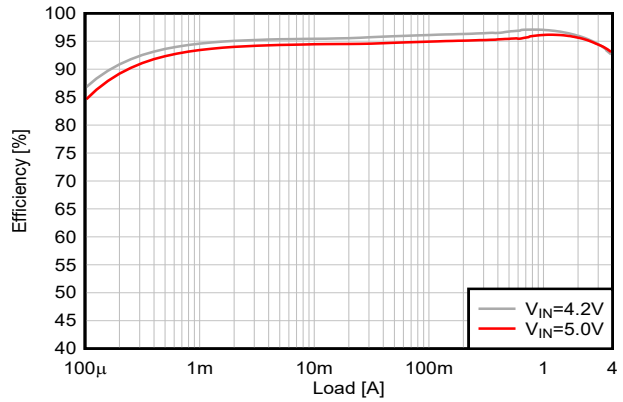
表 8-7. List of Recommended Capacitors

NOMINAL CAPACITANCE [µF]	VOLTAGE RATING [V]	DIMENSIONS [mm]	MFR PART NUMBER(1)
4.7	6.3	1.6 × 0.8 × 0.8	MSASJ168BB7475MTNA01, Taiyo Yuden
4.7	10	2.0 × 1.25 × 1.25	C2012X7R1A475K125AC, TDK
10	10	1.6 × 0.8 × 0.8	GRM188Z71A106KA73#, MuRata

(1) See the *Third-party Products Disclaimer*

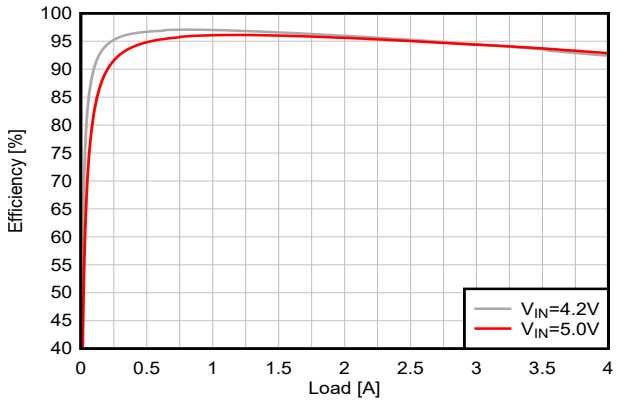
8.2.3 Application Curves

T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.8 V, BOM = 表 8-2 unless otherwise noted.



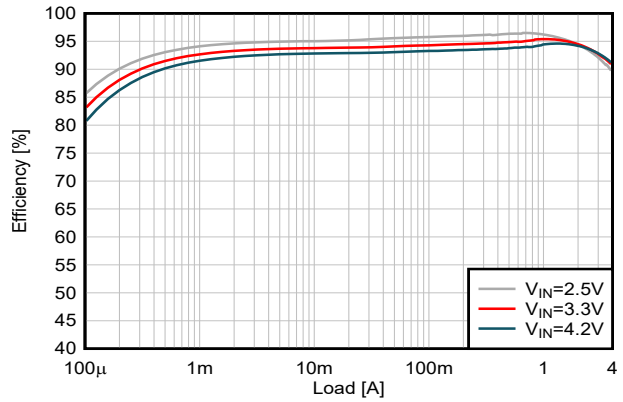
V_{OUT} = 3.3 V PFM

图 8-3. Efficiency versus Output Current



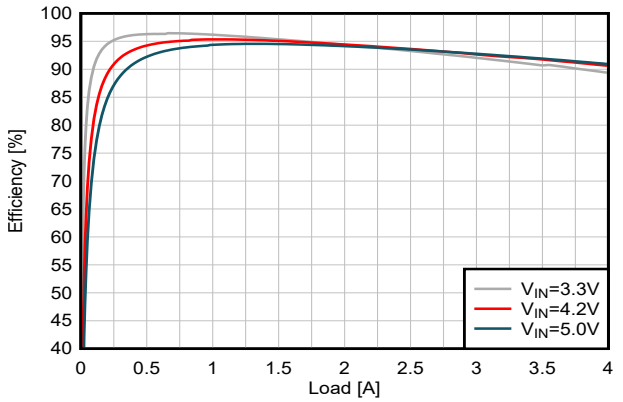
V_{OUT} = 3.3 V PWM

图 8-4. Efficiency versus Output Current



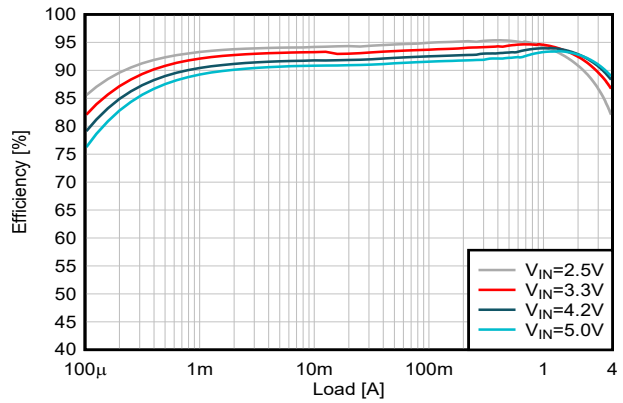
V_{OUT} = 2.5 V PFM

图 8-5. Efficiency versus Output Current



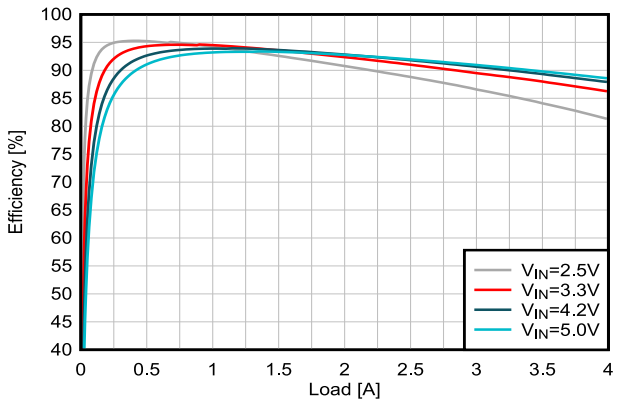
V_{OUT} = 2.5 V PWM

图 8-6. Efficiency versus Output Current



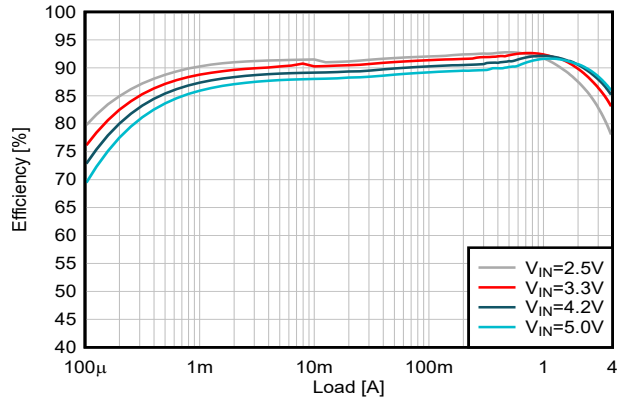
V_{OUT} = 1.8 V PFM

图 8-7. Efficiency versus Output Current



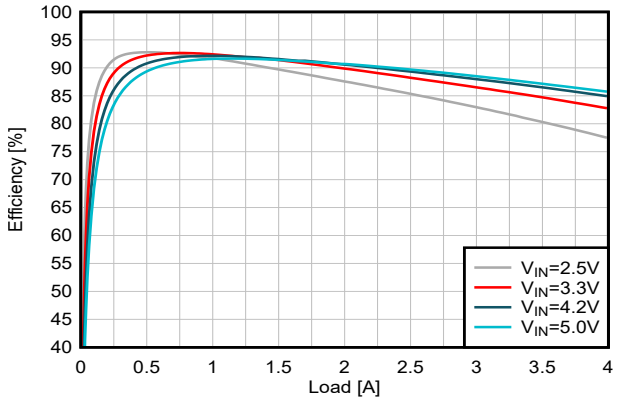
V_{OUT} = 1.8 V PWM

图 8-8. Efficiency versus Output Current



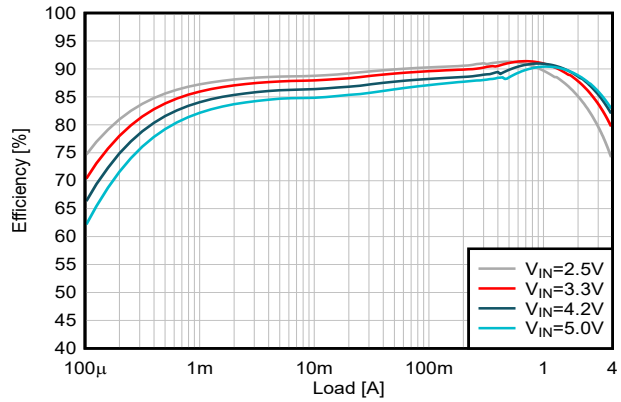
V_{OUT} = 1.2 V PFM

图 8-9. Efficiency versus Output Current



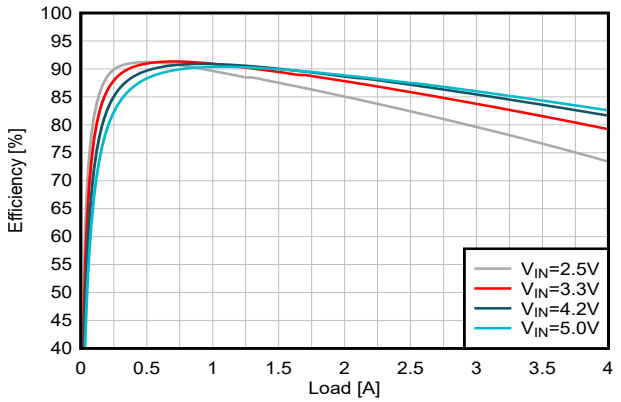
V_{OUT} = 1.2 V PWM

图 8-10. Efficiency versus Output Current



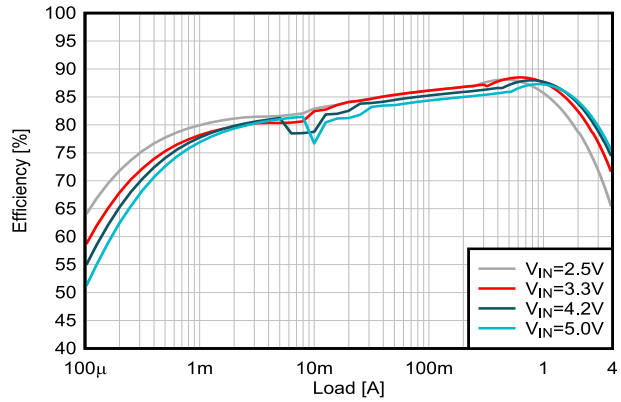
V_{OUT} = 0.9 V PFM

图 8-11. Efficiency versus Output Current



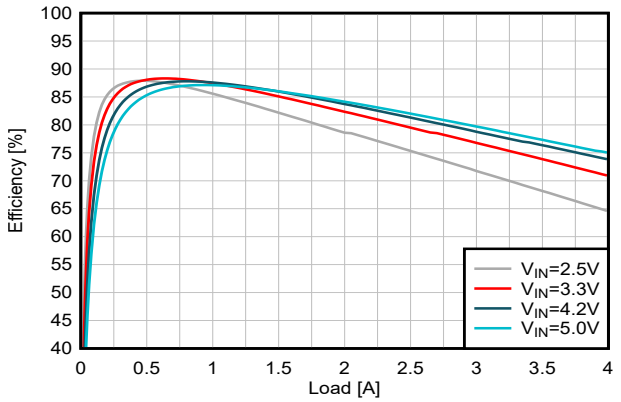
V_{OUT} = 0.9 V PWM

图 8-12. Efficiency versus Output Current



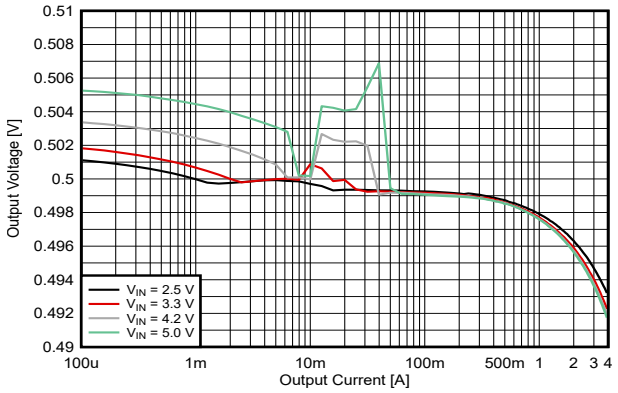
V_{OUT} = 0.5 V PFM T_A = 25 °C

图 8-13. Efficiency versus Output Current



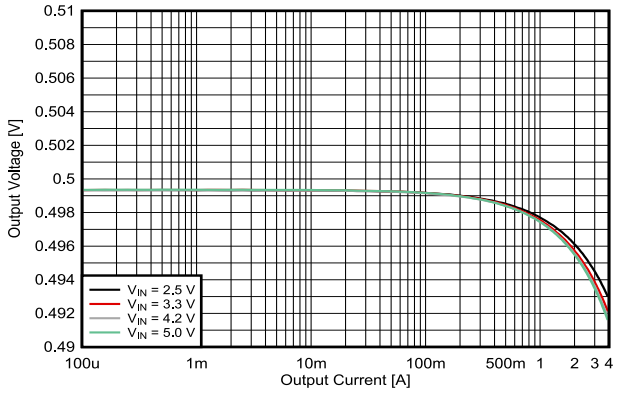
V_{OUT} = 0.5 V PWM T_A = 25 °C

图 8-14. Efficiency versus Output Current



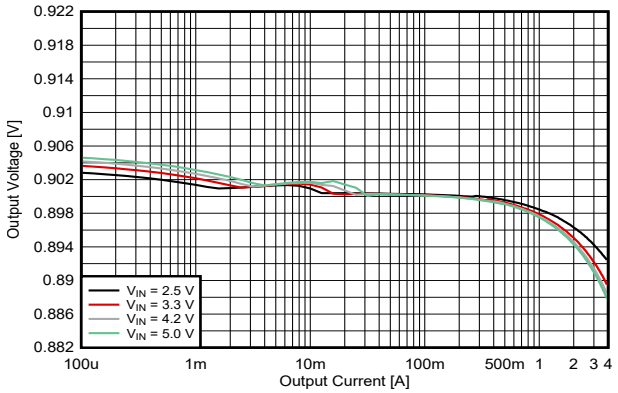
V_{OUT} = 0.5 V PFM

图 8-15. Output Voltage versus Output Current



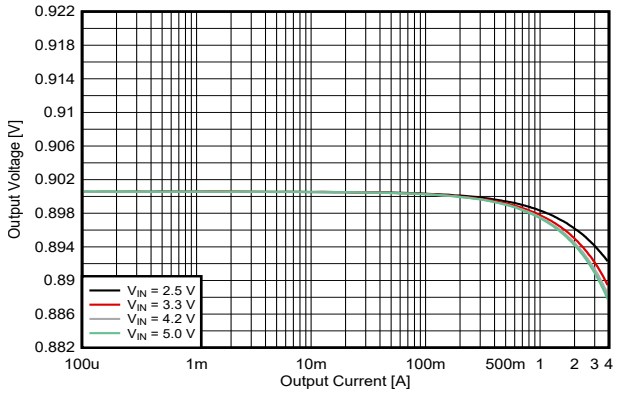
V_{OUT} = 0.5 V PWM

图 8-16. Output Voltage versus Output Current



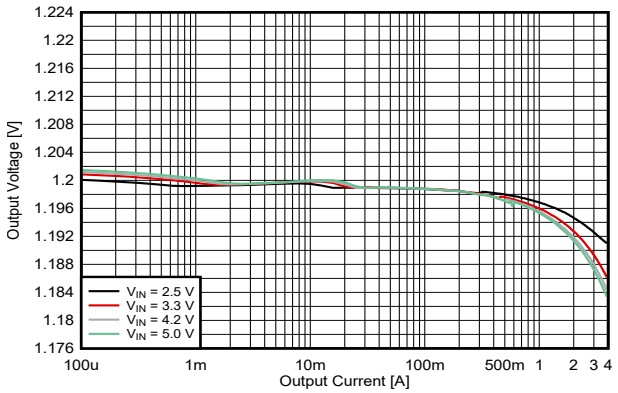
V_{OUT} = 0.9 V PFM

图 8-17. Output Voltage versus Output Current



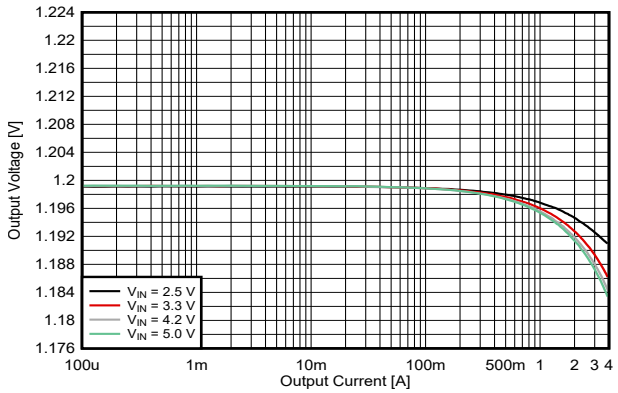
V_{OUT} = 0.9 V PWM

图 8-18. Output Voltage versus Output Current



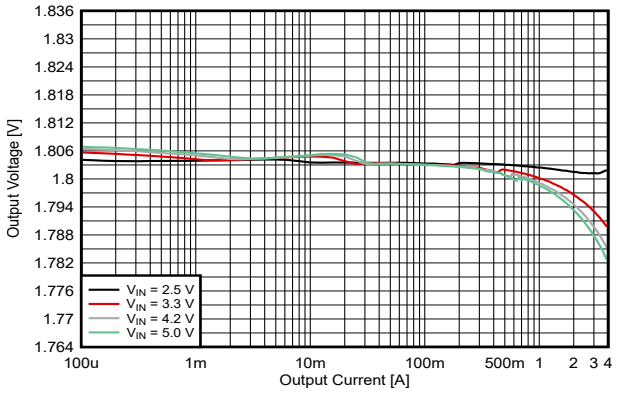
V_{OUT} = 1.2 V PFM

图 8-19. Output Voltage versus Output Current



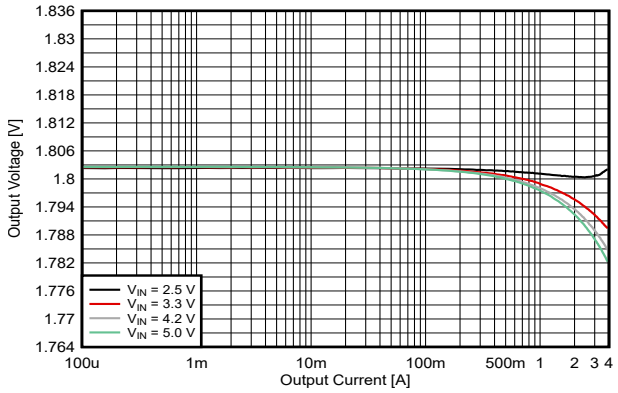
V_{OUT} = 1.2 V PWM

图 8-20. Output Voltage versus Output Current



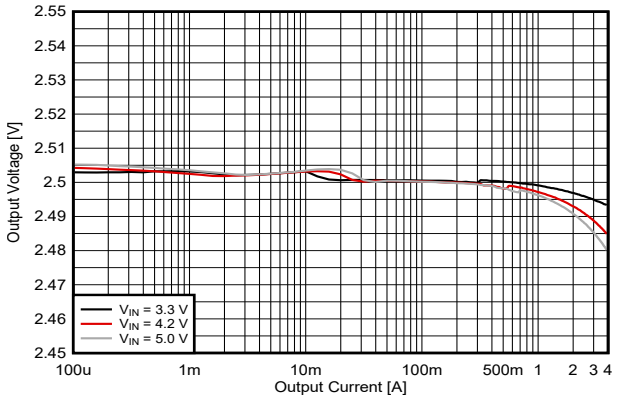
V_{OUT} = 1.8 V PFM

图 8-21. Output Voltage versus Output Current



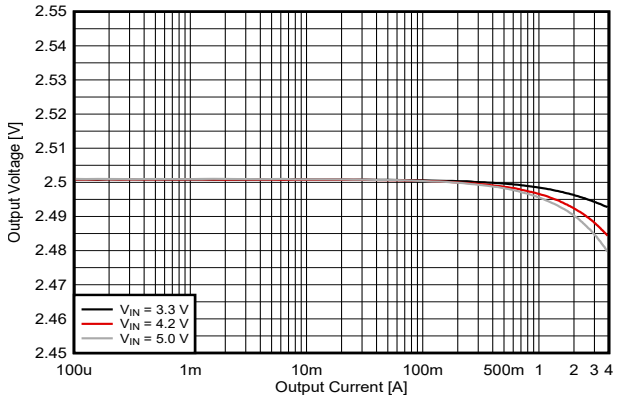
V_{OUT} = 1.8 V PWM

图 8-22. Output Voltage versus Output Current



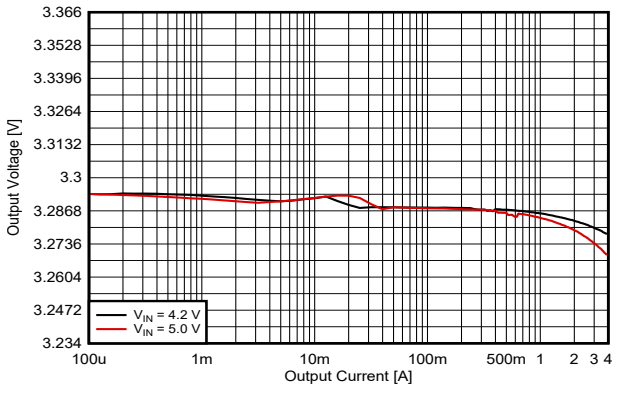
V_{OUT} = 2.5 V PFM

图 8-23. Output Voltage versus Output Current



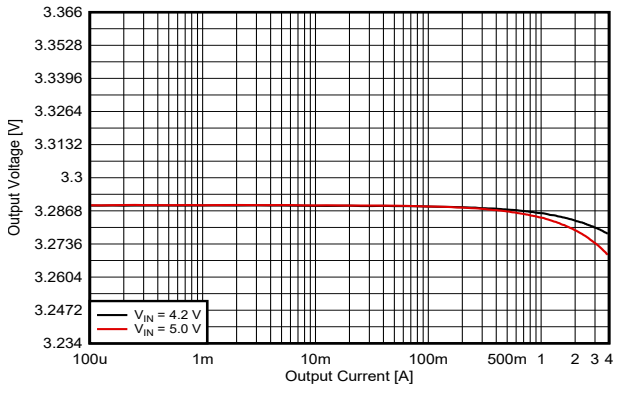
V_{OUT} = 2.5 V PWM

图 8-24. Output Voltage versus Output Current



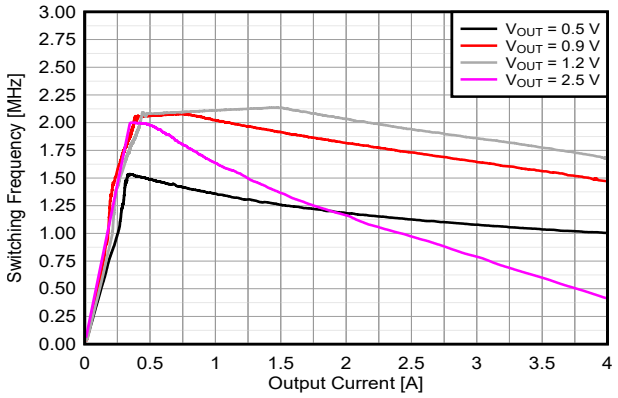
V_{OUT} = 3.3 V PFM

图 8-25. Output Voltage versus Output Current



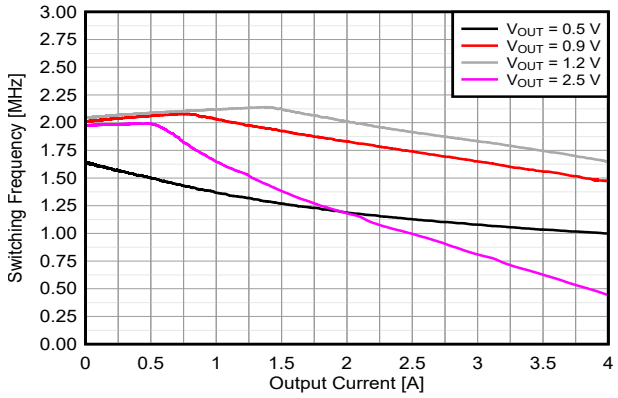
V_{OUT} = 3.3 V PWM

图 8-26. Output Voltage versus Output Current



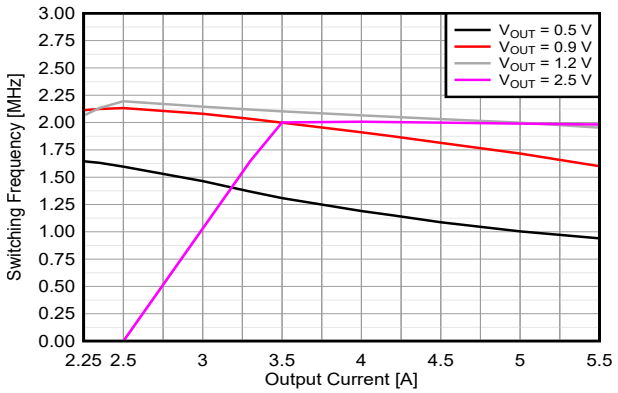
V_{IN} = 3.3 V PFM

图 8-27. Switching Frequency versus Output Current



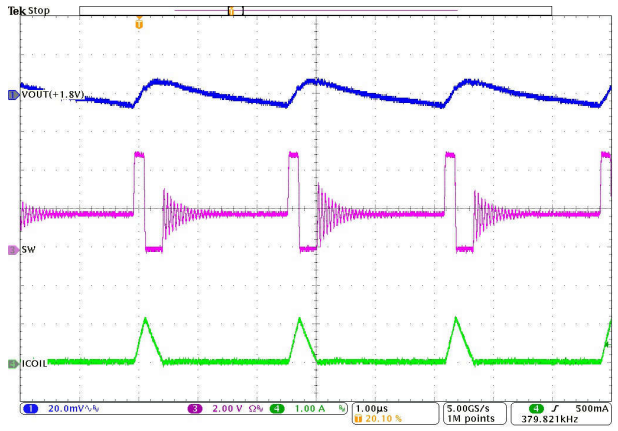
V_{IN} = 3.3 V PWM

图 8-28. Switching Frequency versus Output Current



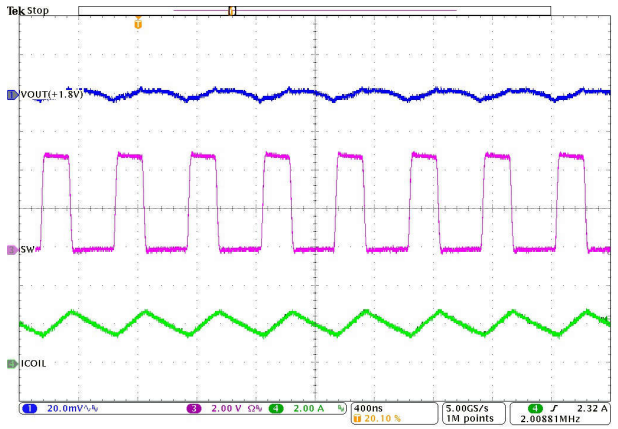
I_{OUT} = 1 A

图 8-29. Switching Frequency versus Input Voltage



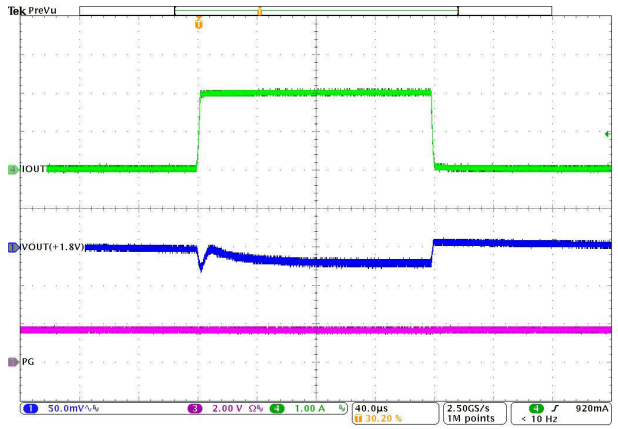
I_{OUT}= 100 mA PFM

图 8-30. Output Voltage Ripple



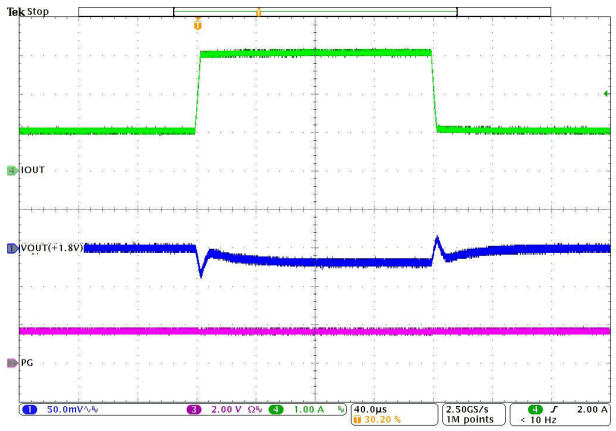
I_{OUT} = 2.0 A PFM or PWM

图 8-31. Output Voltage Ripple



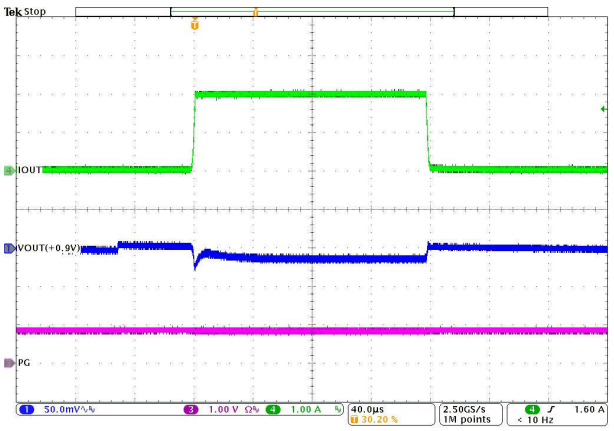
I_{OUT} = 1 mA to 2 A PFM Slew rate = 1 A/ µ s

图 8-32. Load Transient



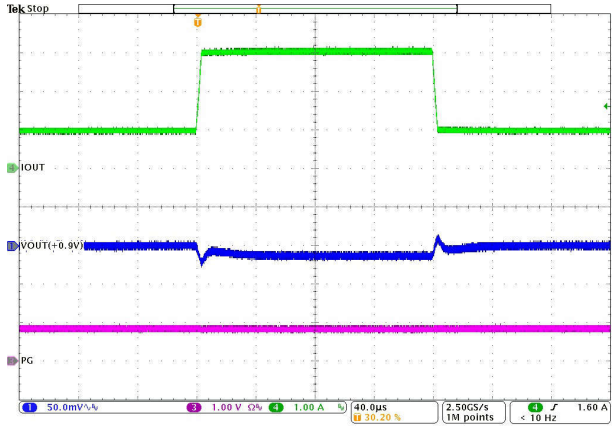
I_{OUT} = 1 A to 3 A　　PWM　　Slew rate = 1 A/ µ s

图 8-33. Load Transient



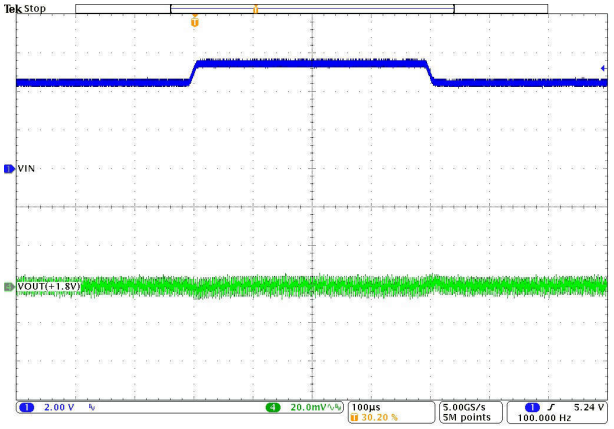
V_{IN} = 3.3 V
V_{OUT} = 0.9 V　　PFM
Transient BoM　　I_{OUT} = 1 mA to 2A
Slew rate = 1 A/ µ s

图 8-34. Load Transient



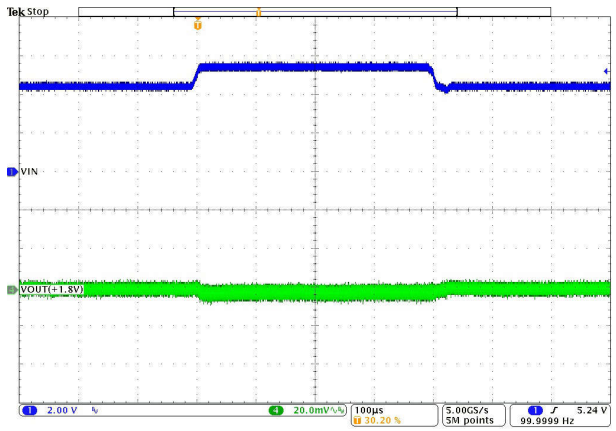
V_{IN} = 3.3 V
V_{OUT} = 0.9 V　　PWM
Transient BoM　　I_{OUT} = 1 A to 3 A
Slew rate = 1 A/ µ s

图 8-35. Load Transient



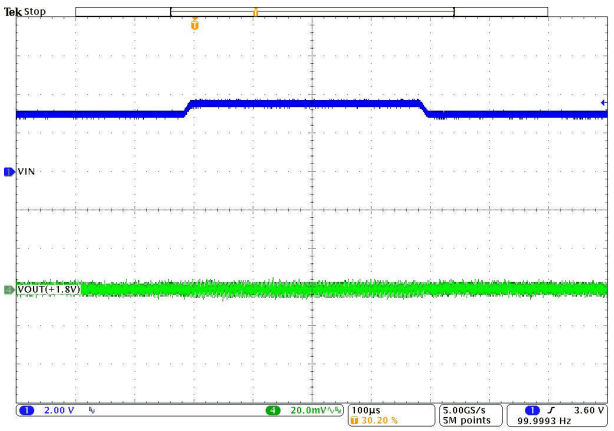
V_{IN} = 4.5 V to 5.5 V　　PFM　　I_{OUT} = 100 mA

图 8-36. Line Transient



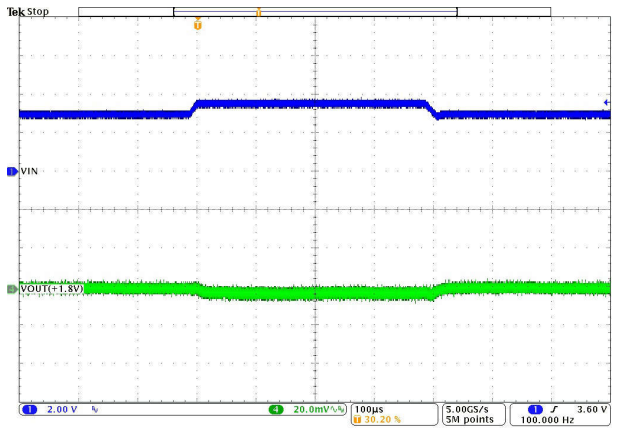
V_{IN} = 4.5 V to 5.5 V　　PWM　　I_{OUT} = 2.0 A

图 8-37. Line Transient



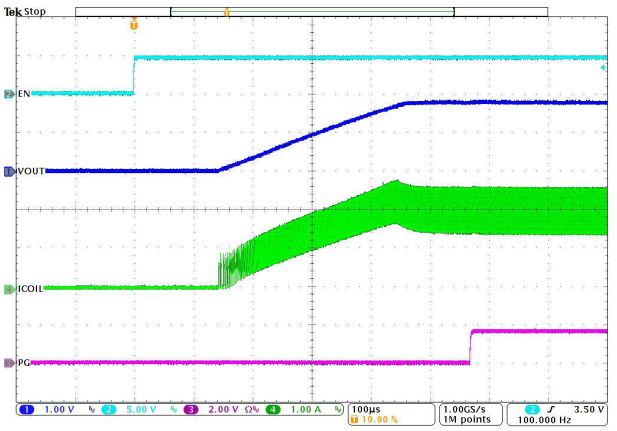
V_{IN} = 3.0 V to 3.6 V　　PFM　　I_{OUT} = 100 mA

图 8-38. Line Transient



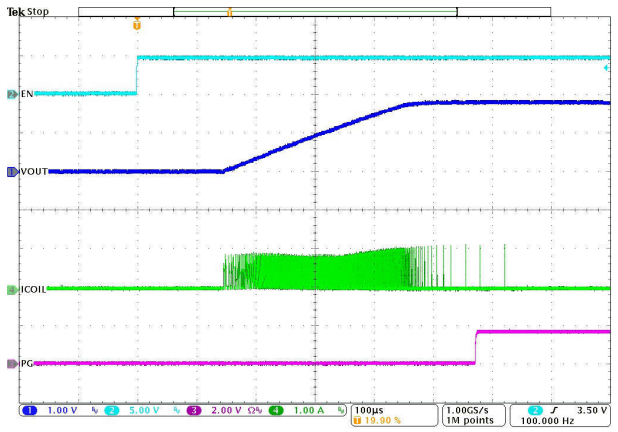
V_{IN} = 3.0 V to 3.6 V PWM I_{OUT} = 2.0 A

图 8-39. Line Transient



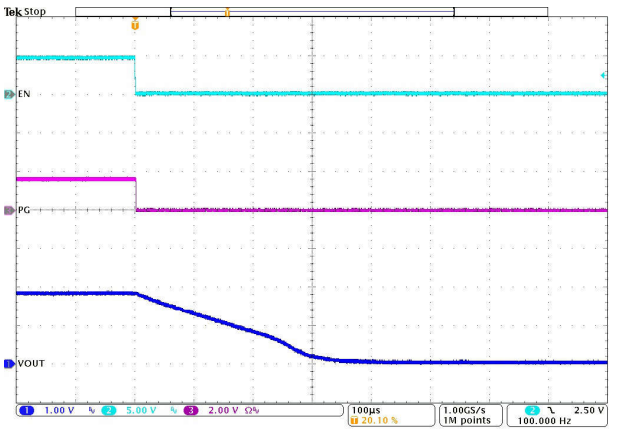
I_{OUT} = 2.0 A PFM or PWM 'A' and 'B' versions T_A = 25 °C

图 8-40. Start-Up With Load



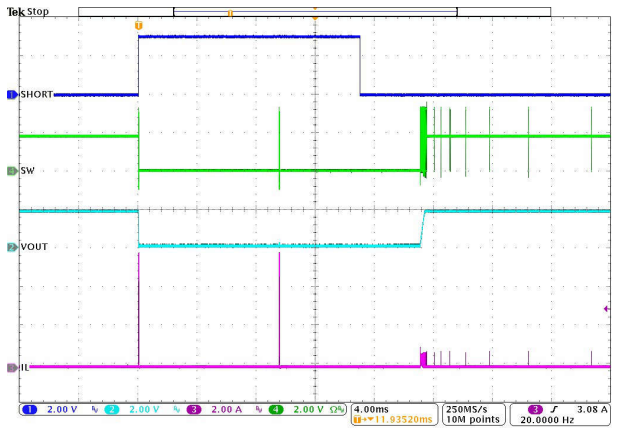
I_{OUT} = 0 mA PFM or PWM 'A' and 'B' versions T_A = 25 °C

图 8-41. Start-Up With No Load



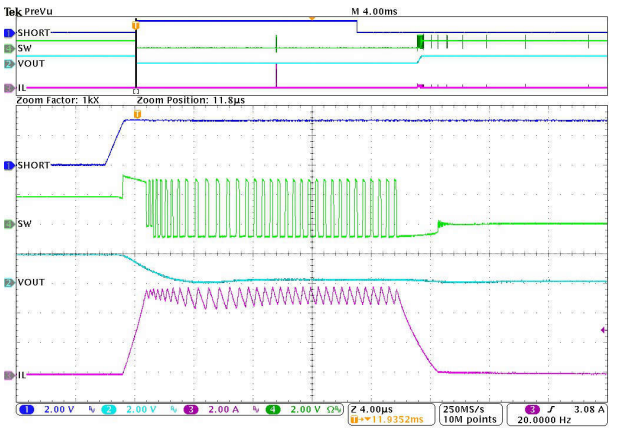
I_{OUT} = 0 mA PFM T_A = 25 °C

图 8-42. Disable, Active Output Discharge at No Load



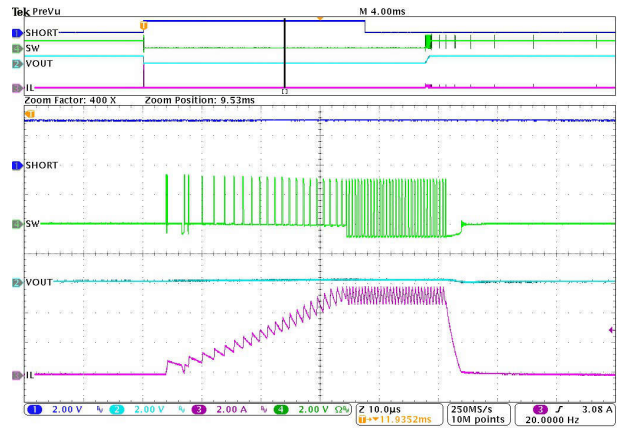
PFM or PWM T_A = 25 °C

图 8-43. HICCUP Short-Circuit Protection



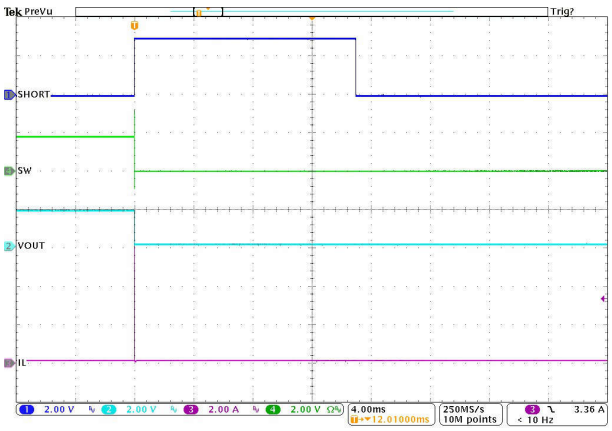
PFM or PWM T_A = 25 °C

图 8-44. HICCUP Short-Circuit Protection (Zoom In)



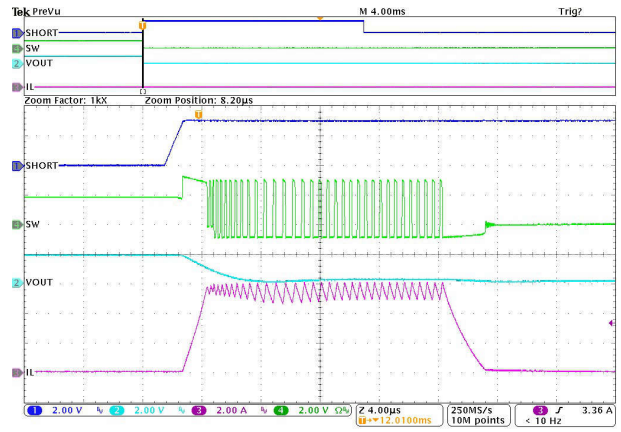
PFM or PWM T_A = 25 °C

图 8-45. HICCUP Short-Circuit Protection (Zoom In - Second Hiccup)



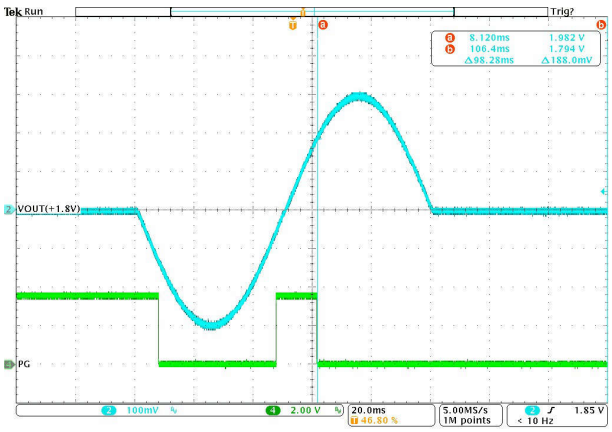
PFM or PWM TPS628303BDRL T_A = 25 °C

图 8-46. Latch-off Short-Circuit Protection



PFM or PWM TPS628303BDRL T_A = 25 °C

图 8-47. Latch-off Short-Circuit Protection (Zoom In)



PFM or PWM TPS628303BDRLR T_A = 25 °C

图 8-48. Latch-off Overvoltage Protection

8.3 Power Supply Recommendations

The TPS62830x family does not have special requirements for the input power supply and is designed to operate from an input voltage supply range from 2.25 V to 5.5 V. The output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the device.

8.4 Layout

8.4.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device. See *Layout Example* for the recommended low EMI PCB layout.

- Place the input and output capacitors and the inductor as close as possible to the IC. This action keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- Connect the low side of the input and output capacitors properly to the GND pin to avoid a ground potential shift.

- Take special care to avoid noise being induced. The sense traces connected to FB is a signal trace. Keep these traces away from SW nodes. The connection of the output voltage trace for the FB resistors must be made at the output capacitor.
- Refer to *Layout Example* for an example of component placement, routing, and thermal design with good EMI performance.

8.4.2 Layout Example

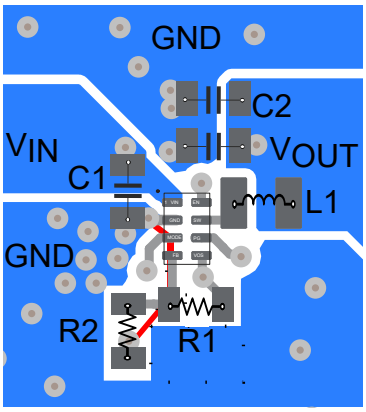


图 8-49. PCB Layout Recommendation (RZE Package)

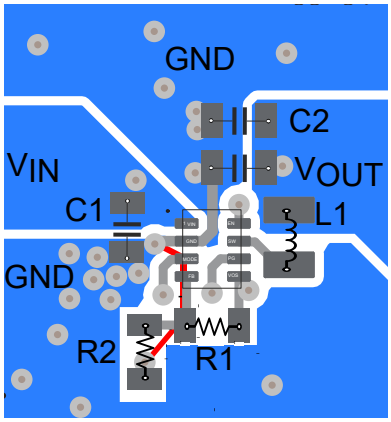


图 8-50. PCB Layout Recommendation (DRL Package)

8.4.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The Thermal Data section in *Thermal Information* provides the thermal metric of the device on the EVM after considering the PCB design of real applications. The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see the Thermal Characteristics application notes, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

9 Device and Documentation Support

9.1 Device Support

9.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62830x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

Changes from Revision A (October 2023) to Revision B (March 2024)	Page
• 在整个数据表中添加了新的可订购器件型号信息	1

Changes from Revision * (February 2023) to Revision A (October 2023)	Page
• 将文档状态从“预告信息”更改为“量产数据”	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS628301ADRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	01A
TPS628301ADRLR.A	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	01A
TPS628301ARZER	Active	Production	WQFN-HR (RZE) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	01A
TPS628301ARZER.A	Active	Production	WQFN-HR (RZE) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	01A
TPS628301KRZER	Active	Production	WQFN-HR (RZE) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	01K
TPS628302ADRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	02A
TPS628302ADRLR.A	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	02A
TPS628302ARZER	Active	Production	WQFN-HR (RZE) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	02A
TPS628302ARZER.A	Active	Production	WQFN-HR (RZE) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	02A
TPS628302KRZER	Active	Production	WQFN-HR (RZE) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	02K
TPS628303ADRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	03A
TPS628303ADRLR.A	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	03A
TPS628303ARZER	Active	Production	WQFN-HR (RZE) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	03A
TPS628303ARZER.A	Active	Production	WQFN-HR (RZE) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	03A
TPS628303BDRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	03B
TPS628303BDRLR.A	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	03B
TPS628303KRZER	Active	Production	WQFN-HR (RZE) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	03K
TPS628304ADRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	04A
TPS628304ADRLR.A	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	04A
TPS628304ARZER	Active	Production	WQFN-HR (RZE) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	04A
TPS628304ARZER.A	Active	Production	WQFN-HR (RZE) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	04A
TPS628304KRZER	Active	Production	WQFN-HR (RZE) | 8	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	04K

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

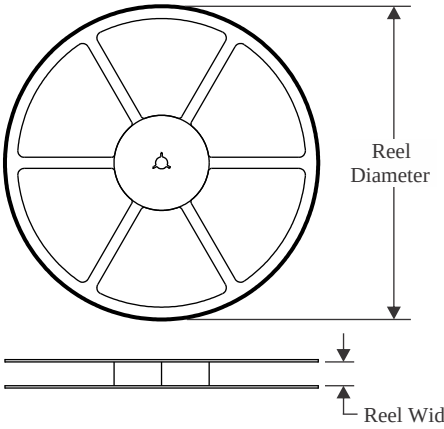
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

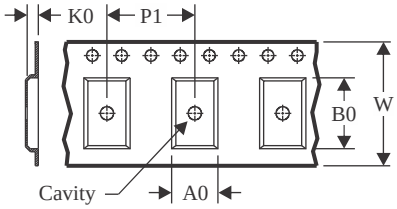
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

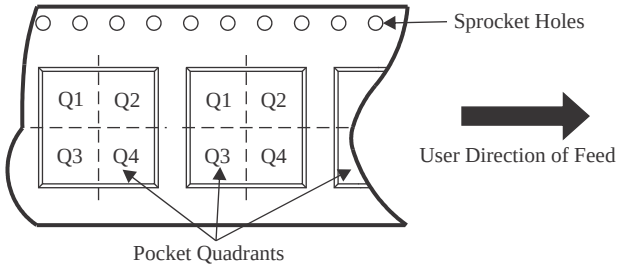


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

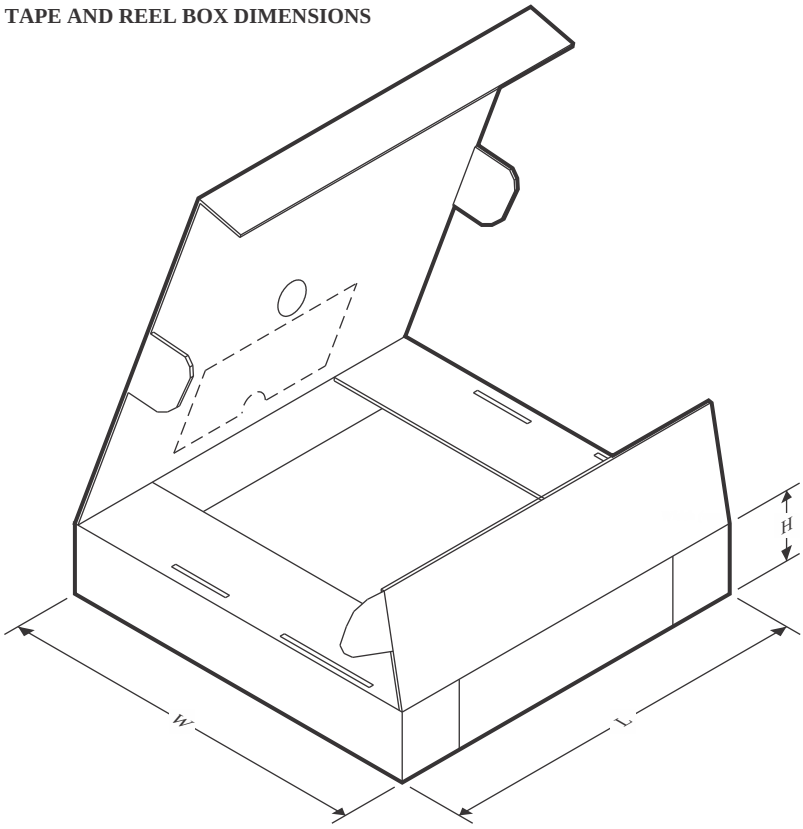


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS628301ADRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS628301ARZER	WQFN-HR	RZE	8	3000	180.0	8.4	1.3	2.3	0.9	4.0	8.0	Q1
TPS628301KRZER	WQFN-HR	RZE	8	3000	180.0	8.4	1.3	2.3	0.9	4.0	8.0	Q1
TPS628302ADRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS628302ARZER	WQFN-HR	RZE	8	3000	180.0	8.4	1.3	2.3	0.9	4.0	8.0	Q1
TPS628302KRZER	WQFN-HR	RZE	8	3000	180.0	8.4	1.3	2.3	0.9	4.0	8.0	Q1
TPS628303ADRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS628303ARZER	WQFN-HR	RZE	8	3000	180.0	8.4	1.3	2.3	0.9	4.0	8.0	Q1
TPS628303BDRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS628303KRZER	WQFN-HR	RZE	8	3000	180.0	8.4	1.3	2.3	0.9	4.0	8.0	Q1
TPS628304ADRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS628304ARZER	WQFN-HR	RZE	8	3000	180.0	8.4	1.3	2.3	0.9	4.0	8.0	Q1
TPS628304KRZER	WQFN-HR	RZE	8	3000	180.0	8.4	1.3	2.3	0.9	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

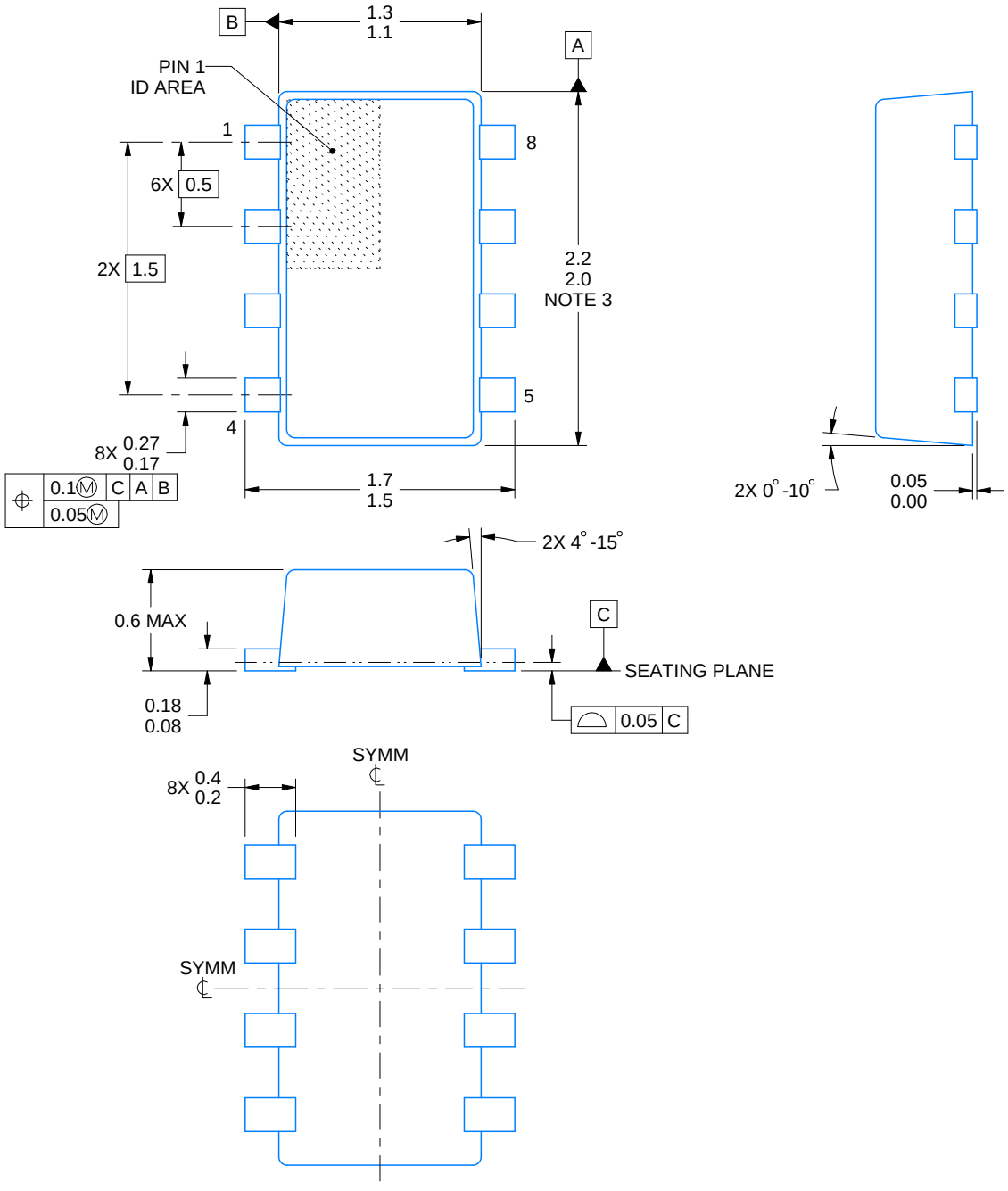
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS628301ADRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS628301ARZER	WQFN-HR	RZE	8	3000	210.0	185.0	35.0
TPS628301KRZER	WQFN-HR	RZE	8	3000	210.0	185.0	35.0
TPS628302ADRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS628302ARZER	WQFN-HR	RZE	8	3000	210.0	185.0	35.0
TPS628302KRZER	WQFN-HR	RZE	8	3000	210.0	185.0	35.0
TPS628303ADRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS628303ARZER	WQFN-HR	RZE	8	3000	210.0	185.0	35.0
TPS628303BDRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS628303KRZER	WQFN-HR	RZE	8	3000	210.0	185.0	35.0
TPS628304ADRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS628304ARZER	WQFN-HR	RZE	8	3000	210.0	185.0	35.0
TPS628304KRZER	WQFN-HR	RZE	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



4224486/G 11/2024

NOTES:

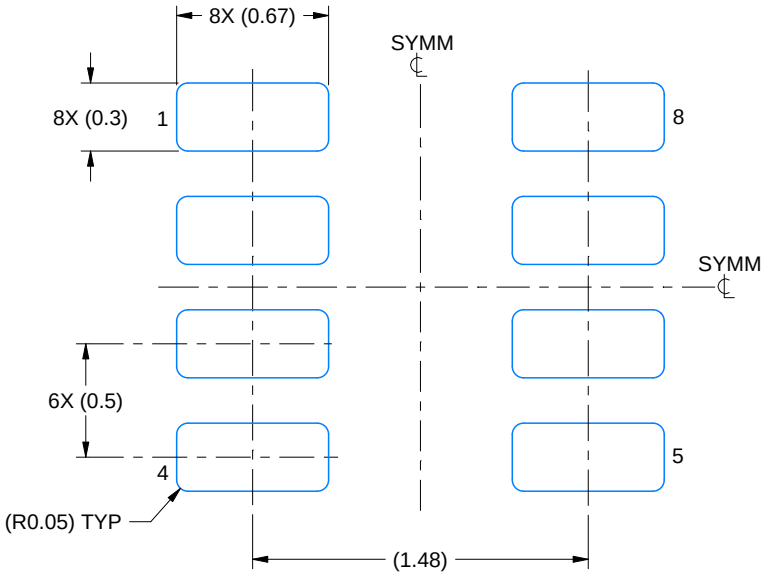
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

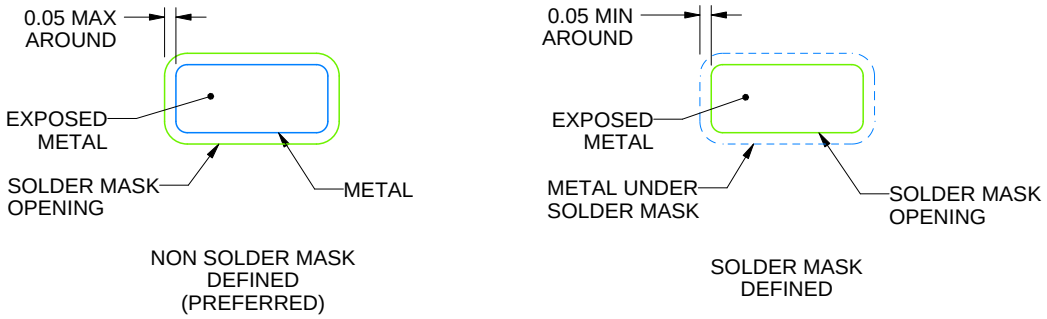
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

4224486/G 11/2024

NOTES: (continued)

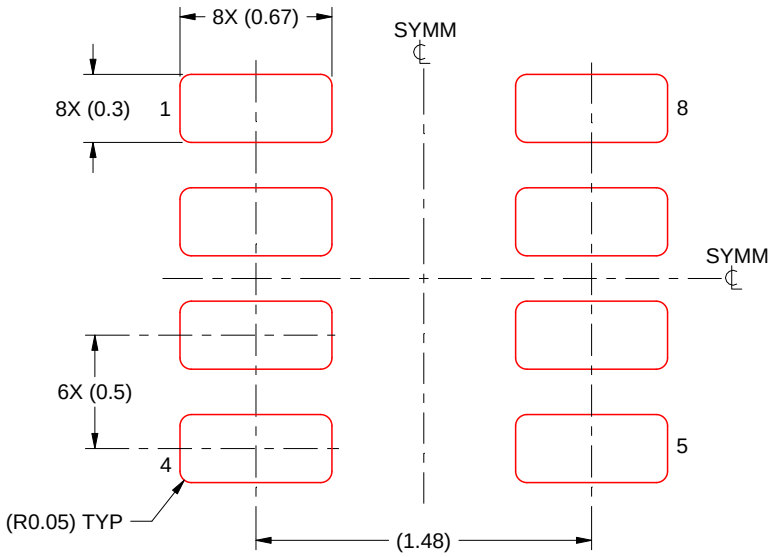
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/G 11/2024

NOTES: (continued)

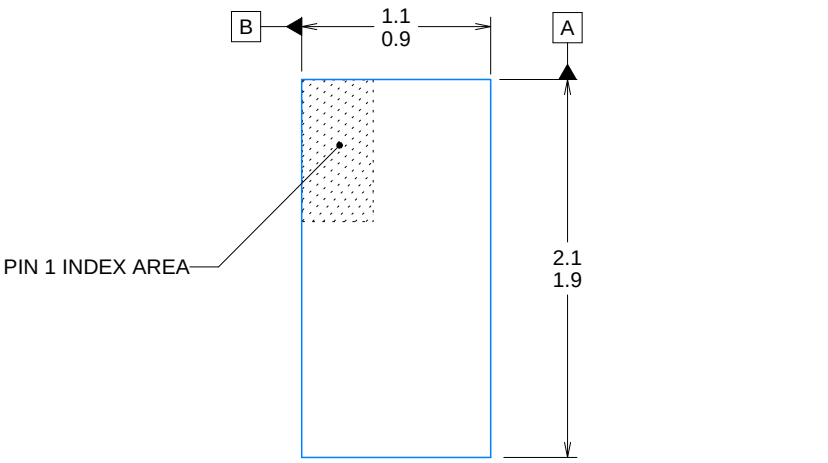
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

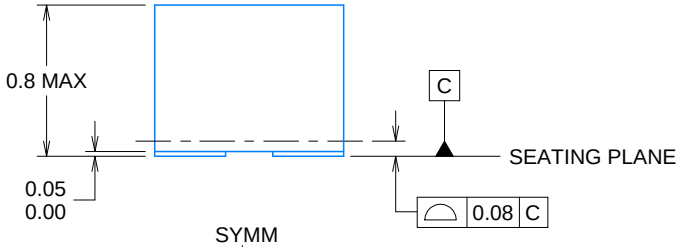
PACKAGE OUTLINE

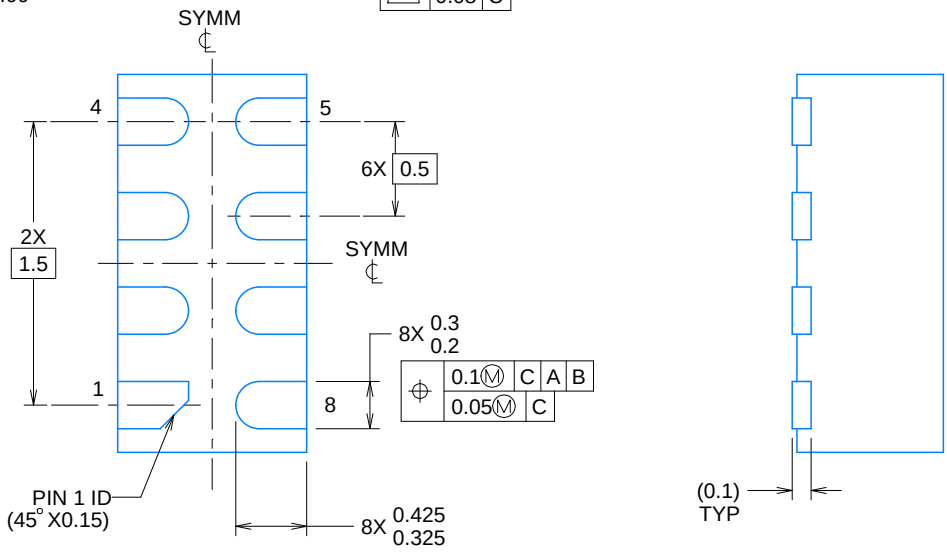
RZE0008A

WQFN-HR - 0.8mm max height

QFN (PLASTIC QUAD FLATPACK - NO LEAD)





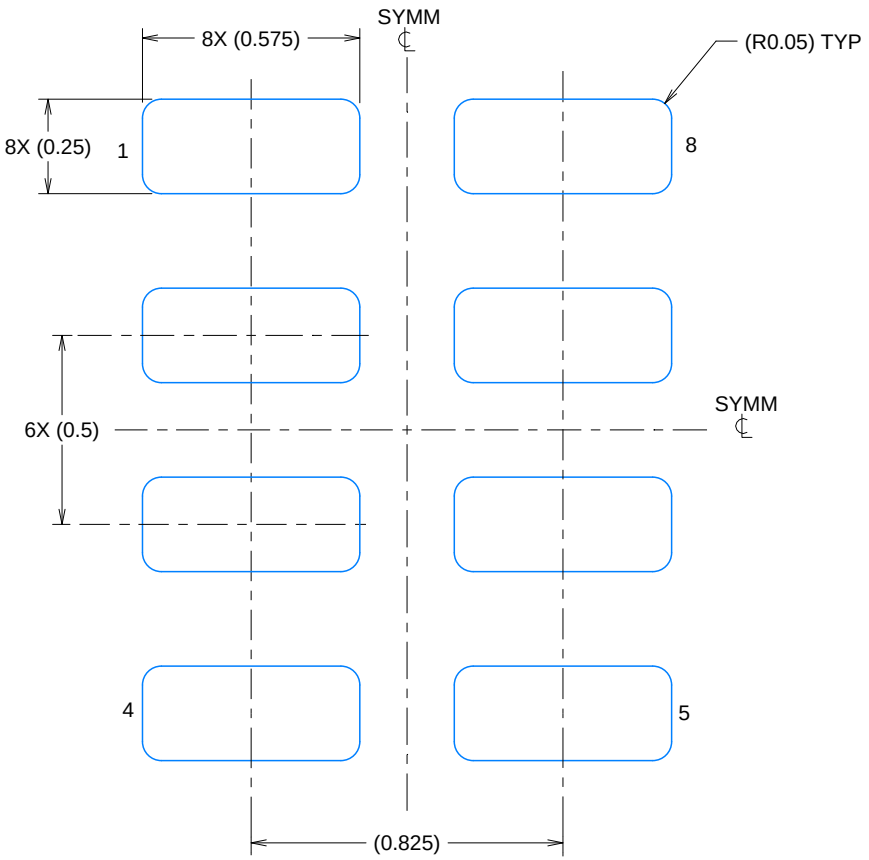


4228328/A 12/2021

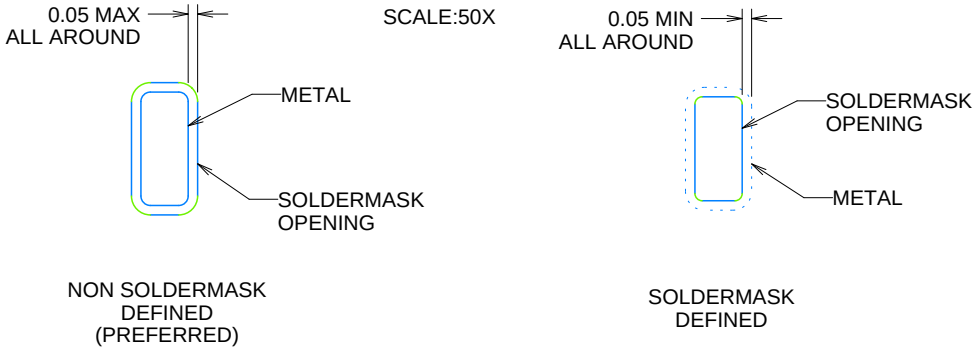
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:50X



SOLDERMASK DETAILS

4228328/A 12/2021

NOTES: (continued)

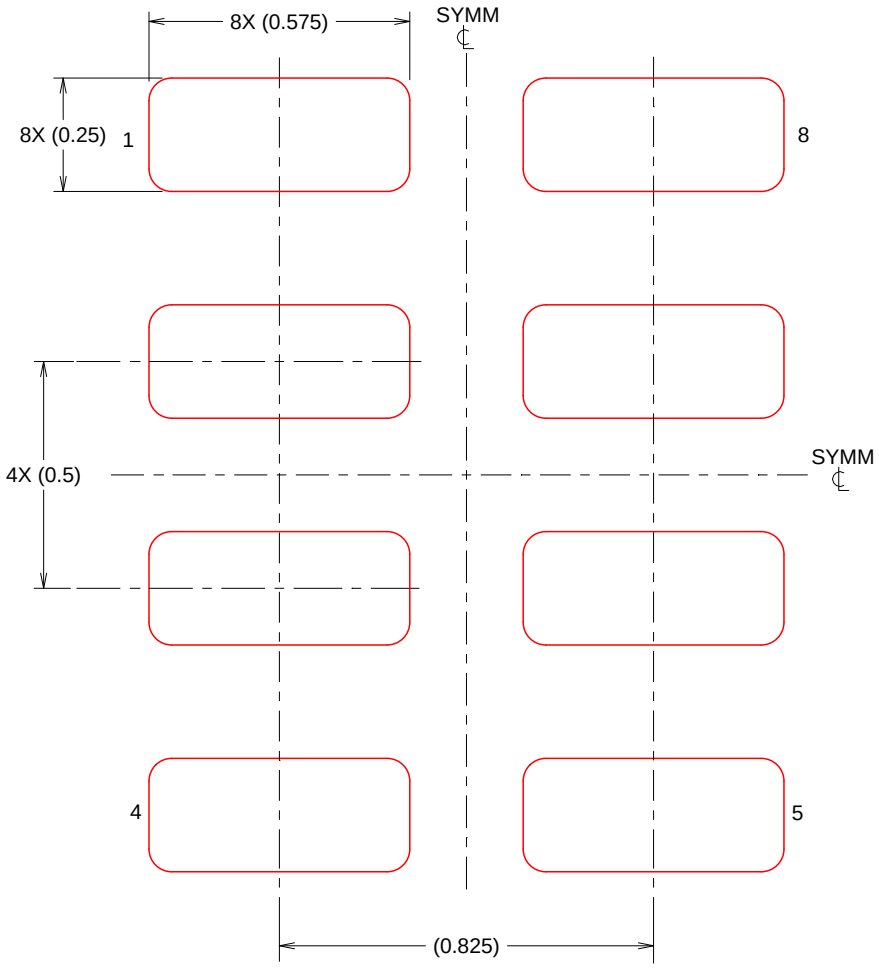
3. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RZE0008A

WQFN-HR - 0.8mm max height

QFN (PLASTIC QUAD FLATPACK - NO LEAD)



SOLDERPASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

SCALE:60X

4228328/A 12/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

最后更新日期：2025 年 10 月