LCD Bias Solution for Monitors

Check for Samples: TPS65149

FEATURES

- **3 V to 6 V Input Voltage Range**
- **Boost Converter With 4 A Switch Current Limit**
- **Boost Converter Output Voltages up to 18 V**
- **Boost Converter Overvoltage Protection**
- **Selectable Switching Frequency (640 kHz or 1.2 MHz)**
- **Programmable Boost Converter Soft-Start**
- **Temperature-Compensated Positive Charge Pump Controller**
- **Negative Charge Pump Controller**
- **Eight Channel Level Shifter**
- **Two Panel Discharge Signals**
- **$\overline{\text{XAO}}$ Reset Signal**
- **Digitally Programmable V_{COM} Buffer**
- **Thermal Shutdown**
- **56-Pin 7×7 mm QFN Package**

APPLICATIONS

- **LCD Monitors using ASG/GIP Technology**

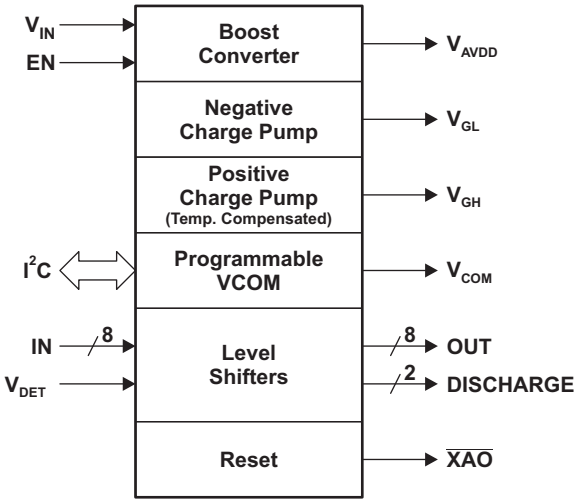
DESCRIPTION

The TPS65149 provides a highly integrated LCD bias solution, primarily intended for monitor applications using ASG/GIP technology.

The device integrates a boost converter to generate the source driver supply voltage (V_{AVDD}), positive and negative charge pump controllers to generate gate driver ON (V_{GH}) and OFF (V_{GL}) voltages, a programmable V_{COM} generator, and an 8-channel level shifter in a single IC. The positive charge pump controller supports temperature compensation to reduce V_{GH} at high temperatures.

In addition to the above functions, the TPS65149 generates two signals to discharge the display panel during power-down, plus an additional active-low $\overline{\text{XAO}}$ reset output.

Supply sequencing during power-up can be controlled by an externally generated enable signal.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	ORDERING	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65149RSHR	56-Pin 7×7 QFN	TPS65149

(1) The device is supplied taped and reeled, with 3000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Pin Voltage(2)	FBN, VL, $\overline{WP}$, SCL, SDA, FBP, RESETIN, CLKIN1, CLKIN2, CLKIN3, CLKIN4, CLKIN5, CLKIN6, FB$\overline{PH}$, FREQ, COMP, RHVS, FB, SS, GD, VIN, DRVN, VDET, STVIN, RNTC, RSET, EN, $\overline{XAO}$	7	V
	DVRO, AVDD, SW, HVS	20	
	DRVP, VGH	40	
	VGL1, VGL2	–20	
	DSCHG1, DSCHRG2, STVOUT, RESETOUT, CLKOUT1, CLKOUT2, CLKOUT3, CLKOUT4, CLKOUT5, CLKOUT6	–20 to 40	
ESD Rating	Human Body Model	2	kV
	Machine Model	200	V
	Charged Device Model	500	V
P_D	Continuous Power Dissipation	See Thermal Table	W
T_A	Ambient temperature	–40 to 85	°C
T_J	Junction temperature	–40 to 150	°C
T_{STG}	Storage temperature	–65 to 150	°C
	Lead temperature (soldering, 10 seconds)	300	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) With respect to the AGND and LGND pins.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS65149 QFN 56 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	27.4	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	20.4	
θ_{JB}	Junction-to-board thermal resistance	7.1	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	7.0	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	2.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	3	5	6	V
V_{AVDD}	Boost converter output voltage range	7(1)		18	V
V_{GH}	Level shifter positive supply voltage range	15		38	V
V_{GL1}	Level shifter negative supply voltage range	–3		–15	V
V_{GL2}	Level shifter negative supply voltage range	–3		–15	V
V_{DET}	Panel discharge threshold voltage	2			V
I_{SET}	Programmable V_{COM} set current		0.1	0.5	mA
C_L	V_L decoupling capacitance	10	100	220	nF
T_A	Operating ambient temperature	–40	25	85	°C
T_J	Operating junction temperature	–40	85	125	°C

(1) Or V_{IN} + 1 V, whichever is lower.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5 V; V_{AVDD} = 13.6 V, V_{GH} = 28 V, V_{GL1} = V_{GL2} = –10 V, T_A = –40°C to 85°C; FREQ = high. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{IN}	V_{IN} supply current	Device not switching, V_{FB} = V_L+5%		0.75		mA
I_{SUP}	Positive supply current			0.04		mA
I_{GH}	Positive supply current	STVIN = 0 V, RESETIN = 0 V, CLKIN1-CLKIN6 = 0 V		0.26		mA
I_{GL1}	Negative supply current	STVIN = 0 V, RESETIN = 0 V, CLKIN1-CLKIN6 = 0 V		0.035		mA
I_{GL2}				0.046		
V_{UVLO}	UVLO threshold	V_{IN} rising		2.5		V
V_{HYS}	UVLO hysteresis	V_{IN} falling		0.25		V
V_L	External reference voltage	I_L = 100 µA	1.215	1.24	1.265	V
I_L	Reference voltage maximum output current	V_L = 1.24 V ±2%	250			µA
CONTROL SIGNALS (EN, HVS, FREQ, $\overline{WP}$)						
V_{IH}	High input voltage threshold	EN, HVS, FREQ, $\overline{WP}$ rising			2.0	V
V_{IL}	Low input voltage threshold	EN, HVS, FREQ, $\overline{WP}$ falling	0.5			V
$R_{PULL-UP}$	Pull-up resistor	EN, FREQ		50		kΩ
$R_{PULL-DOWN}$	Pull-down resistor	HVS, $\overline{WP}$		50		kΩ

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 5 V; V_{AVDD} = 13.6 V, V_{GH} = 28 V, V_{GL1} = V_{GL2} = –10 V, T_A = –40°C to 85°C; FREQ = high. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CONVERTER (AVDD)						
V_{AVDD}	Output voltage	I_{AVDD} = 0.5 A	7		18(1)	V
V_{OVP}	Overvoltage threshold	V_{AVDD} rising	18.0	19.0	20.0	V
$V_{OVP(HYS)}$	Overvoltage hysteresis	V_{AVDD} falling		0.3		V
$V_{SCP(AVDD)}$	Short-circuit threshold voltage	V_{AVDD} rising, during power-up		2.6		V
		V_{FB} falling, during normal operation		0.36		
$V_{FB(PG)}$	Power good threshold	V_{FB} rising		97		% of V_{REF}
		V_{FB} falling		91.7		
$t_{SCP(AVDD)}$	Short circuit timer	OFF time		55		ms
		ON time		5		
V_{FB}	Feedback regulation voltage		1.228	1.240	1.252	V
I_{FB}	Feedback input bias current	V_{FB} = 1.24V	–100		100	nA
$r_{DS(ON)}$	Switch ON resistance	V_{IN} = 5V, I_{SW} = I_{LIM}		0.13	0.18	Ω
I_{LIM}	Switch current limit		4.0	4.6	5.6	A
I_{LK}	Switch leakage current	EN = 0V, V_{SW} = 18.5V			30	µA
I_{SS}	Soft-start capacitor charge current	V_{SS} = 1.24V		4.4		µA
f_{SW}	Oscillator frequency	FREQ connected to V_{IN}	900	1200	1500	kHz
		FREQ connected to 0V	470	640	790	
	Line regulation	V_{IN} = 4 V to 6 V, I_{AVDD} = 0.5 A		0.01		%/V
	Load regulation	I_{AVDD} = 0.1 A to 0.5 A		0.2		%/A
R_{HVS}	HVS switch ON resistance	HVS = 5 V, RHVS = 0 V	400	500	600	Ω
GATE DRIVE (Isolation Switch)						
I_{GD}	Gate drive sink current	EN = 5 V, V_{GD} = TBD V		10		µA
R_{GD}	Gate drive internal pull-up resistance	EN = 0 V, I_{GD} = TBD mA		5		kΩ
POSITIVE CHARGE PUMP CONTROLLER (VGH)						
V_{DRVP}	Base drive voltage range	With external pull-up resistor			40	V
I_{DRVP}	Base drive sink current	Normal operation, sinking, V_{FBP} = 1.575 V, V_{DRVP} = 28 V	2.5			mA
		Short-circuit operation, sinking, V_{FBP} = 0 V, V_{DRVP} = 28 V	40		72	µA
V_{FBP}	Feedback regulation voltage	Lower limit; V_{RNTC} = 2 V, V_{FBPH} = 1.75 V	1.663	1.75	1.838	V
		Lower limit; V_{RNTC} = 1.5 V, V_{FBPH} = 1.75 V	1.425	1.50	1.575	
		Lower limit; V_{RNTC} = 1.0 V, V_{FBPH} = 1.75 V	1.178	1.24	1.302	
$V_{FBP(SCP)}$	Short circuit threshold voltage	V_{FBP} rising, during power-up		124		mV
		V_{FBP} falling, during normal operation		340		
$V_{FBP(PG)}$	Power good threshold	V_{FBP} rising		97.5		% of V_{REF}
		V_{FBP} falling		92.5		
$t_{SCP(VGH)}$	Short circuit timer	Starts from boost converter power good		15		ms
I_{FBP}	FBP input bias current	V_{RNTC} = 1 V, V_{FBPH} = 1.75 V, V_{FBP} = 1.24 V	–100		100	nA
I_{RNTC}	RNTC output current	V_{RNTC} = 1.5 V, matched to I_{FBPH}; T_A = 25 °C	190	200	210	µA
I_{FBPH}	FBPH output current	V_{FBPH} = 1.75 V, trimnmed; at T_A = 25 °C	195	200	205	µA
	Load regulation	I_{GH} = 1 mA to 50 mA		0.05		%/mA

(1) Limited by overvoltage protection function.

ELECTRICAL CHARACTERISTICS (continued)

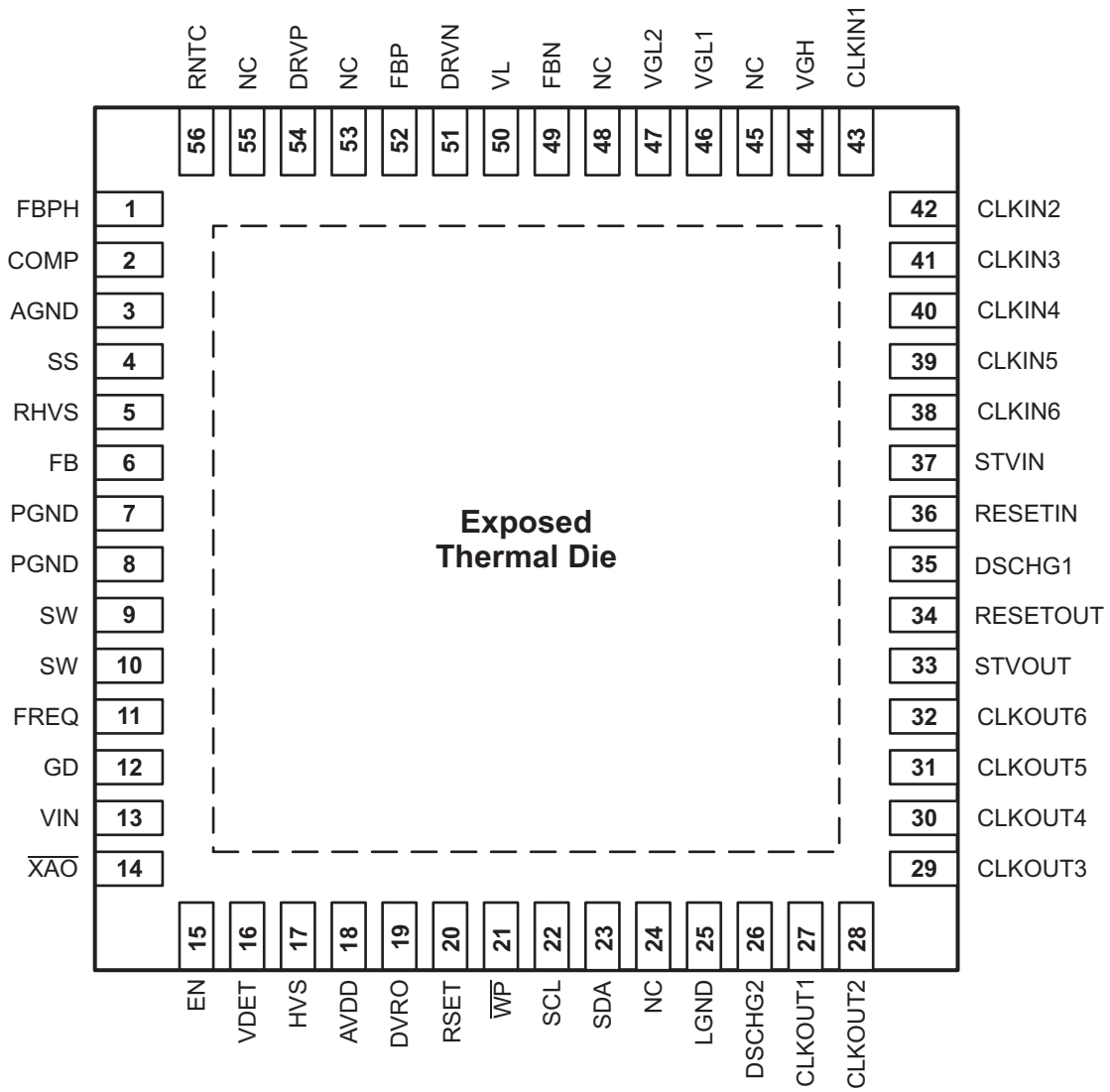
V_{IN} = 5 V; V_{AVDD} = 13.6 V, V_{GH} = 28 V, V_{GL1} = V_{GL2} = –10 V, T_A = –40°C to 85°C; FREQ = high. Typical values are at 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NEGATIVE CHARGE PUMP CONTROLLER (VGL)						
I_{DRVN}	Base drive current	Normal operation, sourcing, V_{FBN} = 25 mV, V_{DRVN} = 0.7V	2.5			mA
		Short-circuit operation, sourcing, V_{FBN} = 1.116 V, V_{DRVN} = 0.7 V	200	300	480	µA
V_{FBN}	Feedback regulation voltage	I_{DRVN} = 1 mA, sourcing	–15		15	mV
I_{FBN}	FBN input bias current	V_{FBN} = 0 V	–100		100	nA
$V_{FBN(SCP)}$	Short circuit threshold voltage	V_{FBN} falling, during start-up		794		mV
		V_{FBN} rising, during normal operation		817		
$V_{FBN(PG)}$	Power good threshold	V_{FBN} falling		2.8		% of V_{REF}
		V_{FBN} rising		7.5		
	Load regulation	I_{GL1} = 1 mA to 50 mA		0.05		%/mA
PROGRAMMABLE VCOM						
SET_{VR}	SET voltage resolution			7		Bits
SET_{ZSE}	SET zero-scale error				1	LSB
SET_{FSE}	SET full-scale error				7	LSB
	V_{AVDD} to V_{SET} voltage ratio			20		V/V
$_{DNL}$	Differential nonlinearity			0.165	0.8	Bits
t_{WRITE}	EEPROM write time				100	ms
N_{WRITE}	Number of specified EEPROM write cycles		1000			cycles
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold			138		°C
T_{HYS}	Thermal shutdown hysteresis			8		°C
LEVEL SHIFTERS (CLK1 to CLK6)						
V_{UVLO}	UVLO threshold	V_{GH} rising.	5.0	7.5	10.0	V
V_{IH}	Level shifter high level input threshold	V_{CLKINx} rising			1.5	V
V_{IL}	Level shifter low level input threshold	V_{CLKINx} falling	0.5			V
$r_{DS(ON)}$	High side ON resistance	$I_{CLKOUTx}$ = 10 mA, sourcing		14		Ω
	Low side ON resistance	$I_{CLKOUTx}$ = 10 mA, sinking		8		
LEVEL SHIFTERS (STV, RESET)						
V_{IH}	Level shifter high level input threshold	V_{STVIN}, $V_{RESETIN}$ rising			1.5	V
V_{IL}	Level shifter low level input threshold	V_{STVIN}, $V_{RESETIN}$ falling	0.5			V
$r_{DS(ON)}$	High side ON resistance	I_{STVOUT}, $I_{RESETOUT}$ = 10 mA, sourcing		35		Ω
	Low side ON resistance	I_{STVOUT}, $I_{RESETOUT}$ = 10 mA, sinking		15		
DISCHARGE (DISCHRG1, DISCHRG2)						
$V_{IL(DET)}$	Discharge threshold voltage	V_{DET} falling	1.221	1.240	1.259	V
V_{HYS}	Discharge hysteresis	V_{DET} rising		50		mV
$r_{DS(ON)}$	High side ON resistance	$I_{DSCHRG1}$, $I_{DSCHRG2}$ = 10 mA, sourcing		15		Ω
	Low side ON resistance	$I_{DSCHRG1}$, $I_{DSCHRG2}$ = 10 mA, sinking		8		
I^2C INTERFACE						
	Bus address			4Fh		
V_{IL}	Low level input voltage	V_{IN} = 4 V to 6 V	0.7			V
V_{IH}	High level input voltage	V_{IN} = 4 V to 6 V			1.5	V
V_{OL1}	Low level output voltage	Sinking 3 mA			0.4	V

DEVICE INFORMATION

PIN ASSIGNMENT

PIN ASSIGNMENT
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
FBPH	1	I	Connecting a resistor between this pin and ground allows the maximum output voltage (i.e., at the voltage at colder temperatures) of the positive charge pump to be set. A current of 200 µA flows out of this pin, and at colder temperatures the positive charge pump regulates to a feedback voltage equal to this current multiplied by the resistor connected between FBPH and ground.
COMP	2	I	Connecting a suitable compensation network between this pin and ground allows the boost converter to be optimized for stable operation and proper performance. A series RC network is adequate for most applications.
AGND	3	P	Analog ground.
SS	4	I	A capacitor connected between this pin and ground allows the start-up characteristic of the boost converter to be controlled. Larger capacitor values lengthen the time required for the boost converter to reach full output power capability and reduce the inrush current drawn from V_{IN}.
RHVS	5	O	A resistor connected between this pin and the FB pin allows the boost converter output voltage during high voltage stress mode to be set.
FB	6	I	Boost converter feedback pin.
PGND	7, 8	P	Power ground.
SW	9, 10	P	Boost converter switch node.
FREQ	11	I	Boost converter frequency select pin. The boost converter's nominal switching frequency is 1.2 MHz when FREQ=high and 640 kHz when FREQ=low. This pin features an internal pull-up and may be left floating if 1.2 MHz operation is desired.
GD	12	O	Gate drive for external isolation switch. This pin sinks a constant current when EN=high and is pulled up by a resistor when EN=low.
VIN	13	P	Supply voltage. This pin should be decoupled using a 100 nF ceramic capacitor connected close to the VIN pin.
$\overline{XAO}$	14	O	Reset output. This open-drain output is pulled low when the voltage applied to the VDET pin is below the internal reference voltage of 1.24 V.
EN	15	I	The TPS65149 is enabled when EN=high and disabled when EN=low. Note that the panel discharge function always works and is not disabled when EN=low.
VDET	16	I	Panel discharge detection. The TPS65149 enters discharge mode (all level shifter outputs and the two discharge signals track V_{GH}) when the voltage applied to the VDET pin is below the internal reference voltage. $\overline{XAO}$ is also pulled low when $V_{DET} < V_{REF}$.
HVS	17	I	High voltage stress mode is selected when HVS=high and normal mode is selected when HVS=low. This pin features an internal pull-down and may be left floating during normal operation.
AVDD	18	P	This pin must be connected to the output of the boost converter. It is used for two main functions: a) the internal reference for the programmable V_{COM} block is derived from it b) boost converter overvoltage and short-circuit conditions are detected by monitoring the voltage on it
DVRO	19	I	This pin is a current sink whose current can be programmed via the I^2C interface. It is typically connected to an external resistor divider connected between AVDD and ground to generate an appropriate input voltage for an external V_{COM} buffer.
RSET	20	I	A resistor connected between this pin and ground sets the full-scale value of the current sink connected to the DVRO pin. Smaller resistor values generate larger currents.
$\overline{WP}$	21	I	Data in the internal EEPROM can only be overwritten when $\overline{WP}$=high. When $\overline{WP}$=low, all write operates to the EEPROM are prevented.
SCL	22	I/O	I^2C interface clock signal.
SDA	23	I/O	I^2C interface data signal.
NC	24	N/A	Not connected. Leave floating or connect to ground.
LGND	25	P	Level shifter ground connection.
DSCHG2	26	O	Level shifter output
CLKOUT1	27	O	Level shifter output
CLKOUT2	28	O	Level shifter output
CLKOUT3	29	O	Level shifter output
CLKOUT4	30	O	Level shifter output
CLKOUT5	31	O	Level shifter output
CLKOUT6	32	O	Level shifter output
STVOUT	33	O	Level shifter output

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RESETOUT	34	O	Level shifter output
DSCHG1	35	O	Level shifter output
RESETIN	36	I	Level shifter input
STVIN	37	I	Level shifter input
CLKIN6	38	I	Level shifter input
CLKIN5	39	I	Level shifter input
CLKIN4	40	I	Level shifter input
CLKIN3	41	I	Level shifter input
CLKIN2	42	I	Level shifter input
CLKIN1	43	I	Level shifter input
VGH	44	P	Level shifter positive supply. This pin should be decoupled using a 0.1 µF to 10 µF ceramic capacitor connected close to the VGH pin.
NC	45	N/A	Not connected. Leave floating or connect to ground.
VGL1	46	P	Level shifter negative supply for all channels except DSCHRG2. This pin should be decoupled using a 0.1 µF to 10 µF ceramic capacitor connected close to the VGL1 pin.
VGL2	47	P	Level shifter negative supply for DSCHRG2 channel. This pin should be decoupled using a 0.1 µF to 10 µF ceramic capacitor connected close to the VGL2 pin.
NC	48	N/A	Not connected. Leave floating or connect to ground.
FBN	49	I	Negative charge pump controller feedback pin.
VL	50	O	This pin can be used to provide an accurate reference voltage for the negative charge pump. It cannot supply large currents and is not intended to supply any other external circuitry. This pin should be decoupled using a 0.1 µF to 1 µF ceramic capacitor connected close to the VL pin.
DRVN	51	O	This pin provides the base drive current for an external NPN transistor used to regulate V_{GL1}.
FBP	52	I	Positive charge pump controller feedback pin.
NC	53	N/A	Not connected. Leave floating or connect to ground.
DRVP	54	O	This pin provides the base drive current for an external PNP transistor used to regulate V_{GH}.
NC	55	N/A	Not connected. Leave floating or connect to ground.
RNTC	56	I	A thermistor-resistor network connected to this pin allows the temperature compensation characteristic of the positive charge pump to be programmed.
Exposed Thermal Die		P	Connect to ground. The copper area of the ground plane must be large enough to ensure adequate thermal performance.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
BOOST CONVERTER			
Efficiency		V_{IN} = 5 V, V_{AVDD} = 13.6 V, I_{AVDD} = 0 A to 1 A	Figure 1
		V_{IN} = 5 V, V_{AVDD} = 18 V, I_{AVDD} = 0 A to 1 A	Figure 2
Frequency	vs Load current	V_{IN} = 5 V, V_{AVDD} = 13.6 V, I_{AVDD} = 0 A to 0.8 A	Figure 3
	vs Supply voltage	V_{IN} = 3.5 V to 6.0 V, V_{AVDD} = 13.6 V, I_{AVDD} = 0.5 A	Figure 4
Undervoltage Protection	f_{SW}=1.2MHz, L=4.7µH	V_{IN} = 5 V, V_{AVDD} = 13.6 V (10 V transient)	Figure 5
Load Transient Response	f_{SW}=640kHz, L=10µH	V_{IN} = 5 V, V_{AVDD} = 13.6 V, I_{AVDD} = 250 mA/750 mA step	Figure 6
	f_{SW}=1.2MHz, L=4.7µH		Figure 7
Soft-start	C_{SS}=22nF	V_{IN} = 5 V, V_{AVDD} = 13.6 V, I_{AVDD} = 0.5 A	Figure 8
Overvoltage Protection	Duration = 75 ms		Figure 9
Short-Circuit Protection	Duration = 75 ms	V_{IN} = 5 V, V_{AVDD} = 13.6 V, I_{AVDD} = 0.5 A	Figure 10
	Duration = 25 ms	V_{IN} = 5 V, V_{AVDD} = 13.6 V, I_{AVDD} = 0.5 A	Figure 11
Switch Node Waveform	CCM operation	V_{IN} = 5 V, V_{AVDD} = 13.6 V, I_{AVDD} = 0.5 A	Figure 12
	DCM operation	V_{IN} = 5 V, V_{AVDD} = 13.6V, I_{AVDD} = 0.1A	Figure 13
POSITIVE CHARGE PUMP			
Load Transient Response	f_{SW} = 640kHz, L = 10µH	V_{IN} = 5V, V_{AVDD} = 13.6V, I_{AVDD} = 0.5A V_{GH} = 28V, I_{GH} = 10 mA/50 mA step	Figure 14
	f_{SW} = 1.2MHz, L = 4.7µH		Figure 15
Temperature Compensation		V_{IN} = 4 V to 6 V, V_{AVDD} = 13.6 V, I_{AVDD} = 0.5A, $V_{GH(COLD)}$ = 28 V, $V_{GH(HOT)}$ = 24 V, T_{COLD} = -10°C, T_{HOT} = 10°C, I_{GH} = 25 mA	Figure 16
NEGATIVE CHARGE PUMP			
Load Transient Response	f_{SW} = 640kHz, L = 10µH	V_{IN} = 5 V, V_{AVDD} = 13.6 V, I_{AVDD} = 0.5 A, V_{GL1} = –10 V, I_{GL1} = 10 mA/50 mA step	Figure 17
	f_{SW} = 1.2MHz, L = 4.7µH		Figure 18
START-UP SEQUENCING			
Power-Up Sequence	V_{IN}, V_{AVDD}, V_{GH}, V_{GL1}	V_{IN} = 5V, V_{AVDD} = 13.6 V, V_{GH} = 28 V, V_{GL1} = –10 V, V_{GL2} = –6 V	Figure 19
Power-Up Sequence	V_{IN}, CLKOUTx, STVOUT, RESETOUT	V_{IN} = 5V, V_{AVDD} = 13.6 V, V_{GH} = 28 V, V_{GL1} = –10 V, V_{GL2} = –6 V	Figure 20
Power-Up Sequence	V_{IN}, DSCHRG1, DSCHRG2, $\overline{XAO}$	V_{IN} = 5V, V_{AVDD} = 13.6 V, V_{GH} = 28 V, V_{GL1} = –10 V, V_{GL2} = –6 V	Figure 21
Power-Down Sequence	V_{IN}, CLKOUTx, STVOUT, RESETOUT	V_{IN} = 5V, V_{AVDD} = 13.6 V, V_{GH} = 28 V, V_{GL1} = –10 V, V_{GL2} = –6 V	Figure 22
Power-Down Sequence	V_{IN}, DSCHRG1, DSCHRG2, $\overline{XAO}$	V_{IN} = 5V, V_{AVDD} = 13.6 V, V_{GH} = 28 V, V_{GL1} = –10 V, V_{GL2} = –6 V	Figure 23
LEVEL SHIFTERS			
Peak Output Current	CLKOUTx	V_{GH} = 28V, V_{GL1} = –10V, V_{GL2} = –6V, 10 nF load	Figure 24
	STVOUT, RESETOUT		Figure 25
	DSCHRGx		Figure 26
Rise Time	CLKOUTx	V_{GH} = 28 V, V_{GL1} = –10 V, V_{GL2} = –6 V, 47Ω + 10 nF load	Figure 27
	STVOUT, RESETOUT		Figure 28
	DSCHRGx		Figure 29
Fall Time	CLKOUTx	V_{GH} = 28 V, V_{GL1} = –10 V, V_{GL2} = –6 V, 47Ω + 10 nF load	Figure 30
	STVOUT, RESETOUT		Figure 31
	DSCHRGx		Figure 32

BOOST CONVERTER EFFICIENCY (V_{AVDD} = 13.6 V)

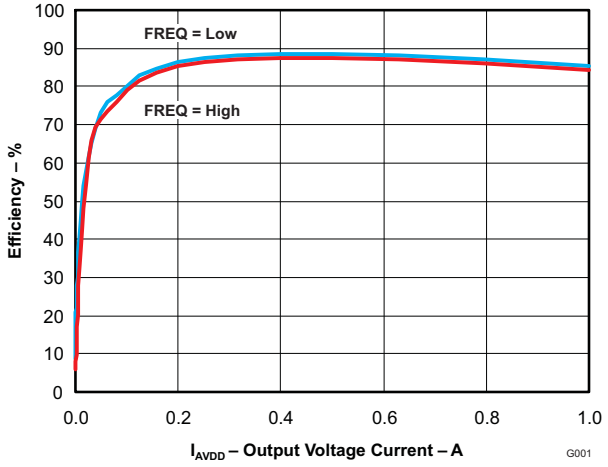


Figure 1.

BOOST CONVERTER EFFICIENCY (V_{AVDD} = 18 V)

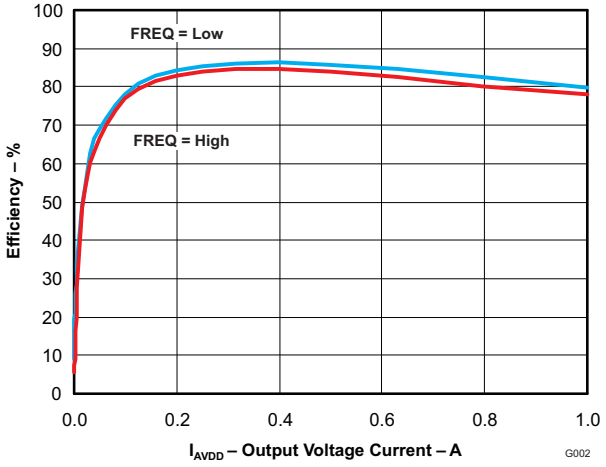


Figure 2.

BOOST CONVERTER FREQUENCY vs. LOAD CURRENT

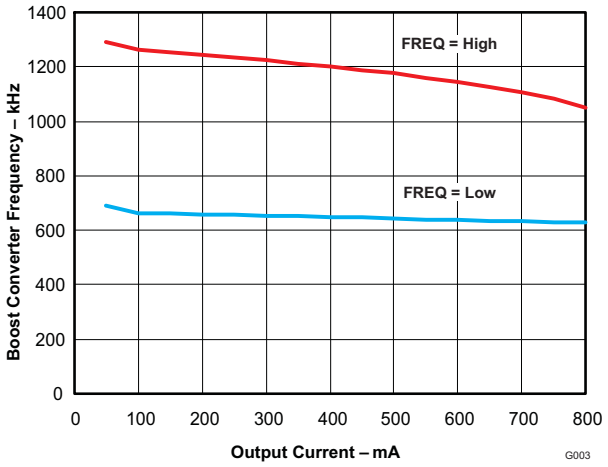


Figure 3.

BOOST CONVERTER FREQUENCY vs. SUPPLY VOLTAGE

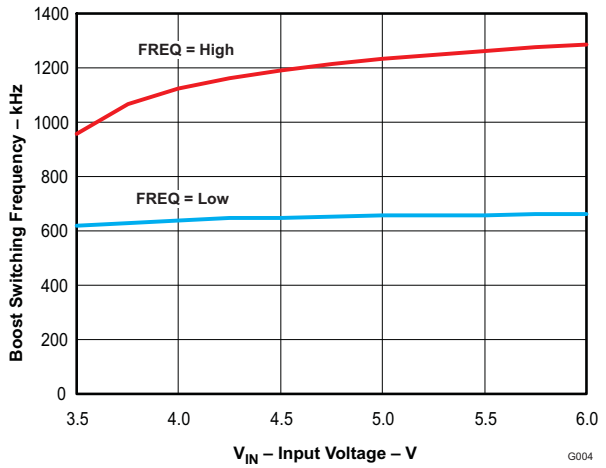


Figure 4.

BOOST CONVERTER UNDERVOLTAGE PROTECTION

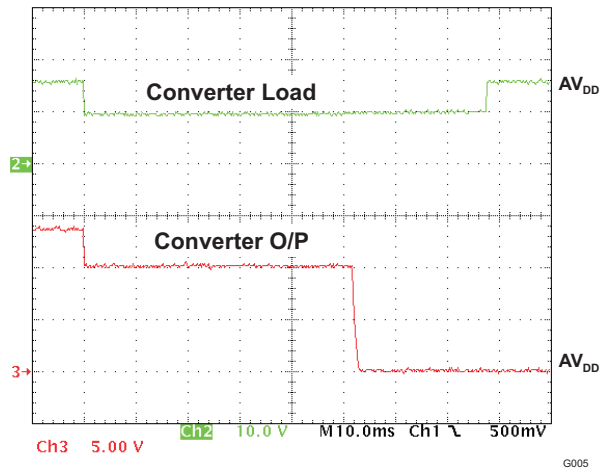


Figure 5.

BOOST CONVERTER LOAD TRANSIENT RESPONSE

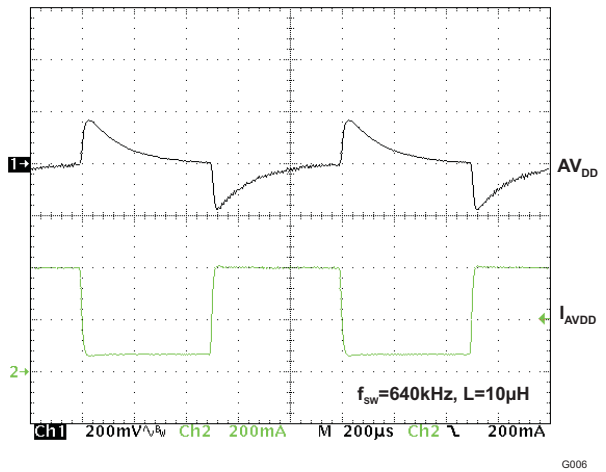


Figure 6.

BOOST CONVERTER LOAD TRANSIENT RESPONSE

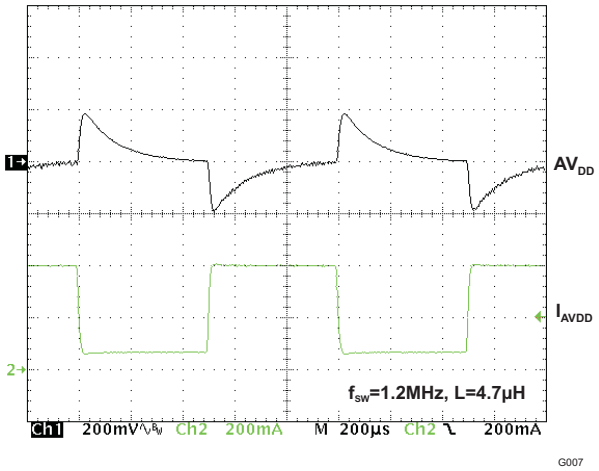


Figure 7.

BOOST CONVERTER SOFT-START

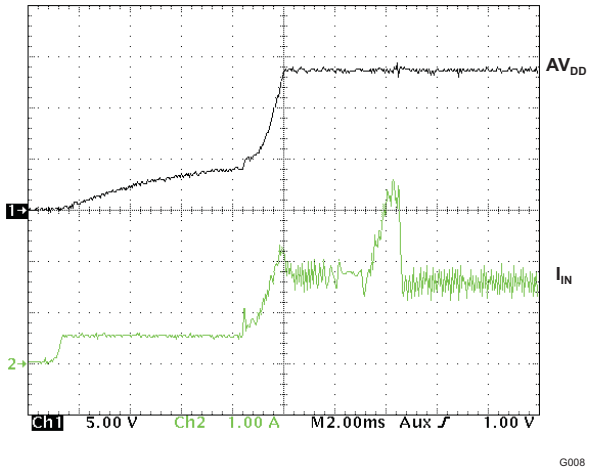


Figure 8.

BOOST CONVERTER OVERVOLTAGE PROTECTION

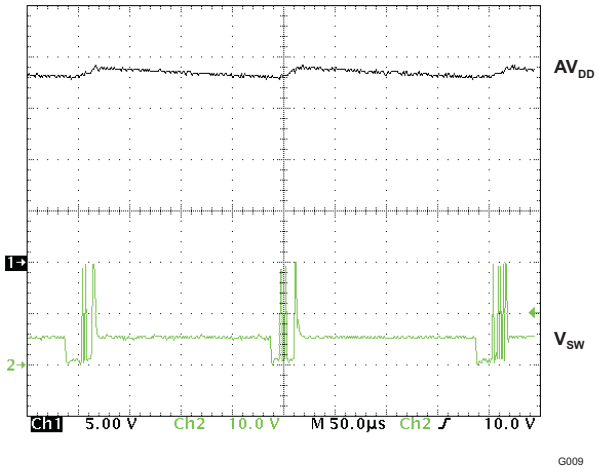


Figure 9.

BOOST CONVERTER SHORT-CIRCUIT PROTECTION

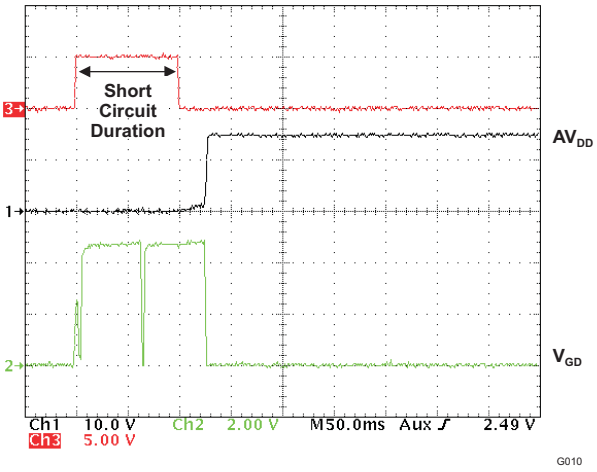


Figure 10.

BOOST CONVERTER SHORT-CIRCUIT PROTECTION

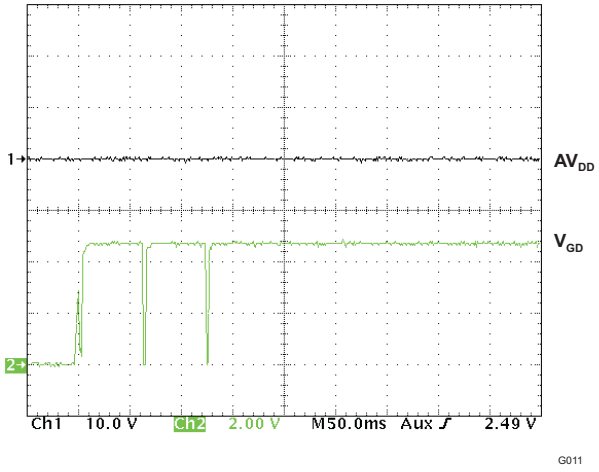


Figure 11.

BOOST CONVERTER SWITCH NODE WAVEFORM (CCM)

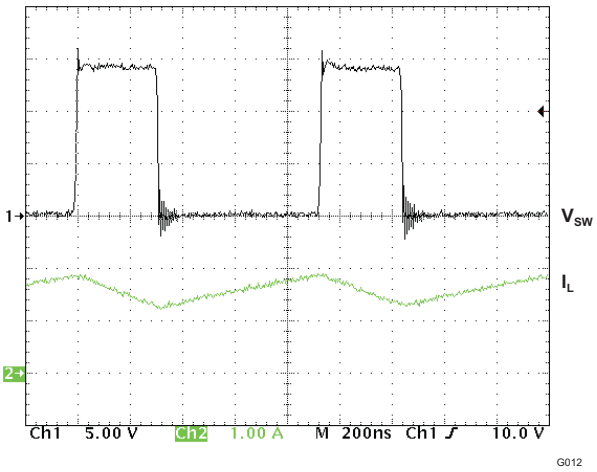


Figure 12.

BOOST CONVERTER SWITCH NODE WAVEFORM (DCM)

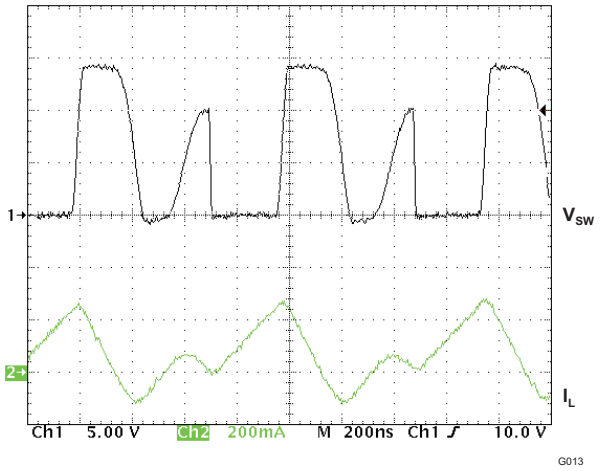


Figure 13.

POSITIVE CHARGE PUMP LOAD TRANSIENT RESPONSE

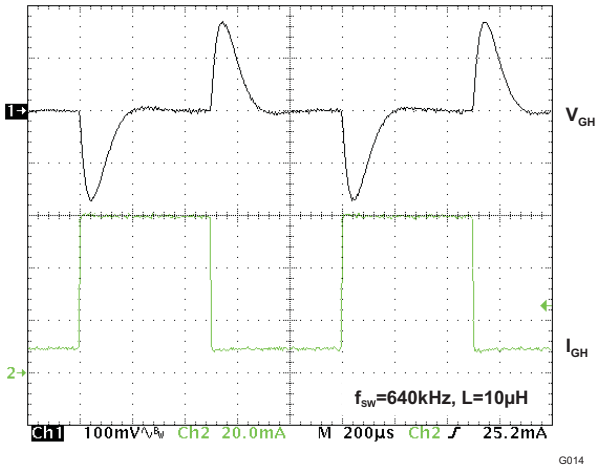


Figure 14.

POSITIVE CHARGE PUMP LOAD TRANSIENT RESPONSE

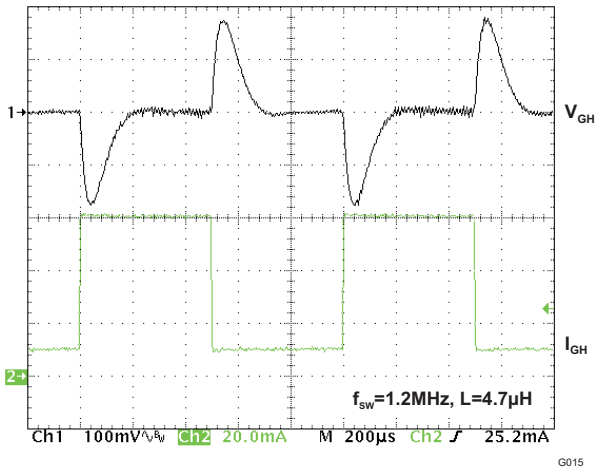


Figure 15.

POSITIVE CHARGE PUMP TEMPERATURE COMPENSATION

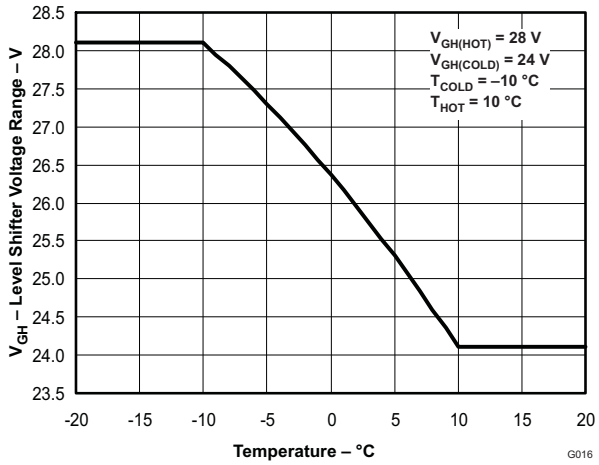


Figure 16.

NEGATIVE CHARGE PUMP LOAD TRANSIENT RESPONSE

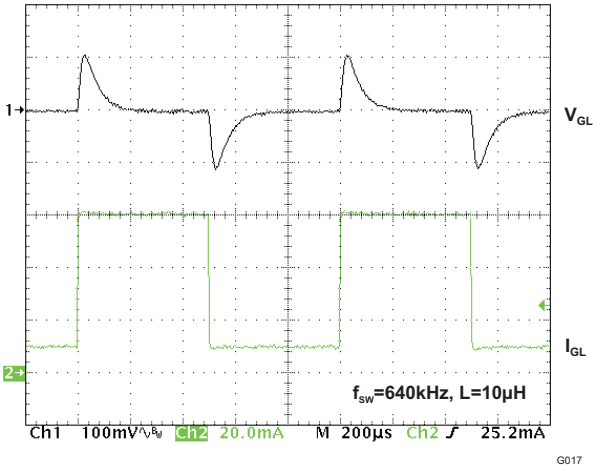


Figure 17.

NEGATIVE CHARGE PUMP LOAD TRANSIENT RESPONSE

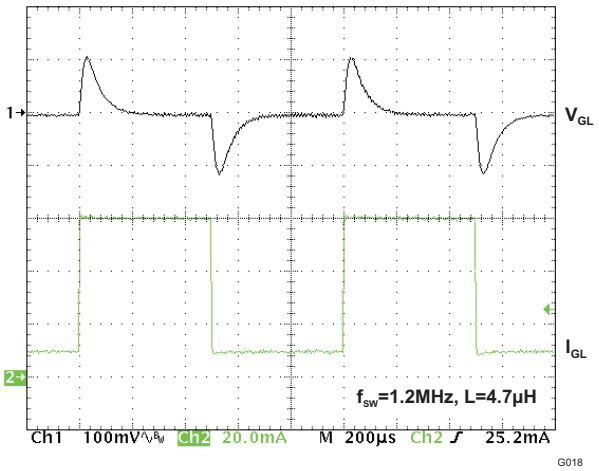


Figure 18.

POWER-UP SEQUENCE #1

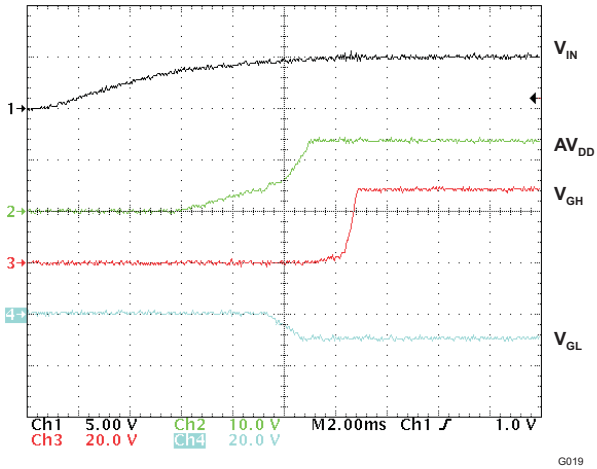


Figure 19.

POWER-UP SEQUENCE #2

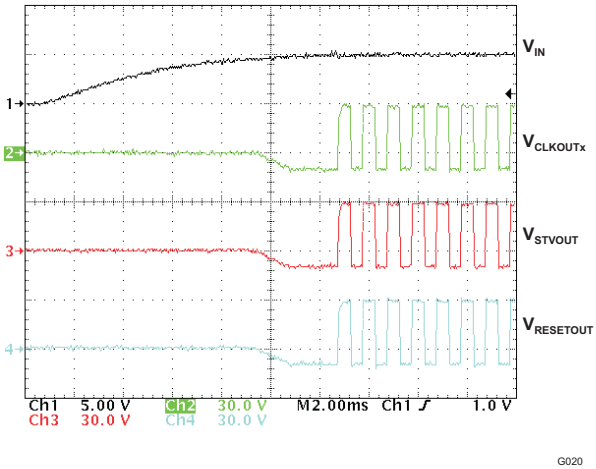


Figure 20.

POWER-UP SEQUENCE #3

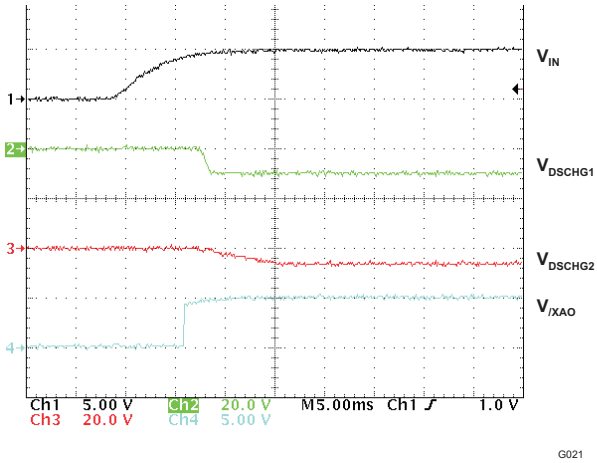


Figure 21.

POWER-DOWN SEQUENCE #1

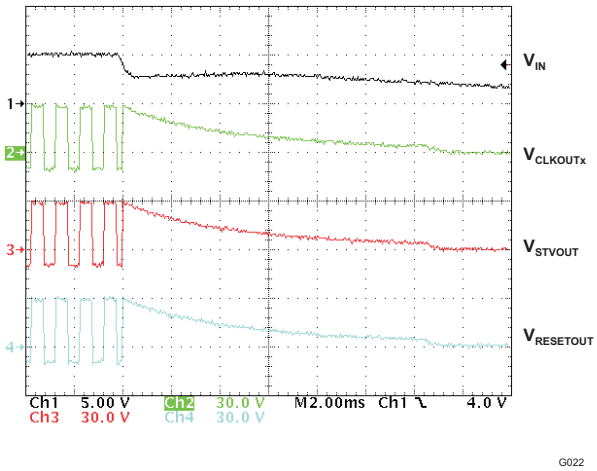


Figure 22.

POWER-DOWN SEQUENCE #2

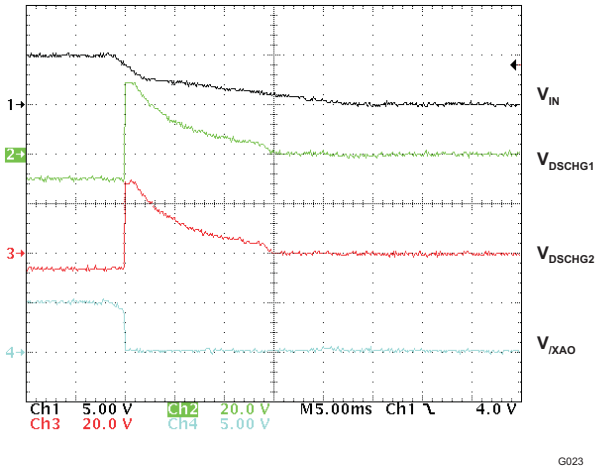


Figure 23.

PEAK OUTPUT CURRENT (CLKx)

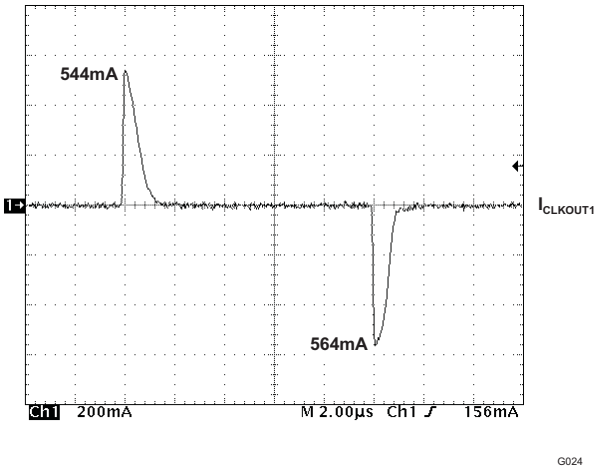


Figure 24.

PEAK OUTPUT CURRENT (STVOUT, RESETOUT)

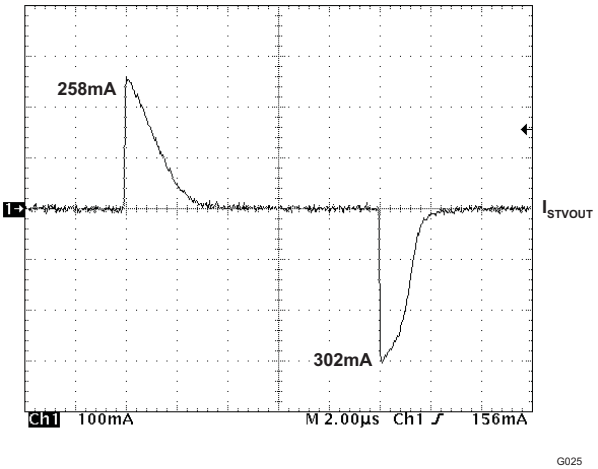


Figure 25.

PEAK OUTPUT CURRENT (DSCHRGx)

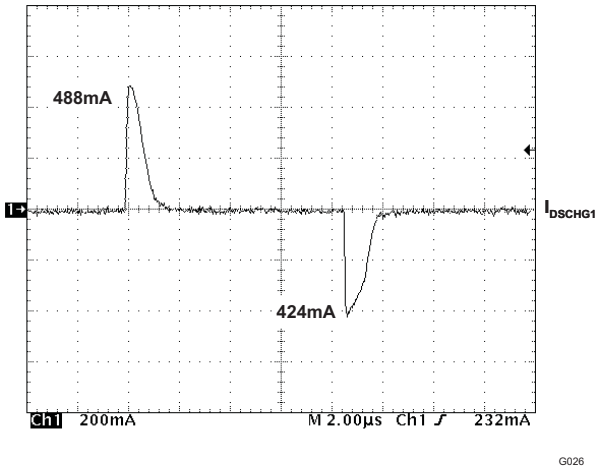


Figure 26.

RISE TIME (CLKOUTx)

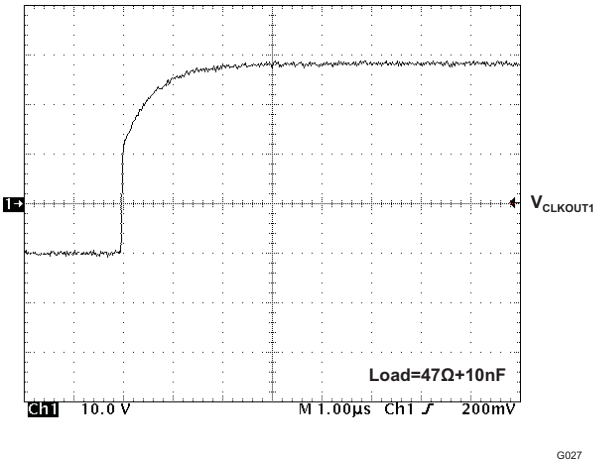


Figure 27.

RISE TIME (STVOUT, RESETOUT)

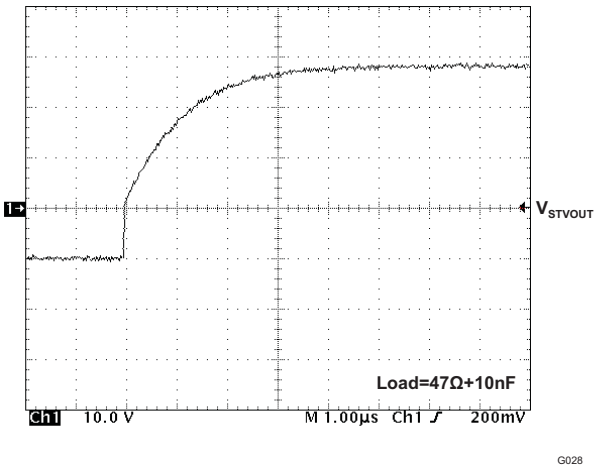


Figure 28.

RISE TIME (DSCHRGx)

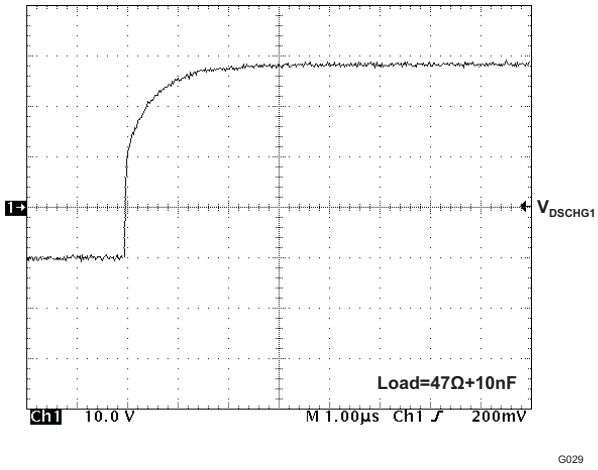


Figure 29.

FALL TIME (CLKOUTx)

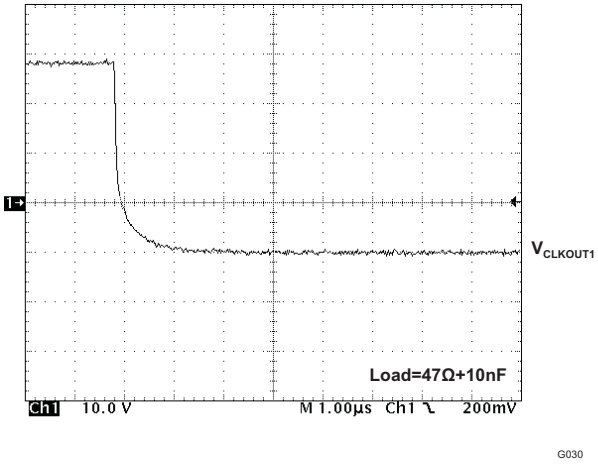


Figure 30.

FALL TIME (STVOUT, RESETOUT)

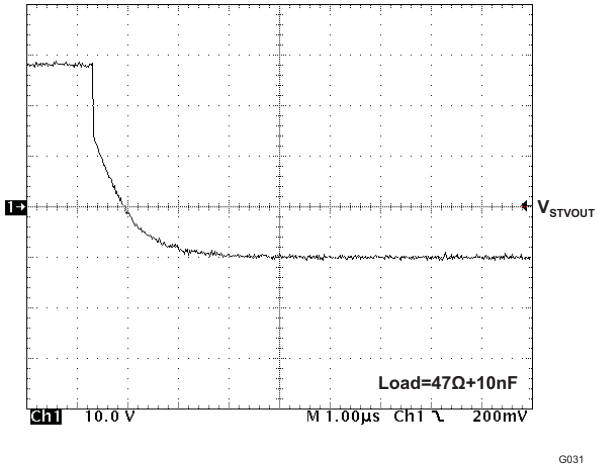


Figure 31.

FALL TIME (DSCHRGx)

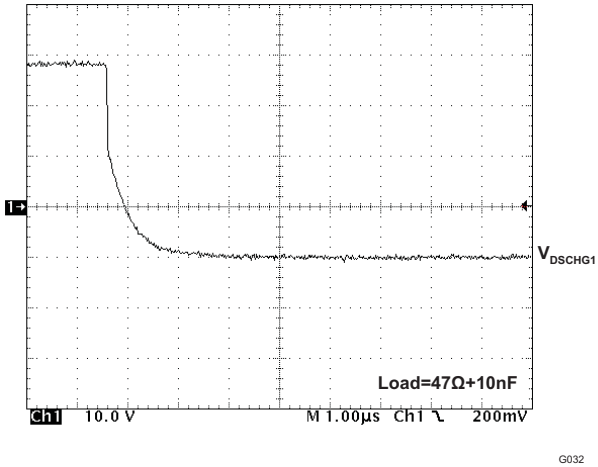


Figure 32.

DETAILED DESCRIPTION

An internal block diagram of the TPS65149 is shown in Figure 33.

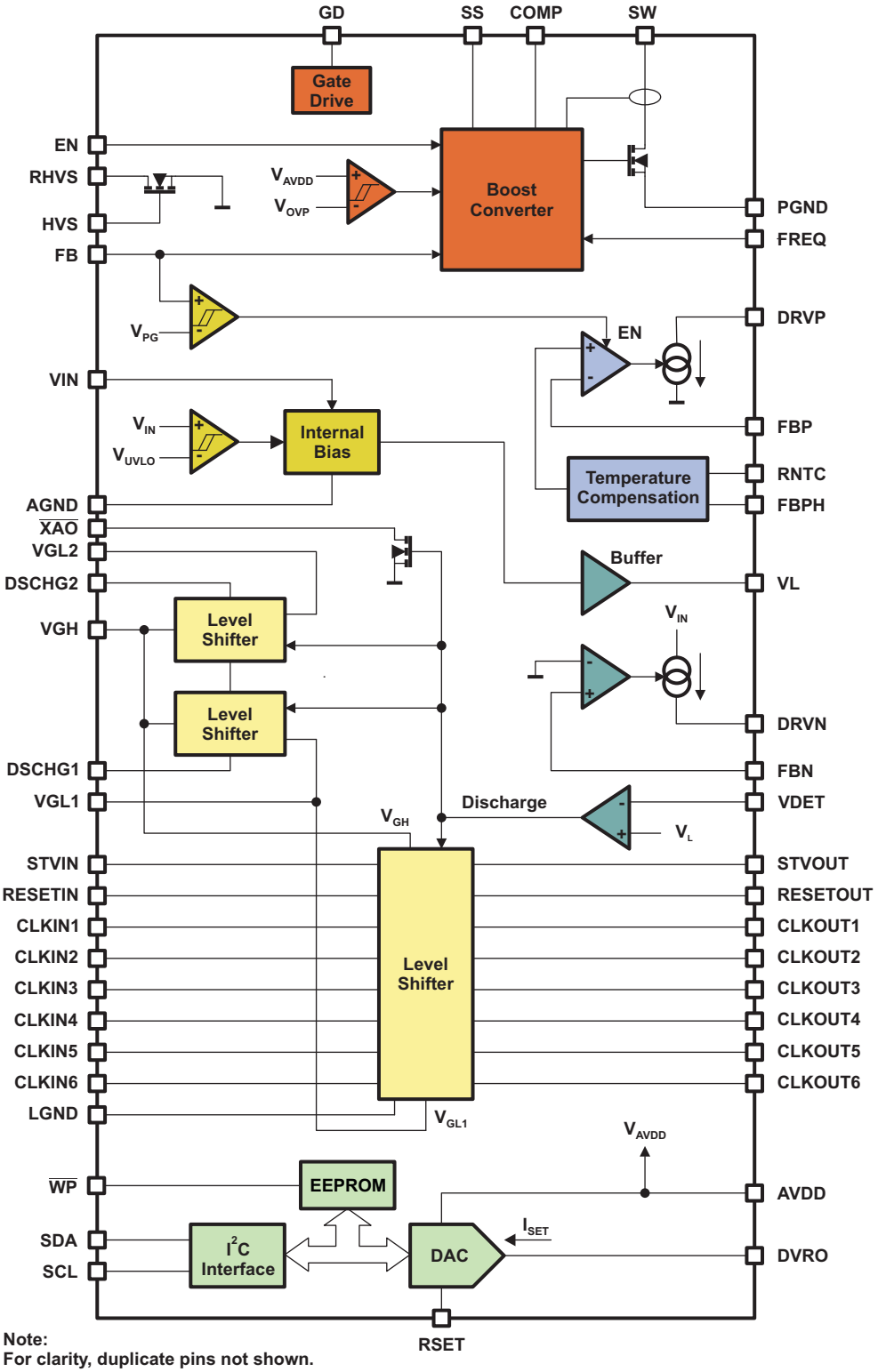


Figure 33. Internal Block Diagram

Boost Converter

An internal block diagram of the boost converter is contained in Figure 34.

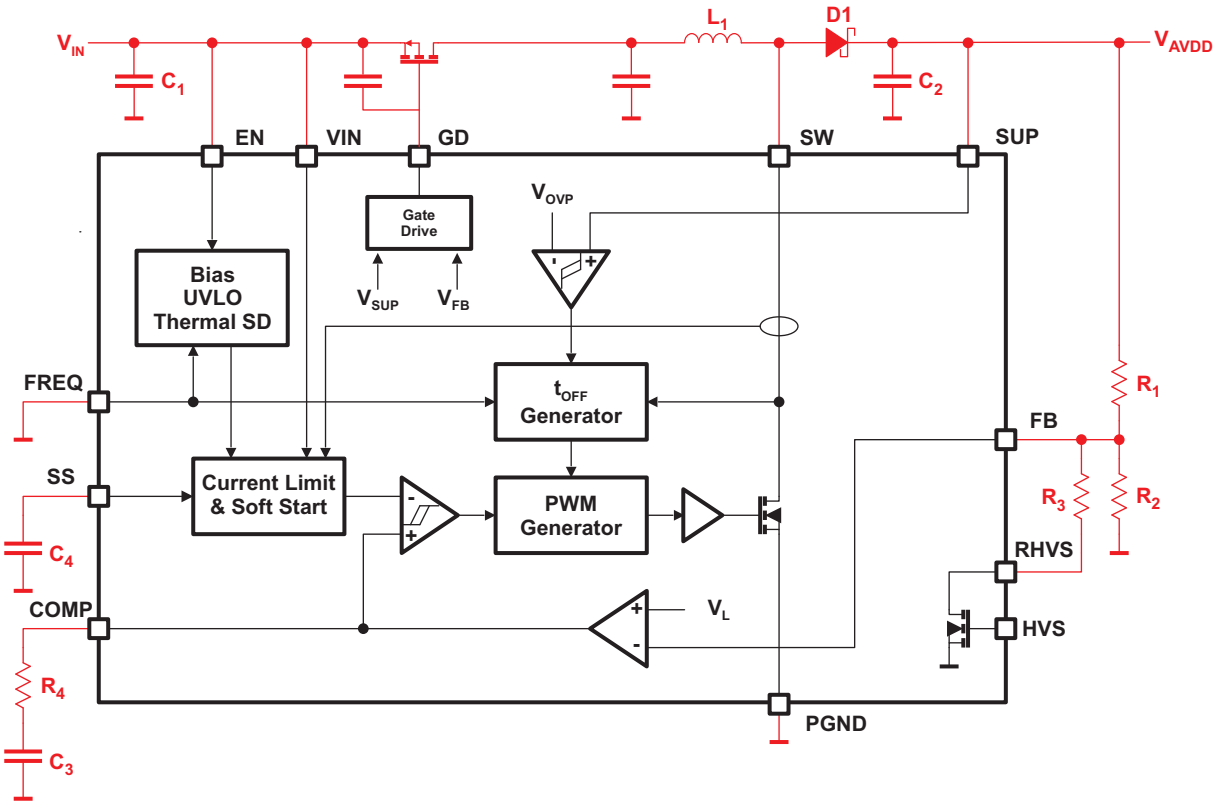


Figure 34. Boost Converter Internal Block Diagram

The boost converter is designed for output voltages up to 18V with a switch current limit of 4 A (guaranteed minimum). The converter uses a current mode, quasi-constant frequency topology, and is externally compensated for maximum flexibility. A soft-start feature limits the current drawn from V_{IN} during start-up, and the converter's switching frequency can be selected between 640 kHz and 1.2 MHz.

The converter's adaptive off-time topology achieves superior transient response and operates over a wider range of applications than conventional converters.

Design Procedure (Boost Converter)

The first step in the design procedure is to calculate the peak switch current. The simplest way to do this is to use the curves in the typical characteristics section to estimate converter efficiency in the intended application. Alternatively, a conservative worst-case value such as 85% can be used.

Once a value for the converter's efficiency η is available, Equation 1 can be used to calculate its duty cycle.

$$D = 1 - \frac{V_{IN} \times \eta}{V_{AVDD}} \tag{1}$$

The next step is to use Equation 2 to calculate the change in inductor current per cycle.

$$\Delta I_L = \frac{V_{IN} \times D}{f \times L} \tag{2}$$

Finally, the peak switch current can be calculated using Equation 3.

$$I_{SW(PK)} = \frac{I_{AVDD}}{1 - D} + \frac{\Delta I_L}{2} \tag{3}$$

The value for peak switch current calculated using Equation 3 must be lower than the minimum specified for the device, and should be calculated under worst-case conditions (minimum V_{IN} and maximum I_{AVDD}).

Inductor Selection (Boost Converter)

The boost converter in the TPS65149 has been optimized for inductors in the range 3.3 µH to 6.8 µH when using the higher switching frequency and in the range 7 µH to 13 µH when using the lower switching frequency.

The saturation current of the inductor must be greater than the peak switch current plus an additional margin to allow for heavy load transients. A saturation current of 130% of the value calculated using Equation 3 is adequate for most applications.

Table 1 shows a selection of inductors suitable for use with the TPS65149.

Table 1. Boost Converter Inductor Selection

INDUCTANCE	MANUFACTURER	PART NUMBER	SIZE	DCR	ISAT
1.2 MHz OPERATION					
4.7 µH	Coiltronics	UP2B-4R7-R	14.0 × 10.4 × 6.0	17 mΩ	5.5 A
4.7 µH	Sumida	CDRH12NP-4R7-M	12.3 × 12.3 × 4.5	18 mΩ	5.7 A
4.7 µH	Sumida	CDRH127	12.3 × 12.3 × 8.0	12 mΩ	6.8 A
640 kHz OPERATION					
10 µH	Coilcraft	DS3316P	13.0 × 9.4 × 5.1	70 mΩ	3.5 A
10 µH	Sumida	CDRH8D43	8.3 × 8.3 × 4.5	29 mΩ	4.0 A
10 µH	Sumida	CDRH127	12.3 × 12.3 × 8.0	16 mΩ	5.4 A
10 µH	Sumida	CDRH127LD	12.3 × 12.3 × 8.0	15 mΩ	6.7 A

Rectifier Selection (Boost Converter)

A Schottky type is recommended for the boost converter rectifier diode because its low forward voltage improves efficiency. The diode's reverse voltage rating must be greater than 20 V, which is the maximum it will experience (the TPS65149's overvoltage protection function prevents this voltage being any higher). The diode's average rectified current rating must be at least as high as the maximum I_{AVDD}. A 2 A rating is sufficient for most applications.

Equation 4 can be used to calculate the power dissipated in the diode. The diode must be capable of handling this power without overheating. A power rating of 500 mW is sufficient for most applications.

$$P = V_F \times I_{AVDD} \quad (4)$$

Where:

V_F is the diode's forward voltage

I_{AVDD} is the average (mean) boost converter output current

Table 2 shows a selection of rectifier diodes suitable for use with the TPS65149.

Table 2. Boost Converter Rectifier Selection

CURRENT	MANUFACTURER	PART NUMBER	SIZE	VR	VF
2 A	Vishay	SL22	SMA	20 V	0.44 V at 2 A
2 A	Vishay	SS22	SMA	20 V	0.5 V at 2 A

Input Capacitor Selection (Boost Converter)

For good supply voltage filtering, low ESR capacitors are recommended. The TPS65149 has an analog supply voltage pin (VIN) that should be decoupled with a ceramic capacitor in the range 100 nF to 1 µF, connected close to the VIN pin.

The main boost converter (i.e. where V_{IN} is connected to the inductor of the boost converter) should also be decoupled. Two 10 µF or one 22 µF ceramic capacitor are adequate for most applications, however, these values can be increased if improved filtering is required.

Setting the Output Voltage (Boost Converter)

The output voltage of the boost converter is set by a resistor divider connected to the FB pin. The boost converter's main error amplifier compares the feedback voltage with the internal reference voltage V_L so that the output is regulated at a voltage given by Equation 5.

$$V_{AVDD} = 1.24 \times \left(\frac{R_1}{R_2} + 1 \right) \quad (5)$$

Soft-Start (Boost Converter)

To reduce the inrush current drawn from V_{IN} during start-up the boost converter includes a soft-start feature. Soft-start is controlled by a capacitor connected to the soft-start (SS) pin. During soft-start, this capacitor is charged up by a current source and the voltage across the capacitor determines the switch current limit: the larger the capacitor, the slower the ramp of the switch current limit and therefore the longer the soft-start time. The maximum switch current limit is achieved when the voltage connected to the boost converter's feedback pin (FB) reaches its power good threshold (approximately 97 percent of its nominal value).

A 22 nF soft-start capacitor is suitable for most applications.

When the EN pin is pulled low, the soft-start capacitor is discharged.

Frequency Select (FREQ)

The frequency select (FREQ) pin can be used to set the nominal boost converter switching frequency to either 640 kHz (FREQ=low) or 1.2 MHz (FREQ=high). A higher switching frequency improves the load transient response and output voltage ripple; a lower switching frequency usually improves efficiency.

A switching frequency of 1.2 MHz is recommended for most applications unless efficiency is the primary concern.

The FREQ pin features an internal pull-up resistor that ensures the higher switching frequency is used if the pin is left floating.

Compensation (COMP)

The boost converter uses an external compensation network connected to its COMP pin to stabilize its feedback loop. The COMP pin is connected to the output of the boost converter's transconductance error amplifier, and a series resistor and capacitor connected between this pin and AGND is sufficient to achieve good performance in most applications. The capacitor primarily influences low frequency gain and the resistor primarily influences high frequency gain. Lower output voltages require higher loop gain and therefore a larger compensation capacitor.

Good starting values, which will work for most applications running from a 5 V supply voltage, are 47 kΩ and 3.3 nF.

In some applications (e.g. those using electrolytic output capacitors), it may be necessary to include a second compensation capacitor between the COMP pin and AGND. This has the effect of adding an additional pole in the feedback loop's frequency response, which can be used to cancel the zero introduced by the electrolytic output capacitor's ESR. It is recommended to include a footprint on the PCB for this optional capacitor, even if it is not used initially.

Overvoltage Protection (Boost Converter)

The boost converter contains an overvoltage protection (OVP) feature that limits its output voltage to a safe maximum if the FB pin is floating or shorted to ground. Overvoltage conditions are detected when the voltage applied to the AVDD pin (V_{AVDD}) exceeds the overvoltage threshold (V_{OVP}). As soon as this happens, the boost converter switch is turned off. It remains off until V_{AVDD} falls below V_{OVP} (minus hysteresis), at which point the boost converter automatically starts switching again.

NOTE

The AVDD pin must be connected to the boost converter output for the overvoltage protection feature to operate correctly.

Short-Circuit and Undervoltage Protection (Boost Converter)

During start-up (i.e., as soon as $V_{IN} > V_{UVLO}$ and EN=high) the GD pin is pulled low and the boost converter's output voltage V_{AVDD} is sensed. If V_{AVDD} does not rise to at least 46% of V_{IN} within 5 ms the GD pin is pulled high for 55 ms before the converter tries to start again. If the short-circuit condition persists after three failed attempts the boost converter stops trying to restart and the GD pin is latched high. Either V_{IN} or EN must be cycled to recover normal operation.

During normal operation (i.e., once the boost converter has reached its power good threshold) a short circuit is detected if the feedback voltage V_{FB} falls below 30% of V_L. If this happens, the boost converter is disabled and the GD pin is latched high. Either V_{IN} or EN must be cycled to recover normal operation.

Undervoltage Lockout Protection (Boost Converter)

During operation, if the output of the boost converter falls below its power good threshold for longer than 55ms, the TPS65149 will detect an undervoltage condition and turn itself off. V_{IN} or EN must be cycled to recover normal operation.

High Voltage Stress Mode (Boost Converter)

The TPS65149 features a special mode to support High Voltage Stress (HVS) testing during manufacturing. The HVS mode is selected when the HVS pin is high and causes the boost converter output to be regulated to a higher voltage than during normal operation. This is achieved by connecting an additional feedback resistor between the FB and RHVS pins (see Figure 2). When HVS mode is enabled, the RHVS pin is switched to AGND and the R_{HVS} is connected in parallel with R_2.

During HVS mode, the *increase* in boost converter output voltage is given by Equation 6.

$$\Delta V_{AVDD} = 1.24 \times \frac{R_1}{R_3 + R_{HVS}} \quad (6)$$

Where R_{HVS} is the $r_{DS(ON)}$ of the internal MOSFET switch.

The HVS pin features an internal pull-down resistor that ensures the HVS mode is disabled if the pin is left floating.

Gate Driver (GD)

The gate driver (GD) pin can be used to control an external isolation switch. The TPS65149 supports PMOS devices positioned between V_{IN} and the boost converter's inductor (see Figure 35). The GD pin is pulled low by a 10 µA current source when $V_{IN} > V_{UVLO}$ and EN=high and features an internal pull-up resistor to turn off the isolation switch when V_{IN} is removed or EN is low.

If the TPS65149 is used in an application without an isolation switch, the GD pin can be left floating.

NOTE

The threshold voltage of the PMOS isolation switch must be lower than V_{IN} for proper operation.

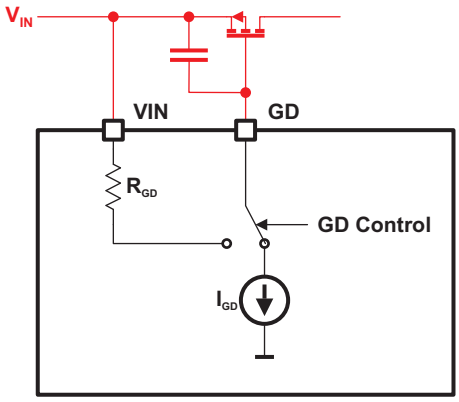


Figure 35. Gate Drive Internal Block Diagram

Positive Charge Pump

Figure 36 shows the internal block diagram of the positive charge pump.

The positive charge pump is driven directly from the boost converter's switch node and then post-regulated by an external PNP transistor. The controller is optimized for transistors having a DC gain (h_{FE}) in the range 100 to 300. The positive charge pump is temperature compensated so that its output voltage decreases at high temperatures (see Figure 16).

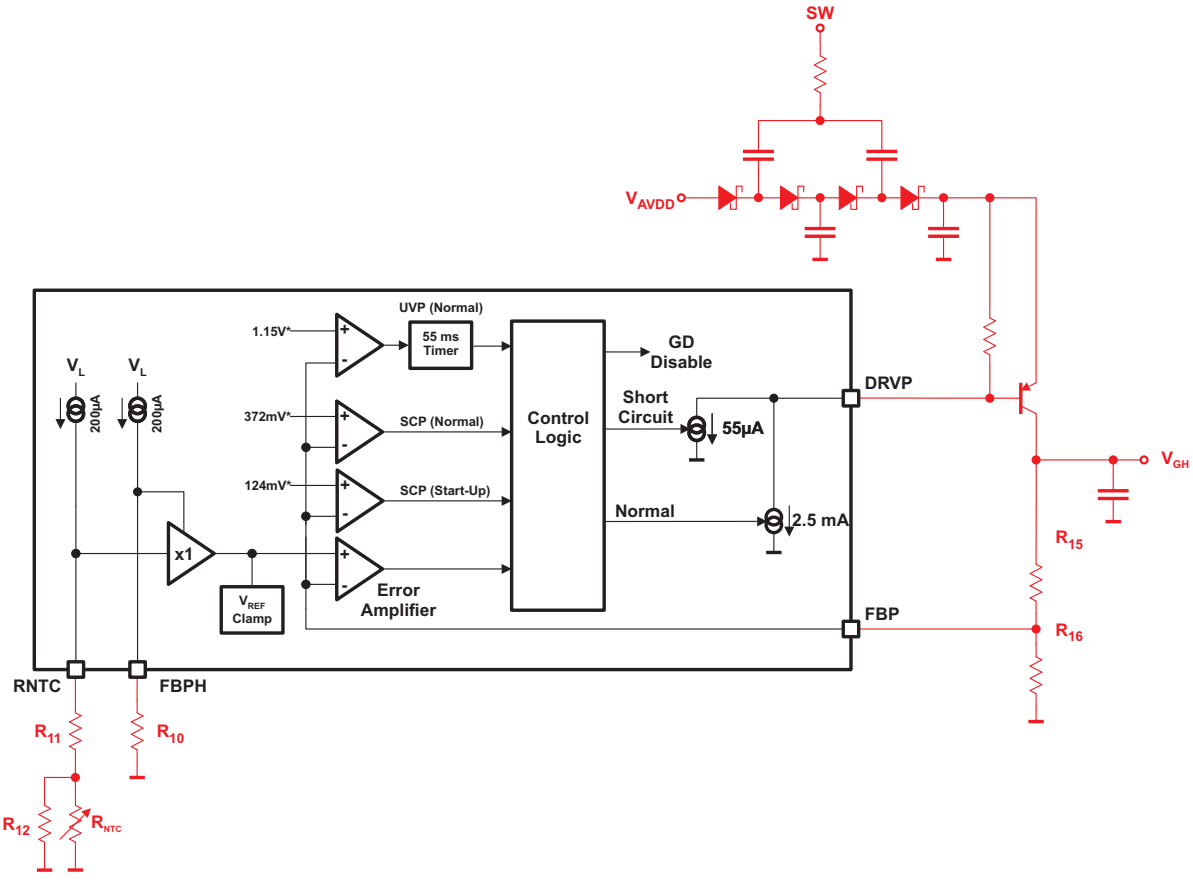


Figure 36. Positive Charge Pump Internal Block Diagram

Setting the Output Voltage (Positive Charge Pump)

The positive charge pump in the TPS65149 is temperature compensated such that its output voltage decreases at high temperatures (see Figure 37). For a detailed description about how to set the output voltage see Temperature Compensation section below.

A current of the order of 1 mA through the feedback resistor network ensures good accuracy and increases the circuit's immunity to noise. It also ensures a minimum load on the charge pump, which reduces output voltage ripple under no-load conditions. A good approach is to assume a value of about 1.2 k for the lower resistor (R_{16}) and then select the upper resistor (R_{15}) to set the desired output voltage.

Note that the maximum voltage in an application is determined by the boost converter's output voltage and the voltage drop across the diodes and PNP transistor. For a typical application in which the positive charge pump is configured as a voltage doubler, the maximum output voltage is given by Equation 7.

$$V_{GH(MAX)} = (2 \times V_{AVDD}) - (2 \times V_F) - V_{CE} \quad (7)$$

Where V_{AVDD} is the output voltage of the boost converter, V_F is the forward voltage of each diode and V_{CE} is the collector-emitter voltage of the PNP transistor (recommended to be at least 1 V, to avoid transistor saturation).

Selecting the PNP Transistor (Positive Charge Pump)

The PNP transistor used to regulate V_{GH} should have a DC gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump's output current. The transistor should also be able to withstand voltages up to V_{GH} across its collector-emitter junction (V_{CE}).

The power dissipated in the transistor is given by Equation 8. The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design.

$$P_Q = \left[(2 \times V_{AVDD}) - (2 \times V_F) - V_{GH}\right] \times I_{GH} \quad (8)$$

Where I_{GH} is the *mean* (not RMS) output current drawn from the charge pump.

A pull-up resistor is also required between the transistor's base and emitter. The value of this resistor is not critical, but it should be large enough not to divert significant current away from the base of the transistor. A value of 100 kΩ is suitable for most applications.

Selecting the Diodes (Positive Charge Pump)

Small-signal diodes can be used for most low current applications (<50 mA) and higher rated diodes for higher power applications. The average current through the diode is equal to the output current, so that the power dissipated in the diode is given by Equation 9.

$$P_D = I_{GH} \times V_F \quad (9)$$

The peak current through the diode occurs during start-up and for a few cycles may be as high as a few amps. However, this condition typically lasts for <1 ms and can be tolerated by many diodes whose repetitive current rating is much lower. The diodes' reverse voltage rating should be equal to two times V_{AVDD}.

Table 3. Positive Charge Pump Diode Selection

PART NUMBER	I_{AVG}	I_{PK}	V_R	V_F	COMPONENT SUPPLIER
BAV99W	150 mA	1 A for 1 ms	75 V	1 V at 50 mA	NXP
BAT54S	200 mA	600 mA for 1s	30 V	0.8 V at 100 mA	Fairchild Semiconductor
MBR0540	500 mA	5.5 A for 8 ms	40 V	0.51 at 500 mA	Fairchild Semiconductor

Selecting the Capacitors (Positive Charge Pump)

For lowest output voltage ripple, low-ESR ceramic capacitors are recommended. The actual value is not critical and values in the range 1 µF to 10 µF are suitable for most applications. Larger capacitors provide better performance in applications where large load transient currents are present.

A flying capacitor in the range 100 nF to 1 µF is suitable for most applications. Larger values experience a smaller voltage drop by the end of each switching cycle, and allow higher output voltages and/or currents to be achieved. Smaller values tend to be physically smaller and a bit cheaper. For best performance, it is recommended to include a resistor of a few ohms (2 Ω is a good value to start with) in series with the flying capacitor to limit peak currents occurring at the instant of switching.

Temperature Compensation (Positive Charge Pump)

The output voltage (V_{GH}) of the positive charge pump controller is defined by two voltages and two temperatures, as illustrated in Figure 37. The temperature compensation scheme is optimized for use with 10 kΩ NTC thermistors.

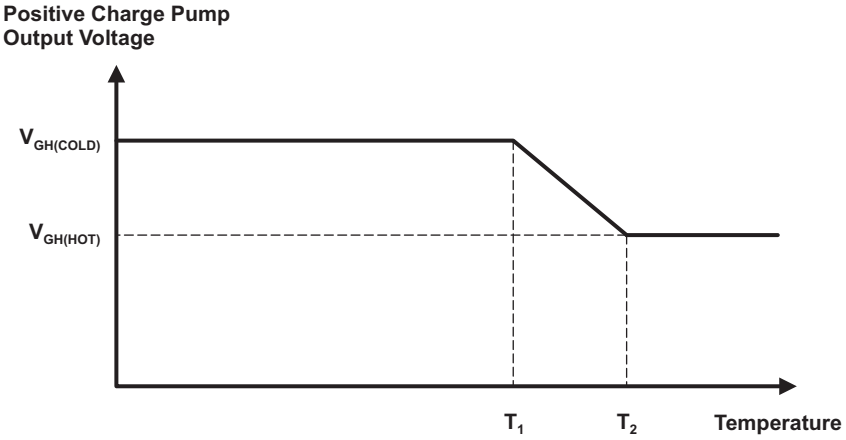


Figure 37. Positive Charge Pump Temperature Compensation

The error amplifier's non-inverting input, which is the reference voltage for V_{GH}, is derived from the FBPH and RNTC pins. A higher reference voltage generates a higher V_{GH}.

$V_{GH(COLD)}$ is determined by the resistor connected to the FBPH and FBP pins:

$$V_{GH(COLD)} = I_{FBPH} \times R_{10} \times \left(1 + \frac{R_{15}}{R_{16}}\right) \quad (10)$$

$V_{GH(HOT)}$ is set by an internal clamping circuit and the resistor divider connected to the FBP pin:

$$V_{GH(HOT)} = V_{REF} \times \left(1 + \frac{R_{15}}{R_{16}}\right) \quad (11)$$

The NTC network connected to the RNTC pin defines the temperatures T_1 and T_2.

Temperature compensation can be disabled by connecting a 10 kΩ resistor between the FBPH pin and AGND and by tying the RNTC pin directly to AGND, in which case Equation 11 should be used to calculate V_{GH}.

Suppose a circuit with the following characteristics is required:

Example

A Microsoft Excel spreadsheet is available that allows easy calculation of temperature compensation components and eliminates the need for the following expressions to be calculated manually. Contact the factory to receive a free copy.

Suppose a circuit with the following characteristics is required:

T_1 = 40°C
T_2 = 60°C
$V_{GH(COLD)}$ = 28 V
$V_{GH(HOT)}$ = 20 V

1. The first step is to calculate the resistance of the NTC at temperatures T_1 and T_2
   At temperature T_1, $R_{NTC(T1)}$ = 5302 Ω
   At temperature T_2, $R_{NTC(T2)}$ = 2486 Ω

2. The next step is to calculate the feedback resistors R_{15} and R_{16} as follows:

$$\frac{R_{15}}{R_{16}} = \frac{V_{GH(HOT)}}{V_{REF}} - 1$$

$$\frac{R_{15}}{R_{16}} = \frac{20V}{1.24V} - 1 = 15.13 \text{ V} \quad (12)$$

   Suitable standard values from the E96 series would be R_{15} = 19.6 kΩ and R_{16} = 1.3 kΩ. With these values, the current through the feedback divider is of the order of 1mA and the nominal output voltage at high temperatures is:

$$V_{GH(HOT)} = V_{REF} \times \left(\frac{R_{15}}{R_{16}} + 1 \right)$$

$$V_{GH(HOT)} = 1.24 \text{ V} \times \left(\frac{19.6 \text{ k}\Omega}{1.3 \text{ k}\Omega} + 1 \right) = 19.94 \text{ V} \quad (13)$$

3. Now calculate V_{FBPH} as follows:

$$V_{FBPH} = V_{GH(HOT)} \times \left(\frac{R_{16}}{R_{15} + R_{16}} \right)$$

$$V_{FBPH} = 28 \text{ V} \times \left(\frac{1.3 \text{ k}\Omega}{19.6 \text{ k}\Omega + 1.3 \text{ k}\Omega} \right) = 1.742 \text{ V} \quad (14)$$

   The value of R_{10} required to generate V_{FBPH} can now be calculated, as follows:

$$R_{10} = \frac{V_{FBPH}}{I_{FBPH}}$$

$$R_{10} = \frac{1.742 \text{ V}}{200 \text{ µA}} = 8.71 \text{ k}\Omega \quad (15)$$

Two 17.4 kΩ resistors in parallel would be suitable for R_{10}, giving an output voltage at low temperatures given by:

$$V_{GH(COLD)} = I_{FBPH} \times R_{10} \times \left(\frac{R_{15}}{R_{16}} + 1 \right)$$

$$V_{GH(COLD)} = 200\ \mu A \times \frac{17.4\ k\Omega}{2} \times \left(\frac{19.6\ k\Omega}{1.3\ k\Omega} + 1 \right) = 28.0\ V \quad (16)$$

The value of R_{12} can be calculated by solving a standard quadratic equation:

$$R_{12} = \frac{-b \pm \sqrt{b^2 - 4 \times a \times c}}{2 \times a} \quad (17)$$

Where:

$$a = \frac{I_{SET}}{V_{FBPH} - V_L} \times \left(R_{NTC(T1)} - R_{NTC(T2)} \right) - 1$$

$$a = \frac{200\ \mu A}{1.74\ V - 1.24\ V} \times \left(5.30\ k\Omega - 2.49\ k\Omega \right) - 1 = 0.124$$

$$b = R_{T1} + R_{T2}$$

$$b = 5.30\ k\Omega + 2.49\ k\Omega = 7.79\ k\Omega$$

$$c = R_{T1} \times R_{T2}$$

$$c = 5.30\ k\Omega \times 2.49\ k\Omega = 13.2 \times 10^6\ \Omega^2$$

Using the coefficients a, b, and c we can solve for R_{12}:

$$R_{12} = \frac{7.79\ k\Omega + \sqrt{7.79\ k\Omega^2 + 4 \times 0.124 \times 13.2 \times 10^6 \Omega^2}}{2 \times 0.124}$$

$$R_{12} = 64.5\ k\Omega$$

A standard value of 64.9 kΩ can be used for R_{12}.

4. The final step is to calculate the value of R_{11} using Equation 11.

$$R_{11} = \frac{V_{REF}}{I_{RNTC}} - \frac{R_{T2} \times R_{12}}{R_{T2} + R_{12}}$$

$$R_{11} = \frac{1.24\ V}{200\ \mu A} - \frac{2.49\ k\Omega \times 64.9\ k\Omega}{2.49\ k\Omega + 64.9\ k\Omega} = 3.8\ k\Omega \quad (18)$$

A standard value of 3.83 kΩ can be used for R_{12}.

Figure 38 shows the temperature dependence of V_{GH} resulting from the above calculated values.

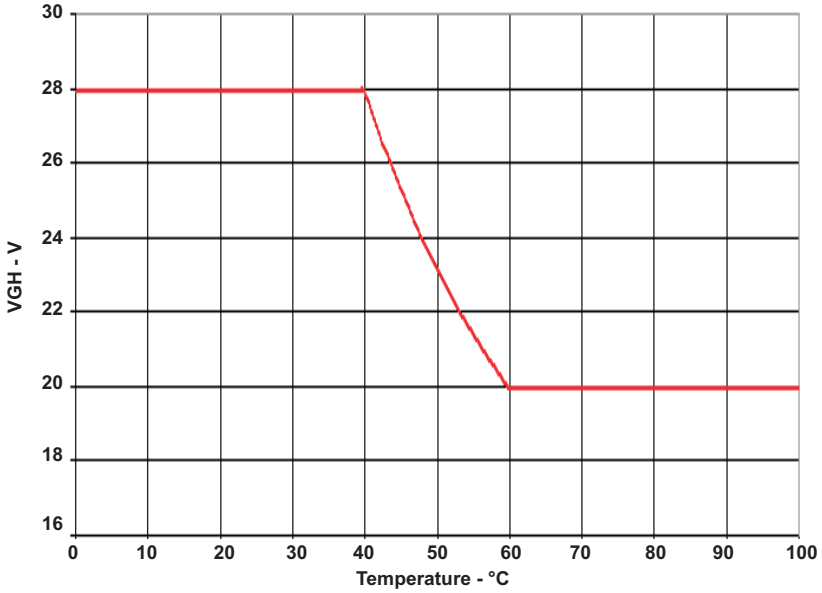


Figure 38. Temperature Compensated V_{GH}

Short-Circuit Protection (Positive Charge Pump)

During start-up, the positive charge pump limits the current available from V_{GH} until V_{FBP} > 124 mV. If V_{FBP} is still less than 124 mV after 15 ms, the boost converter, and positive and negative charge pumps are disabled and the GD pin latched high. Either V_{IN} or EN must be cycled to recover normal operation.

During normal operation (i.e. once the positive charge pump has reached its power good threshold) short circuits are detected if V_{FBP} falls below 0.34 V (approx. 30% of V_L). If this happens the boost converter and positive and negative charge pumps are disabled and the GD pin latched high. Either V_{IN} or EN must be cycled to recover normal operation.

Undervoltage Protection (Positive Charge Pump)

During operation, if the output of the positive charge pump falls below its power good threshold for longer than 55ms, the TPS65149 will detect an undervoltage condition and turn itself off. V_{IN} or EN must be cycled to recover normal operation.

Negative Charge Pump Controller

The negative charge pump controller uses an external NPN transistor to regulate an external charge pump circuit. The controller is optimized for transistors having a DC gain (h_{FE}) in the range 100 to 300. Regulation of the charge pump's output voltage is achieved by using the external transistor as a controlled current source whose output current depends on the voltage applied to the FBN pin. The higher the transistor's output current, the higher (i.e., more negative) the charge pump's output voltage.

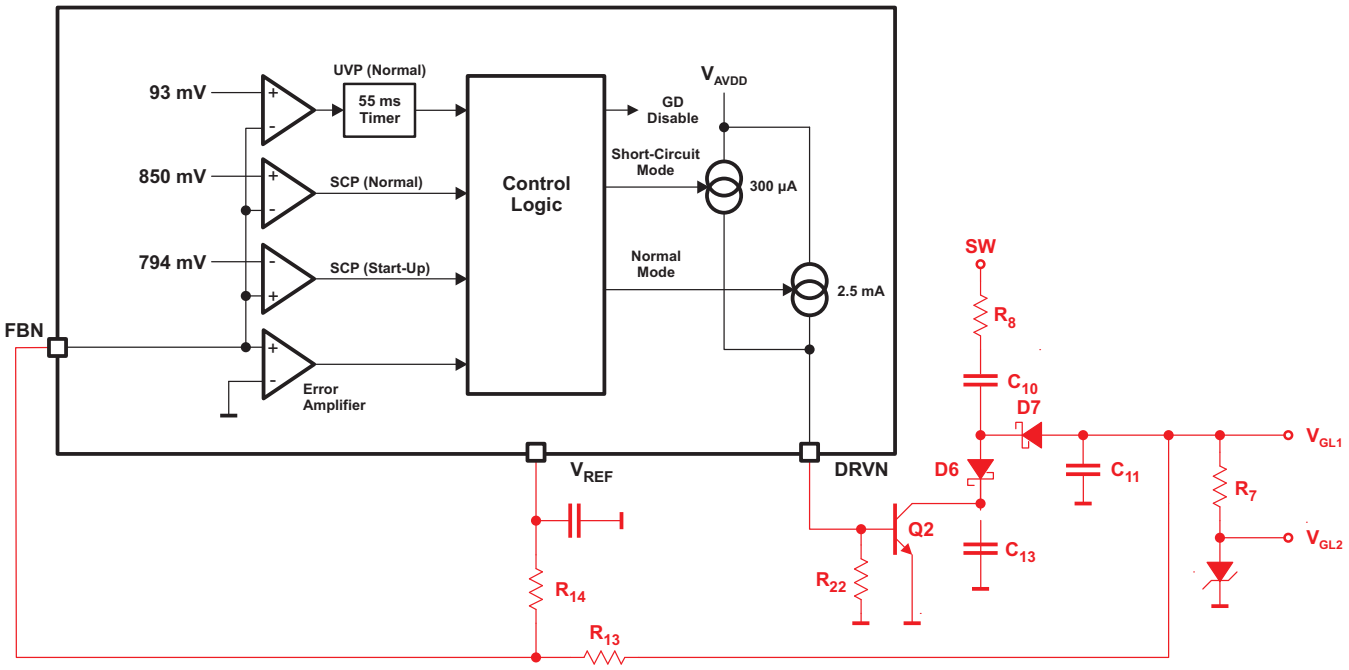


Figure 39. Negative Charge Pump Internal Block Diagram

Setting the Output Voltage (Negative Charge Pump)

The negative charge pump's output voltage is programmed by a resistor divider according to Equation 19.

$$V_{GL1} = -V_{REF} \times \frac{R_{13}}{R_{14}} \tag{19}$$

Rearranging Equation 19, the values of R_{13} and R_{14} can be easily calculated.

$$R_{13} = R_{14} \times \frac{|V_{GL1}|}{V_{REF}} \tag{20}$$

Because of its limited output current capability, it is recommended to keep the current drawn from the VL pin below 250 µA to achieve best accuracy. A good approach is to use a value of at least 5.1 kΩ for the lower resistor (R_{14}) and then select the upper resistor (R_{13}) to set the desired output voltage. If a minimum charge pump load is desired (e.g. to improve regulation at very low load currents), it is best to add an additional resistor between V_{GL1} and GND, rather than reduce the values of R_{13} and R_{14}.

Note that the maximum voltage in an application is determined by the boost converter's output voltage and the voltage drop across the diodes and NPN transistor. For a typical application in which the negative charge pump is configured as a voltage inverter, the maximum (i.e., most negative) output voltage is given by Equation 21.

$$V_{GL1(MAX)} = -V_{AVDD} + (2 \times V_F) + V_{CE} \tag{21}$$

Where V_F is the forward voltage of each diode and V_{CE} is the collector-emitter voltage of the NPN transistor (recommended to be at least 1 V, to avoid transistor saturation).

Selecting the NPN Transistor (Negative Charge Pump)

The NPN transistor used to regulate V_{GL1} should have a DC gain (h_{FE}) of at least 100 when its collector current is equal to the charge pump's output current. The transistor should also be able to withstand voltages up to V_{AVDD} across its collector-emitter (V_{CE}).

The power dissipated in the transistor is given by Equation 22. The transistor must be able to dissipate this power without its junction becoming too hot. Note that the ability to dissipate power depends heavily on adequate PCB thermal design.

$$P_Q = \left[V_{AVDD} - (2 \times V_F) - \left| V_{GL1} \right| \right] \times I_{GL1} \quad (22)$$

Where I_{GL} is the *mean* (not RMS) output current drawn from the charge pump.

Selecting the Diodes (Negative Charge Pump)

Small-signal diodes can be used for most low current applications (<50 mA) and higher rated diodes for higher power applications. The average current through the diode is equal to the output current, so that the power dissipated in the diode is given by Equation 23.

$$P_D = I_{GL1} \times V_F \quad (23)$$

The peak current through the diode occurs during start-up and for a few cycles may be as high as a few amps. However, this condition typically lasts for <1 ms and can be tolerated by many diodes whose repetitive current rating is much lower. The diodes' reverse voltage rating should be equal to at least $2 \times V_{AVDD}$.

Table 4. Negative Charge Pump Diode Selection

PART NUMBER	I_{AVG}	I_{PK}	V_R	V_F	COMPONENT SUPPLIER
BAV99W	150 mA	1 A for 1 ms	75 V	1 V at 50 mA	NXP
BAT54S	200 mA	600 mA for 1 s	30 V	0.8 V at 100 mA	Fairchild Semiconductor
MBR0540	500 mA	5.5 A for 8 ms	40 V	0.51 at 500 mA	Fairchild Semiconductor

Selecting the Capacitors (Negative Charge Pump)

For lowest output voltage ripple, low-ESR ceramic capacitors are recommended. The actual value is not critical and 1 µF to 10 µF is suitable for most applications. Larger capacitors provide better performance in applications where large load transient currents are present.

A flying capacitor in the range 100 nF to 1 µF is suitable for most applications. Larger values experience a smaller voltage drop by the end of each switching cycle, and allow higher output voltages and/or currents to be achieved. Smaller values tend to be physically smaller and a bit cheaper.

A collector capacitor in the range 100 nF to 1 µF is suitable for most applications. Larger values are more suitable for high current applications but can affect stability if they are too big.

Short-Circuit Protection (Negative Charge Pump)

During start-up the negative charge pump limits the current available from V_{GL1} until V_{FBN} is less than 794 mV. If V_{FBN} is still less than 794 mV after ≈20 ms(1), the boost converter, and positive and negative charge pumps are disabled, and the GD pin latched high. Either V_{IN} or EN must be cycled to recover normal operation.

During normal operation (i.e., once the negative charge pump has reached its power good threshold), short circuits are detected if V_{FBN} rises above 850 mV. If this happens, the boost converter, and positive and negative charge pumps are disabled, and the GD pin latched high. Either V_{IN} or EN must be cycled to recover normal operation.

Undervoltage Protection (Negative Charge Pump)

During operation, if the output of the negative charge pump falls below its power good threshold for longer than 55ms, the TPS65149 will detect an undervoltage condition and turn itself off. V_{IN} or EN must be cycled to recover normal operation.

(1) Actually 10ms after the boost converter's power good.

Reset Generator ($\overline{XAO}$)

The TPS65149 generates an open-drain reset signal that can be used to disable the T-CON during power-down. The $\overline{XAO}$ signal is pulled low when $V_{DET} < V_L$ and is high impedance when $V_{DET} > V_L$ (+ hysteresis). The reset generator is not disabled when V_{IN} falls below the UVLO threshold, and continues to function down to very low values of V_{IN}.

Programmable VCOM

The TPS65149 contains a programmable V_{COM} generator (see Figure 40). The output voltage generated (V_{DVRO}) can be adjusted during using the integrated 7-bit DAC, which can be accessed via an I^2C serial interface. The programmable V_{COM} is enabled when $V_{IN} > V_{UVLO}$ and EN = high.

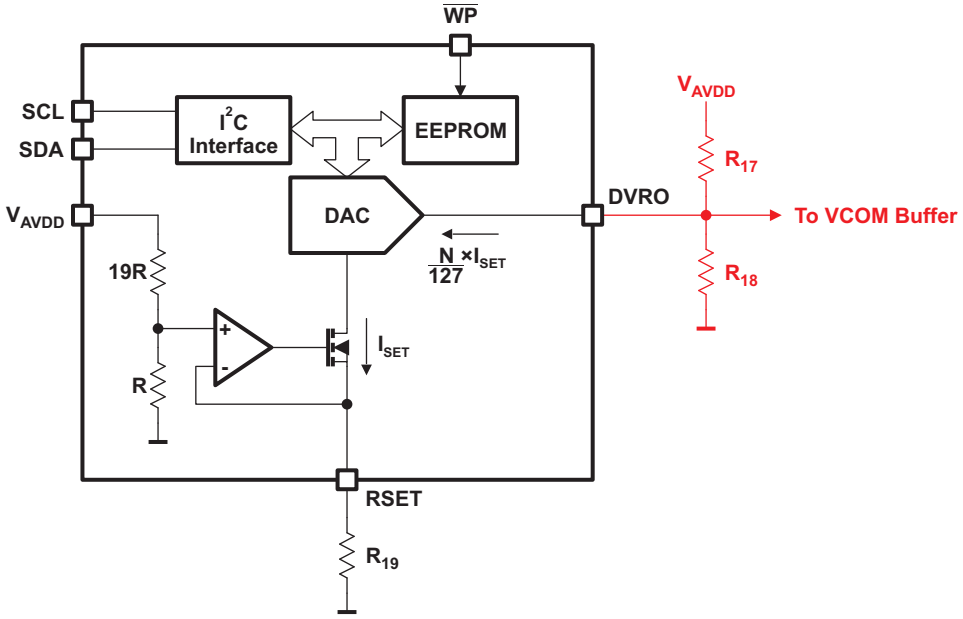


Figure 40. Programmable V_{COM} Buffer Internal Block Diagram

Once the optimum V_{COM} value has been determined, it can be stored in the on-chip EEPROM. The DAC will be programmed with this value every time the TPS65149 is powered up.

NOTE

The factory default DAC setting is 40h, which is the midpoint of the adjustment range.

Programming V_{COM}

The maximum value of V_{COM} occurs when the DAC setting is 0 and is determined by R_{17} and R_{18} connected between V_{AVDD} and GND as follows:

$$V_{COM(MAX)} = \frac{R_{18}}{R_{17} + R_{18}} \times V_{AVDD} \quad (24)$$

The maximum current that can be sunk from the POS pin occurs when the DAC setting is 7Fh and is given by:

$$I_{SET} = \frac{V_{AVDD}}{20 \times R_{19}} \quad (25)$$

The current that will be sunk from the POS pin for a given DAC setting N is given by:

$$I_{POS} = \frac{N}{127} \times I_{SET} \quad (26)$$

where N is a 7-bit integer between 0 and 127 (decimal).

The V_{COM} generated for a given DAC setting N is therefore given by:

$$V_{COM} = V_{AVDD} \times \frac{R_{18}}{R_{17} + R_{18}} \times \left(1 - \frac{N \times R_{17}}{127 \times 20 \times R_{19}}\right) \quad (27)$$

DAC Register (DR)

The DAC Register (DR) contains the current 7-bit setting of the DAC. This register can be written to and read from at any time.

During power-up the contents of the IVR are written into the DR. The contents of the DR are volatile, which means that if they have been changed from the IVR value, they will be lost when power to the TPS65149 is removed.

Initial Value Register (IVR)

The Initial Value Register (IVR) contains the 7-bit setting that is loaded into the DAC during power-up. This register can only be written to when the $\overline{WP}$ pin is high, and cannot be read from directly. The IVR can be read from indirectly by reading the DR immediately after power-up, before any write operations to the DR have been performed.

Write Protect

The TPS65149 features an active low Write Protection pin ($\overline{WP}$) that prevents any changes to the IVR when tied GND. The $\overline{WP}$ pin should be pulled high to allow the desired V_{COM} setting to be stored in the EEPROM, and then tied to GND (to prevent further changes) before the display is finally shipped.

The $\overline{WP}$ pin features is internally pulled down to inhibit write operations if accidentally left floating.

The internal circuitry derives the EEPROM programming voltage from V_{AVDD}. The AVDD pin must therefore be connected to the boost converter output and the EN pin must be high during EEPROM write operations.

I²C Interface

The TPS65149 features an I²C serial interface that allows the contents of the IVR and DR to be read from and written to. The TPS65149 is configured as a slave device that supports 7-bit addressing and whose 7-bit address is 4Fh. Standard and Fast modes of operation are supported.

During normal operation the DAC contains the data last written to the IC. During power-up the contents of the IVR are loaded into the DAC.

Two write operations are possible:

- To the DAC – when the LSB of the data word is "1"
- To the IVR – when the LSB of the data word is "0"

A read operation always reads data from the DR. This data is the same as the IVR if the read operation is performed immediately after a write operation to the DR and the IVR. During a read operation, when the DR and IVR contents are the same the LSB is "0", when they are different, the LSB is "1".

During an EEPROM write operation the TPS65149 ignores all further attempts to access its slave address until the current write operation has finished.

Example – Writing 77h to DR

1. Bus Master sends START condition.
2. Bus Master sends 9Eh (slave address plus low R/$\overline{W}$ bit).
3. TPS65149 acknowledges.
4. Bus Master sends EFh (data to be written plus LSB = "1").
5. TPS65149 acknowledges.
6. Bus Master sends STOP condition

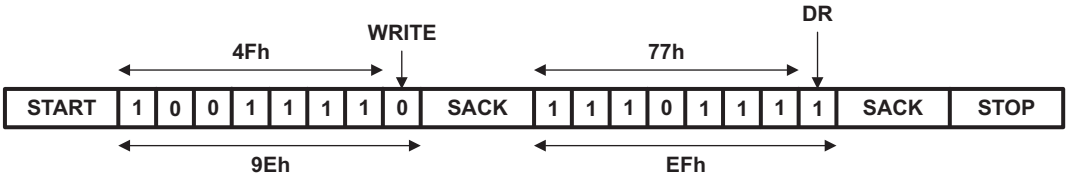


Figure 41. Writing 77h to DAC Register (DR)

Example – Writing 77h to IVR

1. Bus Master sends START condition.
2. Bus Master sends 9Eh (slave address plus low R/$\overline{W}$ bit).
3. TPS65149 acknowledges.
4. Bus Master sends EEh (data to be written plus LSB = "0").
5. TPS65149 acknowledges.
6. Bus Master sends STOP condition

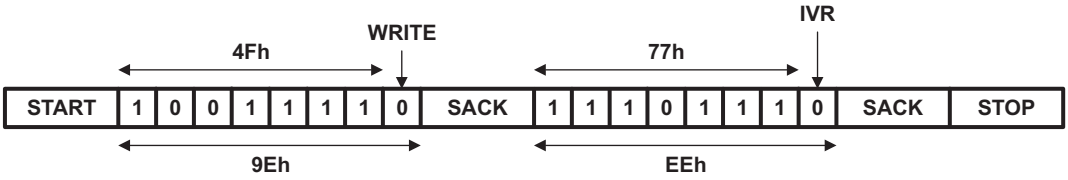


Figure 42. Writing 77h to Initial Value Register (IVR)

Example – Reading from DR when DR and IVR Contents are Identical

1. Bus Master sends START condition.
2. Bus Master sends 9Fh (slave address plus high R/$\overline{W}$ bit).
3. TPS65149 acknowledges.
4. Bus Master sends EEh from DR (LSB = "0").
5. Master does not acknowledge.
6. Bus Master sends STOP condition

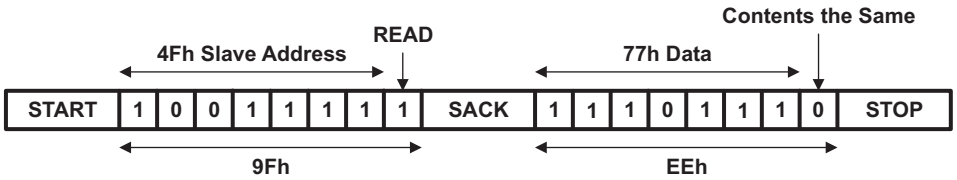


Figure 43. Reading 77h from DAC Register when DR and IVR Contents are the Same

Example – Reading from DR when DR and IVR Contents are Different

1. Bus Master sends START condition.
2. Bus Master sends 9Fh (slave address plus high R/$\overline{W}$ bit).
3. TPS65149 acknowledges.
4. Bus Master sends EFh from DR (LSB = "1").
5. Master does not acknowledge.
6. Bus Master sends STOP condition

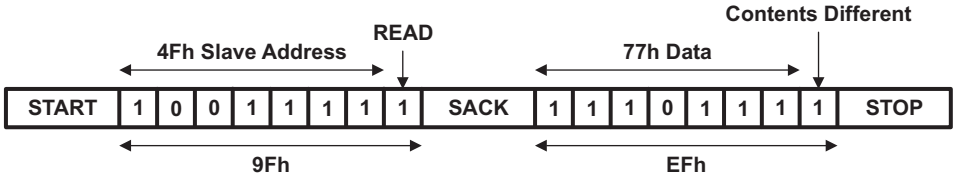


Figure 44. Reading 77h from DAC Register when DR and IVR Contents are Different

Level Shifters

The TPS65149 contains eight level shifter channels (see Figure 45). Each channel features a logic-level input stage and a high-level output stage powered from V_{GH} and V_{GL1}. The output stages are capable of generating high peak currents to drive the capacitive loads typically present in an LCD panel. Because the capacitive load typically connected to the STV and RESET channels is relatively small, the peak current available from these two channels is slightly lower than that available from the CLK channels.

During power-up, the level shifter outputs track V_{GL1}. During power-down, the level shifter outputs track V_{GH}. Power-up and power-down conditions are determined by the V_{DET} threshold of the panel discharge function, which also controls the level shifter channels during power-up and power-down.

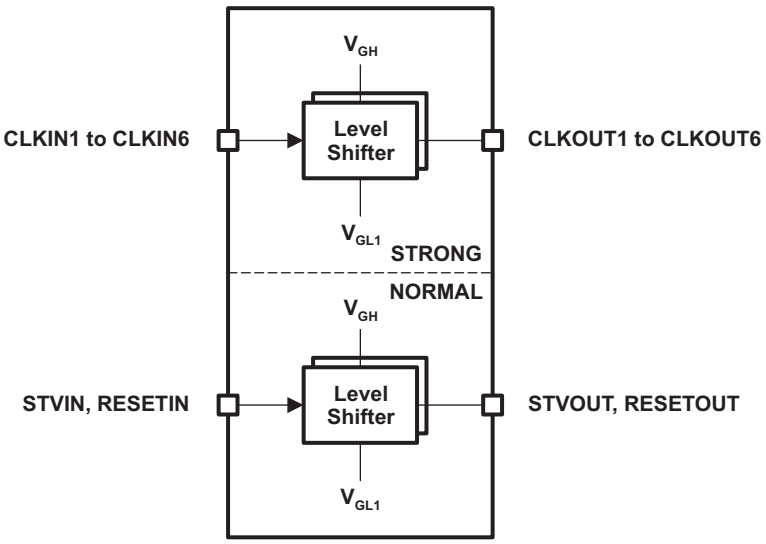


Figure 45. Level Shifter Block Diagram

Panel Discharge

In addition to the eight level shifter channels described above, the TPS65149 contains two level shifter outputs specifically intended for discharging the LCD panel during power-down (see Figure 46). The discharge channels share the input signal connected to the VDET pin, which is compared with V_L. The discharge output stages are identical except that DSCHG1 uses V_{GL1} for its negative supply rail and DSCHG2 uses V_{GL2}. Figure 47 to Figure 50 show the discharge behaviour during power-up and power-down.

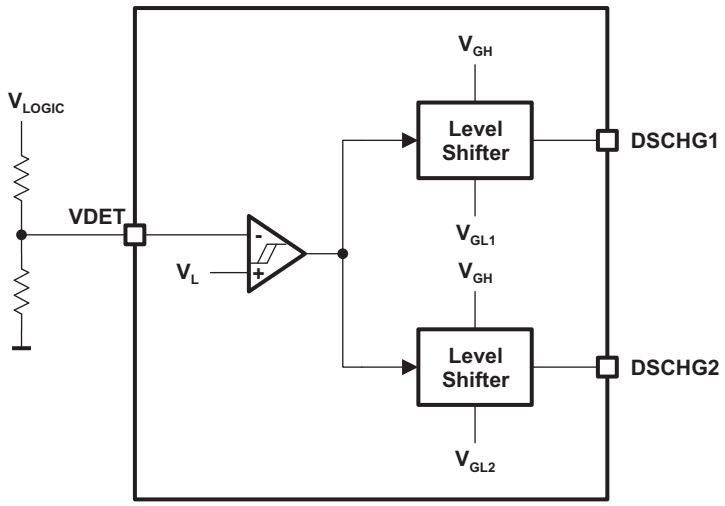


Figure 46. Discharge Internal Bock Diagram

Power Supply Sequencing (Boost, Charge Pumps and V_{COM} Generator)

- When $V_{IN} < V_{UVLO}$, all functions are disabled.(1)
- When $V_{IN} > V_{UVLO}$, all functions are disabled if EN is low.
- When $V_{IN} > V_{UVLO}$ and EN goes high, the boost converter, negative charge pump and V_{COM} generator are enabled first. When the output of the boost converter reaches its power good threshold, the positive charge pump is enabled.
- If EN goes low, all functions are disabled.

Power Supply Sequencing (Level Shifters)

- During power-up, when V_{DET} is below its input threshold, the level shifter outputs track V_{GH}.(2)
- During normal operation, when V_{DET} is above its input threshold, the level shifter outputs follow their inputs.
- During power-down, when V_{DET} falls below its input threshold, the level shifter outputs track V_{GH}.

Power Supply Sequencing (Panel Discharge)

- During power-up, when V_{DET} is below its input threshold, DSCHG1 tracks V_{GL1} and DSCHG2 tracks V_{GL2}.
- During normal operation, when V_{DET} is above its input threshold, DSCHG1 tracks V_{GL1} and DSCHG2 tracks V_{GL2}.
- During power-down, when V_{DET} falls below its input threshold, DSCHG1 and DSCHG2 track V_{GH}.

Power Supply Sequencing (/XAO)

- During power-up, when V_{DET} is still below its input threshold, $\overline{XAO}$ is pulled low.
- During normal operation, when V_{DET} is above its input threshold, $\overline{XAO}$ is high impedance.
- During power-down, when V_{DET} falls below its input threshold, $\overline{XAO}$ is pulled low.

(1) The panel discharge and level shifter discharge functions continue to function for as long as there is sufficient operating voltage on V_{GH}, V_{GL1} and V_{GL2}

(2) The panel discharge and level shifter discharge functions continue to function for as long as there is sufficient operating voltage on V_{GH}, V_{GL1} and V_{GL2}

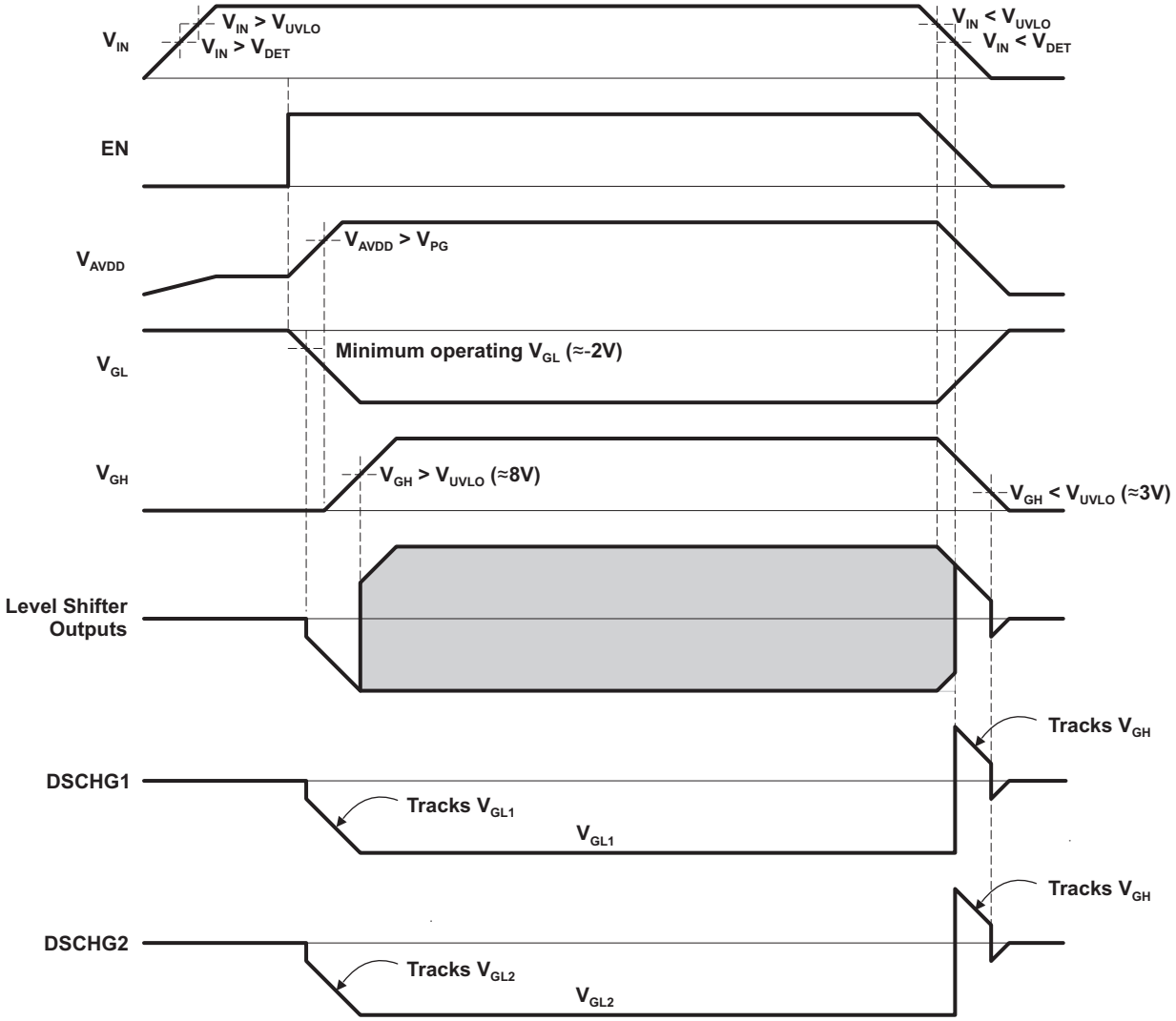


Figure 47. Power Supply Sequencing Using EN Pin, $V_{DET} < V_{UVLO}$

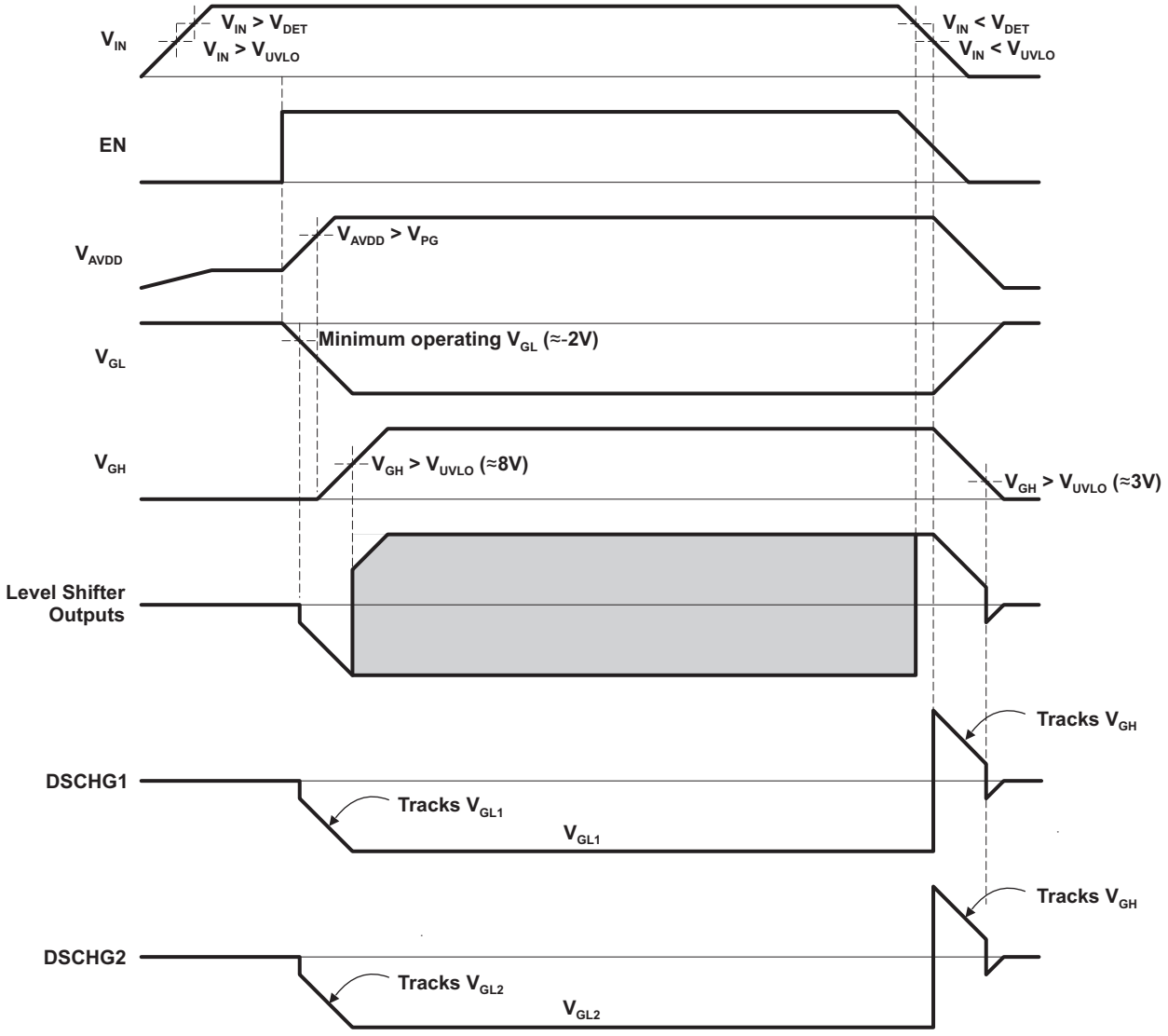


Figure 48. Power Supply Sequencing Using EN Pin, $V_{DET} > V_{UVLO}$

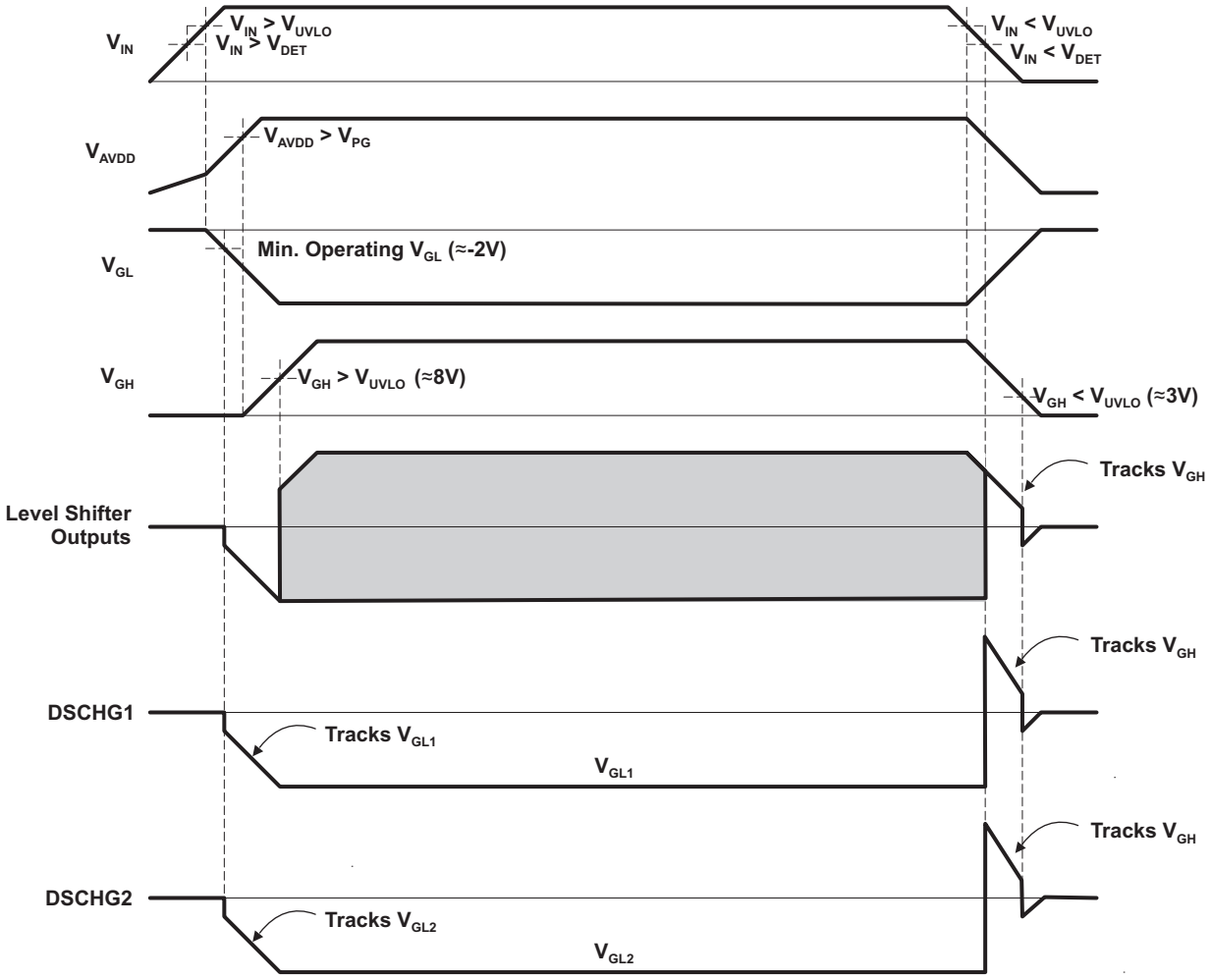


Figure 49. Power Supply Sequencing with EN Pin Tied to V_{IN}, $V_{DET} < V_{UVLO}$

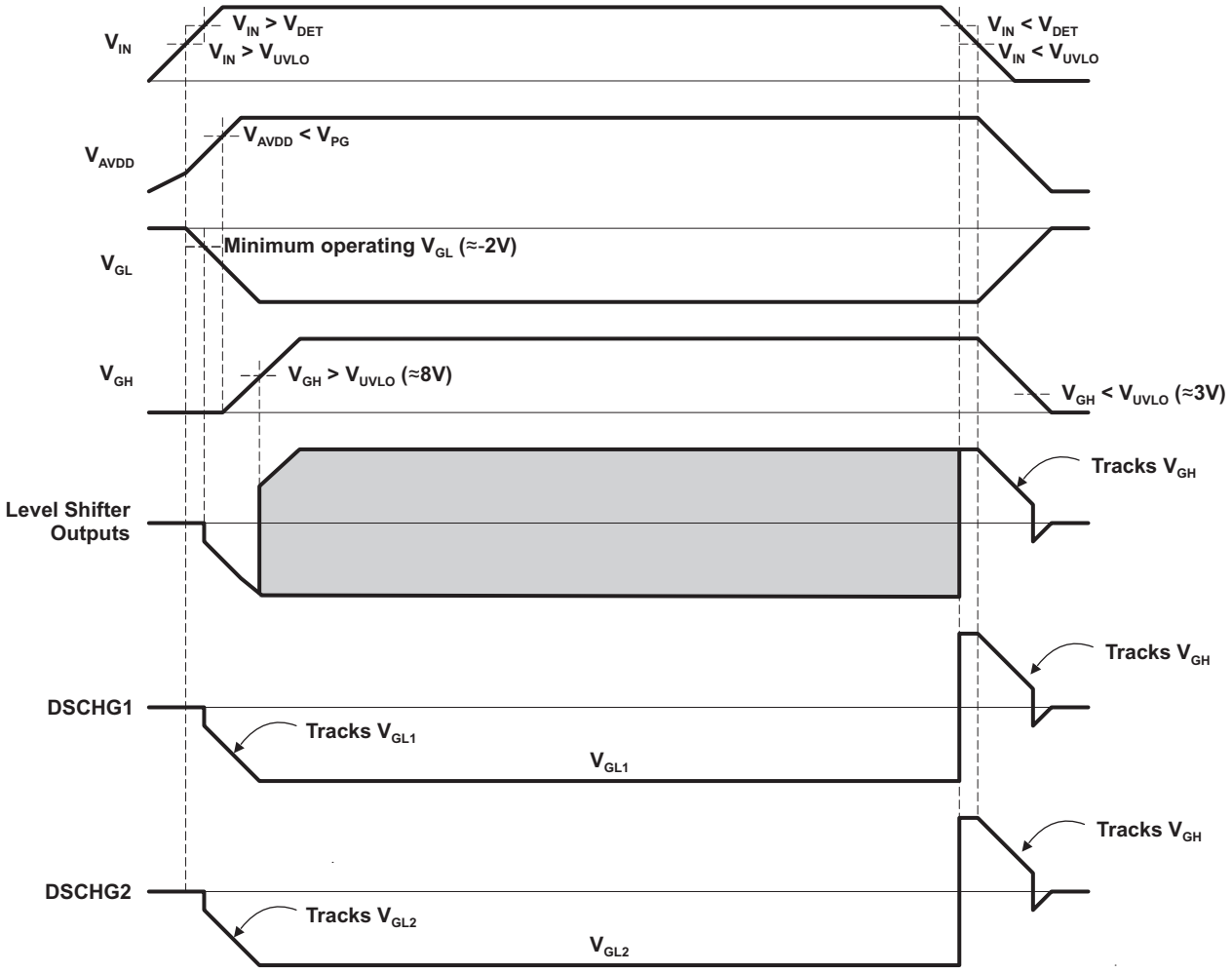


Figure 50. Power Supply Sequencing with EN Pin Tied to V_{IN}, $V_{DET} > V_{UVLO}$

Undervoltage Lockout

The TPS65149 features an undervoltage lockout (UVLO) function that disables the LCD bias functions if the supply voltage (V_{IN}) is below the minimum needed for correct operation (V_{UVLO}).

Thermal Shutdown

A thermal shutdown function automatically disables all LCD bias functions if the device's junction temperature exceeds the safe maximum. The device automatically starts operating again once it has cooled down.

APPLICATION INFORMATION

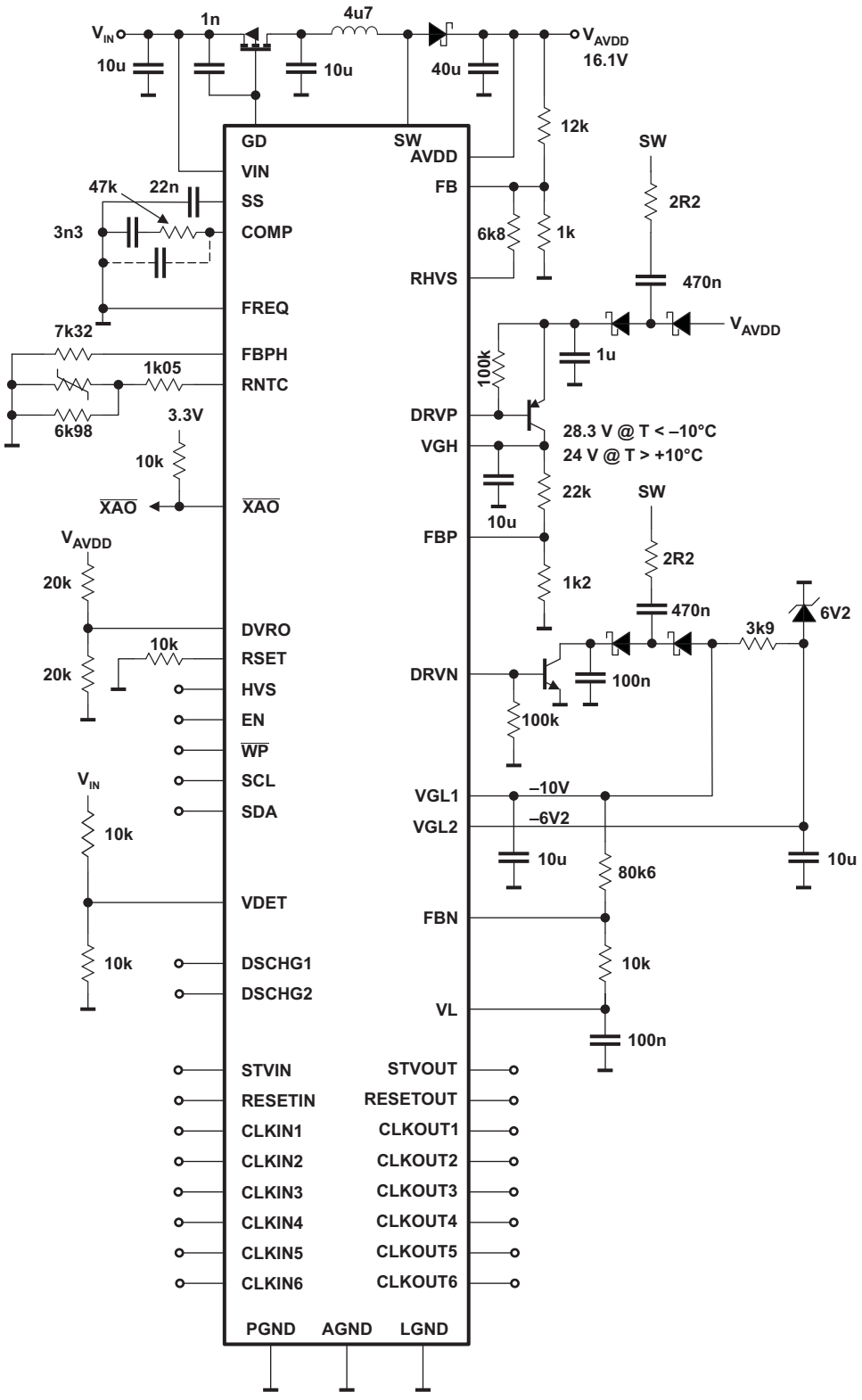


Figure 51. Typical Application Circuit Using Positive Charge Pump in ×2 Configuration

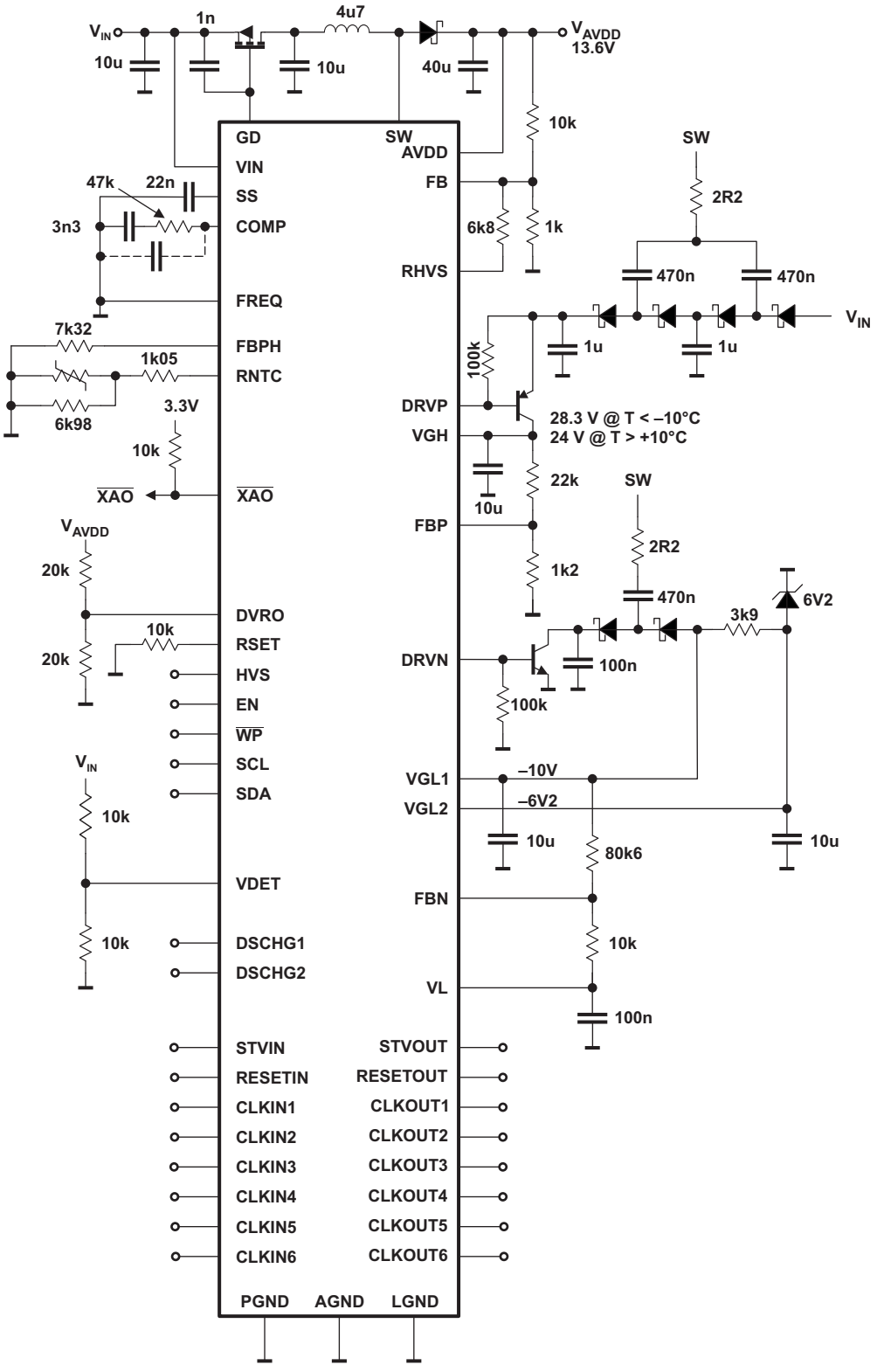


Figure 52. Typical Application Circuit Using Positive Charge Pump in ×2.5 Configuration

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65149RSHR	ACTIVE	VQFN	RSH	56	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65149	Samples
TPS65149RSHT	PREVIEW	VQFN	RSH	56	250	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

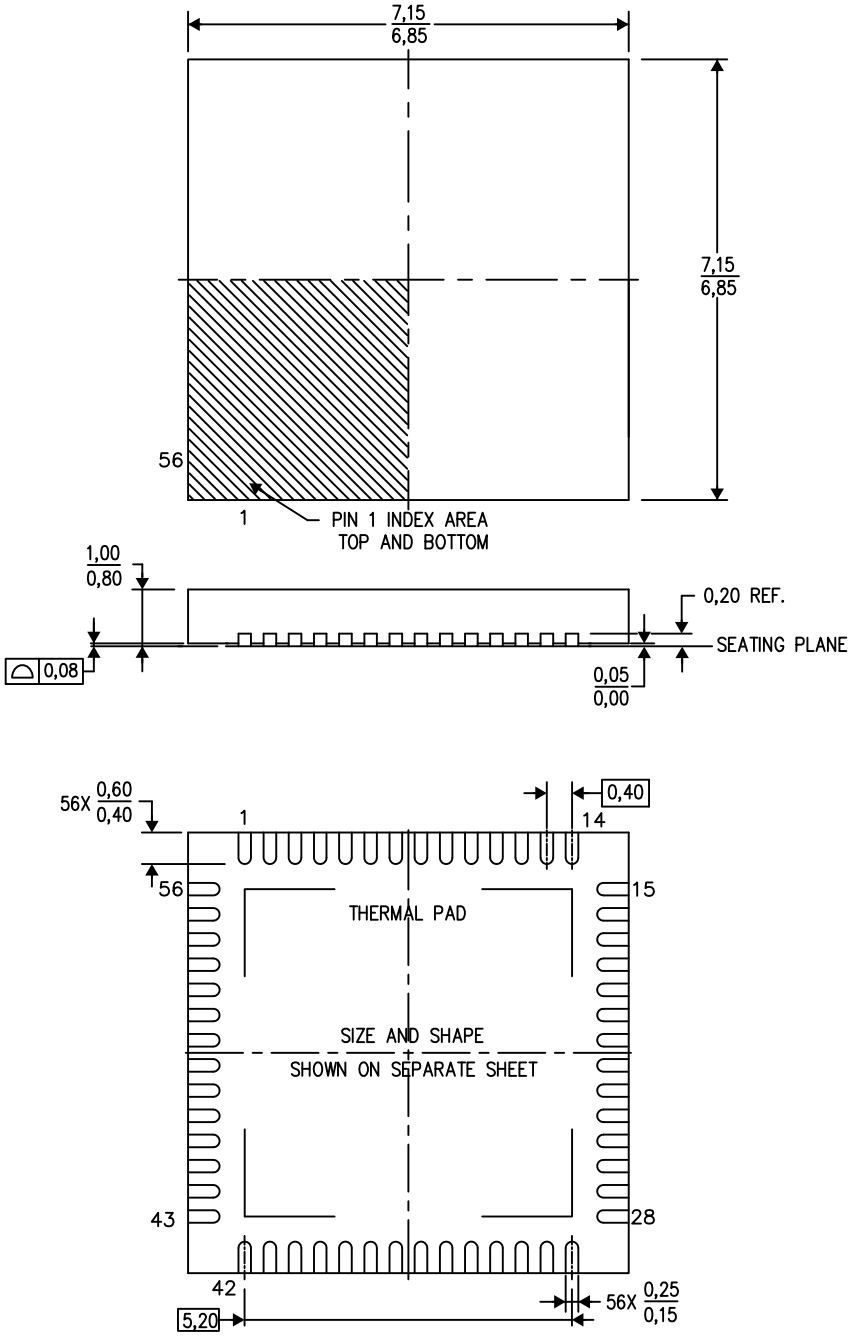
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

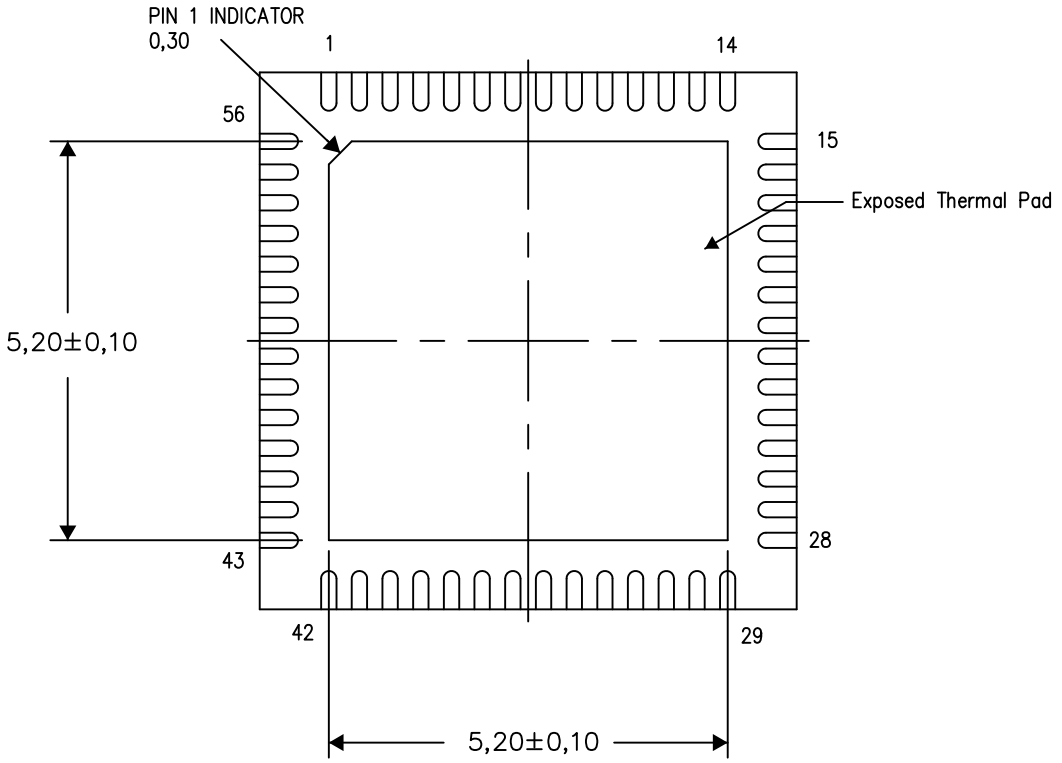
RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



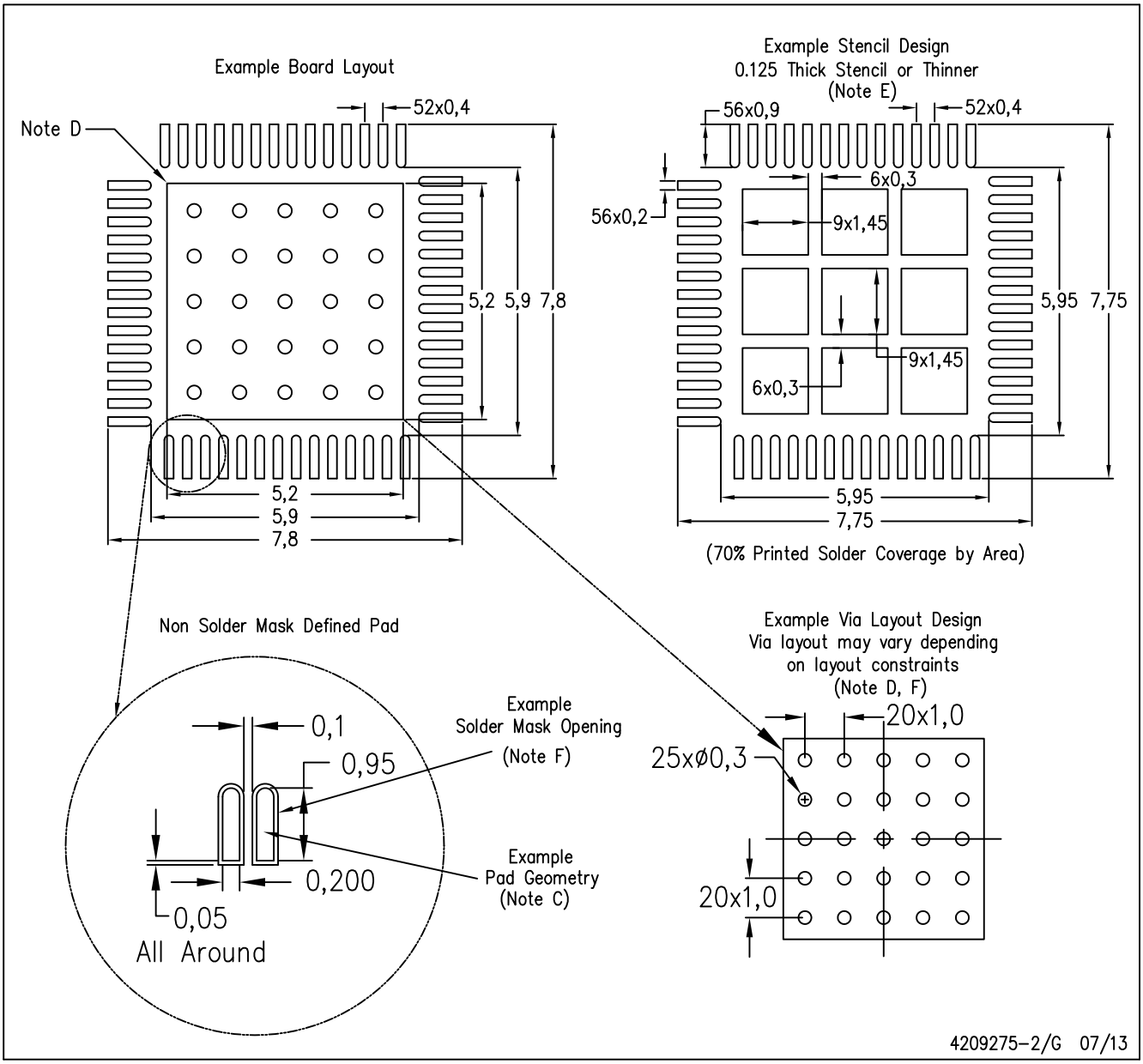
Bottom View

Exposed Thermal Pad Dimensions

4207553–2/I 07/13

NOTE: All linear dimensions are in millimeters

RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65149RSHR	Active	Production	VQFN (RSH) | 56	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65149
TPS65149RSHR.A	Active	Production	VQFN (RSH) | 56	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65149

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

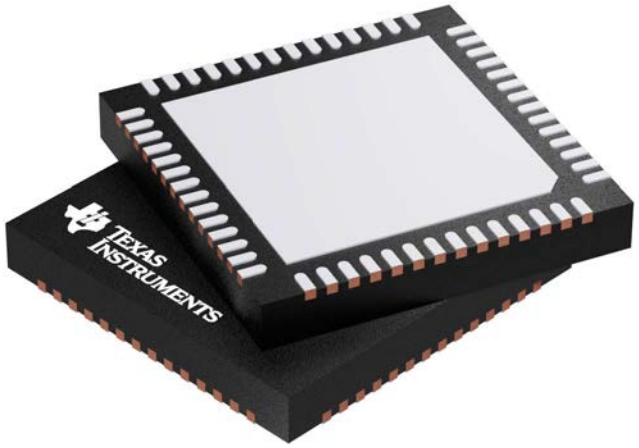
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

RSH 56

VQFN - 1 mm max height

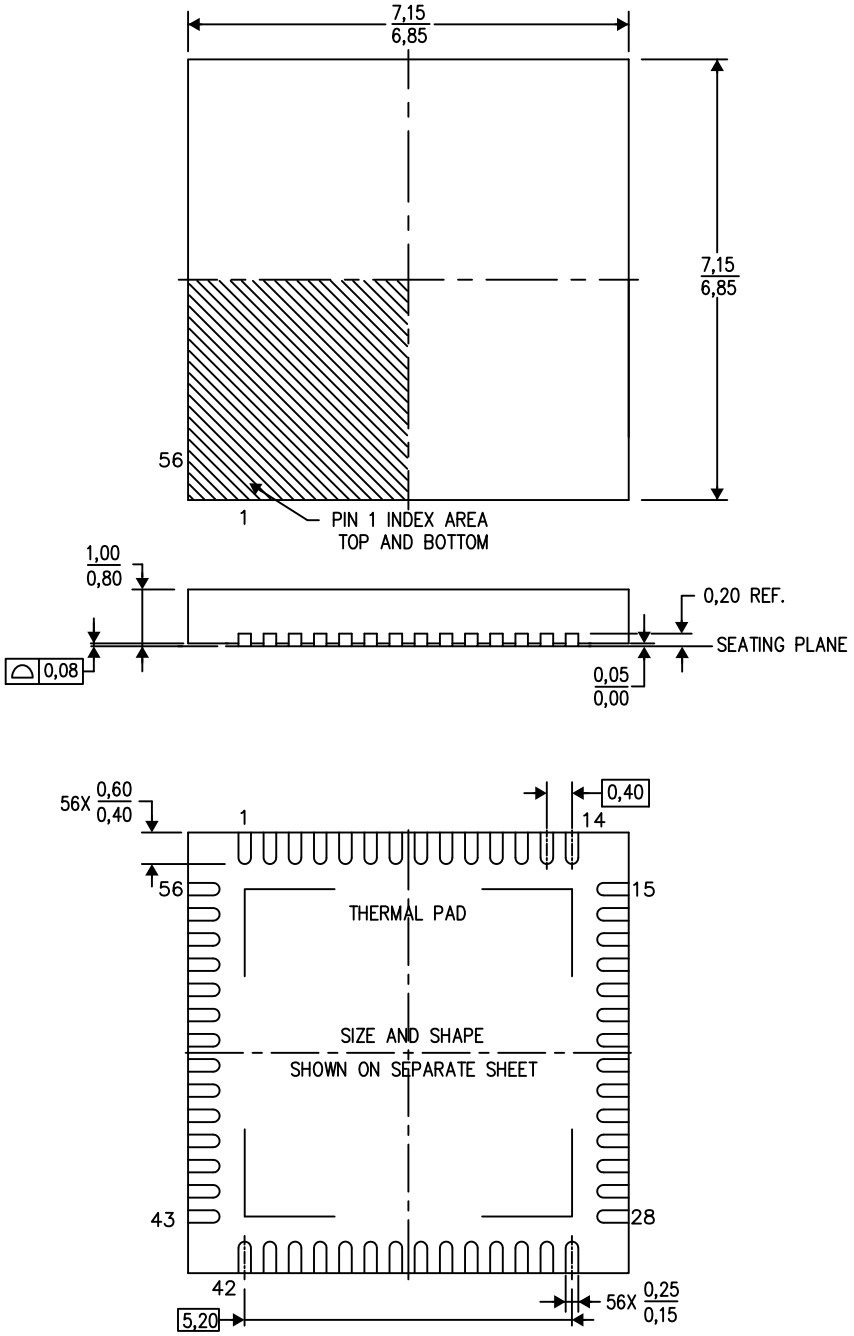
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207513/D

RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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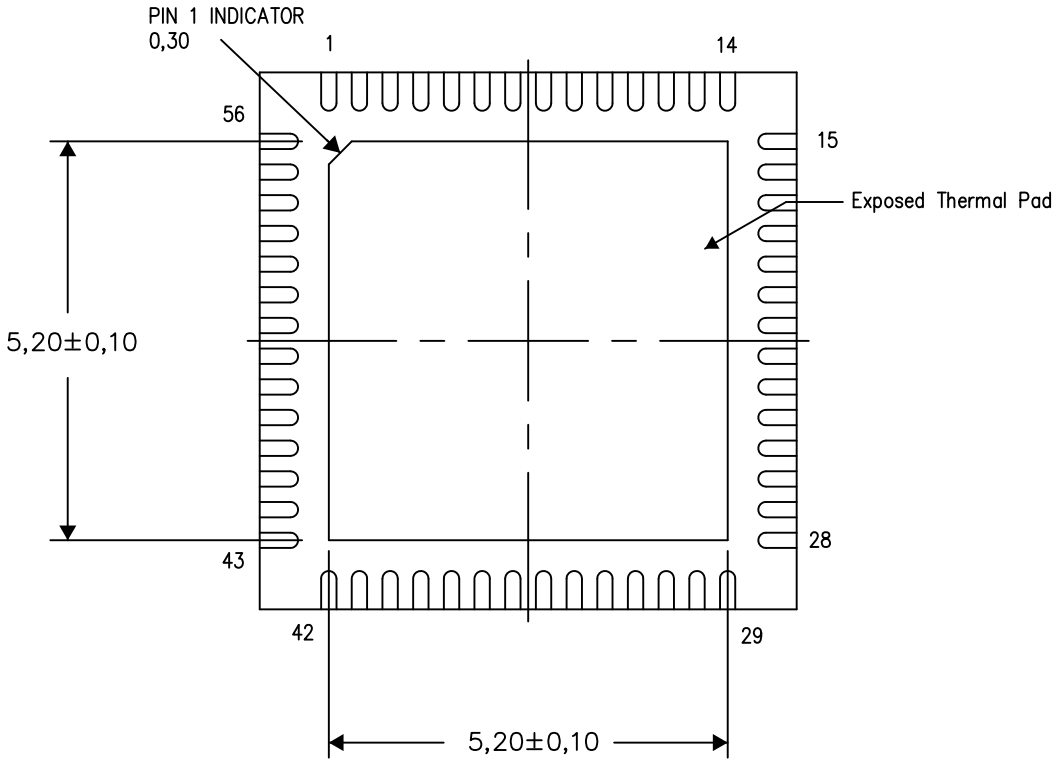
The exposed thermal pad dimensions for this package are shown in the following illustration.



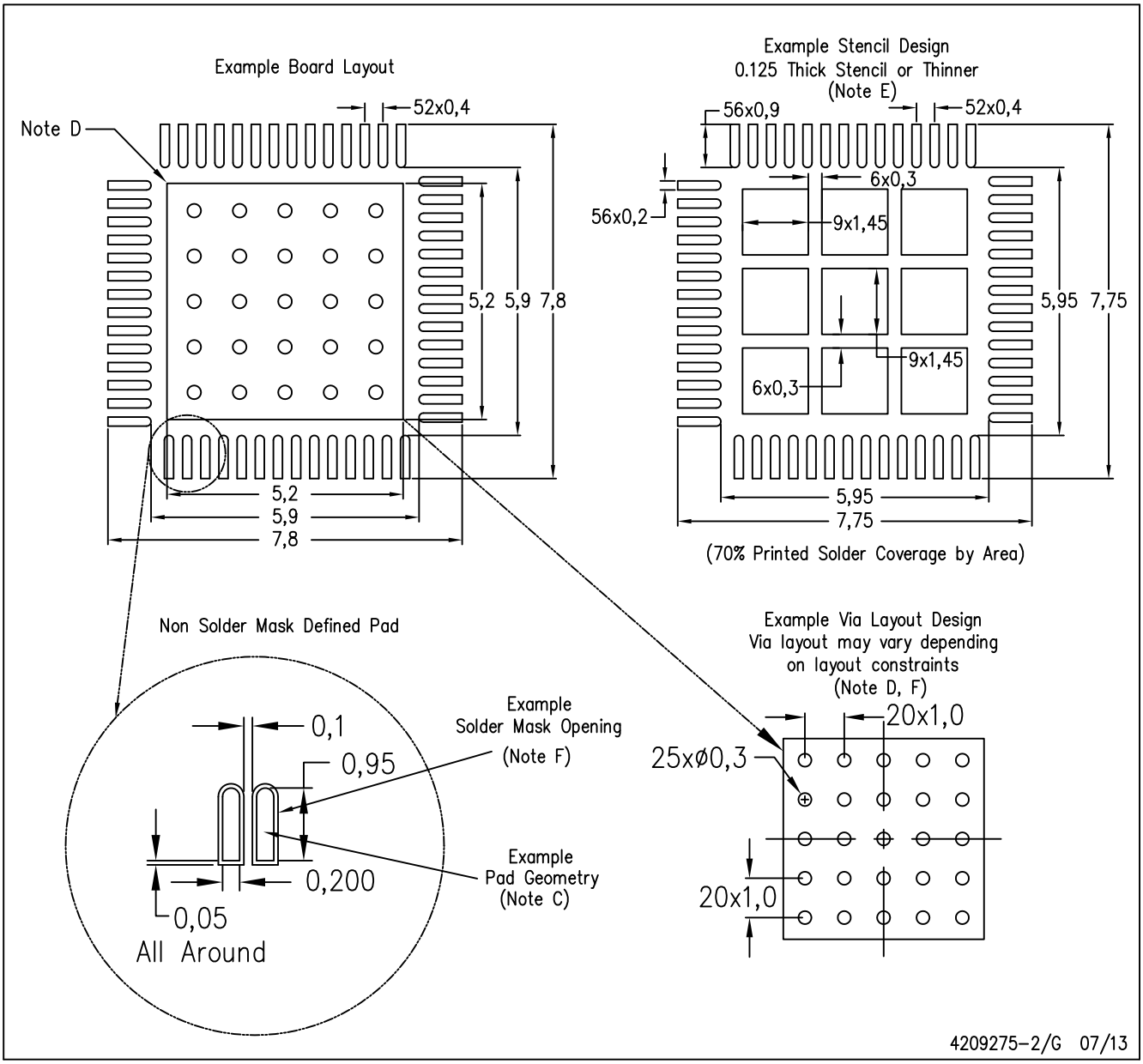
Bottom View

Exposed Thermal Pad Dimensions

4207553–2/I 07/13

NOTE: All linear dimensions are in millimeters

RSH (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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